HACETTEPE
University

VERILOG ASSIGNMENT 1

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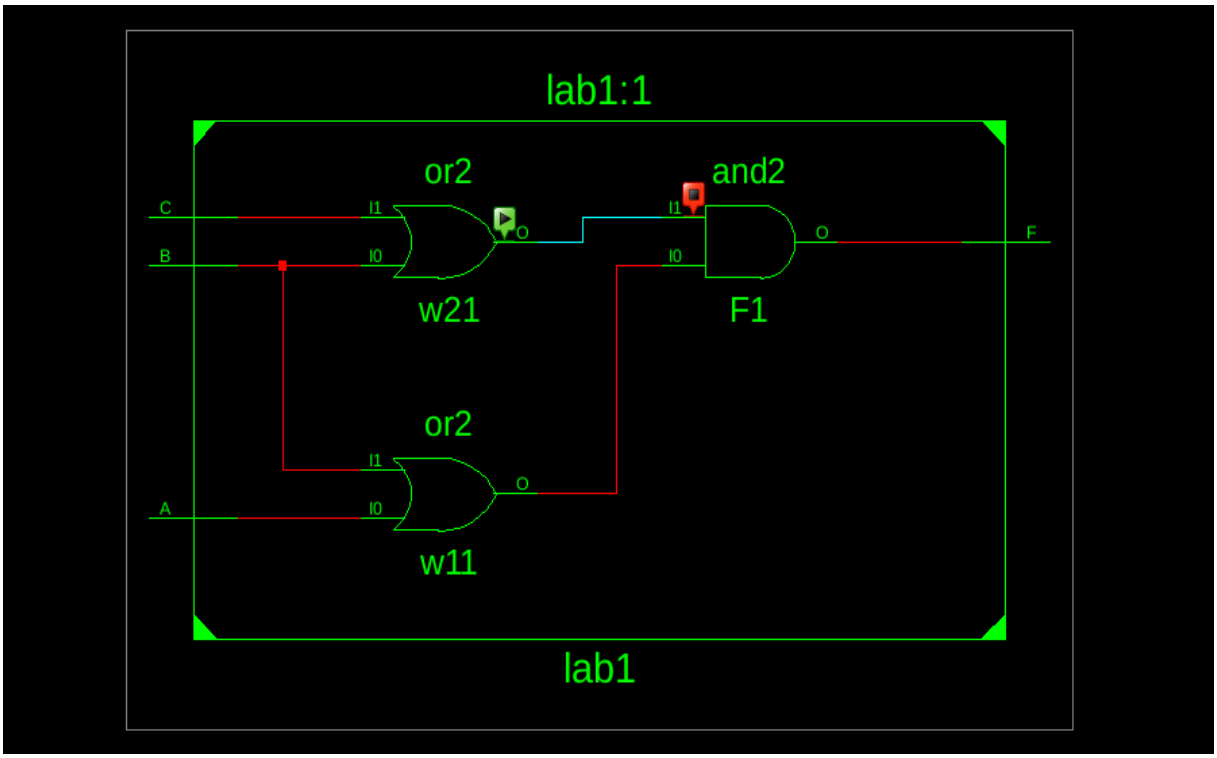
Section : 02
Subject : Implementing Boolean function with Verilog on Xilinx -ISE Design Suite
Function : F = (A+B)(B+C)

Module of İmplementing The Function

```
`timescale 1ns / 1ps
module lab1(
    input A,
    input B,
    input C,
    output F
    );
wire w1,w2;
or(w1,A,B);
or(w2,B,C);
and(F,w1,w2);
endmodule
```

RTL Schematic of Function



Testbench Module Of The Function

```
`timescale 1ns / 1ps
module lab1_testbench;
        // Inputs
        reg A;
        reg B;
        reg C;
        // Outputs
        wire F;
// Instantiate the Unit Under Test (UUT)
        lab1 uut (
                .A(A),
                .B(B),
                .C(C),
                .F(F)
        );
        initial begin
                // Initialize Inputs
                A = 0;
                B = 0;
                C = 0;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 0;
                B = 0;
                C = 1;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 0;
                B = 1;
                C = 0;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 0;
                B = 1;
                C = 1;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 1;
                B = 0;
                C = 0;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 1;
                B = 0;
                C = 1;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 1;
                B = 1;
                C = 0;
        // Wait 100 ns for global reset to finish
                #100;
                // Initialize Inputs
                A = 1;
                B = 1;
                C = 1;
        // Wait 100 ns for global reset to finish
                #100;
                // Add stimulus here
        end
endmodule
```

Waveform from The Simulation