VERILOG EXPERIMENT 3

Name : Muhammed Said
Surname: Kaya
Student Number : 21627428
Section : 02
Subject : Designing 7447

CODE

```
`timescale 1ns / 1ps


module a_result(input A,B,C,D, output a );
        wire A_not , B_not , C_Not , D_Not ;
        not( A_not , A );
        not( B_not , B );
        not( C_not , C );
        not( D_not , D );
        assign a = ( B & D_not ) | ( A_not & B_not & C_not & D );
endmodule


module b_result(input A,B,C,D, output b );
        wire C_not , D_not ;
        not( C_not , C );
        not( D_not , D );
        assign b = ( B & C_not & D ) | ( B & C & D_not );
endmodule


module c_result(input A,B,C,D, output c );
        wire B_not , D_not ;
        not( B_not , B );
        not( D_not , D );
        assign c = ( B_not & C & D_not );
endmodule


module d_result(input A,B,C,D, output d );
        wire B_not , C_not , D_not ;
        not( B_not , B );
        not( C_not , C );
        not( D_not , D );
        assign d = ( B_not & C_not & D ) | ( B & C_not & D_not ) | ( B & C & D );
endmodule


module e_result(input A,B,C,D, output e );
```

```
        wire C_not ;
        not( C_not , C );
        assign e = ( D ) | ( B & C_not );
endmodule

module f_result(input A,B,C,D, output f );
        wire A_not , B_not ;
        not( A_not , A );
        not( B_not , B );
        assign f = ( C & D ) | ( B_not & C ) | ( A_not & B_not & D );
endmodule

module g_result(input A,B,C,D, output g );
        wire A_not ,B_not ,C_not ;
        not(A_not , A );
        not(B_not , B );
        not(C_not , C );
        assign g = ( A_not & B_not & C_not  ) | ( B & C & D );
endmodule
module main( input A,B,C,D, output a,b,c,d,e,f,g);

        a_result a1( A,B,C,D,a );
        b_result b1( A,B,C,D,b );
        c_result c1( A,B,C,D,c );
        d_result d1( A,B,C,D,d );
        e_result e1( A,B,C,D,e );
        f_result f1( A,B,C,D,f );
        g_result g1( A,B,C,D,g );



endmodule
```

TESTBENCH

```
`timescale 1ns / 1ps


module Testbench;

    // Inputs
    reg A;
    reg B;
    reg C;
    reg D;

    // Outputs
    wire a;
    wire b;
    wire c;
    wire d;
    wire e;
    wire f;
    wire g;

    // Instantiate the Unit Under Test (UUT)
    main uut (
        .A(A),
        .B(B),
        .C(C),
        .D(D),
        .a(a),
        .b(b),
```

```
        .c(c),
        .d(d),
        .e(e),
        .f(f),
        .g(g)
    );

    initial begin
        // Initialize Inputs
        A = 0; B = 0; C = 0; D = 0;   #100;
        A = 0; B = 0; C = 0; D = 1;   #100;
        A = 0; B = 0; C = 1; D = 0;   #100;
        A = 0; B = 0; C = 1; D = 1;   #100;
        A = 0; B = 1; C = 0; D = 0;   #100;
        A = 0; B = 1; C = 0; D = 1;   #100;
        A = 0; B = 1; C = 1; D = 0;   #100;
        A = 0; B = 1; C = 1; D = 1;   #100;
        A = 1; B = 0; C = 0; D = 0;   #100;
        A = 1; B = 0; C = 0; D = 1;         #100;

        // Add stimulus here

    end

endmodule
```

Waveform from The Simulation