Department of Electrical, Electronics and Communication Engineering
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Capstone Project – Introduction (PROJ2999), 7th Semester
Academic year: 2025-26

Project Title: EEG Signal Acquisition and alert system for Sleeping disorder patients using RISC-V Processor on FPGA

Guide Name: DR M Arun Kumar

Section:

Section Coordinator Name:

Abstract: **(within 200 words)**

Sleep disorders, including insomnia and sleep apnea, affect millions and impact overall health. Continuous monitoring of brain activity during sleep is essential for early detection and management. This project aims to develop a real-time EEG (Electroencephalogram) signal acquisition and alert system for patients with sleeping disorders, implemented on an FPGA using a 5-stage 32-bit RISC-V processor. The system captures EEG signals via non-invasive electrodes and processes them on the FPGA to identify abnormal patterns. Leveraging the RISC-V processor enables efficient, low-latency computation, while the FPGA architecture allows hardware-level acceleration for signal filtering, feature extraction, and pattern recognition. Upon detecting irregular EEG activity, the system generates alerts to facilitate timely intervention. This project highlights the integration of embedded hardware with biomedical signal processing, aiming to provide a portable, low-cost, and reliable solution for real-time sleep monitoring. The proposed system has the potential to support proactive patient care, improve diagnosis, and enhance the quality of life for individuals affected by sleep disorders.

Team Members (Name & Reg No.):

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Guide's signature & date