Constructor University Bremen

CO-526-B

Electronics Lab

Fall Semester 2023

Lab Experiment 5 – MOSFET

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Introduction

This lab experiment delves into the exploration of Field Effect Transistors (MOSFETs) and their intrinsic characteristics, with a particular focus on their I-V characteristics.

The primary objective is to illustrate the diverse roles MOSFETs play, serving both as amplifiers and switches in electronic circuits. Before delving into the experimental details, it is essential to grasp the fundamental theory behind MOSFETs. A key distinction between FETs and BJTs lies in their applications, with FETs finding prominence in electronic circuits, while BJTs are more common in analog circuits. The regulation mechanism further sets them apart, as FETs are governed by charge, whereas BJTs respond to current or voltage. The analysis of FETs encompasses two main types: junction field-effect transistors (JFETs) and metal oxide semiconductor field-effect transistors (MOSFETs).

Notably, this experiment concentrates on MOSFETs, as they are widely employed in contemporary integrated circuits (ICs), owing to their superior power dissipation characteristics in practical applications. Subsequently, this introduction sets the stage for a detailed exploration of MOSFETs in the upcoming sections, with a specific emphasis on MOSFETs' role as versatile components in electronic circuits.

Prelab - Field Effect Transistor

Problem 1 - Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

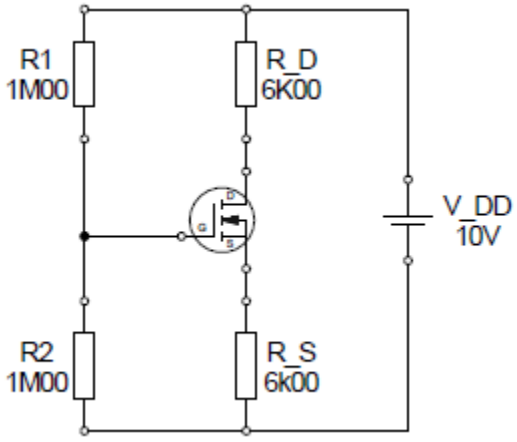
1. **Explain the differences between an enhanced and depletion MOSFET**

In an enhanced MOSFET, the absence of an inherent conduction channel is notable at the outset. This channel is brought into existence by applying a voltage across the gate-source terminals that surpasses the threshold voltage. Consequently, the channel in this context is referred to as an induced channel. In contrast, a depletion MOSFET takes a different approach, establishing a channel permanently during the MOSFET's construction through the utilization of doping techniques.

2. **Explain the differences between an NMOS and PMOS transistor**

In PMOS, the source and drain terminals are made from P-type semiconductor material, while in NMOS, the source and drain are composed of N-type semiconductors. Consequently, the current flowing through the PMOS channel is characterized by hole flow, with holes serving as the majority carriers. In contrast, the current in the NMOS channel involves electron flow, where electrons act as the majority carriers.

Problem 2 - MOSFET as Amplifier



It is assumed that the transistor operates in saturation, so that the drain source current can be described by:

$$I_{DS} = \mu_n C_G \frac{W}{2L}(V_{GS} - V_{th})^2 = k * (V_{GS} - V_{th})^2$$

The prefactor k is given by k = 0.5 mA/V^2, V_{th} = 1 V

1. **Determine the gate-source and drain-source voltage and the drain current for the MOSFET amplifier.**

$V_{R2} = \frac{R_2}{R_1+R_2} V_{DD} = 5V$

$V_{RS} = V_{R2} - V_{GS}$

$I_{DS} = 0.5(V_{GS} - 1)^2 = \frac{V_{RS}}{R_S} = \frac{5-V_{GS}}{6000}$

$V_{GS} = 2V$ (we ignore the negative result)

$V_{DS} = V_{DD} - V_{RS} - V_{RD} = 10 - 3 - 3 = 4V$

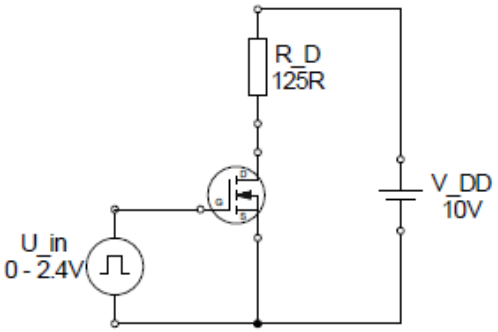
2. **Show that the MOSFET indeed operates in the saturation region.**

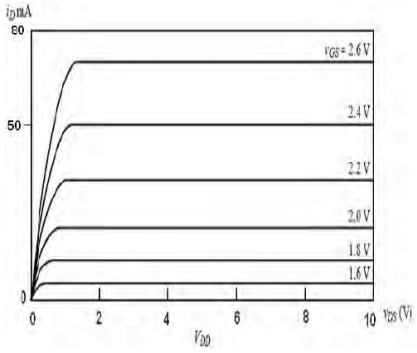
According to calculations, $V_{DS} > V_{GS} - V_{TH}$

As this is true (4 > 2 + 1), it is verified that the MOSFET operates in the saturated region.

Problem 3 - MOSFET as Switch

Determine the operating points of the MOSFET circuit shown below. The MOSFET is used as a switch. The input signal of the circuit varies between 0V and 2.4V. Determine the operating point for both input voltages. Use the output characteristic below to determine the operating point.





For 2.4V input

$$V_{DS} = V_{DD} - V_{RD} = 10 - 125 \cdot 0.05 = 3.75V$$

MOSFET operates in saturation point

For 0V input (no input)

$$V_{DS} = V_{DD} - V_{RD} = 10 - 125 \cdot 0 = 10V$$

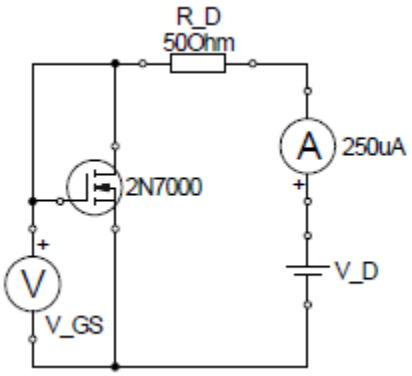
MOSFET operates in cut-off region

Execution Field Effect Transistor

Part 1 - I/V Characteristic of a MOSFET

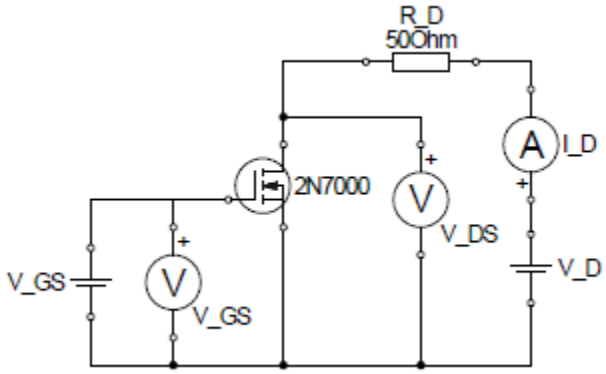
Experimental Setup and Procedure

1. Use the following circuit to determine U_{th}.



$U_{th} = U_{GS} = U_{DS}$ when $I_D = 250\mu$ A. Measure and record U_{th} and I_D.

2. Use the following circuit to measure the transfer characteristic.



The gate source voltage should be scanned from 0V to 3V. Ensure that the drain source voltage U_{DS} is kept constant at 5V while changing U_{GS}!!

3. Use the circuit from before and measure the output characteristic for gate source voltages of 2V, 2.2V, 2.4V, and 2.6V. The drain source voltage should be scanned from 0V to 4V.

Note: All important features of the current / voltage characteristic should be captured: Off region, sub-threshold region, linear region, and saturation region.

Results

In the first step, we measured U_{th} = 2.115V and I_D = 250.28µA

In the second step, we kept V_{DS} at 5V and measured the following values:

V_D (V)	V_{GS} (V)	V_{DS} (V)	I_D (mA)
4.9	0.008	5.001	0.003
4.9	1.801	5.002	0.005
5.0	1.999	5.001	0.067
5.0	2.106	5.003	0.237
5.3	2.206	5.003	0.737
5.9	2.297	5.004	1.843
7.9	2.404	5.008	46.30
8.0	2.502	5.001	48.20
8.1	2.061	5.000	50.33

In the third step, the output characteristics were to be measured for V_{GS} = 2V, 2.2V, 2.4V, 2.6V. We did not measure for 2V as that is below V_{th} and was not useful in our analysis and that would be in the cutoff region. For 2.2V the results are given below:

V_{GS} (V)	V_{GS} - V_{th} (V)	V_{DS} (V)	V_{DS} source (V)	I_D (μA)
2.206	0.091	0.0051	0	14.55
		0.0998	0.3	530.3
		0.201	0.5	603.2
		0.5033	0.8	664.1
		1.0063	1.3	678.7
		1.5013	1.8	686.3
		2.0036	2.3	693.6
		2.499	2.8	700.9
		3.0099	3.3	707.9
		3.4966	3.8	715.5
		3.9926	4.3	723.4

For 2.4V:

V_{GS} (V)	V_{GS} - V_{th} (V)	V_{DS} (V)	V_{DS} source (V)	I_D (mA)
2.406	0.291	0.000	0.0	0.01
		0.048	1.0	1.86
		0.101	1.6	2.87
		0.504	0.7	4.64
		1.005	1.4	8.16
		2.011	2.9	16.96
		3.005	4.6	26.45
		4.086	6.3	36.88

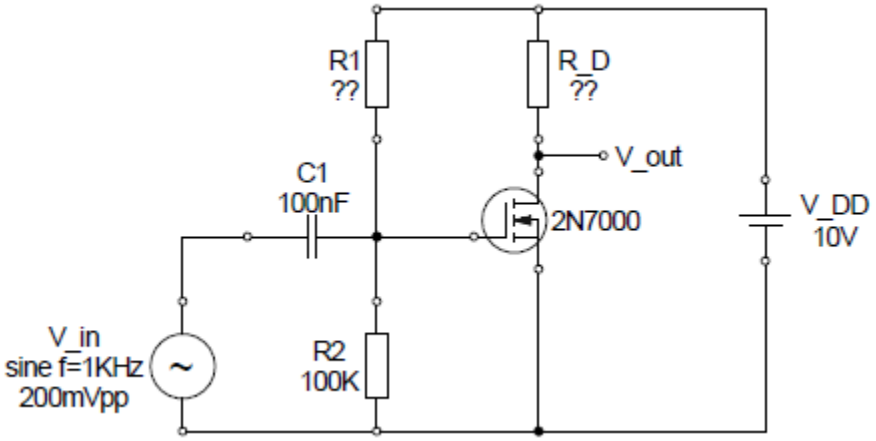
For 2.6V:

V_{GS} (V)	V_{GS} - V_{th} (V)	V_{DS} (V)	V_{DS} source (V)	I_D (mA)
2.603	0.488	0.000	0.0	0.016
		0.101	0.5	8.556
		0.199	0.8	11.879
		0.497	0.9	9.169
		1.005	1.6	12.064
		2.010	3.2	20.905
		2.993	4.8	30.372
		4.088	6.5	40.860

Part 2 - MOSFET as Amplifier

Experimental Setup and Procedure

1. We want to use the following circuit:



V_{GS} = 2.7V, V_{DS} = 5V, k = 72.2mA/V2, U_{th} = use measured value!

2. Determine the values for R_1 and R_D. It can be assumed that the gate source current is zero
3. Assemble the circuit.
4. Apply a sinusoidal input signal with an amplitude of 100mV and a frequency of 1 KHz to the input of the circuit.
5. Take hard copies showing the input and the output signals and the phase relation between them.

Results

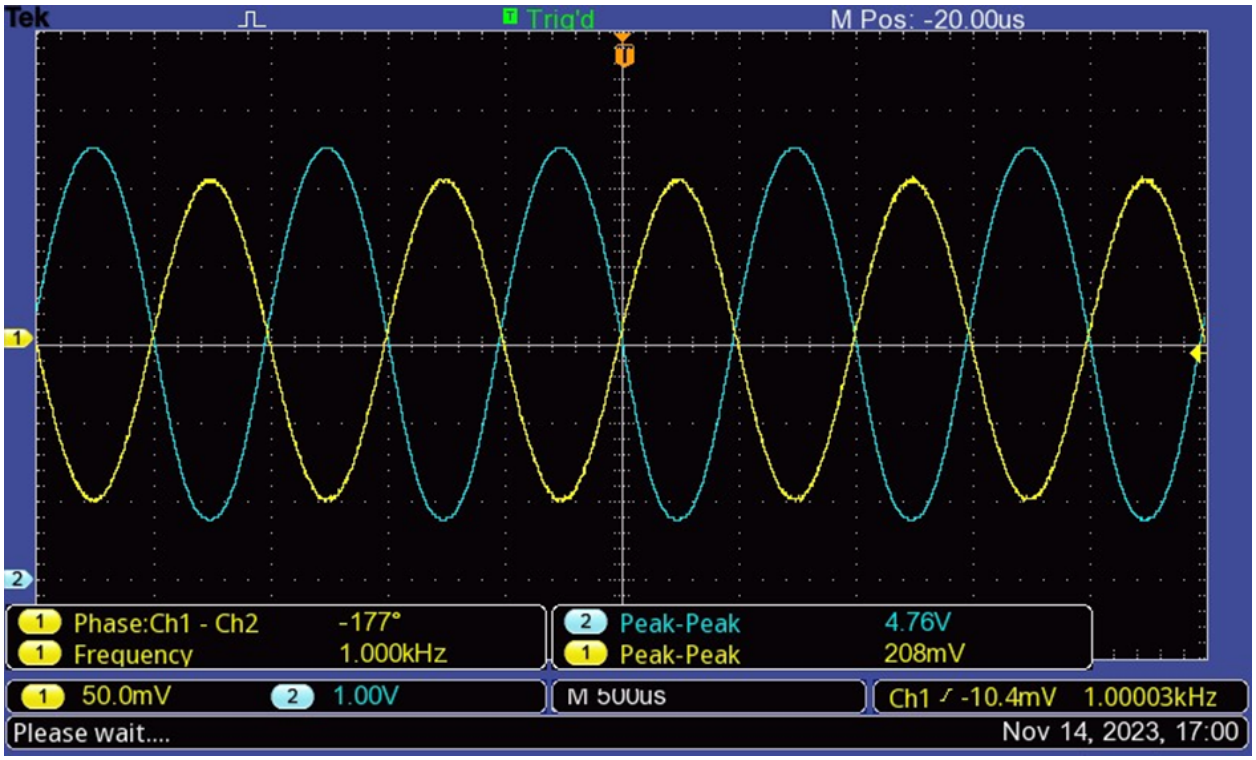
$V_{RD} = V_{DD} - V_{DS} = 10 - 5 = 5V$ and $I_{DS} = 0.0247A$ (using the formula in the prelab)

$$R_D = \frac{V_{RD}}{I_{DS}} = 202.36\Omega$$

$$R_1 = \frac{R_2 V_{DD}}{2V_{R2}} = 270.37k\Omega$$

We found R_1 = 270kΩ and R_D = 202Ω. However, for R_D a 220Ω resistor was used for convenience.

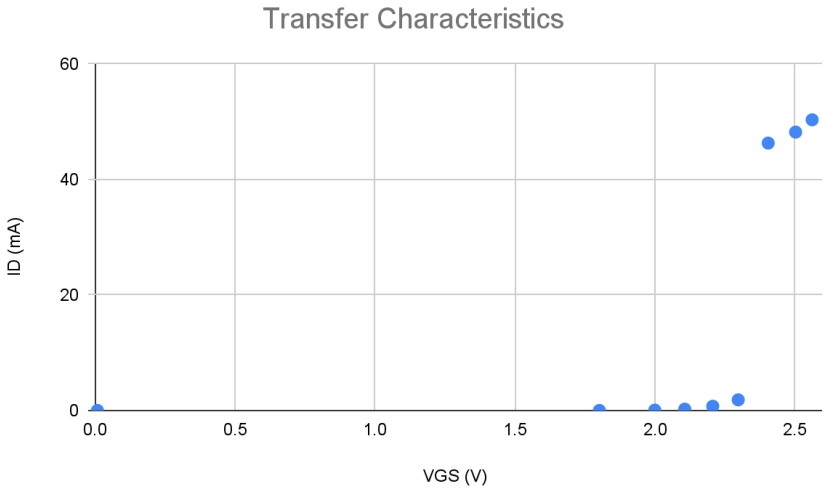
The input and output signals are shown below:



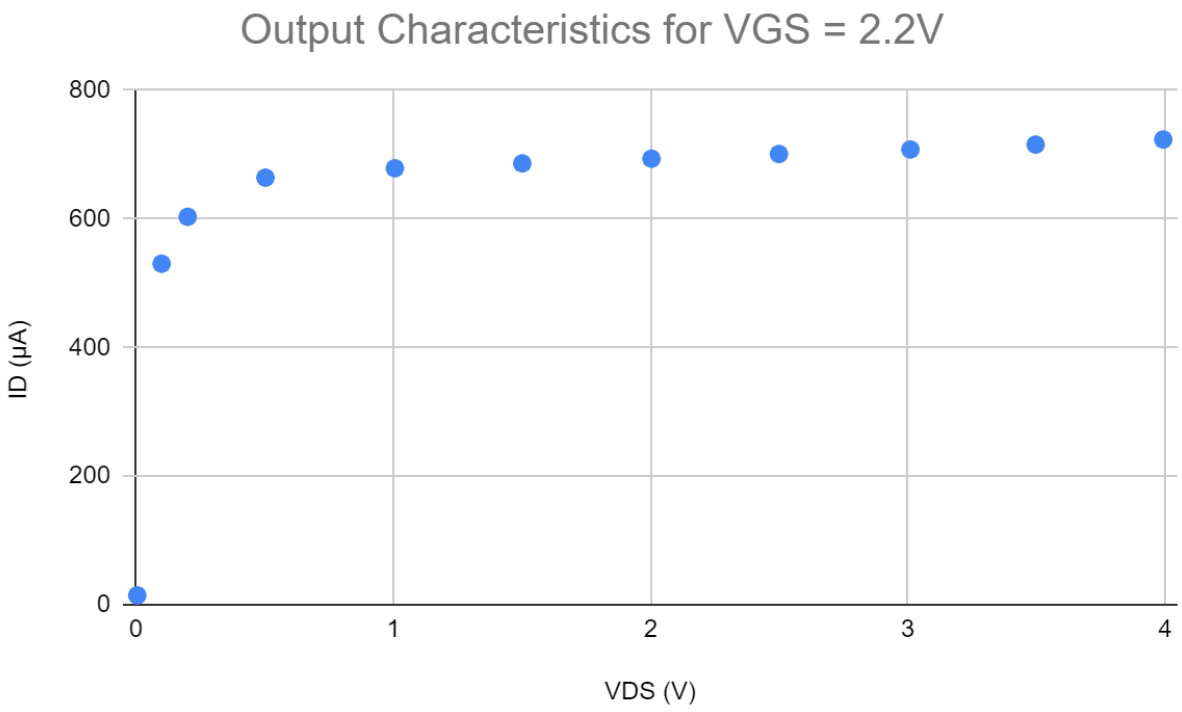
Evaluation

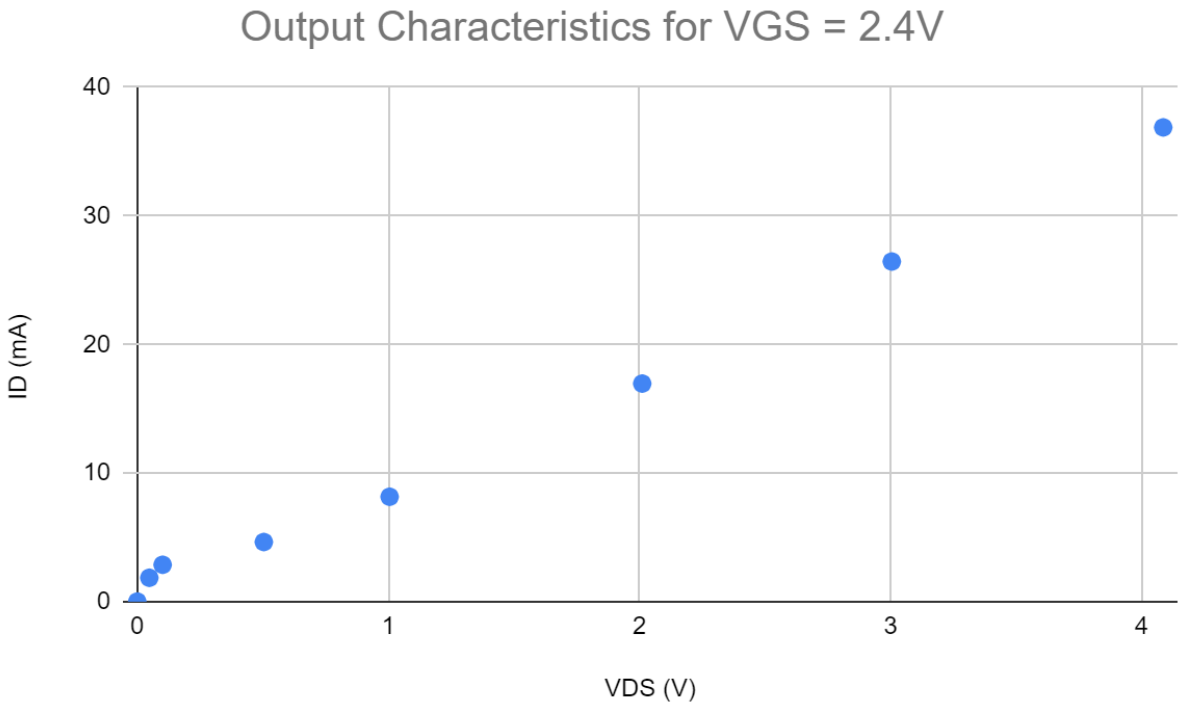
Problem 1 - I/V Characteristic of a MOSFET

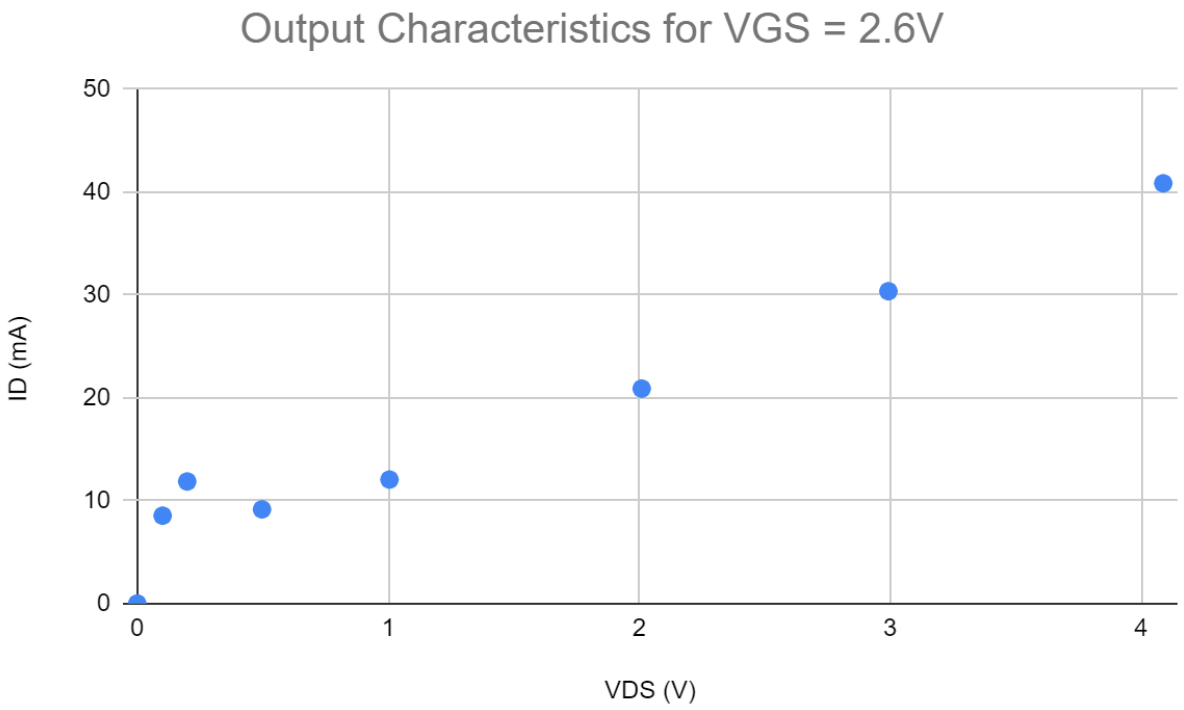
1. **Plot the measured transfer characteristic.**



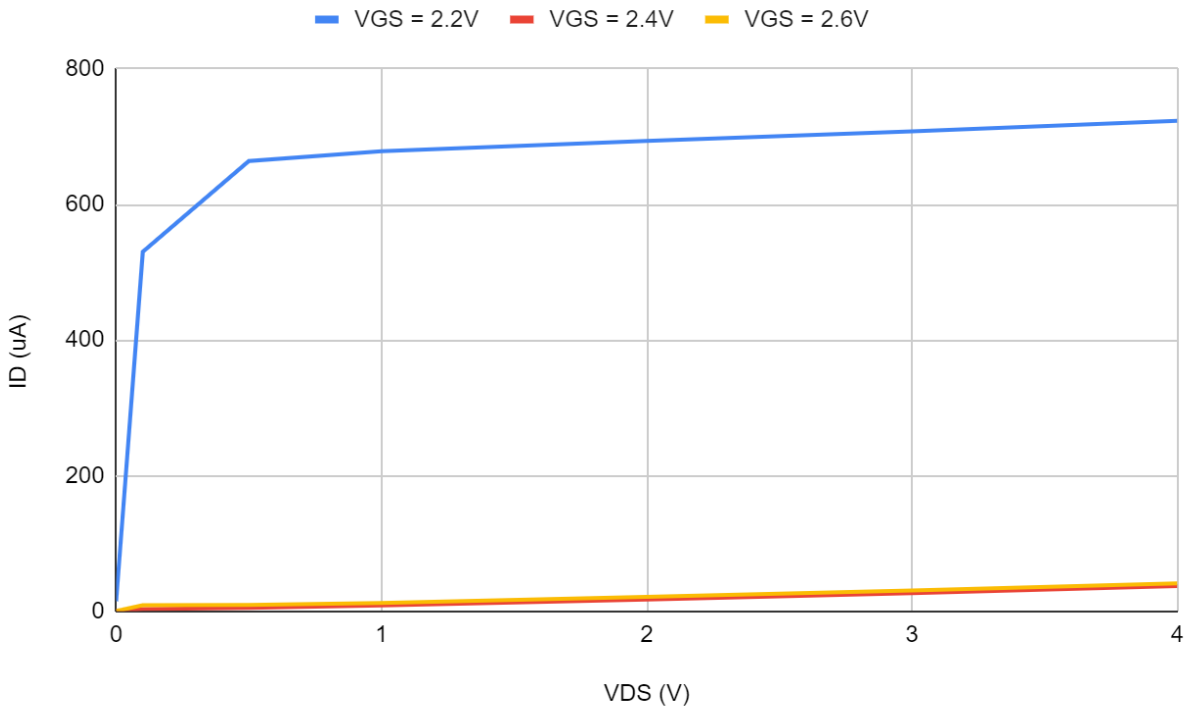
2. **Plot the measured output characteristic for the different gate source voltages.**




Output Characteristics for VGS = 2.4V
ID (mA)
40
30
20
10
0
0
1
2
3
4
VDS (V)


Output Characteristics for VGS = 2.6V
ID (mA)
50
40
30
20
10
0
0
1
2
3
4
VDS (V)

3. **Insert the $V_{DS} = V_{GS} - V_{th}$ line into the output characteristic.**



Problem 2 - MOSFET as Amplifier

1. **In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.**

In saturation mode, I_D is solely determined by V_{GS}, indicating that the circuit's output (V_{out}) relies exclusively on the current passing through R_D. This observation leads to the unequivocal conclusion that the MOSFET is operating in saturation mode.

2. **If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.**

$A_V = \frac{4.76}{0.208} = 22.88$ and $V_{out\ (max)} = 5 + 0.5 \cdot 4.76 = 7.38V$

$V_{in\ (max)} = \frac{7.38}{22.88} = 0.33V$

3. **Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.**

$A_{theoretical} = \frac{V_{out}}{V_{in}} = \frac{V_{DD} - R_D k (V_{GS} - V_{th})^2}{V_{in}}$

4. **Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.**

$$A_{theoretical} = 25.07 \text{ and } A_{experimental} = 22.88$$

As observed, the theoretical and experimental values are closely aligned, with a slight deviation likely attributed to factors such as the use of a resistor with a slightly different value than the theoretical one and other errors like tolerance and precision. In contrast, the experimental gain appears smaller, exhibiting a significant difference from the theoretical value. This difference could stem from the utilization of a 220Ω resistor instead of a 202Ω one for R_D due to availability constraints. Additionally, variations in the transistor's characteristics and the 5% error in the oscilloscope's measure function contribute to the overall discrepancy in the final output value.

5. Explain the phase relation between the input and the output.

Our observations consistently reveal a phase difference of about 180° between the input and output signals. This behavior stems from the circuit dynamics, where an increase in the positive direction of the input signal results in a positive surge in drain current, leading to an upswing in the voltage across R_D and, consequently, a decline in the output voltage. This consistent opposition in the directions of *Vout* and *Vin* manifests as a 180° phase difference.

Conclusion

In this laboratory session, our primary focus was on exploring the characteristics and applications of MOSFETs. The initial phase involved utilizing a MOSFET in a circuit to determine its threshold voltage, followed by integrating the same MOSFET into another circuit to examine its transfer characteristics. While analyzing the collected data, we observed some irregularities, potentially influenced by the self-heating of the transistor. Despite these variations, the data generally aligned with our theoretical understanding, providing insights into the relationship between drain current and gate-source voltage. The developed curves effectively distinguished the saturation mode from the triode mode.

In the second part, we employed a MOSFET as an amplifier, constructing an amplifier circuit with appropriate resistors. The oscilloscope revealed an output that was an amplified version of the input, characterized by a 180° phase difference. Analysis indicated a slightly smaller experimental gain than the theoretical gain, attributed to the utilization of a resistor (R_D) that deviated from the calculated value. Additionally, factors such as oscilloscope resolution and component tolerances contributed to discrepancies between experimental, simulated, and theoretical values, emphasizing the impact of non-ideal conditions on our results.

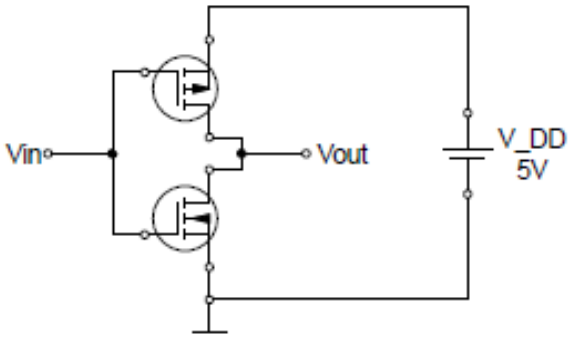
References

Pagel, Uwe. *CO-526-B Electronics Lab Manual*. 2023.

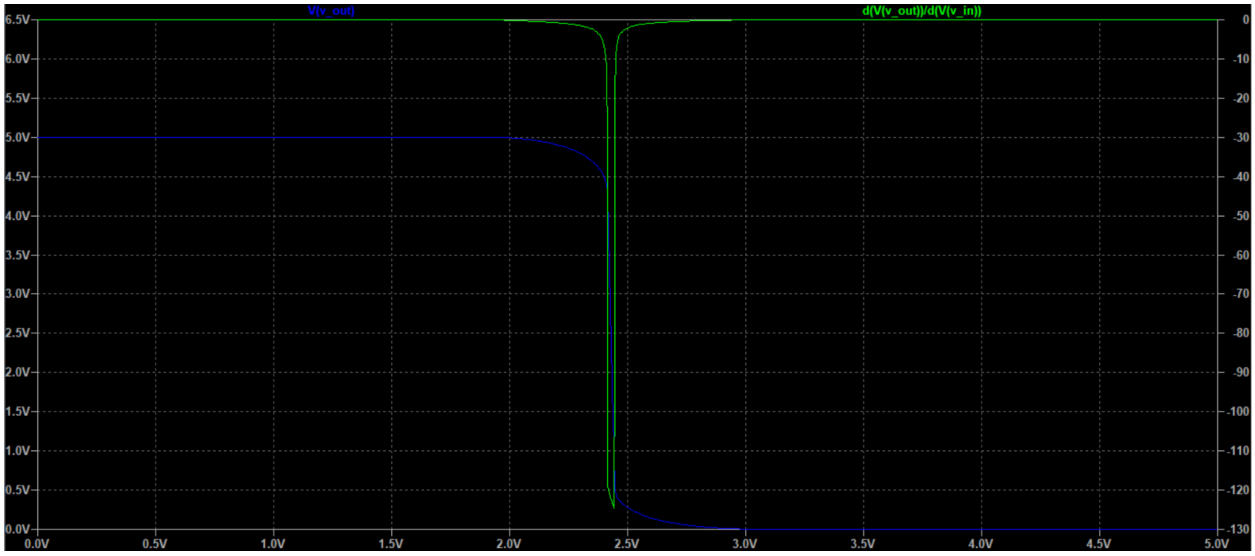
Appendix

Prelab - CMOS Inverter and Logic Gates

Problem 1 - Voltage Transfer Characteristic of a CMOS inverter



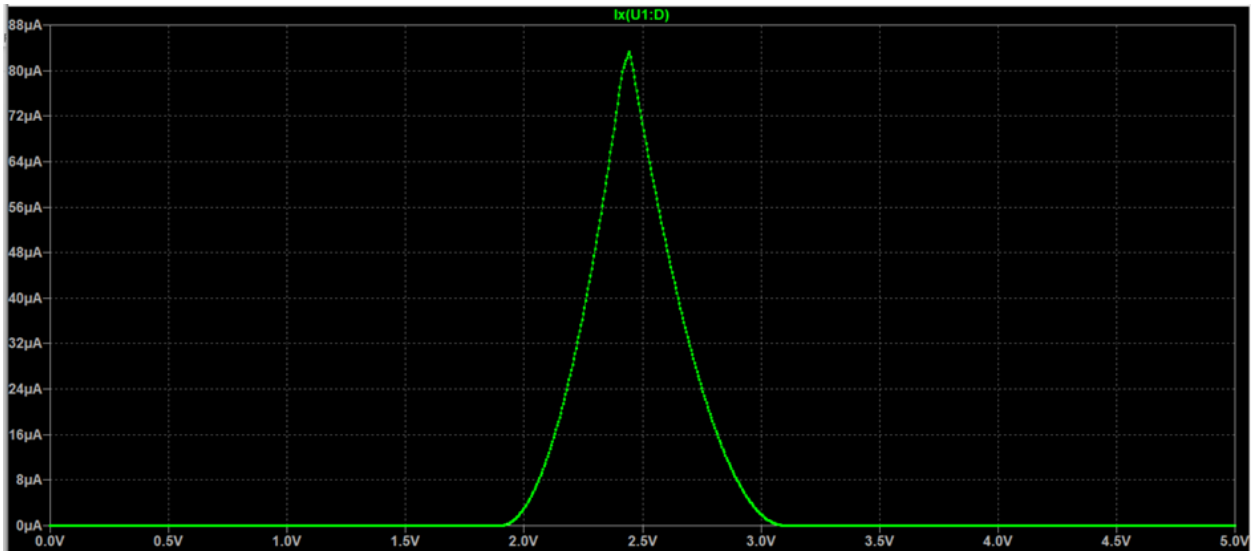
1. **Simulate the voltage transfer characteristic of a CMOS inverter. Use 5V for the power supply V_{DD}. Simulate the voltage transfer curve (VTC) of the CMOS inverter and extract the values of V_{OH}, V_{OL}, V_{IH}, V_{IL}, N_{ML}, N_{MH}, and V_{th}.**



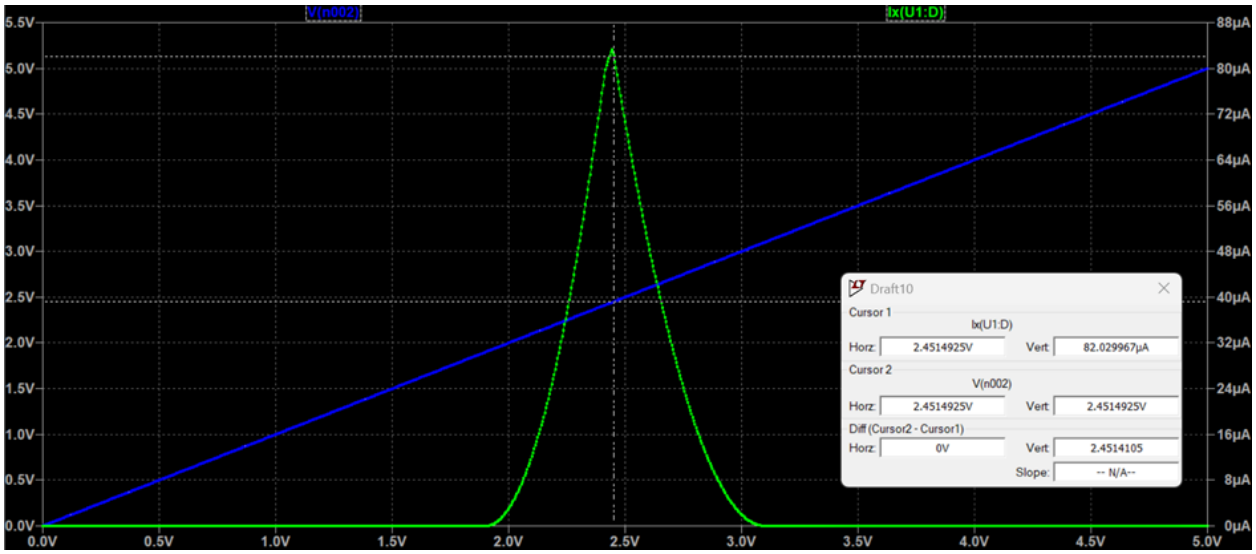
We get the following results:

V_{OH}	4.87V
V_{IL}	2.34V
V_{OL}	166.89mV
V_{IH}	2.57V
NM_L	133.07mV
NM_H	166.89mV

2. Simulate the current flowing through the inverter as a function of the input voltage.

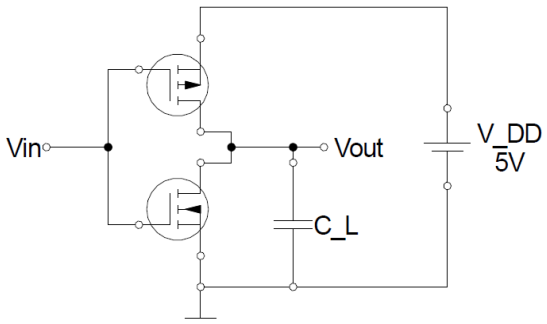


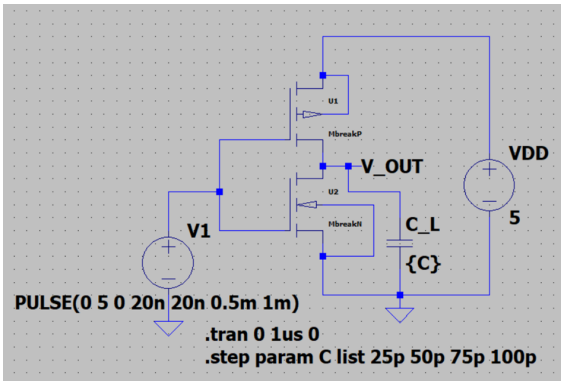
3. **For what input level the current reaches its maximum. Provide an explanation.**



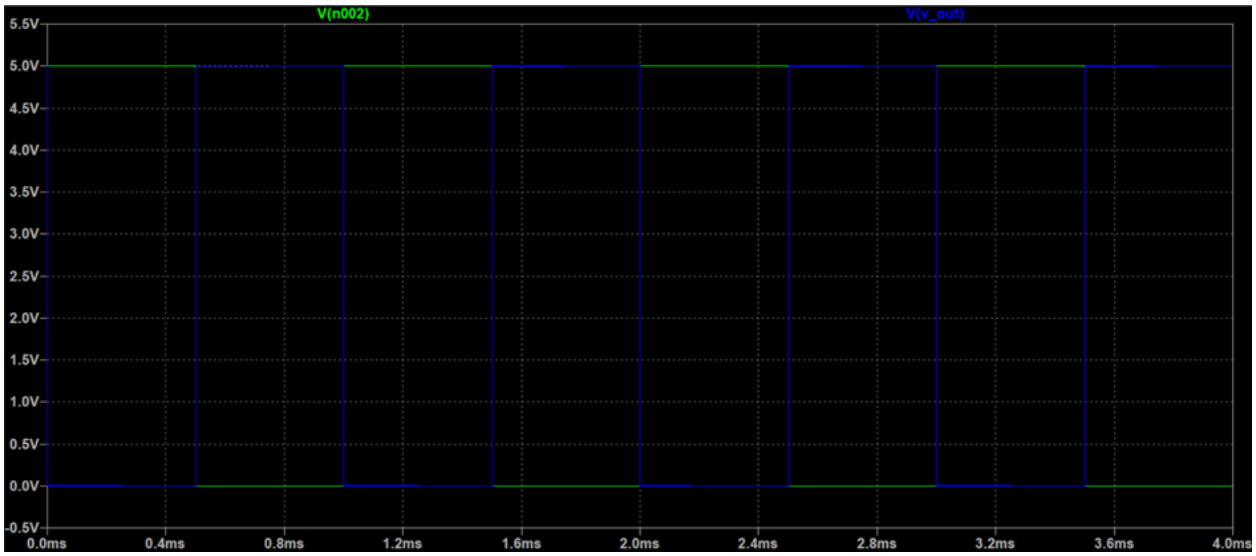
At this stage, in both theoretical analysis and simulation, the maximum current level is attained when the input voltage is 2.45V. At this precise point, the input and output voltages become equal, causing both NMOS and PMOS transistors to turn on simultaneously, resulting in the achievement of the maximum current level, measured at 82.03µA.

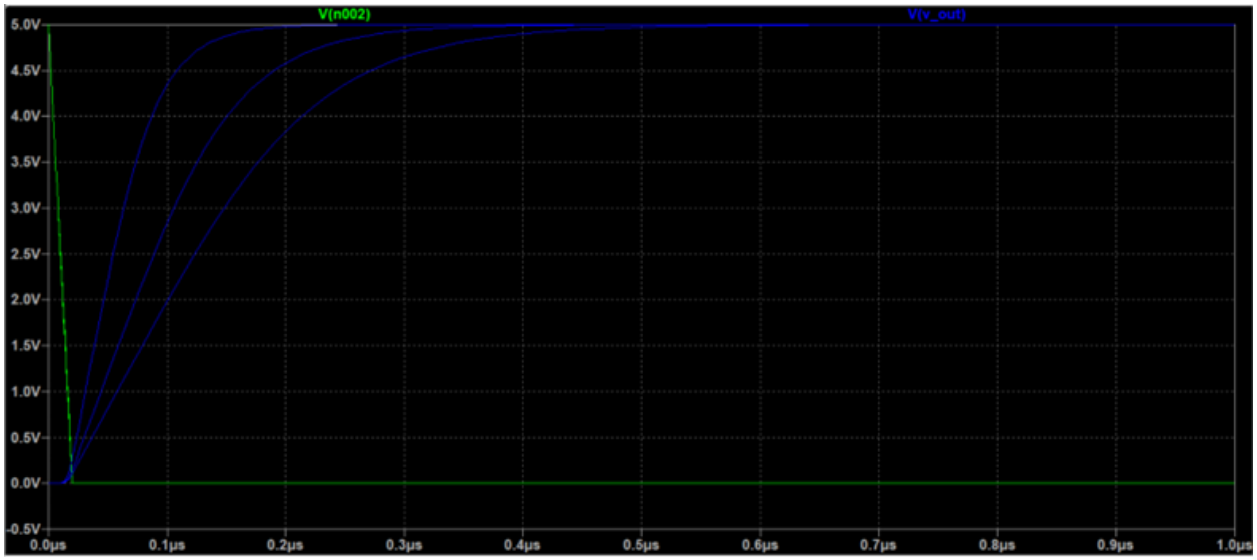
Problem 2 - CMOS Inverter with Capacitive Load





1. **The capacitive load should be varied from 25 pF to 100 pF in 25 pF steps. Determine the propagation delay ($t_{PLH} = t_{PHL}$) if the input signal is given by a 1 kHz square wave with a 20 ns rise and fall time. Use 5V for the power supply V_{DD}.**





Capacitance (pF)	Propagation Delay (ns)
25	231
50	354
75	483
100	668

We can see that as capacitance increases, the time delay increases.

2. **Obtain the dynamic power dissipation of the CMOS inverter for the different load capacitors.**

$P_D = f \cdot C \cdot V_{DD}^2$

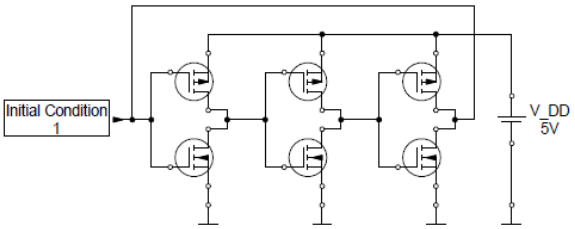
$P_{D1} = 0.625\mu W$

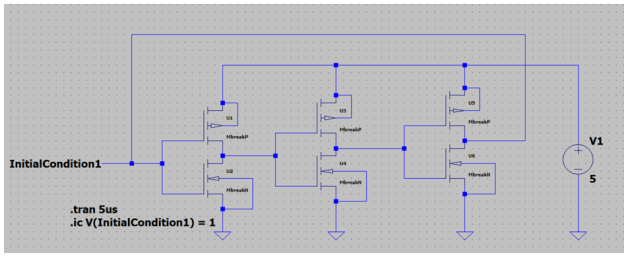
$P_{D2} = 1.25\mu W$

$P_{D3} = 1.88\mu W$

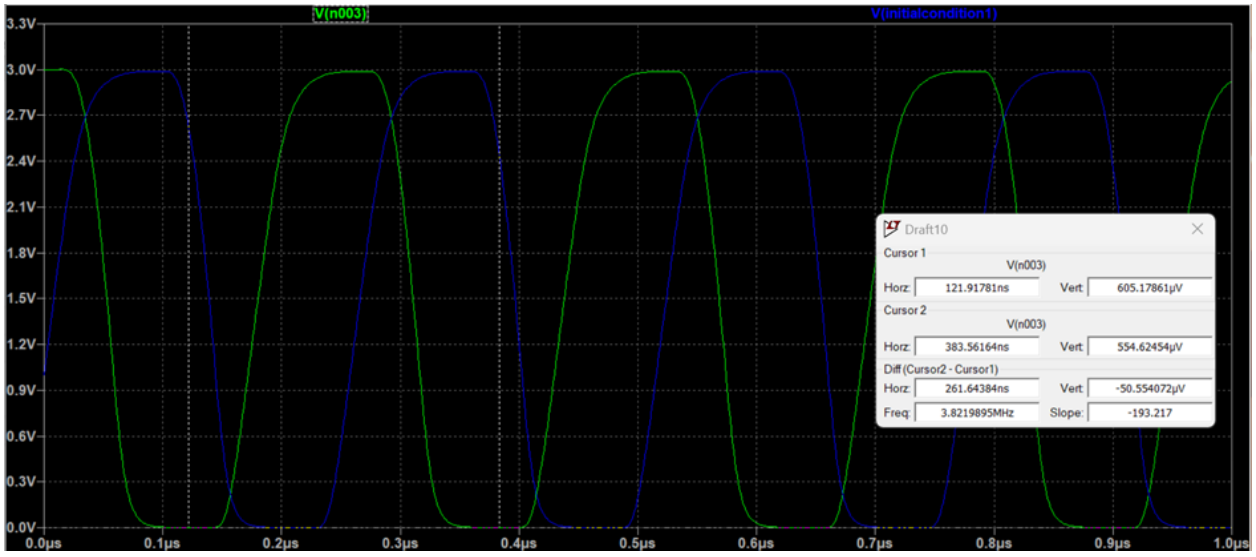
$P_{D4} = 2.5\mu W$

Problem 3 - Propagation Delay of an Inverter Stage





1. **Determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of 3 V, 5 V, 7V and 10 V, respectively.**



Propagation delay is given by:

$$t_d = \frac{1}{2 \cdot N \cdot f}$$

The results are as follows combined with the t_d calculations:

Voltage (V)	Frequency (MHz)	t_d (ns)
3	3.85	43.25
5	23.33	7.14
7	55.25	3.02
10	122.32	1.36

2. **Calculate the dynamic power dissipation per inverter stage for the different supply voltages.**

$$P_D = f \cdot C \cdot V_{DD}^2$$

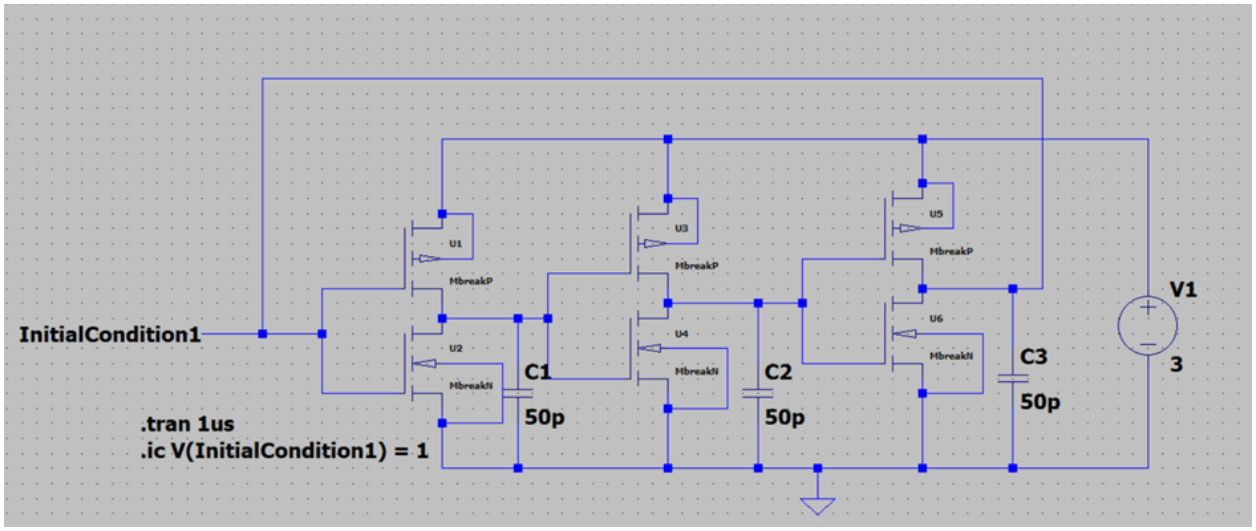
$$P_{D1} = 0.17mW$$

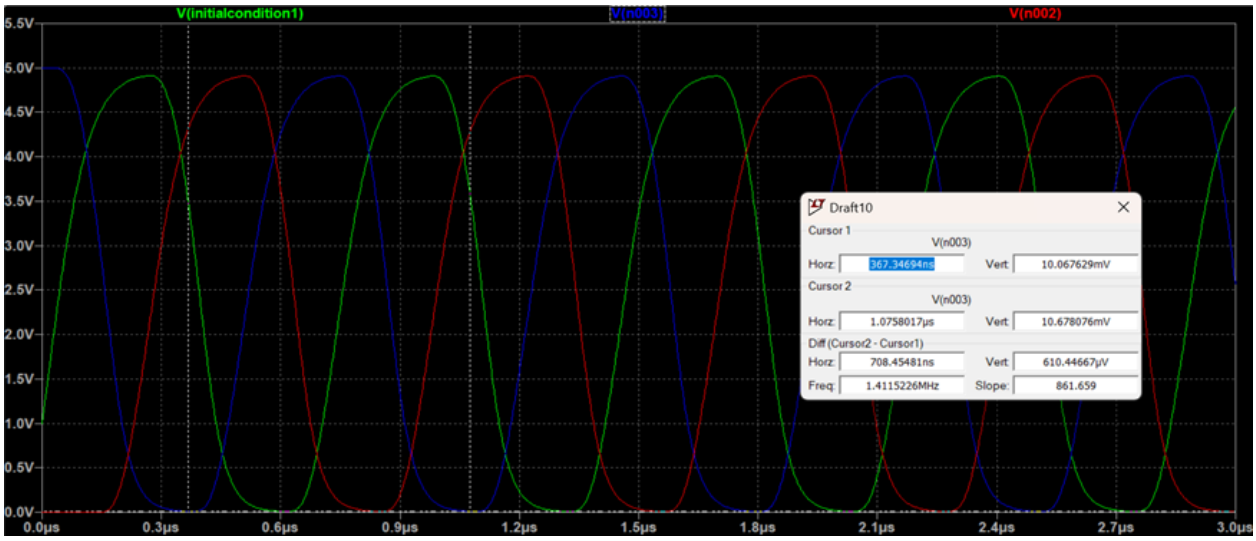
$$P_{D2} = 12.92mW$$

$$P_{D3} = 13.54mW$$

$$P_{D4} = 61.16mW$$

3. **Add a 50pF load capacitor to each inverter of the 3-stage ring oscillator and measure the oscillation frequency and determine the propagation delay per inverter for a power supply of V_{DD} = 5.0V**





Using cursors, we obtained f = 1.41MHz

$$t_d = \frac{1}{2 \cdot N \cdot f} = 118.08ns$$

$$P_D = f \cdot C \cdot V_{DD}^2 = 1.76mW$$

4. **What is the effect of the capacitive load on the propagation delay and the oscillation frequency?**

Because of the capacitive load, there is an increase in propagation delay and a decrease in oscillation frequency.

5. **What is the effect of the capacitive load and the power supply on the power dissipation?**

By observation, we noted that augmenting the power supply leads to an increase in the output frequency, while an increase in load capacitance results in a decrease in frequency. This establishes a direct proportionality between frequency and power dissipation. Consequently, the utilization of load capacitance provides a means to reduce power dissipation without necessitating any adjustments to the power supply.

Note: Experiment 6 was not performed due to medical absence.