

# **Constructor University Bremen**

**CO-526-B**

**Electronics Lab**

**Fall Semester 2023**

## **Lab Experiment 3 – Bipolar Junction Diode**

Experiment conducted by: Abhigyan Deep Barnwal

Place of execution: Room 54, Research I, Jacobs University, 28759 Bremen

Date of execution: 20<sup>th</sup> November 2023

Author of the Report: Abhigyan Deep Barnwal

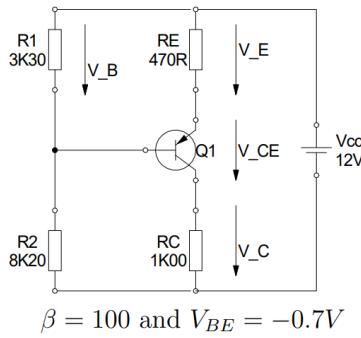
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## Introduction

This experiment aims to acquaint us with bipolar junction transistors (BJTs). A BJT, a semiconductor device with three terminals, is primarily employed in analog circuits, particularly in high-speed amplifiers. BJTs operate in three modes: active mode, cut-off mode, and saturation mode. When functioning as an amplifier, the BJT needs to operate in active mode.

## Prelab - BJT

### Problem 1 - Biasing of Bipolar Junction Transistors



$$\beta = 100 \text{ and } V_{BE} = -0.7V$$

#### 1. Analyze the above circuit:

a. Calculate  $V_B$ ,  $V_E$ ,  $V_{CE}$ , and  $V_C$

b. Calculate  $I_B$ ,  $I_E$ , and  $I_C$

We can make a thevenin equivalent circuit to calculate the required values:

$$V_{TH} = \frac{R_1 V_{cc}}{R_1 + R_2} = 3.44V$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 2353.04\Omega$$

$$V_E + V_{EB} + V_{RTH} = V_{TH}$$

$$(\beta + 1)I_B R_E + V_{EB} + I_B R_{TH} = V_{TH}$$

$$I_B = \frac{V_{TH} - V_{EB}}{R_E(\beta+1) + R_{TH}} = 5.49 \cdot 10^{-5} A$$

$$I_E = (\beta + 1)I_B = 5.54 \cdot 10^{-3} A$$

$$I_C = \beta I_B = 5.49 \cdot 10^{-3} A$$

$$V_E = I_E R_E = 2.60V$$

$$V_C = I_C R_C = 5.49V$$

$$V_{CE} = V_{CC} - V_E - V_C = 3.91V$$

$$V_B = V_E + V_{EB} = 3.30V$$

**2. Use the same circuit. Calculate the necessary biasing resistors ( $R_1$ ,  $R_2$ ,  $R_C$  and  $R_E$ ) under the assumption that  $V_{CEQ} = 8V$  and  $I_{CQ} = 8mA$ . The transistor operates in the active mode. Other parameters:  $V_{CC} = 20V$ ,  $\beta = 150$ ,  $V_E = 4V$ ,  $R_{th} = 0.1\beta R_E$**

$$I_E + I_B = I_C$$

$$I_B = \frac{I_C}{\beta} = 5.33 \cdot 10^{-5} A \text{ and } I_E = (\beta + 1)I_B = 8.05 \cdot 10^{-3} A$$

$$R_E = \frac{V_E}{I_E} = \frac{4}{8.05 \cdot 10^{-3}} = 496.73\Omega \text{ and } R_C = \frac{V_C}{I_C} = \frac{8}{8 \cdot 10^{-3}} = 1000\Omega$$

$$V_E + V_{EB} + V_{RTH} = V_{TH} \text{ so then } V_{TH} = 5.10V$$

$$V_{TH} = \frac{R_1 V_{CC}}{R_1 + R_2} \text{ and } R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

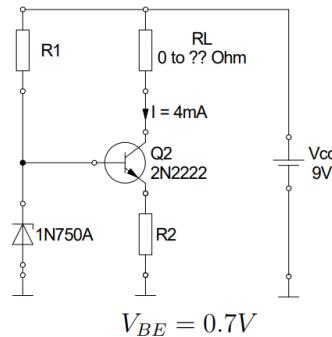
Solving the above two equations simultaneously:

$$R_1 = 0 \text{ or } R_1 = 9999\Omega \text{ and } R_2 = 0 \text{ or } R_2 = 29.24k\Omega$$

Bias can't be 0

$$R_1 \approx 10k\Omega \text{ and } R_2 \approx 29k\Omega$$

## Problem 2 - Constant Current Source



Find the values for  $R_1$  and  $R_2$  to get a constant current of  $I_C \approx 4\text{mA}$

$$V_{R1} = V_{CC} - V_Z = 4.3V$$

$$R_1 = \frac{V_{R1}}{I_Z} = \frac{4.3}{0.02} = 215\Omega$$

$$I_E \approx I_C = 4\text{mA}$$

$$R_2 = \frac{V_{R2}}{I_E} = \frac{V_Z - V_{BE}}{I_E} = 1k\Omega$$

What is the maximum value for  $R_L$  to still get  $I_C \approx 4\text{mA}$ ?

$$V_C = V_{CC} - V_{CE} - V_E$$

$$R_L = \frac{V_{CC} - V_{CE} - V_E}{I_C} = \frac{9 - V_C - 4}{0.004} = 250(5 - V_{CE})$$

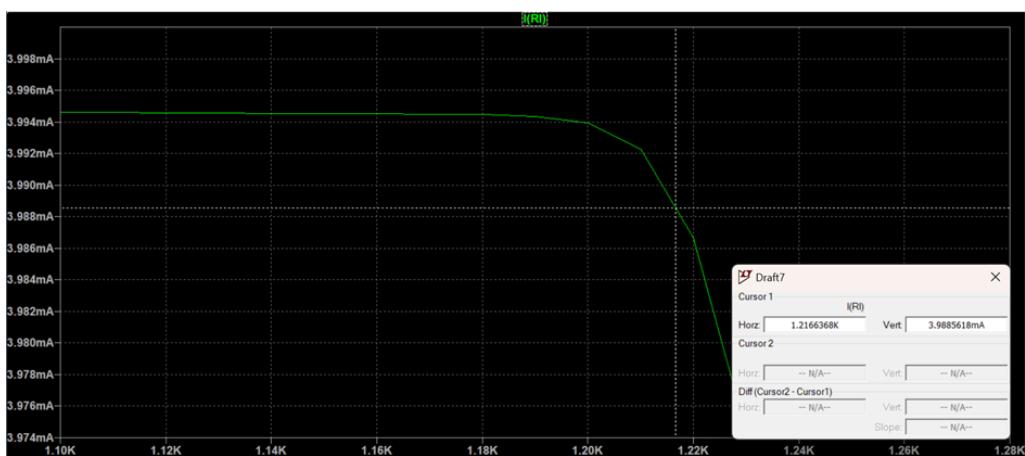
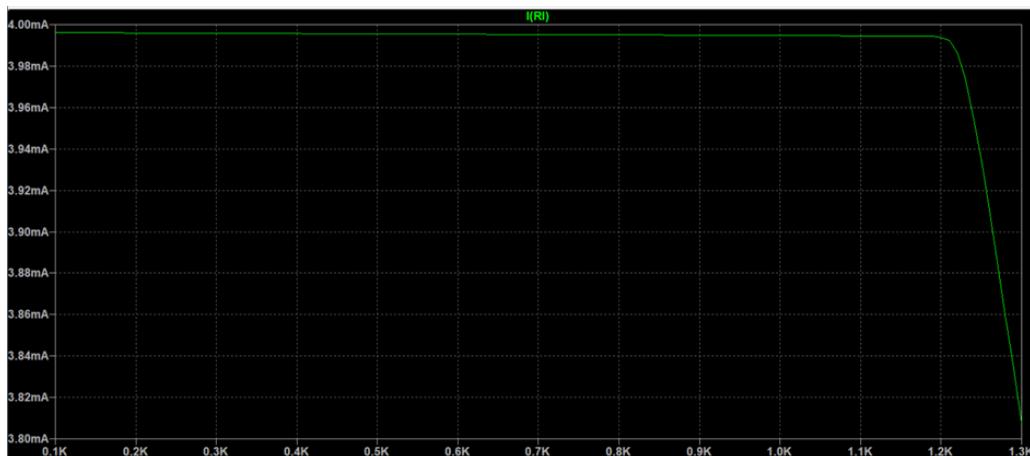
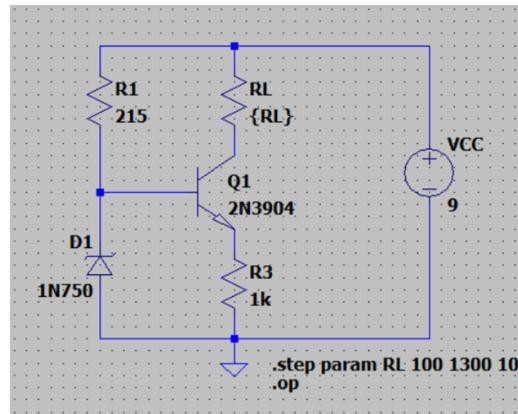
For the active region,  $V_{BE}$  has to be forward biased (non-negative) and  $V_{BC}$  must be reverse biased, so  $V_{CB}$  is non-negative.

$$V_{CE} - V_{BE} \geq 0$$

$V_{CE} \geq V_{BE} = 0.7$  so then  $V_{CE} \geq 0.7$  and the minimum  $V_{CE}$  can give the max  $R_L$

$$R_L = 250(5 - V_{CE}) = 1075\Omega$$

**Implement the circuit in LTSpice and verify your calculations! Use the .step command to vary RL.**



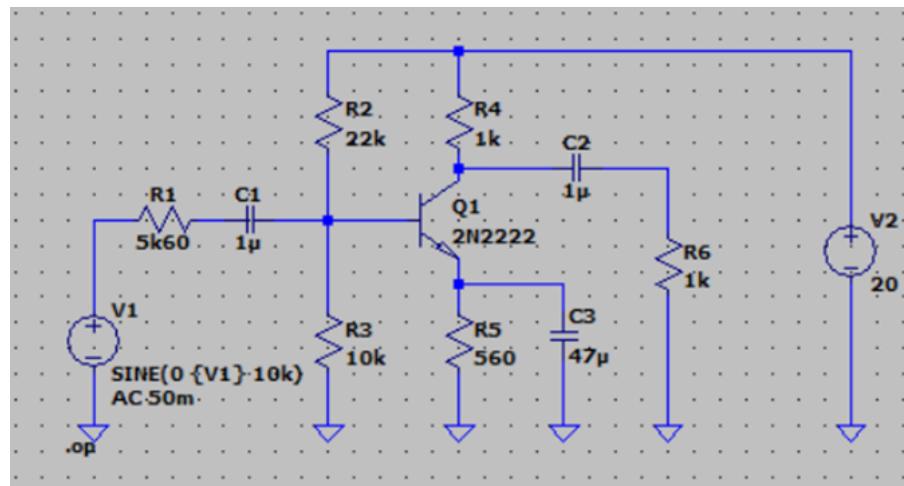
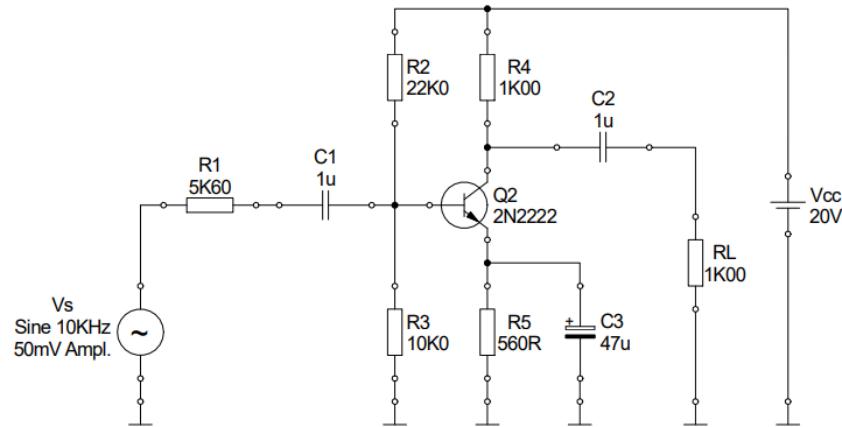
$R_L=1.22\text{k}\Omega$  which is quite close to the calculated value.

### Explain the function principle of the circuit!

The Zener diode plays a crucial role as a voltage stabilizer in this circuit, maintaining a constant voltage of 4.7V. This stability ensures a constant voltage across  $R_1$ , resulting in a consistent  $I_{R1}$ . With  $V_{BE}$  remaining constant,  $V_E$  across  $R_2$  also stays steady. Consequently,  $I_E$  remains constant, and with negligible  $I_B$ ,  $I_C = I_E = \text{constant}$ . This behavior holds true for varying  $R_L$ , as long as we do not surpass the threshold. The overall effect is that, when the current through the Zener diode reaches its operational level, the voltage remains constant, turning the circuit into a reliable constant current source, as long as the threshold is not crossed.

### Problem 3 - Amplifier circuit

#### 1. Implement the following circuit in LTSpice



## 2. Determine the DC operation point values for $V_B$ , $V_{BE}$ , $V_C$ , $V_{CE}$ , $V_E$ , $I_C$ , and $I_B$ .

--- Operating Point ---

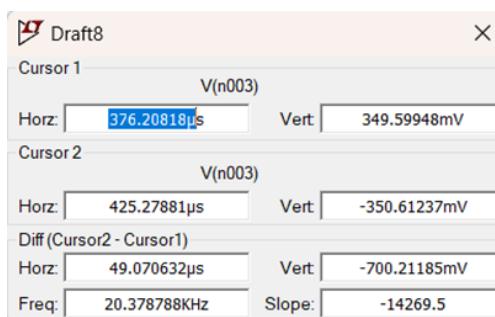
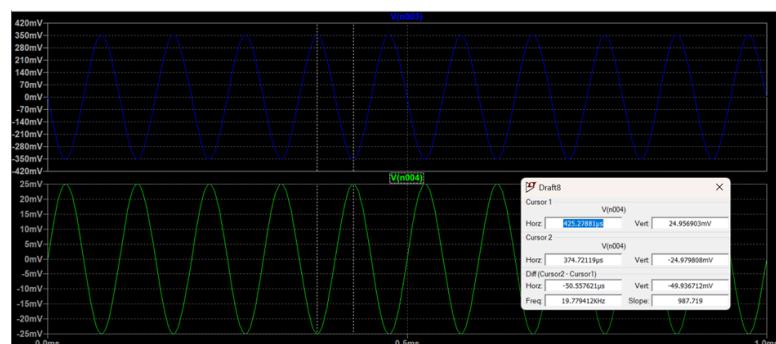
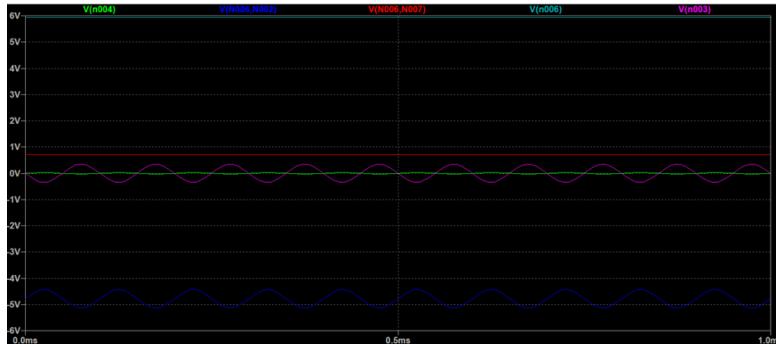
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V(n004) : 0 voltage
V(n005) : 3.17103e-014 voltage
V(n006) : 5.66256 voltage
V(n002) : 11.4554 voltage
V(n007) : 4.83284 voltage
V(n001) : 20 voltage
V(n003) : 1.14554e-014 voltage
Ic(Q1) : 0.00854462 device_current
Ib(Q1) : 8.54462e-005 device_current
Ie(Q1) : -0.00863007 device_current
I(C2) : -1.14554e-017 device_current
I(C3) : 2.27143e-016 device_current
I(C1) : 5.66256e-018 device_current
I(R6) : 1.14554e-017 device_current
I(R5) : 0.00863007 device_current
I(R4) : 0.00854462 device_current
I(R2) : 0.000651702 device_current
I(R3) : 0.000566256 device_current
I(R1) : 5.66256e-018 device_current
I(V2) : -0.00919632 device_current
I(V1) : 5.66256e-018 device_current

```

Parameter	Value
$V_B$	5.66V
$V_{BE}$	829.72mV
$V_C$	11.46V
$V_{CE}$	6.62V
$V_E$	4.83V
$I_C$	8.54mA
$I_B$	85.44 $\mu$ A

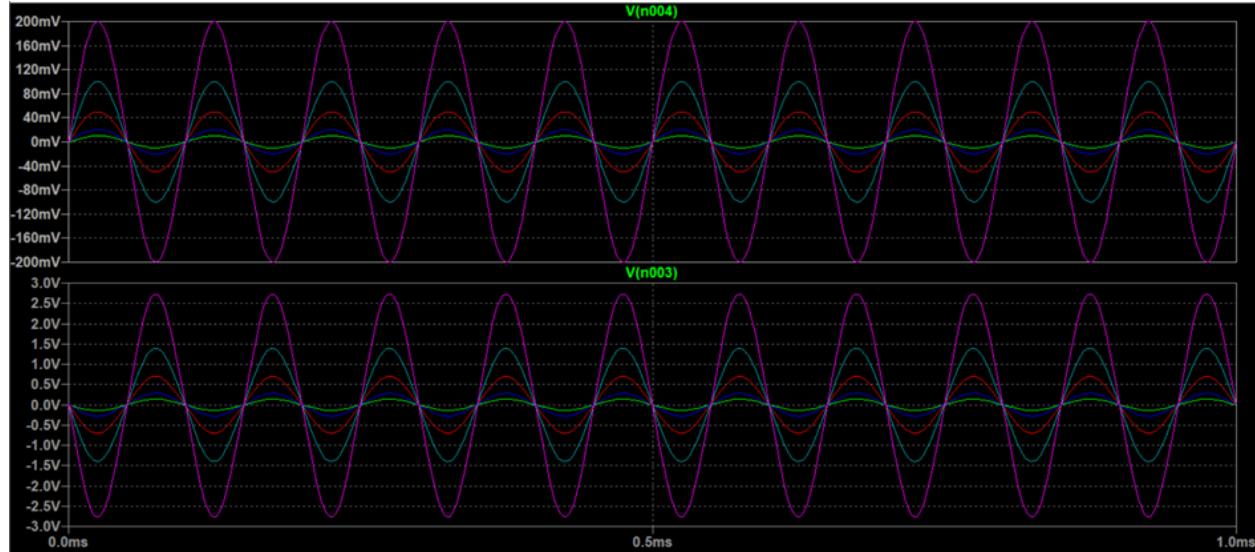
3. Perform a transient analysis for about 2 cycles of a sinusoidal input signal. Use  $V_s = 50 \text{ mV}_{\text{PP}}$  input amplitude and  $f = 1\text{kHz}$ . Display  $V_s$ ,  $V_B$ ,  $V_{BE}$ , and the voltage across the load resistance  $R_L$ . Determine the voltage gain  $Gain = V_{out}/V_s$ .



To determine the system's gain, we utilize the cursor to measure the peak-to-peak output value and then divide it by the corresponding input value.

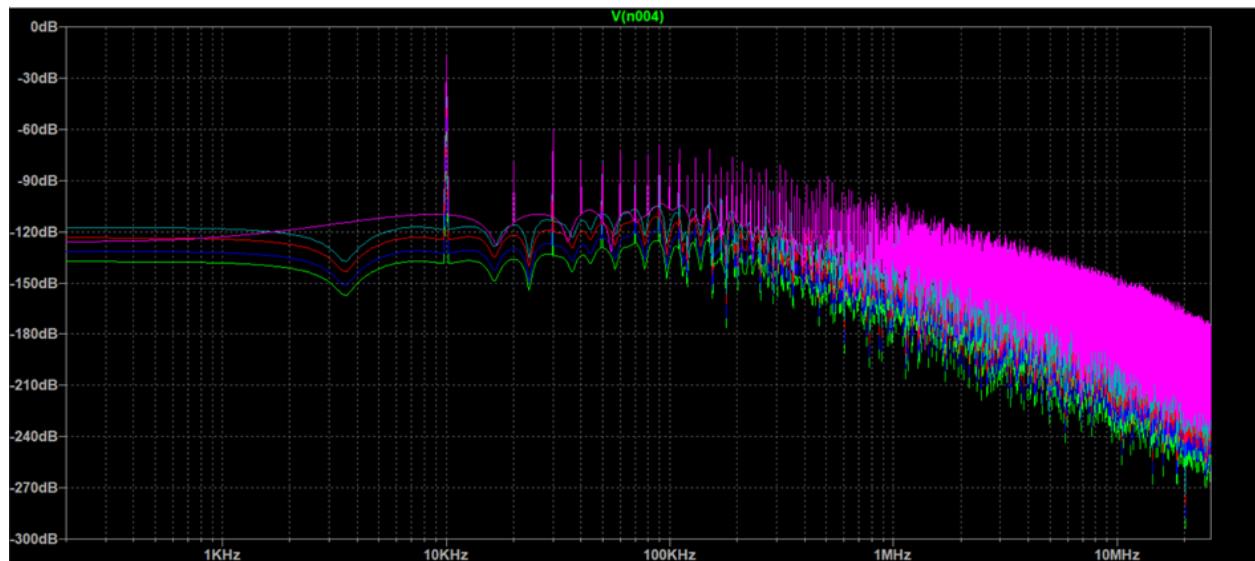
$$Gain = \frac{V_{RL}}{V_s} = 14.02$$

4. Determine the quality of the amplified signal at RL. Use the .step command to vary  $V_S$  by 10mV<sub>PP</sub>, 20mV<sub>PP</sub>, 50mV<sub>PP</sub>, 100mV<sub>PP</sub>, and 200mV<sub>PP</sub>. Use a FFT or determine the harmonic distortion to give a statement.

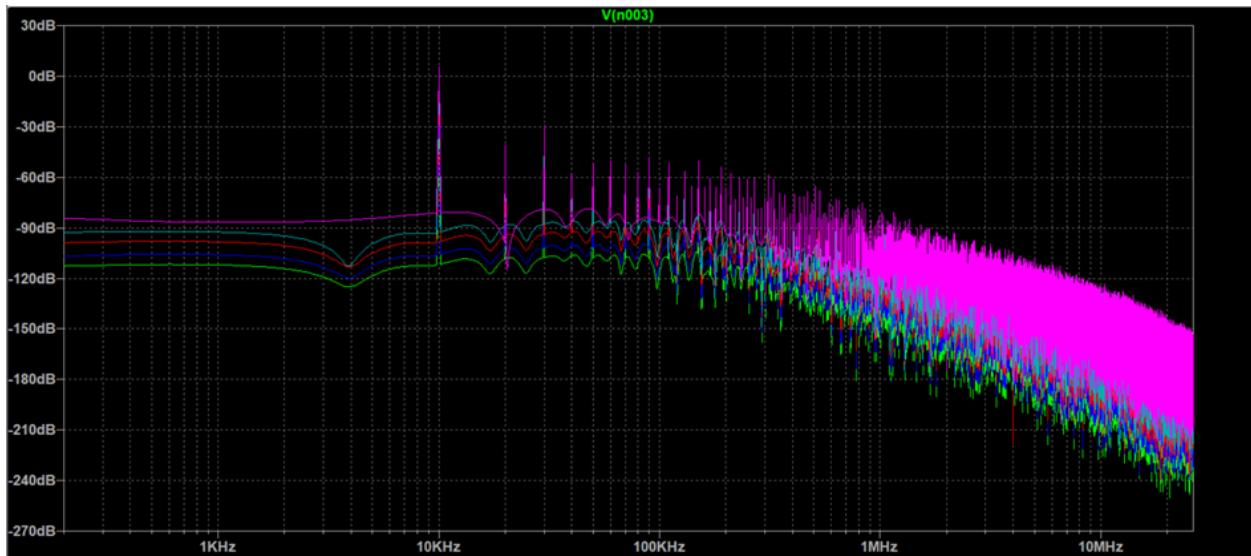


From the plots, it is evident that the output signal is an amplified version of the input signal, maintaining the same frequency but exhibiting a larger amplitude. When examined in the time domain, no visible distortions are observed. Now that we have visualized both the input and output signals, we are prepared to analyze their spectra.

FFT of Input Signal:

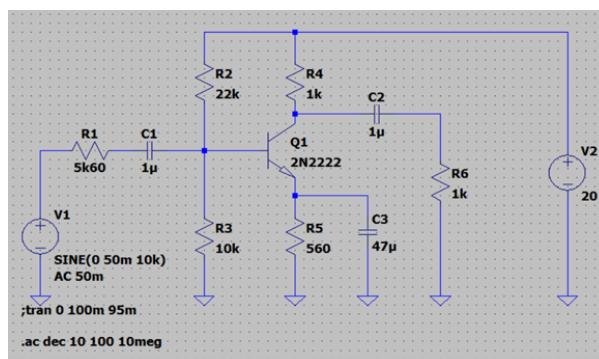


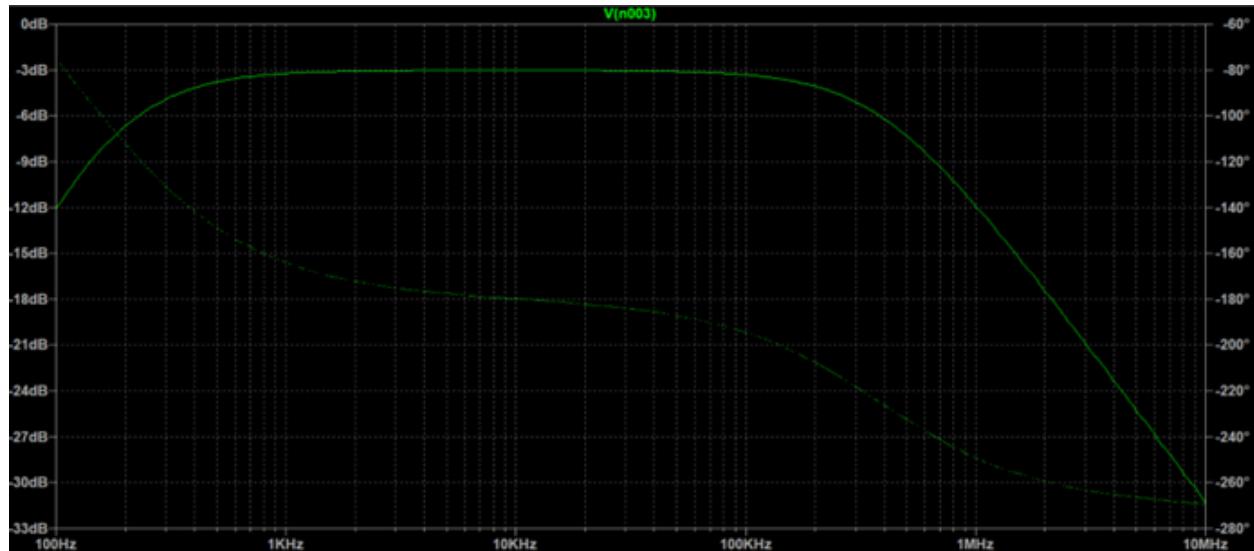
FFT of Output signal:



Upon scrutinizing the input spectra, it is apparent that they all display a singular peak at 10kHz, corresponding to the frequency of our input signal. However, in the output signal spectra, an increase in the number of peaks is observed with the growing amplitude of the input/output signals. In an ideal scenario, there should only be one peak at 1kHz, indicating that the output signal is a straightforward amplification of the input. The existence of additional peaks serves as evidence of distortion in the output signal. This could be due to harmonic distortion.

**5. Perform an AC analysis. Keep the amplitude of the input signal constant at 50mV. Vary the frequency from 100Hz to 1MHz with 10 points per decade and display the voltage across the load resistance  $R_L$ .**





6. Use the LTSpice '.MEASURE' command (see help file and example 'MeasureBW.asc') to determine the lower and upper -3dB frequencies and the bandwidth.

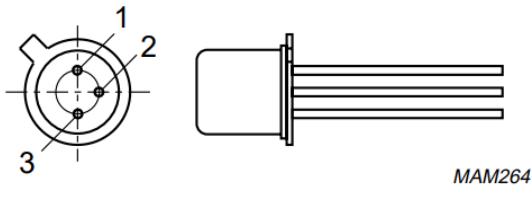
Using the measure function we get: B=384624.86Hz

## Experimental Set-up and Results

### Part 1 - Determine Type and Pin Assignment of a Bipolar Transistor

#### Experimental Setup and Procedure

The goal of the experiment is to identify the type of a BJT (Bipolar Junction Transistor). We label the base pins as in the image (from a bottom view). We first identify the base terminal, then it is possible to identify which type of BJT it is. Finally the emitter and collector terminals are identified.



Multimeter Leads connected to BJT		Diode Check value (reading or .0L)
+ Terminal	Gnd Terminal	—
1	2	
2	1	
1	3	
3	1	
2	3	
3	2	

1. Set the multimeter to diode testing and measure readings between every pair of terminals as in the diagram. The terminals that read **OL** in both polarities will be either the emitter or transmitter, and the remaining terminal is the base terminal.
2. Connect the common lead of the multimeter to base. Then test the other terminals with the positive lead. If the readings both show **OL** then the type is **NPN** else the type is **PNP**. Go to step 1 if this didn't work out.
3. Connect the base and the other terminals in such a polarity that you observe a diode forward voltage drop. Measure and note readings between terminals in a table. The lower reading indicates the collector terminal and the higher reading indicates the emitter.

Transistor Type	
Base Terminal	
Emitter Terminal	
Collector Terminal	

## Results

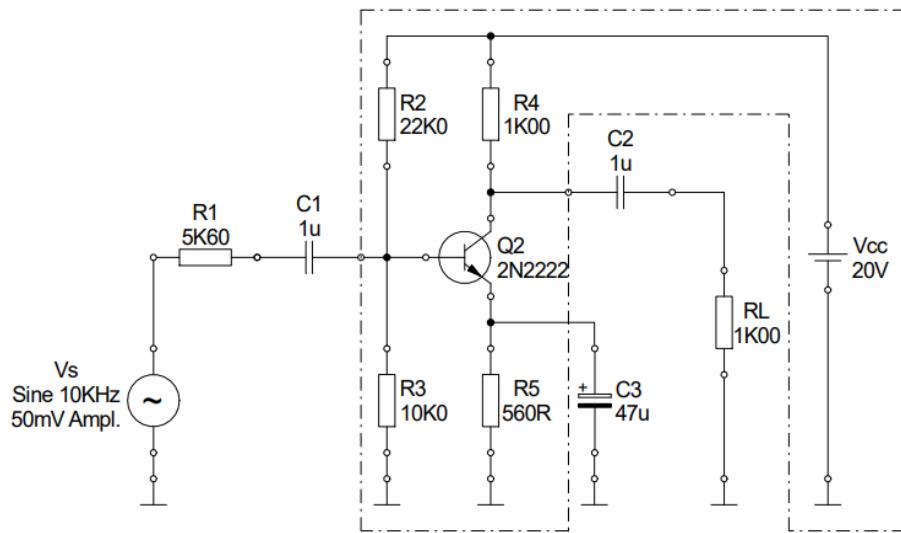
Multimeter Leads Connected to BJT		Diode Check Value
+ Terminal	- Terminal	-
1	2	Overload
2	1	0.742
1	3	Overload
3	1	Overload
2	3	0.741
3	2	Overload

We then figure out that the base terminal is pin 2 and that it is an NPN transistor. Then the identity of the other two pins can be determined.

Transistor Type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

## Part 2 : Operating point of BJTs

### Experimental Setup and Procedure



Assemble the circuit in the dashed area. Our goal is to ensure that the BJT is correctly biased for active operation. Switch on the power supply. Use a multimeter to measure and record the voltages  $V_{CC}$ ,  $V_B$ ,  $V_{BE}$ ,  $V_C$ ,  $V_{CE}$ , and  $V_E$ .  $V_{CC}$  is the voltage indicated in the diagram.

### Results

Measurement	Voltage (V)
$V_{CC}$	20.065
$V_B$	5.968
$V_{BE}$	0.6422
$V_C$	10.584
$V_{CE}$	5.233
$V_E$	5.348

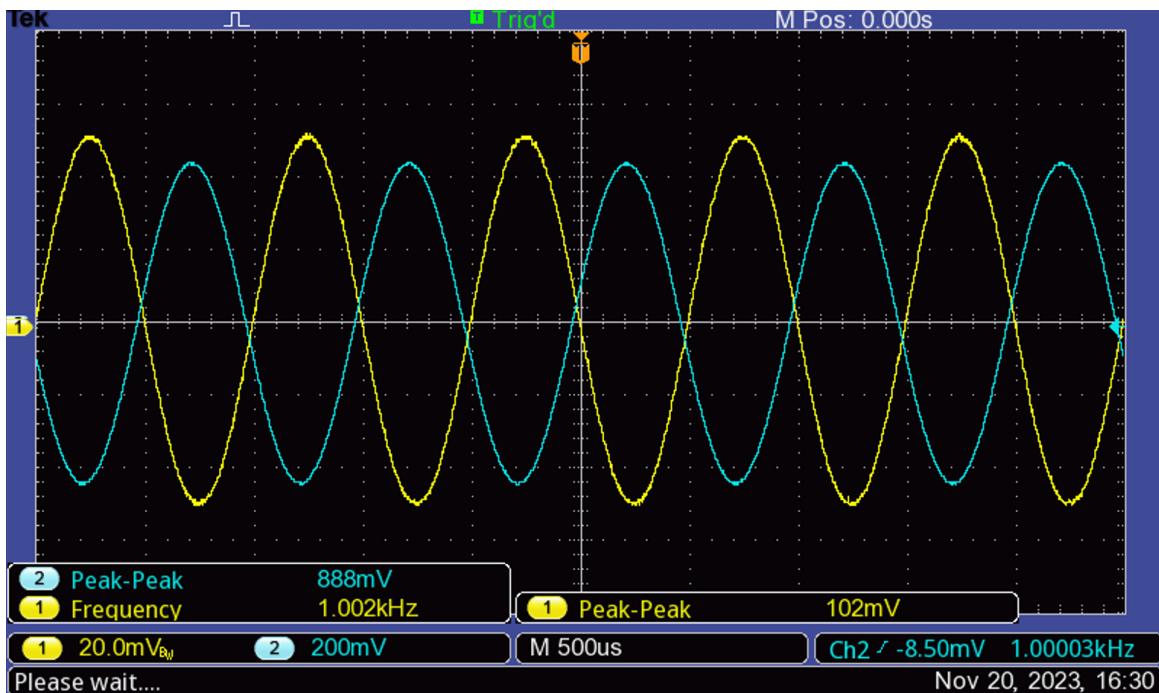
## Part 3 - Common emitter circuit

### Experimental Setup and Procedure

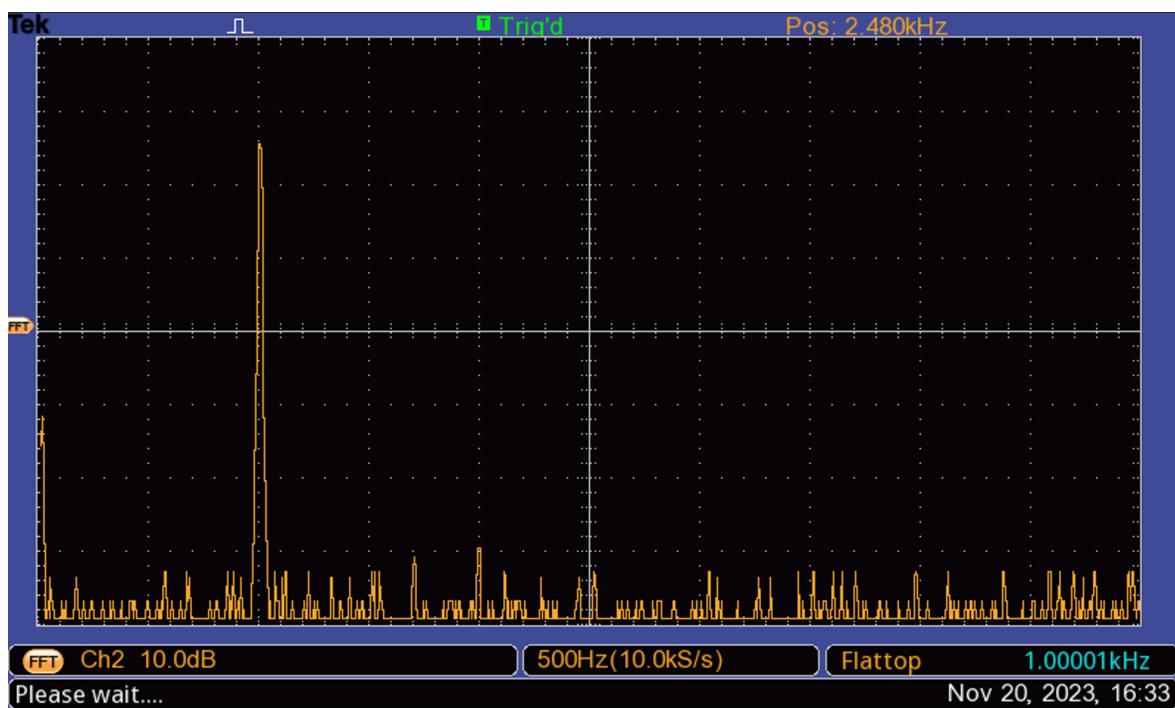
1. Complete the circuit shown in part 2
2. Connect oscilloscope to  $V_S$  over  $R_L$ . Start with input signal  $V_S = 50\text{mV}_{\text{PP}}$  and  $f = 1\text{kHz}$ .
3. Measure  $f$ ,  $V_S$ , and  $V_{RL}$ . Second, get the FFT of  $V_{RL}$ . Use 10 kS/s sampling rate. Take a hardcopy
4. Repeat the two measurements with  $V_S = 100 \text{ mV}_{\text{PP}}$ , and  $V_S = 200 \text{ mV}_{\text{PP}}$

## Results

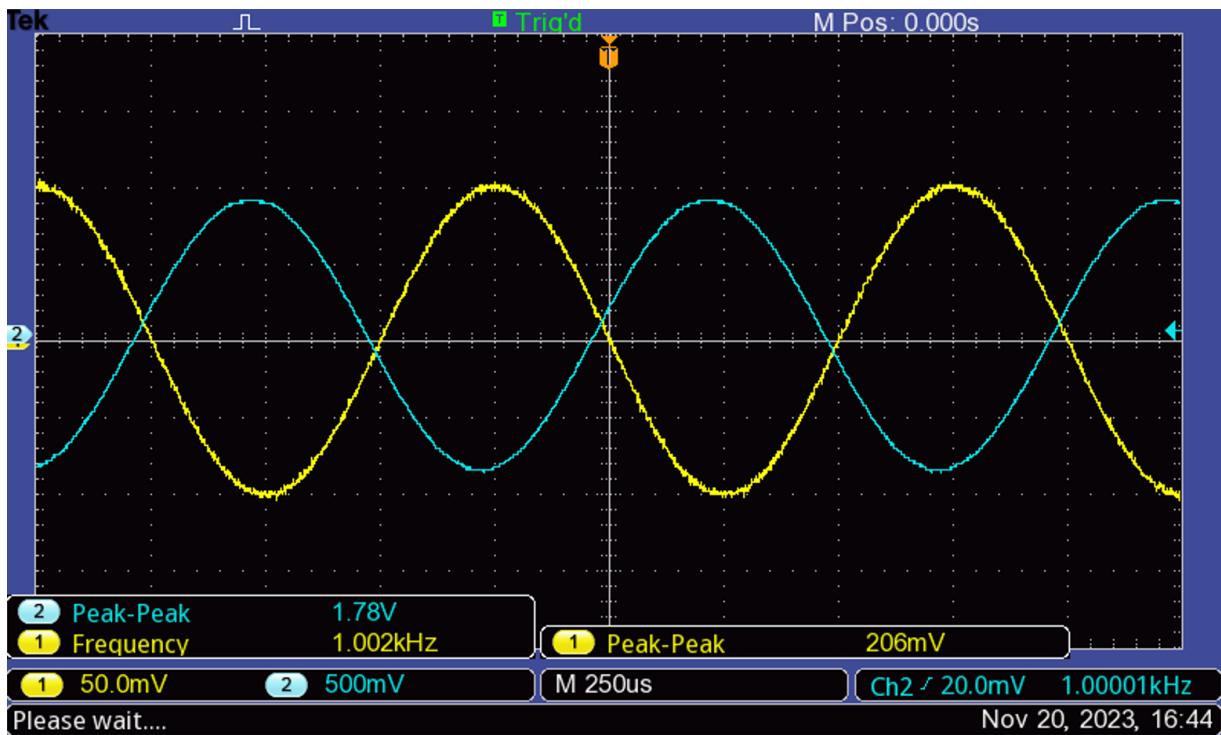
Input signal as 50mV<sub>PP</sub>:



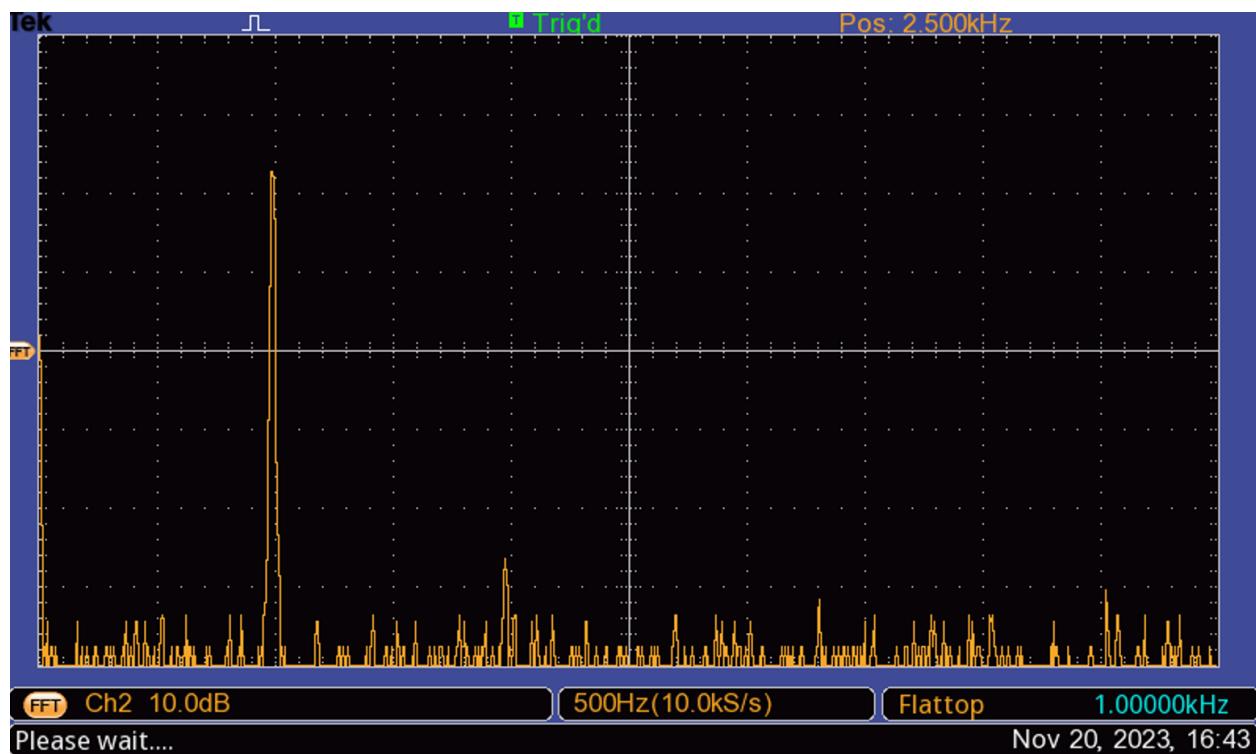
FFT Spectrum with input signal as 50mV<sub>PP</sub>:



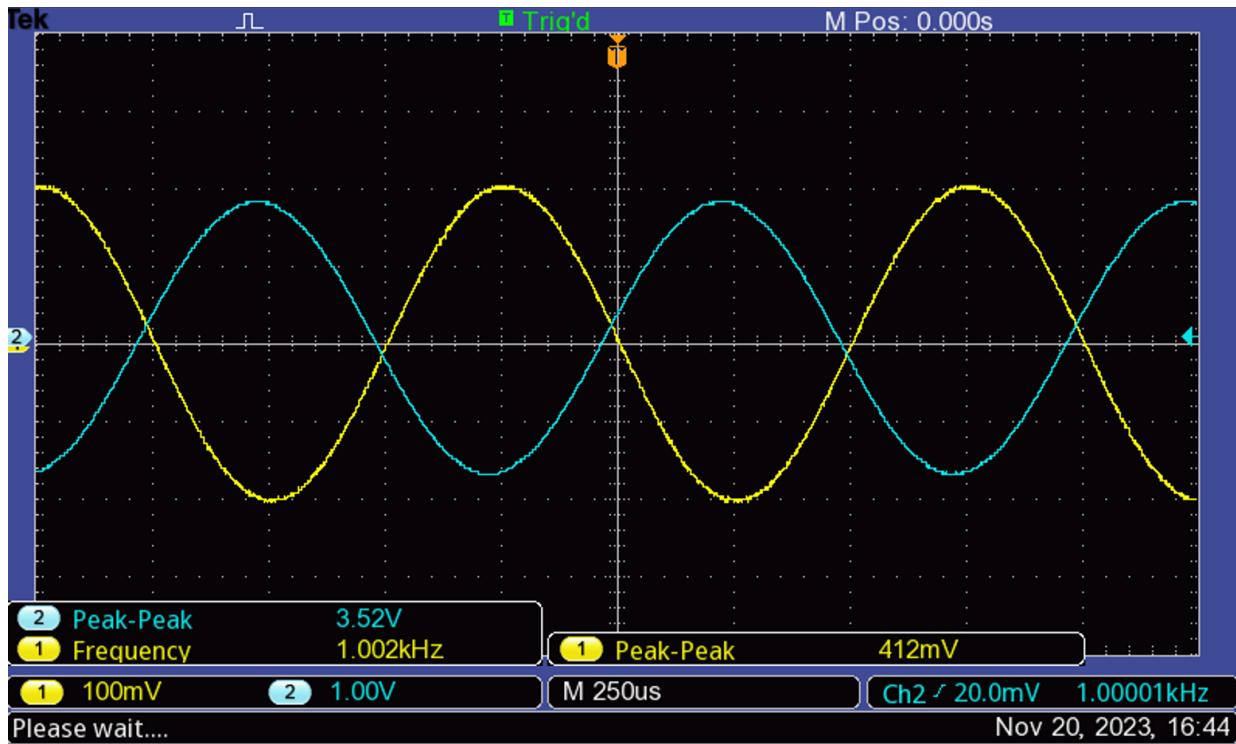
Input signal as 100mV<sub>pp</sub>:



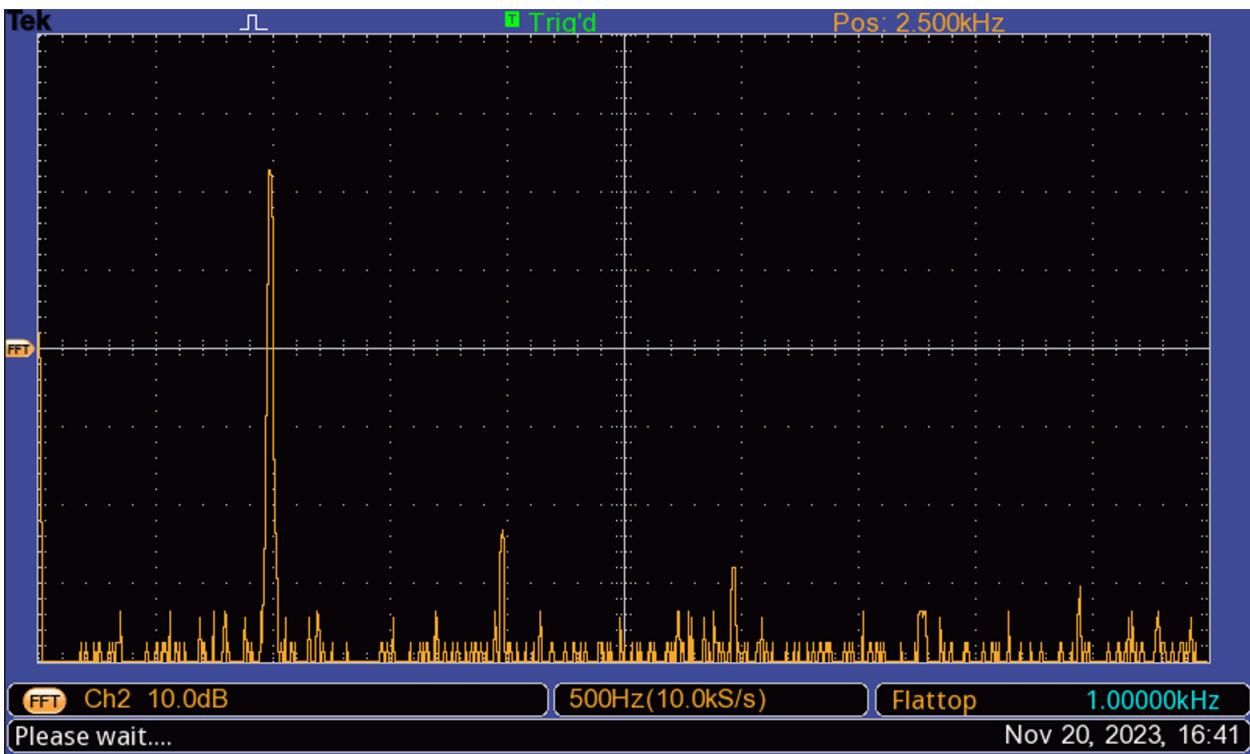
FFT Spectrum with input signal as 100mV<sub>pp</sub>:



Input signal as 200mV<sub>pp</sub>:



FFT Spectrum with input signal as 200mV<sub>pp</sub>:

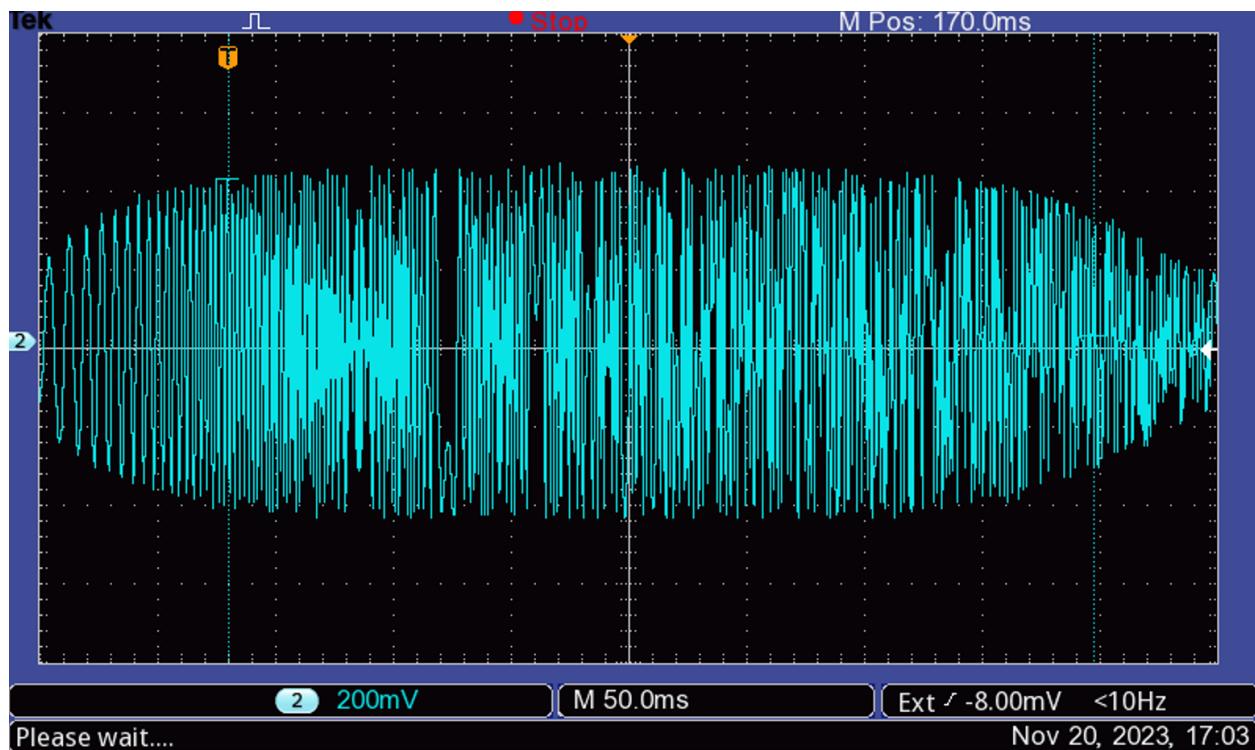


## Part 4 - Bandwidth of amplifier circuit

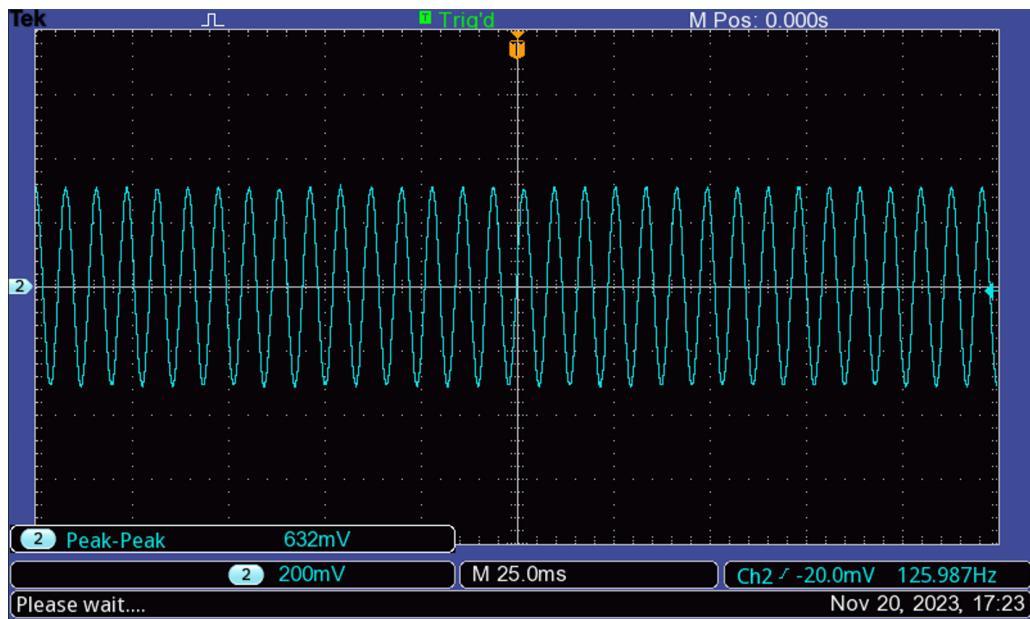
### Experimental Setup and Procedure

1. Using 50 mV peak for  $V_s$ . Enable the sweep mode of the function generator for the following settings:
  - a. START F : 100 Hz
  - b. STOP F : 1 MHz
  - c. SWP TIME : 500 ms
  - d. SWP MODE : logarithmic
2. Adjust the oscilloscope to observe the full sweep of the output signal. Take a hardcopy.
3. Disable the sweep mode of the function generator. Without changing the amplitude of  $V_s$ , manually change the frequency of the function generator to obtain the lower and upper  $-3$  dB cut-off frequencies.

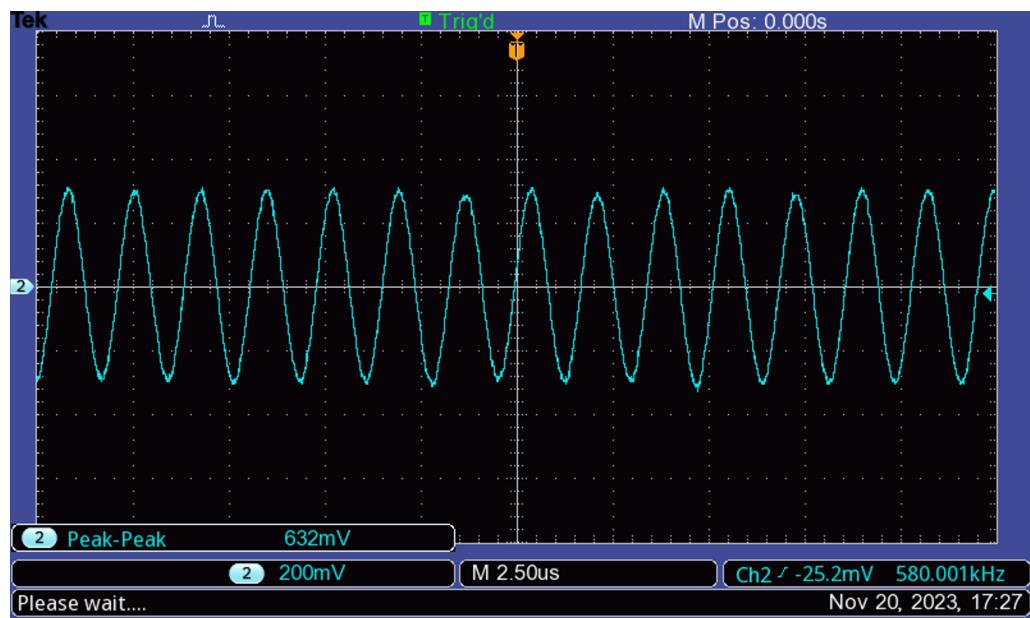
### Results



The upper and lower bounds were obtained by finding when the peak-to-peak voltage had dropped to half of its original value.



Lower Bound: 126Hz



Upper Bound: 580kHz

## Evaluation

### Problem 1 - Determine Type and Pin Assignment of a Bipolar Transistors

1. Explain why the remaining terminal is the base when the other two terminals give overload .0L with both polarities of the multimeter applied?

When the multimeter was connected to the first and third terminals, an Overload reading indicated no direct movement of charge carriers between these two pins. This led to the conclusion that the first and third pins served as the emitter and collector terminals of the transistor. By process of elimination, it was inferred that the second pin corresponded to the base terminal.

2. Explain why Part 1 (2) can be used to determine whether the transistor is 'NPN' or 'PNP'.

We identified the type of transistor by connecting the COM port to the base and the positive port to each of the other terminals. Obtaining an 0L reading for both configurations signified an absence of current flow, leading us to conclude that the transistor was of the NPN type.

3. Explain why Part 1 (3) can be used to determine the collector and the emitter terminals.

The emitter, having a higher doping concentration than the collector, resulted in disparate base-terminal voltages. Our measurements revealed that one voltage was higher than the other. Considering the heavier doping in the emitter, we inferred that the elevated base-terminal voltage indicated the base-emitter voltage, identifying the corresponding terminal as the emitter and the other as the collector.

## Problem 2 - Operating point of BJTs

1. Compare the measured values with the theoretical ones. Discuss the differences.

Parameter	Simulation Value (V)	Experimental Value (V)
$V_{CC}$	—	20.065
$V_B$	5.663	5.968
$V_{BE}$	0.8297	0.6422
$V_C$	11.455	10.584
$V_{CE}$	6.623	5.233
$V_E$	4.833	5.348

The experimental data closely aligns with the simulated data, with differences potentially arising from various factors. Tolerance in components, such as the 10% tolerance in the transistor and variations in the actual transistor used compared to the simulated one, can contribute to discrepancies. Additionally, errors introduced during signal supply from the generator, the resolution of the oscilloscope, and the inherent errors associated with cursor measurements and measurements using the measure function all play a role. Cumulatively, these errors deviate the final experimental values from those obtained under ideal conditions.

2. Calculate the common emitter current gain  $\beta$ . Use only measured values!

$$V_{R4} = V_{CC} - V_{CE} - V_E$$

$$V_{R4} = 20.065 - 5.233 - 5.348 = 9.484V$$

$$I_C = \frac{V_{R4}}{R_4} \text{ and } I_E = \frac{V_E}{R_5} \text{ and } I_B = I_E - I_C \text{ and } I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B} = \frac{\frac{V_{R4}}{R_4}}{\frac{V_E}{R_5} - \frac{V_{R4}}{R_4}} = 143.70$$

**3. Determine the error sources with approximate values and CALCULATE the relative error of the calculated  $\beta$ . Check the plausibility of your previous calculated value by comparing it to the simulation. If the error is too high what is the reason and is there a way to avoid it?**

$$\beta_{simulated} = \frac{I_C}{I_B} = \frac{0.00854}{0.00008544} = 99.95$$

$$\Delta I_B = 1.44 \cdot 10^{-5} A$$

$$\Delta I_C = 1.09 \cdot 10^{-3} A$$

$$\Delta \beta = \left| \frac{\partial}{\partial I_C} \left( \frac{I_C}{I_B} \right) \cdot \Delta I_C \right| + \left| \frac{\partial}{\partial I_B} \left( \frac{I_C}{I_B} \right) \cdot \Delta I_B \right| = 18.10$$

$$\beta_{rel\ error\ expected} = \frac{\Delta \beta}{\beta} = 13.37\%$$

$$\beta_{rel\ error\ actual} = \frac{|\beta_{experimental} - \beta_{simulated}|}{\beta_{simulated}} = 43.76\%$$

The circuit comprises diverse components, including capacitors, resistors, and a signal generator, each with a specific tolerance unaccounted for in our calculations. Additionally, utilizing the oscilloscope's measurement function introduces a 5% error, while measurements using the cursor exhibit approximately a 10% error. Our experimental setup involved a transistor different from the one used in the simulation, resulting in varied characteristics. Consequently, errors from these parameters collectively contribute to the significant error observed in our calculations.

To mitigate these errors, using the same transistor as in the simulations and employing an oscilloscope with enhanced resolution can be beneficial.

### Problem 3 - Common emitter circuit

- 1. In what region of the output characteristic is the circuit for a distorted positive or negative amplitude? Explain!**

The distorted positive amplitude occurs in the saturation region, stemming from a significant increase in the base current until the base-emitter junction is no longer forward-biased.

Simultaneously, the distorted negative amplitude arises in the cut-off region. Without this, the output signal would replicate the input with a larger gain, but instead, an inverted waveform is observed due to the conditions in the cut-off region.

- 2. Using the measurements taken in the lab, calculate the voltage gain  $A_V$  of the amplifier. Compare to simulations.**

$$A_V = \frac{V_{out}}{V_{in}}$$

$$A_{V=50} = \frac{1776}{102} = 17.41$$

$$A_{V=100} = \frac{1780}{206} = 17.28$$

$$A_{V=200} = \frac{3.52}{412} = 17.09$$

$$A_{V sim} = \frac{700.21}{49.93} = 14.02$$

Based on the calculations, we observe that the gain calculated from the first dataset is closest to the gain from the simulated data, indicating a deviation of approximately 10%. Similarly, the gain calculated from the last experiment is closest to the simulated gain, with an observed error of about 15%. These deviations could be attributed to similar errors discussed in previous problems.

**3. Determine from the hard copies, what is the phase relationship between the input and the output signals? Explain the reason for such a relation.**

In the saturation region, the distorted positive amplitude emerges due to an increase in base current. Upon examining hard copies, a  $180^\circ$  phase difference between the input and output is evident, as the output signal is inverted. This inversion results from the heightened base current leading to increased collector current, causing a larger voltage drop across R4 and consequently reducing the output voltage. The operational disparity indicates that the output signal undergoes a change opposite to that of the input, contributing to the observed phase shift.

**4. Compare the FFTs with the different input signals to the simulation.**

In both the simulation and experiment, an increase in the amplitude of the input signal led to a higher number of peaks in the output. The FFT of the input signal displayed a single peak, indicating a pure sinusoidal signal at 1 kHz. However, the output was not a simple amplification of the input; it underwent distortion during the amplification process, resulting in harmonic distortion. The harmonic distortion occurs due to nonlinearities in the amplification process, causing the output to include harmonics or multiples of the fundamental frequency. As a result, the output represented a combination of multiple sinusoidal signals with different frequencies, contributing to the observed harmonic distortion. Consequently, the FFT Spectrum for the output in both experimental and simulated cases exhibited multiple peaks at different frequencies, reflecting the complex nature of the output comprising various sinusoids with diverse frequencies.

## Problem 4 - Bandwidth of amplifier circuit

### 1. In Part 4 (2), explain your observation.

In this part, we conducted an observation of the complete range displayed on the oscilloscope, leading to the generation of a Bode Plot representation. The Bode Plot reveals that the circuit exhibits low gain at both low and high frequencies, characteristic of a bandpass filter. The attenuation at higher frequencies is attributed to the Miller Effect, caused by the parasitic capacitance of the amplifier acting as a limiting factor for the gain. Conversely, the attenuation at lower frequencies results from the high impedance of the capacitor. Since the capacitor is in parallel to RL in the circuit, a smaller portion of the output is directed to RL due to voltage division.

### 2. Using the measurements made in the lab, calculate the amplifier bandwidth.

$$B = 580000 - 126 = 579874\text{Hz}$$

### 3. Compare to the simulation! What are the reasons for the different cutoff frequencies?

From the simulation, the obtained bandwidth is 384624.86Hz. When contrasting the experimental findings with the simulated results, a significant deviation in bandwidth is observed. This discrepancy can be attributed to various factors, primarily the tolerances of components, resolution errors, precision errors, and equipment errors. Another potential factor could be the impact of the circuit's design on the breadboard, as the compact nature of our design might have influenced the resulting cut-off frequency of the signal.

## Conclusion

In this comprehensive laboratory exploration focused on Bipolar Junction Transistors (BJTs) and their practical applications, we navigated through theoretical understandings, simulations, and practical implementations. The prelab activities involved solving BJT circuits to extract parameters, conducting simulations to compare theoretical and simulated data, and constructing a constant current source with a Zener diode. Theoretical principles, datasheets, and simulations were utilized for analysis and validation.

Simulations on LTSpice included amplifier circuits with operating point analyses, DC sweeps, FFT spectrum analysis, and Bode Plots. The observed distortion in the output signals and the increase in the number of peaks in the FFT spectrum with higher input amplitudes provided insights into amplifier behavior. The AC analysis revealed the bandpass filter characteristics of the circuit, with the Miller Effect causing suppression at higher frequencies and capacitor impedance influencing lower frequencies.

In the experimental phase, we determined transistor characteristics, built circuits on a breadboard, and conducted operating point analyses. The amplifier circuit exhibited similar distortion patterns as observed in simulations, validating theoretical concepts. Experimental evaluation highlighted discrepancies from simulations, attributing them to component tolerances, equipment errors, and the impact of circuit design on the breadboard.

Overall, this lab journey equipped us with a holistic understanding of BJT circuits, spanning theoretical foundations, simulations, and practical applications such as amplification, distortion analysis, and frequency response. The integration of theoretical insights with hands-on experimentation fostered a deeper appreciation for the complexities and practical considerations involved in electronic circuit design.

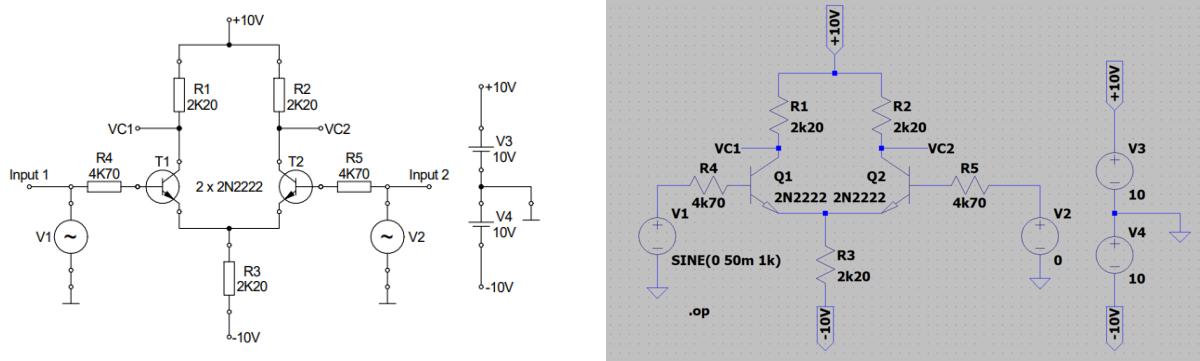
## References

Pagel, Uwe. *CO-526-B Electronics Lab Manual*. 2023.

## Appendix

### Prelab - Operational Amplifier

#### Problem 1 - Differential amplifier using a fixed emitter resistor



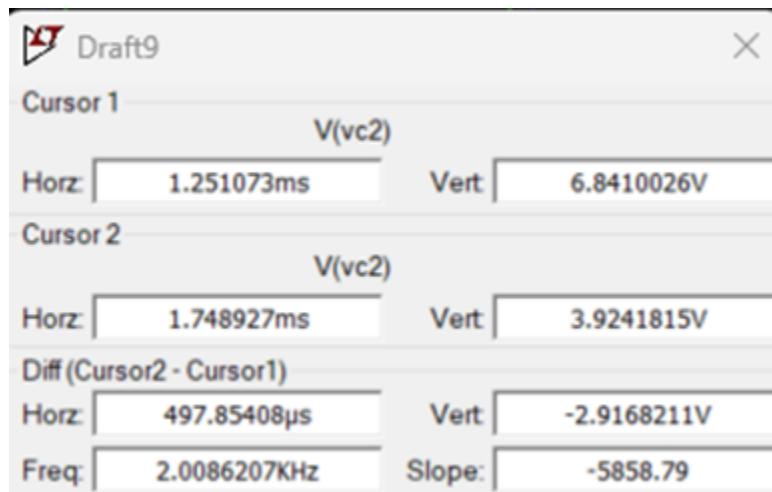
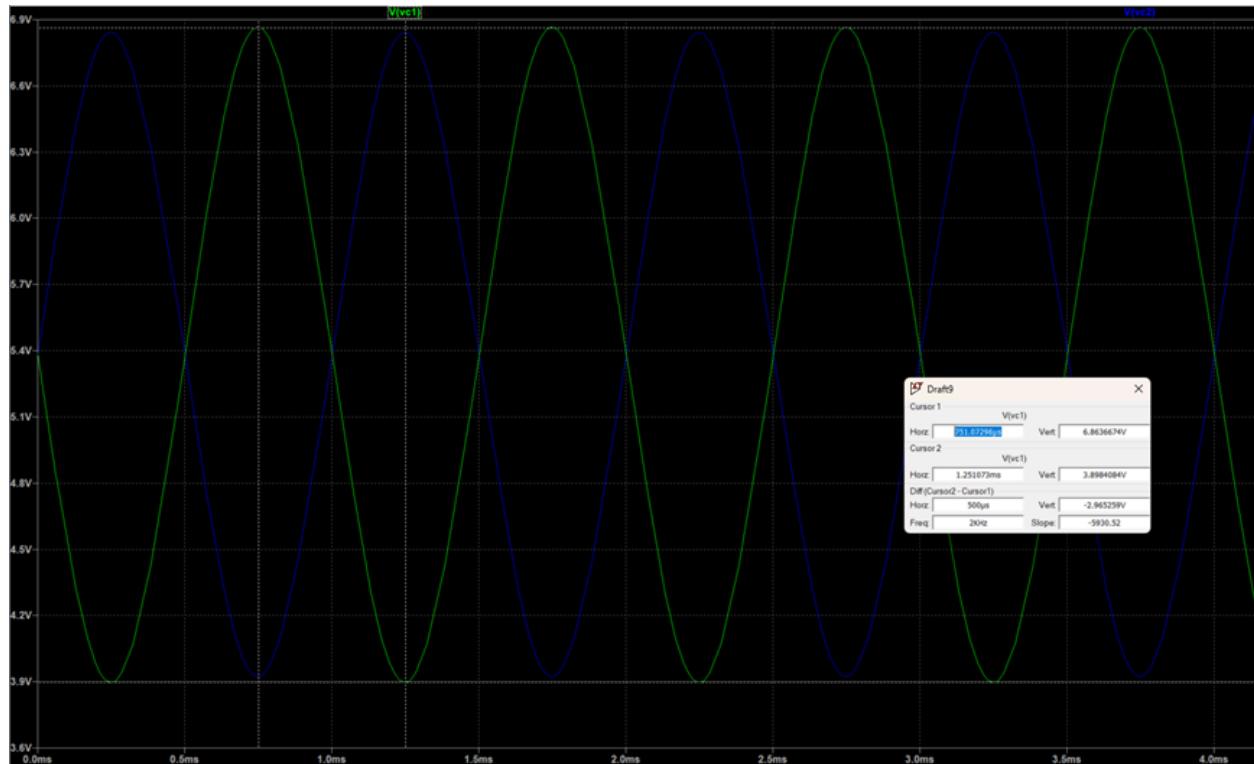
1. Perform a DC operation point analysis for the above circuit. Determine the values for  $V_{BE}(T_1, T_2)$ ,  $V_C(T_1, T_2)$ ,  $I_C(T_1, T_2)$ ,  $I_E(T_1, T_2)$ , and  $I_{RE}$ . What would happen with the values in the two branches if the transistors are not absolutely identical.

	T1	T2
$V_{BE}$	673.62mV	673.62mV
$V_C$	5.38	5.38
$I_C$	2.10mA	2.10mA
$I_E$	-2.11mA	-2.11mA
$I_{RE}$	4.22mA	4.22mA

2. Perform a transient analysis. Use single-ended input mode. Set  $V_1$  at input 1 to Sine,  $f = 1\text{kHz}$ ,  $\hat{u} = 50\text{mV}$ , and  $V_2$  at input 2 to GND. Display and measure the two collector voltages! Calculate  $A_{V_{diff}}$  in dB.

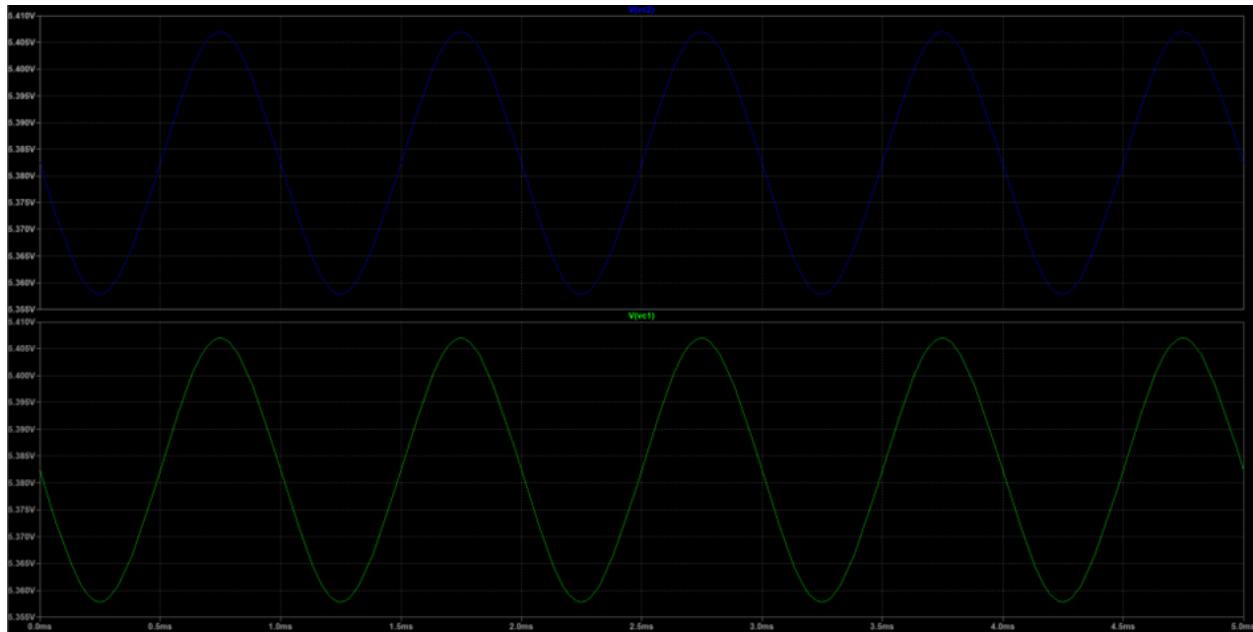
By utilizing the cursors, we extract the peak-to-peak difference in  $V_{out}$ , and subsequently, we determine the gain:

Experiment 3 - BJT  
 Lab Report 2 - Abhigyan Deep Barnwal



$$dB A_{vdiff} = 20 \log \left( \frac{2.92}{0.1} \right) = 29.30 dB$$

**3. Perform a simulation with common mode input. Set  $V_1$  and  $V_2$  at input 1 and 2 to Sine,  $f = 1\text{kHz}$ ,  $\hat{u} = 50\text{mV}$ , and  $V_2$  to Gnd. Display and measure the two collector voltages. Calculate  $A_V$  in dB.**



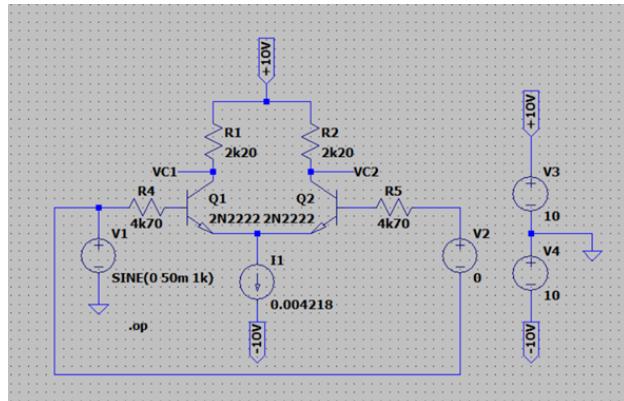
$$dBA_{vcm} = 20\log\left(\frac{45.68}{0.1}\right) = (-6.81)\text{dB}$$

**4. Calculate the common-mode rejection ratio in dB**

$$CMRR = 20\log\left(\frac{A_{vdiff}}{A_{vcm}}\right) = 36.16\text{dB}$$

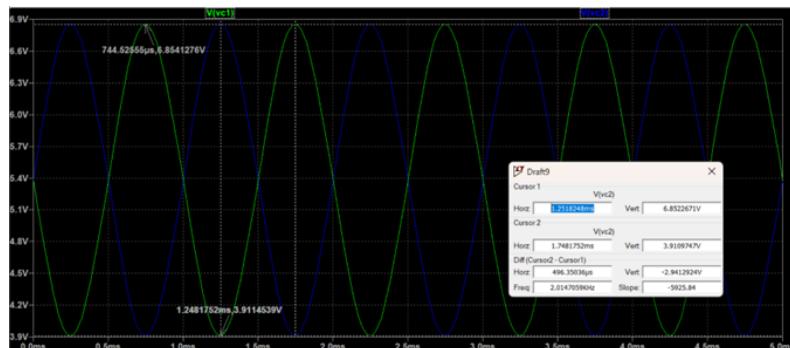
5. Replace the resistor  $R_3$  with a current source. Use the same current you got from the .op analysis in step 1 for  $I_{R3}$ . Repeat steps 1 - 4 for the new circuit.

Step 1 - Replacing the resistor and running the DC point analysis:



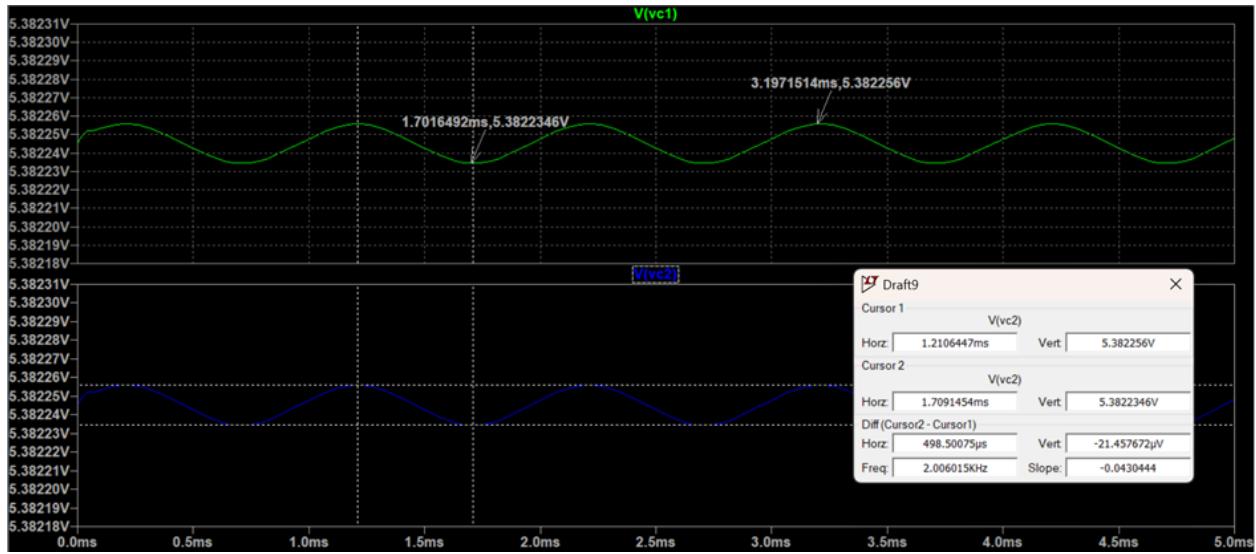
	T <sub>1</sub>	T <sub>2</sub>
V <sub>be</sub>	673.62mV	673.62mV
V <sub>c</sub>	5.38V	5.38V
I <sub>c</sub>	2.10mA	2.10mA
I <sub>e</sub>	2.11mA	2.11mA
I <sub>re</sub>	4.22mA	4.22mA

Step 2 - Performing transient analysis to get  $A_{vdif}$ :



$$dB A_{vdif} = 20 \log\left(\frac{2.94}{0.1}\right) = 29.37 dB$$

Step 3 - Simulation with common mode input to get  $A_{vcm}$ :

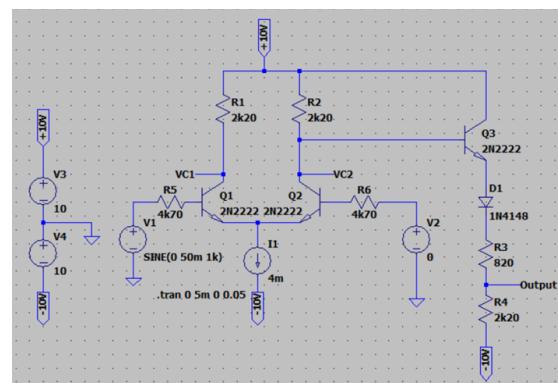
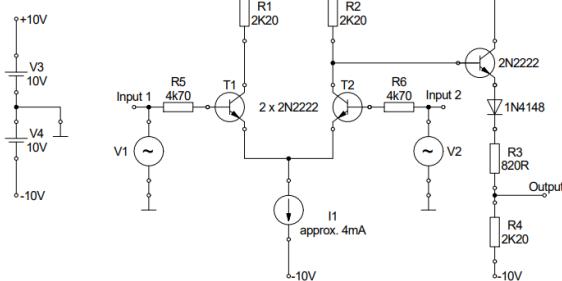


$$dB A_{vcm} = 20 \log \left( \frac{21.48 \cdot 10^{-6}}{4.28 \cdot 10^{-5}} \right) = (-5.99) dB$$

Step 4 - Calculating the CMRR

$$CMRR = 20 \log \left( \frac{A_{vdiff}}{A_{vcm}} \right) = 35.36 dB$$

## Problem 2 - Construct an OP-Amp



- 1. Calculate the voltage at the output of the emitter follower when both inputs are connected to ground. Assume  $\beta = 200$  and  $U_{BE} = 0.7V$ . The forward voltage drop of the diode is 0.7V.**

$$I_{C2} = I_{E2} = \frac{I_1}{2} = 2mA$$

$$V_{CB} = V_{R2} = I_{C2} R_2 = 4.4V$$

$$V_{CE} = V_{CB} + V_{BE} = 5.2V$$

$$I_{E3} = 4.70mA$$

$$V_{out} = 0.34V$$

2. Perform a dc operation point analysis. Determine the output voltage and compare to your calculation.

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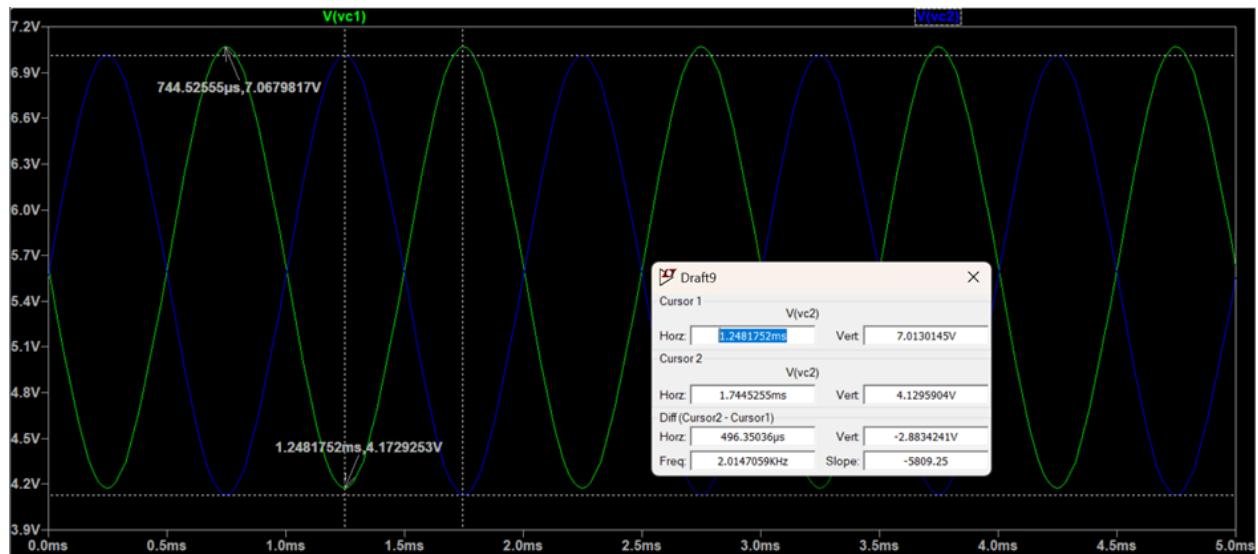
--- Operating Point ---

$V(n002)$ :	0	voltage
$V(n003)$ :	-0.0445579	voltage
$V(vc1)$ :	5.61987	voltage
$V(n006)$ :	-0.71672	voltage
$V(vc2)$ :	5.57175	voltage
$V(n004)$ :	-0.044558	voltage
$V(+10v)$ :	10	voltage
$V(n005)$ :	0	voltage
$V(-10v)$ :	-10	voltage
$V(n001)$ :	4.87625	voltage
$V(n007)$ :	4.2192	voltage
$V(output)$ :	0.358357	voltage
$Ic(Q3)$ :	0.00468557	device_current
$Ib(Q3)$ :	2.27702e-005	device_current
$Ie(Q3)$ :	-0.00470834	device_current
$Ic(Q2)$ :	0.00199007	device_current
$Ib(Q2)$ :	9.48043e-006	device_current
$Ie(Q2)$ :	-0.00199955	device_current
$Ic(Q1)$ :	0.00199097	device_current
$Ib(Q1)$ :	9.48041e-006	device_current
$Ie(Q1)$ :	-0.00200045	device_current
$I(D1)$ :	0.00470834	device_current
$I(I1)$ :	0.004	device_current
$I(R4)$ :	0.00470834	device_current
$I(R3)$ :	0.00470834	device_current
$I(R6)$ :	9.48043e-006	device_current
$I(R2)$ :	0.00201284	device_current
$I(R1)$ :	0.00199097	device_current
$I(R5)$ :	-9.48041e-006	device_current
$I(V4)$ :	-0.00870834	device_current
$I(V3)$ :	-0.00868938	device_current
$I(V2)$ :	-9.48043e-006	device_current
$I(V1)$ :	-9.48041e-006	device_current

Our simulated result ( $V_{out} = 0.36V$ ) is then very close to theory (0.34V)

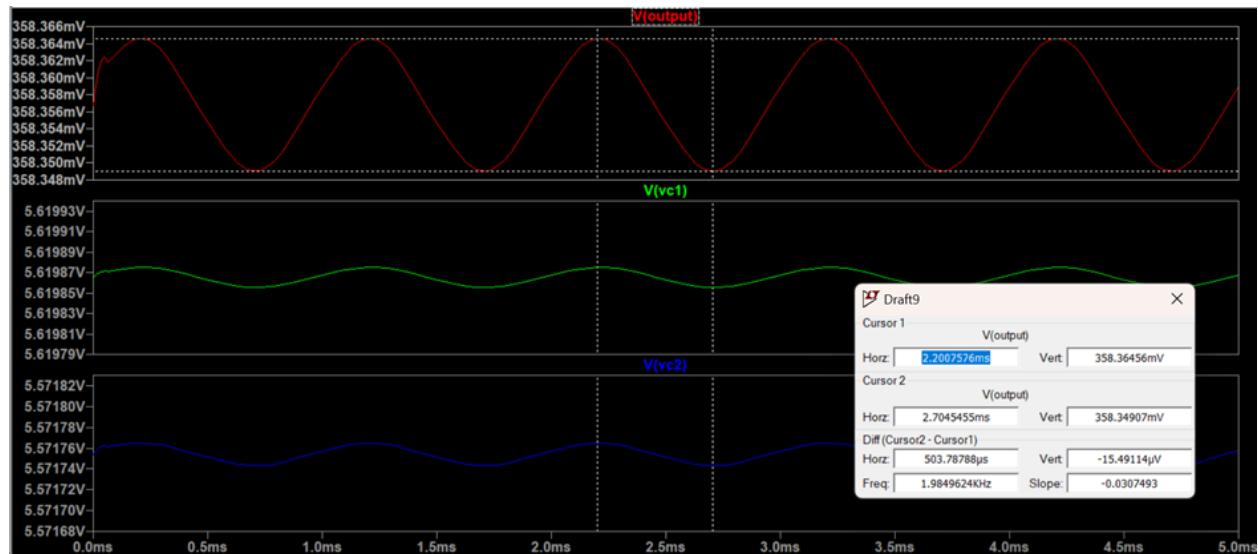
### 3. Determine $A_{V_{diff}}$ , $A_{V_{cm}}$ , and the common-mode rejection ratio in a similar way like in problem 1.

Step 1 - Performing transient analysis to get  $A_{V_{diff}}$ :



$$dBA_{V_{diff}} = 20 \log\left(\frac{2.88}{0.1}\right) = 29.20dB$$

Step 2 - Simulation with common mode input to get  $A_{V_{cm}}$ :



$$dBA_{V_{cm}} = 20 \log\left(\frac{1.55 \cdot 10^{-5}}{0.1}\right) = (-79.20)dB$$

### Step 3 - Calculating CMMR

$$CMRR = 20 \log\left(\frac{A_{vdiff}}{Avcm}\right) = 35.36dB$$

#### 4. What is the inverting and what is the non inverting input?

From the simulation, we see that the output is inverted for an input  $V_2$ . Therefore,  $V_2$  is the inverting input.

Note: Experiment 4 was not performed due to medical absence.