10bit_750M_SAR

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1. post-simulation

corner: tt

	THIS WORK
architecture	SAR
Technology	28nm
Sampling rate	750MS/s
Resolution	10bits
Supply	0.9V
Input Swing	1.26V
SNDR	55.78dB
Power	2.655mW

In other corners, the structure can work normally.

2. Details of layout

CELL NAME	LAYOUT
SH_Comb_Converter_V2	layout4
SAR_Core_v1	layout2
SAR_Converter_v1_layout	layout5
Comparator_Buffer_v1	layout
Logic_SAR_dynamic_layout_V2	layout_v1, layout
SAR_Cap_DAC_layout	layout
bootstrap_switch_v1	layout1

Notes:

> - *Logic_SAR_dynamic_layout_V2: layout_v1 has no voltage and layout has it.*
> - *SAR_Cap_DAC_layout: schematic needs checking LVS and schematic_ideal is used in just schematic*

3. Extra messages

When the power supply equals 0.9V, the maximum sampling rate is 760MS/s

When the power supply equals 0.93V, sampling rate is up to 800MS/s

4. Some advice

> - *change some vlt transistor with ulvt transistor, which includes inverters of CDAC and dynamic logic.*

5. version

VERSION	CHANGE	TIME AND AUTHOR
V1	add 4.some advice	1.8.2024 Jingxiang