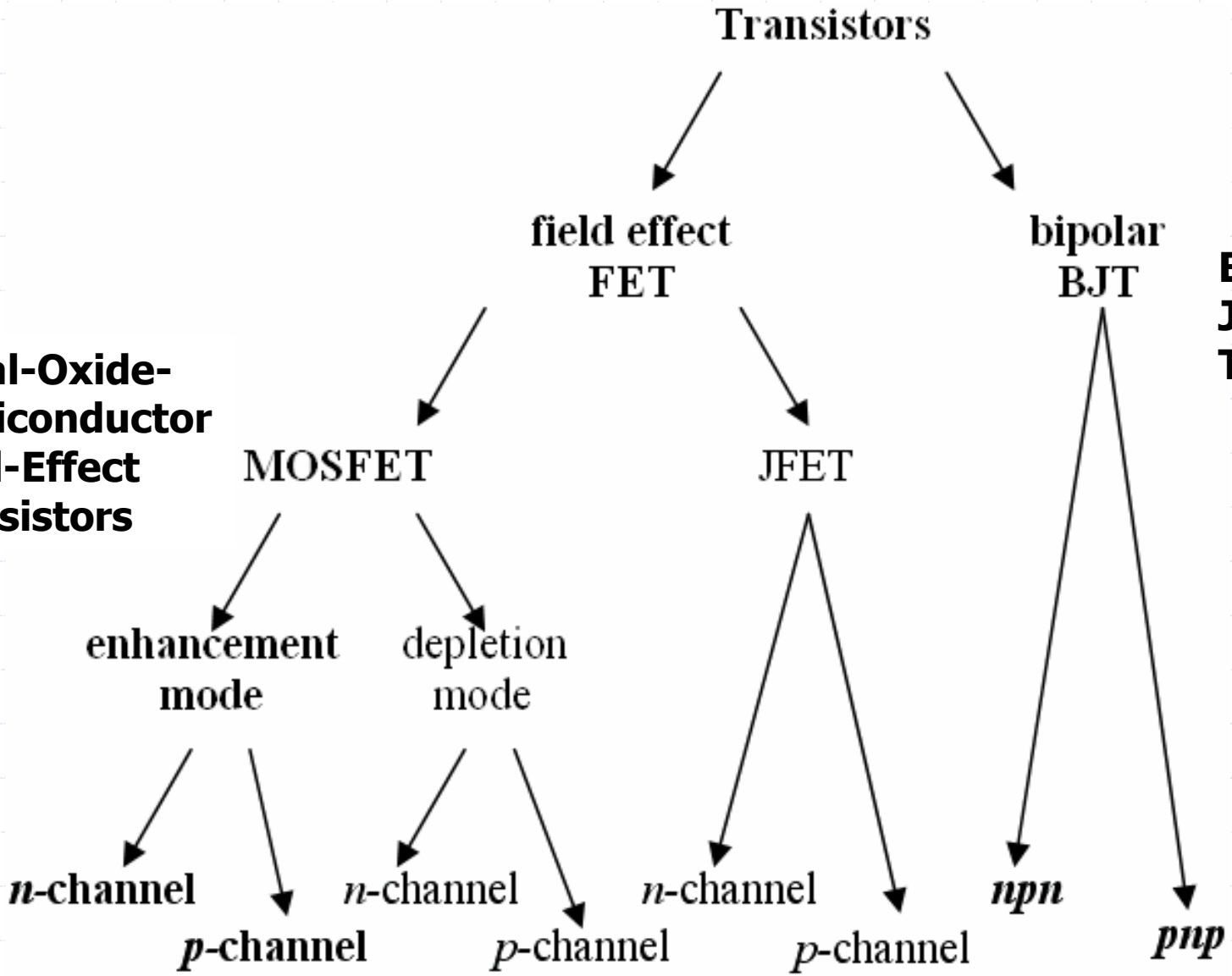
Transistor Digital Circuits

TRANSISTORS

- **active** semiconductor devices (with three terminals)
- Operating **principle**: using a **voltage** between two terminals (command) **to control the current** through the third terminal.
- Transistors: ***voltage-controlled current sources***

- transistors: essential components of every electronic circuit
- Pentium 4 microprocessors : ~ 43,5 milion field effect tranzistors
- for the next Intel microprocessors a billion of transistors are anticipated

Transistor types



Metal-Oxide-Semiconductor Field-Effect Transistors

Bipolar Junction Transistors

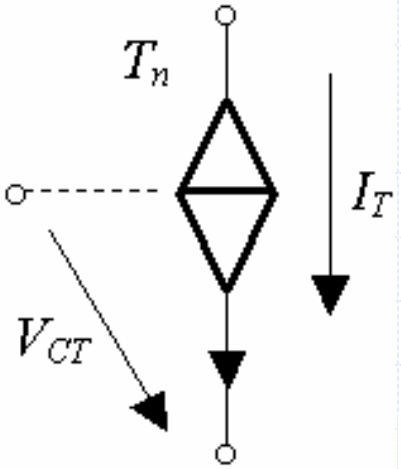
Operating principle and regions

Transistor – controlled current source

- DC model – ideal voltage controlled current source

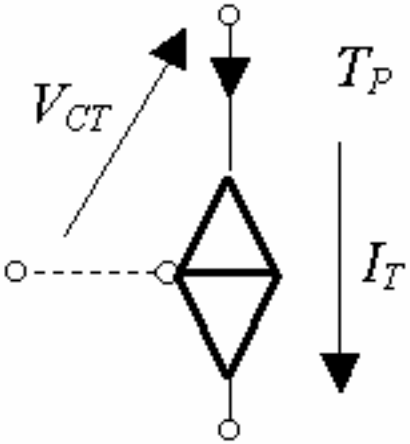
n-type

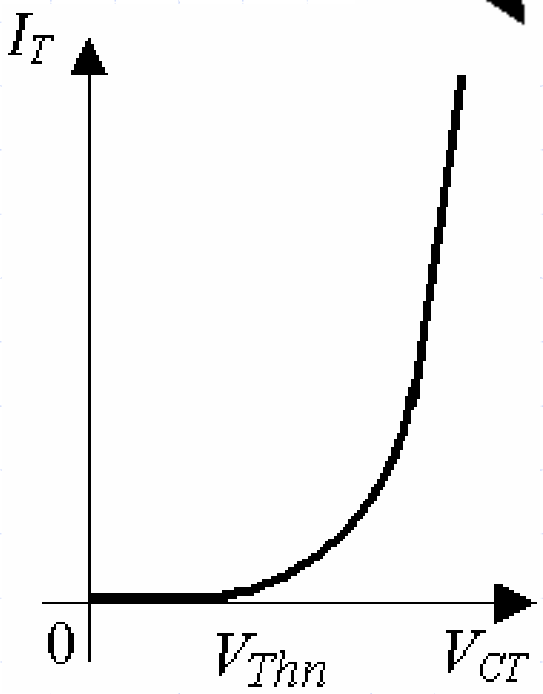
- *n* -channel MOSFET
- *npn* BJT

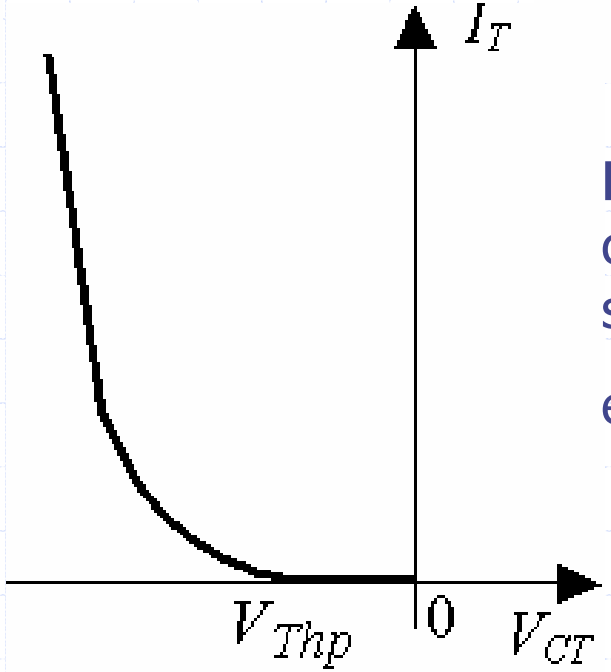


p-type

- *p-channel* MOSFET
- *pnp* BJT





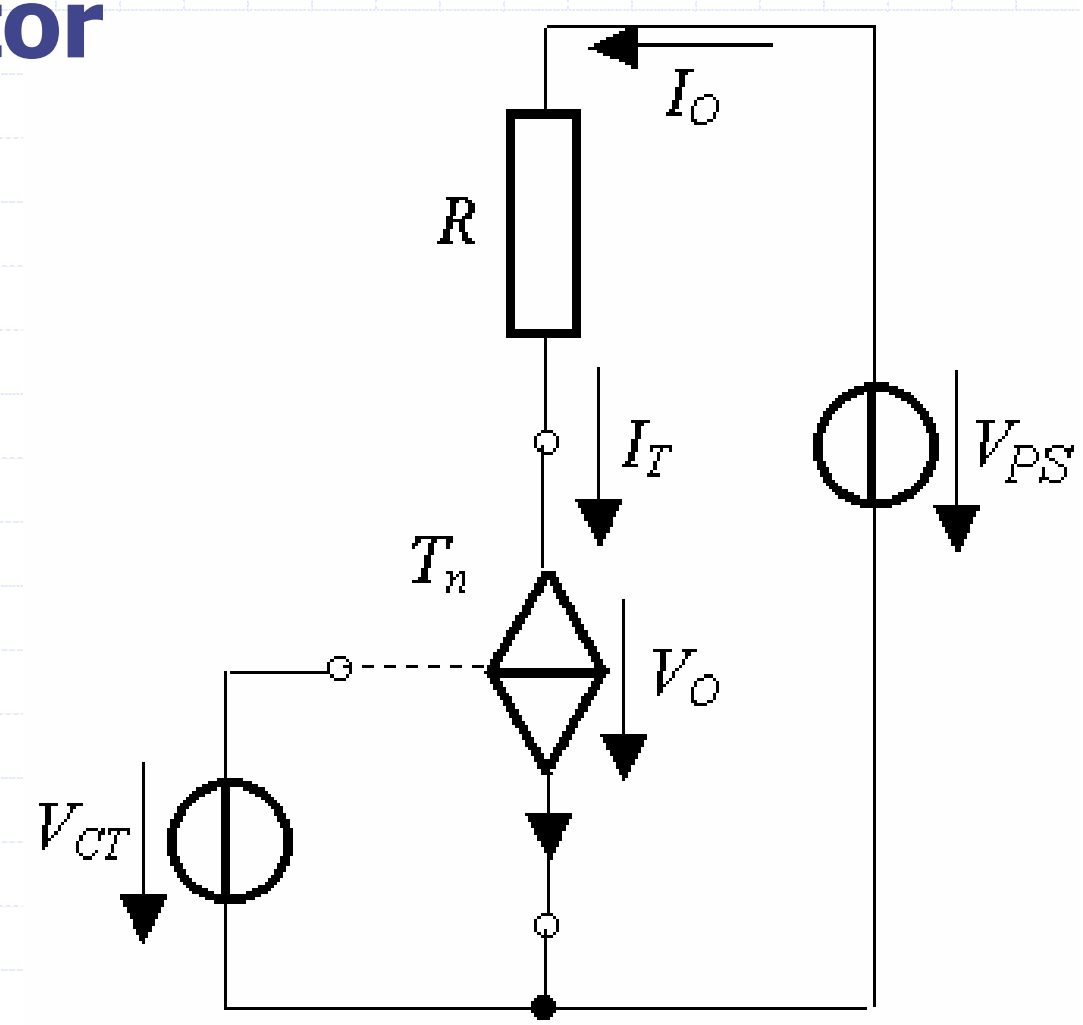


Non-linear controlled sources:
square - MOSFET

exponential – BJT

Using T_n transistor

Why is R necessary ?
Output quantities: I_O, V_O
transfer characteristics:
$I_O(V_{CT})$, $V_O(V_{CT})$



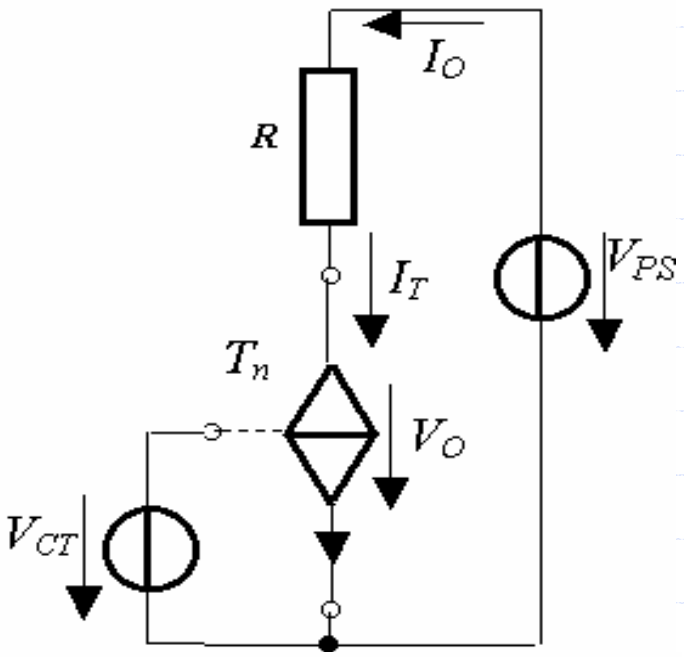
Transfer Characteristics

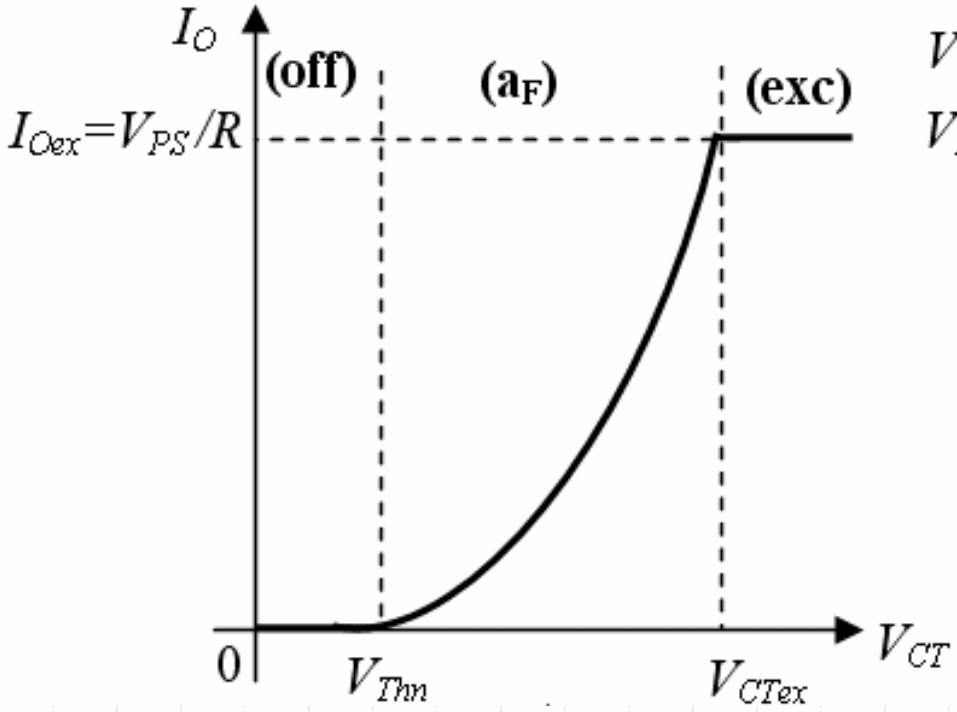
- $V_{CT}<V_{Thn}$, T_n – off, $I_O=I_T=0$
- $V_{CT}>V_{Thn}$, T_n – on, $I_O=I_T>0$

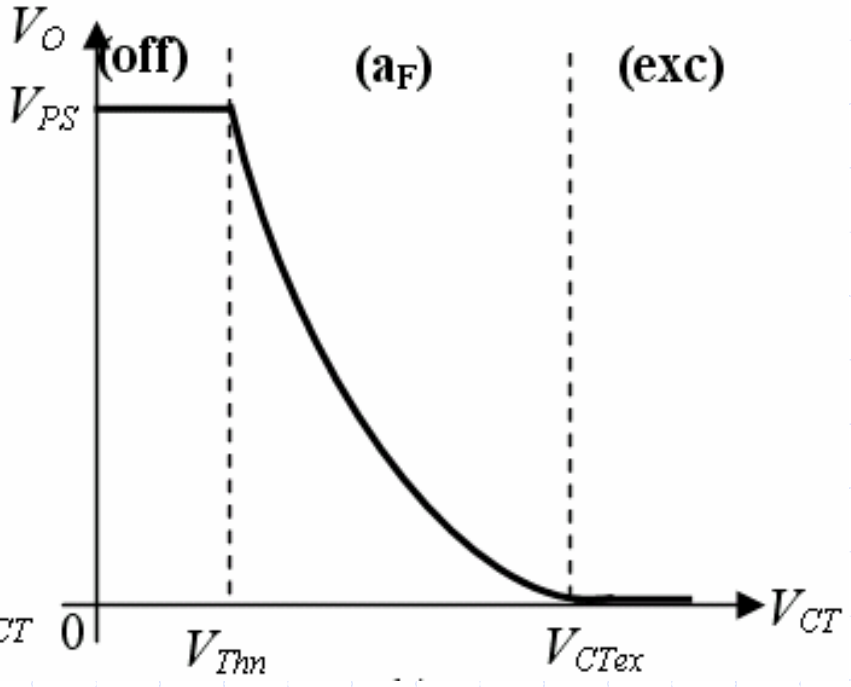
$V_{PS}=RI_O+V_O$; $V_O= V_{PS}- RI_O$

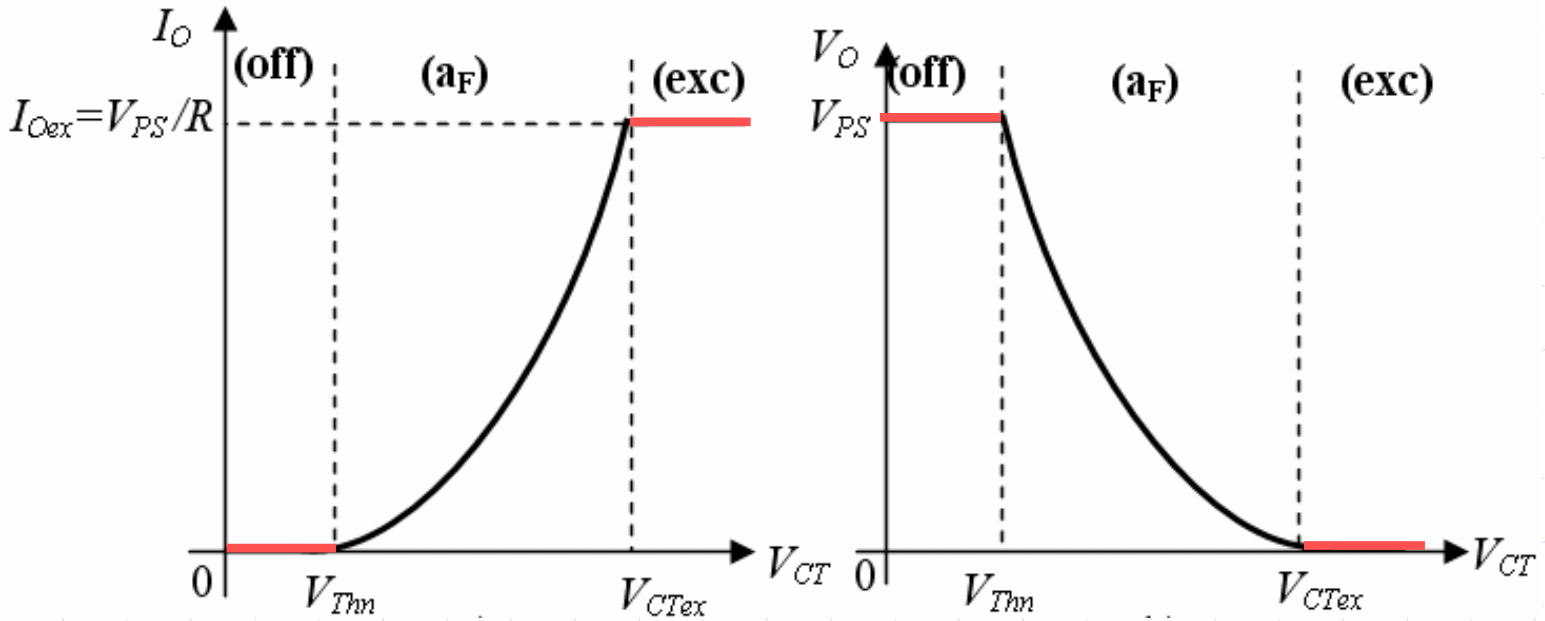
$V_{CT}\uparrow$, $I_O\uparrow$, $V_O\downarrow$

$V_{O,min}=0$ $\qquad I_{Oex}=\dfrac{V_{PS}}{R}$









- Two **extreme regions,** passive regions:

 - **cutoff (*off*)** $I_T=0$; $V_O>0$; ideal switch in off state

 - **extreme conduction (*exc*)** $I_T=I_{Oex}$; $V_O=0$; ideal switch in the on state

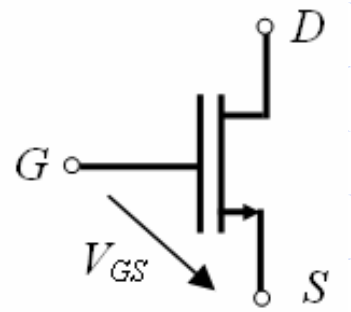
If $V_{CT}<V_{Thn}$ or $V_{CT}>V_{CTex}$ **switching transistor**

- An **intermediary region**, active forward region $\mathbf{a_F}$

$V_{CT}\in(V_{Thn}; V_{CTex})$, - **permanent conduction (amplifier)**

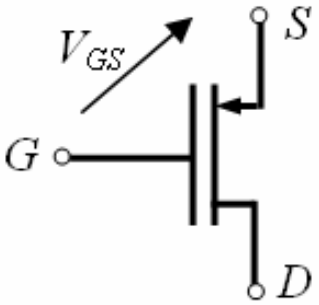
Symbols of the transistors

n-type



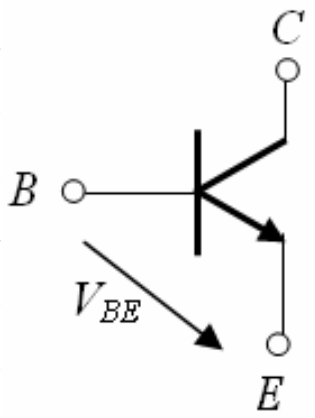
n-channel enhancement-type MOSFET

p-type

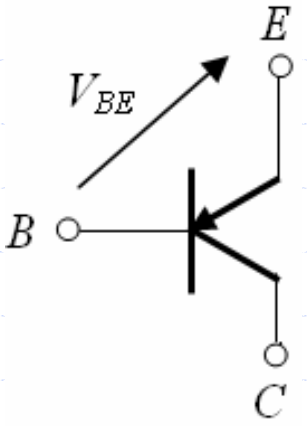


p-channel enhancement-type MOSFET

G - gate or grid
D - drain
S - source



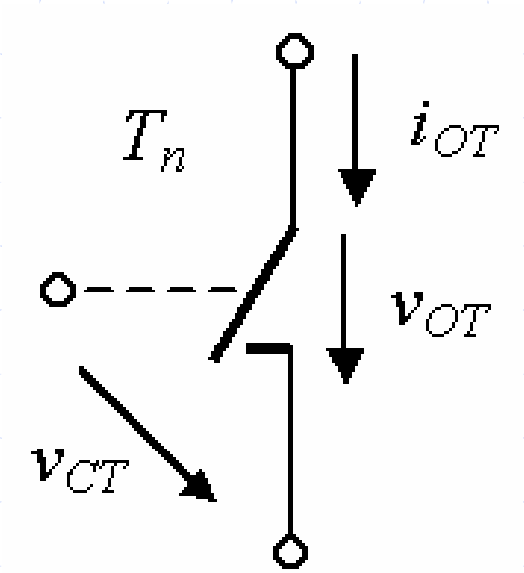
npn BJT

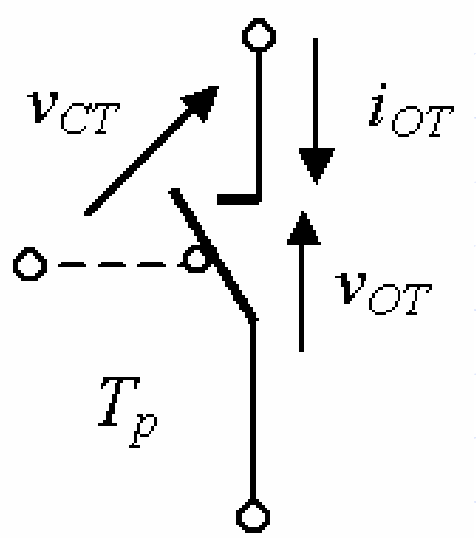


pnp BJT

B – base
C – collector
E – emitter

The Controlled Switch Model for Transistors





$v_{CT} > V_{Thn}$; T- (exc) ; $i_{OT} > 0$; $v_{OT} \approx 0$

$v_{CT} < V_{Thn}$; T- (off) ; $i_{OT} = 0$

$v_{CT} > V_{Thp}$; T- (off) ; $i_{OT} = 0$

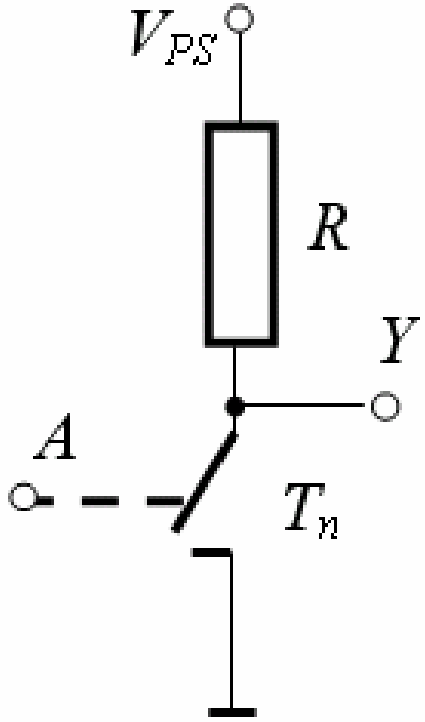
$v_{CT} < V_{Thp}$; T- (exc) ; $i_{OT} > 0$; $v_{OT} \approx 0$

The controlled switches are complementary.

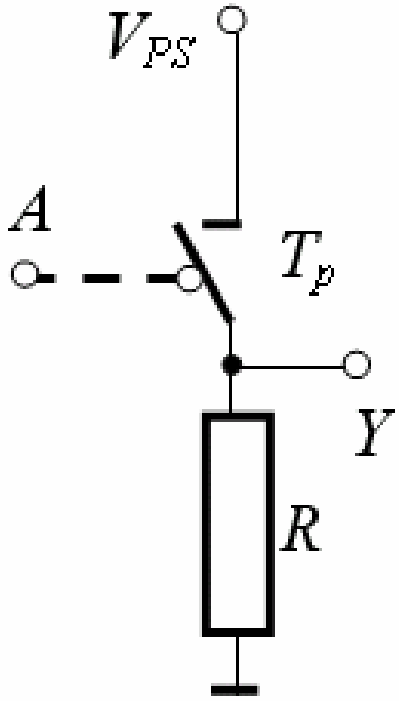
MOSFET DIGITAL CIRCUITS

- Ideal controlled switch model
- Implementation with MOSFET

Logic inverter

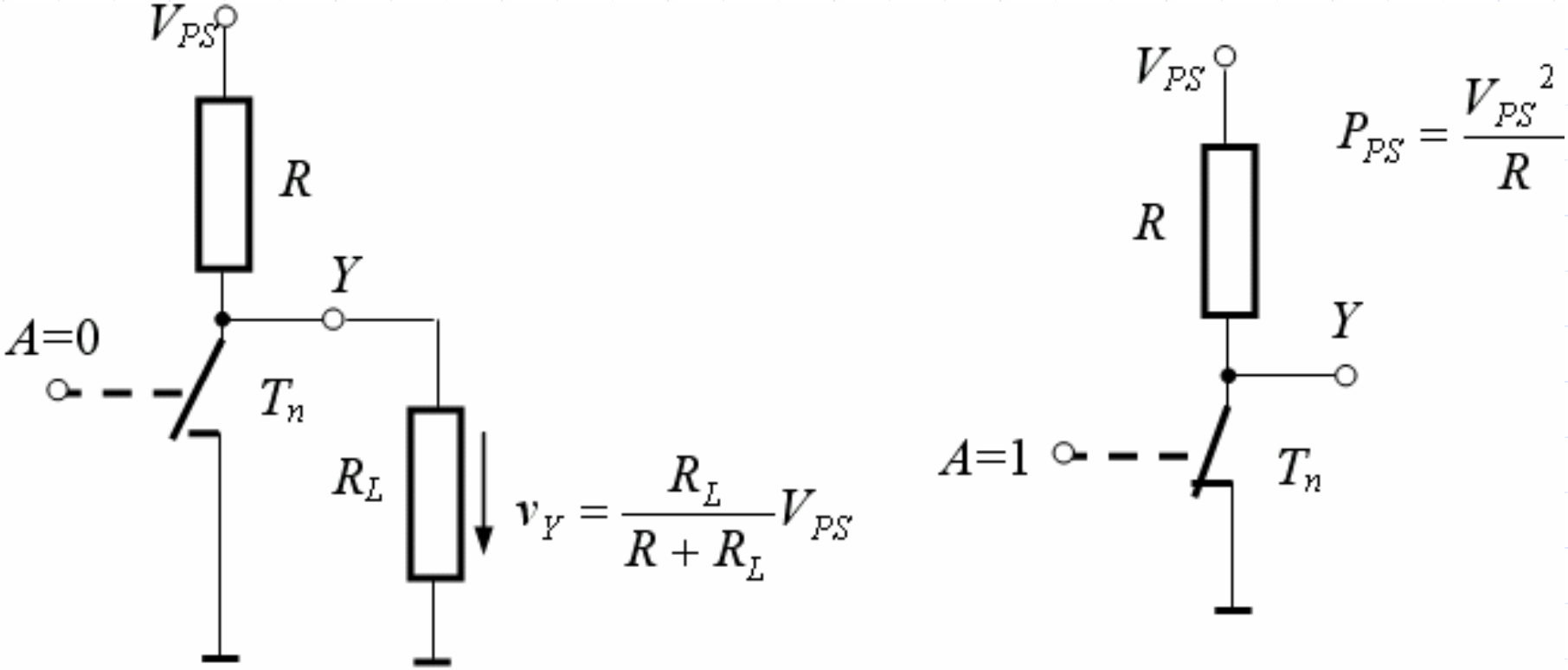


A	T_n	Y
0	*(off)*	1
1	*(on)*	0



A	T_p	Y
0	*(on)*	1
1	*(off)*	0

Critical analysis of the inverter with a T_n controlled switch and R



Diminishing the disadvantage:

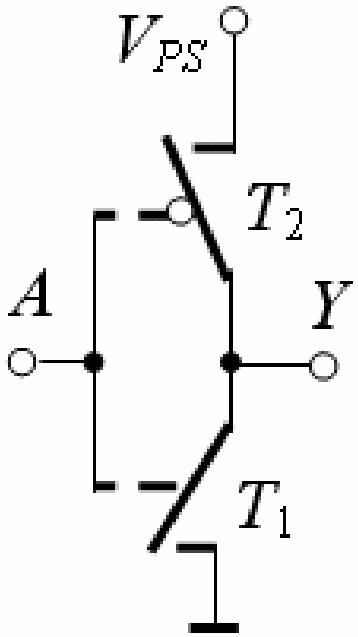
R **as small as possible, ideal** $R \rightarrow 0$; ***R*** **as large as possible, ideal** $R \rightarrow \infty$

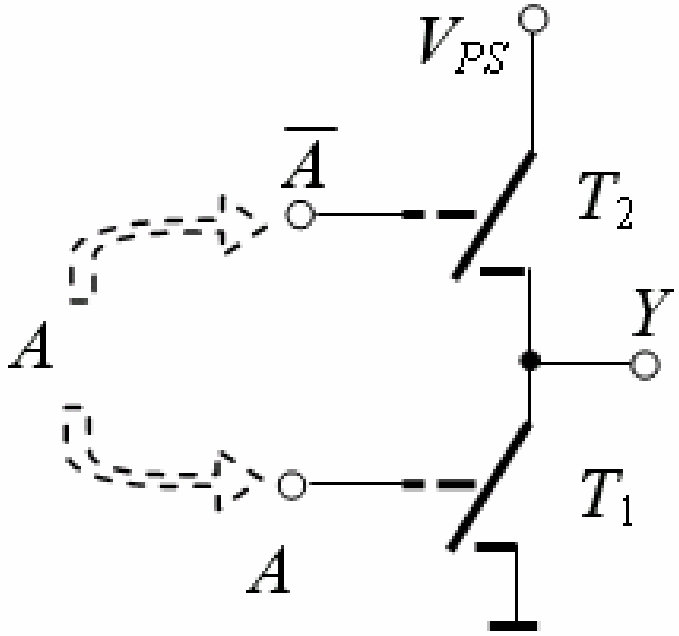
Solution: replacement of *R* with a controlled switch

Two solutions:

complementary switches

complementary control





A	T_1	T_2	Y
0	*(off)*	*(on)*	1
1	*(on)*	*(off)*	0

good bye!

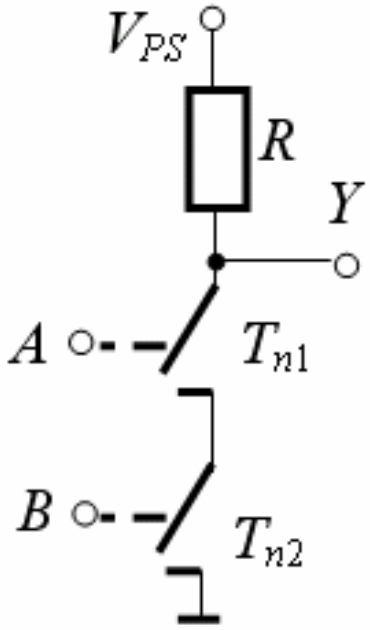
output voltage division

power dissipation

CMOS

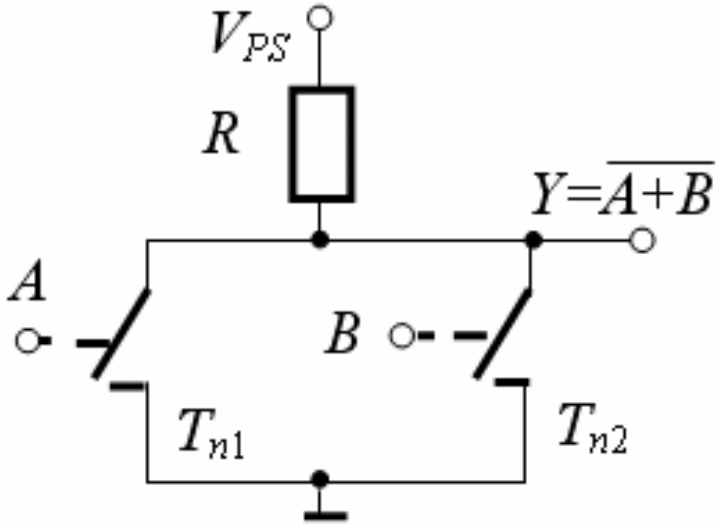
TTL

Logic function NAND, NOR



A	B	T_{n1}	T_{n2}	$Y=\overline{A \cdot B}$
0	0	*(off)*	*(off)*	1
0	1	*(off)*	*(on)*	1
1	0	*(on)*	*(off)*	1
1	1	*(on)*	*(on)*	0

How can we eliminate the disadvantages due to the presence of *R*?



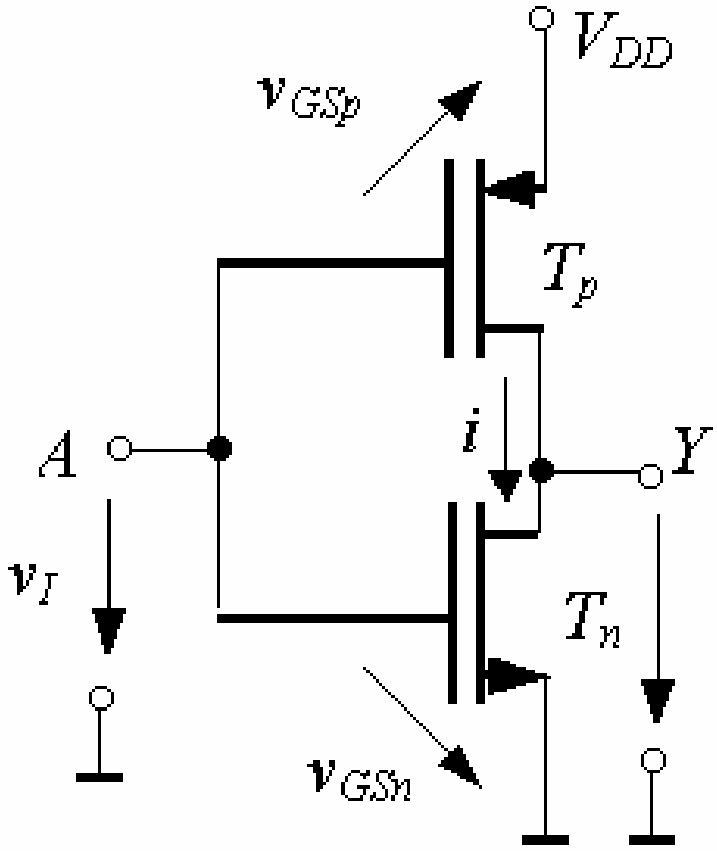
A	B	T_{n1}	T_{n2}	$Y=\overline{A+B}$
0	0	*(off)*	*(off)*	1
0	1	*(off)*	*(on)*	0
1	0	*(on)*	*(off)*	0
1	1	*(on)*	*(on)*	0

CMOS Logic Gates

- **CMOS inverter**

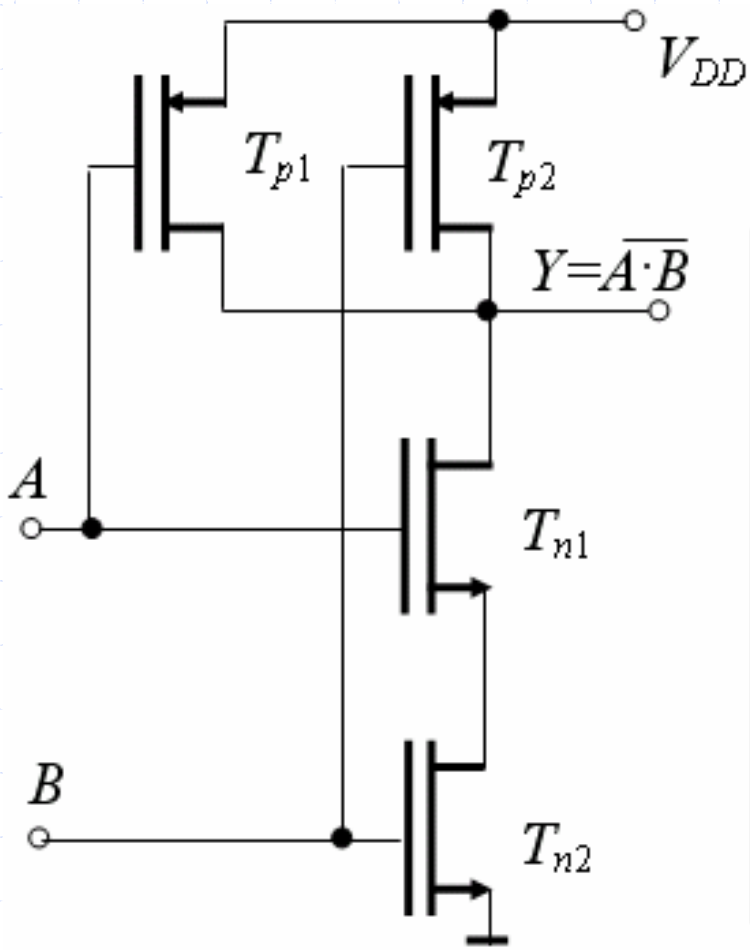
$$v_{GSn}=v_I$$

$$v_{GSp}=v_I-V_{DD}$$



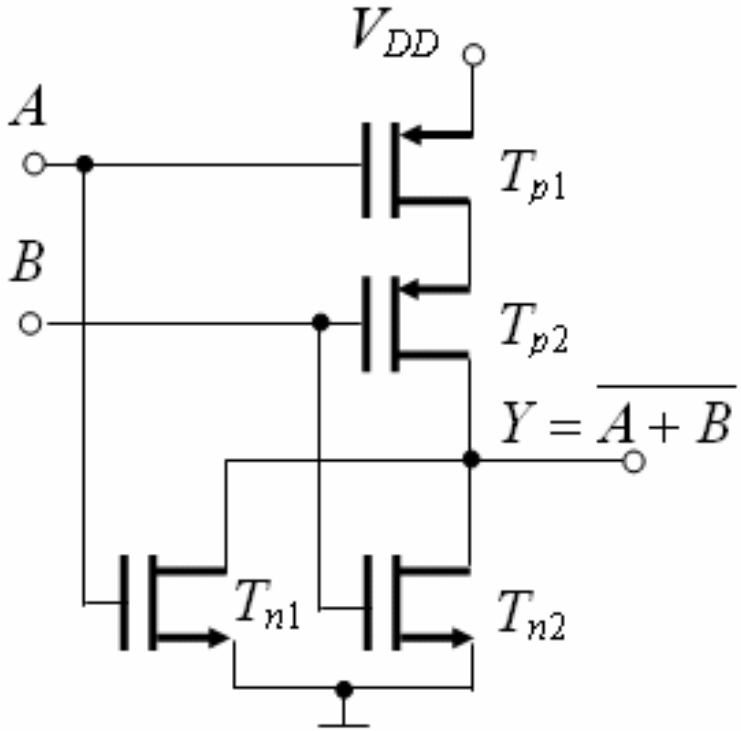
v_I	v_{GSn}	v_{GSp}	T_n	T_p	v_O
0V	$0V<V_{Thn}$	$-V_{DD}<V_{Thp}$	*(off)*	*(on)*	$\approx V_{DD}$
V_{DD}	$V_{DD}>V_{Thn}$	$0>V_{Thp}$	*(on)*	*(off)*	$\approx$0V

NAND

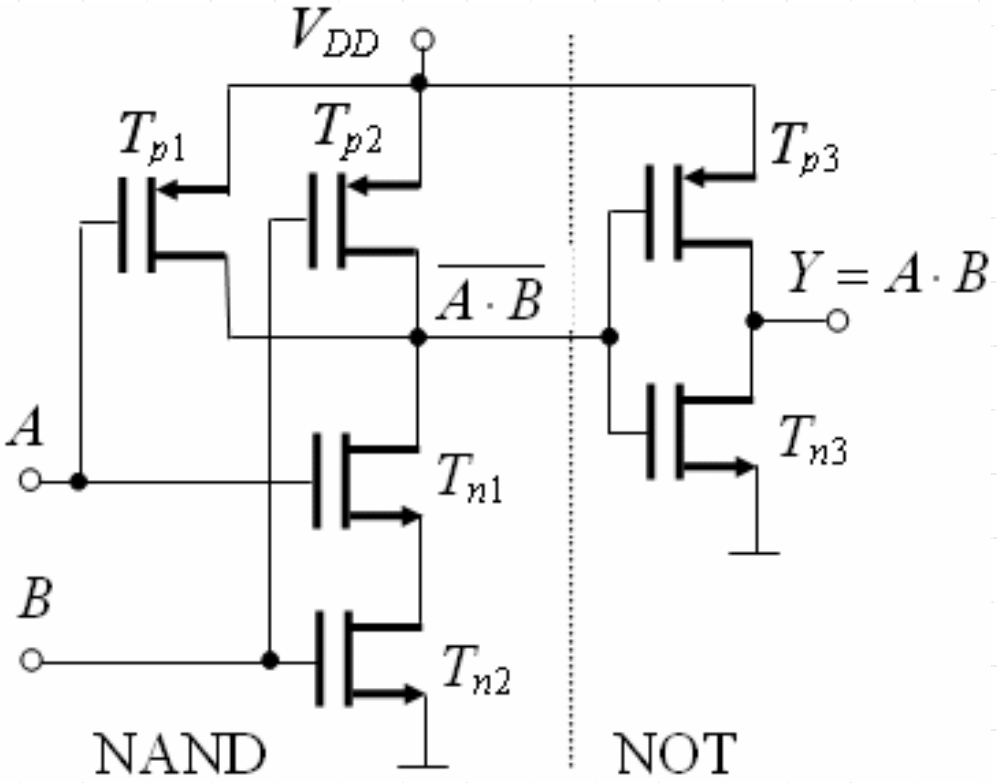


A	B	T_{n1}	T_{n2}	T_{P1}	T_{P2}	$Y=\overline{A\cdot B}$
0	0	*(off)*	*(off)*	*(on)*	*(on)*	1
0	1	*(off)*	*(on)*	*(on)*	*(off)*	1
1	0	*(on)*	*(off)*	*(off)*	*(on)*	1
1	1	*(on)*	*(on)*	*(off)*	*(off)*	0

NOR


V_{DD}
A
B
T_{p1}
T_{p2}
$Y = \overline{A + B}$
T_{n1}
T_{n2}

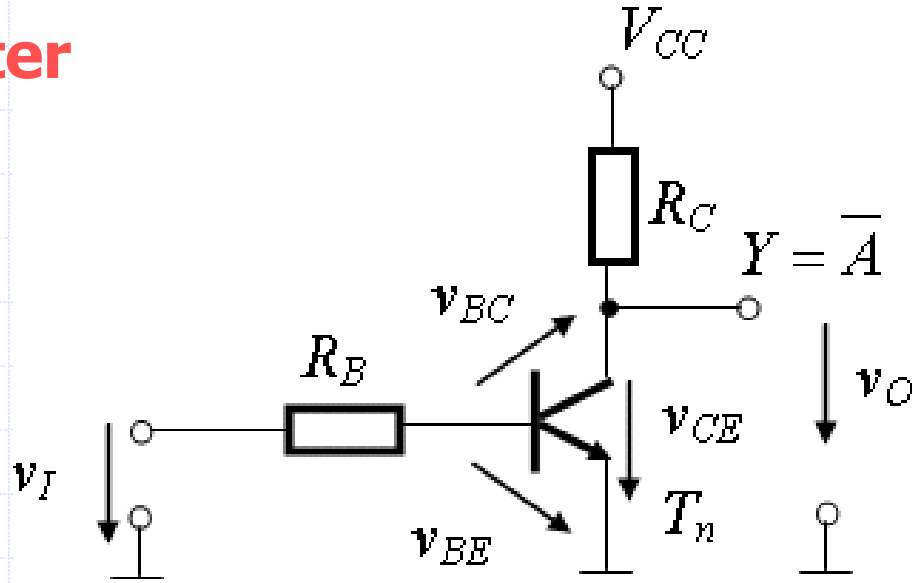
AND


V_{DD}
T_{p1}
T_{p2}
T_{p3}
$\overline{A \cdot B}$
$Y = A \cdot B$
A
T_{n1}
T_{n3}
B
T_{n2}
NAND
NOT

Bipolar Digital Circuits

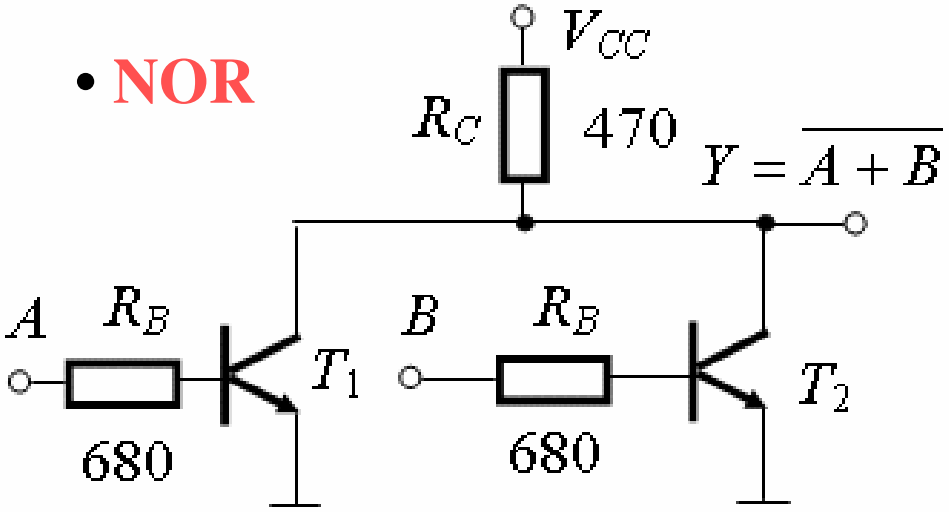
- **Inverter**

RTL Technology



v_I	T_n	v_O
0V	*(off)*	V_{CC}
V_{CC}	*(on)*	0.2V

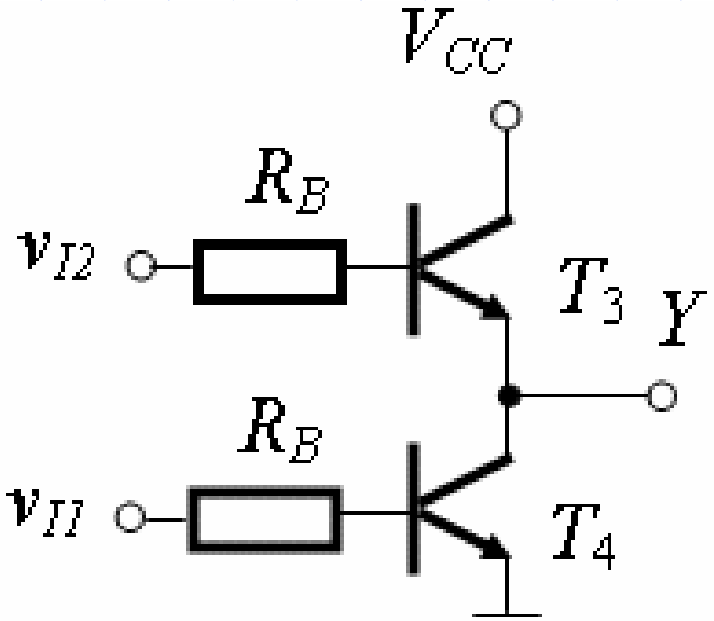
- **NOR**



A	B	T_1	T_2	$Y = \overline{A + B}$
0	0	*(off)*	*(off)*	1
0	1	*(off)*	*(on)*	0
1	0	*(on)*	*(off)*	0
1	1	*(on)*	*(on)*	0

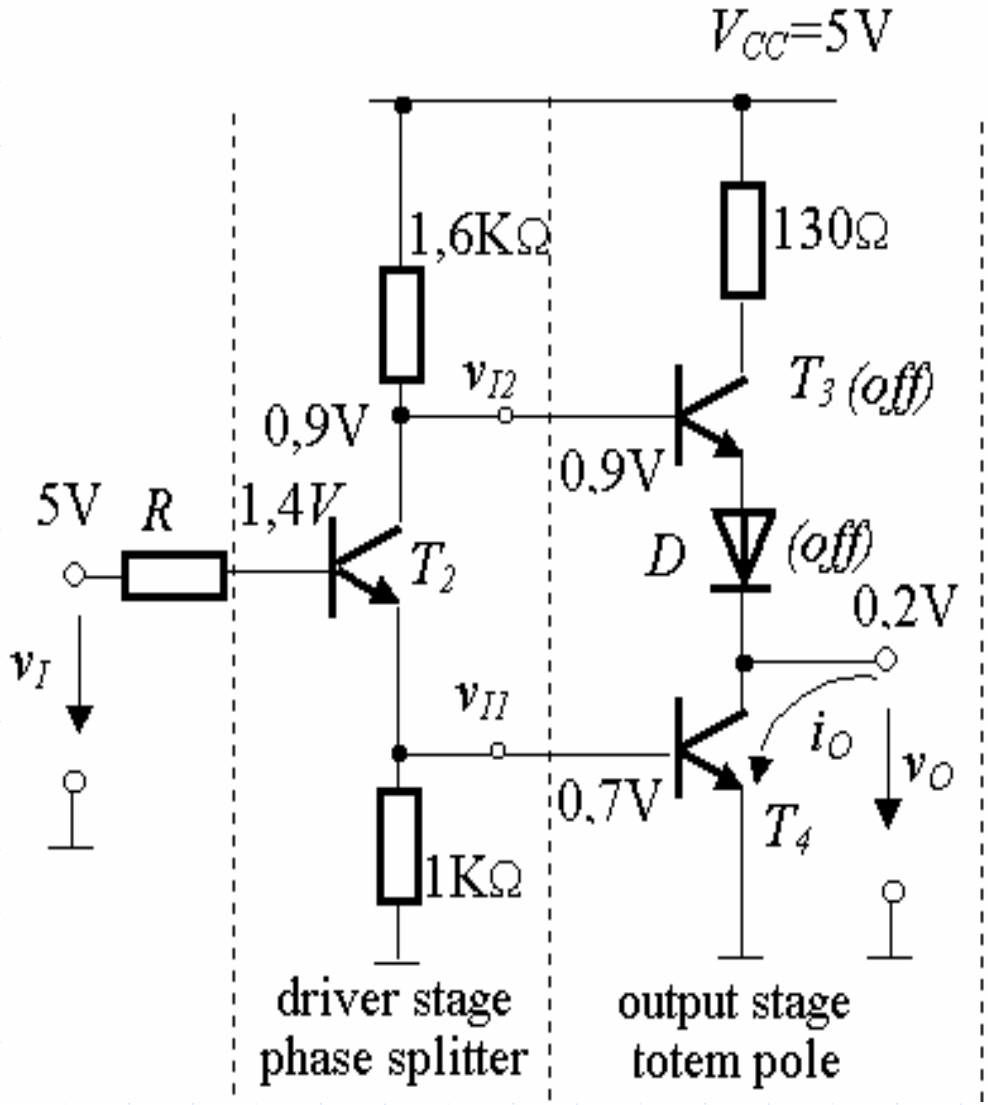
TTL: Transistor-Transistor Logic

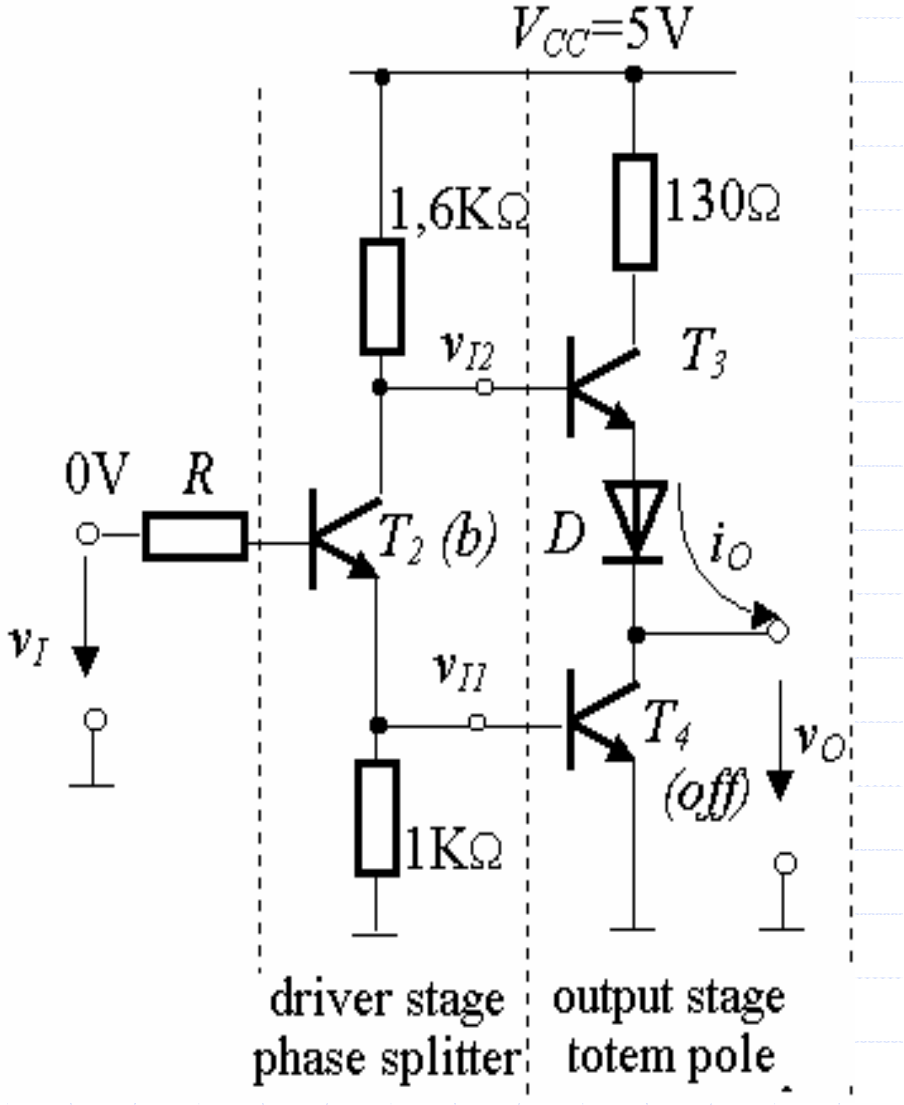
- Logic Inverter
- from technological reasons in TTL integrated circuits the use of only npn type transistors is preferred
- identical transistors but complementary control



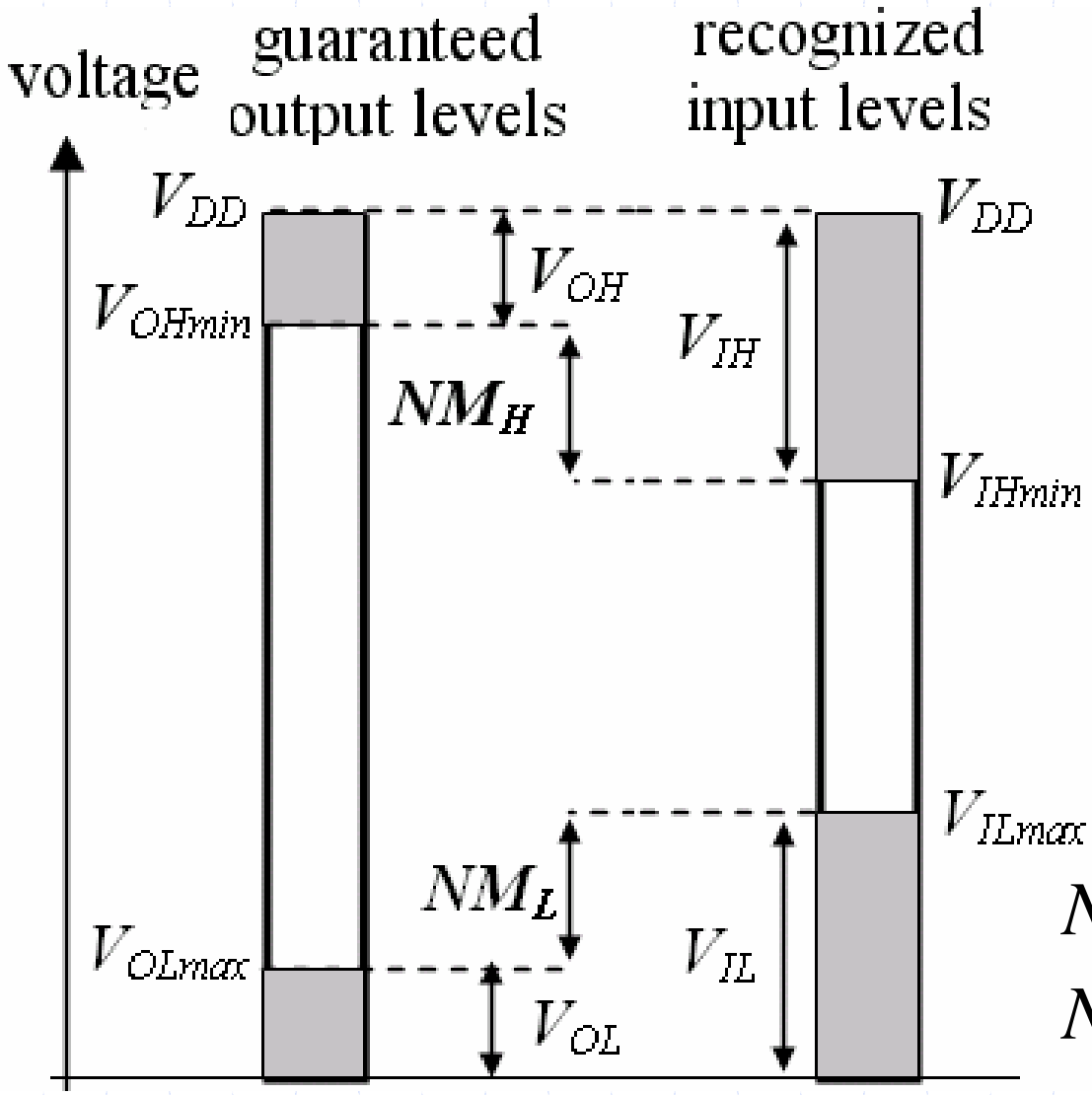
T_3	T_4	Y
(on)	(off)	1
(off)	(on)	0

Standard TTL gate





Noise margins



$$NM_H = V_{OH\,min} - V_{IH\,min}$$

$$NM_L = V_{ILmax} - V_{OLmax}$$

Voltage levels and noise margins for CMOS family operated with 5V

$$NM_L = 1.5\text{V} - 0.5\text{V} = 1\text{V}$$

$$NM_H = 4.5\text{V} - 3.5\text{V} = 1\text{V}$$

The voltage levels and noise margins for TTL family