Assignment 2

Due date: October 18, 2017

Group No: 5

Students:
Lalit Bhat: 01671833
Priya Parikh: 01679645

Objectives:

To build a 32 location by 8-bit contents RAM using 4 16x4RAMs. DIP switches are used for address line as well as data lines. Toggle switch is used for read and write action. When the toggle switch is high, read the data; when the toggle switch is low, write the data.
The main idea here is to learn to design RAM i.e. to increase word size and to increase the ram space, and to learn to address, read and write in the ram.

List Of components:

Part description	Qty
Proto board PB-105T	1
7489 RAM	4
17DIP8SS 8-Switch DIP Switch sets	2
08TIE524 Dual 7 Segment Display	1
74LS240 Tri State Buffer	2
74LS247 BCD to 7 Segment Display	2
74LS04 Hex Invertor	1
5V Power supply	1
200Ω Resistor	13
330Ω Resistor	2
Cable, Banana with Alligator Clips	2
Jumper wires	
Wire cutter	2
Logic Probe	1

Experimental Approach:

1. On paper we designed a 16x8 RAM using 2 16X4 RAM chips by giving the 2 chips the same address lines and giving the input data and output data in parallel (here we get 4*2= 8 bits)

2. We designed 2 such RAMs of 16x8 each.

3. We then made a 32x8 RAM using the 4 ram chips and using a chip enable as the 5^{th} address line.

4. We cannot short the wires (Example: outputs x1 and x5 from the ram chips in the schematics) of the RAM chips, to solve this we use a tri-state buffer which is a high impedance chip and helps us isolate the data lines coming out of the ram chips.

5. The tri state buffer chip works in such a way that when G1 is low 1A1 to 1A4 are high and when G2 is low an G1 is high 2A1 to 2A4 are high (Refer to the chip 240 in the schematics).

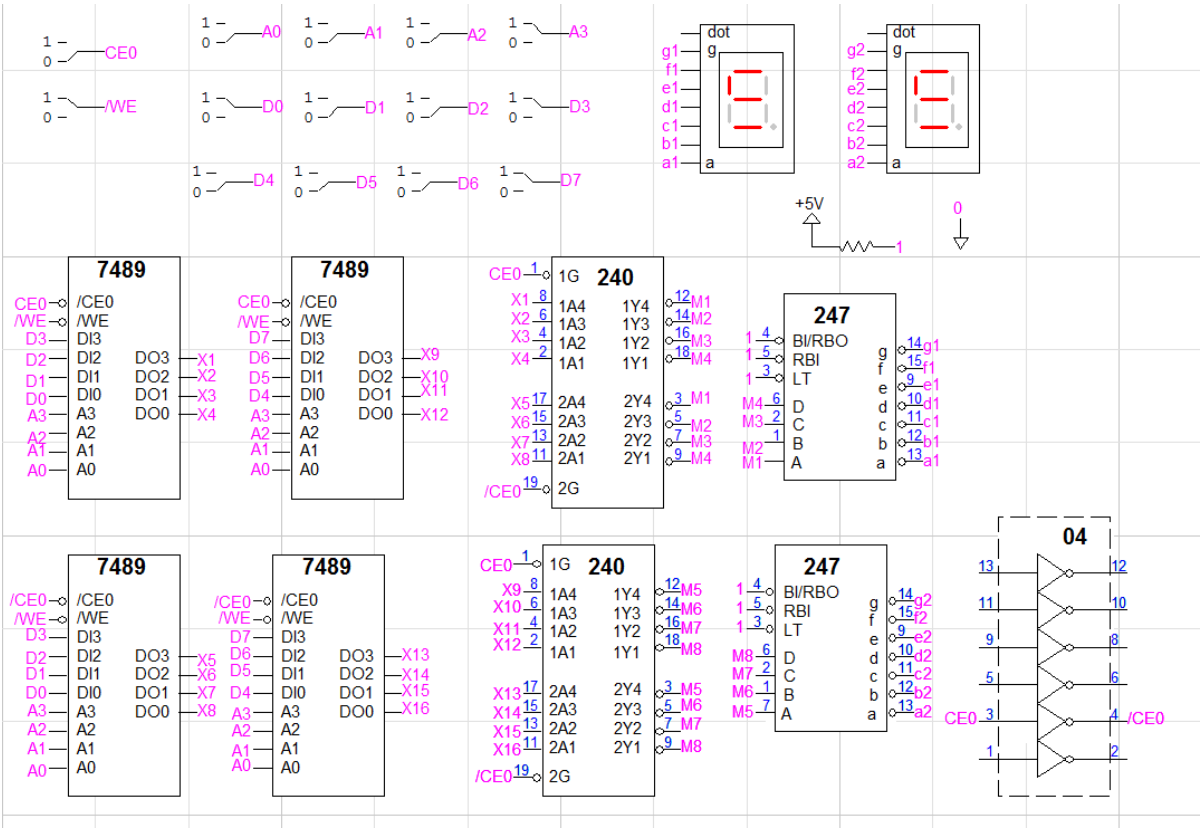
6. The outputs of the tristate buffer are given to the chip 247 (BCD to 7-segment), and the output of these were connected to the led.

7. We then constructed the circuit on logic works and simulated it to find if there were any bugs.

8. After the successful simulation, the schematics designed on Logic works was realized on the Proto board.

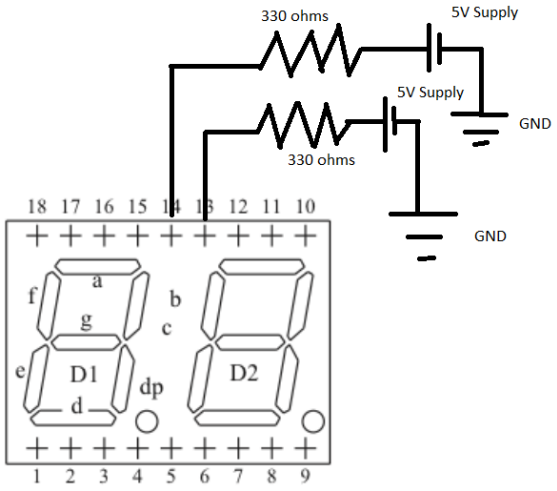
9. Implemented the hardware and made minor changes to fix the bugs.

Logic works schematics:



7-Segment display

Pin No.	Assignment	Assignment
1	Cathode e1	Anode e1
2	Cathode d1	Anode d1
3	Cathode c1	Anode c1
4	Cathode dp1	Anode dp1
5	Cathode e2	Anode e2
6	Cathode d2	Anode d2
7	Cathode g2	Anode g2
8	Cathode c2	Anode c2
9	Cathode dp2	Anode dp2
10	Cathode b2	Anode b2
11	Cathode a2	Anode a2
12	Cathode f2	Anode f2
13	Common Anode D2	Common Cathode D2
14	Common Anode D1	Common Cathode D1
15	Cathode b1	Anode b1
16	Cathode a1	Anode a1
17	Cathode g1	Anode g1
18	Cathode f1	Anode f1



Results:

During the demonstration the TA asked us to write several values in different memory locations, and then later checked if the we could read the data stored in the same memory locations and that the data was not stored in any other address due to any wiring bug.

We could read and write the data accurately in the RAM.

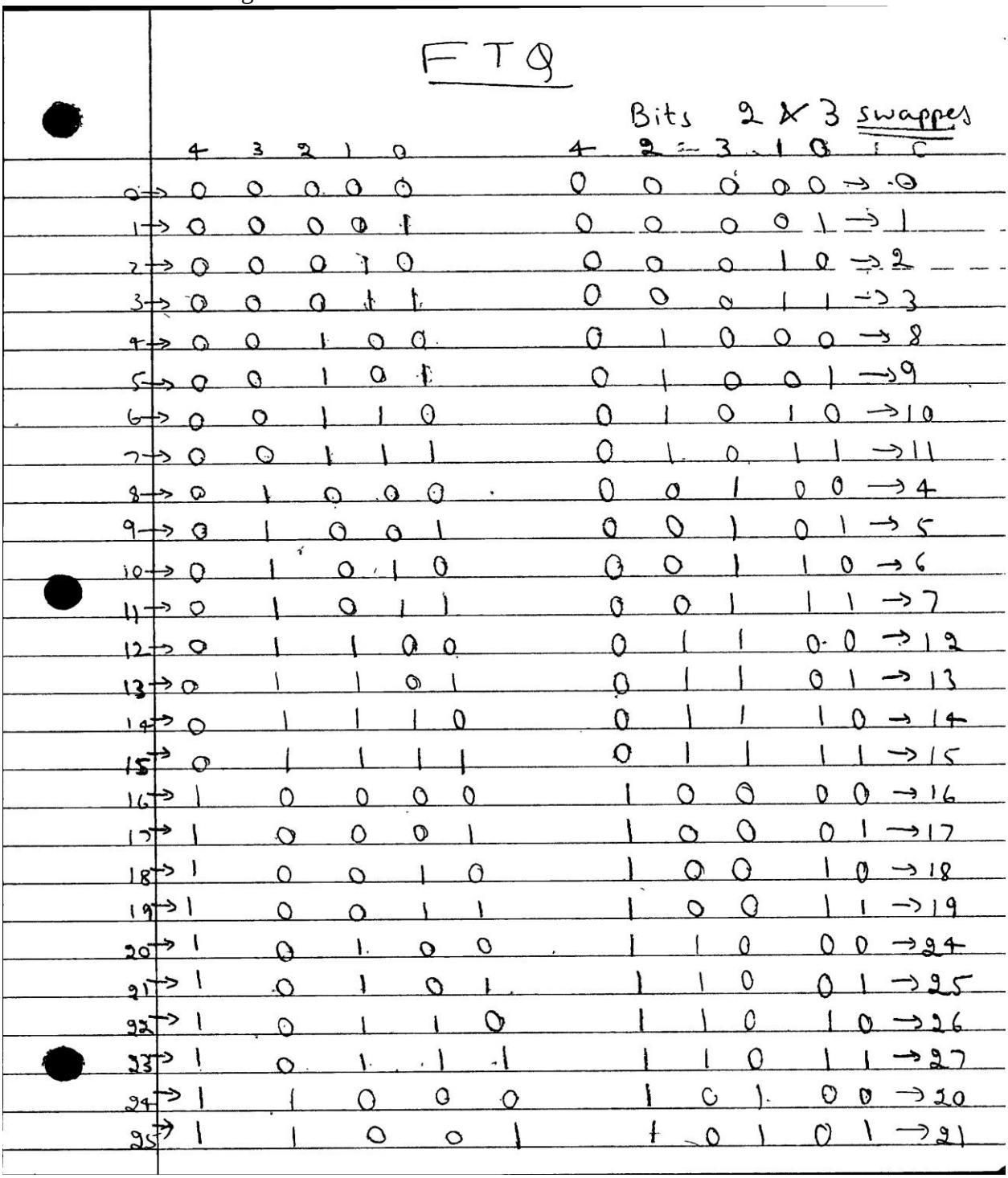
Conclusion:

We successfully designed, simulated and made a hardware realization for a 32x8 RAM from 4 16x4 RAMs, and learnt how to design our own ram with the desired word size and storage space.

FTQs:

1. What would the Order of Memory Addresses if Bits 2 and 3 were swapped? [Lalit Bhat]

   If the bits 2 and 3 were changed then the addresses would change in some of the cases as shown in the below diagrams.



Bits 2 & 3 swapped

	4	3	2	1	0		4	3	2	1	0	
26 →	1	1	0	1	0		1	0	1	1	0	→ 22
27 →	1	1	0	1	1		1	0	1	1	1	→ 23
28 →	1	1	1	0	0		1	1	1	0	0	→ 28
29 →	1	1	1	0	1		1	1	1	0	1	→ 29
30 →	1	1	1	1	0		1	1	1	1	0	→ 30
31 →	1	1	1	1	1		1	1	1	1	1	→ 31

2. What is tri-state buffer and what is it used for? [Priya Parikh]

A tri-state buffer is a useful device that allows us to control when current passes through the device, and when it doesn't.

It has two inputs: enable input and input A.

Enable input controls whether the primary input is passed to its output or not. If the enable inputs signal is 1, the tri-state buffer behaves like a normal buffer. If the "enable" input signal is 0, the tri-state buffer passes a high impedance (or hi-Z) signal, which effectively disconnects its output from the circuit.

Enable input	Input A	Output Y
0	0	Z
0	1	Z
1	0	0
1	1	1

Symbol of tri state buffer: