Assignment 1

Due date: October 4, 2017

Group No: 5

Students:
Lalit Bhat: 01671833
Priya Parikh: 01679645

Objectives:

To design, build and test a counter with external control and perform the following. When no switch is triggered, the 7-segment display, displays EVEN number (0-2-0-2) in forward. When switch 1 is triggered, it displays ODD numbers (1-3-1-3) in forward. When Only switch 2 is triggered, it displays EVEN numbers (2-0-2-0) in reverse. When both switches triggered, it displays ODD numbers (3-1-3-1) in reverse.

List Of components:

Part description	Qty
Proto board PB-105T	1
17DIP8SS 8-Switch DIP Switch sets	1
08TIE524 Dual 7 Segment Display	1
74LS74 D Flipflop	1
74LS247 BCD to 7 Segment Display	1
74LS00 NAND Gate	4
74LS04 Hex Invertor	1
Function Generator	1
5V Power supply	1
330Ω Resistor	1
Cable, Banana with Alligator Clips	2
Jumper wires	
Wire cutter	2
Oscope Probe- Hook End Adapter	1

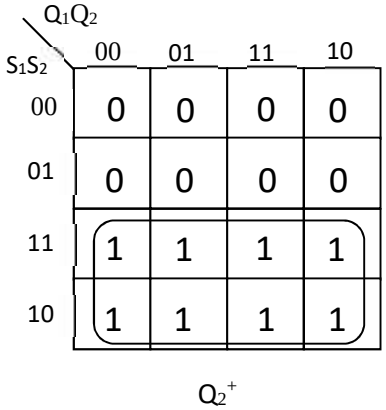
Experimental Approach:

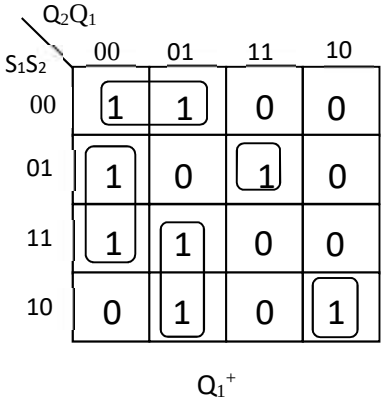
1. Assigned states to the switches:
    - S1= switch1, S2= switch2
    - State1= 00 EVEN forward
    - State2= 01 EVEN reverse
    - State3= 10 ODD forward
    - State4 = 11 ODD reverse
2. Drew the truth table according to the states showing the present as well as next state of the output for every combination.
3. Plotted the K-maps in accordance of the truth table and deduced the equations for the next states.
4. Designed and simulated the circuit in Logic works.
5. After the successful simulation, the schematics designed on Logic works was realized on the Proto board.
6. We used a function generator to provide the clock pulses to the D flipflop in the circuit.
7. Implemented the hardware and made minor changes to fix the bugs.

Truth table

Switches		Present State		Next State	
S1	S2	Q1	Q2	Q1+	Q2+
EVEN Forward					
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	1	0	0
EVEN Reverse					
0	1	0	0	1	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	1	0
ODD Forward					
1	0	0	0	0	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	0	1
EVEN Reverse					
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	1	0	1

K:map



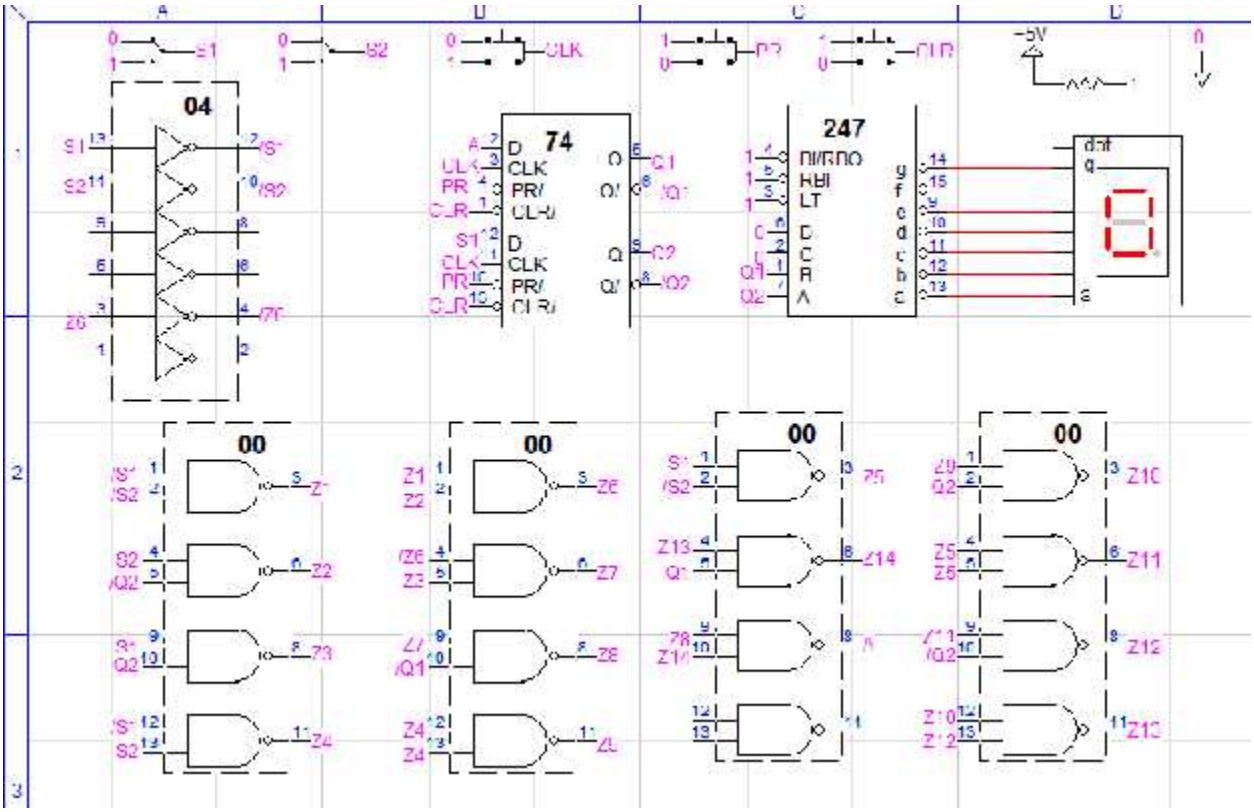


$Q_2^+ = S_1$

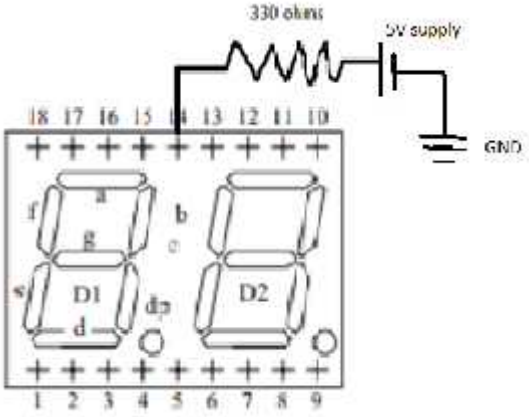
$Q_1^+ = Q_1'S_1'S_2' + S_2Q_1'Q_2' + S_1Q_1'Q_2 + S_1'S_2Q_1Q_2 + S_1S_2'Q_1Q_2'$

$= Q_1'(S_1'S_2' + S_2Q_2' + S_1Q_2) + Q_1(S_1'S_2Q_2 + S_1S_2'Q_2')$

Logic works schematics:



7-Segment display



PIN NO:	Description
1	e1
2	d1
3	c1
14	Common anode d1
15	b1
16	a1
17	g1
18	f1

Results:

During the demonstration the TA gave us several instances of the current state and which mode to run the circuit in, each of these instances gave the desired outputs.

Conclusion:

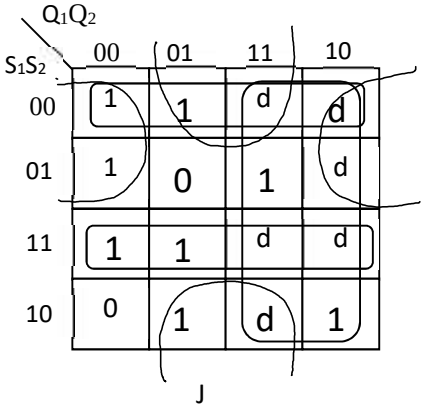
We successfully designed, simulated and made a hardware realization for a counter with external control.

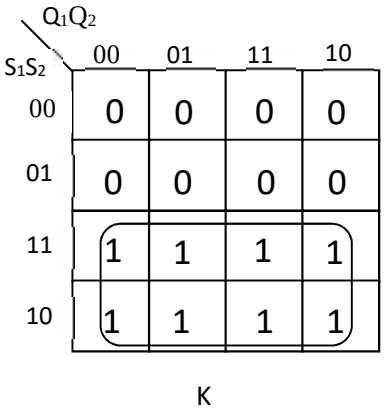
FTQs:

1. Would the circuit be simpler with both the ODD/EVEN bit and UP/DOWN bit opposite to what you have? (Priya Parikh)

    - The states are assigned as per the designer's choice. If designer take exactly the opposite values than it won't make any difference in the logic of circuit.

2. Quickly redo the K-map for Q_0 with a JK flipflop. (Lalit Bhat)





$J = S_1'S_2' + S_1S_2 + S_2'Q_2 + S_2Q_2' + Q_1$

$K = S_1S_2' + S_2Q_2$