Assignment 3

Due date: November 3, 2017

Group No: 5

Students:
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Objectives:

To design and build a multiplier circuit which multiply two 4-bit number and displays the least significant bit first, followed by 4-most significant bits. All computations are to be completed within 10 clock pulses.

List Of components:

Part description	Qty
Proto board PB-105T	1
17DIP8SS 8-Switch DIP Switch sets	2
08TIE524 Dual 7 Segment Display	1
74LS174 Hex D-type Flip-flop with clear	1
74LS247 BCD to 7 Segment Display	2
74LS00 NAND Gate	2
74LS04 Hex Invertor	1
74LS195 4-bit shift register	1
74LS164 8-bit serial shift register	1
74LS181 ALU	1
5V Power supply	1
1kΩ Resistor	10
10kΩ Resistor	2
Cable, Banana with Alligator Clips	2
Jumper wires	
Wire cutter	2
Logic probe	1

Experimental Approach:

1. We first studied the data sheets of the shift registers, hex D-type FF, ALU and started planning what mode we need to hard code our ALU and other registers to get the bits to shift in the right direction and for accurate addition as required.

2. Made a rough outline of the circuit on paper.

3. Constructed this circuit on logic works and simulated it to find and fix any bugs.

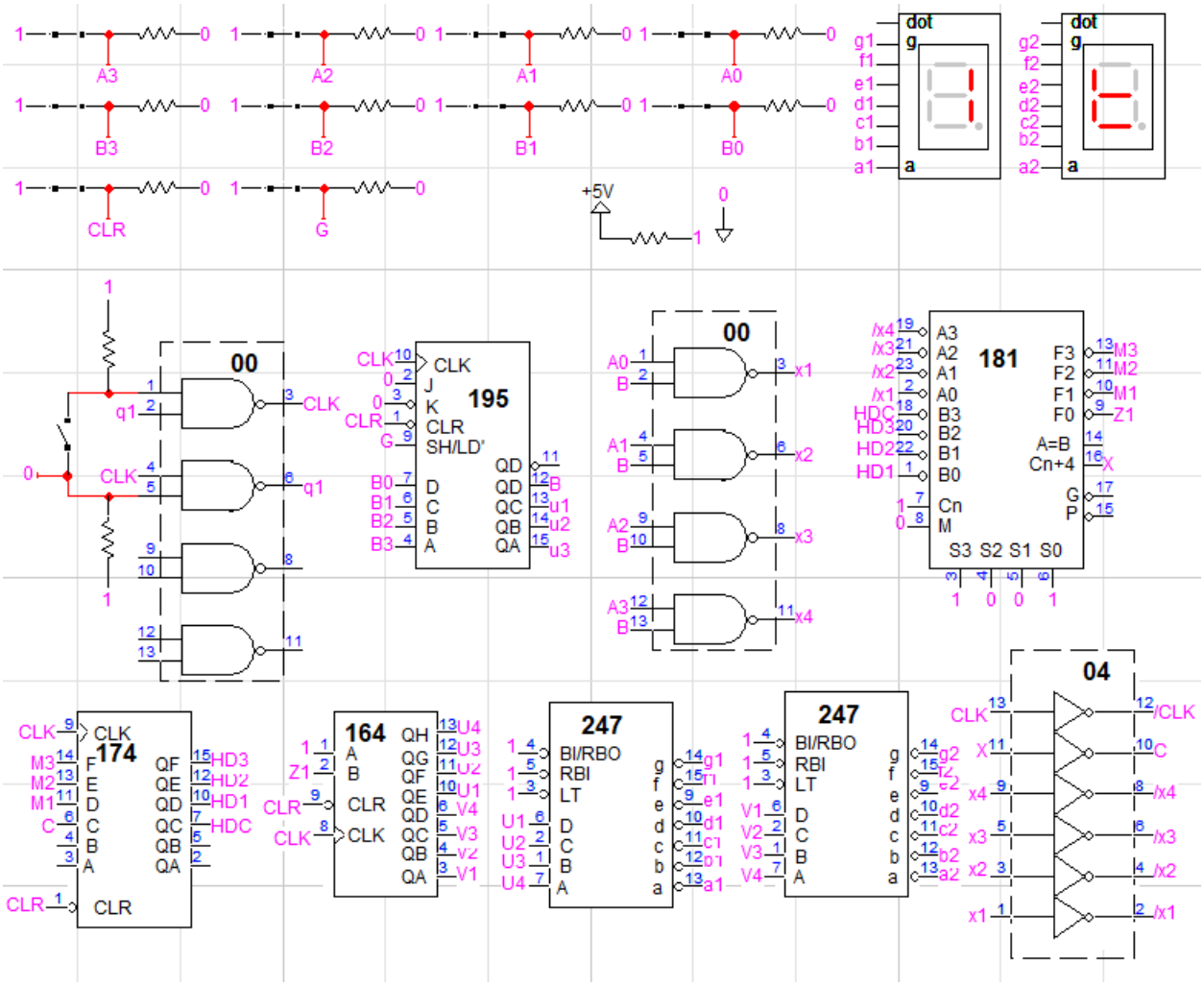
4. After simulating the circuit successfully, the hardware circuit was built on a Proto-Board.

5. In this circuit we used pullup resistors for the dip switches to get logical 1 and 0 at the input of the registers.

6. Instead of using the function generator to give us our clock pulses we built our own clock circuit using a toggle switch and a nand-gate chip.

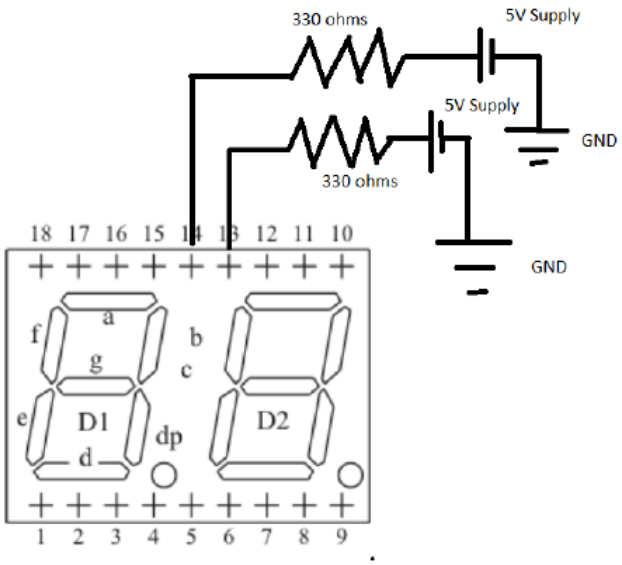
7. We implemented out hardware and after several debugging steps we could get the desired multiplication output.

Logic works schematics:



7-Segment display

Pin No.	Assignment	Assignment
1	Cathode e1	Anode e1
2	Cathode d1	Anode d1
3	Cathode c1	Anode c1
4	Cathode dp1	Anode dp1
5	Cathode e2	Anode e2
6	Cathode d2	Anode d2
7	Cathode g2	Anode g2
8	Cathode c2	Anode c2
9	Cathode dp2	Anode dp2
10	Cathode b2	Anode b2
11	Cathode a2	Anode a2
12	Cathode f2	Anode f2
13	Common Anode D2	Common Cathode D2
14	Common Anode D1	Common Cathode D1
15	Cathode b1	Anode b1
16	Cathode a1	Anode a1
17	Cathode g1	Anode g1
18	Cathode f1	Anode f1



Results:

During the demonstration the TA asked us to multiply different combinations of 2 four-bit numbers to check if our circuit executes accurately and it displays the least significant bits first followed by the most significant bits.

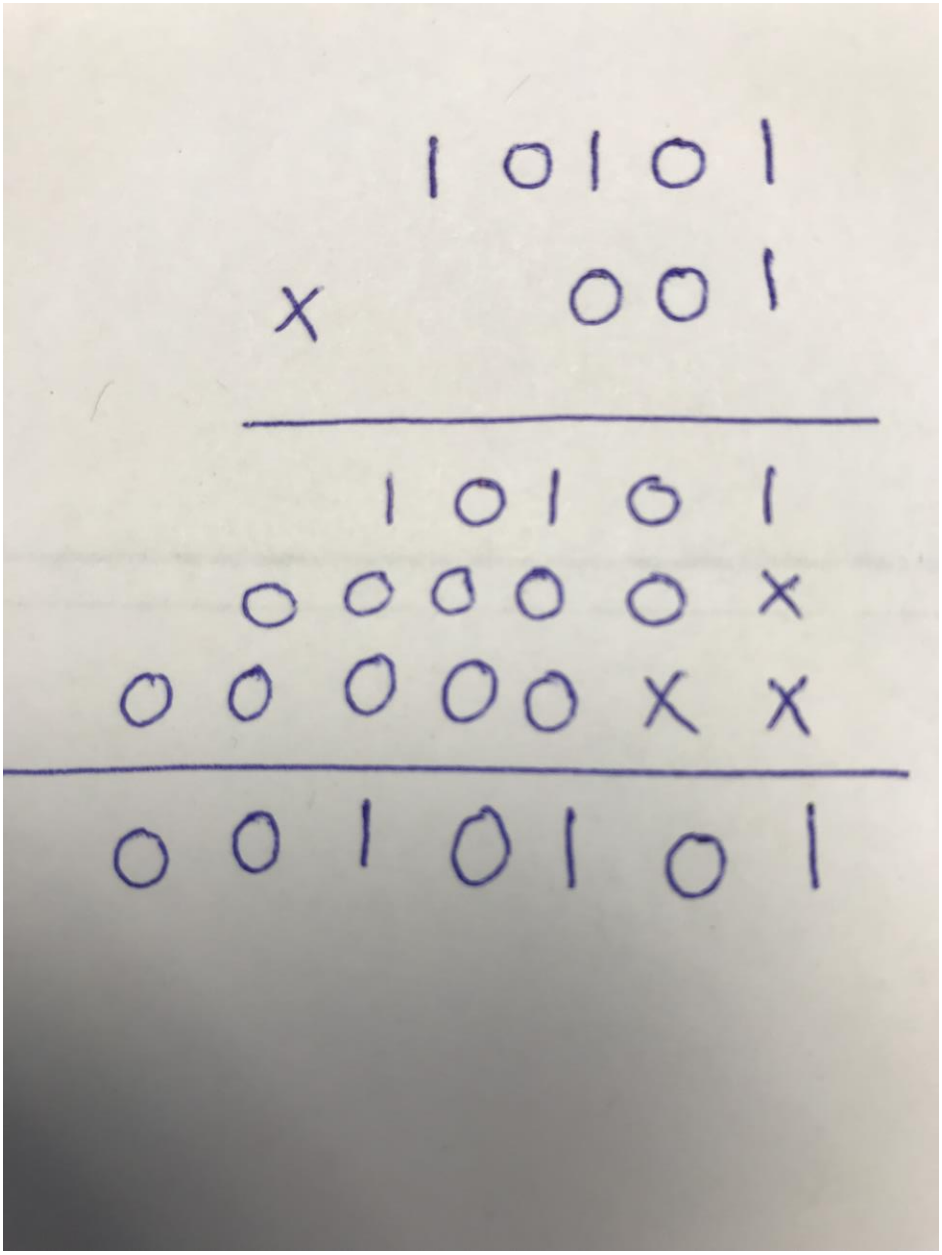
In each of these combinations we got our desired outputs.

Conclusion:

We successfully designed, simulated and made a hardware realization for 4-bit by 4-bit multiplier and used a de-bounced toggle switch to provide clock pulses.

FTQs:

1. Multiply 001 and 10101 by hand (Priya Parikh)



2. What is the minimum number of clock cycles (Not including Load) needed for multiplying two 6-bit numbers? (Lalit Bhat)

Ans: Minimum Six Clock cycles. This is because when the numbers are loaded from the switches to the shift parallel shift register in positive clock and at the same time when the numbers are being shifted from the accumulator to the output shift register at negative clock cycles at the same time, for this minimum of 6 clock pulses are required.