# Report for the implementation of a data register and a program counter

## Specification verification of the data register

To test the register, various tests were written. The testing procedures are now briefly described. First, the power-on-reset gets tested. As the output q is zero, the test is OK. Next, zero gets written when the output is already at zero. No change can be seen here. This test is repeated in the last tests.

The values get loaded and checked afterwards following the pattern to set the load and enable bits and then the value on the data bus. The next clock cycle both get deactivated, and the output is asserted.

In the last two tests there is checked if the reset sets the output to zero, even if the data bus has a value and the enable and load bits are set. As can be seen in figure 1 the data register works as intended.

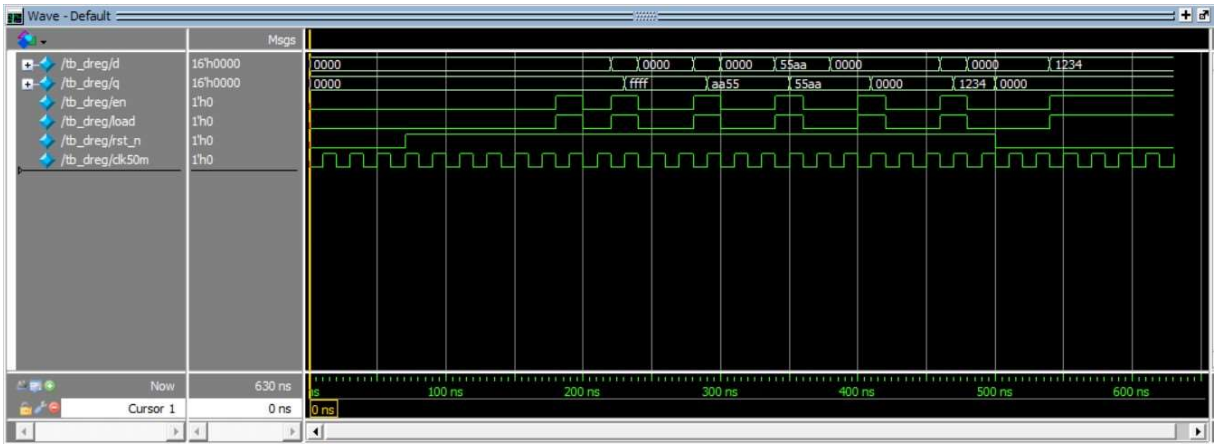


*Figure 1: Test of the data register*

## Specification verification of the program counter

These tests follow the same structure as before. First the power-on-reset gets tested. Then the enable and increase bits are set and for every clock cycle it is asserted that the value increases by one. Then the inc and enable bit gets reset and the value for a few cycles observed. After that, the reset bit is used to set the counter to zero again. Next the value 0x1e is loaded in the counter. This is done by setting the cnt_in-bus to the given value and set the load and enable bits. Then the counter is checked if it is again increasing when setting the corresponding bits. As can be seen in figure 2, all specifications are met.

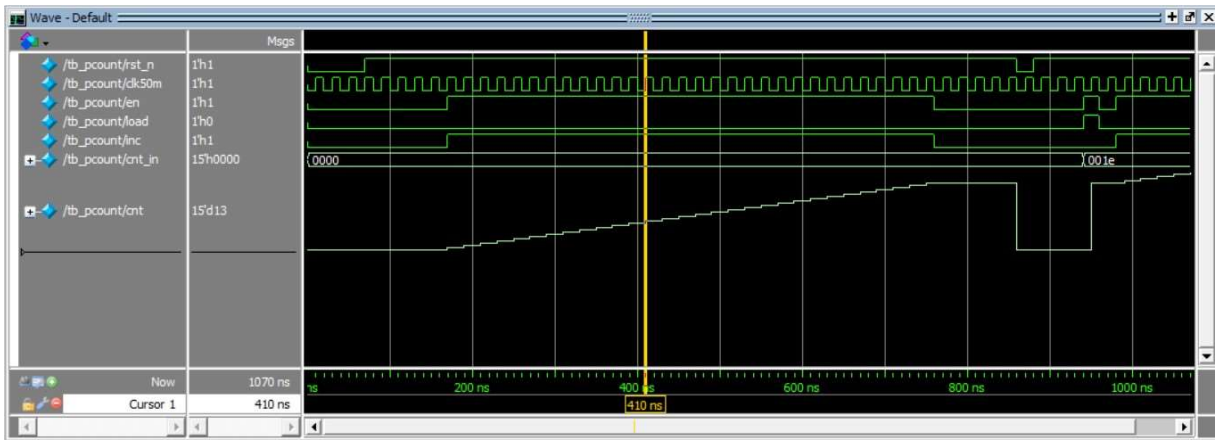


*Figure 2: Test of the program counter*

## Explanation for the 16k RAM test bench

To test the RAM, all the RAM cells are first set to all zeroes and then to all ones. To write, the wren bit is set. In the same time frame the data is set to all zeroes or ones. Then the address is increased every clock cycle. The values are written to the whole block and afterwards read. To accomplish this the wren bit is reset and all address values get read and checked. Because of this the test end message has 49 152 successful tests. This is three times the whole RAM block.

The third test was to write to each address their address as value. The same procedure is used to check all these values.

As can be seen in figure 3, the RAM block functions as intended.

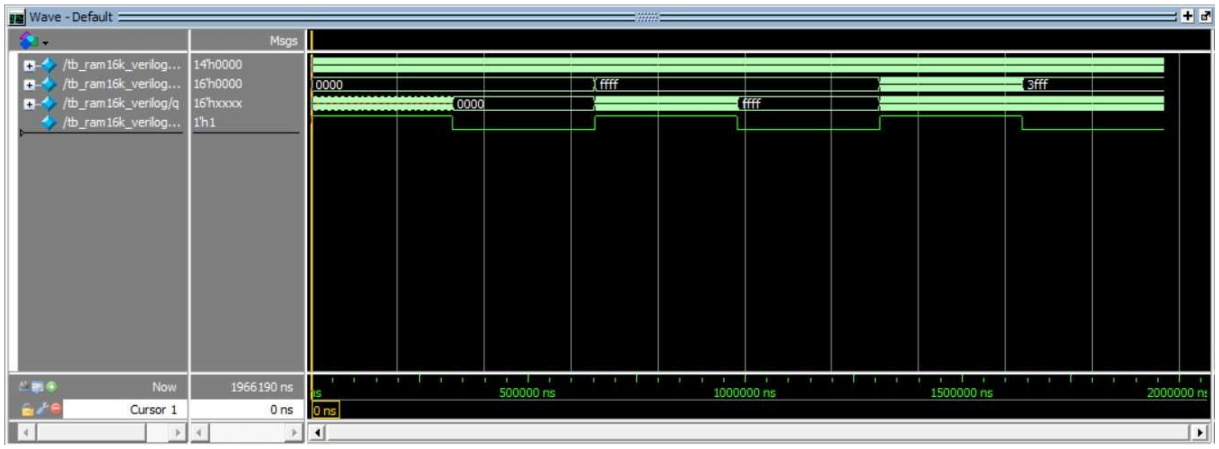


*Figure 3: Test for the RAM block*

## Implementation method

The implementation method used for the program counter and the data register was to adapt a D-flip-flop. As of now, there is no other method known to the student to implement the given task.