ETDB – WS23 HDL

## Report for the implementation of a UART RX Module

## Specification verification for the UART RX Module

For the specification verification, two separate testing procedures were used. First there were two commands used as forced input for the RX-Module. Here, the data as was sent and everything was okay. As can be seen in figure XXX, the data was sent and read as specified.

The second test case was to send data and then interrupt and force the stop bit low for at least one cycle. When this was tested, the expected error signal can be seen at the specified logic line.

As a third test, the four signals a5, 5a, ff and 00 were tried to send without any error. The data was stored in a structure and then applied one by one to the referring channel. As can also be seen in figure XXX, the specification is fully met.

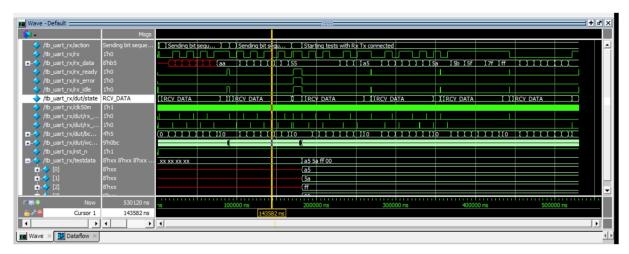


Figure 1: Data sending and receiving with the programmed modules.

## Implementation of the UART RX Module

For implementation the following procedure was used: First, get the test data from the referring data structure and put it on to the corresponding bus. This bus is the data\_in of the TX Module. Then the start impulse was applied. After the RX module had a high signal on data ready, the data on the bus is read and compared to the input data. If this is okay, the test I okay.