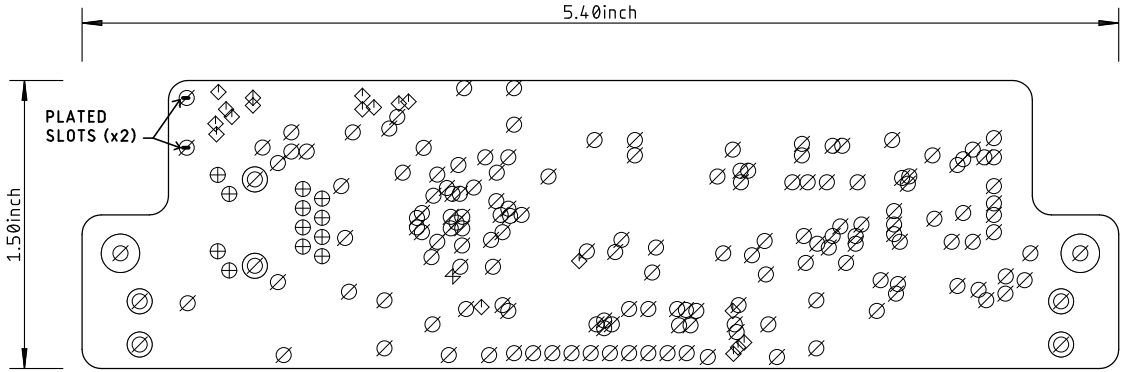
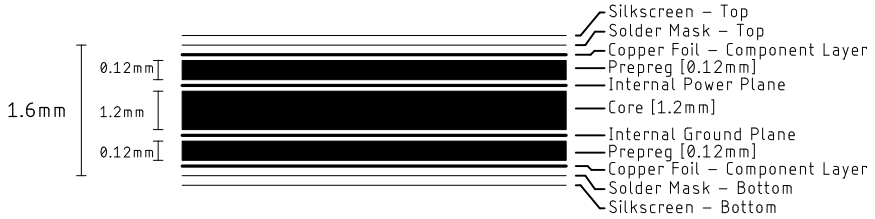
NOTES: (unless otherwise specified)

1. Inches (in) are the controlling dimensions for the drawings and supplied data. Millimeters (mm) dimensions are for reference only.
2. Fabricate PCB in accordance with IPC-6012A, Class 2; per IPC-6011 using customer supplied data files.
3. Materials:
   A) Laminate and Prepreg (B-stage) to be in accordance with IPC-4101/23 or IPC-4101/24. Material must meet UL 94V-0 flammability rating.
   B) Copper foil to be in accordance with IPC-MF-150. Unless otherwise specified, all copper weight for inner layers to be 18um (0.5 oz) and for outer layers 35um (1 oz). Copper weight shall be considered "finished".
4. All holes shall be located within 0.008" (0.2mm) Diameter of True Position. Layer to layer registration shall be within 0.005" (0.125mm).
5. Finish:
   A) All exposed conductive pattern areas not covered with solder mask or other plating shall be Electroless Nickel Immersion Gold (ENIG) plated per IPC-4552.
   B) Apply liquid photo imageable solder mask (color black) per IPC-SM-840, class H, to both sides of the board over bare copper. Via holes covered with solder mask do not need to be plugged.
   C) Only solder mask images that are the same size as the component pads may be enlarged and shall not be enlarged beyond 0.003" (0.08mm) per side or 0.006" (0.15mm) overall. All other solder mask images shall not be enlarged.
   Silkscreen shall be white, permanent, organic, non-conductive ink. There shall be no silkscreen on any solderable component pad.
6. Marking:
   A) Board part number and revision letter is rendered in etch on the bottom side of the board. Revision letter shall be identical to this drawing.
   B) UL logo, manufacturer's identification and date code letter shall be rendered in etch on the bottom side of the board approximately where shown.
7. Test requirements:
   A) 100% netlist electrical verification using customer supplied IPC-D-356 netlist for opens and shorts. All nets shall be accessed simultaneously or as otherwise mutually agreed upon.
   B) HiPot test all prepreg/core material less than 0.004" (0.1mm) thick at 500 Vdc for 30 seconds minimum. Test should be done at the layer stage and again prior to packaging.
8. Tolerances:
   A) Warp or twist of board shall not exceed 1%.
   B) Conductor widths and spacing shall be within ± 0.001" (0.03mm) of Gerber data.
   C) Remove all burrs and break sharp edges 0.015" (0.4mm) maximum.
   D) Surface Mount Pad plating must be flat to a maximum of 0.003" (0.08mm) above board surface.
   E) 0.06" (1.5mm) maximum radius on any inside corner.
9. Thieving:
   A) Supplier may add thieving to compensate for low copper density areas on this design.
   B) The following guidelines must be adhered to in order to maintain electrical and mechanical integrity of the design:
      a. Thieving to card edge spacing 0.100" (2.5mm) minimum.
      b. Thieving to Fiducial spacing 0.200" (5mm) minimum.
      c. Thieving to non-plated through holes 0.200" (5mm) minimum.
      e. Thieving to all other features 0.100" (2.5mm) minimum.
      f. There shall be no exposed thieving in any areas free of solder mask or internal copper plane.





Title:	PCB FABRICATION DETAILS		
Part Name:	BAAAHS Brain Controller		
Part Number:	BAAAHS-BRN01	Revision:	E
Engineer:	TS & AB	Date:	06/23/2019