Report for Computer Assignment 6

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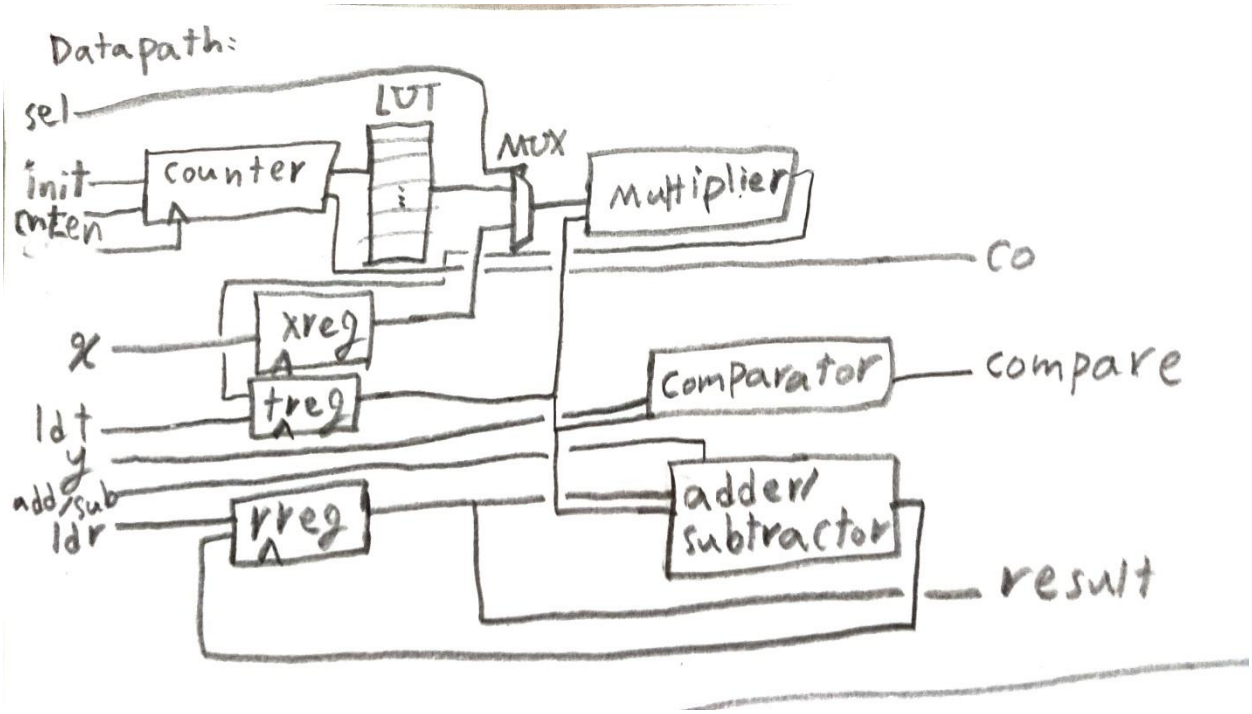
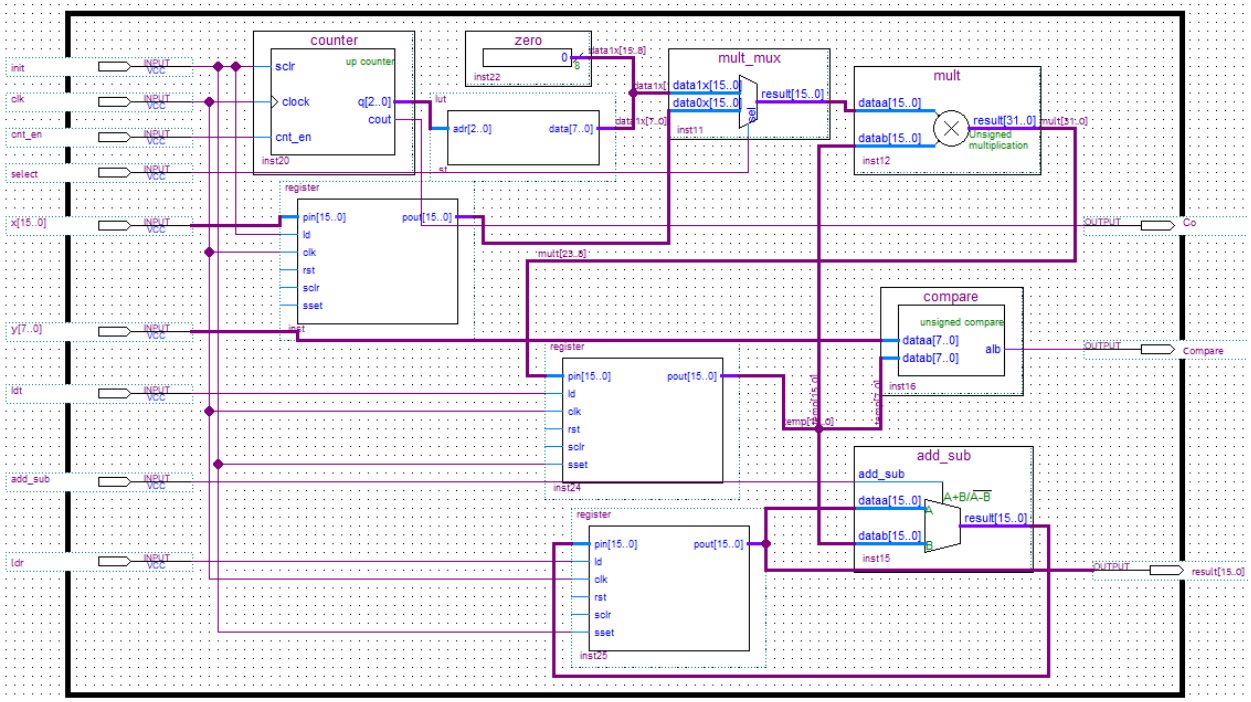
ECE 367 Fall 1402

Datapath:


Datapath:
sel
LUT
init
Counter
MUX
Multiplier
cnten
Co
xreg
x
treg
Comparator
compare
ldt
y
add/sub
ldr
yreg
adder/
subtractor
result


counter
zero
mult_mux
mult
compare
register
add_sub
init
clk
cnt_en
select
x[15..0]
y[7..0]
ldt
add_sub
ldr
INPUT
VCC
sclr
clock
cnt_en
up counter
q[2..0]
cout
inst20
inst22
adr[2..0]
data[7..0]
data1x[15..8]
data1x[7..0]
data1x[15..0]
data0x[15..0]
result[15..0]
inst11
dataa[15..0]
datab[15..0]
result[31..0]
Unsigned multiplication
inst12
mult[31..0]
OUTPUT
Co
pin[15..0]
pout[15..0]
ld
clk
rst
sclr
sset
inst
mult[23..8]
unsigned compare
dataa[7..0]
datab[7..0]
alb
inst16
Compare
inst24
inst25
A+B/A-B
result[15..0]
inst15

Flow Status	Successful - Sat Jan 06 22:06:42 2024
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	cosx
Top-level Entity Name	cosx
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	372 / 14,400 (3 %)
Total registers	51
Total pins	49 / 81 (60 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

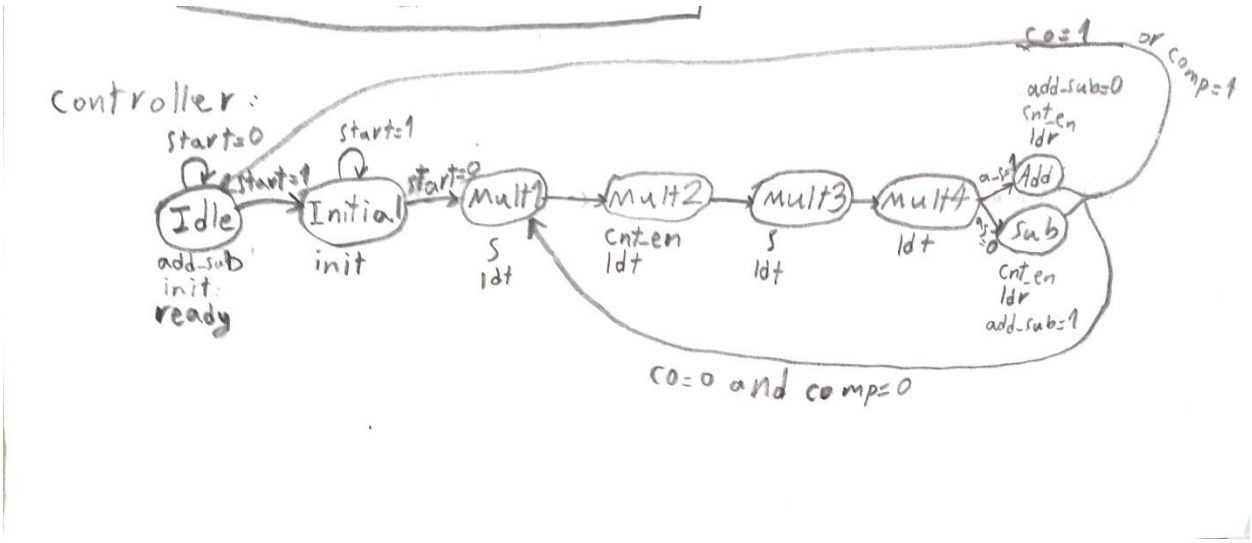
Look Up Table:

```
1   `timescale 1ns/1ns
2   module lut(input [2:0] adr, output [7:0] data);
3       reg [15:0] datat;
4       always @(adr) begin
5           case(adr)
6               0: datat =  16'hFF;// 1/1
7               1: datat =  16'h80;// 1/2
8               2: datat =  16'h55;// 1/3
9               3: datat =  16'h40;// 1/4
10              4: datat =  16'h33;// 1/5
11              5: datat =  16'h2B;// 1/6
12              6: datat =  16'h25;// 1/7
13              7: datat =  16'h20;// 1/8
14          endcase
15      end
16      assign data = datat;
17  endmodule
```

Register:

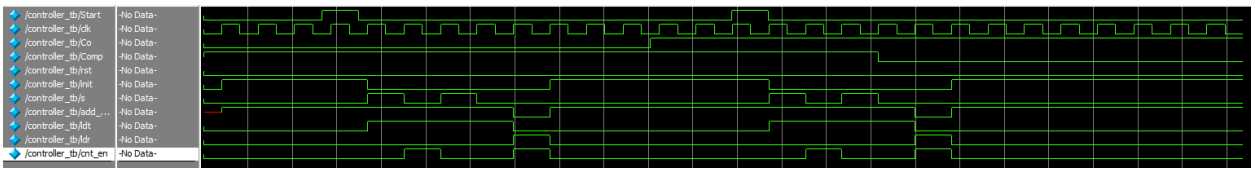
```
`timescale 1ns/1ns
module register(input [15:0] pin, input ld,clk,rst,sclr,sset, output reg [15:0] pout);
    always @(posedge clk, posedge rst) begin
        if(rst)
            pout <= 16'd0;
        else begin
            if(sclr)
                pout <= 16'd0;
            else if(sset)
                pout <= 16'b100000000;
            else if(ld)
                pout <= pin;
        end
    end
endmodule
```

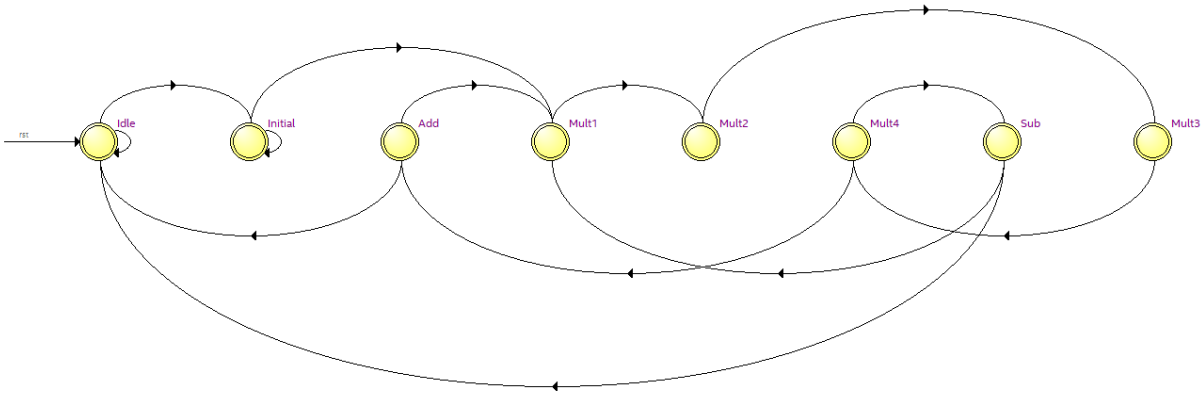
Controller:



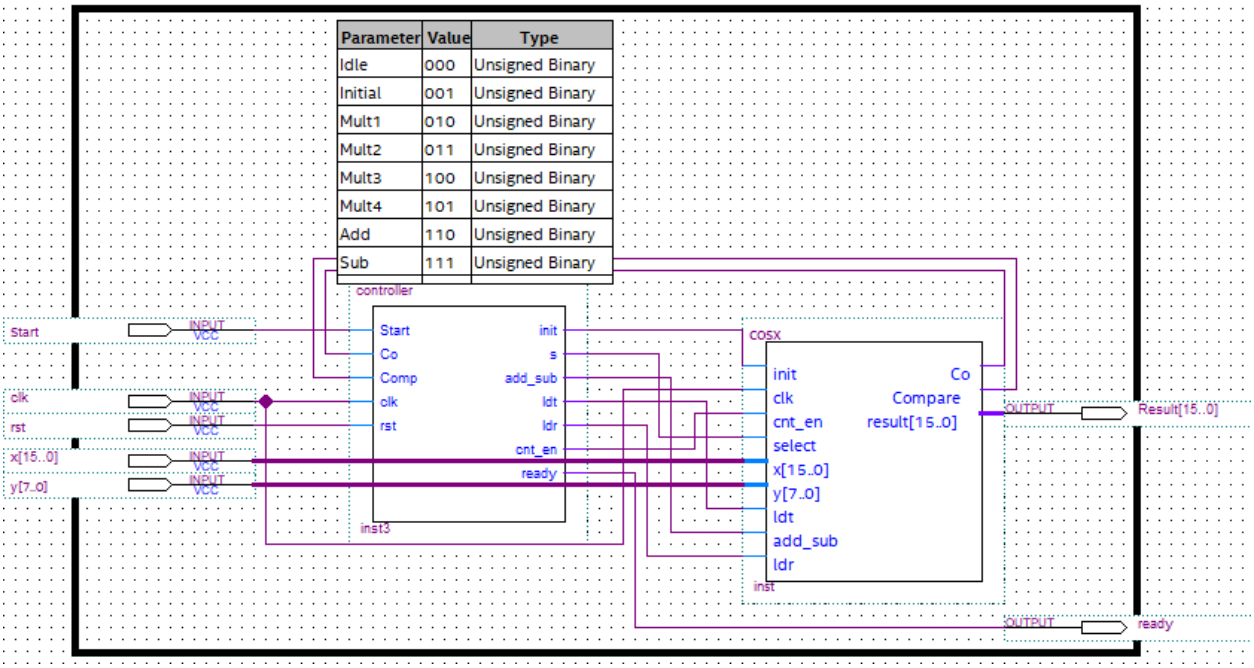
```
`timescale 1ns/1ns
module controller(input Start,Co,Comp,clk,rst, output reg init, s, add_sub,ldt,ldr,cnt_en,ready);
    parameter [2:0] Idle=0,Initial=1,Mult1=2,Mult2=3,Mult3=4,Mult4=5,Add=6,Sub=7;
    reg [2:0] ns,ps;
    always@(ps,Start) begin
        ns=Idle;
        {init,s,ldt,ldr,cnt_en,ready} = 7'b0;
        case (ps)
            Idle: begin ns = Start ? Initial : Idle; add_sub = 1'b1; init = 1'b1; ready=1'b1; end
            Initial: begin ns = Start ? Initial : Mult1; init = 1'b1; end
            Mult1: begin ns = Mult2; s=1'b1; ldt=1'b1; end
            Mult2: begin ns = Mult3; cnt_en=1; ldt=1'b1; end
            Mult3: begin ns = Mult4; s=1'b1; ldt=1'b1; end
            Mult4: begin ns = add_sub ? Add : Sub; ldt=1'b1; end
            Add: begin ns = Co ? Idle : Comp ? Idle : Mult1; cnt_en=1; ldr=1'b1; add_sub = 1'b0; end
            Sub: begin ns = Co ? Idle : Comp ? Idle : Mult1; cnt_en=1; ldr=1'b1; add_sub = 1'b1; end
            default: ns= Idle;
        endcase
    end
    always@(posedge clk, posedge rst) begin
        if(rst)
            ps<=Idle;
        else
            ps<=ns;
    end
endmodule
```

```
1   `timescale 1ns/1ns
2   module controller_tb();
3       reg Start=0,clk=0,Co=0,Comp=1,rst=0;
4       wire init,s,add_sub,ldt,ldr,cnt_en,ready;
5       controller ctrl(Start,Co,Comp,clk,rst,init,s,add_sub,ldt,ldr,cnt_en,ready);
6       always begin #41;clk=~clk;end
7       initial begin
8           #82;
9           #82;
10          #82;
11          #20; Start = 1;
12          #82; Start=0;
13          #82;
14          #82;
15          #82;
16          #82;
17          #82;
18          #82;
19          #82;
20          #82; Co = 1;
21          #82;
22          #82;
23          #20; Start = 1;
24          #82; Start=0;
25          #82;
26          #82;
27          #82;Comp=0;
28          #820;
29          $stop;
30      end
31  endmodule
```

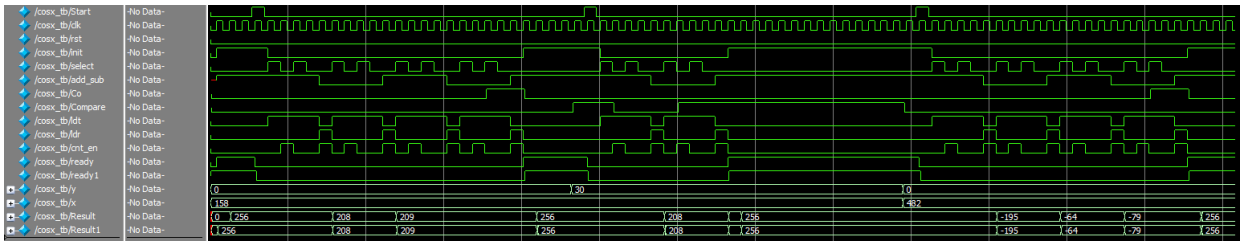




Datapath with Controller:




```
`timescale 1ns/1ns
module cosx_tb();
    reg Start=0,clk=0,rst=0;
    wire init,select,add_sub,Co,Compare,ldt,ldr,cnt_en,ready,ready1;
    reg [7:0] y=8'b0;
    reg [15:0] x=16'b0000000010011110;//0.6171875 -> cos -> 0.81550939694 -> 00000000.11010000
    wire [15:0] Result;
    wire [15:0] Result1;
    controller ctrl(Start,Co,Compare,clk,rst,init,select,add_sub,ldt,ldr,cnt_en,ready);
    cosx dp(Co,init,clk,cnt_en,Compare,y,ldt,select,x,Result,ldr,add_sub);
    cosx_with_controller t(ready1,Start,clk,x,y,rst,Result1);
    always begin #41;clk=~clk;end
    initial begin
        #82;
        #82;
        #82;
        #20; Start = 1;
        #82; Start=0;
        #1640;
        #82;
        #82;
        #82;
        #82; y=8'b00011110;
        #82; Start = 1;
        #82; Start=0;
        #1640;
        #82;
        #82;
        #82;#82; y=8'b0; x=16'b0000000111100010;//1.8828125 -> cos -> -0.30697808454 -> 11111111.10110010
        #82; Start = 1;
        #82; Start=0;
        #1640;
        #82;
        #82;
        #82;
        #82;
        $stop;
    end
endmodule
```



Flow Status	Successful - Mon Jan 08 14:05:28 2024
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	complete_cosx
Top-level Entity Name	cosx_with_controller
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	381 / 14,400 (3 %)
Total registers	59
Total pins	44 / 81 (54 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)