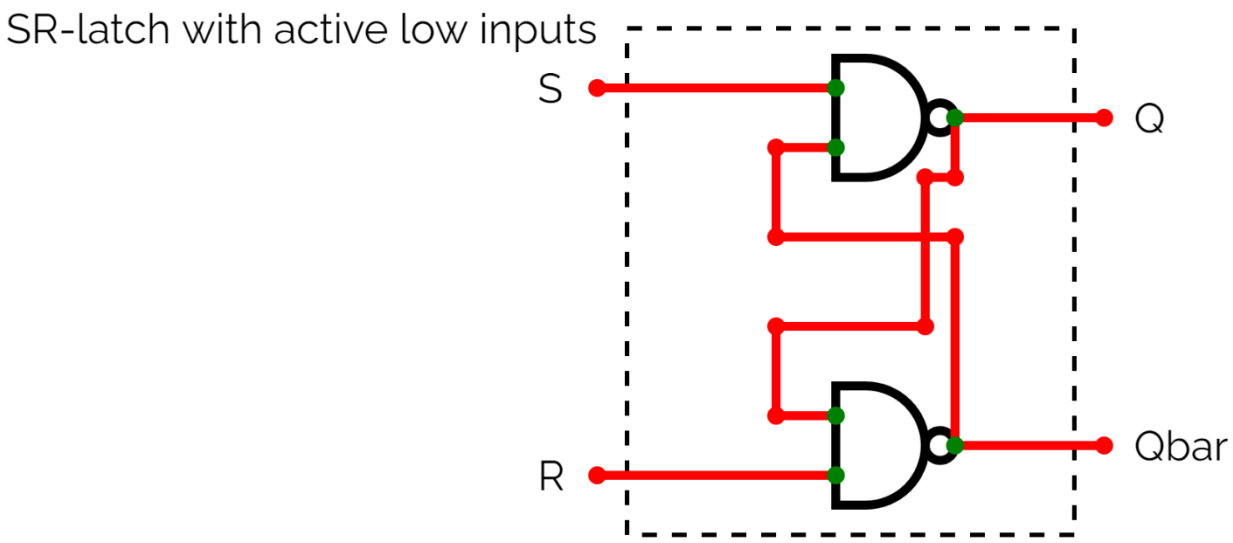
Report for computer assignment #4

Babak Hosseini Mohtasham

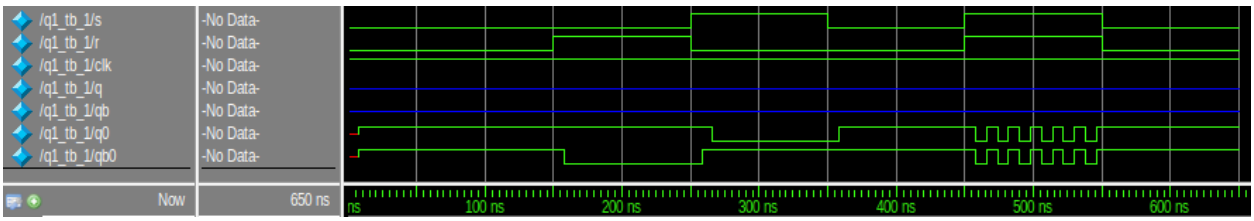
810101408

1.



```
1  `timescale 1ns/1ns
2  module q1_sr_latch_1 #(parameter q_inputs_cnt = 2, qb_inputs_cnt=2) (input S, R, S1,R1, output Q, Qb);
3      nand #(q_inputs_cnt*4) n0(Q,S,S1,Qb);
4      nand #(qb_inputs_cnt*4) n1(Qb,R,R1,Q);
5  endmodule
```

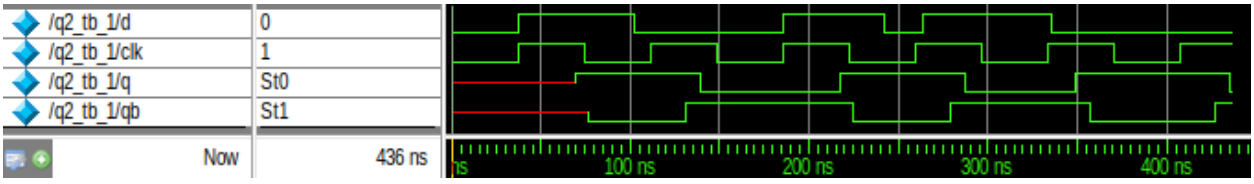
```
1   `timescale 1ns/1ns
2   module q1_tb_1();
3       reg s=1'd0;
4       reg r=1'd0;
5       reg clk=1'd1;
6       wire q,qb;
7       q1_sr_latch_1 #(2,2) a1(s,r,clk,clk,q0,qb0);
8       initial begin
9           s=0; r=0;
10          #50; s=0; r=0;
11          #50; s=0; r=0;
12          #50; s=0; r=1;
13          #50; s=0; r=1;
14          #50; s=1; r=0;
15          #50; s=1; r=0;
16          #50; s=0; r=0;
17          #50; s=0; r=0;
18          #50; s=1; r=1;
19          #50; s=1; r=1;
20          #50; s=0; r=0;
21          #50; s=0; r=0;
22          #50;
23      end
24  endmodule
```



2.

```
`timescale 1ns/1ns
module q2_edge_trigger(input D, clk, output Q, Qb);
    wire q0,qb0,q1,qb1;
    wire z=1'd1;
    q1_sr_latch_1 #(3,2) a0(qb1,D,clk,z,q0,qb0);
    q1_sr_latch_1 #(2,2) a1(qb0,clk,z,z,q1,qb1);
    q1_sr_latch_1 #(2,2) a2(qb1,q0,z,z,Q,Qb);
endmodule
```

```
`timescale 1ns/1ns
module q2_tb_1();
    reg d=1'd0;
    reg clk=1'd0;
    wire q,qb;
    q2_edge_trigger a1(d,clk,q,qb);
    always #37 clk=~clk;
    initial begin
        d=0;
        #37; d=1;
        #37; d=1;
        #28; d=0;
        #83; d=1;
        #20;
        #37; d=0;
        #22; d=1;
        #72; d=0;
        #100; $stop;
    end
endmodule
```



Setup time of 0 to 1=0ns

Setup time of 1 to 0=10ns

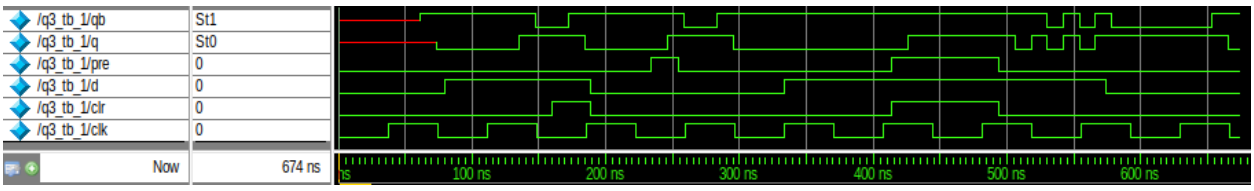
Hold time of 0 to 1=0ns

Hold time of 1 to 0=4ns

3.

```
`timescale 1ns/1ns
module q3(input D, clk,pre,clr, output Q, Qb);
    wire q0,qb0,q1,qb1;
    q1_sr_latch_1 #(3,3) a0(qb1,D,clk,clr,q0,qb0);
    q1_sr_latch_1 #(3,3) a1(qb0,clk,pre,clr,q1,qb1);
    q1_sr_latch_1 #(3,3) a2(qb1,q0,pre,clr,Q,Qb);
endmodule
```

```
`timescale 1ns/1ns
module q3_tb_1();
    reg d=1'd0;
    reg pre=1'd0;
    reg clr=1'd0;
    reg clk=1'd0;
    wire q,qb;
    q3 a1(d,clk,~pre,~clr,q,qb);
    always #37 clk=~clk;
    initial begin
        d=0; clr=0; pre=0;
        #50;
        #30; d=1;
        #80; clr=1;
        #29; d=0; clr=0;
        #45; pre=1;
        #20; pre=0;
        #80; d=1;
        #80; clr=1; pre=1;
        #80; pre=0; clr=0;
        #80; d=0;
        #100; $stop;
    end
endmodule
```



When D changes from 0 to 1 delay of:

Q=24 and Qbar=36ns

When D changes from 1 to 0 delay of:

Q=36 and Qbar=24ns

When CLR changes from 0 to 1 delay of:

Q=24 and Qbar=12ns

When PRE changes from 0 to 1 delay of:

Q=12 and Qbar=24ns

When both CLR and PRE change from 0 to 1 the delay is:12ns