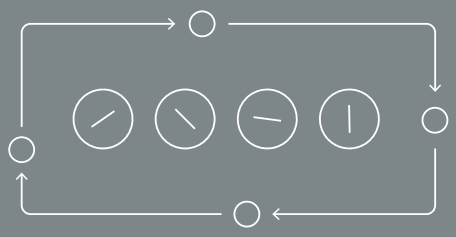
Jawaharlal Nehru Technological University



Optimization For noise reduction In a Five-Level Cascaded H-Bridge Inverter Using Genetic Algorithms for Harmonic Reduction

1. Theoretical Study and Understanding

OBJECTIVE

To understand the principles of MLIs, their advantages (e.g., reduced harmonic distortion, lower dv/dt), and the specific cascaded H-bridge topology used for generating multiple voltage levels.

KEY CONCEPTS

Multilevel inverters generate stepped waveforms using multiple voltage levels, improving power quality compared to two-level inverters.

- The cascaded H-bridge topology uses multiple H-bridges connected in series, each with a separate DC source. For a five-level inverter, the formula for output levels is 2s+1, where s is the number of H-bridges per phase (here, s=2, yielding 5 levels: $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$).
- Selective Harmonic Elimination (SHE) was identified as a technique to reduce specific harmonics (e.g., 5^{th} and 7^{th}) by determining optimal switching angles.

OUTCOME

A solid theoretical foundation was established, guiding the subsequent simulation and hardware phases.

2. Simulation Model Development

SETUP

The model included two H-bridges per phase, each fed by a separate DC source (e.g., E_{dc1}= E_{dc2} =48V), connected in series to produce the five-level output.

COMPONENTS

The simulation incorporated power switches (e.g., MOSFETs) and pulse generators to control switching.

PARAMETERS

The output frequency was set to 50 Hz (time period = 20 ms), and initial switching angles were chosen arbitrarily for testing.

PURPOSE

To simulate the inverter’s behavior and generate an output waveform for analysis.

3. Initial Simulation Run

SWITCHING ANGLES

α1=25∘ and α2=70∘.

PULSE GENERATOR SETTINGS

Pulse width
= 50% of the period (10 ms)

Phase delays calculated as:

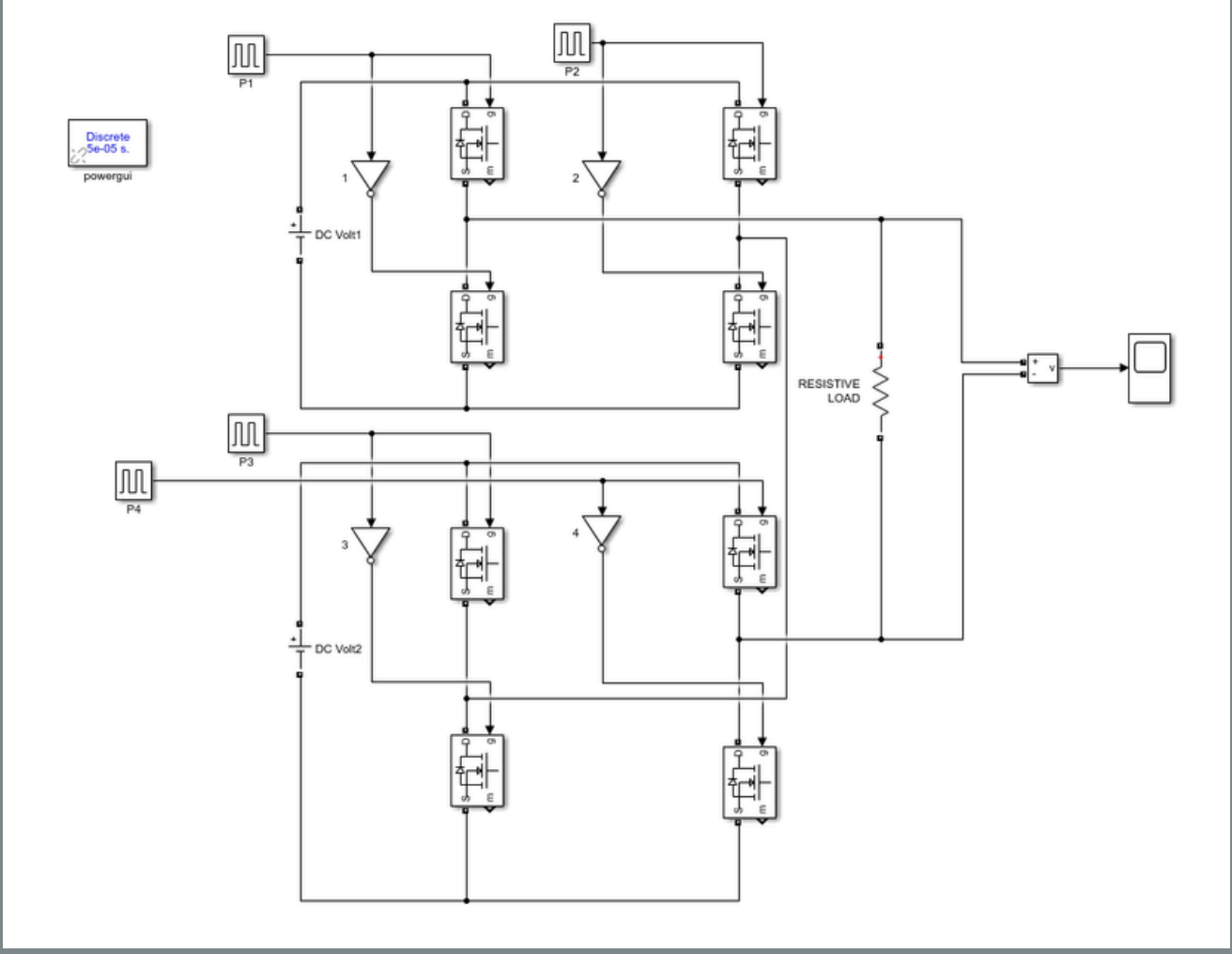
Delay for 25∘
= (25×20) / 360 = 1.388ms

Delay for 70∘
= (70×20) / 360 = 3.88ms

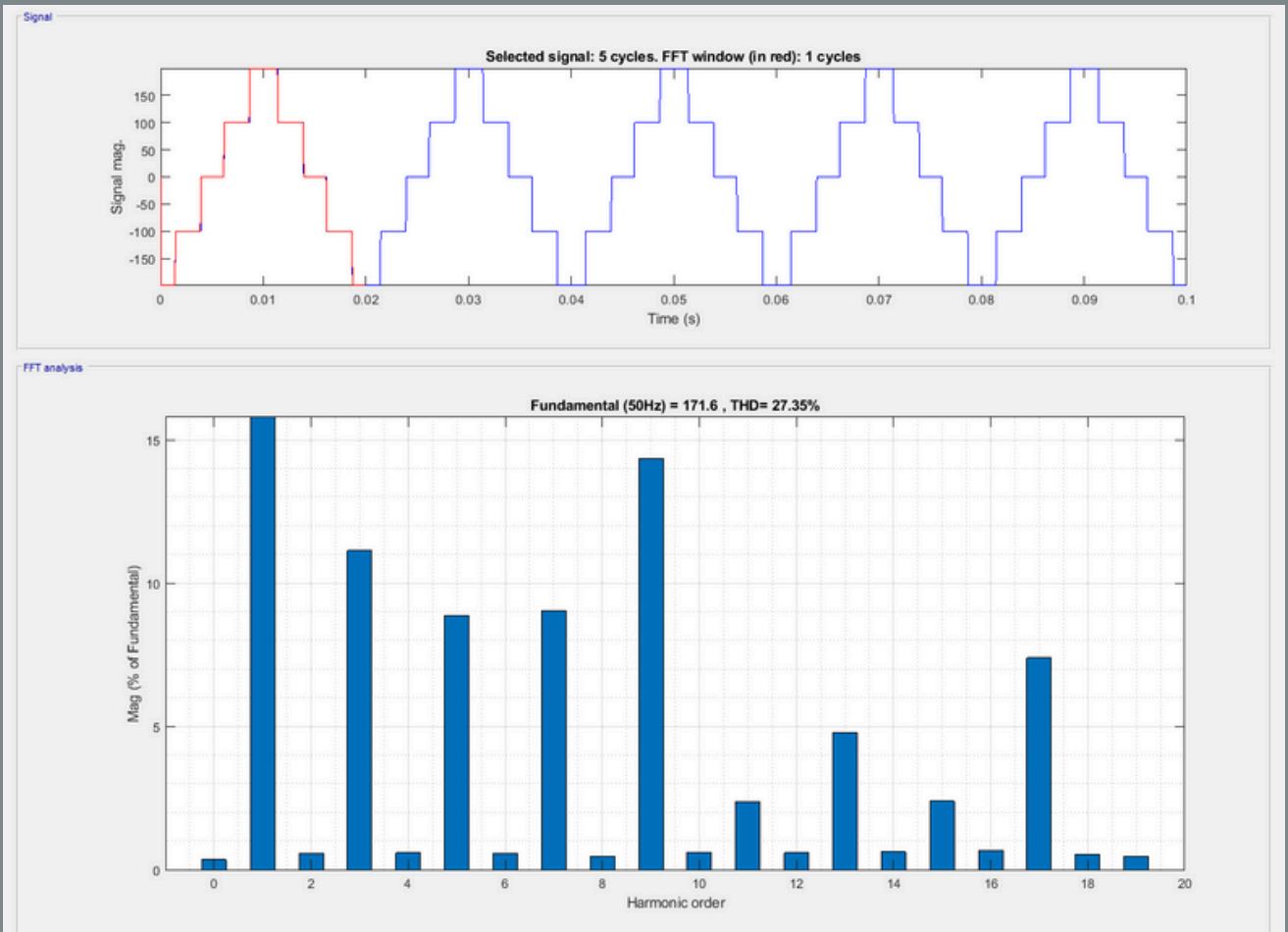
ANALYSIS

The output waveform was analyzed using Fast Fourier Transform (FFT). The Total Harmonic Distortion (THD) was 27.35%, with significant 5th and 7th harmonics.

SIMULATION MODEL



OUTPUT


Signal
Selected signal: 5 cycles. FFT window (in red): 1 cycles
Signal mag.
150
100
50
0
-50
-100
-150
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1
Time (s)
FFT analysis
Fundamental (50Hz) = 171.6 , THD= 27.35%
Mag (% of Fundamental)
15
10
5
0
0
2
4
6
8
10
12
14
16
18
20
Harmonic order

4. Selective Harmonic Elimination (SHE) Equation Formulation

EQUATIONS

$\cos(\alpha_1) + \cos(\alpha_2) = 2mI$
(controls the fundamental voltage, where mI is the modulation index)

$\cos(5\alpha_1) + \cos(5\alpha_2) = 0$
(eliminates the 5th harmonic)

$\cos(7\alpha_1) + \cos(7\alpha_2) = 0$
(eliminates the 7th harmonic)

CONSTRAINT

$0 < \alpha_1 < \alpha_2 \leq 90^\circ$.

PURPOSE

To find switching angles that minimize the specified harmonics while maintaining the desired fundamental voltage.

5. Genetic Algorithm Application

PROCESS

Chromosome Representation
Each chromosome represented a set of switching angles (α_1, α_2).

Population Initialization
A population of 200 random solutions was generated.

Fitness Function
Designed to minimize the 5th and 7th harmonics and THD,
e.g., $y=[10 \times (1.2738 \times \cos(\alpha_1) + 0.254 \times \cos(5\alpha_1))]$.

Evolution
Through reproduction, crossover, and mutation, the GA evolved the population over generations to optimize the angles.

RESULT

$\alpha_1=36^\circ$ and $\alpha_2=72^\circ$.

6. Optimized Simulation

SWITCHING ANGLES

α_1=36° and α_2=72°.

PULSE GENERATOR SETTINGS

Pulse width
= 50% (10 ms).

Phase delays:

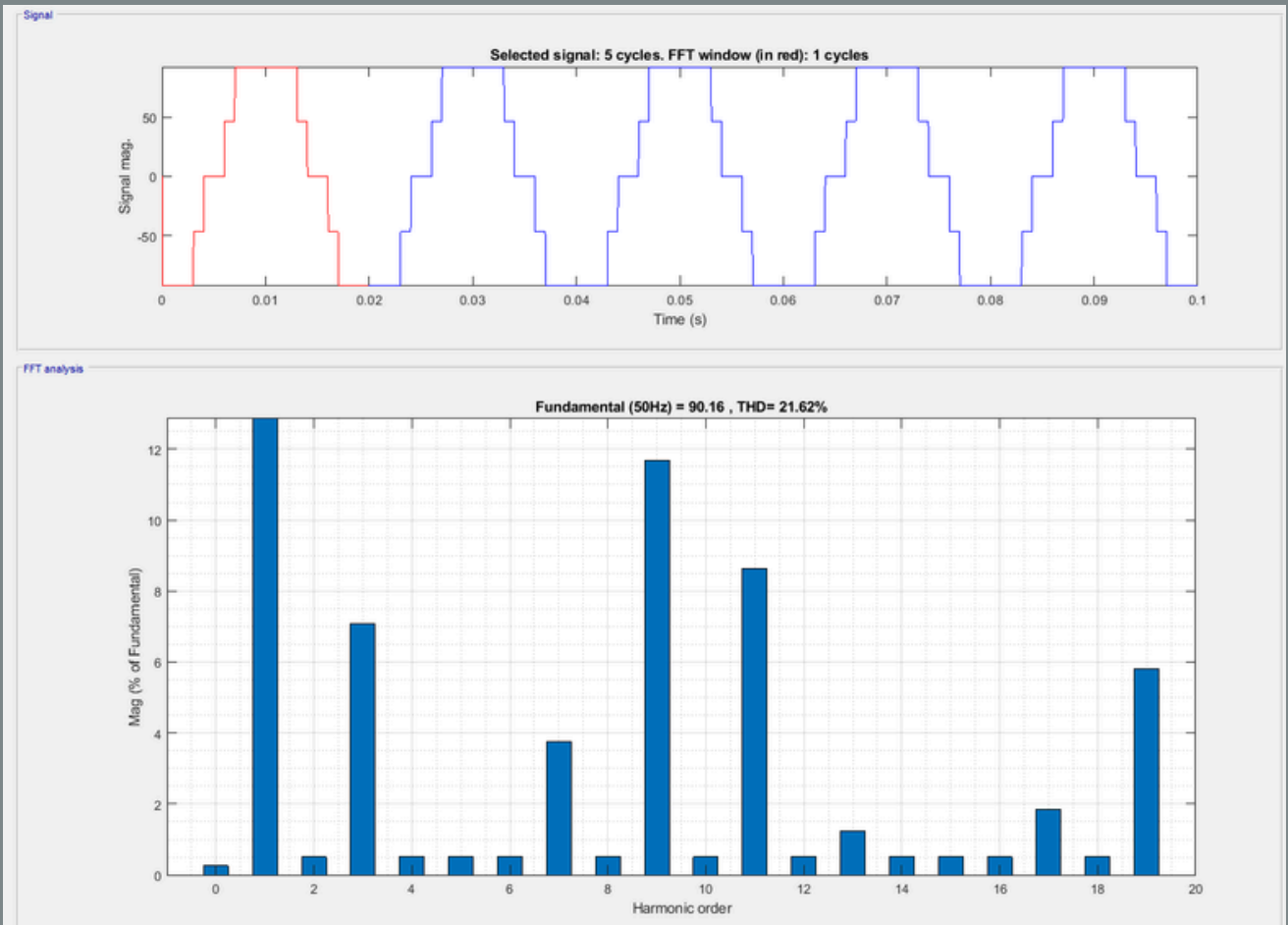
For 36∘
= (36×20)/360 = 2ms

For 72∘
= (72×20)/360 = 4ms

ANALYSIS

A Reduced THD of 21.62%, with the 5th and 7th harmonics significantly minimized.

OUTCOME



The simulation confirmed the effectiveness of the GA-optimized angles in improving waveform quality.

7. Hardware Design

COMPONENTS

H-Bridges
Two H-bridges, each with four MOSFETs (IRF740) and LEDs for status indication.

Optocouplers (4N35)
For isolating the control signals from the power circuit.

Microcontroller (Arduino)
To generate firing pulses.

Power Supply
A 230/48V AC transformer, rectified to 48V DC per H-bridge (max output = 96V).

Rectifiers and Capacitors
1000 µF, 100V capacitors to filter ripple.

Load
A 10W bulb (resistive load), though the system can drive up to 400V, 10A loads.

PURPOSE

To physically implement the simulated inverter and test real-world performance.

8. Hardware Assembly

CONNECTIONS

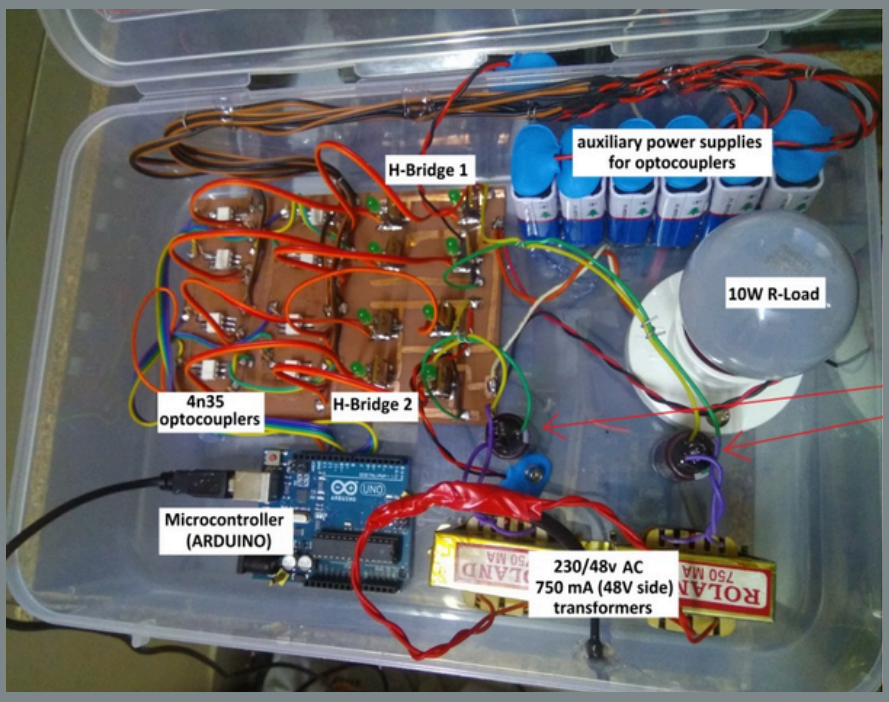
Each H-bridge was powered by a 48V DC source from the transformer and rectifier circuit.

Optocouplers linked the Arduino to the MOSFET gates for safe signal transmission.

The two H-bridges were connected in series to produce the five-level output.

RESULT

A complete hardware prototype ready for testing.



9. Microcontroller Programming

SETTINGS

Frequency = 50 Hz (period = 20 ms).

Phase delays for α_1=36° and α_2=72°:
2ms and 4ms, respectively.

PIN CONFIGURATION

First H-bridge:
S11 (Pin 13), S12 (Pin 10),
S13 (Pin 12), S14 (Pin 11).

Second H-bridge:
S21 (Pin 13), S22 (Pin 10),
S23 (Pin 12), S24 (Pin 11).

COMPLEMENTARY SWITCHING

Switches in each leg (e.g., S11 and S12) operated complementarily.

RESULT

The Arduino successfully controlled the MOSFETs to produce the desired five-level waveform.

10. Hardware Testing

INITIAL TEST

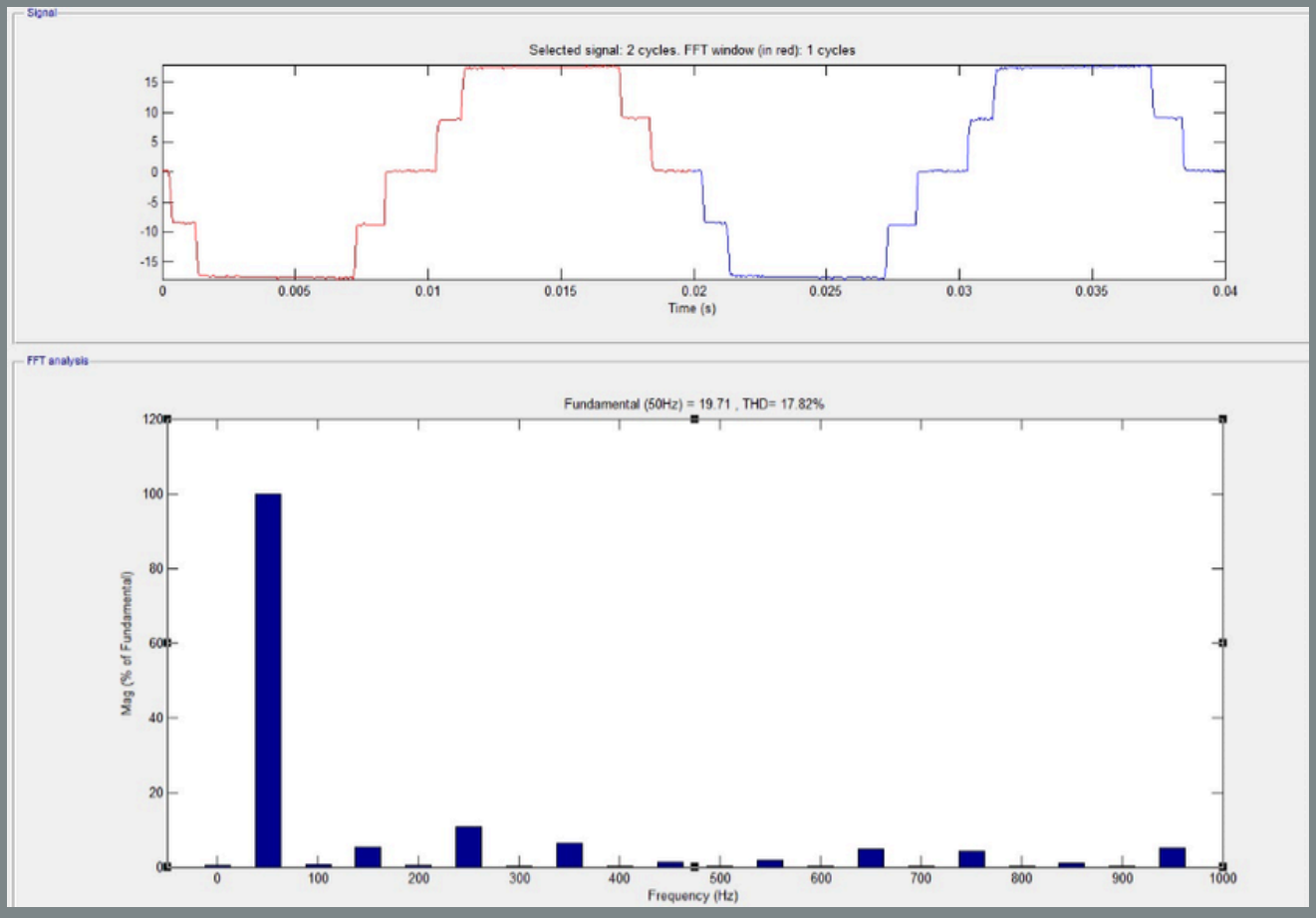
α_1=25° and α_2=70°.

OPTIMIZED TEST

α_1=36° and α_2=72°.

RESULT

Optimized THD of 17.82%, lower than the simulation's 21.62%, indicating effective harmonic reduction.



11. Result Comparison and Analysis

THD COMPARISON

Initial simulation
27.35%.

Optimized simulation
21.62%.

Hardware with optimized angles
17.82%.

FINDINGS

The GA-optimized angles significantly reduced the 5^{th} and 7^{th} harmonics in both simulation and hardware.

The hardware THD was lower than the simulation, possibly due to real-world filtering effects.

CONCLUSION

The project successfully demonstrated the effectiveness of SHE with GA in reducing harmonics, achieving a high-quality output suitable for loads up to 400V, 10A.