**BUSITEMA UNIVERSITY**

**FACULTY OF ENGINEERING**

**DEPARTMENT OF COMPUTER ENGINEERING**

**ASSIGNMENT**

**COMPUTER ORGANISATION**

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**Question one**

1. **Justify why does DMA have priority over the CPU when both request memory transfer**

The transfer of data between a fast storage device such as a magnetic disk and memory is often limited by speed of the CPU. Since the goal of computer design is to optimize throughput, removing the CPU from the path and letting the peripheral mange the memory buses directly using DMA improves the speed of transfer. Therefore, DMA is given priority because it offers the fastest transfer compare the CPU.

1. **Write short notes on RS-232 C IEEE 488 USB**

RS-232 is an established standard that describes the physical interface and protocol for relatively low speed serial data communication between computers and related devices. It is an interface that the computer uses to exchange data with serial devices like a modem, USB flash disk etc. data is transferred using UART chip from the computer to an internal or external serial device from its Data Terminal Equipment (DTE) interface. The UART coverts parallel streams of bits to serial streams of bits. As the computer’s DTE agent, it also communicates with the modem or other serial device, which in accordance with RS-232C standard has a complimentary interface called the Data Communications Equipment (DCE) interface.

OR

This is a standard originally introduced in 1990 for serial communication transmission of data. It formally defines signals connecting between DTE (Data Terminal Equipment) such as a computer and a DCE (Data Communication Equipment) such as a modem. The standard defines characteristics and timing of signals, meaning of signals, physical size and pinout of connectors.

Compared with later interfaces such as RS-422, RS-485 and ethernet, RS-232 has lower transmission speeds, shorter cable length, larger voltage swings and larger standard connectors.

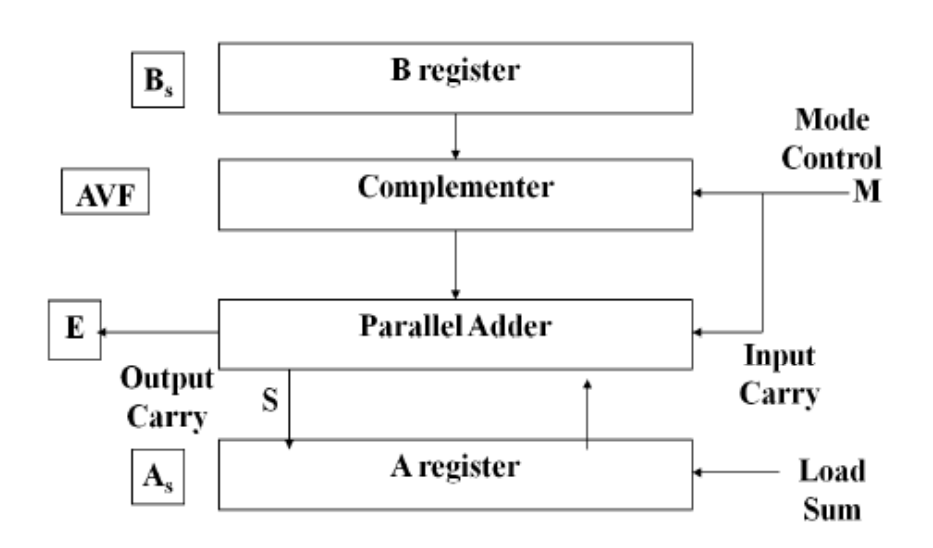
1. **What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without interrupt?**

In interrupt driven data transfer, whenever I/O device is ready for data transfer, it will interrupt the CPU and in the ISR, the CPU will perform the data transfer. This method is efficient as the CPU does not have to waste time on checking if the I/O devices are ready hence giving better performance.

On the other hand, program-based data transfer slows down other tasks being executed a s the processor ha s to keep checking if the I/O devices are ready for data transfer from time to time.

For example instead of CPU checking, when the data is available on the keyboard, the keyboard should interrupt the CPU when a key is pressed. Thus time will not be wasted in repeatedly checking the keyboard when the user is not typing at all.

1. **Describe the design of the hardware of addition and subtraction of fixed point signed magnitude numbers.**



To implement the two arithmetic operations with hardware, we have to store numbers into two registers A and B. Let As and Bs be two flip-flops that hold the corresponding signs. The results are transferred to A and As. A and as together form an accumulator.

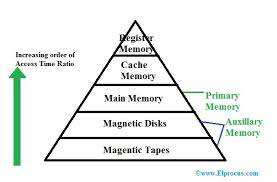
We need: Two registers A and B and sign flip-flops As and Bs, an A magnitude comparator: to check if A>B, A<B, or A = B. an A parallel adder: to perform A+B and two parallel subtractions: for A-B and B-A. The sign relationships are determined from an X-OR gate with As and Bs as inputs.

**Question two**

1. **Distinguish between hardwired controlled unit and micro programmed controlled unit**

|  |  |
| --- | --- |
| **Hardwired control unit** | **Microprogrammed control Unit** |
| Hardwired control unit generates the control signals needed for the processor using logic circuits | Microprogrammed control unit generates the control signals with the help of micro instructions stored in control memory |
| Hardwired control unit is faster because control signals are generated with help of hardware | This is slower as micro-instructions are used to generate signals |
| Difficult to modify as the control signals that need to be generated are hard wired | Easy to modify as the modification need to be done only at the instruction level |
| More expensive as everything has to be implemented in logic | Less costly as only micro-instructions are used |
| It cannot handle complex instructions as the circuit design for it becomes complex | It can handle complex instructions |
| Used in computer that makes use of Reduced Instruction Set Computers(RISC) | Used in computer that makes use of Complex Instruction Set Computers(CISC) |

1. **Expound on the design of the memory hierarchy in a computer system**



In the Computer System Design, Memory Hierarchy is an enhancement to organize the memory such that it can minimize the access time. Memory hierarchy affects performance in computer architecture design, algorithm predictions, and lower-level programming constructs involving locality of reference. The Memory Hierarchy was developed based on a program behavior known as locality of references. The total memory capacity of a computer can be visualized by hierarchy of components. The memory hierarchy system consists of all storage devices contained in a computer system from the slow Auxiliary Memory to fast Main Memory and to smaller Cache memory.

1. **Explain the importance of different addressing modes in computer architecture with suitable example.**

|  |  |
| --- | --- |
| Addressing | Application |
| Immediate addressing mode | To initialize registers to a constant value |
| Direct addressing mode and register direct addressing mode | To access static data  To implement variables |
| Indirect addressing mode and Register indirect addressing mode | To implement pointers because pointers are memory locations that store the address of another variable  To pass array as a parameter because array name is the base address and pointer is needed to point the address |
| Relative addressing mode | For program relocation at run time i.e. for position independent code  To change the normal sequence of execution of instructions  For branch type instructions since it directly updates the program counter |
| Index addressing | For array implementation or array addressing  For records implementation |
| Base register addressing mode | For writing relocatable code i.e. for relocation of program in memory even at run time  For handling recursive procedures |

1. **Describe how you can illustrate the performance of memory**

RAM performance is all about the relationship between speed and latency. Latency refers to time delay between when a command is entered and when the data is available

**Question three**

1. **Explain two design elements of a bus and state their performance effect to the computer system**

**Bus Width**

The width of the data has an impact on system execution. The wider the data bus, the higher the number of bits moved at one time. The width of the address bus has an impact on system capacity, that is, the wider the address bus, the higher the dimension of locations that can be referenced.

**Bus Types**

Bus lines can be reported into two generic types are dedicated and multiplexed. A dedicated bus line is permanently authorized either to one function or a physical subgroup of computer components. A multiplexed bus line is assigned too many functions based on some parameters.

1. **Explain four cases which can result into generation of an interrupt during execution of a program.**

I/O devices tell the CPU that an I/O request h l t d b di t has completed by sending an interrupt signal to the processor. • I/O errors may also generate an interrupt. • Most computers have a timer which interrupts the CPU every so many interrupts the CPU every so many milliseconds.

When the hardware detects that the program is doing something wrong, it will usually generate an interrupt usually generate an interrupt. – Arithmetic error - Invalid Instruction – Addressing error - Hardware malfunction – Page fault - Debugging • A Page Fault interrupt is not the result of a program error, but it does require the operating system to get control. • Internal interrupts are sometimes called exceptions.

Most computers have an instruction that generat i t li t t tes an internal interrupt. • Program generated interrupts are a means for user programs to call a function of the operating system • Some systems refer to these interrupts as Some systems refer to these interrupts as a SuperVisor Call or SVC

1. **A computer has 16MB main memory and 64KB cache. The block size is 16 bytes. Assuming a direct mapping technique is used:**
2. How many cache lines does the computer have?

Lines = cache size/ block size

Lines = 64x 1024/16

**Cache lines = 4096 lines**

1. How many blocks does the main memory have?

Blocks = memory size/block size

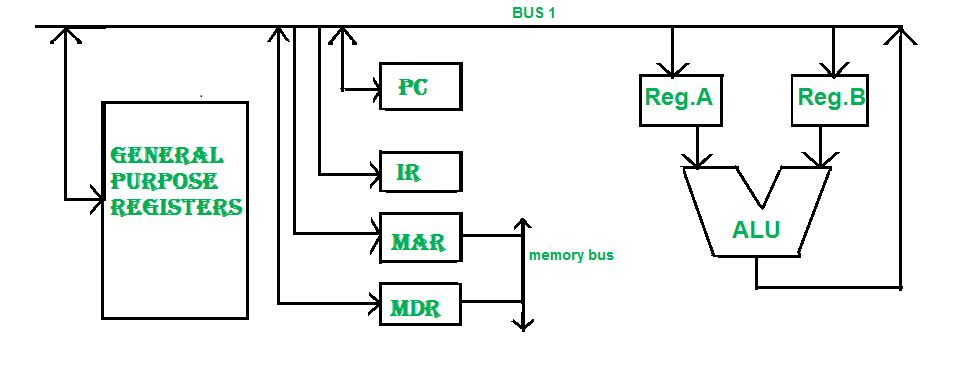
Blocks = 16x 1024x1024/16

**Blocks = 1048576 blocks**

1. Give the starting a dresses of memory blocks which are directly mapped to cache lines.

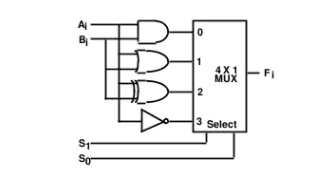
**Question four**

1. **Design a neat labelled diagram of working principle of single bus organization of the data path inside the CPU.**



In one bus organization, a single bus is used for multiple purposes. A set of general-purpose registers, program counters, instruction registers, memory address registers (MAR), memory data registers (MDR) are connected with the single bus. Memory read/write can be done with MAR and MDR. The program counterpoints to the memory location from where the next instruction is to be fetched. Instruction register is that very register will hold the copy of the current instruction. In the case of one bus organization, at a time only one operand can be read from the bus.

1. **Explain the hardware implementation of logical micro operation for AND, OR, XOR and complement logic gates.**



The hardware implementation of logic rnicrooperations requires that logic gates be inserted for each bit or pair of bits in the registers to perform the required logic function. Although there are 16 logic rnicrooperations, most computers use only four-AND, OR, XOR (exclusive-OR), and complement from which all others can be derived.

It consists of four gates and a multiplexer. Each of the four logic operations is generated through a gate that performs the required logic. The outputs of the gates are applied to the data inputs of the multiplexer. The two selection inputs 51 and 50 choose one of the data inputs of the multiplexer and direct its value to the output. The diagram shows one typical stage with subscript i. For a logic circuit with n bits, the diagram must be repeated n times for i = 0, 1, 2, ... , n - 1. The selection variables are applied to all stages. The function table in Fig. 4-10(b) lists the logic rnicrooperations obtained for each combination of the selection variables.

1. **Describe the different types of memory mapping techniques used in cache memory**

**Associative mapping**

In this type of mapping the associative memory is used to store content and addresses both of the memory word. This enables the placement of the any word at any place in the cache memory. It is considered to be the fastest and the most flexible mapping form.

**Direct mapping**

In direct mapping the RAM is made use of to store data and some is stored in the cache. An address space is split into two parts index field and tag field. The cache is used to store the tag field whereas the rest is stored in the main memory. Direct mapping`s performance is directly proportional to the Hit ratio

**Set-associative mapping**

This form of mapping is a modified form of the direct mapping where the disadvantage of direct mapping is removed. Set-associative mapping allows that each word that is present in the cache can have two or more words in the main memory for the same index address.