

SNx4HC138 3-Line To 8-Line Decoders/Demultiplexers

1 Features

- Targeted Specifically for High-Speed Memory Decoders and Data-Transmission Systems
- Wide Operating Voltage Range (2 V to 6 V)
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Maximum I_{CC}
- Typical $t_{pd} = 15$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1- μ A Maximum
- Active Low Outputs (Selected Output is Low)
- Incorporate Three Enable Inputs to Simplify Cascading or Data Reception

2 Applications

- LED Displays
- Servers
- White Goods
- Power Infrastructure
- Building Automation
- Factory Automation

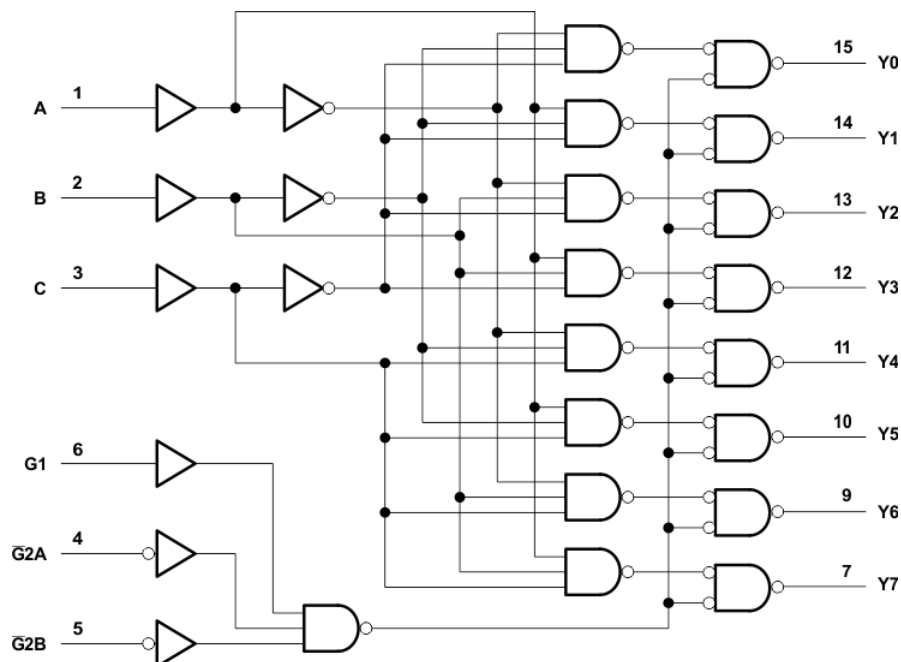
3 Description

The SNx4HC138 devices are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories using a fast enable circuit, the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|--------------------|
| SN74HC138D | SOIC (16) | 9.90 mm x 3.90 mm |
| SN74HC138DB | SSOP (16) | 6.20 mm x 5.30 mm |
| SN74HC138N | PDIP (16) | 19.32 mm x 6.35 mm |
| SN74HC138NS | SO (16) | 10.20 mm x 5.30 mm |
| SN74HC138PW | TSSOP (16) | 5.00 mm x 4.40 mm |
| SN54HC138J | CDIP (16) | 21.34 mm x 6.92 mm |
| SN54HC138W | CFP (16) | 10.16 mm x 6.73 mm |
| SN54HC138FK | LCCC (20) | 8.89 mm x 8.89 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Functional Block Diagram



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Table of Contents

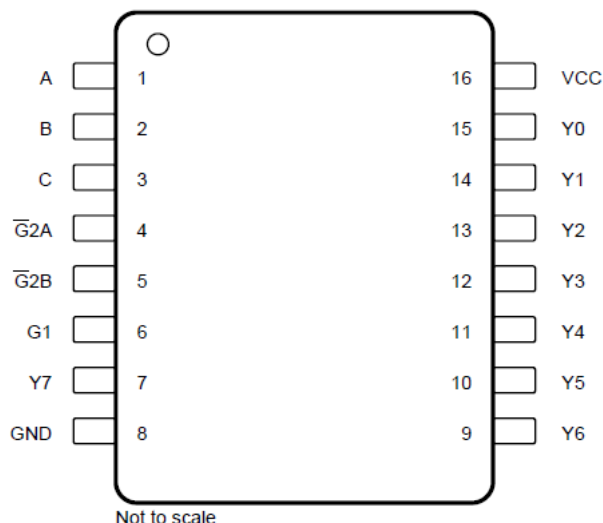
| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 8.1 Overview..... | 9 |
| 2 Applications | 1 | 8.2 Functional Block Diagram..... | 9 |
| 3 Description | 1 | 8.3 Feature Description..... | 9 |
| 4 Revision History | 2 | 8.4 Device Functional Modes..... | 10 |
| 5 Pin Configuration and Functions | 3 | 9 Application and Implementation | 11 |
| Pin Functions..... | 3 | 9.1 Application Information..... | 11 |
| 6 Specifications | 4 | 9.2 Typical Application..... | 11 |
| 6.1 Absolute Maximum Ratings..... | 4 | 10 Power Supply Recommendations | 12 |
| 6.2 ESD Ratings: SN74HC138..... | 4 | 11 Layout | 12 |
| 6.3 Recommended Operating Conditions..... | 4 | 11.1 Layout Guidelines..... | 12 |
| 6.4 Thermal Information: SN74HC138..... | 5 | 11.2 Layout Example..... | 12 |
| 6.5 Thermal Information: SN54HC138..... | 5 | 12 Device and Documentation Support | 13 |
| 6.6 Electrical Characteristics..... | 5 | 12.1 Documentation Support..... | 13 |
| 6.7 Electrical Characteristics: SN74HC138..... | 6 | 12.2 Related Links..... | 13 |
| 6.8 Electrical Characteristics: SN54HC138..... | 6 | 12.3 Receiving Notification of Documentation Updates.. | 13 |
| 6.9 Switching Characteristics..... | 6 | 12.4 Support Resources..... | 13 |
| 6.10 Switching Characteristics: SN74HC138..... | 7 | 12.5 Trademarks..... | 13 |
| 6.11 Switching Characteristics: SN54HC138..... | 7 | 12.6 Electrostatic Discharge Caution..... | 13 |
| 6.12 Typical Characteristic..... | 7 | 12.7 Glossary..... | 13 |
| 7 Parameter Measurement Information | 8 | 13 Mechanical, Packaging, and Orderable Information | 13 |
| 8 Detailed Description | 9 | | |

4 Revision History

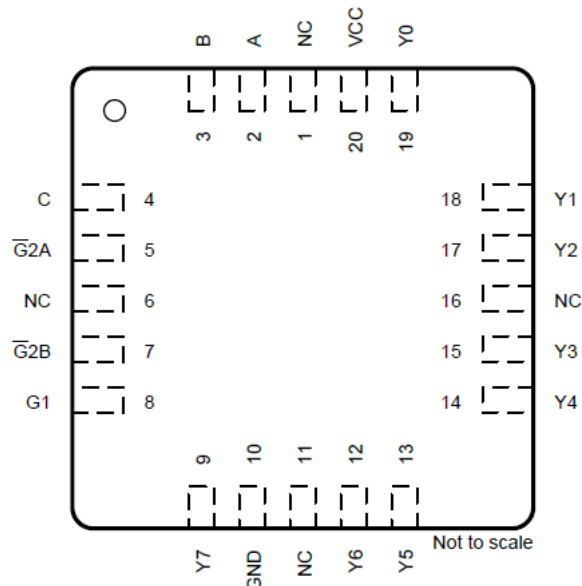
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (September 2003) to Revision F (September 2016) | Page |
|---|-------------|
| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Deleted Ordering Information table; see POA at the end of the data sheet..... | 1 |
| • Changed $R_{\theta JA}$ values from 73 to 87.3 (D), from 82 to 104.3 (DB), from 67 to 54.8 (N), from 64 to 91.1 (NS), and from 108 to 114.6 (PW)..... | 5 |
| Changes from Revision F (September 2016) to Revision G (October 2021) | Page |
| • Updated the ESD ratings table to fit modern data sheet standards..... | 4 |

5 Pin Configuration and Functions



SOIC, SSOP, PDIP, SO, TSSOP, CDIP, or CFP
Package
16-Pin D, DB, N, NS, PW, J or W
Top View



NC: No internal connection
LCCC Package
20-Pin FK
Top View

Pin Functions

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|------------------|--|--------------|--------------------|--|
| | SOIC, SSOP, PDIP, SO, TSSOP, CDIP, CFP | LCCC | | |
| A | 1 | 2 | I | Select input A (least significant bit) |
| B | 2 | 3 | I | Select input B |
| C | 3 | 4 | I | Select input C (most significant bit) |
| $\overline{G2A}$ | 4 | 5 | I | Active low enable A |
| $\overline{G2B}$ | 5 | 7 | I | Active low enable B |
| G1 | 6 | 8 | I | Active high enable |
| GND | 8 | 10 | — | Ground |
| NC | — | 1, 6, 11, 16 | — | No internal connection |
| V _{CC} | 16 | 20 | — | Supply voltage |
| Y0 | 15 | 19 | O | Output 0 (least significant bit) |
| Y1 | 14 | 18 | O | Output 1 |
| Y2 | 13 | 17 | O | Output 2 |
| Y3 | 12 | 15 | O | Output 3 |
| Y4 | 11 | 14 | O | Output 4 |
| Y5 | 10 | 13 | O | Output 5 |
| Y6 | 9 | 12 | O | Output 6 |
| Y7 | 7 | 9 | O | Output 7 (most significant bit) |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|-----|--------|
| V _{CC} | Supply voltage range | −0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | | ±20 mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 mA |
| | Continuous current through V _{CC} or GND | | | ±50 mA |
| T _J | Junction temperature | | | 150 °C |
| T _{stg} | Storage temperature | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings: SN74HC138

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|-----------------|---|-------------------------|------|-----------------|------|
| V _{CC} | Supply voltage | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | V |
| | | V _{CC} = 4.5 V | 3.15 | | |
| | | V _{CC} = 6 V | 4.2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | V |
| | | V _{CC} = 4.5 V | | 1.35 | |
| | | V _{CC} = 6 V | | 1.8 | |
| V _I | Input voltage | 0 | | V _{CC} | V |
| V _O | Output voltage | 0 | | V _{CC} | V |
| Δt/Δv | Input transition rise or fall time | V _{CC} = 2 V | | 1000 | ns |
| | | V _{CC} = 4.5 V | | 500 | |
| | | V _{CC} = 6 V | | 400 | |
| C _{pd} | Power dissipation capacitance (no load) | | 85 | | pF |
| T _A | Operating free-air temperature | SN54HC138 | −55 | 125 | °C |
| | | SN74HC138 | −40 | 85 | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

6.4 Thermal Information: SN74HC138

| THERMAL METRIC ⁽¹⁾ | | SN74HC138 | | | | | UNIT |
|-------------------------------|--|-----------|-----------|----------|---------|------------|------|
| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 87.3 | 104.3 | 54.8 | 91.1 | 141.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 45.8 | 54.7 | 42.1 | 49.5 | 49.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 44.8 | 54.9 | 34.8 | 51.5 | 59.6 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 14.2 | 17.7 | 27 | 17.8 | 6.9 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 44.5 | 54.4 | 34.7 | 51.2 | 59.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: SN54HC138

| THERMAL METRIC ⁽¹⁾ | | SN54HC138 ⁽²⁾ | | | UNIT |
|-------------------------------|--|--------------------------|---------|-----------|------|
| | | J (CDIP) | W (CFP) | FK (LCCC) | |
| | | 16 PINS | 16 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | — | — | — | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 45.4 | 68.1 | 49 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | — | 118.4 | 47.7 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | — | — | 7.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 62.5 | — | — | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 17.7 | 9 | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) R_{θJC} follows MIL-STD-883, and R_{θJB} follows JESD51.

6.6 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-------------------------|-------|-------|------|
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = −20 μA | V _{CC} = 2 V | 1.9 | 1.998 | V |
| | | | V _{CC} = 4.5 V | 4.4 | 4.499 | |
| | | | V _{CC} = 6 V | 5.9 | 5.999 | |
| | | I _{OH} = −4 mA, V _{CC} = 4.5 V | | 3.98 | 4.3 | |
| | | I _{OH} = −5.2 mA, V _{CC} = 6 V | | 5.48 | 5.8 | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | V _{CC} = 2 V | 0.002 | 0.1 | V |
| | | | V _{CC} = 4.5 V | 0.001 | 0.1 | |
| | | | V _{CC} = 6 V | 0.001 | 0.1 | |
| | | I _{OL} = 4 mA, V _{CC} = 4.5 V | | 0.17 | 0.26 | |
| | | I _{OL} = 5.2 mA, V _{CC} = 6 V | | 0.15 | 0.26 | |
| I _I | V _I = V _{CC} or 0, V _{CC} = 6 V | | | ±0.1 | ±100 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V | | | | 8 | μA |
| C _i | V _{CC} = 2 V to 6 V | | | 3 | 10 | pF |

6.7 Electrical Characteristics: SN74HC138

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-------------------------|------|-----|-------|------|
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = −20 μA | V _{CC} = 2 V | 1.9 | | | V |
| | | | V _{CC} = 4.5 V | 4.4 | | | |
| | | | V _{CC} = 6 V | 5.9 | | | |
| | | I _{OH} = −4 mA, V _{CC} = 4.5 V | | 3.84 | | | |
| | | I _{OH} = −5.2 mA, V _{CC} = 6 V | | 5.34 | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | V _{CC} = 2 V | | | 0.1 | V |
| | | | V _{CC} = 4.5 V | | | 0.1 | |
| | | | V _{CC} = 6 V | | | 0.1 | |
| | | I _{OL} = 4 mA, V _{CC} = 4.5 V | | | | 0.33 | |
| | | I _{OL} = 5.2 mA, V _{CC} = 6 V | | | | 0.33 | |
| I _I | V _I = V _{CC} or 0, V _{CC} = 6 V | | | | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V | | | | | 80 | μA |
| C _i | V _{CC} = 2 V to 6 V | | | | | 10 | pF |

6.8 Electrical Characteristics: SN54HC138

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-------------------------|-----|-----|-------|------|
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = −20 μA | V _{CC} = 2 V | 1.9 | | | V |
| | | | V _{CC} = 4.5 V | 4.4 | | | |
| | | | V _{CC} = 6 V | 5.9 | | | |
| | | I _{OH} = −4 mA, V _{CC} = 4.5 V | | 3.7 | | | |
| | | I _{OH} = −5.2 mA, V _{CC} = 6 V | | 5.2 | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | V _{CC} = 2 V | | | 0.1 | V |
| | | | V _{CC} = 4.5 V | | | 0.1 | |
| | | | V _{CC} = 6 V | | | 0.1 | |
| | | I _{OL} = 4 mA, V _{CC} = 4.5 V | | | | 0.4 | |
| | | I _{OL} = 5.2 mA, V _{CC} = 6 V | | | | 0.4 | |
| I _I | V _I = V _{CC} or 0, V _{CC} = 6 V | | | | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0, V _{CC} = 6 V | | | | | 160 | μA |
| C _i | V _{CC} = 2 V to 6 V | | | | | 10 | pF |

6.9 Switching Characteristics

$T_A = 25^\circ C$ and $C_L = 50 \text{ pF}$ (unless otherwise noted; see [Section 7](#))

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------|---|------------------|-----|-----|-----|------|
| t_{pd} | From A, B, or C (input) to any Y (output) | $V_{CC} = 2 V$ | | 67 | 180 | ns |
| | | $V_{CC} = 4.5 V$ | | 18 | 36 | |
| | | $V_{CC} = 6 V$ | | 15 | 31 | |
| | From enable (input) to any Y (output) | $V_{CC} = 2 V$ | | 66 | 155 | |
| | | $V_{CC} = 4.5 V$ | | 18 | 31 | |
| | | $V_{CC} = 6 V$ | | 15 | 26 | |
| t_t | To any output | $V_{CC} = 2 V$ | | 38 | 75 | ns |
| | | $V_{CC} = 4.5 V$ | | 8 | 15 | |
| | | $V_{CC} = 6 V$ | | 6 | 13 | |

6.10 Switching Characteristics: SN74HC138

over recommended operating free-air temperature range and $C_L = 50$ pF (unless otherwise noted; see [Section 7](#))

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|------------------|-----|-----|------|
| t_{pd} | From A, B, or C (input) to any Y (output) | $V_{CC} = 2$ V | | 225 | ns |
| | | $V_{CC} = 4.5$ V | | 45 | |
| | | $V_{CC} = 6$ V | | 38 | |
| | From enable (input) to any Y (output) | $V_{CC} = 2$ V | | 195 | |
| | | $V_{CC} = 4.5$ V | | 39 | |
| | | $V_{CC} = 6$ V | | 33 | |
| t_t | To any output | $V_{CC} = 2$ V | | 95 | ns |
| | | $V_{CC} = 4.5$ V | | 19 | |
| | | $V_{CC} = 6$ V | | 16 | |

6.11 Switching Characteristics: SN54HC138

over recommended operating free-air temperature range and $C_L = 50$ pF (unless otherwise noted; see [Section 7](#))

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|------------------|-----|-----|------|
| t_{pd} | From A, B, or C (input) to any Y (output) | $V_{CC} = 2$ V | | 270 | ns |
| | | $V_{CC} = 4.5$ V | | 54 | |
| | | $V_{CC} = 6$ V | | 46 | |
| | From enable (input) to any Y (output) | $V_{CC} = 2$ V | | 235 | |
| | | $V_{CC} = 4.5$ V | | 47 | |
| | | $V_{CC} = 6$ V | | 40 | |
| t_t | To any output | $V_{CC} = 2$ V | | 110 | ns |
| | | $V_{CC} = 4.5$ V | | 22 | |
| | | $V_{CC} = 6$ V | | 19 | |

6.12 Typical Characteristic

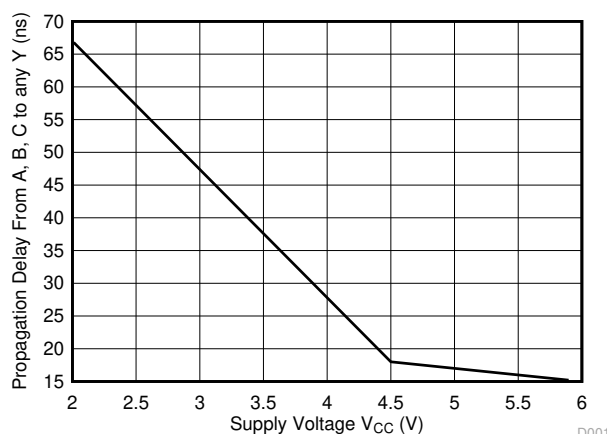
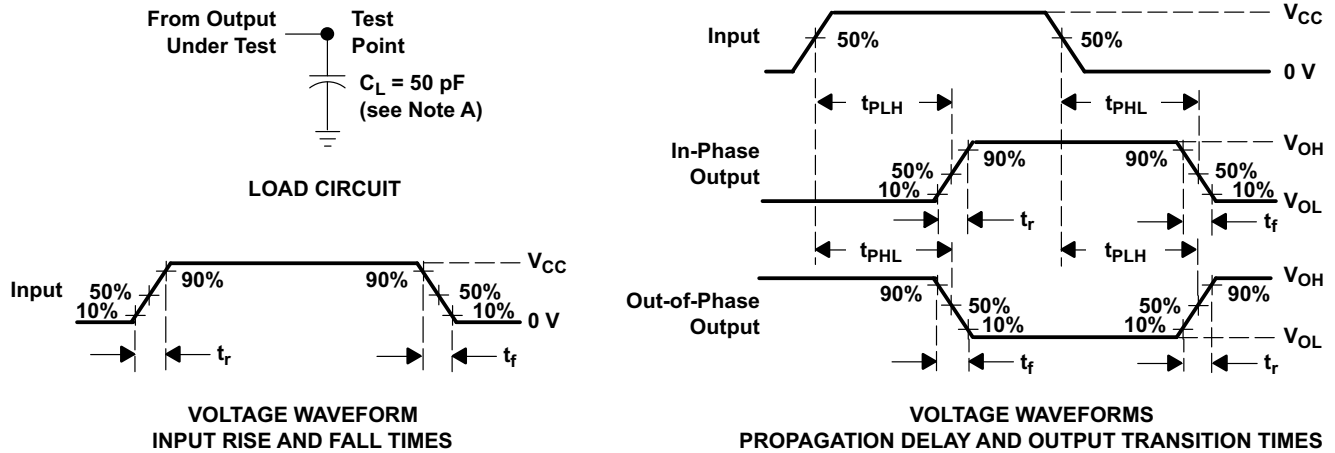


Figure 6-1. Typical Propagation Delay vs Supply Voltage

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

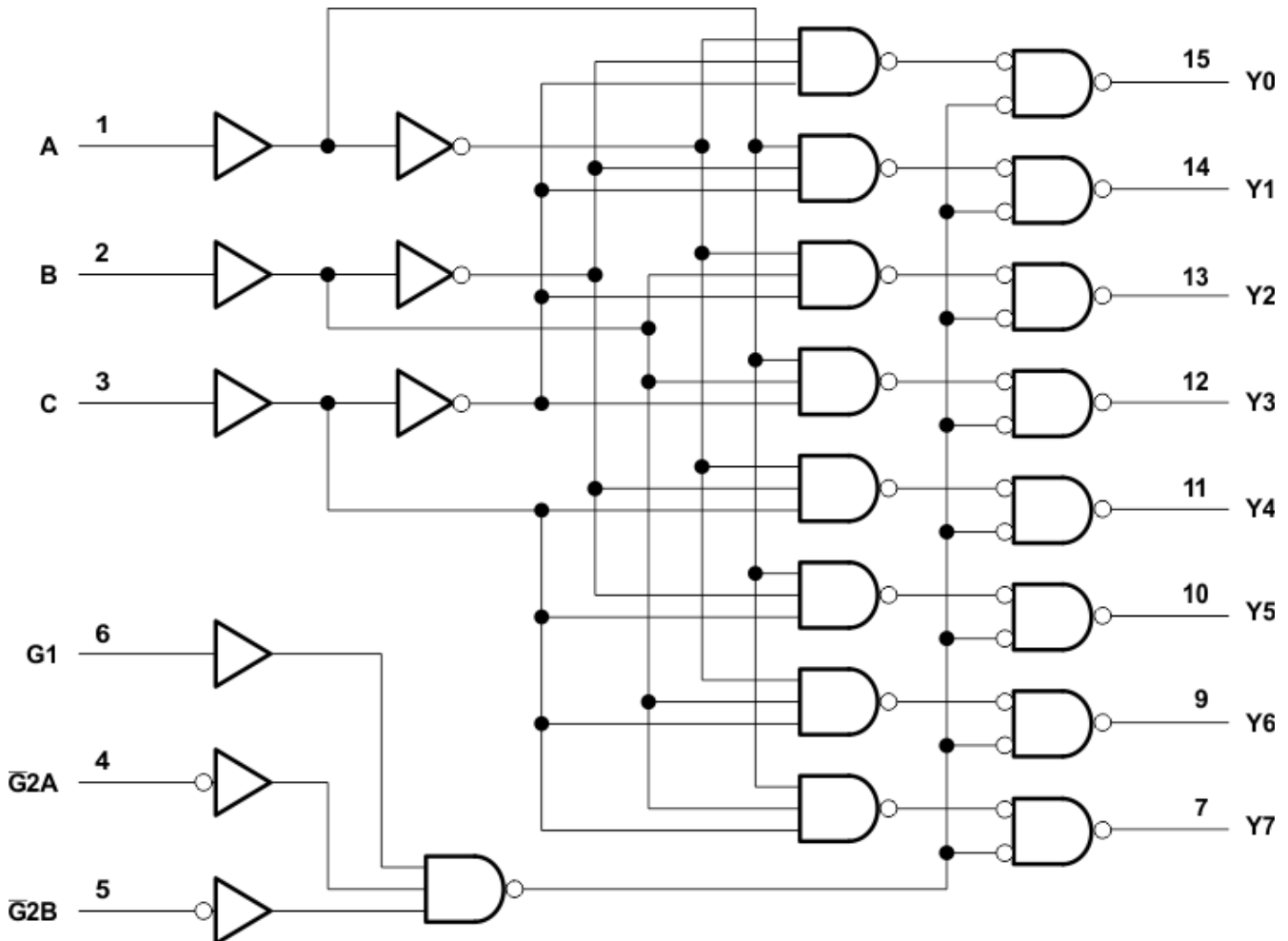
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HC138 devices are 3-to-8 decoders and demultiplexers. The three input pins, A, B, and C, select which output is active. The selected output is pulled LOW, while the remaining outputs are all HIGH. The conditions at the binary-select inputs at the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the requirement for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

8.2 Functional Block Diagram



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Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

8.3 Feature Description

This device features three binary inputs to select a single active-low output. Three enable pins are also available to enable or disable the outputs. One active high enable and two active low enable pins are available, and any enable pin can be deactivated to force all outputs high. All three enable pins must be active for the output to be enabled.

8.4 Device Functional Modes

Table 8-1 lists the functions of the SNx4HC138 devices.

Table 8-1. Function Table

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|--------|------------------|------------------|--------|---|---|---------|----|----|----|----|----|----|----|
| ENABLE | | | SELECT | | | | | | | | | | |
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

9 Application and Implementation

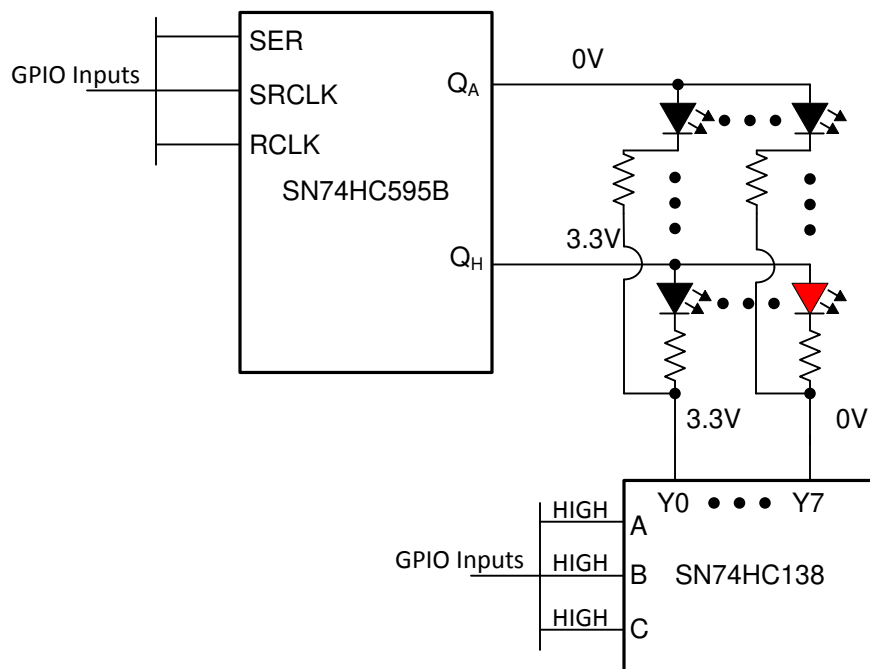
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC138 is useful as a scanning column selector for an LED Matrix display as it can be used for the low side drive of the LED string. The decoder functionality ensures that no more than one output is pulled to a low-level logic voltage so that only a single column is enabled at any point in time.

9.2 Typical Application



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Figure 9-1. LED Matrix Driver Application

9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - For switch time specifications, see propagation delay times in [Section 6.9](#).
 - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in [Section 6.6](#).
- Recommended Output Conditions
 - Outputs must not be pulled above V_{CC} or below GND.

9.2.3 Application Curve

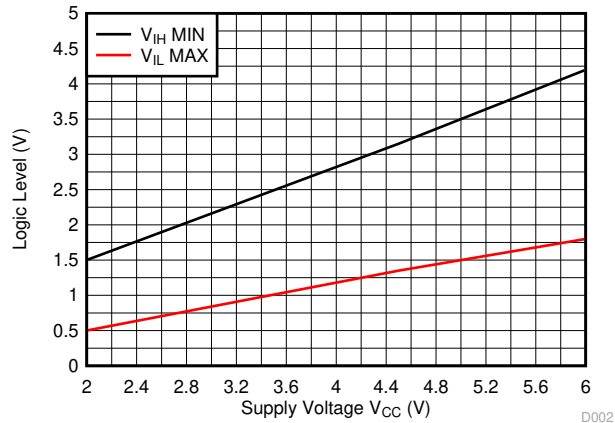


Figure 9-2. Input High and Input Low Thresholds vs Supply Voltage

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 6.3](#).

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F bypass capacitor is recommended to be placed close to the V_{CC} terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. [Figure 11-1](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

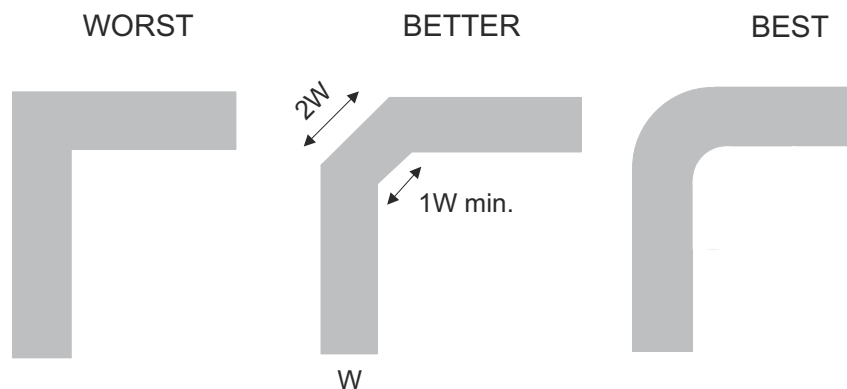


Figure 11-1. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54HC138 | Click here | Click here | Click here | Click here | Click here |
| SN74HC138 | Click here | Click here | Click here | Click here | Click here |

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-8406201VEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8406201VE A SNV54HC138J | Samples |
| 5962-8406201VFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8406201VF A SNV54HC138W | Samples |
| 84062012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 84062012A SNJ54HC 138FK | Samples |
| 8406201EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8406201EA SNJ54HC138J | Samples |
| 8406201FA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8406201FA SNJ54HC138W | Samples |
| JM38510/65802B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65802B2A | Samples |
| JM38510/65802BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65802BEA | Samples |
| M38510/65802B2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65802B2A | Samples |
| M38510/65802BEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65802BEA | Samples |
| SN54HC138J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC138J | Samples |
| SN74HC138D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DE4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DG4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DRE4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------------|-------------------------|
| SN74HC138DRG4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138DT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU SN | N / A for Pkg Type | -40 to 85 | SN74HC138N | Samples |
| SN74HC138NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC138N | Samples |
| SN74HC138NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138PW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SN74HC138PWT | ACTIVE | TSSOP | PW | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC138 | Samples |
| SNJ54HC138FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 84062012A SNJ54HC 138FK | Samples |
| SNJ54HC138J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8406201EA SNJ54HC138J | Samples |
| SNJ54HC138W | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8406201FA SNJ54HC138W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC138, SN54HC138-SP, SN74HC138 :

- Catalog : [SN74HC138](#), [SN54HC138](#)
- Automotive : [SN74HC138-Q1](#), [SN74HC138-Q1](#)
- Military : [SN54HC138](#)
- Space : [SN54HC138-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC138DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC138DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC138NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HC138NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.85 | 5.45 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC138PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC138PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

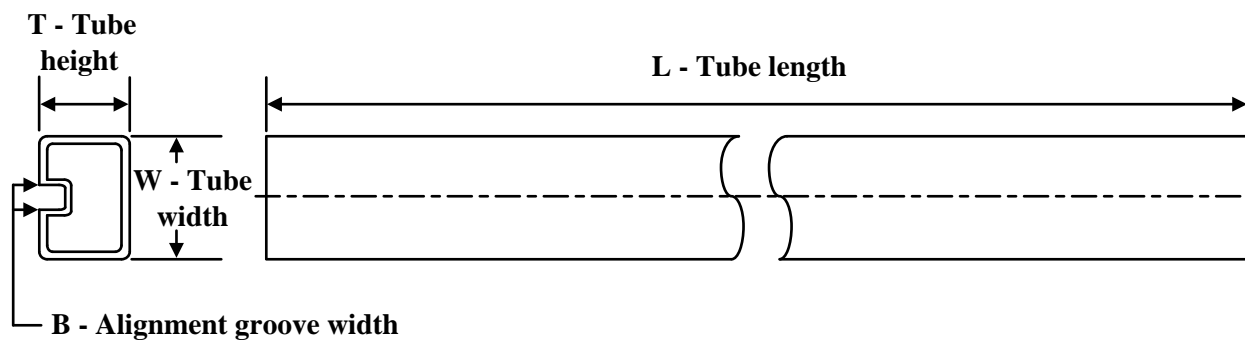
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC138DBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC138DR | SOIC | D | 16 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HC138DRG4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC138NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74HC138PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138PWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC138PWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8406201VFA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| 84062012A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 8406201FA | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |
| JM38510/65802B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| M38510/65802B2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SN74HC138D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC138DE4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC138DG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74HC138N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC138N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC138N | N | PDIP | 16 | 25 | 506.1 | 9 | 600 | 5.4 |
| SN74HC138NE4 | N | PDIP | 16 | 25 | 506.1 | 9 | 600 | 5.4 |
| SN74HC138NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC138NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC138PW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54HC138FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC138W | W | CFP | 16 | 1 | 506.98 | 26.16 | 6220 | NA |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

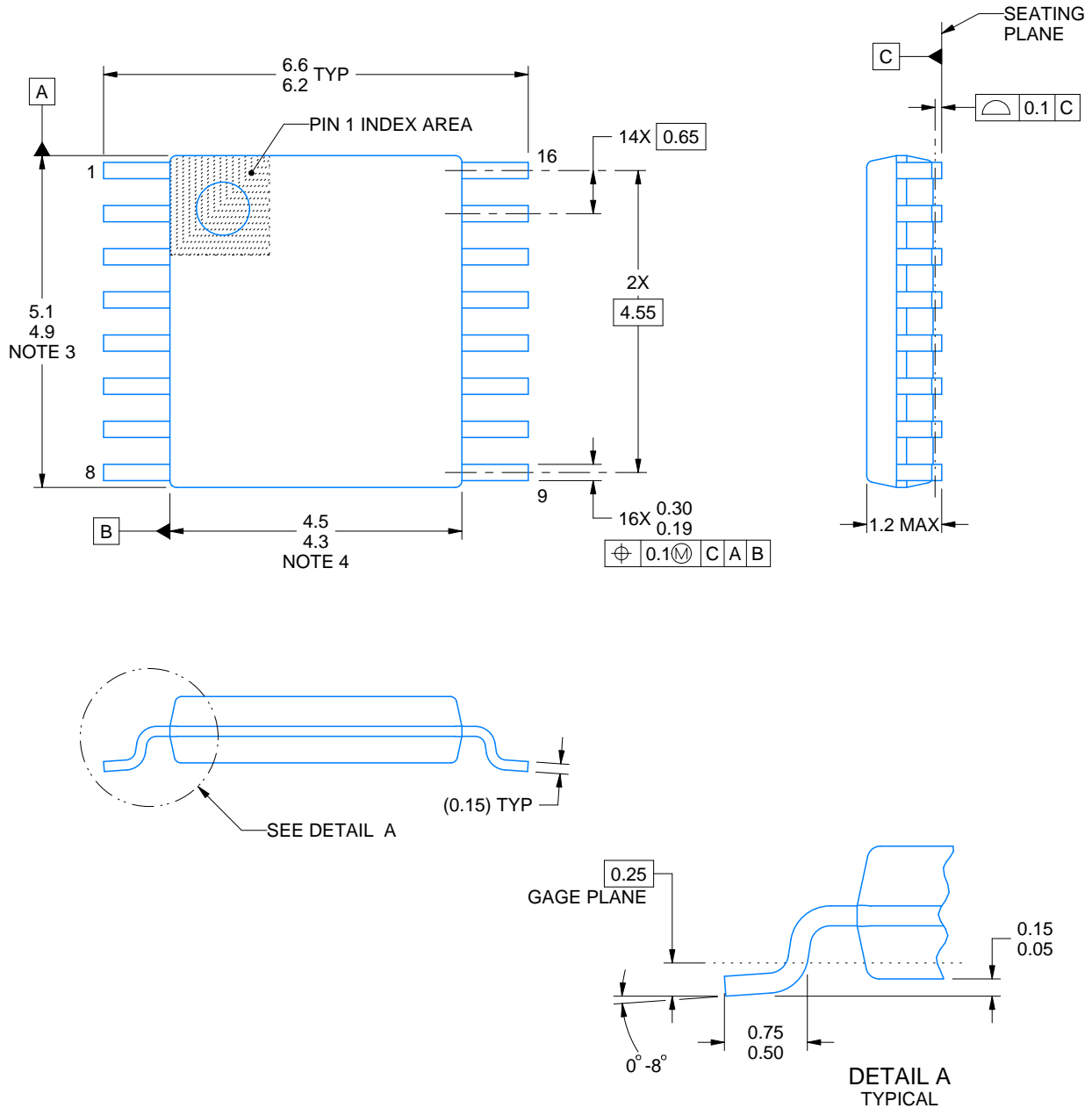
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

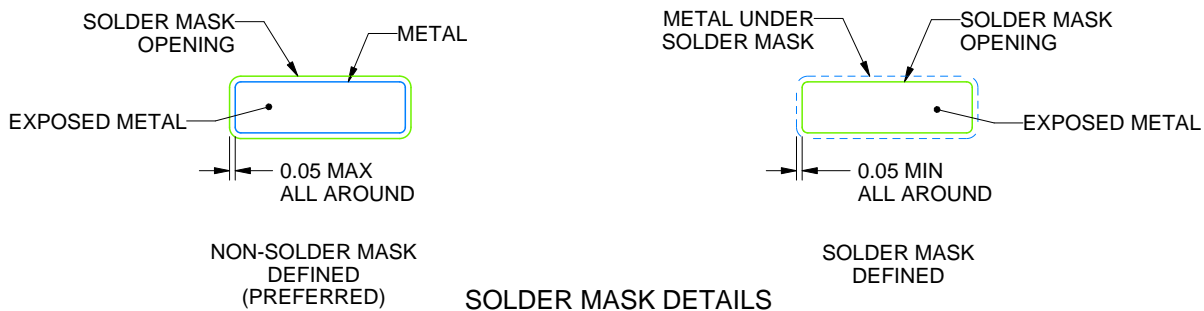
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

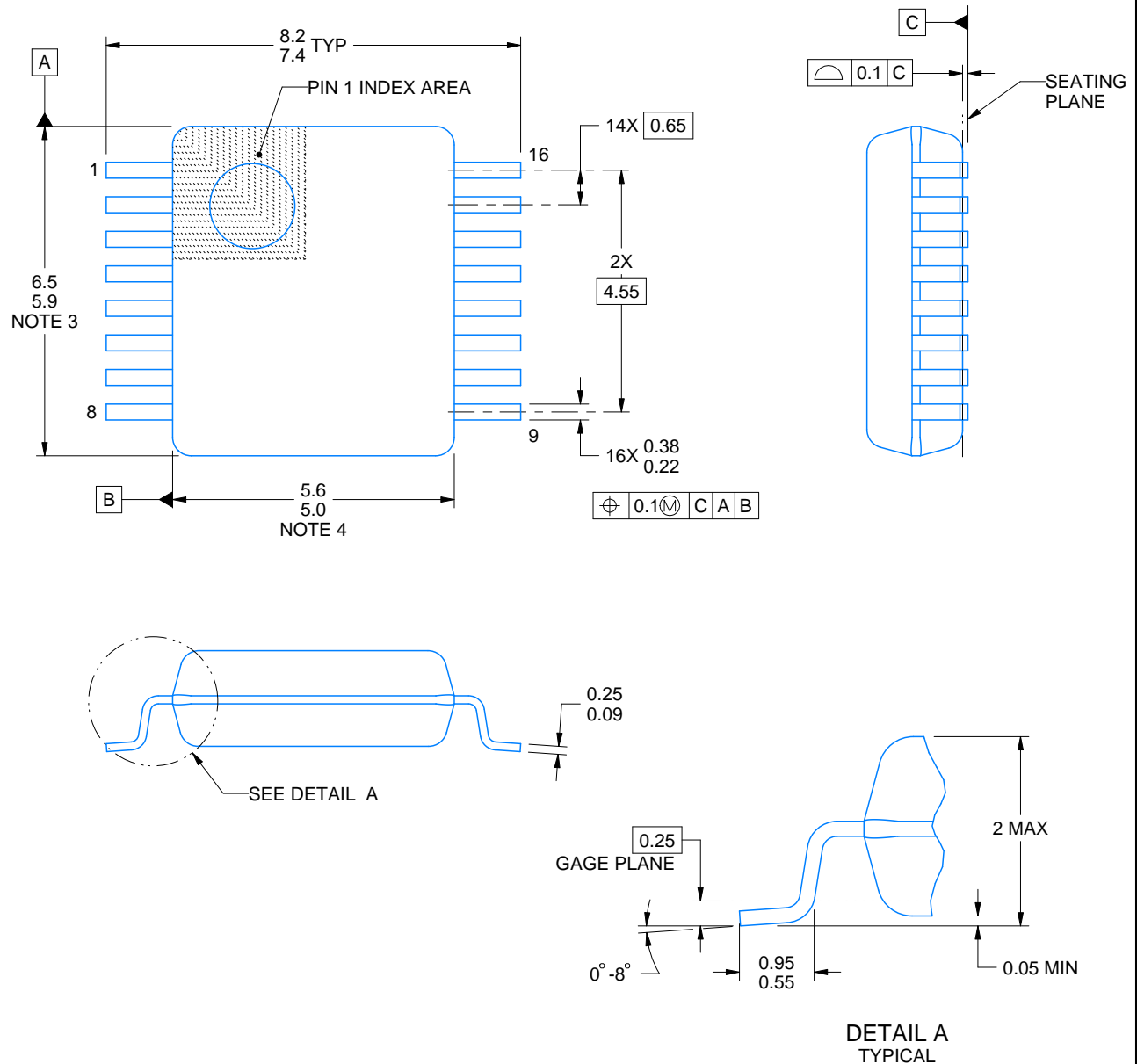


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

NOTES:

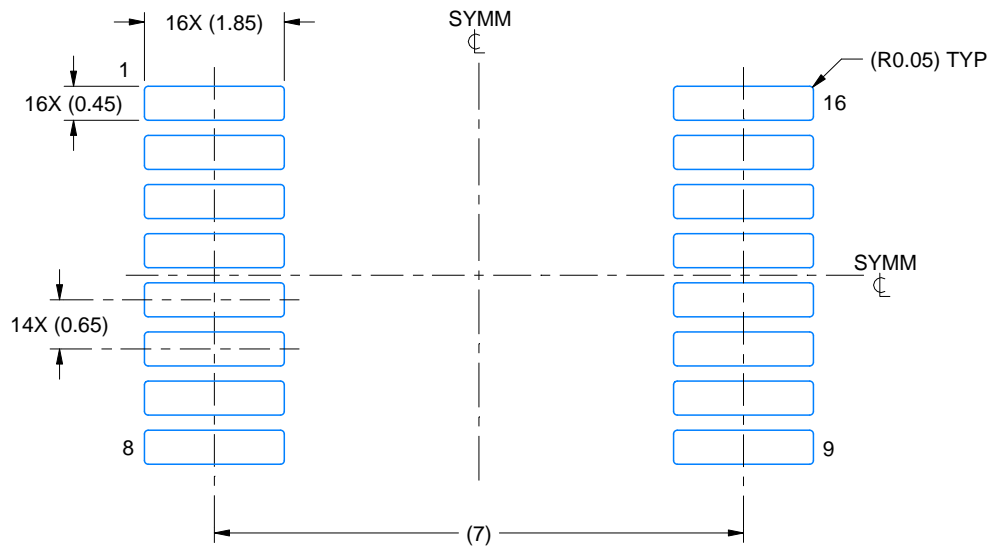
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

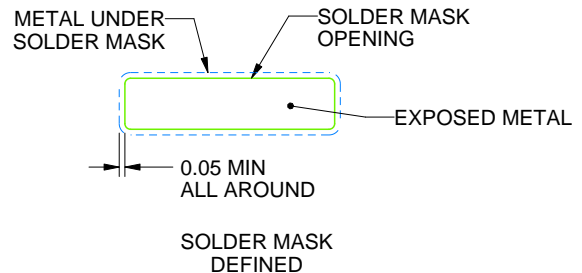
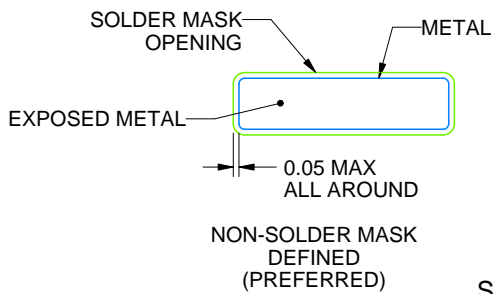
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

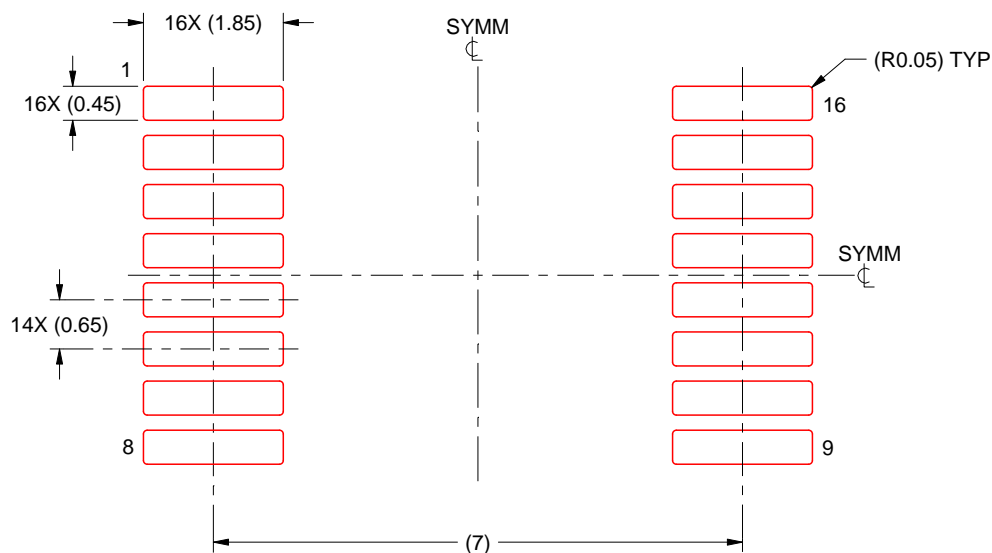
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

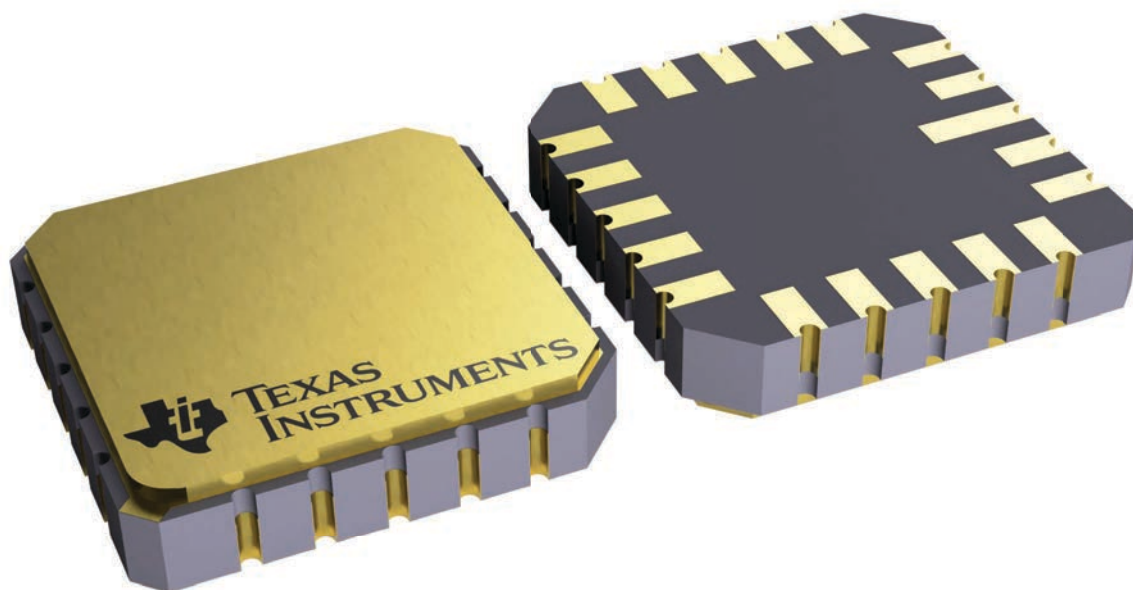
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

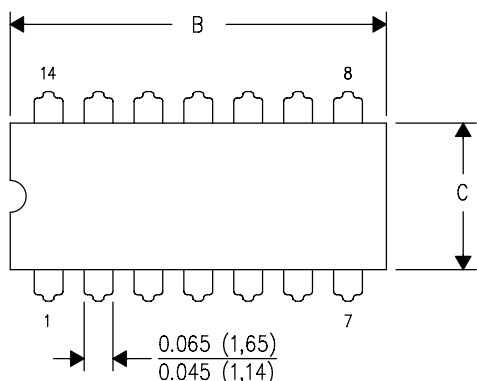


4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN



PLASTIC DUAL-IN-LINE PACKAGE

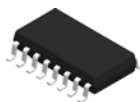


| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

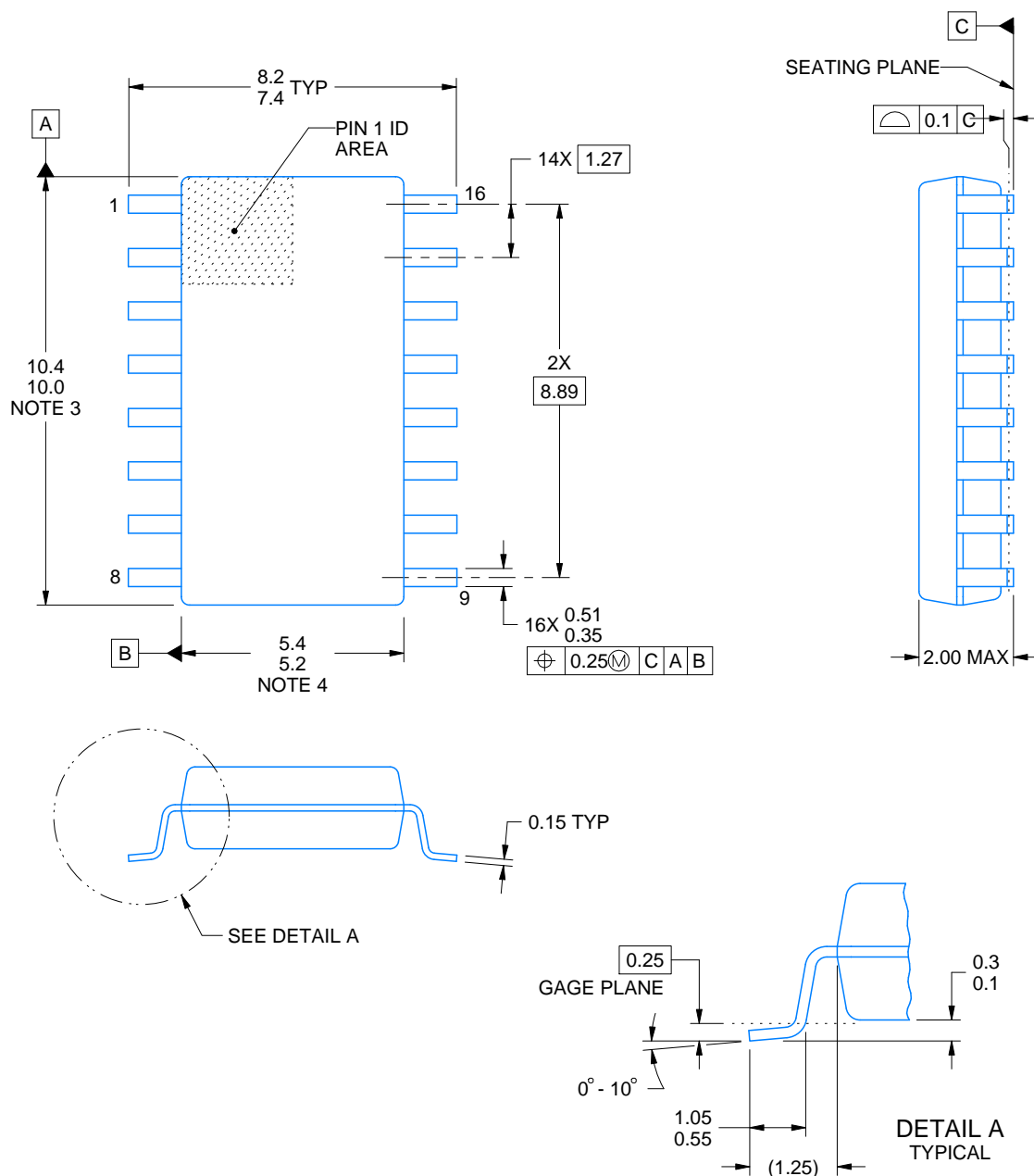


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

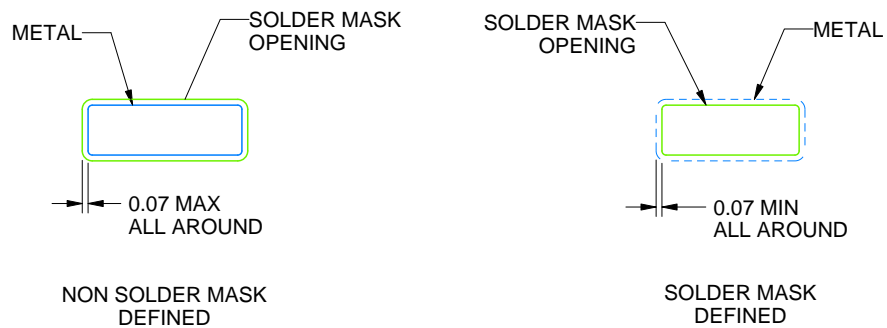
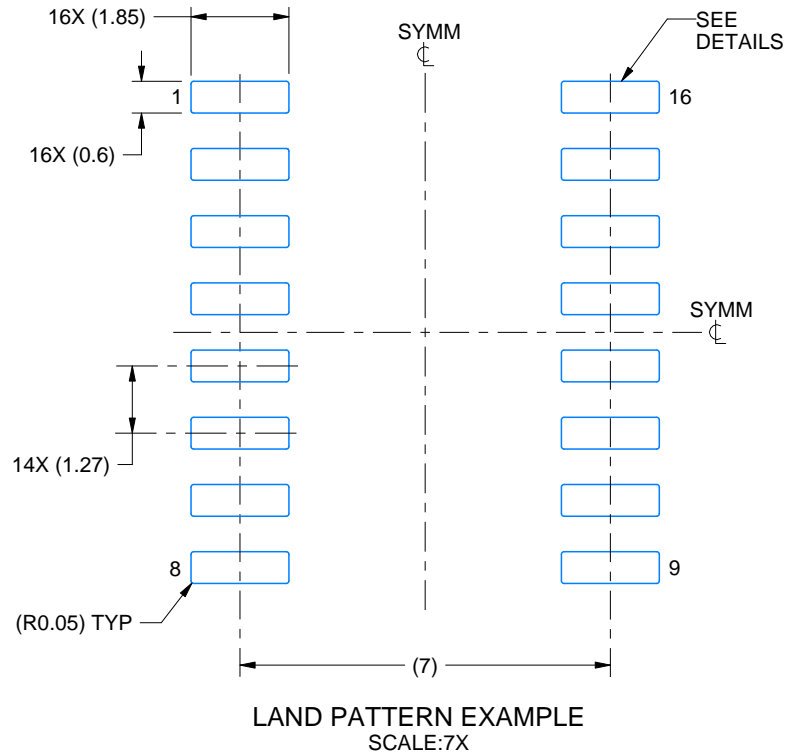
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

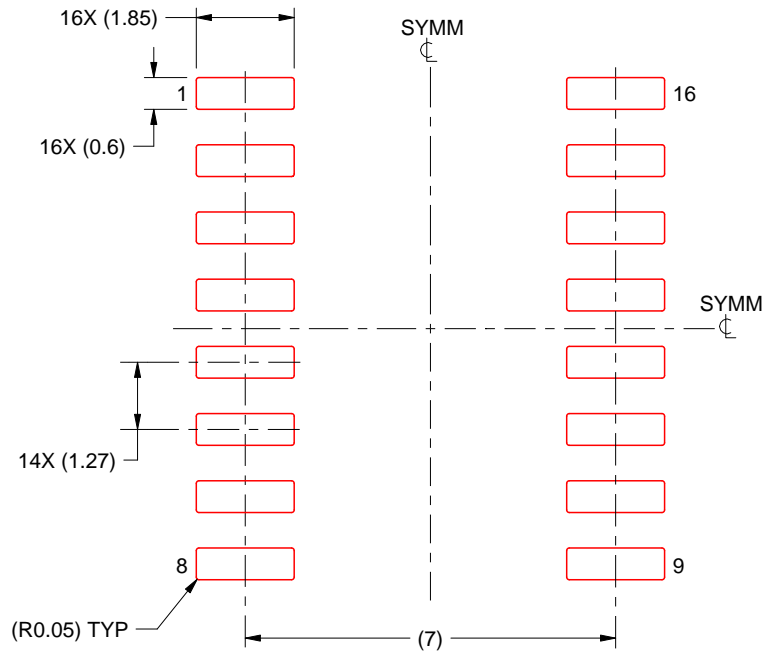
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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