

**Requirements Document**

**EPRD**

()

**SanDisk Corporation**

**Systems Engineering Department**

**C O N F I D E N T I A L**

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| --- | --- | --- | --- |
| Revision History | | | |
| **Revision** | **Author** | **Revision description** | **Date** |
| 0.1 | Nadav Grosz | Initial draft | 3/23/2010 |
| 0.2 | Nadav Grosz | Added iNAND Extreme, Updated specs revisions, Updated performance, Added WP & Vdet requirement, Updated AFM, Updated operating power, Updated schedules. | 5/26/2010 |
| 0.3 | Nadav Grosz | Removed iNAND Ultra support | 6/17/2010 |
| 0.4 | Nadav Grosz | Added back iNAND Ultra support | 6/21/2010 |
| 0.5 | Nadav Grosz | Updated crypto performance. Updated non captive NAND. Removed MS support | 7/20/2010 |
| 0.6 | Nadav Grosz | Removed support for non-captive NAND. Removed test pads. Updated iNAND+ performance. | 7/29/2010 |

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| --- | --- | --- | --- |
| Reference Documents | | | |
| **Name** | **Author** | **Revision** | **Date** |
| SDMMC PL Performance and Speed Class measurements | David K. | <http://sprocketil.sandisk.com/Tefen/PLM/SD_PL/Document%20Library/SD%20MMC%20Product%20Line%20Performance%20and%20Speed%20Class%20measurements%20Requirements.doc> |  |
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# Executive Summary

The following EPRD sets the requirements for the ComboS6HMp6 (TSMC65nm). ComboS6HMp6 is designed to support the next generation of SanDisk secure products using next generation memory technology of 32nm and 2Xnm, 1Xnm memory.

ComboS6HMp6 is designed to support following Products:

1. SDC
2. JIL
3. Enterprise
4. SD Retail
5. Imaging & Gaming
6. slotRadio
7. slotVideo SD
8. iNAND & iNAND Ultra

In addition, ComboS6HMp6 provides a cryptographic module for TrustedFlash security applications and dedicated RAM for application.

ComboS6HMp6 die cost target is $0.38

ComboS6HMp6 ASIC and FW architectures will be optimized to support SanDisk’s memory of 32nm and 2Xnm, 1Xnm.

Major features:

* Support SD 3.0 Specification (including UHS-50/104)
* Support eMMC 4.41 Specification
* Blue label, Ultra, Extreme and UHS performance
* Standard x16 and x8 NAND Flash interface
* Toggle mode HV (3.3V) support (133MB/Sec)Support for captive 2Xnm, 1Xnm X2; 32nm X2, X3 NAND Flash memory
* Maximum ECC capability: 122-bit/2K for 32nm X3, 32nm eX3, and 52-bit ECC for 32nm X2
* AFM support (Adaptive Flash Management)
* Security core engine

Target tape-out date: Jan. 15th, 2011

Tentative Product ACT date: Jun. 30th, 2011

(Final ACT date will be determined by the core team)

# Strategy

|  |  |
| --- | --- |
| Goals | 1. Develop controller to support 2Xnm, 1Xnm and 32nm memory 2. Develop controller to support next generation of secure products |
| Objectives | 1. Support new memory technology 2Xnm, 1Xnm and 32nm with secure products 2. Support markets mainstream for 2010/2011 with the product families listed below. |
| Markets Addressed | 1. MicroSD, SD/SDHC/SDXC/eMMC |
| Development Strategy | 1. Controller ASIC architecture, firmware architecture to be developed by Corporate/Central Engineering. 2. In general provide appropriate hooks in the controller to realize cost savings at product level. |
| Product Families | 1. Secure products – SDC, JIL, SlotRadio, slotVideo SD etc… 2. Blue Line retail and generic OEM cards 3. Ultra Line retail and generic OEM cards 4. Extreme Line retail 5. Extreme Pro Line retail 6. SD UHS-50 based Line retail generic OEM cards 7. SD UHS-104 based Line retail generic OEM cards 8. iNAND eMMC boot & storage OEM Embedded 9. iNAND Ultra |
| High Level Milestones | |  |  | | --- | --- | | Milestone | Date | | Tape-Out | Jan. 15th,2011 | | Final ROM Release | Jan. 15th,2011 | | ASIC blind build | TBD | | Tested Engineering samples | TBD | | FW for DLT | TBD | | GM Flashware | TBD | | ACT | Jun. 30th, 2011 | |

The presented dates are only recommendation and not committed

# Technology Profile

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Interfaces** | Host I/F | 1. SD 3.0 Specification 2. eMMC 4.41 Specification 3. Plan for eMMC 4.5 – TBD 4. Plan for SD 4.0 – TBD | | | | | * UHS-II is not required |
| Flash I/F | 1. x8 support 2. x16 support 3. Toggle mode HV (3.3V) support (133MB/Sec) | | | | |  |
| SD  Bus Speed | 1. SD Normal Speed 2. SD High Speed 3. UHS50 (1.8V signaling) 4. SDR12 5. SDR25 6. SDR50 7. DDR50 8. UHS104 (1.8V signaling) 9. SDR12 10. SDR25 11. SDR50 12. SDR104 13. DDR50 | | 0-25Mhz  0-50Mhz  0-25Mhz  0-50Mhz  0-100Mhz  0-50Mhz  0-25Mhz  0-50Mhz  0-100Mhz  0-208Mhz  0-50Mhz | | |  |
| eMMC  Bus Speed | 1. MMC Normal Speed 2. MMC High Speed 3. MMC DDR52 | | 0-20Mhz; 0-26Mhz  0-52Mhz  0-52Mhz | | |  |
| **Memory** | Supported Capacities | 1. SD 2. uSD 3. eMMC | | 1GB – 256GB  1GB – 64GB  1GB – 128GB | | |  |
| Flash Configuration | 1. Maximum of 16 flash dies 2. Die interleave as needed with power consumption limitation 3. Plane interleave as needed 4. Support 4 FCE pins (2 dedicated pads + 2 additional FCE either dedicated pads if core limited or multiplexed on upper flash data bus if pad limited) | | | | | 1. 16 flash dies support to be evaluated by packaging group for SD only 2. 16 dies might require a bus switch for performance |
| ECC Tabs | * 52bit/2K BCH ECC error correction * 77bit/2K BCH ECC error correction * 104bit/2K BCH ECC error correction * 122bit/2K BCH ECC error correction | | | | |  |
| **Memory** | Supported Memory | 1. SNDK 2Xnm 2. SNDK 1Xnm 3. SNDK 32nm | | 32Gb X1 (ABL)  64Gb X2 (HBL)  64Gb X2 (ABL)  32Gb X2 (ABL)  64Gb eX3  32Gb eX3    32Gb X1 (ABL)  64Gb X2 (ABL)  16Gb X2 (HBL)  128Gb eX3  64Gb eX3  32Gb eX3  16Gb X1  32Gb X2  16Gb X2  8Gb X2  64Gb eX3  32Gb eX3  16Gb eX3 | | |  |
| **Performance Targets** | SD Performance Targets | 1. SD/uSD BL 2. SD/uSD Ultra (HS) 3. SD Extreme (HS) 4. SD Extreme (UHS-50) 5. SD Extreme Pro (UHS-50) 6. SD UHS-104 based | | 3/5 MB/Sec  7/15 MB/Sec  20/20 MB/Sec  30/30 MB/Sec  45/45 MB/Sec  100/100 MB/Sec  (Min. 70/70 MB/Sec) | | | 1. ASIC to support 104MB/sec throughput 2. All SD product must support UHS-50 regardless of performance grades |
| SD Security  Performance  Targets | 1. Non side load mode 2. Side load mode   Supported modes:   1. Din🡪AES🡪AES🡪Dout 2. Din🡪AES + Hash 3. Din🡪AES 4. Din🡪AES🡪Hash🡪AES🡪Dout 5. Din🡪AES🡪Hash🡪Dout 6. Din🡪AES🡪Hash | | 30/30 MB/Sec  50/50 MB/Sec | | | 1. For Side load mode, active power may reach up to 400mA |
| SD Speed Class | 1. SD/uSD Blue 2. SD/uSD Ultra 3. SD Extreme 4. SD Extreme Pro 5. SD UHS-104 based | | Class 4  Class 6  Class 10  Class 10 + 3V-AV  Class 10 + 3V-AV | | | 1. SD Speed class applies only to 4GB and above. 2. 3V-AV = UHS speed grade > 10MB/Sec |
| eMMC Sequential Performance Targets | 1. eMMC   (0-26Mhz, power class0)   1. eMMC high speed mode (52Mhz, power class0) 2. eMMC “side load” mode (52MHz; not exceeding power class 4) 3. iNAND Ultra for enhanced area (52Mhz - 8bit - DDR mode) 4. iNAND Ultra for user area (52Mhz - 8bit - DDR mode) | | | | 9/15 MB/Sec  9/30 MB/Sec  20/40 MB/Sec  40/60 MB/Sec  30/50 MB/Sec | 1. iNAND Ultra will only use eX3 memory |
| eMMC Random Performance Targets | 1. W/R for X2 memory 2. W/R for eX3 memory 3. MLC Area 4. Enhanced Area 5. iNAND Ultra for enhanced area (52Mhz - 8bit - DDR mode) 6. iNAND Ultra for user area (52Mhz - 8bit - DDR mode) | | | | 150/1000  50/1000  150/1000  1000/4000 (512B)  500/3000 (4KB)  250/1500  (8KB)  1000/4000 (512B)  500/3000 (4KB)  250/1500  (8KB) | 1. All numbers are access per second 2. For iNAND, SD Class 4 equiv. for user area is required 3. For iNAND Ultra, SD Class 6 equiv. for user area is required 4. Please refer to 6.6 for detailed performance tests |
| eMMC  Class | 1. MMC Class B for X2 based 2. MMC Class B for eX3 based 3. MMC Class 0 for DDR mode | | | | | 1. eMMC Classes are according to TestMetrix 3.1i (Patch 5c) |
| **Power Consumption** | Operating Power  (card level) | 1. SD Normal Speed/High Speed 2. SD UHS-50 3. SDR12 4. SDR25 5. SDR50 6. DDR50 7. SD UHS-104 8. SDR12 9. SDR25 10. SDR50 11. SDR104 12. DDR50 13. eMMC (not side loading) 14. eMMC (side loading) | | | | 100mA/200mA  100mA  200mA  400mA  400mA  100mA  200mA  400mA  400mA  400mA  Class 0  Up to Class4 (as low as possible) | 1. Measurement method: SD&eMMC - max average over 16 mS window 2. For 8 flash dies, uSD/SD/iNAND card level room temp (across voltage and process range) max: 350uA |
| **Power Consumption** | Operating Power  (controller) | 1. Controller power to be defined to meet the product level power requirements based on the controller and flash activities within the 16ms measured window | | | | |  |
| Standby Power  (controller) | 1. SD/iNAND (typ)      1. SD/iNAND (across PVT) | | | Room temp (across voltage and process range) max: 110uA  750uA – desired | | 1. SD controller standby to be finalized based on ASIC yield results |
| **Packaging** | Packaging | 1. SIP for uSD 2. SD SIP 3. 48 BGA production package (for SD SMT) 4. iNAND JEDEC BGA packages 5. 256BGA (engineering package) | | | | | 1. 256BGA must be compatible with previous controllers |
| **Operating & Storage** | Operating Conditions | 1. SD/eMMC 2. SD HV 3. eMMC Dual voltage | -25C to 90C  2.7V to 3.6V  2.7V to 3.6V,  1.7V to 1.95V | | | | 1. eMMC voltage of 1.2V not supported |
| Storage Conditions | 1. eMMC | -40°C to 90°C | | | |  |
| **Specifications** | Security Requirements | 1. For detail Security requirement please refer to section 6.5 | | | | |  |
| SD Specific Requirements | 1. SDA Spec 3.0 Specification | | | | |  |
| eMMC Specific Requirements | 1. eMMC 4.41 | | | | |  |
| AFM Specific Requirements | 1. According to eMMC4.41 2. According to SanDisk’s AFM proposal | | | | |  |
| **Misc.** | Analog Requirements | 1. On-chip capless regulators designed to eliminate the need for an external regulator capacitors 2. Write protect and Voltage detector support for Power loss/Partial Page Programming (PPP) are required | | | | | 1. Please evaluate the impact on the active power consumption |
| Peripherals/ GPIO | 1. UART Tx (Rx not mandatory) 2. JTAG | | | | |  |
| Design for Manufacture | 1. No support for test pads | | | | |  |
| Cost Reduction | 1. Compliant with memory test during card test (MTCT) over FBCC standard 2. Reducing product level transformational cost | | | | | Incorporate all the cost reduction techniques employed on existing platforms |
| **Reliability** | Reliability | 1. SD host pins 4kV HBM JEDEC 22a114d 2. SD host pins 200V MM JEDEC 22a115a 3. SD host pins 500V CDM in the final product form factor per JEDEC spec 22c101c 4. Embedded product pins 2kV HBM per JEDEC spec 22a114d 5. Embedded product pins 500V CDM per JEDEC spec 22c101c on either embedded product or engineering test package. Not test pads. 6. All non-host pins that will be wire bonded in any product configuration 1kV HEDEC HBM 7. All pads 200V CDM on the die that are probed or bonded during production test or manufacturing in the engineering test package. | | | | |  |
| **Product Priority** | SD Product Priority | 1. UHS-104 based products | | | | |  |
| eMMC Product Priority | TBD | | | | |  |

# Resources and Expenses

## Resources

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Resources** | | | | **Q1'10** | | | **Q2'10** | | | **Q3'10** | | | **Q4'10** | | | **Q1'11** | | |
| **Rep** | **Group** | **Resource description** | **Man month** | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 |
|  | **ASIC** | ASIC Development |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **BE** | ROM Development |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **BE** | BE FW integration |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **BE** | BE Memory Systems |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **PLM** | Dev, Test, Mng, Int |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **FW** | FE ROM & FW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **HW** | Hardware |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **QA** | Quality and reliability |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **PROD** | Production and testing |  |  |  |  |  |  |  |  |  |  |  | **.2** | **.2** | **.5** | **.5** | **.5** |
|  | **APPS** | Apps and compatibility |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | **PKG** | Package and SMT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **Total Man Months** | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

## Expenses

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **#** | **Dep.** | **Item** | **Cost (in $)** | **Resource** |
|  | Quality & Rel | MUB, qty 5 | 5 x $300 each |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  | Total Cost: | |  |  |

# Risks

|  |  |  |  |
| --- | --- | --- | --- |
| **Risk** | **Details** | **Level** | **Action/Owner** |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

# Appendix

## Memory Footprint Estimates

|  |  |
| --- | --- |
| **Controller Memory Type** | **Size (KB)** |
| ROM |  |
| ARC/RISCs Code (MRAM) |  |
| SBRAM |  |
| ARC Cache |  |
| Host I/F |  |

## Roles and Responsibility (SD)

|  |  |  |  |
| --- | --- | --- | --- |
| **Deliverable/Function** | **Group** | **Division Head** | **Lead** |
| EPRD Sign-off | SD PLM | Yosi Zatelman | David Zehavi |
| Platform architecture | SD PLM | Yosi Zatelman | Orna P. |
| Overall Project Management | SD PLM | Yosi Zatelman | David Zehavi |
| ASIC Design | ASIC | Stan C. |  |
| ASIC Verification | ASIC | Stan C. |  |
| ASIC Integration | ASIC | Stan C. |  |
| ASIC Project Management | ASIC | Stan C. |  |
| FPGA Image development | ASIC | Stan C. |  |
| Product PCB development | SD PLM | Yosi Zatelman | Meiri A. |
| BE Memory System Design | BE Systems | Jian C |  |
| BE FW ROM | BE FW | Carlos G. | Matt F. |
| SD FE ROM | SD PLM | Yosi Zatelman | Shmuel C. |
| BE Flashware | BE FW | Carlos G. | Matt F. |
| FE Flashware | SD PLM | Yosi Zatelman | Shmuel C. |
| Controller Product Test and Controller Product Engineering | ASIC | Alex Shevachman |  |
| Controller Quality and Reliability | ASIC | Alex Shevachman |  |
| Controller Characterization | ASIC | Alex Shevachman |  |
| Card Product Engineering | CPE | Larry Roland |  |
| Product Engineering | SD PLM | Yosi Zatelman | Reuven E. |
| Product Qual & Reliability | RELIABILITY | Arun Malhotra |  |

## Performance & Configurations Table

For updated performance & configurations table please see:

<http://sprocketil.sandisk.com/Tefen/PLM/SD_PL/Lists/BE%20Configurations/SD%20Road%20Map%20For%20BE%20Sys.aspx>

## Security Requirements



## MMC Random Performance

* 52Mhz, 8-bit interface
* Write: 50 accesses per second. Should be verified on 512B/1K/2K/4K chunk sizes.
* Read: 1000 accesses per second. Should be verified on 512B/1K/2K/4K chunk sizes.
* Random sector address. Address can be unaligned to chunk size.
* Over 100MB
* Nokia use case: repeat the test 10K times, one chunk size per test (chunk sizes not interleaved):

Numebr of accesses = 10000

Chunk\_size = 512Bytes

While (chunk\_size <= 4Kbytes)

{

            For (i=0;i< Numebr of accesses;i++)

{

            Sector Address = (Random(seed)) % (device total capacity in sectors)

            //Start measure time

            Write(Sector address, chunk size) OR Read(Sector address, chunk size)

            //stop measure time

            i++

}

Calculate Min, Max and average time for the current chunk\_size.

Calculate Min, Max, average IOS per second (based on total data that was read / written (chunk\_size \*  number of accesses) and performance measured)

Chunk\_size = chunk\_size\*2

}