

# 4

## Ripple-Based Control Technique Part I

Control methods for DC/DC converters can be simply classified into three types: current-mode control, voltage-mode control, and ripple-based control. The transient response of current-mode or voltage-mode control is constrained by the bandwidth, which is mainly determined by the operating mode (continuous conduction mode (CCM) or discontinuous conduction mode (DCM)) and its compensation technique. Generally speaking, the compensation technique determines both converter stability and regulation performance. By contrast, ripple-based control has the advantage of fast transient response while maintaining system stability without any complicated compensation network. Another advantage of ripple-based control is low quiescence because of its simple structure, which can extend the battery usage time in portable electronics.

In recent years, portable electronics powered by batteries have needed their heavy and light load efficiencies extended to increase the battery usage time, which is a major concern in the design of wearable electronics. Ripple-based control can be used for such applications because of its fast transient response and high efficiency to meet the specifications of high slew rate and extensive load current ranges, respectively. For example, on-time control, which is one of the ripple-based control techniques, features fast transient response and high efficiency in case of loading current variations. As the term “constant on-time” implies, the constant value is composed of the product of the on-time period and the input voltage to obtain the feedforward function. By contrast, the off-time period can be automatically extended for high efficiency when the loading current decreases continuously at light loads. In a steady state, the off-time period is kept approximately constant. Thus, the converter behaves as a pseudo-constant frequency operation. In case of any loading current variation, the off-time period inversely varies with the load current to achieve a fast transient response. Constant on-time control has become a well-known control technique because of its advantages of feedforward function, fast transient response, and high efficiency at light loads to meet the demand of high-quality portable electronics.

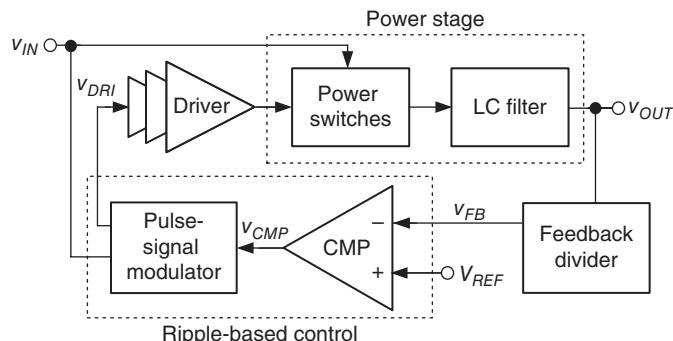
In subsequent sections, a review of basic ripple-based control topologies reveals the characteristics of each technique, including their advantages and disadvantages. The preliminary design presents the operation principle and stability analysis. In turn, several techniques are introduced to improve the regulation performance, including electromagnetic interference reduction, output voltage ripple reduction, and line/load regulation improvement. Finally, the bootstrap architecture, which is more adequate for high input voltage, is presented for high-power applications.

## 4.1 Basic Topology of Ripple-Based Control

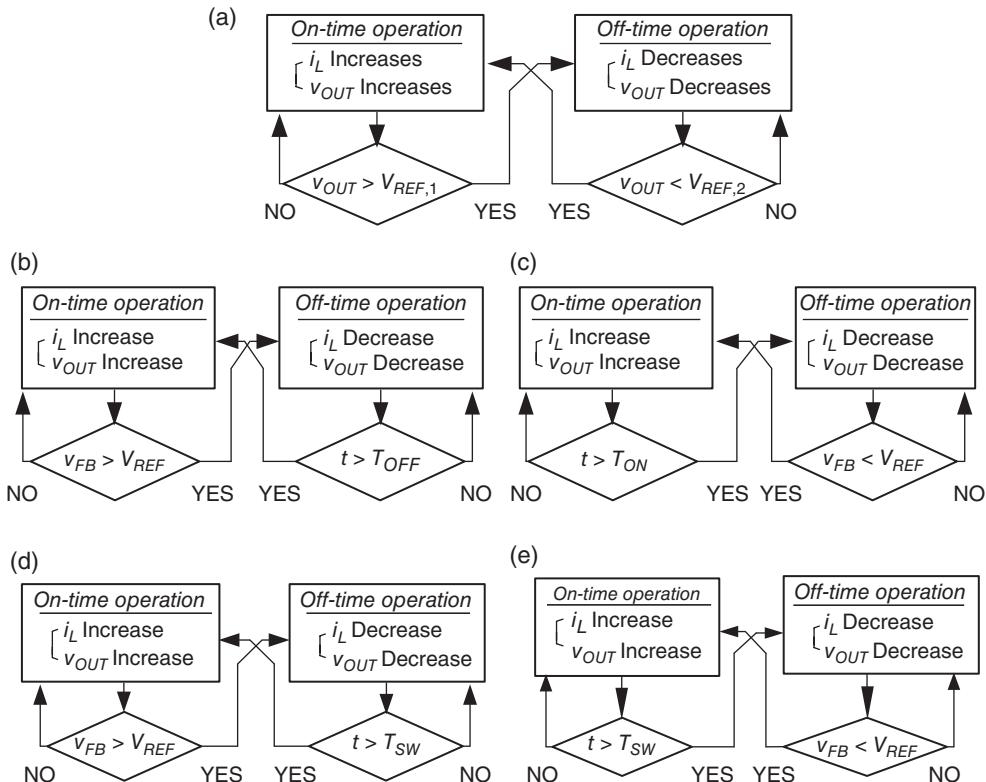
Ripple-based control commonly refers to DC/DC converters that use output voltage ripple information to compare with the reference voltage and control power switches on/off to determine adequate power delivery paths. Figure 4.1 shows a generic block diagram of a DC/DC buck converter with ripple-based control technique. A power stage with power switches and inductance–capacitance (LC) filter stores and releases energy. Thus, the power stage converts a high input voltage ( $V_{IN}$ ) to a low output voltage ( $V_{OUT}$ ). The output voltage is fed directly or through a feedback divider to the ripple-based controller, where the feedback signal is denoted as  $V_{FB}$ . The ripple-based controller basically includes a pulse signal modulator and a comparator (CMP). It can be used to determine the output  $V_{CMP}$  of the CMP by comparing  $V_{FB}$  with  $V_{REF}$ . Determining the output through the pulse signal modulator depends on the ratio of  $V_{OUT}$  and  $V_{IN}$ . As such, the output signal  $V_{DRI}$  can be used to determine the PWM signal of the power stage to regulate  $V_{OUT}$ .

Ripple-based control monitors the output voltage level and directly determines whether the delivered energy is sufficient. Given the fast transient response of the comparator, the power stage can be immediately controlled to deliver energy from  $V_{IN}$  to  $V_{OUT}$  corresponding to any sudden load transient variations. Thus, the output voltage is well regulated because periodic charging and discharging of adequate energy to the output capacitor occur through the use of an output voltage ripple as the PWM signal.

Ripple-based control techniques can be further classified according to on/off-time determination using the pulse signal modulator, as shown in Figure 4.2. The control parameters typically



**Figure 4.1** Generic block diagram of the ripple-based control technique



**Figure 4.2** Types of ripple-based control: (a) hysteretic-mode control; (b) constant off-time with peak voltage control; (c) constant on-time with valley voltage control; (d) constant frequency with peak voltage control; (e) constant frequency with valley voltage control

used to determine power delivery paths include peak/valley voltage, on/off-time of power switches, and clock-controlled or clock-free operation.

On-time and off-time periods are defined as the time periods when the inductor current increases and decreases, respectively. Within a switching cycle, inductor voltage-second balance in steady state is established if the inductor current waveform increases and decreases portions equally. Considering energy conservation and complementary theory, the capacitor charge-second balance also ensures that no extra net charge is retained at the output capacitor in steady state.

The subsequent discussion shows how each control method determines the pulse width, including its starting and ending times. We can call the determination of starting and ending times as the setting (S) and resetting (R) points of the pulse width, respectively. For example, the hysteretic control shown in Figure 4.2(a) utilizes peak and valley voltages to compare two predefined reference voltages, namely the upper bound  $V_{REF,1}$  and the lower bound  $V_{REF,2}$ , and determine the R and S points of one PWM signal, respectively. In this implementation, two comparators are needed.

However, the off-time control shown in Figure 4.2(b) utilizes a constant off-time (COT) period to determine the next pulse starting time (S point) and one upper bond reference voltage, which is the peak voltage detection, to determine the ending time (R point) of the pulse. By contrast, the on-time control shown in Figure 4.2(c) utilizes a constant on-time period to determine the ending time (R point) of the pulse width and one lower bond reference voltage, which is the valley voltage detection, to determine the next pulse starting time (S point). In this implementation, only one comparator is needed, as shown in Figure 4.2(b) or (c).

The methods shown in Figure 4.2(a)–(c) are called clock-free control because they lack the constant frequency generated by the clock generator. Filtering out the switching noise is sometimes difficult, because the switching frequency is variable and unpredictable. Therefore, a constant frequency with peak voltage control, as shown in Figure 4.2(d), utilizes one constant switching frequency and peak voltage detection to regulate the output. Similarly, Figure 4.2(e) uses constant frequency with valley voltage control to regulate the output voltage. Given that the constant switching period ( $T_{SW}$ ) is known, the output filter is easily designed to remove any switching noise.

The characteristics of a boost converter, which is different from a ripple-based control buck converter, induce several design challenges if ripple-based control is used. For example, the use of a discontinuous inductor current for the output node results in difficult current sensing through the equivalent series resistance of the output capacitor because it lacks one part of the inductor current information if the low-side power switch is turned on. Moreover, the inherent RHP zero causes difficulty during stability analysis. Generally speaking, the RHP zero should not be smaller than the UGF because the RHP zero increases the gain but degrades the phase. The compensated system loop is designed to push the RHP zero beyond the UGF.

As a result, the maximum UGF is constrained not only by its inherent switching frequency but also by the existing RHP zero. The transient response performance degrades because of the limited UGF. After describing the ripple-based control buck converter, the ripple-based control boost converter will be discussed by introducing specific techniques used to obtain fast transient response without being affected by the RHP zero.

Detailed analyses and design principles for different types of ripple-based control buck converters are also discussed in subsequent sections. The asynchronous power stage of the buck converter, which contains a high-side switch ( $M_S$ ), asynchronous diode ( $D$ ), inductor ( $L$ ), and capacitor ( $C$ ), is used to simplify the analysis. Moreover, before stability is considered and analyzed in detail later, an ESR in the output capacitor is assumed to be sufficiently large so that the output voltage ripple is proportional to the inductor current ripple.

#### 4.1.1 Hysteretic Control

Figure 4.3 shows the architecture of a buck converter with hysteretic control. The hysteretic window ( $V_H$ ) in the comparator can determine the DC voltage level and the peak-to-peak voltage ripple at the output. In the steady state, the output voltage is limited within the predefined hysteresis window.

Figure 4.4 illustrates the mechanism of the waveforms of feedback voltage ( $v_{FB}$ ), driving signal ( $v_G$ ), inductor current ( $i_L$ ), and output loading condition ( $i_{Load}$ ). Comparing  $v_{FB}$  with the upper and lower boundaries  $V_{REF}$  and  $V_{REF} + V_H$ , respectively, determines the on-time and off-time periods, where  $V_H$  is the hysteresis window of the comparator. When the converter

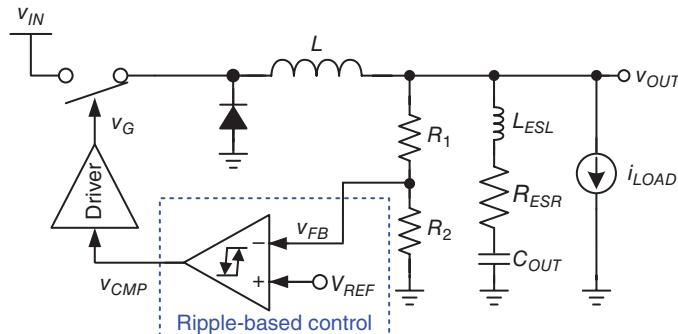


Figure 4.3 DC/DC buck converter with hysteretic control

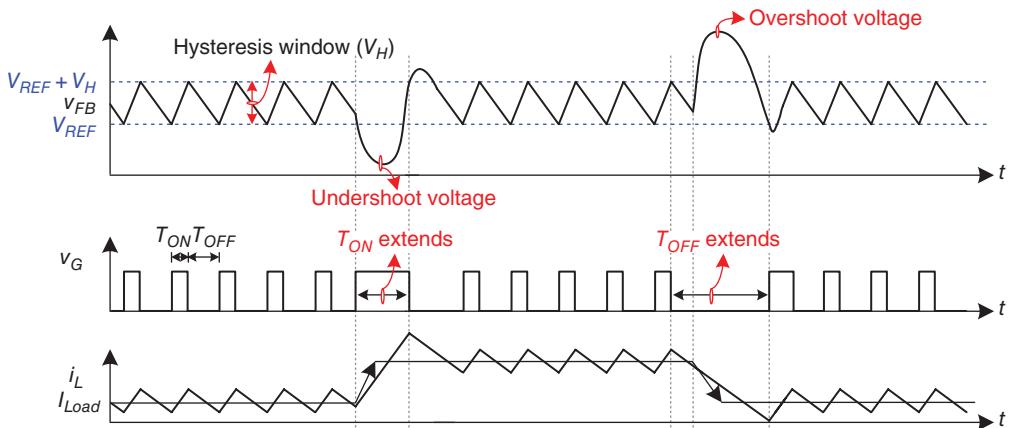


Figure 4.4 Waveforms of the buck converter with hysteretic-mode control

operates in the on-time period,  $M_S$  turns on to store energy in the inductor  $L$ . Thus,  $i_L$  increases and causes an increase in  $v_{OUT}$  and  $v_{FB}$ . When  $v_{FB}$  exceeds the value  $V_{REF} + V_H$ , the on-time period expires. The converter switches to the off-time period. In other words,  $M_S$  turns off to release the energy stored in the inductor  $L$  to the output. Thus,  $i_L$  decreases and causes a decrease in  $v_{OUT}$  and  $v_{FB}$ . When  $v_{FB}$  is less than  $V_{REF}$ , the off-time period expires to repeat another on-time period in the next switching cycle.

When the load current changes from light to heavy, the undershoot voltage at  $v_{OUT}$  triggers an extension of the on-time period until  $v_{FB}$  crosses the value  $V_{REF} + V_H$ . By contrast, in case of heavy-to-light load change, the overshoot voltage at  $v_{OUT}$  extends the off-time period and prevents extra energy from being delivered to the output. When  $v_{FB}$  is less than  $V_{REF}$ , the off-time ends and the on-time period starts again. The extension of the on/off-time period can speed up the transient response because of effective energy control to the output. Compared with PWM control, the hysteretic mode of ripple-based control can instantly adjust the duty cycle equivalent to 100% or 0% even during light-to-heavy or heavy-to-light load transient response,

respectively. As for PWM, the changing speed of the duty cycle depends on the UGF of the system loop, and the duty cycle can only increase or decrease gradually according to the slow change of output voltage of the error amplifier. Specifically, hysteretic mode control achieves fast transient response.

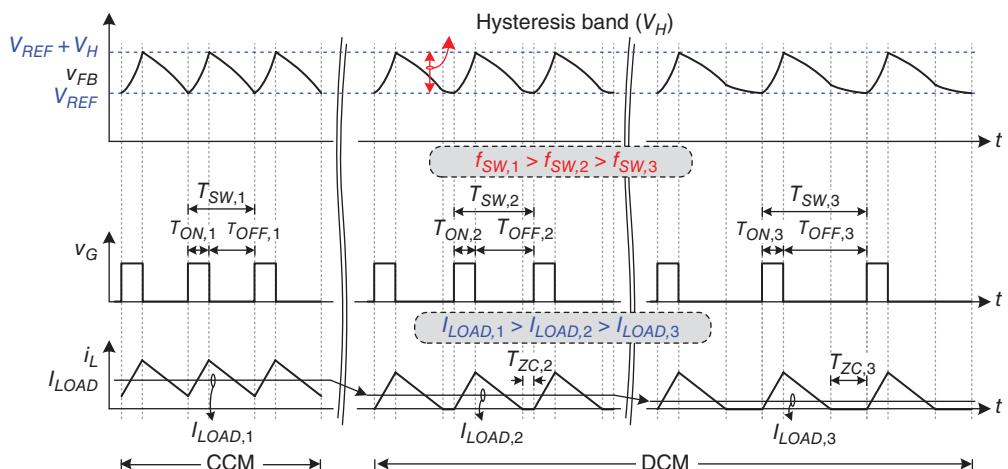
The switching frequency ( $f_{SW}$ ) of hysteretic mode control is expressed in Eq. (4.1). A major disadvantage of hysteretic mode control is the large variation of  $f_{SW}$ , a variation that is caused by the variable ESR of the output capacitor, output inductor, and input and output voltages. The effective hysteresis window  $V_{H(eff)}$  can be expressed in Eq. (4.2) if non-ideal effects are considered.

$$f_{SW} = \frac{R_{ESR}}{V_{H(eff)}L} \cdot \frac{(v_{IN} - v_{OUT}) \times v_{OUT}}{v_{IN}} \quad (4.1)$$

where

$$V_{H(eff)} = V_H \cdot \left( 1 + \frac{R_2}{R_1} \right) - \frac{L_{ESL}}{L} \cdot v_{IN} + T_{OFF} \cdot \frac{v_{IN} - v_{OUT}}{L} \cdot R_{ESR} + T_{ON} \cdot \frac{v_{OUT}}{L} \cdot R_{ESR} \quad (4.2)$$

Consequently, defining the operating frequency in comparison with other clock-based control techniques is difficult. Hysteretic mode control is unsuitable for several circuits that are sensitive to EMI because of the varying switching frequency, which apparently decreases when the converter operates in the DCM. As shown in Figure 4.5, the value of  $f_{SW}$  and the output voltage waveform in the CCM are different from those in the DCM. In DCM operation, the inductor current is reset to zero before the beginning of the next on-time period. Assuming that  $R_{ESR}$  of the output capacitor is sufficiently large to have an in-phase relationship between  $v_{OUT}$  and  $i_L$ , the constant value of the hysteresis window indicates that constant power is delivered to the inductor because of the constant on-time period,  $T_{ON,1} = T_{ON,2} = T_{ON,3}$ . By contrast, the



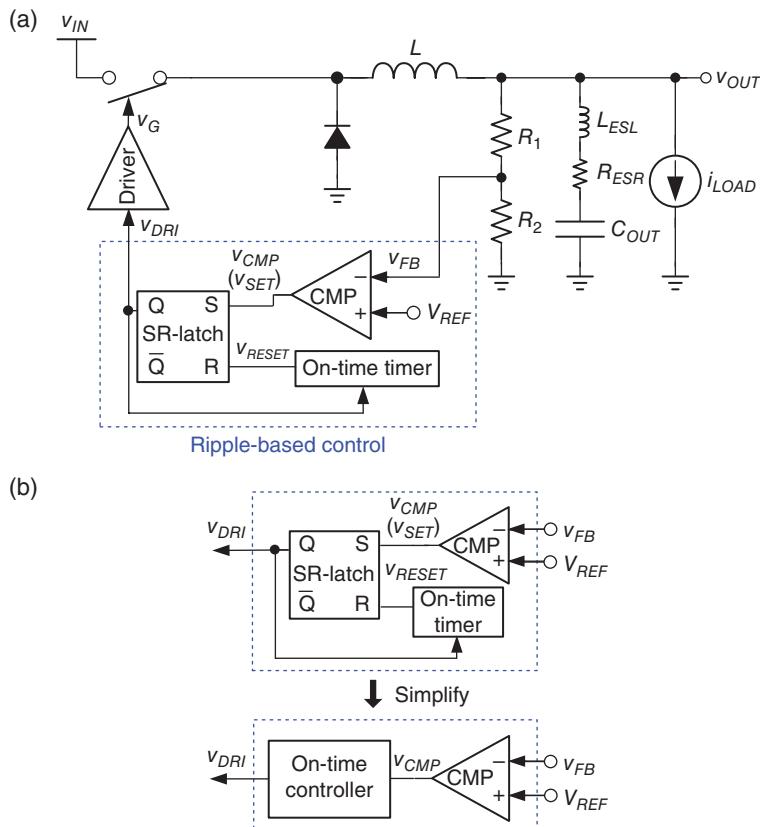
**Figure 4.5** Characteristics of frequency variation in the buck converter with hysteretic-mode control when working in CCM and DCM under different loading conditions

energy dissipation rate slows down if a longer off-time period exists at light loads compared with that at heavy loads. As a result, the off-time period is extended if a constant on-time period is set; in other words,  $T_{OFF,1} < T_{OFF,2} < T_{OFF,3}$ . Thus, the switching frequency decreases; in other words,  $f_{SW,1} > f_{SW,2} > f_{SW,3}$ . Consequently, the switching loss is reduced to improve the power-conversion efficiency.

Hysteretic-mode control exhibits a simple structure and fast transient response. However, determining the hysteretic window  $V_H$  to achieve the expected specifications and identify the trade-off between output voltage ripple and regulation performance is complex because the output voltage ripple and switching frequency depend heavily on  $V_H$ ,  $v_{IN}$ ,  $v_{OUT}$ ,  $L$ , and several parasitic components.

#### 4.1.2 On-Time Control

Figure 4.6(a) shows the architecture of the buck converter with on-time control. Figure 4.6(b) illustrates simplified block diagrams for easy analysis in this book. The characteristics of the

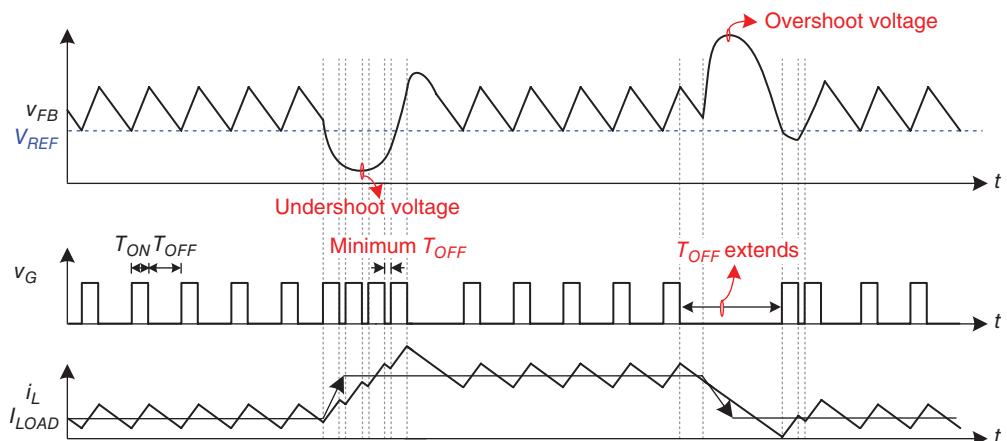


**Figure 4.6** (a) DC/DC buck converter with constant on-time control technique. (b) Simplification of the on-time controller

on-time controller with slew rate (SR) latch include one constant on-time timer and one comparator, which are used to determine the on-time and off-time periods, respectively. During the on-time period, the increasing inductor current causes a simultaneous increase in  $v_{OUT}$  and  $v_{FB}$ . After a time period predefined by the on-time timer, the resetting pulse can be determined and the on-time period is ended to start the off-time period. Similarly, the decreasing inductor current causes a decrease in  $v_{OUT}$  and  $v_{FB}$  during the off-time period. When  $v_{FB}$  crosses the lower boundary  $V_{REF}$ , the comparator determines the setting pulse and outputs a low-to-high signal to end the off-time period and initiate the next on-time period.

Figure 4.7 shows the steady-state and transient waveforms. Undershoot voltage at  $v_{OUT}$  and  $v_{FB}$  occurs when the load current changes from light to heavy. The on-time period starts instantly once  $v_{FB}$  is less than  $V_{REF}$ . Several on-time periods are triggered continuously with the addition of the minimum off-time period between each on-time period, until  $v_{FB}$  is higher than  $V_{REF}$  again. Although the maximum duty cycle is constrained by the minimum off-time, the duty cycle can change instantly from the steady-state value to the maximum value in case of load transient response. Thus, on-time control can achieve a fast transient response compared with the gradual adjustment in PWM control by an error-voltage amplifier. By contrast, the off-time period is extended to ensure that surplus energy can be adequately discharged to output loading because of the overshoot voltage at  $v_{OUT}$  and  $v_{FB}$  in case of a heavy-to-light load change. Consequently, determining adequate power delivery paths during load transient response can benefit fast charging or discharging at the output capacitor by prolonging the on-time or off-time periods, respectively.

The worst case in transient response and overshoot voltage is any sudden load release during the on-time period if a constant on-time period is used, because the on-time period cannot be instantly terminated until the predefined constant on-time period expires. Unexpected power delivery paths result in a large overshoot voltage with surplus energy at the output. In particular, the overshoot voltage may cause permanent damage to the back-end circuits in the nanometer process, which implies low voltage stress ability.



**Figure 4.7** Waveforms of the DC/DC buck converter with constant on-time control in the CCM operation

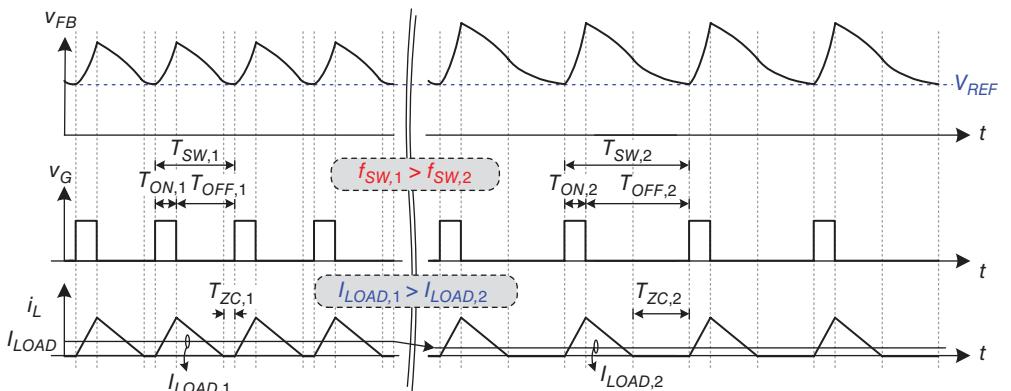
The switching frequencies in CCM and DCM are expressed in Eqs. (4.3) and (4.4), respectively:

$$f_{SW} = \frac{v_{OUT}}{v_{IN} \cdot T_{ON}} \quad (4.3)$$

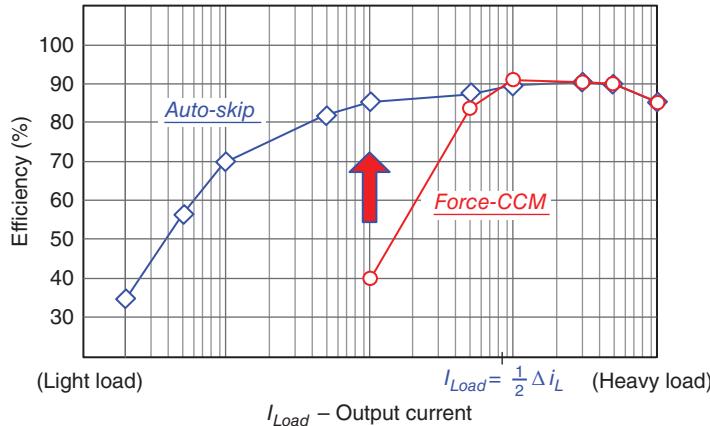
$$f_{SW} = \frac{2Li_{LOAD}v_{OUT}}{T_{ON}^2(v_{IN} - v_{OUT})v_{IN}} \quad (4.4)$$

The switching frequency  $f_{SW}$  in the CCM operation without any internal clock generators can easily be defined by  $v_{IN}$ ,  $v_{OUT}$ , and  $T_{ON}$ . If a predefined on-time period is determined, then  $f_{SW}$  in the CCM can be kept constant. By contrast,  $f_{SW}$  in the DCM is proportional to the output loading condition  $i_{Load}$ , which is similar to the pulse frequency modulation (PFM) control [1].

Figure 4.8 shows the reduction in switching power loss because of the decrease in switching frequency at light loads. During the predefined constant on-time period, the inductor current increases to the same peak value and induces the same energy, which is delivered to the output. In the beginning of the off-time period, the inductor current first decreases to zero. At this moment, the output voltage is still higher than the rated voltage, indicating that a switching operation to deliver energy to the output is unnecessary. Before  $v_{FB}$  reaches  $V_{REF}$ , the output capacitor mainly provides energy to the output loading. Figure 4.8 shows that the light loading condition extends the off-time period ( $T_{OFF,1} < T_{OFF,2}$ ) because the power dissipation rate becomes slow at light loads ( $T_{ZC,1} < T_{ZC,2}$ ). As a result, the switching period should be extended ( $T_{SW,1} < T_{SW,2}$ ) if the same energy is stored in the inductor during one constant on-time phase ( $T_{ON,1} = T_{ON,2}$ ). When the loading current decreases continuously, the extended switching period implies a continuously reduced switching frequency ( $f_{SW,2} < f_{SW,1}$ ) and reduces the switching power loss for high power efficiency. The constant on-time control has the advantage of an approximately constant switching frequency design in the CCM operation. Meanwhile, the converter can automatically transfer to variable frequency control in the DCM operation to save power without adding any mode decision control circuits. A seamless transition from



**Figure 4.8** Waveforms of the DC/DC buck converter with constant on-time control in the DCM operation



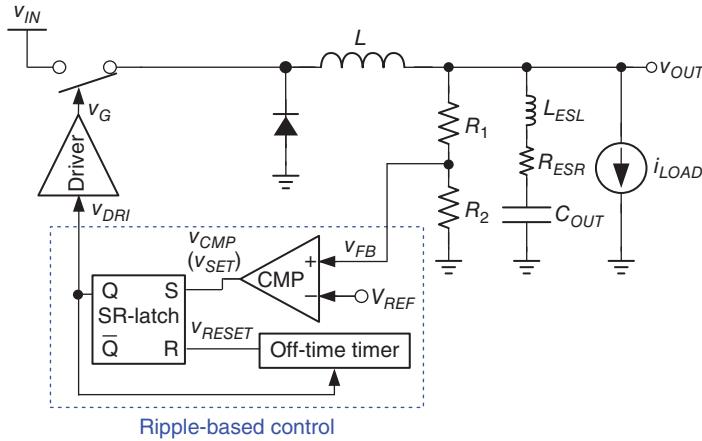
**Figure 4.9** Power-conversion efficiency of the DC/DC converter with constant on-time control

CCM to DCM, and vice versa, occurs in this type of control method. As such, the constant on-time control has become well known in recent portable electronics because of its power-saving ability at light loads.

Figure 4.9 shows an example of efficiency improvement by DCM operation in the constant on-time control buck converter. When the operating mode of the converter is set as Force-CCM mode, the inductor current exhibits a triangular waveform without any zero current detection regardless of whether heavy or light loading conditions occur. When the average load current is smaller than half the inductor current ripple ( $I_{LOAD} < 1/2\Delta i_L$ ), the inductor current crosses the zero current and is negative, where  $\Delta i_L$  is the inductor current ripple. This operating mode can result in an approximately constant switching frequency. However, the light-load power-conversion efficiency will degrade drastically because the switching loss dominates the power loss and the negative inductor current consumes extra conduction loss. By contrast, when the operating mode of the converter is set as Auto-Skip mode and when the load current is larger than half the inductor current ripple ( $I_{LOAD} > 1/2\Delta i_L$ ), the inductor current is operated in the CCM. When the load current is smaller than half the inductor current ripple ( $I_{LOAD} < 1/2\Delta i_L$ ), the converter automatically changes the operating mode to DCM and the switching frequency can decrease dynamically, corresponding to the decreasing loading conditions. The switching power loss can thus be reduced.

#### 4.1.3 Off-Time Control

Figure 4.10 displays the architecture of a buck converter with the constant off-time control. In contrast to the COT, the constant off-time control uses one constant off-time timer instead of a constant on-time timer. Thus, the comparator compares  $v_{FB}$  and the upper boundary  $V_{REF}$  to determine the on-time period. During the on-time period, the increasing inductor current causes an increase in  $v_{OUT}$  and  $v_{FB}$ . When  $v_{FB}$  exceeds  $V_{REF}$ , the resetting pulse can be determined and the on-time period expires to start the off-time period. Similarly, the decreasing inductor current causes a decrease in  $v_{OUT}$  and  $v_{FB}$ . The constant off-time timer provides a predefined off-time



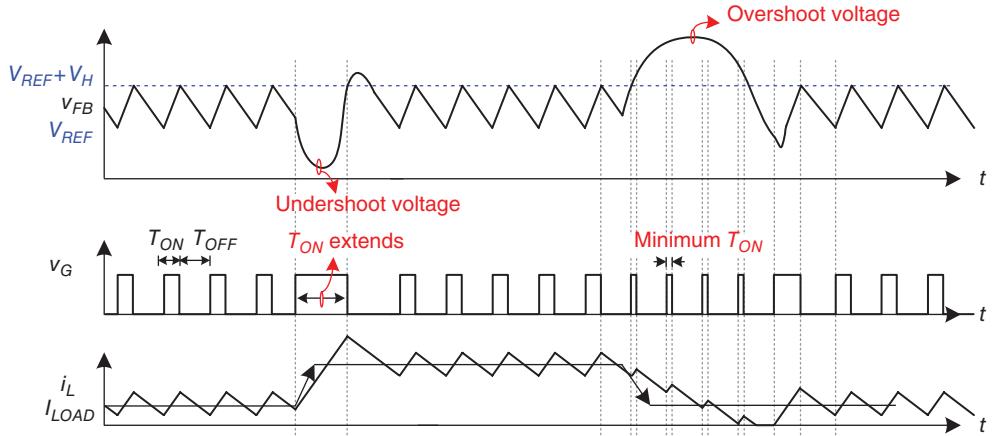
**Figure 4.10** DC/DC buck converter with constant off-time control

period to determine the setting pulse when the off-time period is over, so that the converter can initiate the next on-time period. Given that the off-time period is constant, the switching frequency can vary within a small range in steady state. With the constant off-time control, the on-time period also varies with the corresponding adequate value to meet the requirements of conversion ratio and loading conditions. It indicates the switching frequency cannot be decreased to improve efficiency and to extend battery usage time because the on-time period is reduced in the DCM operation. As such, the constant off-time control seems unsuitable for portable electronics because this control has a constant off-time period and fails to improve efficiency.

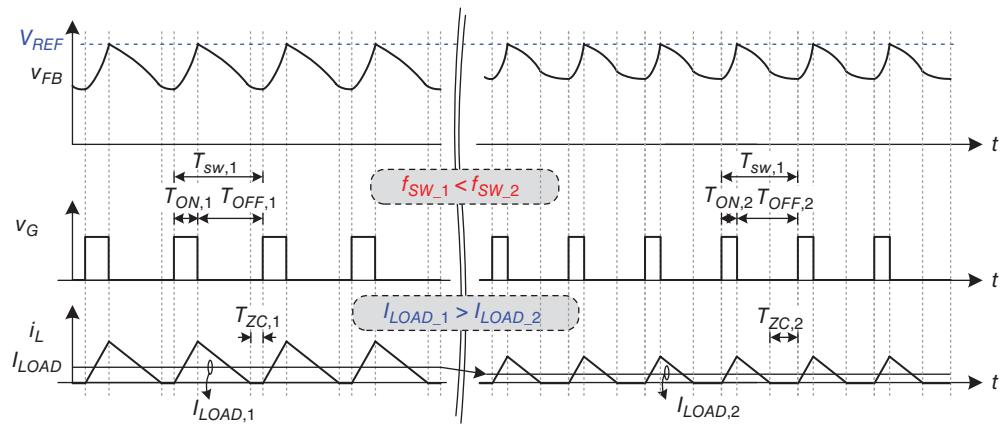
Figure 4.11 shows the steady-state and transient response waveforms. When the load current changes from light to heavy, the undershoot voltage at  $v_{OUT}$  and  $v_{FB}$  triggers the on-time period until  $v_{FB}$  is higher than  $V_{REF}$ . By contrast, in case of a load change from heavy to light, the converter keeps operating in numbers of predefined off-time-period fragments with the addition of the minimum on-time period. In other words, compared with hysteretic mode control, off-time control exhibits the same performance of the load transient when a light-to-heavy load transient occurs, but exhibits slow performance when a heavy-to-light load transient occurs. However, compared with PWM control with an error-voltage amplifier, instantly adjusting the adequate power delivery paths during a load transient can still result in fast charging and discharging at the output capacitor with adjustable on-time and off-time periods, respectively. A disadvantage of constant off-time control is that the switching frequency increases at light loads because of the decrease in on-time period. Thus, constant off-time control is unsuitable for portable electronics. Furthermore, in case of a light-to-heavy load change during constant off-time period, another disadvantage is the unexpected power delivery paths that result in a large undershoot voltage and insufficient energy delivered at the output.

In steady state, the switching frequency in CCM operation is derived as:

$$f_{sw} = \frac{v_{IN} - v_{OUT}}{v_{IN} T_{OFF}} \quad (4.5)$$



**Figure 4.11** Waveforms of the DC/DC buck converter with constant off-time control in the CCM operation



**Figure 4.12** Waveforms of the DC/DC buck converter with constant off-time control in the DCM operation

Equation (4.5) shows that the switching frequency can easily be designed and kept constant without the need for any internal clock generators if  $v_{IN}$ ,  $v_{OUT}$ , and  $T_{OFF}$  are well known. However, light loading conditions cause high switching frequencies when the converter operates in DCM. The switching frequency in DCM is expressed in Eq. (4.6), based on the principle of inductor voltage-second balance:

$$f_{SW} = \left( T_{OFF} + \frac{L \cdot i_{LOAD} \cdot v_{OUT}}{(v_{IN} - v_{OUT})v_{IN}} + \sqrt{\frac{(L \cdot i_{LOAD} \cdot v_{OUT})^2}{((v_{IN} - v_{OUT})v_{IN})^2} + \frac{2T_{OFF}}{(v_{IN} - v_{OUT})v_{IN}}} \right)^{-1} \quad (4.6)$$

Figure 4.12 shows that the reduced on-time period ( $T_{ON,1} > T_{ON,2}$ ) causes the lower peak inductor current corresponding to the decrease in loading current because of the constant

off-time period ( $T_{OFF,1} = T_{OFF,2}$ ) in each switching cycle. Energy storage and release at the output capacitor can be in a state of equilibrium. Thus, the output voltage can be regulated. However, the increase in switching frequency ( $f_{SW,1} < f_{SW,2}$ ) at light loads results in a high switching power loss and low power-conversion efficiency.

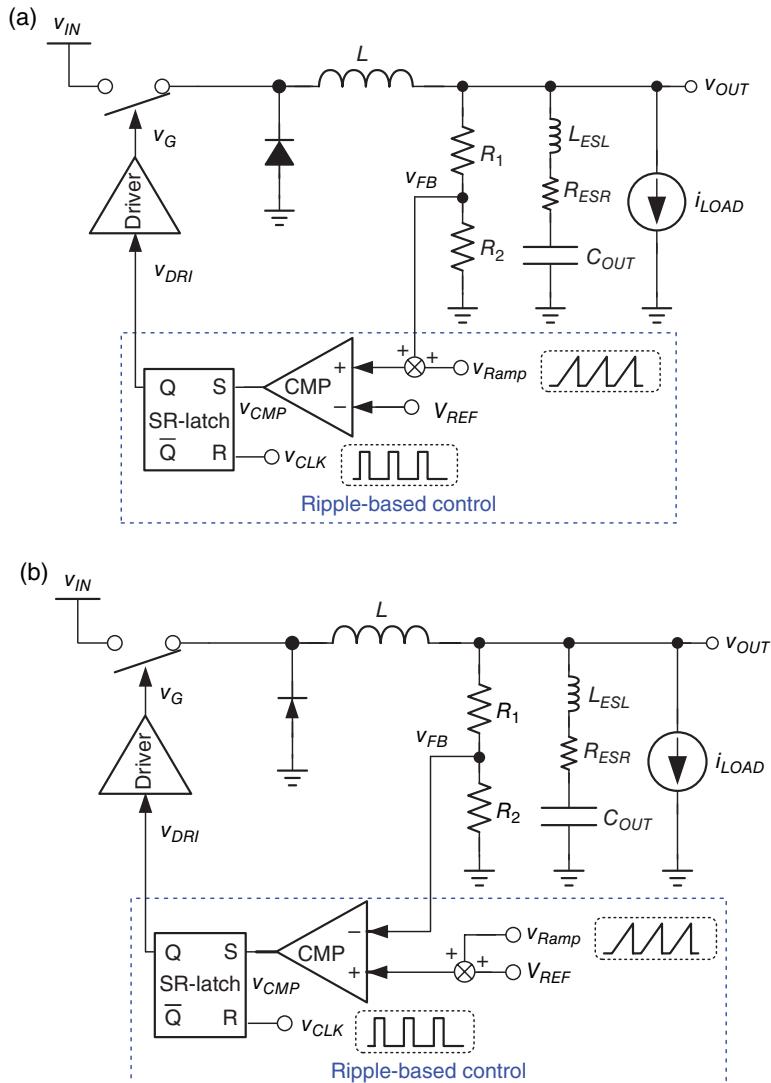
Constant off-time control exhibits a good transient response and a simple structure that can be used to design the switching frequency in the CCM. However, constant off-time control exhibits poor power-conversion efficiency in the DCM. By contrast, peak voltage control with constant off-time control can have a constant current-driving capability in power converters for commercial light-emitting diode (LED) drivers, because LEDs need constant current-driving control.

#### *4.1.4 Constant Frequency with Peak Voltage Control and Constant Frequency with Valley Voltage Control*

Figure 4.13(a), (b) shows the constant frequency with peak voltage control and the constant frequency with valley voltage control, respectively. To our knowledge, constant on-time and off-time controls determine the on-time and off-time periods and the beginning times of the off-time and on-time, respectively. Similarly, the constant frequency with peak voltage control determines the beginning of the on-time and the off-time by simply using the clock and peak voltage detection, respectively. By contrast, the constant frequency with valley voltage control determines the beginning of the on-time and the off-time by using valley voltage detection and the clock, respectively.

Moreover, the switching frequency is constant so that it induces a reduction in EMI, because the EMI filter can be well designed if the switching frequency is known. However, a constant switching frequency results in a slightly slow transient response and high power consumption compared with the previous control topologies. This outcome is attributed to the operation maintaining a constant switching frequency in the CCM and DCM without the ability to increase or decrease the switching frequency for fast transient response or power saving, respectively. The switching power loss cannot be reduced by the decrease in switching frequency, so that the power-conversion efficiency with the DCM operation is worse than that with the COT control. An additional load-dependent controller can be used to dynamically adjust the switching frequency at light loads at the cost of circuit complexity, thus improving the power-conversion efficiency.

The inductor current ripple is derived through inductor charging or discharging of the output capacitor if the ESR is sufficiently large. Without using any error amplifiers, a fast transient response can be obtained compared with current-mode/voltage-mode PWM control. An extra sawtooth signal can be added to the feedback path to improve the noise margin between the two input terminals of the comparator. Double-pulse phenomena will not occur after enlarging the noise margin because the difference between the two inputs of the comparator is sufficiently large to have high noise immunity. The reference voltage  $V_{REF}$  can also be replaced by an integrating error amplifier with two inputs, namely  $V_{REF}$  and  $v_{OUT}$ , to improve accuracy. Two feedback signals from the output contribute to the design of the V-square ( $V^2$ ) control, which can ensure fast transient response and high accuracy at the same time.



**Figure 4.13** (a) Constant frequency with peak voltage control. (b) Constant frequency with valley voltage control

#### 4.1.5 Summary of Topology of Ripple-Based Control

The common advantages of ripple-based control methods are listed as follows:

1. The modulation signal is derived directly from the comparator without using any error amplifiers.
2. The comparator has a wide bandwidth for fast transient response.

3. A simple structure can be achieved because of the absence of error amplifiers and an extra compensation network.
4. Clock-free operation, excluding constant frequency control, does not need any clock generators.
5. High power-conversion efficiency is obtained because of the variable switching frequency at light loads in the hysteretic mode and constant on-time controls.

Simple ripple-based control without any complex compensation network has the advantage of low cost. In particular, a wide bandwidth guarantees a fast transient response because of the utilization of a comparator. Furthermore, when operating at light loads, the switching frequency is automatically adjusted with the implementation of a zero current detector according to the output loading condition without additional complex frequency tuners. In other words, the converter is controlled by variable frequency modulation (VFM) to save significant switching power loss for high power-conversion efficiency at light loads for portable power electronics. Consequently, ripple-based control has become a suitable choice in many power management designs.

However, ripple-based control has several practical problems and limitations, as follows:

1. Trade-off between sub-harmonic instability and output voltage ripple owing to the selection constraint of the output capacitor.
2. EMI caused by the poorly defined switching frequency of the clock-free characteristic (except for constant frequency control).
3. Jitter behavior caused by low noise immunity.
4. Inaccurate DC regulation caused by low gain loop and direct peak/valley control.

Some of these problems can be improved by recently developed techniques. Table 4.1 shows a comparison of the different structures of ripple-based control in DC/DC buck converters. The superior performance of on-time control has led to its popularity in portable electronics.

**Table 4.1** Comparison of different structures of ripple-based control in buck converter

	Transient response	Frequency in CCM	Frequency in DCM	Efficiency in DCM
Hysteretic control	Excellent	Difficult to determine and keep constant	Decreased frequency with decreased load	Very good
On-time control	Very good	Easy to determine and keep constant	Decreased frequency with decreased load	Excellent
Off-time control	Very good	Easy to determine but difficult to keep constant	Increased frequency with decreased load	Very poor
Constant frequency with peak voltage control	Good	Constant	Constant	Poor
Constant frequency with valley voltage control	Good	Constant	Constant	Poor

## 4.2 Stability Criterion of On-Time Controlled Buck Converter

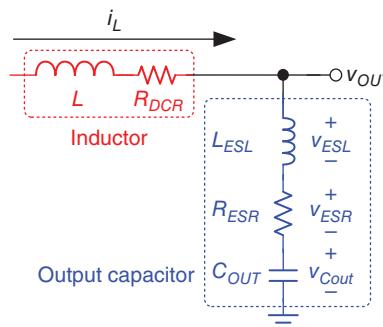
Among the above topologies, on-time control is the most popular nowadays because the converter with on-time control features a fast transient and high efficiency. This kind of power converter is the most likely solution for Soc power supply, with its wide load range and minimized variation at the supply voltage in transient response and steady state. Thus, we need to derive the stability criterion of on-time control. This will be discussed later. Other topologies can use the same criterion to guarantee converter stability. However, similar to PWM control, only constant frequency control suffers from sub-harmonic oscillation. In order to prevent sub-harmonic oscillation, slope compensation can also be taken into consideration.

### 4.2.1 Derivation of the Stability Criterion

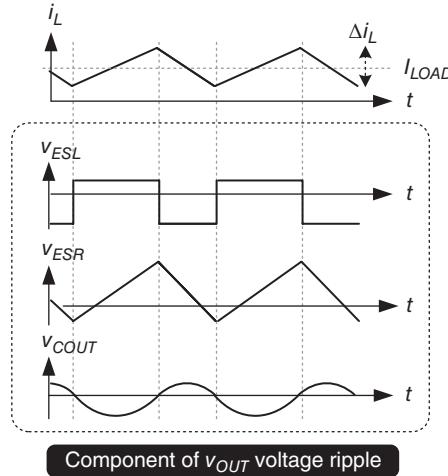
A power stage, with power switches and an LC filter, has energy storage and power transfer functions. Figure 4.14 shows such an LC filter. The inductor is modeled as one ideal inductor,  $L$ , and one parasitic DC resistance,  $R_{DCR}$ . The output capacitor is modeled as three components, including an equivalent series inductance,  $L_{ESL}$ ; an ESR,  $R_{ESR}$ ; and an ideal  $C_{OUT}$ . The output voltage waveform is generated by the voltage variation across each component due to the inductor current variation. The two parasitic components  $L_{ESL}$  and  $R_{ESR}$  in the output capacitor should be considered during ripple-based control because the output voltage waveform is significantly affected by these parasitic components. Thus, stability should be increased even under the influence of parasitic effects.

Figure 4.15 shows the waveforms of the inductor current and the voltages across each component in the output capacitor. The AC component of the inductor current flows into the output capacitor and results in  $v_{ESL}$ ,  $v_{ESR}$ , and  $v_{COUT}$ , which are contributed by  $L_{ESL}$ ,  $R_{ESR}$ , and  $C_{OUT}$ , respectively. The corresponding equations for these voltage ripples are derived as Eqs. (4.7)–(4.9):

$$\begin{aligned} \text{On-time phase: } v_{ESR}(t) &= R_{ESR} \left( \frac{\Delta I \cdot t}{D \cdot T_{SW}} - \frac{\Delta I}{2} \right) \\ \text{Off-time phase: } v_{ESR}(t) &= R_{ESR} \left( \frac{\Delta I}{2} - \frac{\Delta I \cdot t}{(1-D) \cdot T_{SW}} \right) \end{aligned} \quad (4.7)$$



**Figure 4.14** Modeling the output filter including the ideal inductor, the capacitor, and their corresponding parasitic characteristics



**Figure 4.15** Inductor current waveform and voltage waveform of each component in the complete output capacitor modeling

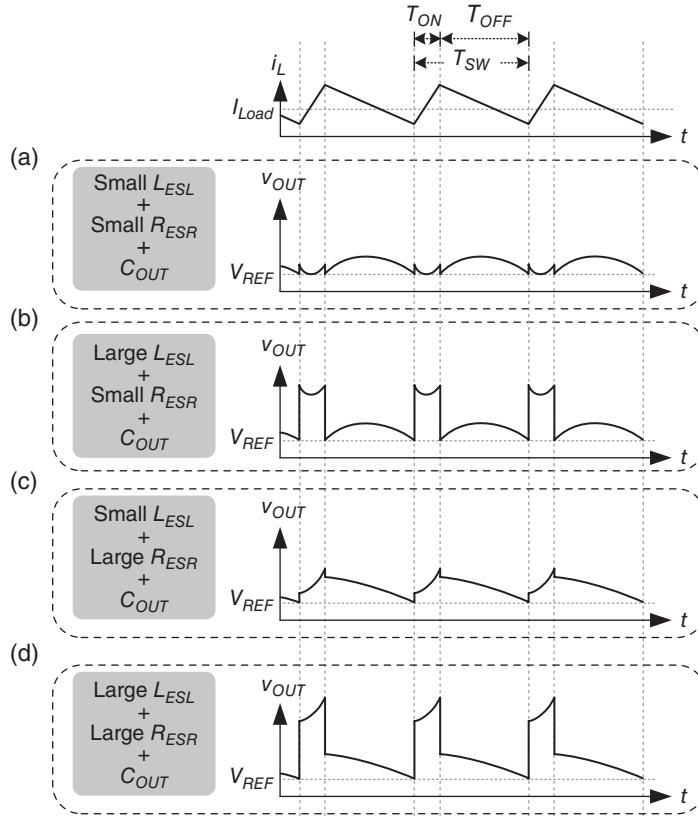
$$\begin{aligned} \text{On-time phase: } v_{ESL}(t) &= \frac{L_{ESL} \cdot \Delta I_L}{D \cdot T_{SW}} \\ \text{Off-time phase: } v_{ESL}(t) &= \frac{L_{ESL} \cdot \Delta I_L}{(1-D) \cdot T_{SW}} \end{aligned} \quad (4.8)$$

$$\begin{aligned} \text{On-time phase: } v_{COUP}(t) &= \frac{\Delta I_L \cdot t^2}{2C_{OUT} \cdot D \cdot T_{SW}} - \frac{\Delta I_L \cdot t}{C_{OUT}} \\ \text{Off-time phase: } v_{COUP}(t) &= \frac{\Delta I_L \cdot t}{C_{OUT}} - \frac{\Delta I_L \cdot t^2}{2C_{OUT} \cdot (1-D) \cdot T_{SW}} \end{aligned} \quad (4.9)$$

$$v_{COUP}(t) = \frac{\Delta I_L \cdot t}{C_{OUT}} - \frac{\Delta I_L \cdot t^2}{2C_{OUT} \cdot (1-D) \cdot T_{SW}}$$

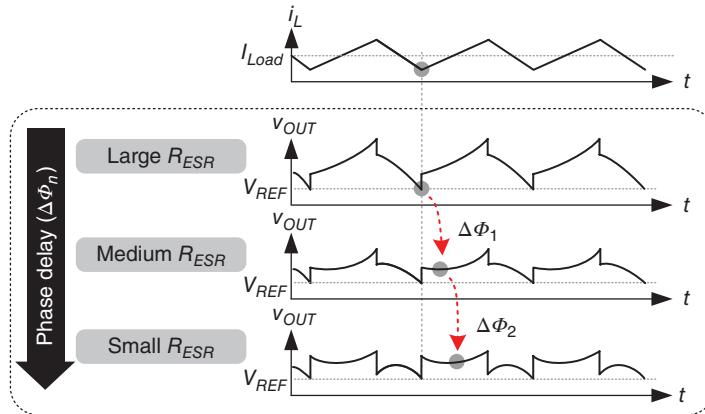
As a result, different output waveforms are generated by different quantities contributed by  $v_{ESL}$ ,  $v_{ESR}$ , and  $v_{COUP}$ . Figure 4.16 shows four examples to illustrate the waveforms with different values of  $L_{ESL}$ ,  $R_{ESR}$ , and  $C_{OUT}$ .

To compare the difference,  $L_{ESL}$  and  $R_{ESR}$  are varied, whereas  $C_{OUT}$  is set as constant. In case (a) with a small  $L_{ESL}$  and a small  $R_{ESR}$ , the voltage ripple caused by the inductor current charging/discharging  $C_{OUT}$  dominates  $v_{OUT}$ . The inductor current information is obtained by differentiating the output voltage ripple. Although a large  $C_{OUT}$  can be used to filter out the voltage ripple of the SWR and thus obtain a better quality of supply voltage, the small voltage ripple indicates that the differentiated voltage ripple will be small. In other words, the inductor current derived by the differentiating function has low noise immunity if a large  $C_{OUT}$  is used. The large inductor current information derived by the differentiating function and the low output ripple obtained by using a large  $C_{OUT}$  have conflicting requirements. Furthermore, in case (b) with a



**Figure 4.16** Output voltage ripple composed of different quantities contributed by  $v_{ESL}$ ,  $v_{ESR}$ , and  $v_{COUT}$  because of the different values of ESL, ESR, and  $C_{OUT}$ , respectively

large  $L_{ESL}$  and a small  $R_{ESR}$ , the voltage ripple caused by the ESL dominates  $v_{OUT}$ . The voltage ripple caused by a large  $L_{ESL}$  also deteriorates all the output ripples. Specifically, the use of the differentiating function to derive the inductor current will be more difficult because the differentiated signal is influenced by the ESL effect. In case (c) with a small  $L_{ESL}$  and a large  $R_{ESR}$ , the voltage ripple caused by  $R_{ESR}$  dominates  $v_{OUT}$ . The output ripple is in phase with the inductor current; that is, a large  $R_{ESR}$  can be used to generate the inductor current. In case of any switch turning on/off, the voltage ripple caused by the ESL will not affect the current-sensing performance. As such, ripple-based control always uses a large  $R_{ESR}$  to derive the inductor current information. Considering one possible scenario in which a large  $L_{ESL}$  and a large  $R_{ESR}$  occur simultaneously, as shown in case (d), the inductor current generated by  $R_{ESR}$  will initially deteriorate when the switch is turned on/off. Although the DC level of the sensing signal will change, the inductor current information can be derived by ripple-based control. Thus, we can conclude that the inductor current information can be derived through the use of a large  $R_{ESR}$ , which is the method used in conventional ripple-based control, or through the differentiating function that will be introduced in subsequent sections. Importantly, two methods are possibly



**Figure 4.17** Relationship between  $i_L$  and output voltage ripple under different  $R_{ESR}$  values

influenced by the large ESL. This finding indicates that several techniques that can inhibit the ESL effect should be proposed to ensure the robust operation of ripple-based control.

Considerable attention should be focused on selecting the appropriate output capacitor with certain quantities of parasitic components to guarantee the stability of ripple-based control. As shown in Figure 4.17, the output capacitor with different  $R_{ESR}$  values results in different output ripple characteristics. This phenomenon can be translated to the phase delay ( $\Delta\Phi$ ) related to the inductor current  $i_L$  caused by different parasitic  $R_{ESR}$  values. A small  $R_{ESR}$  value results in a long phase delay observed at the lowest value of  $v_{OUT}$ . Given a small  $R_{ESR}$  value, the system stability decreases because of an insufficient linear relationship between the inductor current ripple and the output voltage ripple. A small  $R_{ESR}$  value will decrease the system stability.

The stability criterion derived by using aspects of the S-domain and the time domain will be reviewed in detail to establish design guidelines.

#### 4.2.1.1 S-Domain Derivation (RHP Pole Consideration)

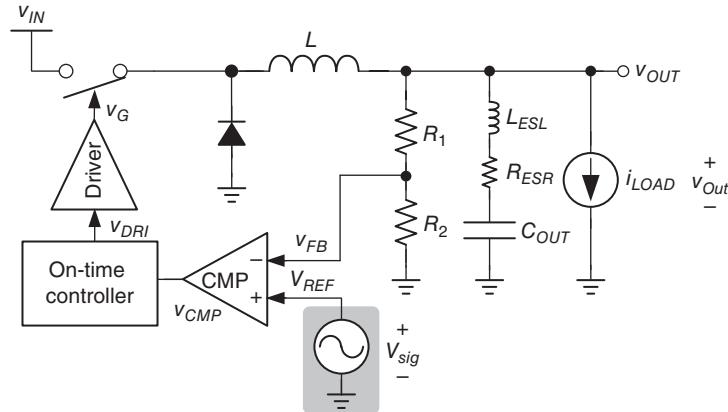
If the DC operating points are determined, then an AC test signal can be fed into the node of  $V_{REF}$  in Figure 4.18 to analyze the stability in the S-domain.

Based on the Padé approximant, the transfer function from the reference voltage to the output is approximated to a fourth-order equation, as expressed in Eqs. (4.10) and (4.11):

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{(R_{ESR}C_{COUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)} \quad (4.10)$$

where

$$\omega_1 = \frac{\pi}{T_{ON}}, \quad Q_1 = \frac{2}{\pi}, \quad \omega_2 = \frac{\pi}{T_{SW}}, \quad Q_2 = \frac{T_{SW}}{\left(R_{ESR}C_{COUT} - \frac{T_{ON}}{2}\right) \cdot \pi} \quad (4.11)$$



**Figure 4.18** Setup for deriving the transfer function

When the on-time value  $T_{ON}$  is sufficiently small and  $\omega_1$  locates at high frequencies, the transfer function can be simplified to a second-order equation:

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{(R_{ESR}C_{OUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)} \quad (4.12)$$

Given that  $Q_2$  must be larger than zero, the inequality in Eq. (4.13) can be derived to eliminate the unexpected RHP poles:

$$Q_2 = \frac{T_{SW}}{\left(R_{ESR}C_{OUT} - \frac{T_{ON}}{2}\right) \cdot \pi} > 0 \quad (4.13)$$

Then, the stability criterion is obtained:

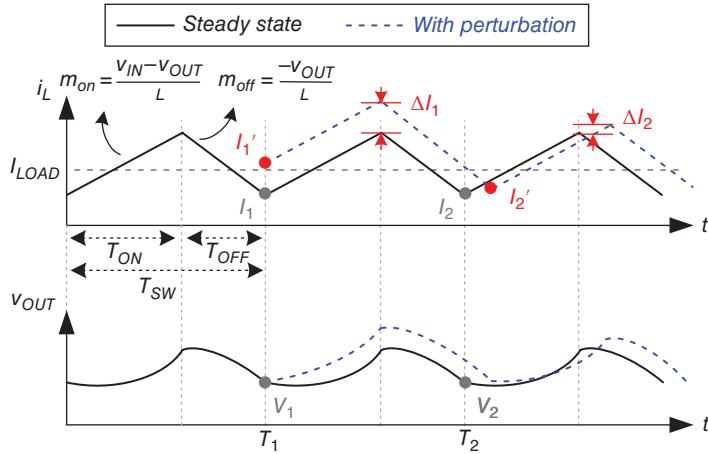
$$R_{ESR} \cdot C_{OUT} > \frac{T_{ON}}{2} \quad (4.14)$$

The time constant and the selection of  $R_{ESR}$  should meet the following requirement:

$$R_{ESR} > \frac{T_{ON}}{2C_{OUT}} \quad (4.15)$$

#### 4.2.1.2 Time Domain Derivation (Convergence Consideration)

When the stability criterion is derived based on the constraint set by the output capacitor, only  $C_{OUT}$  and  $R_{ESR}$  should be considered. The  $L_{ESL}$  effect can be ignored because the voltage ripple caused by the ESL is constant if  $v_{IN}$ ,  $v_{OUT}$ ,  $L$ , and  $L_{ESL}$  are kept constant. Figure 4.19 shows the



**Figure 4.19** Steady-state and perturbed waveforms caused by perturbation

steady-state and perturbed waveforms caused by perturbation in the time domain. The net change in output voltage should be zero after one switching period, as expressed in Eq. (4.16). In the CCM, the switching period  $T_{SW}$  is the summation of  $T_{ON}$  and  $T_{OFF}$ , which denote the on-time and off-time periods, respectively. The on-time and off-time inductor current slopes are expressed in Eq. (4.17).

$$V_2 - V_1 = \frac{1}{C_{OUT}} \int_0^{T_{SW}} [i_L(t) - i_{LOAD}] dt + (I_2 - I_1) R_{ESR} = 0 \quad (4.16)$$

where

$$T_{SW} = T_{ON} + T_{OFF} \text{ and } \begin{cases} \frac{di_L(t)}{dt} = \frac{v_{IN} - v_{OUT}}{L}, & \text{during the on-time period} \\ \frac{di_L(t)}{dt} = \frac{-v_{OUT}}{L}, & \text{during the off-time period} \end{cases} \quad (4.17)$$

In this study,  $T_{OFF}$  can be expressed as follows:

$$T_{OFF} = \left( \frac{v_{IN}}{v_{OUT}} - 1 \right) T_{ON} \quad (4.18)$$

By substituting Eq. (4.18) into Eq. (4.16), we derive

$$\frac{v_{IN}}{v_{OUT}} \cdot \frac{T_{ON}}{C_{OUT}} (I_1 - I_{OUT}) + \frac{T_{ON}^2}{2C_{OUT}L} \cdot \frac{v_{IN}}{v_{OUT}} (v_{IN} - v_{OUT}) + R_{ESR}(I_2 - I_1) = 0 \quad (4.19)$$

after evaluating the integration and simplification.

To conclude the stability criterion and linearization (Eq. (4.19)), the small perturbation signals  $\Delta I_1$  and  $\Delta I_2$  are considered in the steady-state inductor currents  $I_1$  and  $I_2$ . These currents, as shown in Eq. (4.20), are at  $T_1$  and  $T_2$ , respectively, according to the inductor current waveform in Figure 4.19.

$$\begin{cases} I_1 = i_{LOAD} - \frac{T_{ON}}{2L}(v_{IN} - v_{OUT}) \\ I_2 = i_{LOAD} - \frac{T_{ON}}{2L}(v_{IN} - v_{OUT}) \end{cases} \quad (4.20)$$

Consequently, the perturbed inductor currents  $I'_1$  and  $I'_2$  caused by perturbation at  $T_1$  and  $T_2$ , respectively, are expressed as:

$$\begin{cases} I'_1 = \Delta I_1 + i_{LOAD} - \frac{T_{ON}}{2L}(v_{IN} - v_{OUT}) \\ I'_2 = \Delta I_2 + i_{LOAD} - \frac{T_{ON}}{2L}(v_{IN} - v_{OUT}) \end{cases} \quad \text{and } I'_2 - I'_1 = \Delta I_2 - \Delta I_1 \quad (4.21)$$

The substitution of Eq. (4.21) into Eq. (4.19) derives

$$\Delta I_1 \left( R_{ESR} - \frac{v_{IN}}{v_{OUT}} \frac{T_{ON}}{C_{OUT}} \right) - \Delta I_2 R_{ESR} = 0 \quad (4.22)$$

$\Delta I_2 / \Delta I_1$  must be gradually converged to zero in steady state to increase the stability. Thus, the inequality is derived as Eq. (4.23) and simplified as Eq. (4.24):

$$\left| \frac{\Delta I_2}{\Delta I_1} \right| = \left| \frac{R_{ESR} - \frac{v_{IN}}{v_{OUT}} \frac{T_{ON}}{C_{OUT}}}{R_{ESR}} \right| < 1 \quad (4.23)$$

$$R_{ESR} \cdot C_{OUT} > \frac{T_{ON}}{2} \cdot \frac{v_{IN}}{v_{OUT}} \quad (4.24)$$

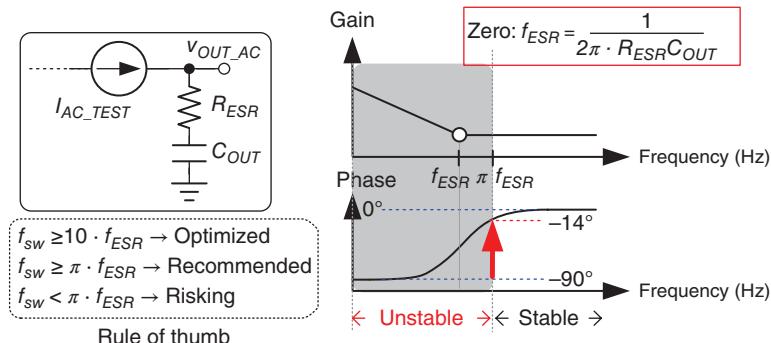
Finally, based on the definitions expressed in Eqs. (4.25) and (4.26), Eq. (4.27) is obtained to validate that the stability is not only related to the relationship of  $R_{ESR}$  and  $C_{OUT}$ , but also affected by the switching frequency.

$$f_{SW} = \frac{v_{OUT}}{v_{IN}} \cdot \frac{1}{T_{ON}} \quad (4.25)$$

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} C_{OUT}} \quad (4.26)$$

$$f_{SW} > \pi f_{ESR} \quad (4.27)$$

Capacitor choices are clearly limited to guarantee system stability. The stability criterion expressed in Eq. (4.27) also corresponds to the frequency response shown in Figure 4.20.



**Figure 4.20** Test model of the output capacitor and its frequency response with the stability criterion

The obtained AC response of the output ( $v_{OUT\_AC}$ ) indicates the design guideline. The combination of  $R_{ESR}$  and  $C_{OUT}$  contributes one zero to reduce the phase delay between inductor current ripple and output voltage ripple. System stability can be guaranteed because the phase is boosted from  $-90^\circ$  to  $-14^\circ$  at the preferred operation switching frequency. Consequently, we need to ensure that the switching frequency is sufficiently high to derive an adequate in-phase relationship between the two signals.

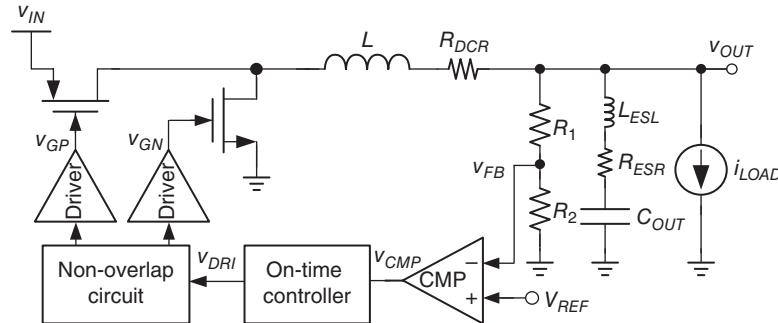
Based on the stability criterion, the switching frequency should be sufficiently high when a specific capacitor with a certain ESR value is used. When operating at high switching frequencies, the problem of phase delay can be solved. However, infinitely increasing the switching frequency to solve the stability issue is impractical because unreasonable switching power loss degrades the power-conversion efficiency. Moreover, the delay of the comparator influences stability. As such, any type of delay should be considered when the switching frequency is beyond megahertz values. By contrast, a large ESR value can increase the system stability.

However, a large ESR significantly increases the undershoot/overshoot voltage during transient response and results in a large output voltage ripple. The ESR value also varies with temperature and influences the average level of the output voltage. That is to say, the variation of output voltage and switching noise easily influences the supplied circuits. As a result, a suitable selection of capacitors with an adequate ESR is important. A robust converter cannot be influenced by the variation in ESR. The system stability and output performance of ripple-based control depend on the careful selection of output capacitor. The following examples show the design with the specialty polymer capacitor (SP-CAP). A stable operation can possibly be ensured if the switching frequency is increased to high.

#### Example 4.1: The basic on-time controlled DC/DC buck converter is affected by the $R_{ESR}$ value

Figure 4.21 shows the basic structure of the on-time controlled DC/DC buck converter. The specifications are listed in Table 4.2. Moreover, the other parameters are set as follows:  $R_1 = 200 \text{ k}\Omega$  and  $R_2 = 400 \text{ k}\Omega$ .

With a feedback loop, the expected  $v_{OUT}$  is 900 mV,  $f_{sw}$  is 1 MHz, and the duty ratio is 18% when the system is stable. Based on the stability criterion derived using Eq. (3.8) or Eq. (3.21), the stability of on-time control relies strongly on  $R_{ESR}$ .



**Figure 4.21** Basic on-time controlled DC/DC buck converter

**Table 4.2** Basic specifications used in Example 4.1

$V_{IN}$	$V_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	900 mV	600 mV	4.7 $\mu$ H	0 m $\Omega$	4.7 $\mu$ F	0 nH	180 ns	1 MHz

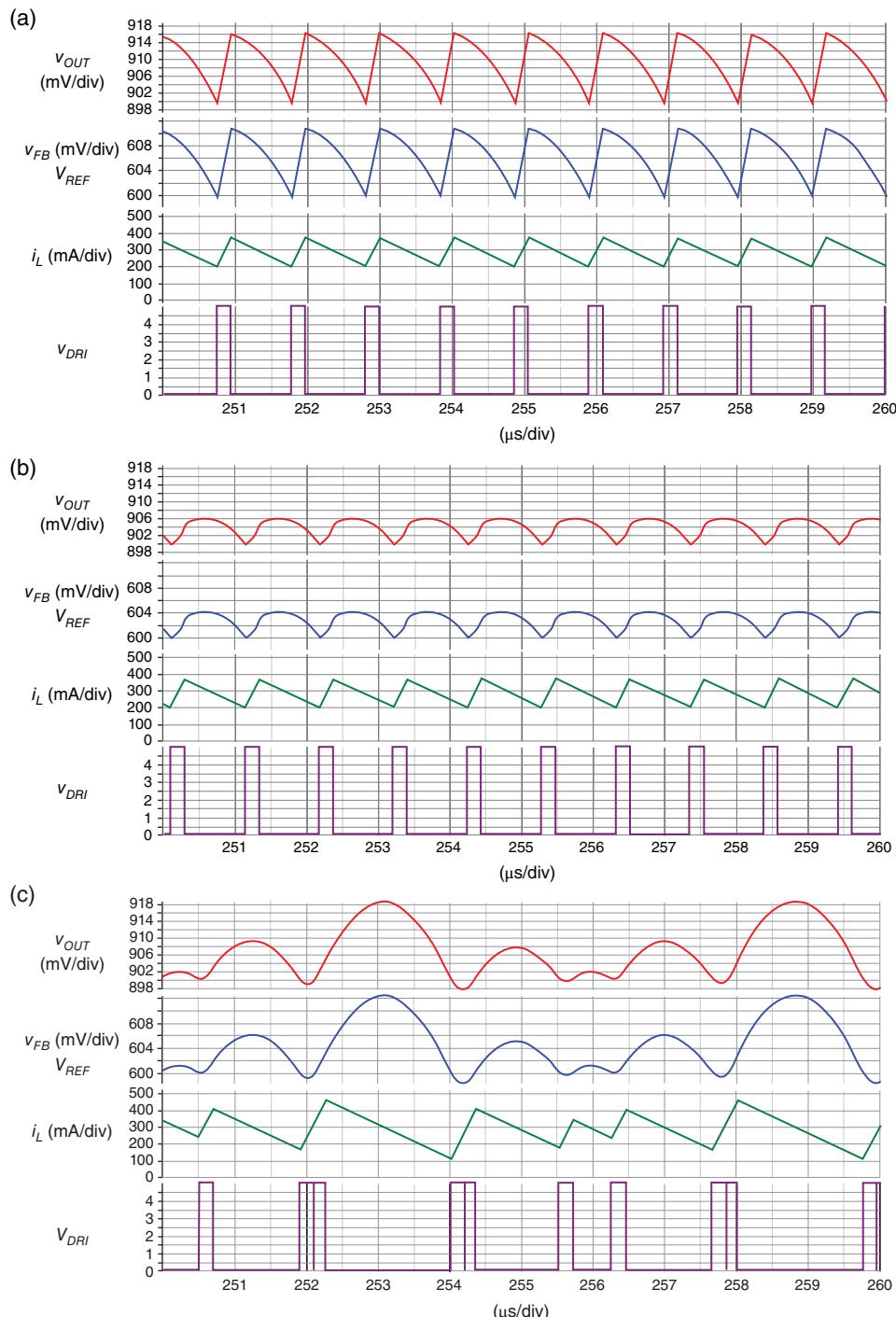
The simulation results with different values of  $R_{ESR}$  (i.e., 100, 28, and 10 m $\Omega$ ) are observed and shown in Figure 4.22(a)–(c), respectively (Table 4.3).

The simulation tool used is SIMPLIS. With an adequate  $R_{ESR}$  value, Figure 4.22(a), (b) shows stable operating waveforms. Moreover,  $v_{OUT}$  is regulated. A comparison of Figure 4.22(a), (b) reveals that the large output ripple,  $v_{OUT,pp}$ , is caused by a large  $R_{ESR}$ . Figure 4.22(a) shows that the  $R_{ESR}$  value of 100 m $\Omega$  results in a  $v_{OUT,pp}$  of approximately 16 mV. Figure 4.22(b) shows that the  $R_{ESR}$  value of 28 m $\Omega$  results in a  $v_{OUT,pp}$  of approximately 6 mV. The valley voltage of  $v_{OUT}$  shown in Figure 4.22(a), (b) is 900 mV in both cases, because  $v_{OUT}$  is monitored using valley voltage control. However, the average of  $v_{OUT}$ ,  $v_{OUT,avg}$ , can be calculated as:

$$v_{OUT,avg} = V_{REF} \cdot \left( \frac{R_1 + R_2}{R_2} \right) + \frac{1}{2} v_{OUT,pp} \quad (4.28)$$

As a result, the  $v_{OUT,avg}$  of 908 mV shown in Figure 4.22(a) has the worse offset voltage compared with the  $v_{OUT,avg}$  of 903 mV shown in Figure 4.22(b). When the voltage accuracy requirement is strict, the inductor, output capacitor, and switching frequency should be carefully designed because  $v_{OUT,pp}$  depends strongly on the ripple of  $i_L$ ,  $C_{OUT}$ , and  $R_{ESR}$ .

In Figure 4.22(c), a small  $R_{ESR}$  of 10 m $\Omega$  does not result in the smallest  $v_{OUT,pp}$  because  $R_{ESR}$  is relatively small to guarantee stable operation. Unstable operation increases the  $v_{OUT,pp}$  and  $\Delta i_L$ . In other words, an unstable  $v_{OUT}$  may result in an unexpected overvoltage to induce over-stress on back-end circuits. In addition, the peak inductor current may be considerably large and damage the components at the output stage.



**Figure 4.22** Simulation results of the on-time controlled DC/DC buck converter in SIMPLIS if  $R_{ESR}$  is (a) 100 mΩ, (b) 28 mΩ, and (c) 10 mΩ

**Table 4.3** Value of  $R_{ESR}$  for three cases

Case	$R_{ESR}$ (mΩ)
(a)	100
(b)	28
(c)	10

### SIMPLIS Setting

Figure 4.23 shows the circuit setup in the circuit simulation software SIMPLIS, which corresponds to that shown in Figure 4.21. The high-side or low-side switch has parallel diodes that form a practical MOSFET.

Figures 4.24 and 4.25 provide zoom-in partial drawings of Figure 4.23. There are four critical devices to be set. Figure 4.26 illustrates the windows for setting parameters.

Figure 4.26(a) is a window to edit the device parameter of the output capacitor, whose value is  $4.7 \mu\text{F}$ . “Level” is set as “2” to activate the value setting of ESR. In different cases, the values of ESR are set as 100, 28, and 10 mΩ.

Figure 4.26(b) is a window to edit the device parameter of the inductor, whose value is  $4.7 \mu\text{H}$ . “Series Resistance” is the  $R_{DCR}$ , set as 0 mΩ.

Figure 4.26(c) is a window to edit the device parameter of the change in loading conditions. First “Wave shape” is selected as “One pulse,” then “Time/Frequency” can be set for the time of load change. In this setting, the loading condition remains at light loads until the time is  $500 \mu\text{s}$ , and then it changes from light to heavy load in  $2 \mu\text{s}$ . In turn, the loading condition remains at heavy loads until the time is  $550 \mu\text{s}$ , and then it changes from heavy to light load in  $2 \mu\text{s}$ . Besides, the value of the load change is set by adjusting the value of “Resistance load” in Figure 4.24.

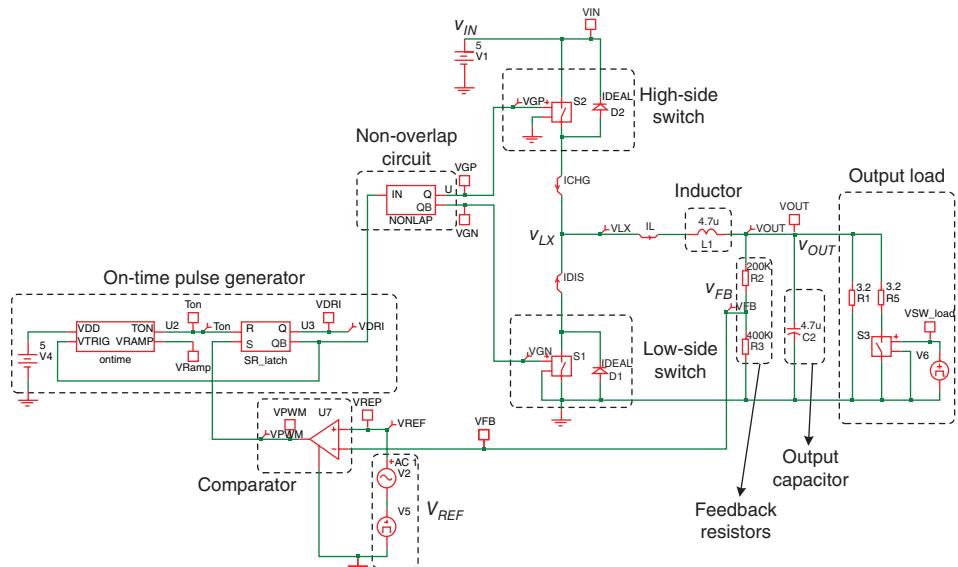
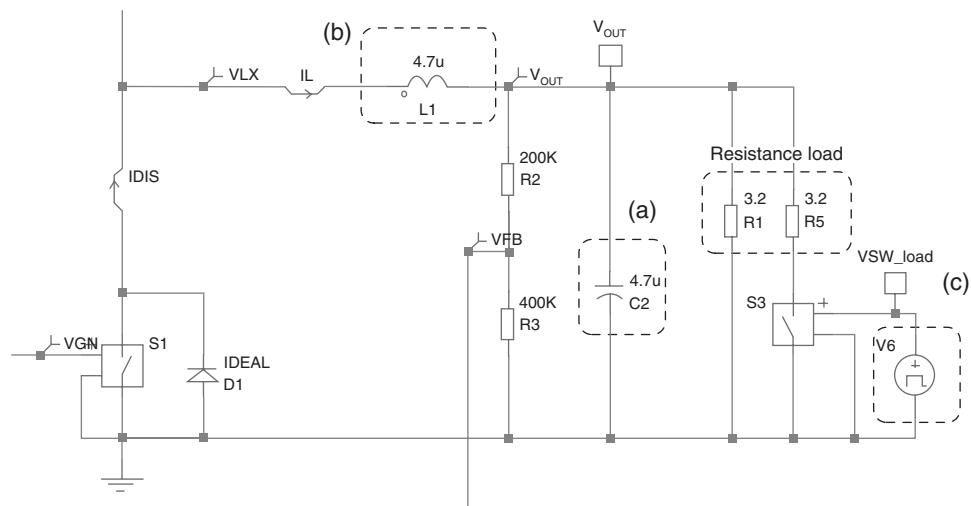
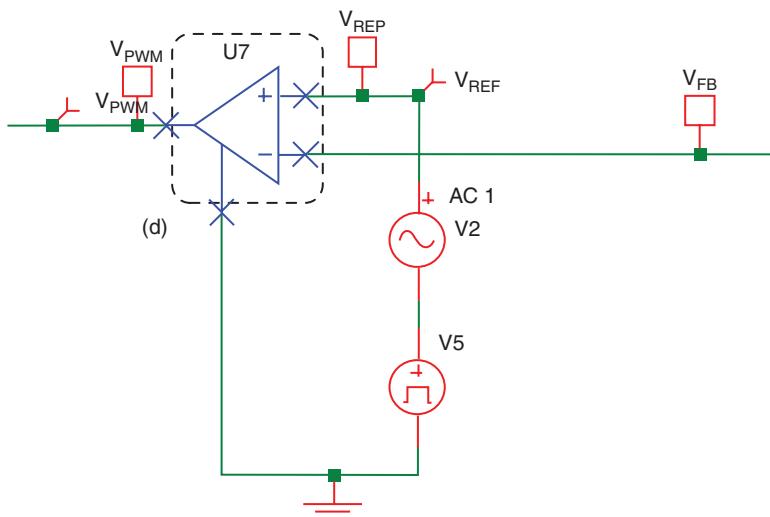


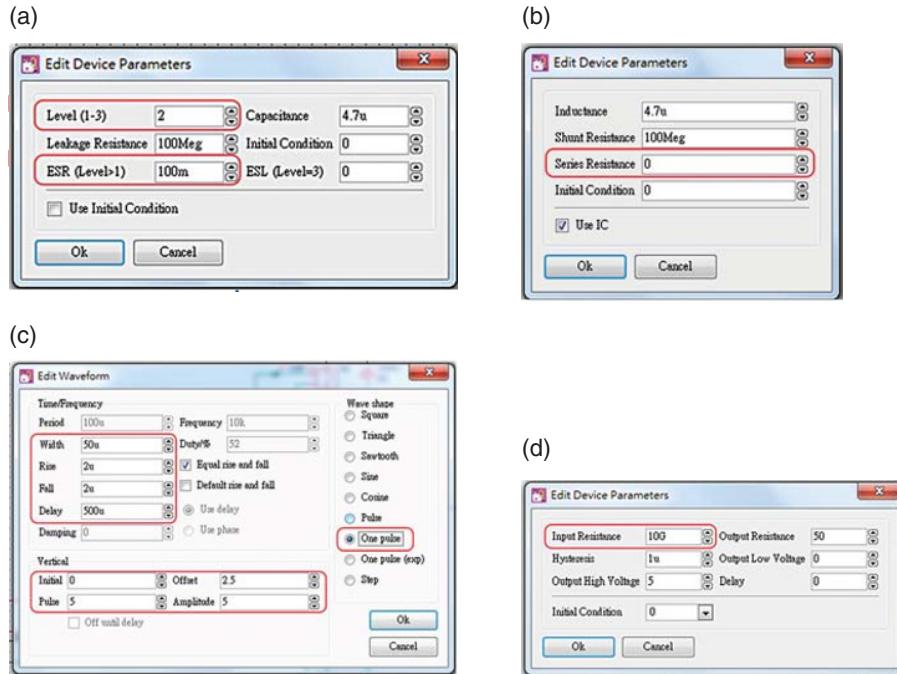
Figure 4.26(d) is a window to edit the device parameter of the comparator in the feedback path. Care should be taken in setting “Input Resistance,” because the value of this resistance has a load effect on the voltage value of  $V_{FB}$  fed from  $V_{OUT}$  through feedback resistance.



**Figure 4.24** Zoom-in drawing of output filter and loading



**Figure 4.25** Zoom-in drawing of feedback path.



**Figure 4.26** Windows for setting device parameters. (a) Output capacitor. (b) Inductor. (c) Output load. (d) Comparator

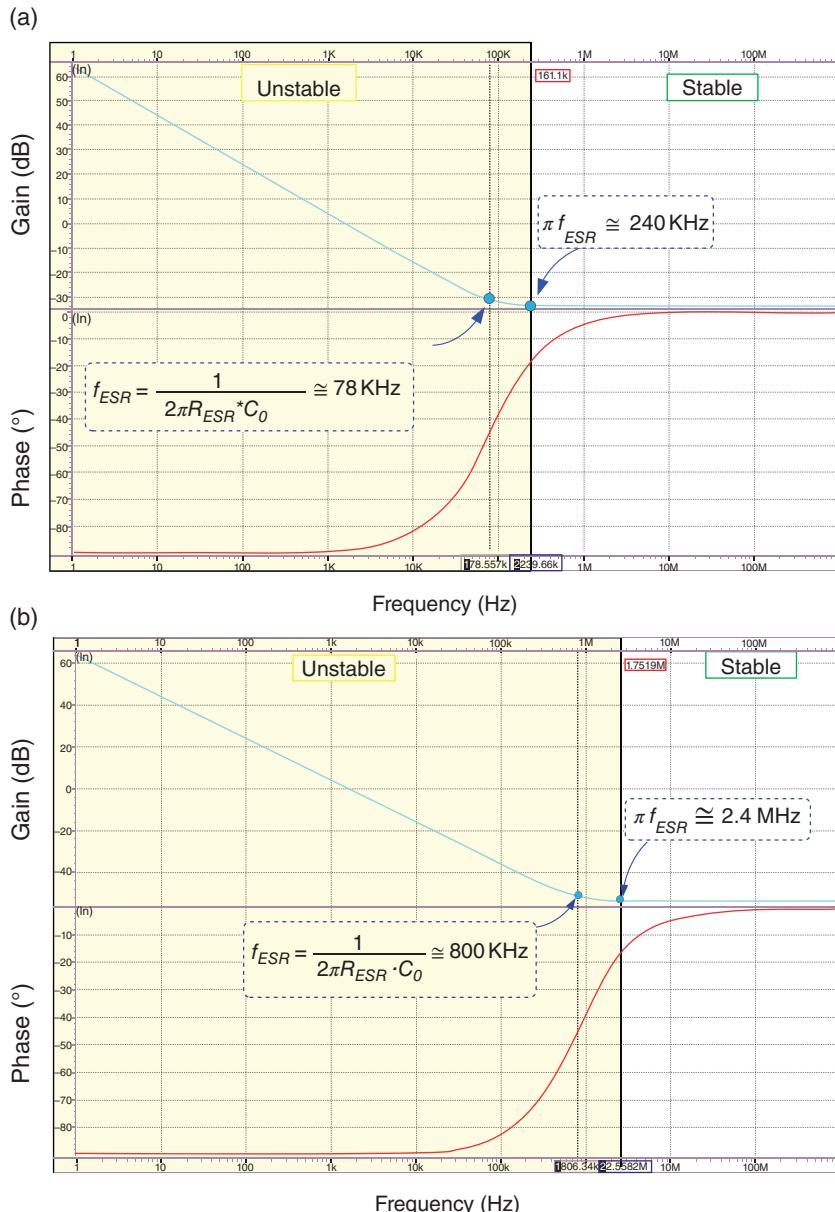
### Example 4.2: Increasing the switching frequency to meet the stability criteria if low $R_{ESR}$ is used

SP-CAP with a value of  $100 \mu\text{F}$  has  $R_{ESR}$  value of  $10 \text{ m}\Omega$ . This finding indicates that  $f_{ESR}$  is approximately  $78 \text{ kHz}$ . Specifically,  $f_{SW}$  should be greater than  $240 \text{ kHz}$  to obtain the maximum phase delay of  $14^\circ$ , as shown in Figure 4.27(a). Selecting the appropriate SP-CAPs to increase the stability of the on-time controlled system is easy, but the cost is high and the magnitude of the output ripple is large. Meanwhile, the  $R_{ESR}$  of the multi-layer ceramic capacitor (MLCC) is only several milliohms when considering the same output capacitor of  $100 \mu\text{F}$ . In Figure 4.27(b), the value of  $R_{ESR}$  is  $2 \text{ m}\Omega$  and the value of  $f_{ESR}$  is approximately  $800 \text{ kHz}$ , resulting in the lowest allowable switching frequency that is close to or even higher than  $2.4 \text{ MHz}$ . However, a high switching operation induces a large switching power loss and a worse jitter problem.

Generally, the MLCC is unsuitable for conventional adaptive on-time controlled methods. Thus, the appropriate output capacitor must be selected to increase system stability.

#### 4.2.2 Selection of Output Capacitor

The switching regulator design must deal with a multi-dimensional trade-off among the input voltage, output voltage, output filter including a capacitor and an inductor, and switching frequency to obtain a regulated output voltage with improved performance. The capacitor has energy storage and voltage ripple filter functions. Thus, the characteristic of the output



**Figure 4.27** Frequency response of the output capacitor. (a) SP-CAP of 100  $\mu\text{F}$  and  $R_{ESR}$  of 10  $\text{m}\Omega$ . (b) MLCC of 100  $\mu\text{F}$  and  $R_{ESR}$  of 2  $\text{m}\Omega$ .

capacitor is one of the factors used to determine the regularity and constancy of the output voltage. For ripple-based control in particular, the characteristics of the output capacitor, including the ideal capacitance, ESR, and ESL values, also determine whether the system is stable. Consequently, correctly selecting a capacitor with suitable properties has a direct influence on converter performance.

**Table 4.4** Characteristics of different capacitor types

	Material	Electrolytic	Voltage stress (V)	Capacity ( $\mu\text{F}$ )
Al capacitor	Aluminum oxide	Polarity	4–400	470–10 000
TA capacitor	Tantalum oxide	Polarity	2.5–50	0.470–1000
Film capacitor	Plastic film	Non-polarity	50–1600	0.001–10
MLCC	Ceramic material	Non-polarity	6.3–250	0.001–100

**Table 4.5** Advantages and disadvantages of different capacitor types

	Advantage	Disadvantage	
Al capacitor	<ul style="list-style-type: none"> <li>• High-voltage stress</li> <li>• Robust capacity over time</li> </ul>	<ul style="list-style-type: none"> <li>• Shortens lifetime when electrolytes are lost</li> <li>• Large volume</li> </ul>	
TA capacitor	<ul style="list-style-type: none"> <li>• Large capacitance</li> <li>• Robust capacity over time</li> </ul>	• Short circuit in failure	
Film capacitor	<ul style="list-style-type: none"> <li>• High-voltage stress</li> </ul>	<ul style="list-style-type: none"> <li>• Small capacitance</li> <li>• Few package options</li> </ul>	
MLCC	<ul style="list-style-type: none"> <li>• Compact size</li> <li>• Good characteristic at high frequencies</li> </ul>	<ul style="list-style-type: none"> <li>• Capacity change over time</li> <li>• Easily broken and collapsed</li> </ul>	

Tables 4.4–4.6 summarize the characteristics of various types of capacitors. Common technology options include an aluminum (Al) capacitor, tantalum (Ta) capacitor, film capacitor, and MLCC. The tables also rank the performance of the technology options according to each characteristic. In the tables, F-C and T-C represent the variation in quality at different frequencies and temperatures, respectively. High-voltage and High-temperature represent the limitation of the highest voltage and temperature, respectively.

Al electrolytic capacitors are devices with anode and cathode polarities. These capacitors are composed of Al plates, aluminum oxide electrolyte, and dielectric. Al electrolytic capacitors can easily achieve large capacitance. Conventional Al electrolytic capacitors use liquid electrolyte, and the quality of the electrolyte can determine the capacity and lifetime. As a result, a high temperature induces the capacitors to lose electrolytes. Capacitance decreases and ESR increases, resulting in the failure of circuits to function. Poor F-C and T-C also make the Al electrolytic capacitors impractical for high-frequency applications.

SP-CAP with solid polymer electrolyte as the specialty polymer electrolyte has been created to resolve this problem. Based on Al electrolytic capacitor technology, the solid type has the advantage of a long lifetime. OS-CAPs use organic semiconductor electrolytes to obtain a similar performance.

**Table 4.6** Different capacitor types

	Capacity	F-C	T-C	High-voltage	High-temperature	Size	Life	Cost	$R_{ESR}$
Al capacitor	Electrolyte	✗✓	✗	✓	○	✓	✗	✓✓	Large
	OS-CAP	✗✓	✓	✗	✗	○	✓	○	Large
	SP-CAP	✗✓	✓	✗	○	○	✓	○	Large
TA capacitor (POS-CAP)	✓	○	✗✓	○	✓	○	✓	✓	Medium
Film capacitor	✗	✗✓	✗✓	✗✓	○	✗	✗✓	○	Small
	✓	✗✓	○	✗✓	✗✓	✓	✗✓	✓	Small

✗, Bad; ○, Fair; ✓, Good; ✗✓, Excellent.

Solid Al electrolytic capacitors have good properties but a high price, and are used extensively in consumer applications. These capacitors are suitable for bypassing low-frequency noise and storing large amounts of energy. When SP-CAPs are applied in SWRs as the output capacitor, a large ESR value will result in a large output ripple and degrade the output voltage quality. Considering this disadvantage, SP-CAPs are rarely used as output capacitor when a power supply of high quality is required. By contrast, for conventional ripple-based control converters, SP-CAPs are a good choice because of their accurate and stable ESR properties.

Ta electrolytic capacitors use tantalum oxide as the electrolyte and have polarity. These capacitors exhibit improved performance at high temperature. As such, the lifetime of Ta electrolytic capacitors is longer than that of liquid Al electrolytic capacitors. Compared with Al electrolytic capacitors, Ta electrolytic capacitors exhibit a more stable capacitance, lower DC leakage, and lower impedance at high frequencies. The ESR value of Ta electrolytic capacitors is lower than that of Al electrolytic capacitors but higher than that of MLCC. Moreover, a small ESR value will result in a short circuit if the capacitance decreases. This short circuit will result in failure of the circuits to function.

Film capacitors are composed of thin plastic films as the dielectric. They have good stability, low inductance, and low ESR value, and are not polarized. As such, film capacitors are suitable for an AC signal. Compared with MLCCs, film capacitors have a significant capacitance within  $\pm 5\%$  of its rated value. These capacitors can withstand voltages in the kilovolt range and high temperature. However, low capacitance and scarce package types are disadvantages that limit the flexibility of utilizing film capacitors.

MLCC is a non-polarity device composed of numerous thin ceramic layers. These capacitors have a compact size and are utilized extensively for switching power converters because of their small ESR and ESL compared with other types. Small parasitic values also imply a reduction in power loss and high performance.

As previously mentioned, the SP-CAP is the most common choice in conventional ripple-based control buck converters because system stability can be guaranteed simply by a large ESR value based on the derived stability criterion. However, a large ESR value results in a large output voltage ripple in steady state and degrades the overshoot/undershoot transient voltage variation during transient response. By contrast, the MLCC has become more attractive because of its low price, compact size, and low ESR value, as listed in Table 4.6. However, a low ESR value cannot provide a substantial time constant value to ensure stability for ripple-based control converters. The stability problem is a significant challenge for the designer in maintaining the superior characteristics of the ripple-based control technique while using MLCC as the output capacitor. In the subsequent section, we will introduce several techniques used to overcome this problem.

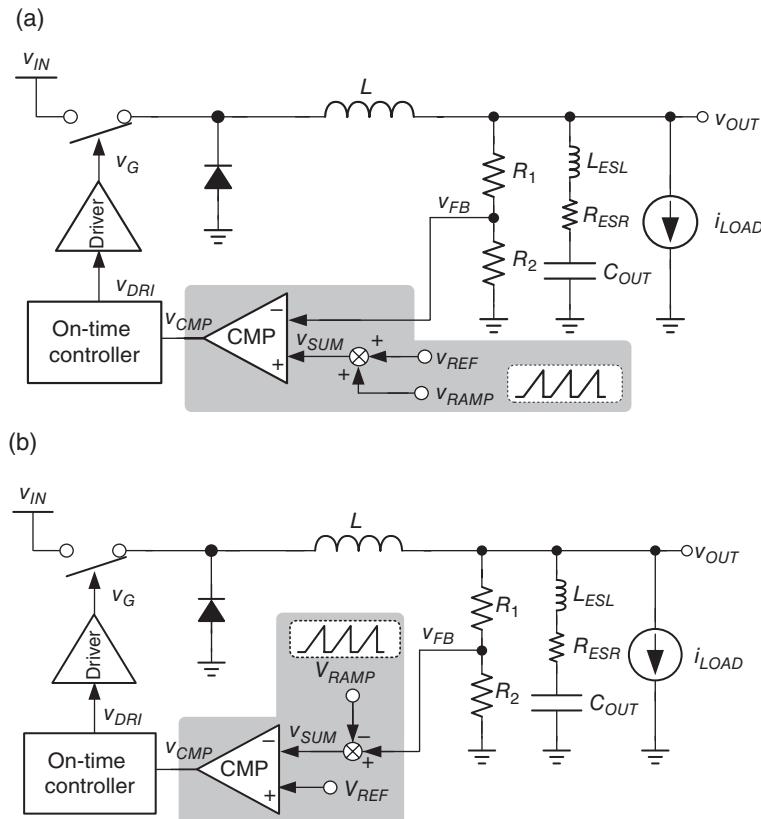
### 4.3 Design Techniques When Using MLCC with a Small Value of $R_{ESR}$

The ESR is a critical factor in determining the stability criterion. In the conventional ripple-based control technique, the value of  $R_{ESR}$  determined by the selection of the output capacitor should be sufficiently large to increase stability. Notable disadvantages are the increase in output voltage ripple in the steady state and the inevitable large undershoot/overshoot voltage that occurs in case of a load transient response. Owing to their inherent large output voltage ripples, conventional ripple-based control DC/DC converters are unsuitable for use in directly

supplying power to sensitive analog circuits. In recent years, facilitating this technique and avoiding the use of large ESRs have become the trend in commercial products. These developed techniques will be discussed in the following.

#### 4.3.1 Use of Additional Ramp Signal

If an additional ramp signal  $v_{Ramp}$  is used to enlarge the noise margin, then the converter with ripple-based control can have the advantage of low output voltage ripple through the use of a cheap ceramic capacitor that has a small  $R_{ESR}$ . The implementation of on-time control shown in Figure 4.28 uses two methods to enlarge the noise margin by the insertion of an external ramp signal.  $v_{OUT}$  is unable to linearly reflect the inductor current ripple if the output capacitor has a low ESR. By contrast, the small output voltage ripple is derived by charging/discharging  $C_{OUT}$ . The difference of the two terminals of the comparator can be enlarged by either adding an extra ramp to  $V_{REF}$ , as shown in Figure 4.28(a), or subtracting an extra ramp from  $V_{FB}$ , as shown in Figure 4.28(b). In other words, the noise margin is enlarged to ensure stability.



**Figure 4.28** On-time control with an extra ramp signal for the use of a capacitor with a small  $R_{ESR}$ : (a) adding  $V_{RAMP}$  to  $V_{REF}$  and (b) subtracting  $V_{RAMP}$  from  $V_{FB}$

Similar to the analysis presented in Section 4.2, Eq. (4.30) is an approximation of the transfer function from the reference voltage to the output expressed as follows:

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{1}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)} \cdot \frac{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)(R_{ESR}C_{COUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)\left(1 + \frac{s}{Q_1\omega_2} + \frac{s^2}{\omega_2^2}\right) + \frac{m_{Slope,r}}{m_{ESR,f}} R_{ESR}C_{COUT}T_{SW} \cdot s^2} \quad (4.29)$$

where

$$\omega_1 = \frac{\pi}{T_{ON}}, \quad Q_1 = \frac{2}{\pi}, \quad \omega_2 = \frac{\pi}{T_{SW}}, \quad Q_2 = \frac{T_{SW}}{\left(R_{ESR}C_{COUT} - \frac{T_{ON}}{2}\right) \cdot \pi} \quad (4.30)$$

In this study,  $m_{Slope,r}$ , the slope of the additional ramp signal, and  $m_{ESR,f}$ , the off-time slope of the output voltage ripple expressed in Eq. (4.31) derived by using the ESR, have the same positive sign:

$$m_{ESR,f} = R_{ESR} \cdot V_{OUT}/L \quad (4.31)$$

When  $T_{ON}$  is sufficiently small, the transfer function in Eq. (4.29) can be simplified as follows:

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{(R_{ESR}C_{COUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_{2r}\omega_2} + \frac{s^2}{\omega_2^2}\right)} \quad (4.32)$$

where

$$Q_{2r} = \frac{T_{SW}}{\left[\left(2\frac{m_{Slope,r}}{m_{ESR,f}} + 1\right)R_{ESR}C_{COUT} - \frac{T_{ON}}{2}\right] \cdot \pi} \quad (4.33)$$

Then the stability criterion is obtained:

$$\left(2\frac{m_{Slope,r}}{m_{ESR,f}} + 1\right)R_{ESR}C_{COUT} > \frac{T_{ON}}{2} \quad (4.34)$$

In other words, the required  $R_{ESR}$  can be obtained:

$$R_{ESR} > \frac{T_{ON}}{2C_{COUT}} \cdot \frac{1}{\left(2\frac{m_{Slope,r}}{m_{ESR,f}} + 1\right)} \quad (4.35)$$

A comparison of Eqs. (4.15) and (4.35) reveals that the additional ramp contributes to the factor of  $m_{Slope,r}$  so that we obtain an equivalent large  $R_{ESR}$  without the need for a physically

large ESR. Consequently the MLCC, even with an ultra-small  $R_{ESR}$ , can be used in on-time control so that the output voltage ripple and the transient voltage variation can be small in the steady state and the transient response simultaneously.

#### 4.3.2 Use of Additional Current Feedback Path

The use of an additional current feedback (CF) path is another practical technique if the ripple-based control uses a ceramic capacitor with a small  $R_{ESR}$ . Figure 4.29 shows the implementation of the on-time control with an additional CF path.  $R_{SEN}$  in Eq. (4.36) represents the converting transfer function from the current signal to the voltage signal. Thus,  $v_{SEN}$  is linearly proportional to the inductor current  $i_{SEN}$ . Then,  $v_{SEN}$  is added to  $v_{FB}$  so that  $v_{SUM}$  with a modified slope can adequately determine the switching operation point from the off-time to the on-time:

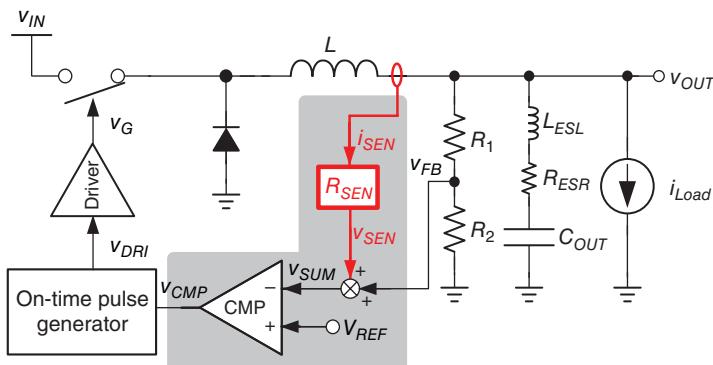
$$R_{SEN} = \frac{v_{SEN}}{i_{SEN}} \quad (4.36)$$

With an additional CF path, the new transfer function from the reference voltage to the output is derived as follows:

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{(R_{ESR}C_{COUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)} \quad (4.37)$$

where

$$\omega_1 = \frac{\pi}{T_{ON}}, \quad Q_1 = \frac{2}{\pi}, \quad \omega_2 = \frac{\pi}{T_{SW}}, \quad Q_{2s} = \frac{T_{SW}}{\left[\left(\frac{R_{SEN}}{R_{ESR}} + 1\right)R_{ESR}C_{COUT} - \frac{T_{ON}}{2}\right] \cdot \pi} \quad (4.38)$$



**Figure 4.29** With an additional CF path, the ripple-based control can use a ceramic capacitor, even with a small  $R_{ESR}$

If  $T_{ON}$  is sufficiently small, then the transfer function can be simplified to a second-order equation:

$$\frac{\hat{v}_{OUT}(s)}{\hat{v}_{REF}(s)} \approx \frac{(R_{ESR}C_{COUT} \cdot s + 1)}{\left(1 + \frac{s}{Q_{2s}\omega_2} + \frac{s^2}{\omega_2^2}\right)} \quad (4.39)$$

Equation (4.41) should be able to remove the unexpected RHP poles; that is,  $Q_{2s}$  is always larger than zero:

$$Q_{2s} = \frac{T_{SW}}{\left[\left(\frac{R_{SEN}}{R_{ESR}} + 1\right)R_{ESR}C_{OUT} - \frac{T_{ON}}{2}\right] \cdot \pi} > 0 \quad (4.40)$$

Therefore, the stability criterion is obtained:

$$\left(\frac{R_{SEN}}{R_{ESR}} + 1\right)R_{ESR}C_{OUT} > \frac{T_{ON}}{2} \quad (4.41)$$

Compared with Eq. (4.14),  $Q_{2s}$  shows that the current signal equivalently increases the value of  $R_{SEN}$  by a factor of  $(R_{SEN}/R_{ESR} + 1)$ . Besides, the criterion in Eq. (4.42) can be extended from Eq. (4.24), and the stability is then easier to guarantee:

$$\left(\frac{R_{SEN}}{R_{ESR}} + 1\right)R_{ESR}C_{OUT} > \frac{T_{ON}}{2} \cdot \frac{V_{IN}}{V_{OUT}} = \frac{1}{2f_{SW}} \quad (4.42)$$

Without the need for a large  $R_{ESR}$ , the additional CF signal releases the stability constraint. Some general implementations of the CF path will be introduced next to discuss the individual characteristics of each implementation.

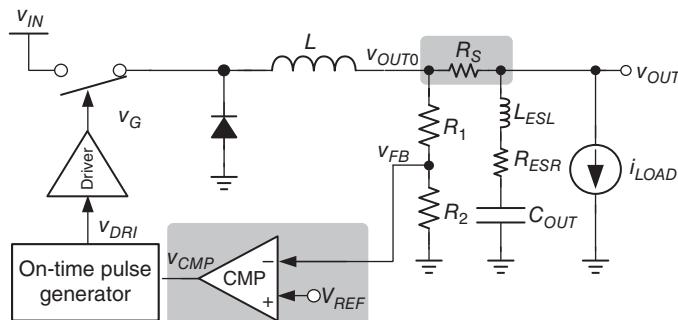
#### 4.3.2.1 CF-type1 (Extra Sensing Resistor)

To sense the inductor current, the sensing resistor  $R_S$  should be directly in series with the inductor, as shown in Figure 4.30. The inductor current can easily be obtained because the sensing resistor is placed on the power delivery path. Through  $R_S$ , the feedback information  $v_{OUT0}$  can be used to obtain the extra inductor current information:

$$v_{OUT0}(t) = v_{OUT}(t) + [i_L(t) \cdot R_S] \quad (4.43)$$

The voltage  $v_S$  across  $R_S$  is composed of information from the output voltage and the inductor current. Thus, the stability criterion can be derived from Eq. (4.14) to obtain:

$$(R_{ESR} + R_S) \cdot C_{OUT} > \frac{T_{ON}}{2} \quad (4.44)$$



**Figure 4.30** Insertion of the sensing resistor  $R_S$  in series can enhance system stability but can also cause extra power loss and voltage droop under different loading conditions

However,  $v_{OUT}$  is excluded from the feedback loop because  $R_S$  is used to obtain the inductor current information. In other words, directly monitoring  $v_{OUT}$  through the feedback loop is unnecessary. By contrast, the feedback loop can only modulate  $v_{OUT0}$  based on the valley voltage control and the reference voltage  $V_{REF}$ . The average value of  $v_{OUT0}$  is expressed in Eq. (4.45) as

$$v_{OUT0,avg} = V_{REF} \cdot \left( \frac{R_1 + R_2}{R_2} \right) + \frac{1}{2} v_{OUT0,pp} \quad (4.45)$$

When Eq. (4.43) is substituted in Eq. (4.45), Eq. (4.46) can reveal the relationship between  $v_{OUT0,avg}$  and  $v_{OUT,avg}$  to determine the deviation caused by different loading conditions. Moreover, the simplified Eq. (4.47) can show the deviation of  $v_{OUT,avg}$  from the expected regulation value:

$$v_{OUT,avg} = v_{OUT0,avg} - \left( i_{L,avg} + \frac{1}{2} i_{L,pp} \right) \cdot R_S + \frac{1}{2} v_{OUT,pp} \quad (4.46)$$

$$v_{OUT,avg} = V_{REF} \cdot \left( \frac{R_1 + R_2}{R_2} \right) - \left( i_{L,avg} + \frac{1}{2} i_{L,pp} \right) \cdot R_S + \frac{1}{2} v_{OUT,pp} \quad (4.47)$$

Although easy to generate, the additional sensing resistor  $R_S$  in series causes the system to suffer from the disadvantages of extra power loss and voltage droop under different loading conditions. These disadvantages are undesired in recent portable electronics.

### Example 4.3: Insertion of $R_S$ to add more inductor current information

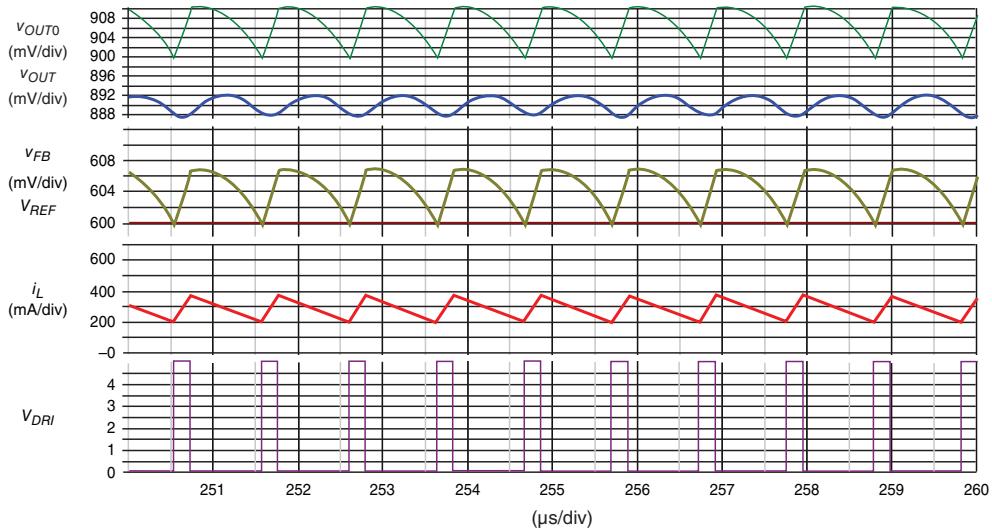
Figure 4.30 shows the basic structure of an on-time control DC/DC buck converter. Table 4.7 lists the basic specifications. The other parameters are set as follows:  $R_1 = 200 \text{ k}\Omega$  and  $R_2 = 400 \text{ k}\Omega$ .

Given the negative feedback loop, the system is sufficiently stable to obtain the expected  $V_{OUT}$  of 900 mV when  $f_{sw}$  is 1 MHz and the duty ratio is 0.18. Simulation results with different values of  $R_S$ , 60 and 20 mΩ, are observed, as shown in Figure 4.31(a), (b), respectively. The simulation results are also obtained by using the simulation tool SIMPLIS.

**Table 4.7** Basic specifications used in Example 4.3

$V_{IN}$	$V_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	900 mV	600 mV	4.7 $\mu$ H	0 m $\Omega$	4.7 $\mu$ F	0 m $\Omega$	0 nH	180 ns	1 MHz

(a)



(b)

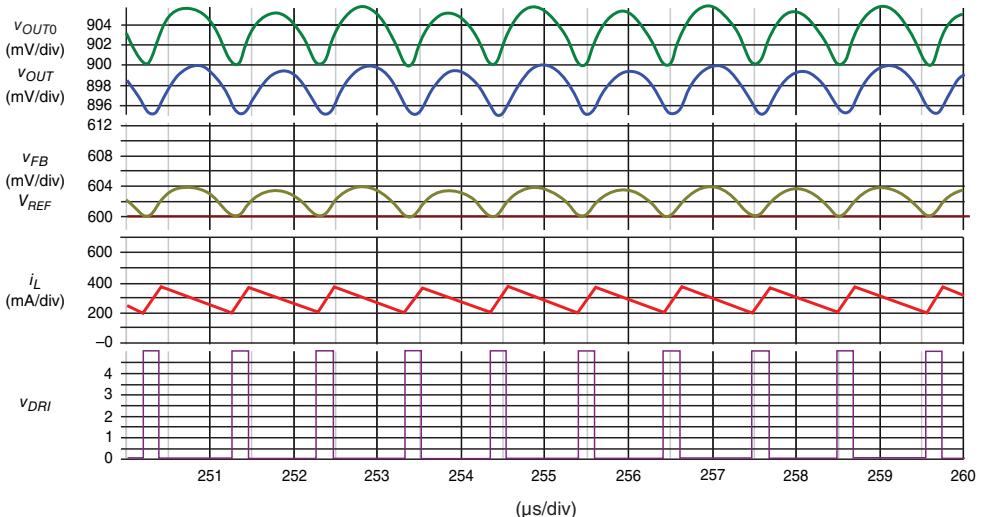
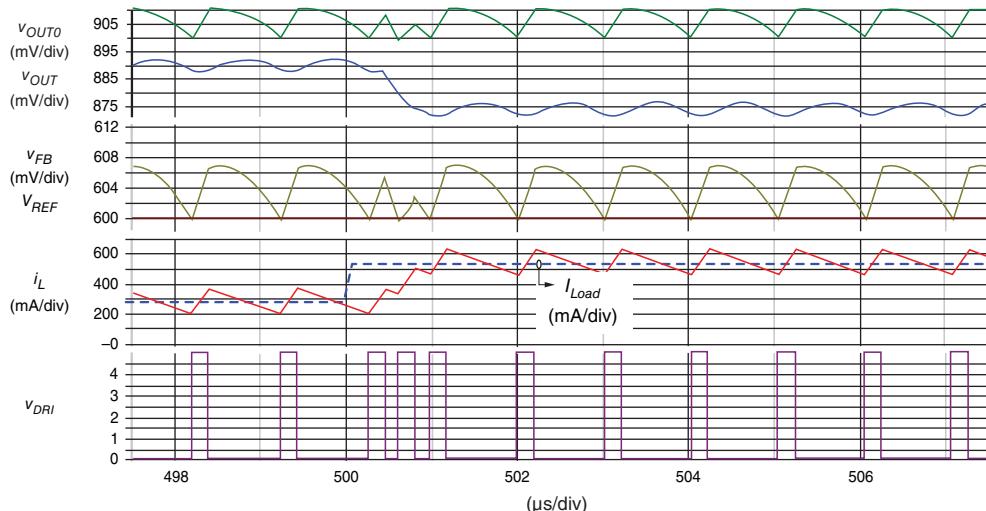
**Figure 4.31** Simulation results obtained using SIMPLIS when the on-time controlled DC/DC buck converter uses different values of sensing resistor  $R_s$ : (a) 60 m $\Omega$  and (b) 20 m $\Omega$

Figure 4.31(a) shows stable operating waveforms with an adequate  $R_{ESR}$  of 60 mΩ. Moreover,  $v_{OUT}$  is well regulated. The waveform of  $v_{OUT}$  with  $R_{ESR} = 0$  mΩ clearly contributes little linear information to  $i_L$ . Through  $R_S$ , the waveform of  $v_{OUT0}$  contributes additional information to  $i_L$ . The linearity between  $v_{OUT0}$  and  $i_L$  is also increased, which validates the result derived using Eq. (4.43). Through  $R_1$  and  $R_2$ , the feedback loop can regulate  $v_{OUT0}$  and provide a stable  $v_{OUT}$ . The waveforms also reveal that  $R_S$  results in a deviation voltage of -12 mV between  $v_{OUT0}$  and  $v_{OUT}$ , an outcome that proves the result derived using Eq. (4.48). In Figure 4.31(b), the small  $R_S$  of 20 mΩ is used. The deviation voltage between  $v_{OUT0}$  and  $v_{OUT}$  is reduced to -4 mV compared with the value of -12 mV in the case of  $R_S = 60$  mΩ. Additionally, the waveforms reveal that  $R_{ESR} = 20$  mΩ is relatively small to ensure system stability. Thus,  $v_{OUT}$  is slightly unstable (Table 4.8).

Figure 4.32 shows a transient response in case of  $R_S = 60$  mΩ when the load changes from 280 to 560 mA at a time of 500 μs. Evidently, the deviation voltage between  $v_{OUT}$  and  $v_{OUT0}$  is different. By comparing the deviation voltage at  $I_{Load} = 280$  and 560 mA, the deviation voltage increases because  $i_{L,avg}$  increases. Moreover,  $v_{OUT0}$  is still well regulated and its valley is 900 mV even under different loading conditions. This phenomenon can also be expected when calculating Eq. (4.47). In other words,  $v_{OUT}$  exhibits a voltage droop that is strongly dependent on the value of  $R_S$  and  $i_{Load}$ . When high voltage accuracy is required, the structure shown in Figure 4.30 may not be a suitable method.

**Table 4.8** Design parameters of two cases

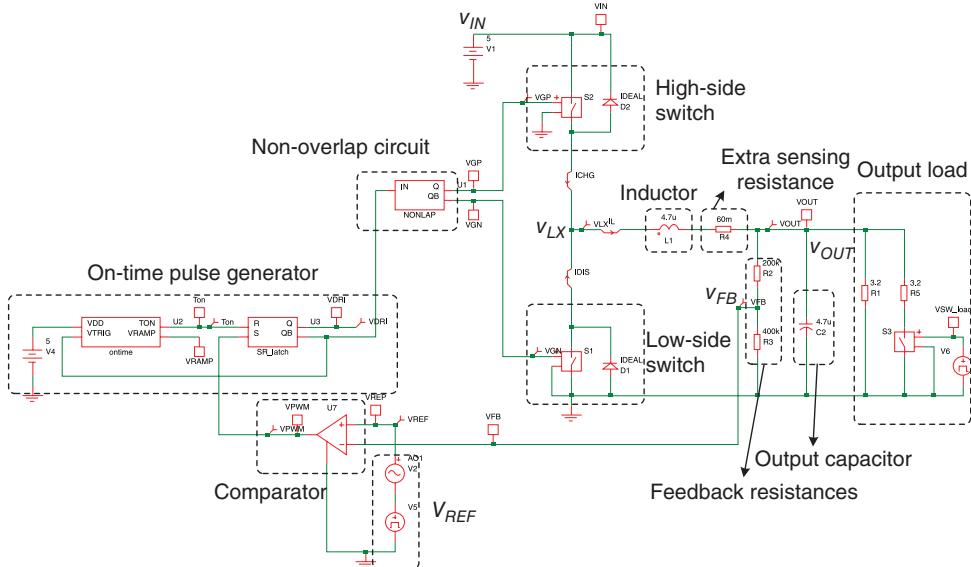
Case	$L$	$R_{DCR}$	$L_{ESL}$	$R_{ESR}$	$C_{OUT}$	$R_S$ (mΩ)
(a)	4.7 μH	0 mΩ	0 nH	0 mΩ	4.7 μF	60
(b)						20



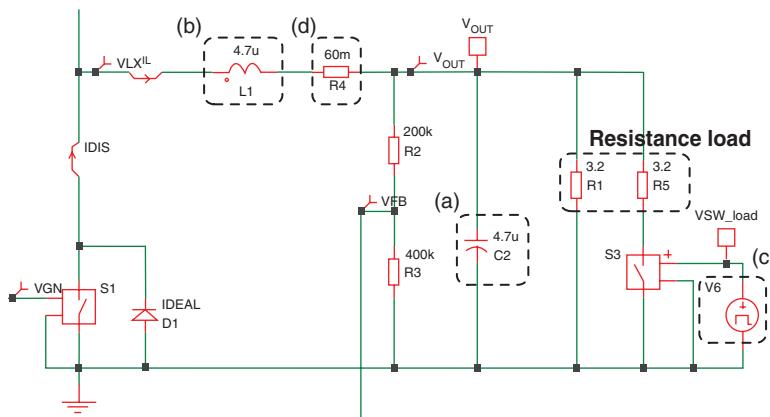
**Figure 4.32** Transient response of the on-time controlled DC/DC buck converter if  $R_S = 60$  mΩ when the load changes from 280 to 560 mA

### SIMPLIS Setting

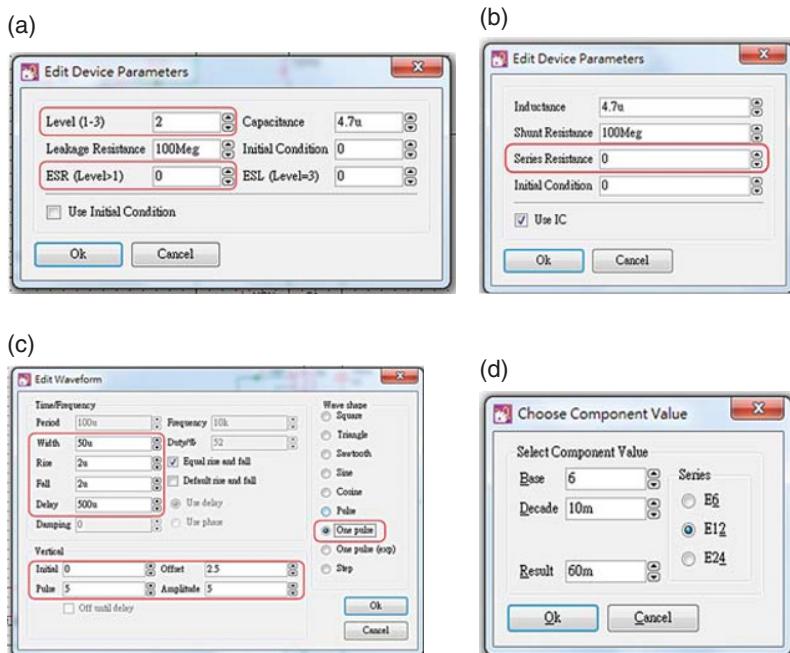
Figure 4.33 shows the setup circuit in the SIMPLIS simulation corresponding to Figure 4.30. Each high-side or low-side switch is placed parallel with a diode to form an equivalent MOSFET device. Besides, Figure 4.34 provides a zoomed-in view of the partial portion of Figure 4.33. The values of four critical devices should be decided to see the differentiation of the performance, where Figure 4.35 illustrates the setting windows for these parameters.



**Figure 4.33** Setup circuit in SIMPLIS



**Figure 4.34** Zoom-in views of output filter and loading



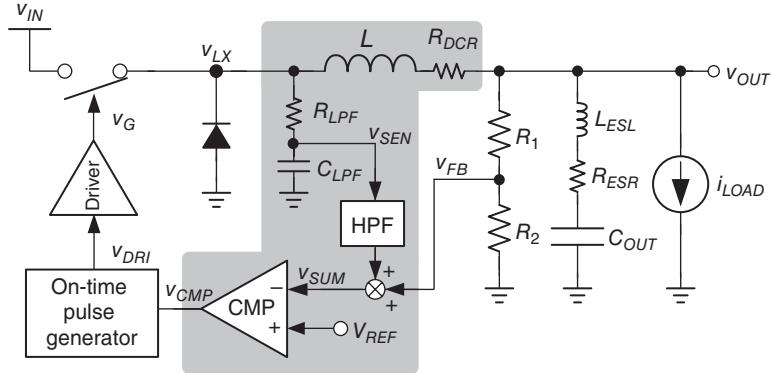
**Figure 4.35** Windows for setting device parameters. (a) Output capacitor. (b) Inductor. (c) Output load. (d) Extra sensing resistance in series with the inductor

Figure 4.35(a) is a window to edit the device parameter of the output capacitor, whose value is  $4.7 \mu\text{F}$ . “Level” is set as “2” to activate the value setting of ESR. However, to demonstrate the function of extra sensing resistance, the value of ESR is  $0 \text{ m}\Omega$  now. Figure 4.35(b) is a window to edit the device parameter of the inductor, whose value is  $4.7 \mu\text{H}$ . “Series Resistance” is the  $R_{DCR}$ , set as  $0 \text{ m}\Omega$ . Figure 4.35(c) is a window to edit the device parameter of the change in loading conditions. “Wave shape” is first selected as “One pulse,” then “Time/Frequency” can be set for the time of load change. In this setting, the loading condition remains at light loads until the time is  $500 \mu\text{s}$ , and then changes from light to heavy load in  $2 \mu\text{s}$ . In turn, the loading condition remains at heavy loads until the time is  $550 \mu\text{s}$ , and then changes from heavy to light load in  $2 \mu\text{s}$ . Besides, the value of the load change is set by adjusting the value of “Resistance load” in Figure 4.34. Figure 4.35(d) is a window to edit the device parameter of extra sensing resistance in series with the inductor. Its value is set at  $60$  and  $20 \text{ m}\Omega$  in Example 4.3.

#### 4.3.2.2 CF-type2 (Integral RC-Filter)

In Figure 4.36,  $R_{LPF}$  and  $C_{LPF}$  with a time constant of  $\tau_{LPF}$  in Eq. (4.49) act as a low-pass filter (LPF) to integrate the signal variation at  $v_{LX}$ , which is the node between the high-side and low-side switches. Thus, on-time and off-time can denote the value of  $v_{IN}$  and ground, respectively, by monitoring  $v_{LX}$ :

$$\tau_{LPF} = R_{LPF} \cdot C_{LPF} \quad (4.48)$$



**Figure 4.36** LPF composed of  $R_{LPF}$  and  $C_{LPF}$  with a time constant of  $\tau_{LPF}$  integrating the signal variation at  $v_{LX}$

The slope of  $v_{SEN}$  during the on-time and off-time periods,  $m_{SEN,r}$  and  $m_{SEN,f}$ , can be expressed in Eqs. (4.49) and (4.50), respectively, when  $\tau_{LPF}$  is larger than the switching period:

$$m_{SEN,r} = \frac{v_{IN} - v_{OUT}}{\tau_{LPF}} \quad (4.49)$$

$$m_{SEN,f} = \frac{-v_{OUT}}{\tau_{LPF}} \quad (4.50)$$

The average model is used to derive the DC value of  $v_{SEN}$ . In the steady state, the average current through  $R_{LPF}$  is zero. The average value of  $v_{LX}$  can be expressed in Eq. (4.51), where the complex value  $D$  is assumed constant to simplify the analysis:

$$v_{LX,avg} = v_{IN} \cdot D \quad (4.51)$$

Considering the average model, the inductor can be viewed as shorted. The DC voltage (or average value) of  $v_{SEN}$  can be derived using Eq. (4.52), where  $i_{L,avg}$  is the average inductor current:

$$v_{SEN,avg} = v_{OUT,avg} - i_{L,avg} \cdot R_L \quad (4.52)$$

In Eqs. (4.49), (4.50), and (4.52),  $v_{SEN}(t)$  represents information from the inductor current. In other words,  $v_{SEN}(t)$  consists of the DC and AC information from the inductor current. When adding  $v_{SEN}(t)$  to the feedback path to enhance stability, a high-pass filter (HPF) is needed to transmit the AC information from  $v_{SEN}(t)$  so that the DC information from  $v_{SEN}(t)$  will not worsen the accuracy of the  $v_{OUT}$  regulation. One approach that can provide a simple method

to summarize  $v_{FB}$  and  $v_{SEN}$  is to short these two nodes directly. The design complexity is significantly reduced without the use of any mixing circuits. However, the phase delay characteristic between  $v_{FB}$  and  $v_{SEN}$  degrades the transient response. The accuracy of  $v_{OUT}$  regulation will also be deteriorated.

#### 4.3.2.3 CF-type3 (Parallel RC-Filter)

In Figure 4.36, based on the integral function of the filters of  $C_{LPF}$  and  $R_{LPF}$ , the current-sensing information,  $v_{SEN}$ , has a phase delay corresponding to the actual inductor current information,  $i_L$ . Therefore, the load transient response is restricted because the output voltage variation cannot effectively be reflected back to the controller. In Figure 4.37, the filter of  $R_S$  and  $C_S$ , which is placed parallel to the inductor  $L$ , can have a similar inductor current-sensing effect. Transient results have a slight difference.

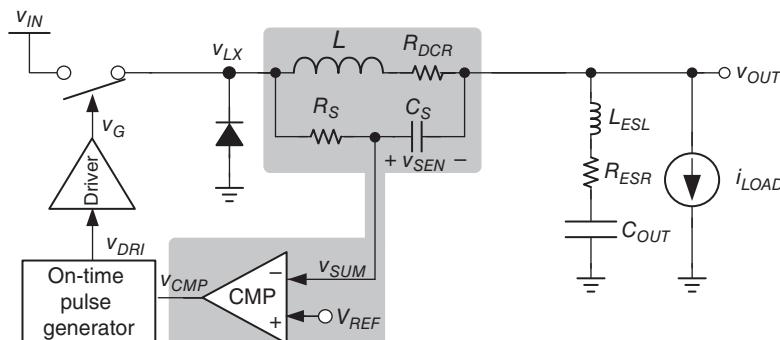
In this study, the parasitic DCR of the inductor,  $R_{DCR}$ , is utilized to sense the inductor current. No extra power loss occurs when no sensing resistor is used on the energy delivery path. The sensing pair of  $R_S$  and  $C_S$  is placed parallel with  $L$  and  $R_{DCR}$  to sense the current flowing through  $R_{DCR}$ . The voltage across  $C_S$  can be derived using

$$v_{SEN}(s) = \frac{i_L \cdot (R_{DCR} + sL)}{1 + sR_S C_S} = (i_L \cdot R_{DCR}) \cdot \left[ \frac{1 + s(L/R_{DCR})}{1 + sR_S C_S} \right] \quad (4.53)$$

The DC term (i.e.,  $s = 0$ ) in Eq. (4.53) implies that the sensing result can be derived simply by using the  $R_{DCR}$  of the inductor. However, the frequency-dependent term, including one pole/zero pair, will influence the linearity of inductor current sensing. If the time constant values of  $L/R_{DCR}$  and  $R_S C_S$  are equal, as shown in Eq. (4.54), then the voltage  $v_{SEN}$  across the capacitor  $C_S$  can be completely proportional to the inductor current  $i_L$ :

$$L/R_{DCR} = R_S C_S \quad (4.54)$$

The derived current-sensing signal can be independent of frequency without being affected by any time constant values from the inductor or sensing network. The values of  $L$  and  $R_{DCR}$



**Figure 4.37** Parallel-sensing technique can enhance the sensing signal

should be known in advance to design the sensing network composed of  $R_S$  and  $C_S$  appropriately. A disadvantage of this method is the limited design flexibility. Another compromise method is to adjust the external resistor  $R_S$  value to ensure design flexibility.

During the on-time and off-time periods,  $v_{LX}$  is shortened to  $v_{IN}$  and ground, respectively. When charging and discharging the capacitor  $C_S$  during the on-time and off-time periods, respectively, the rising slope  $m_{SEN,r}$  and the falling slope  $m_{SEN,f}$  during the on-time and off-time periods can be expressed in Eqs. (4.55) and (4.56):

$$m_{SEN,r} = \frac{v_{IN} - v_{OUT}}{\tau_{SEN}} \quad (4.55)$$

$$m_{SEN,f} = \frac{-v_{OUT}}{\tau_{SEN}} \quad (4.56)$$

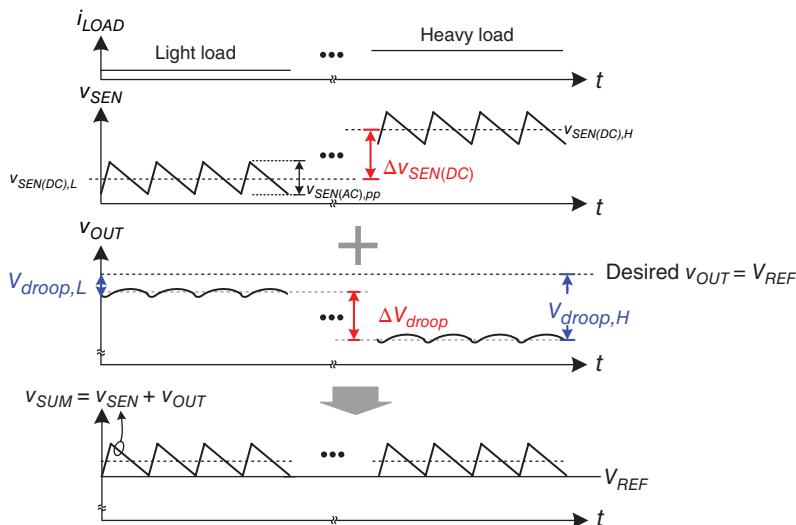
In this study, the switch on-resistance is assumed to be sufficiently small to be ignored, and the time constant  $\tau_{SEN}$  is equal to the product of  $R_S$  and  $C_S$ :

$$\tau_{SEN} = R_S \cdot C_S \quad (4.57)$$

$v_{SUM}(t)$  can be derived using Eq. (4.58) to show that the amount of current ripple is effectively increased to improve system stability:

$$v_{SUM}(t) = v_{OUT}(t) + v_{SEN}(t) \quad (4.58)$$

However, the DC value of the sensed inductor current is also included. A disadvantage of the DC value of  $v_{SUM}$  is that it depends on the loading current conditions. Thus, this approach still suffers from voltage droop. Figure 4.38 shows the operating waveforms to explain the offset



**Figure 4.38**  $v_{OUT}$  of voltage droop and offset voltage under different loading conditions

voltage and the voltage droop at  $v_{OUT}$  under different loading conditions. Owing to the valley control, the valley of  $v_{SEN}$  is regulated at  $V_{REF}$ . Based on Eq. (4.58), the DC values of  $v_{OUT}$  and  $v_{OUT(DC)}$  can be derived using Eq. (4.59).  $V_{droop}$  and  $v_{offset}$  in Eqs. (4.60) and (4.61) represent the voltage droop and the offset voltage, respectively. Notably,  $V_{droop}$  includes only  $v_{SEN(DC)}$ , whereas  $v_{offset}$  includes  $v_{OUT(AC),pp}$  and  $v_{SEN(AC),pp}$ , which represent the peak-to-peak voltages of  $v_{OUT(AC)}$  and  $v_{SEN(AC)}$ , respectively.

$$v_{OUT(DC)} = V_{REF} + V_{droop} + V_{offset} \quad (4.59)$$

$$V_{droop} = \frac{1}{2} v_{SEN(DC)} \quad (4.60)$$

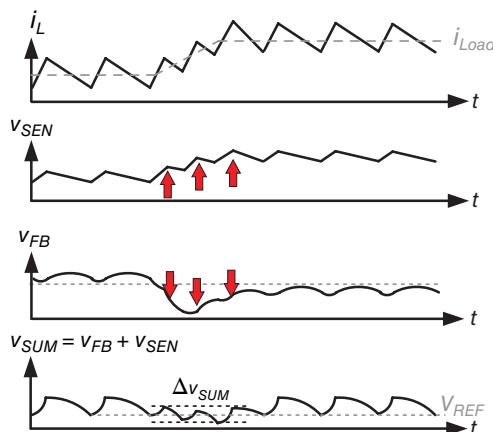
$$v_{offset} = \frac{1}{2} v_{SEN(AC),pp} + \frac{1}{2} v_{OUT(AC),pp} \quad (4.61)$$

When MLCC is used for a small ripple, the small value of  $v_{OUT(AC),pp}$  can be ignored. Thus, Eq. (4.61) is simplified as follows:

$$v_{offset} \approx \frac{1}{2} v_{SEN(AC),pp} \quad (4.62)$$

However,  $R_{SEN}$  should be sufficiently large to meet the inequality requirement in Eq. (4.41), which indicates that  $v_{SEN}$  is large. Moreover, the load-dependent voltage droop  $V_{droop}$  at  $v_{OUT}$  is caused by  $v_{SEN}$  under different loading conditions. By considering the regulation of  $v_{OUT(DC)}$ , Eq. (4.59) shows that  $v_{SEN(AC),pp}$  results in a large offset voltage at  $v_{OUT}$ . Significantly, the change in  $v_{SEN(DC)}$  under different loading conditions influences the value of  $V_{droop}$  at  $v_{OUT}$ .

In case of the load transient response shown in Figure 4.39, the larger  $v_{SEN(AC)}$  is, the smaller  $\Delta v_{SUM}$  will be because the trend of  $v_{SEN}$  is opposite to that of  $v_{OUT}$ . Meanwhile, the on-time period becomes smaller than that in the steady state. Although the approach uses an additional CF path to stabilize the system, the performance of load regulation and transient response deteriorates.

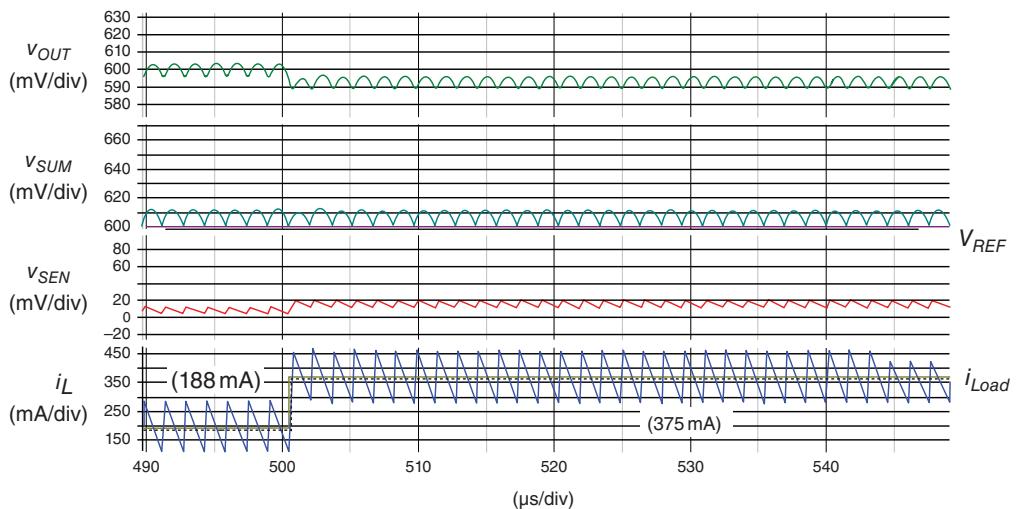


**Figure 4.39** Deterioration of load transient response because of the additional CF path

**Example 4.4:** The DC value is seriously affected by the additional current-sensing value  $v_{SEN}$ ; besides, the contribution of the additional sensing should be sufficiently large if we observe the change in  $C_s$

Figure 4.40 shows the load transient response from 188 to 375 mA derived using the simulation tool SIMPLIS. The basic specifications are listed in Table 4.9. Based on Eq. (4.58),  $v_{OUT}$  is regulated at approximately 600 mV. The DC value of  $v_{SEN}$  increases when  $i_{Load}$  increases. Evidently,  $v_{OUT(DC)}$  is influenced by  $v_{SEN}$ .

In this study, different characteristics are observed by monitoring different amplitudes of  $v_{SEN}$  if the size of  $C_s$  is changed but the same  $R_s$  value is kept. After using five values of  $C_s$ , Table 4.10 lists the critical parameters and Figure 4.41 shows the corresponding operating waveforms.



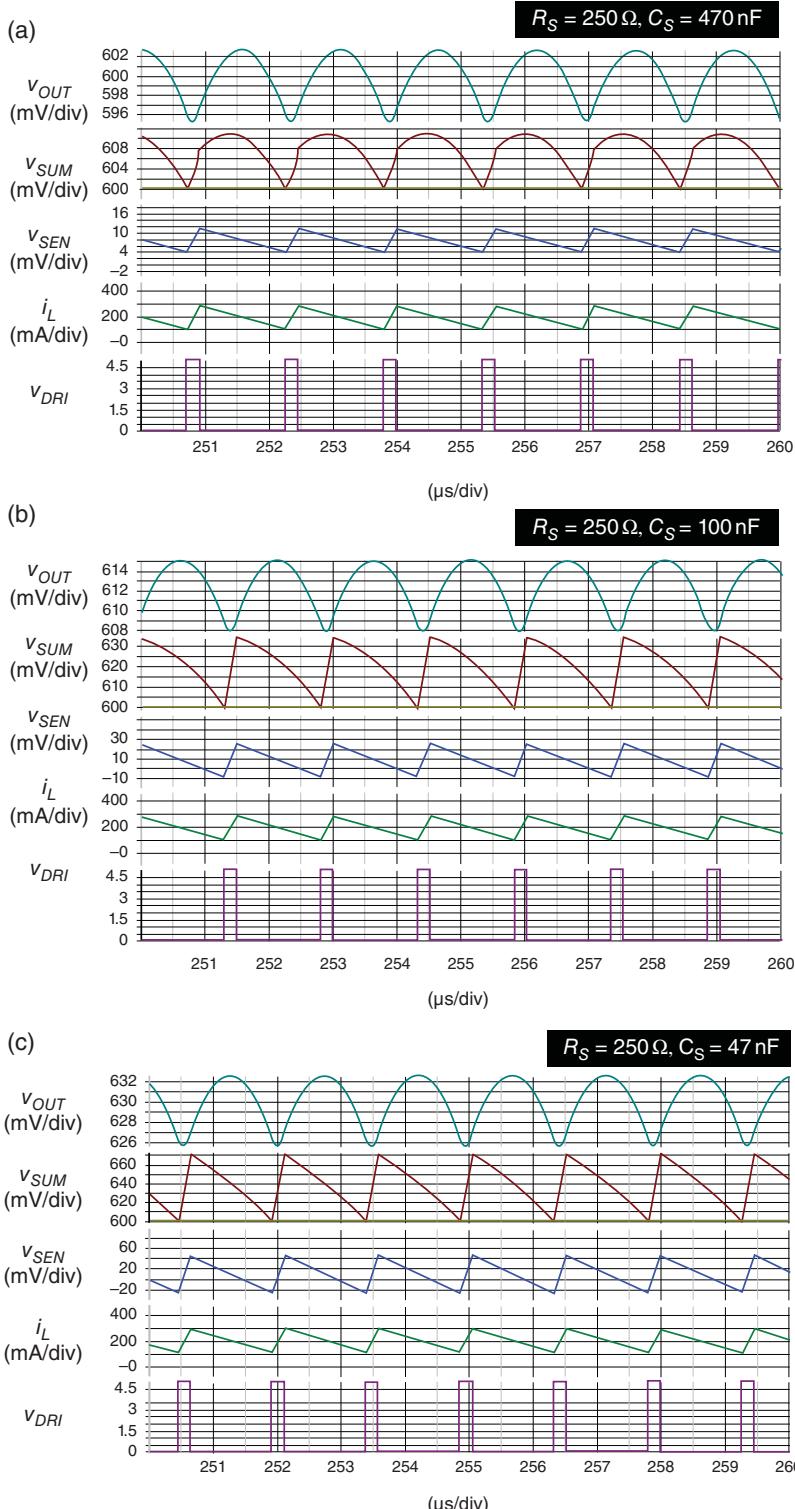
**Figure 4.40** Load transient response

**Table 4.9** Basic specifications used in Example 4.4

$V_{IN}$	$V_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu$ H	40 m $\Omega$	4.7 $\mu$ F	0 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.10** Designing parameters for five cases

Case	$L$	$R_{DCR}$	$L_{ESL}$	$R_{ESR}$	$C_{OUT}$	$R_s$	$C_s$
(a)	4.7 $\mu$ H	40 m $\Omega$	0 nH	0 m $\Omega$	4.7 $\mu$ F	250 $\Omega$	470 nF
(b)							100 nF
(c)							47 nF
(d)							1.0 $\mu$ F
(e)							4.7 $\mu$ F



**Figure 4.41** External components include  $L = 4.7 \mu\text{H}$ ,  $R_{DCR} = 40 \text{ m}\Omega$ ,  $L_{ESL} = 0 \text{ nH}$ ,  $R_{ESR} = 0 \text{ m}\Omega$ , and  $C_{OUT} = 4.7 \mu\text{F}$ . (a)  $R_S = 250 \Omega$  and  $C_S = 470 \text{ nF}$ . (b)  $R_S = 250 \Omega$  and  $C_S = 100 \text{ nF}$ . (c)  $R_S = 250 \Omega$  and  $C_S = 47 \text{ nF}$ . (d)  $R_S = 250 \Omega$  and  $C_S = 1.0 \mu\text{F}$ . (e)  $R_S = 250 \Omega$  and  $C_S = 4.7 \mu\text{F}$

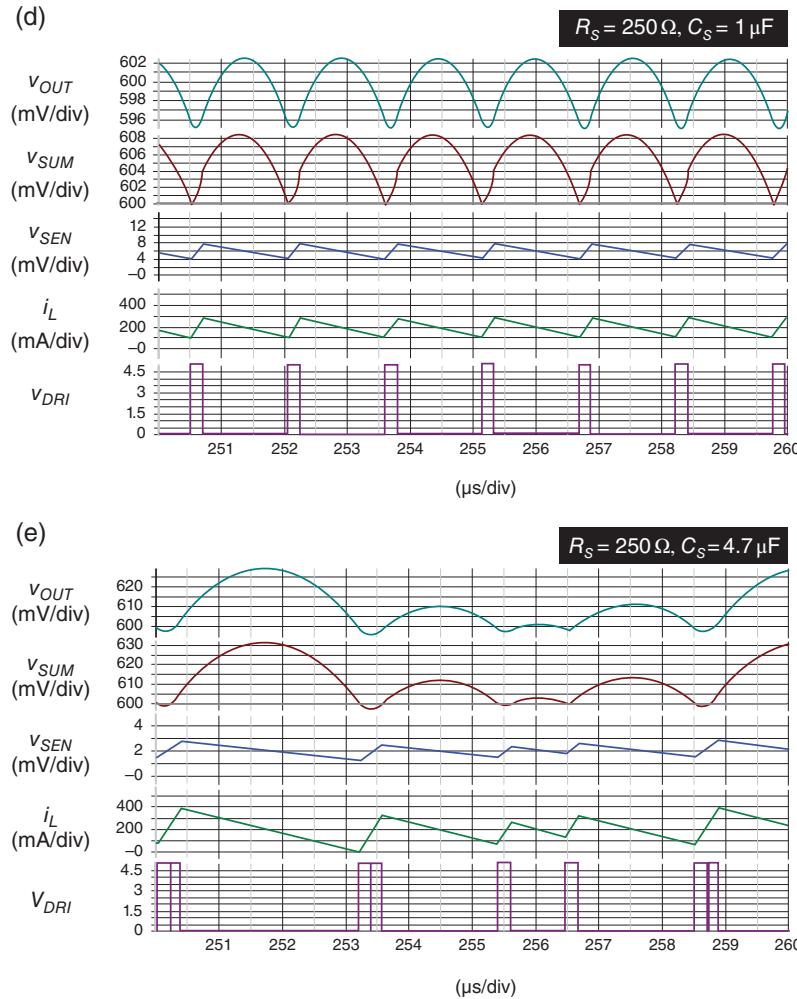


Figure 4.41 (Continued)

In Figure 4.41(a),  $R_S$  and  $C_S$  are  $250 \Omega$  and  $470 \text{ nF}$ , respectively, as determined using Eq. (4.54). Thus,  $v_{SEN}$  is proportional to  $i_L$ , and  $v_{FB}$  is composed of information from  $v_{OUT}$  and  $i_L$ . As a result, stability is guaranteed although  $R_{ESR}$  is zero. The valley of  $v_{SUM}$  is  $600 \text{ mV}$  because the two inputs of the comparator in the feedback loop are  $V_{REF}$  and  $v_{SUM}$ . However, the valley of  $v_{OUT}$  is equal to  $600 \text{ mV} - v_{SEN(AC),pp} - v_{SEN(DC)}$ . In other words, the average value of  $v_{OUT}$  varies with different values of  $V_{REF}$  and  $v_{SEN(AC),pp}$ . Based on Eqs. (4.56) and (4.57), the time constant  $\tau_{SEN}$  can determine  $v_{SEN(AC),pp}$ :

$$v_{SEN(AC),pp} = T_{ON} \cdot m_{SEN,r} = T_{ON} \cdot \left( \frac{V_{IN} - v_{OUT}}{\tau_{SEN}} \right) \quad (4.63)$$

Decreasing  $C_S$  causes a different value of  $v_{SEN(AC),pp}$ , which is the offset voltage at  $v_{OUT}$ . In Figure 4.41(b),  $\tau_{SEN}$  is smaller than that in Figure 4.41(a) if the value of  $C_S$  decreases to  $100 \text{ nF}$ .

$v_{SEN(AC),pp}$  is 8 mV in Figure 4.41(a), whereas  $v_{SEN(AC),pp}$  is 37.6 mV in Figure 4.41(b). Comparison of Figure 4.41(a) and (b) reveals that the value of  $v_{SEN(AC),pp}$  is proportional to the value of  $C_S$ .

Furthermore,  $v_{SEN(AC),pp}$  is 80 mV in Figure 4.41(c) because  $\tau_{SEN}$  becomes smaller than its original value when  $R_S$  is 250  $\Omega$  and  $C_S$  is 47 nF. A larger  $v_{SEN(AC),pp}$  results in a  $v_{FB}$  that is more proportional to  $i_L$ . Thus, the noise immunity of the feedback signal increases. However, a larger  $v_{SEN(AC),pp}$  also causes a worse offset voltage at  $v_{OUT}$ . The value of  $v_{OUT(DC)}$  in Figure 4.41(a)–(c) is 599, 611, and 630 mV, respectively. By contrast, the results reveal that  $\tau_{SEN}$  increases with an increase in the value of  $C_S$ , as shown in Figure 4.41(d), (e). If  $R_S$  is 250  $\Omega$  and  $C_S$  is 1.0  $\mu\text{F}$ , then the value of  $v_{SEN(AC),pp}$  decreases to approximately 3.76 mV.  $v_{OUT}$  is still well regulated and its waveform is similar to that of  $v_{SUM}$ . However, the linearity between  $v_{SUM}$  and  $i_L$  is worse. As a result, the operation is unstable when a smaller  $\tau_{SEN}$  with  $C_S = 4.7 \mu\text{F}$  is used, as shown in Figure 4.41(e).

In other words, stability is strongly determined by the value of  $\tau_{SEN}$ . Compared with the conventional on-time control with a sufficiently large value of  $R_{ESR}$ , the ripple of  $v_{SEN}$  replaces the function ripple of  $V_{ESR}$ . Equation (4.64) defines  $R_{eq,SEN}$  as the equivalent resistance for stability compensation:

$$R_{eq,SEN} = \frac{v_{SEN(AC),pp}}{i_{L,pp}} = \frac{L}{\tau_{SEN}} \quad (4.64)$$

The stability criterion expressed in Eq. (4.14) can be modified to obtain Eqs. (4.65) and (4.66) simultaneously, and thus reduce the practical ESR:

$$(R_{ESR} + R_{eq\_SEN}) \cdot C_{OUT} > \frac{T_{ON}}{2} \quad (4.65)$$

$$\left( R_{ESR} + \frac{L}{\tau_{SEN}} \right) \cdot C_{OUT} > \frac{T_{ON}}{2} \quad (4.66)$$

#### Example 4.5: Transient response is affected by different $\tau_{SEN}$ values because $v_{SEN}$ and $v_{OUT}$ exhibit opposite trends during transient response

According to the analysis results, another design consideration is the influence of different  $\tau_{SEN}$  values on the transient response. Tables 4.11 and 4.12 list the basic specifications and several important parameters, respectively. Figure 4.42 shows the waveforms of the transient response if the same  $R_S$  of 250  $\Omega$  and different  $C_S$  of 470 nF, 100 nF, and 1.0  $\mu\text{F}$  are used.

The time constant constituted by different  $R_S$  and  $C_S$  is defined as  $\tau_{SEN,I}$ ,  $\tau_{SEN,II}$ , and  $\tau_{SEN,III}$ , corresponding to cases I, II, and III. Their relationship is shown as:

$$\tau_{SEN,II} < \tau_{SEN,I} < \tau_{SEN,III} \quad (4.67)$$

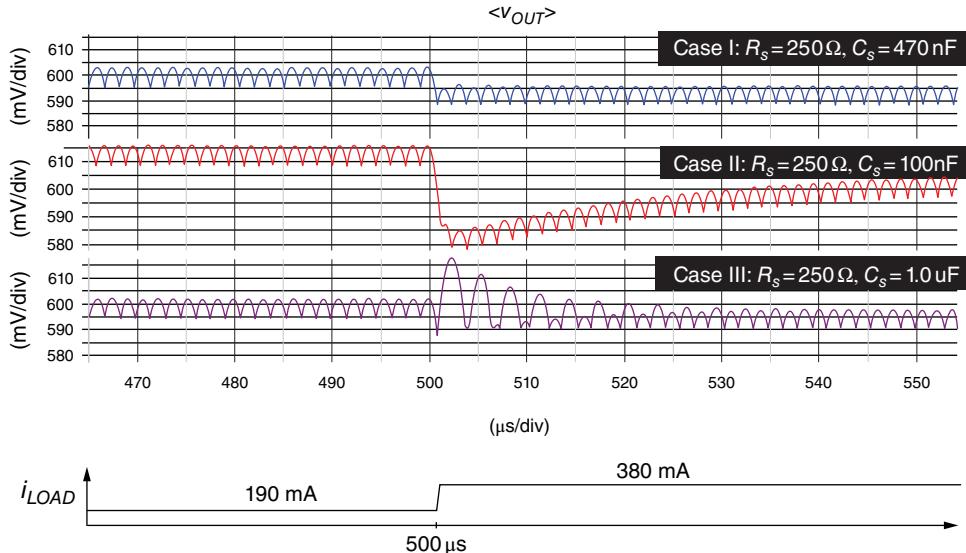
**Table 4.11** Basic specifications used in Example 4.3

$V_{IN}$	$V_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu\text{H}$	40 m $\Omega$	4.7 $\mu\text{F}$	0 m $\Omega$	0 nH	180 ns	660 kHz

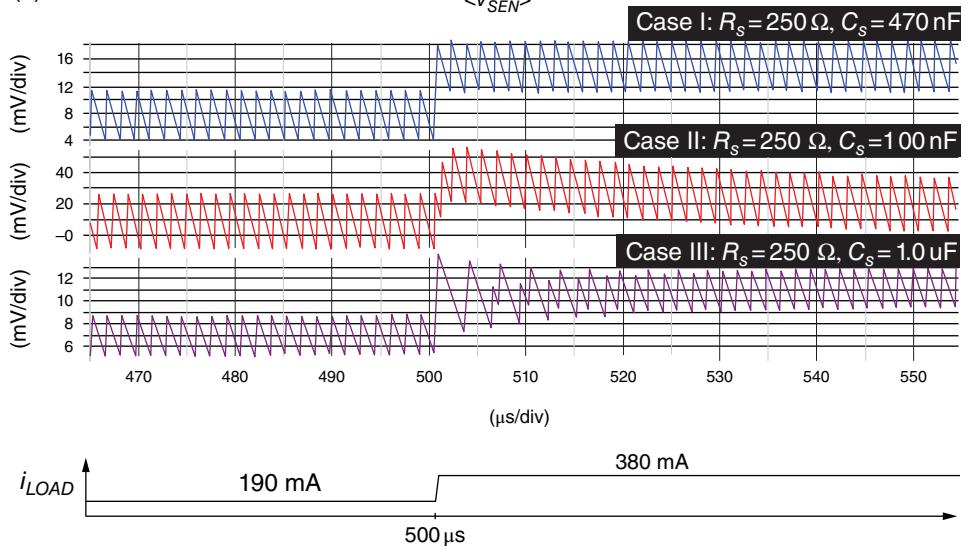
**Table 4.12** Designing parameters and characteristics in three different cases

Case	$L$	$R_{DCR}$	$R_S$	$C_S$	Characteristic	Transient response
I	4.7 $\mu$ H	40 m $\Omega$	250 $\Omega$	470 nF	Pole/zero cancellation	Optimum
II				100 nF	Phase lead	Insensitive
III				1.0 $\mu$ F	Phase delay	Sensitive

(a)



(b)

**Figure 4.42** Waveforms of (a)  $v_{OUT}$ , (b)  $v_{SEN}$ , (c)  $v_{SUM}$ , and (d)  $i_L$  in case of three values of  $C_S$  (470 nF, 100 nF, and 1.0  $\mu$ F) and the same  $R_S$  (250  $\Omega$ ) during load transient response

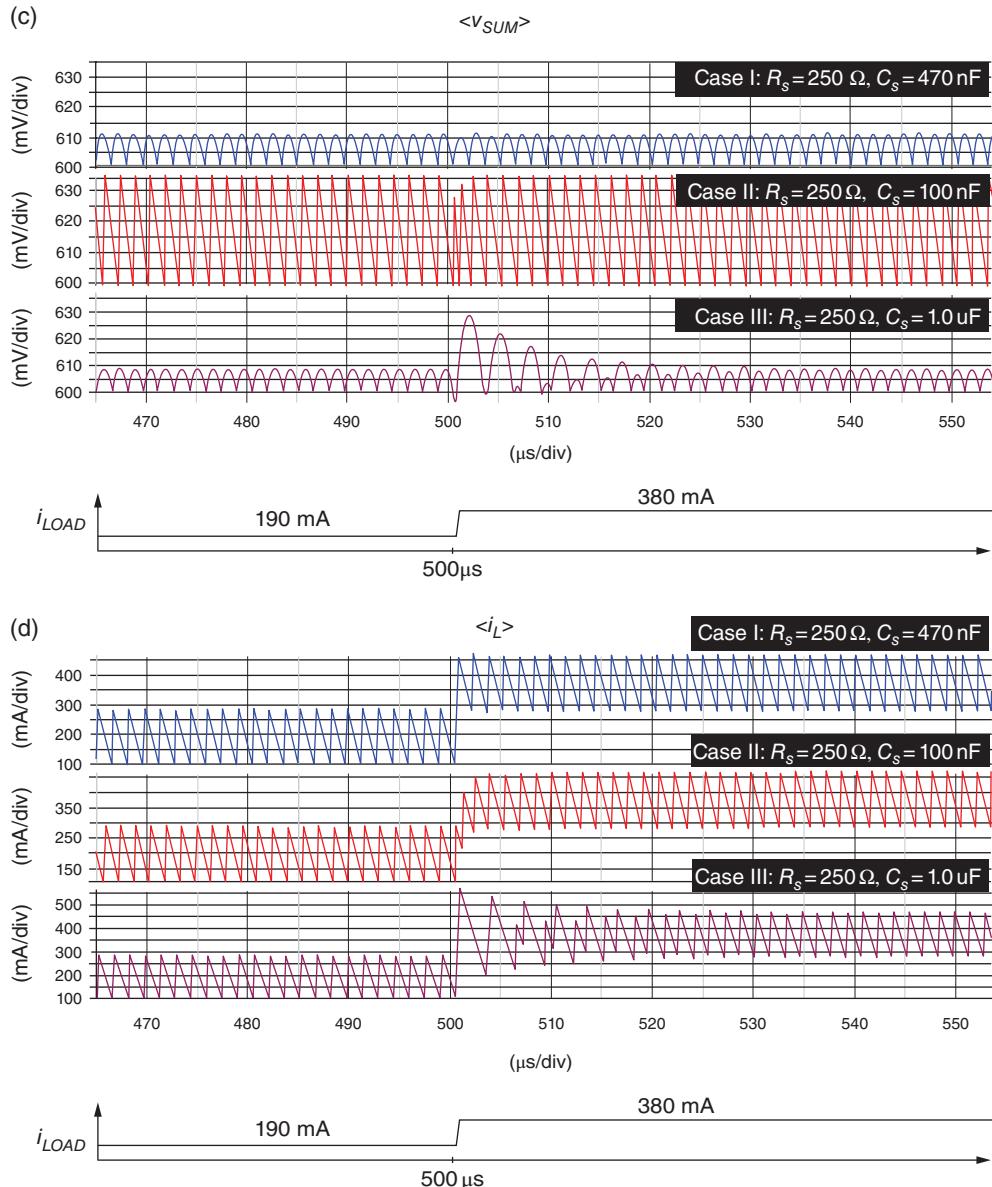


Figure 4.42 (Continued)

Figure 4.42(a)–(d) shows the waveforms of  $v_{OUT}$ ,  $v_{SEN}$ ,  $v_{FB}$ , and  $i_L$ , respectively. The waveforms of  $v_{SEN}$  reflect the similar waveforms of  $i_L$ , whereas the waveforms of  $v_{FB}$  reflect the information from  $v_{OUT}$  and  $v_{SEN}$ . The loading condition changes from 188 to 375 mA at 500  $\mu\text{s}$ . In Figure 4.42(a), the waveforms of  $v_{OUT}$  in the three cases present different transient responses. The waveforms in case II exhibit a slow response, resulting in a significant undershoot voltage. The waveforms in case III exhibit a fast response, resulting in an overshoot

voltage. We analyze this characteristic by observing the trends of  $v_{OUT}$  and  $v_{SEN}$  at the load transient response. As previously mentioned,  $v_{SEN}$  and  $v_{OUT}$  exhibit opposite trends during transient response. The variation of  $v_{SUM}$  becomes less evident. Therefore, the transient response is inhibited. The waveforms of  $v_{SEN}$  shown in Figure 4.42(b) reveal that different time constants reflect different responses of current sensing and determine the response of  $v_{OUT}$  during the transient period. In cases II and III, Eq. (4.54) does not hold. Different values of pole and zero in Eq. (4.53) result in the phase lead and phase delay functions corresponding to cases II and III, respectively. By contrast, the waveforms in case I exhibit an adequate response because the value of  $\tau_{SEN,I}$  meets the requirement of Eq. (4.54). Considering the phase lead function,  $v_{SEN}$  in case II becomes more sensitive to  $i_L$  sensing, as shown in Figure 4.42(d). As a result, although voltage droop occurs at  $v_{OUT}$ ,  $v_{SUM}$  shown in Figure 4.42(c) has a small variation, which slows down the transient response. Similarly,  $v_{SEN}$  in case III becomes less sensitive to  $i_L$  sensing because of the phase lead function.

**Example 4.6: The influence on  $v_{OUT}$  ripples and power loss is not the same for different values of  $R_S$  and  $C_S$  with the same time constant  $\tau_{SEN}$**

According to the analysis of Example 4.4, we discuss the performance in three cases which have different values of  $R_S$  and  $C_S$  but with time constant  $\tau_{SEN}$  the same. Although the time constant is the same, the influence on  $v_{OUT}$  ripples and power loss is not the same in each case. Tables 4.13 and 4.14 list the basic specifications and the critical parameters, respectively.

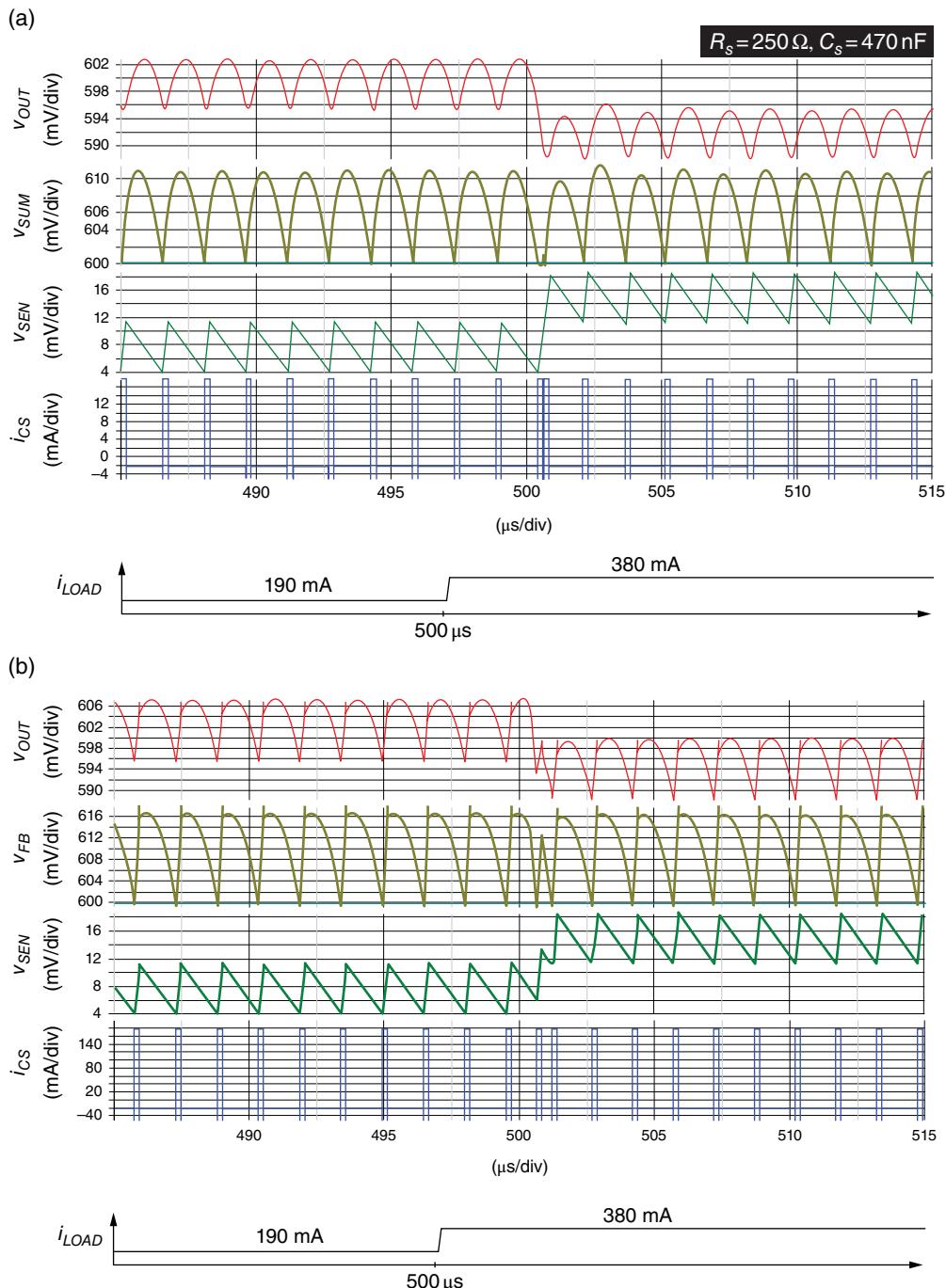
The only different condition is that  $R_{ESR} = 10 \text{ m}\Omega$  compared with Example 4.4. Figure 4.43 gives three cases I, II, and III, with pairs of  $[R_S, C_S]$  equal to  $[250 \Omega, 470 \text{ nF}]$ ,  $[25 \Omega, 4.7 \mu\text{F}]$ , and  $[2.5 \text{ k}\Omega, 0.47 \text{ nF}]$ , respectively. Owing to the same  $\tau_{SEN}$  in the three cases,  $v_{SEN}$  reflects the same waveforms in the steady-state period and the transient period. The peak-to-peak value and the DC value of  $v_{SEN}$  in the three cases are similar. As a result,  $v_{OUT}$  in the three cases has a similar droop and transient response. However, it's worth noticing that the  $i_{CS}$  are quite different in these cases, where  $i_{CS}$  is the current flow from  $C_S$  to  $v_{OUT}$ . With a smaller value of  $R_S$  and a larger value of  $C_S$  in Figure 4.43(b), the peak value of  $i_{CS}$ ,  $i_{CS,peak}$ , is 180 mA. Basically, a higher peak value of  $i_{CS}$  is not expected because a larger current consumes more conduction loss. Besides, this current appearing during the on-time period can inject/sink the extra current into/from  $C_{OUT}$ . For this reason, in addition to the AC component of  $i_L$ ,  $i_{CS}$  also flows through  $R_{ESR}$  and  $C_{OUT}$ . That's why the waveform of  $v_{OUT}$  shown in Figure 4.43(b) suffers from an obvious step at the switching time from on-time period to off-time period and vice versa, compared with Figure 4.43(a), (c).

**Table 4.13** Basic specifications used in Example 4.5

$v_{IN}$	$v_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu\text{H}$	40 m $\Omega$	4.7 $\mu\text{F}$	10 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.14** Designing parameters in three cases

Case	$L$	$R_{DCR}$	$R_S$	$C_S$
(a)	4.7 $\mu\text{H}$	40 m $\Omega$	250 $\Omega$	470 nF
(b)			25 $\Omega$	4.7 $\mu\text{F}$
(c)			25 k $\Omega$	47 nF



**Figure 4.43** Load transient waveforms if (a)  $R_s = 250 \Omega$  and  $C_s = 470 \text{ nF}$ , (b)  $R_s = 25 \Omega$  and  $C_s = 4.7 \mu\text{F}$ , and (c)  $R_s = 2.5 \text{ k}\Omega$  and  $C_s = 47 \text{ nF}$  where external components include  $L = 4.7 \mu\text{H}$ ,  $R_{DCR} = 40 \text{ m}\Omega$ ,  $L_{ESL} = 0 \text{ nH}$ ,  $R_{ESR} = 10 \text{ m}\Omega$ , and  $C_{OUT} = 4.7 \mu\text{F}$

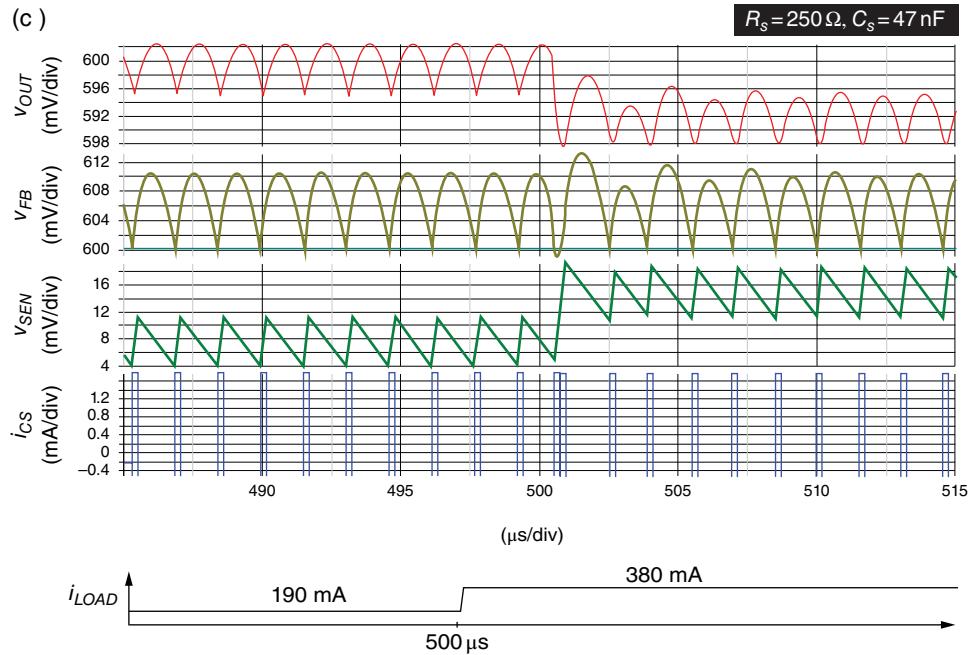


Figure 4.43 (Continued)

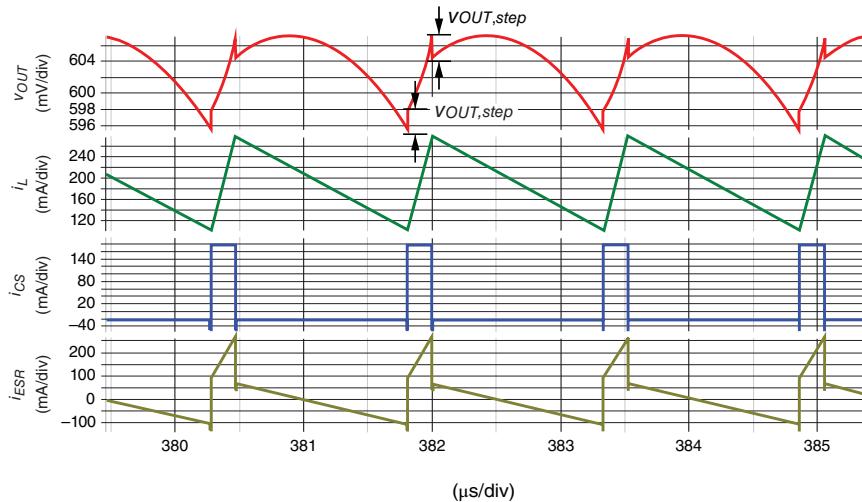
Figure 4.44 Operation waveforms for the case of  $R_S = 25 \Omega$  and  $C_S = 4.7 \mu F$ 

Figure 4.44 shows more detailed waveforms, including  $v_{OUT}$ ,  $i_L$ ,  $i_{CS}$ , and  $i_{ESR}$ . Here  $i_{ESR}$  is the current flowing through  $R_{ESR}$ , which can be derived from  $i_L$  and  $i_{CS}$ :

$$i_{ESR}(t) = i_L(t) - i_{L,avg} + i_{CS}(t) \quad (4.68)$$

The value of the extra step,  $v_{OUT,step}$ , in the waveform of  $v_{OUT}$  is determined by  $i_{CS,peak}$  and the value of  $R_{ESR}$ , as expressed in Eq. (4.69).  $v_{OUT,step}$  is only 1.8 mV, because  $R_{ESR}$  is 10 mΩ. However, the extra  $v_{OUT,step}$  should be considered carefully because of the high-frequency noise and extra voltage ripple when  $R_{ESR}$  is large.

$$v_{OUT,step} = i_{CS,peak} \cdot R_{ESR} \quad (4.69)$$

As a result, we recommend that the designer chooses a larger  $R_S$  but a smaller  $C_S$  for small conduction power loss, less current density demand, and a small voltage ripple. Furthermore, a capacitance of several pico-farads also benefits the possibility of full integration.

### Setting in SIMPLIS

Figure 4.45 illustrates the setup circuit via SIMPLIS corresponding to Figure 4.37. This circuit is composed of a comparator, on-time pulse generator, non-overlap circuit, high-side switch, low-side switch, inductor, parallel RC-filter, output capacitor, and output loading. High-side and low-side switches are parallel with a diode to form an equivalent MOSFET device.

Figure 4.46 provides a zoomed-in view of the partial portion of Figure 4.45. Some critical devices should be defined, and Figure 4.47 illustrates the setting windows for those parameters.

Figure 4.47(a) shows the window to edit the device parameter of the output capacitor, whose value is 4.7 μF. “Level” is set as “2” to activate the value setting of ESR. However, with the parallel RC-filter function of Example 4.4, the value of ESR is 0 mΩ. Figure 4.47(b) shows the window to edit the device parameter of the inductor, whose value is 4.7 μH. “Series Resistance” is  $R_{DCR}$ , set as 40 mΩ.

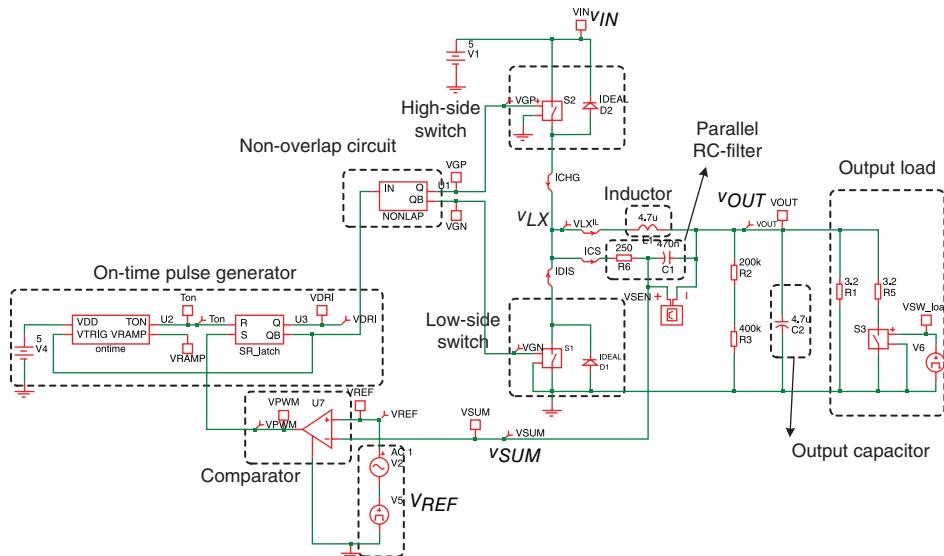
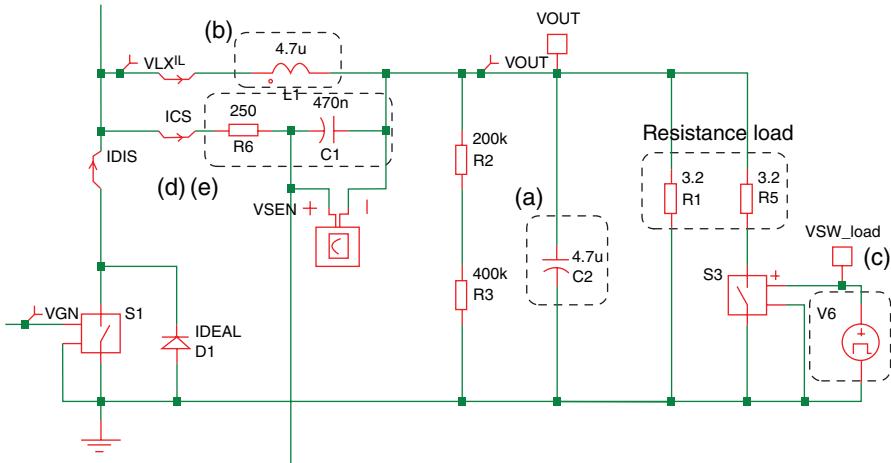
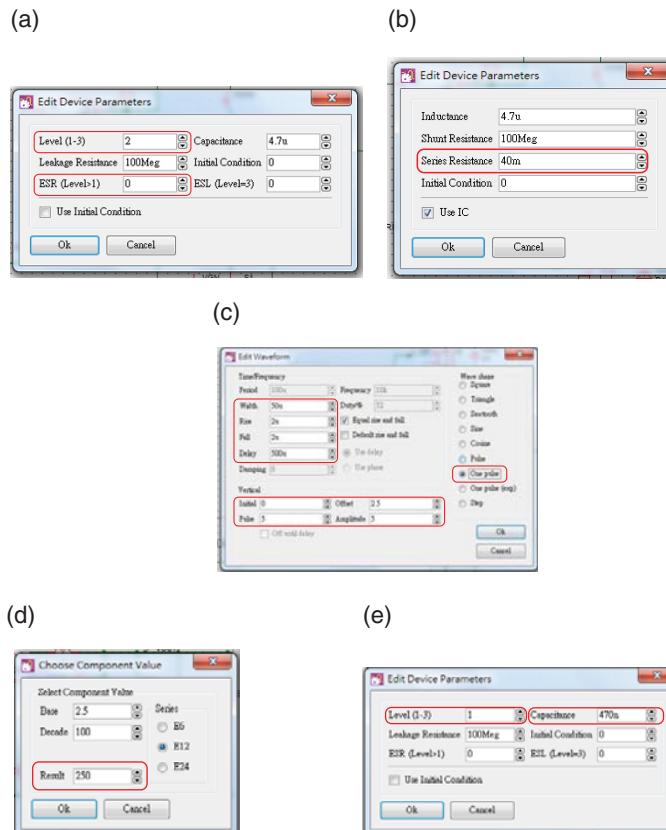


Figure 4.45 Setup circuit in SIMPLIS



**Figure 4.46** Zoom-in views of output filter, RC-filter, and output loading



**Figure 4.47** Windows for setting device parameters. (a) Output capacitor. (b) Inductor. (c) Output load. (d) Resistance of parallel RC-filter. (e) Capacitance of parallel RC-filter

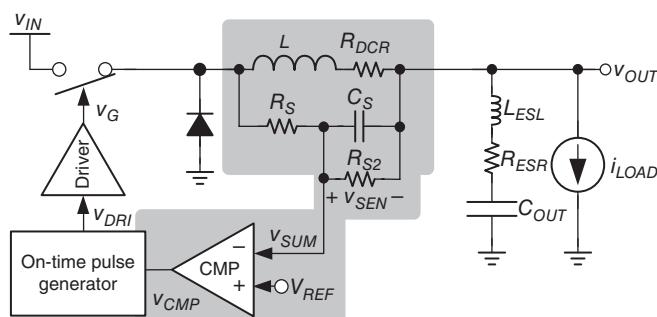
Figure 4.47(c) shows the window to edit the device parameter of the change in loading conditions. “Wave shape” is selected first as “One pulse,” then “Time/Frequency” can be set for the time of load change. In this setting, the loading condition remains at light load until a time of 500  $\mu$ s, and then changes from light load to heavy load in 2  $\mu$ s. In turn, the loading condition remains at heavy load until the time is 550  $\mu$ s, and then changes from heavy load to light load in 2  $\mu$ s. Besides, the value of the load change is adjusted by the value of “Resistance load,” as labeled in Figure 4.24.

Figure 4.47(d), (e) shows the windows to edit the device parameters of resistance and capacitance of the parallel RC-filter, respectively. Different values are set in Examples 4.4 and 4.5.

#### 4.3.2.4 CF-type4 (Parallel RC-Filter with AVP Function)

When Eq. (4.54) holds for pole/zero cancellation, the output exhibits resistive impedance rather than inductive or capacitive impedance. In other words, the converter features an adaptive voltage positioning (AVP) function. Voltage droop exists in different loading conditions. When the load transient changes from light to heavy load, as shown in Figure 4.40,  $v_{OUT}$  decreases because the instant load change extracts charges from the output capacitor. The output voltage is regulated at low voltage levels at heavy loading conditions because of the AVP. Then, the converter does not need to recharge the charge to the output capacitor, so the transient period is shortened. Similarly, the output voltage is regulated at high voltage levels at light loading conditions.

The voltage droop is dependent on the DC value of  $v_{SEN}$ , which is determined based on several parameters, as expressed in Eq. (4.53). In portable devices, the layout of the PCB and the size of the component are restricted. An inductor with a small size usually has a large DCR value. The bonding wires and conducting path on the PCB should also be considered in estimating the DCR value. The original current-sensing technique shown in Figure 4.37 is unsuitable to achieve adequate droop. Figure 4.49 below shows another RC-filter structure used to sense inductor current information. Using  $R_{S2}$  in parallel with  $C_S$ , as shown in Figure 4.48,  $v_{SEN}(s)$  can be derived as in Eq. (4.70). Compared with Eq. (4.53), the DC gain can be adjusted



**Figure 4.48** Sensing technique with additional parallel  $R_{S2}$  for the AVP function

using  $R_{S2}$ , as shown in Eq. (4.70). Thus, the DC value of  $v_{SEN}$  can be adjusted, as expressed in Eq. (4.71). Consequently, the extra parallel resistor  $R_{S2}$  can enhance the flexibility of the AVP function to achieve a fast transient response.

$$v_{SEN}(s) = \left[ R_{DCR} \cdot i_L \cdot \left( \frac{R_{S2}}{R_S + R_{S2}} \right) \right] \cdot \frac{1 + s(L/R_{DCR})}{1 + s\left(\frac{R_S \cdot R_{S2}}{R_S + R_{S2}}\right)C_S} \quad (4.70)$$

$$v_{SEN(DC)} = R_{DCR} \cdot i_L \cdot \left( \frac{R_{S2}}{R_S + R_{S2}} \right) \quad (4.71)$$

#### 4.3.2.5 CF-type5 (Parallel RC-Filter with Voltage Droop Cancellation)

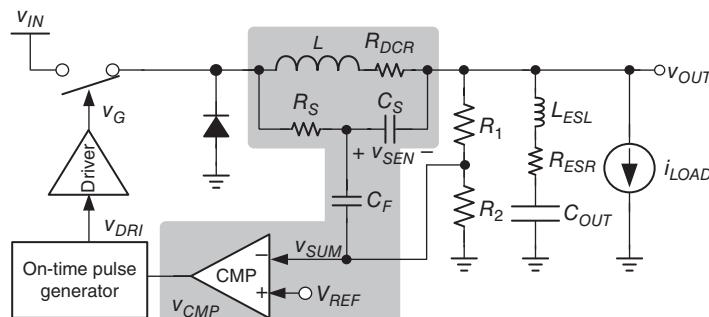
In several applications, the  $v_{OUT}$  of the converter is required for good load regulation. Specifically, voltage droop is not expected at different loading conditions. In the aforementioned current-sensing technique with voltage droop, the voltage droop is caused by varying DC values of current-sensing information  $v_{SEN}$ , which is linear in  $i_L$ . Removing the DC component from the current-sensing information  $v_{SEN}$  is necessary to eliminate the effect of voltage droop.

As shown in Figure 4.49, a decoupling capacitor  $C_F$  is added directly to conduct the AC component of  $v_{SEN}$  but blocks the DC component of  $v_{SEN}$ . Moreover, the DC information from  $v_{OUT}$  is conducted using the feedback dividers  $R_1$  and  $R_2$ . The output voltage can be regulated without voltage droop with the AC component of  $i_L$  and the DC component of  $v_{OUT}$ , respectively.

Although the extra capacitor  $C_F$  is added through the path of  $v_{SEN}$  to extract  $v_{SEN(AC)}$ , the voltage droop is removed but the offset voltage still remains, as expressed in Eq. (4.72) in comparison with Eq. (4.59), where  $v_{offset}$  in Eq. (4.73) represents the offset voltage:

$$v_{OUT(DC)} \approx \frac{1}{\beta} V_{REF} + v_{offset} \quad (4.72)$$

$$v_{offset} = \frac{1}{\beta} \cdot \left( \frac{1}{2} v_{SEN(AC),pp} \right) + \frac{1}{2} v_{OUT(AC),pp} \quad (4.73)$$

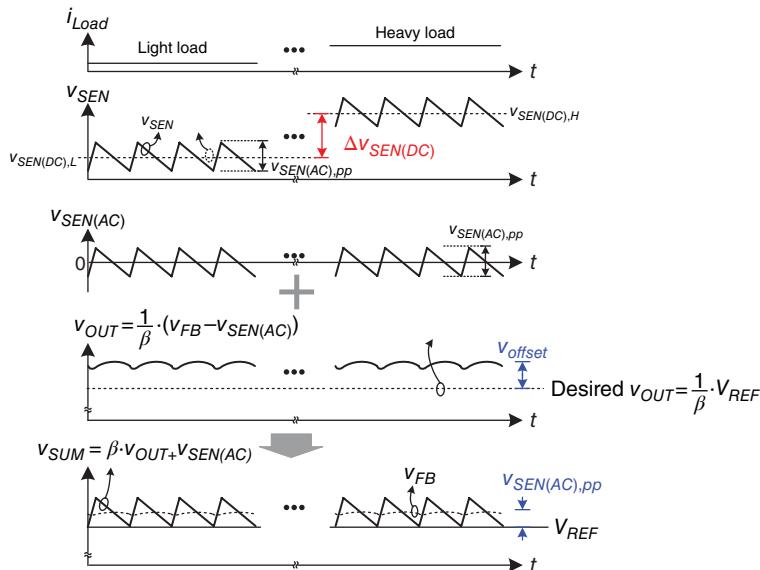


**Figure 4.49** Current-sensing technique with decoupling capacitor  $C_F$

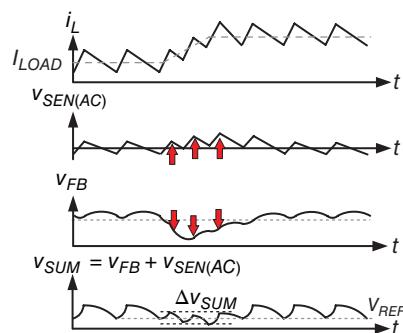
When MLCC is used for a small ripple, the small value of  $v_{OUT(AC),pp}$  can be ignored to simplify Eqs. (4.73) and (4.74):

$$v_{offset} = \frac{1}{\beta} \cdot \left( \frac{1}{2} v_{SEN(AC),pp} \right) \quad (4.74)$$

Figure 4.50 shows that the offset voltage is caused by  $v_{SEN(AC),ripple}$ . Figure 4.51 shows that the transient response is not improved, which is similar to the result shown in Figure 4.39 without extra  $C_F$ , because  $v_{SEN(AC)}$  also exhibits an opposite trend to the variation of  $v_{FB}$  during transient response.



**Figure 4.50**  $V_{OUT}$  has a voltage offset at different loading conditions



**Figure 4.51** Deterioration of the load transient response because of the additional CF path

However, the direct use of  $C_F$  has poor capability to be a good HPF for conducting only the AC component of  $v_{SEN}$ . The other resistances and capacitances, such as  $R_1$ ,  $R_2$ ,  $R_S$ ,  $C_S$ , and  $C_F$ , can influence the HPF bandwidth. In the aspect of a large signal, these resistances and capacitances also influence the driving capability of the AC component through  $C_F$  and the DC component through the feedback divider. The transfer function of this structure is complex. In other words, determining the weight of the AC component of  $i_L$  and the DC component of  $v_{OUT}$  for  $v_{FB}$  is difficult. Suitable stability and transient response are difficult to achieve at the same time.

Figure 4.52 shows the structure of another RC-filter used to achieve the same function. Two pairs of RC-filters are utilized. The first RC-filter is composed of  $R_S$  and  $C_S$  placed parallel with the inductor. The second RC-filter is composed of  $R_{S2}$  and  $C_{S2}$  placed parallel with  $C_S$ . Initially, these two RC-filters are assumed to be independent of each other to understand the function of this current-sensing technique easily. Based on Eq. (4.53),  $v_{S1}$  shown in Figure 4.52 includes information on the AC and DC components of  $i_L$ .  $v_{S1}$  is approximately expressed as follows:

$$v_{S1}(s) = \left[ R_{DCR} \cdot i_L \cdot \frac{1 + s(L/R_{DCR})}{1 + sR_S C_S} \right] + v_{OUT} \quad (4.75)$$

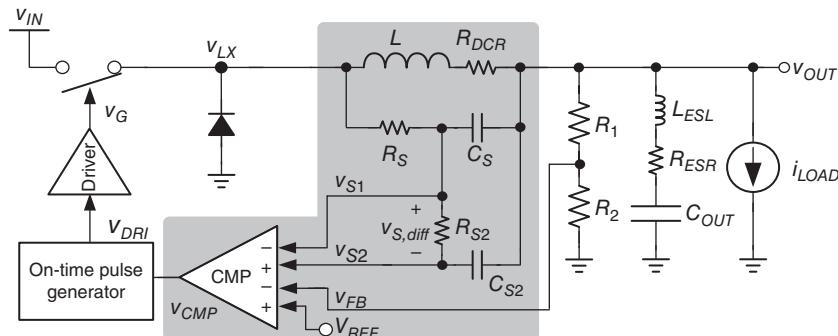
By intuition, the second RC-filter can be viewed as the LPF used to filter the AC component of  $v_{S1}$  so that  $v_{S2}$  includes only the DC component of  $v_{S1}$ . As a result, the difference between  $v_{S1}$  and  $v_{S2}$ ,  $v_{S,diff}$ , represents the AC component of  $i_L$ , which is fed into the comparator.  $v_{S,diff}$  is expressed as follows:

$$v_{S,diff} = v_{S1} - v_{S2} \quad (4.76)$$

By contrast,  $v_{FB}$  and  $V_{REF}$  are also fed into the same comparator. Therefore,  $v_{SUM}$  is expressed as:

$$v_{SUM} = v_{FB} + v_{S,diff} \quad (4.77)$$

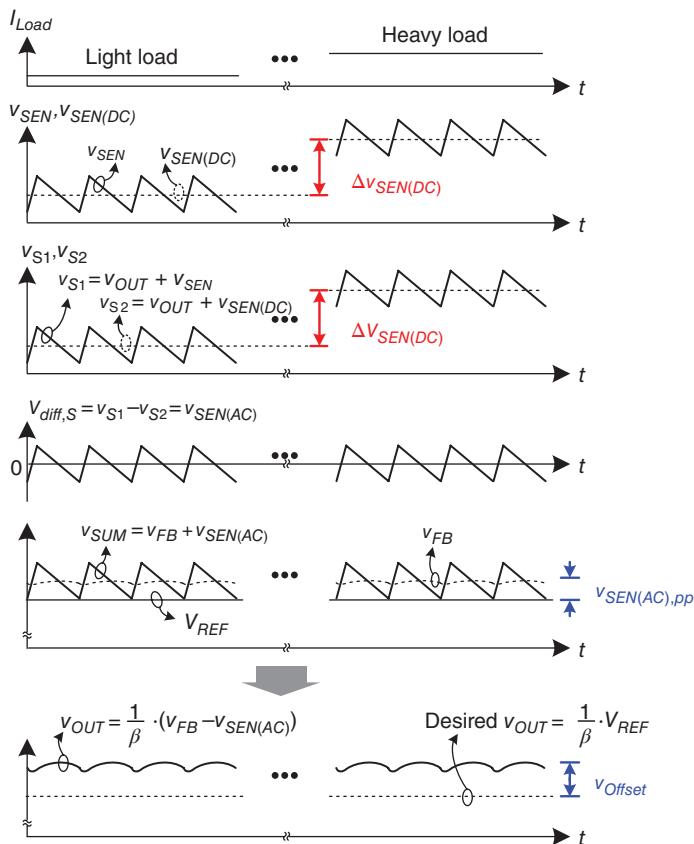
Thus, the output signal of the comparator represents the response of the AC component of  $i_L$  and the DC component of  $v_{OUT}$ . Table 4.15 lists the signal and the corresponding components.



**Figure 4.52** Current-sensing technique with two pairs of RC-filters

**Table 4.15** Signal and corresponding components

Signal	Component
$v_{S1}$	DC + AC
$v_{S2}$	DC
$v_{S,diff}$	AC

**Figure 4.53** Voltage offset of  $v_{OUT}$  at different loading conditions

Similar to the result shown in Figure 4.50, the structure shown in Figure 4.52 can remove the voltage droop at the DC component of  $v_{SUM}$  at different loading conditions so that the voltage droop at  $V_{OUT}$  is removed. The operating waveform is shown in Figure 4.53.

The valley of  $v_{SUM}$  is regulated at  $v_{REF}$  because of the comparator in the feedback loop. However, the valley of  $v_{SUM}$  is not equal to the valley of  $v_{FB}$  because the average value of  $v_{SUM}$  is zero. The ripple of  $v_{S,diff}$  generates a DC offset at  $v_{SUM}$ , ( $V_{offset,v_{SUM}}$ ), between the averages of  $v_{SUM}$  and  $v_{REF}$ , where  $v_{FB}$  is derived from Eq. (4.77) as:

$$v_{FB} = v_{SUM} + v_{S,diff} \quad (4.78)$$

$v_{offset,vSUM}$  is calculated as follows:

$$v_{offset,vSUM} = \frac{1}{2} v_{SUM,pp} \quad (4.79)$$

The DC offset of  $v_{OUT}$  can then be calculated as:

$$v_{offset,vOUT} = \frac{R_1 + R_2}{R_2} \cdot \frac{1}{2} v_{SUM,pp} \quad (4.80)$$

The DC offset of  $v_{OUT}$  is unexpected because the accuracy of  $v_{OUT}$  has deteriorated.

Furthermore, Figure 4.54 shows that an extra voltage-controlled voltage source (VCVS) linear amplifier is inserted between  $v_{S,diff}$  and the comparator to control the weight of the AC component of  $i_L$  and the DC component of  $v_{OUT}$ . The gain of this VCVS linear amplifier is defined as  $G$ . Therefore,  $v_{SUM}$  is expressed as:

$$v_{SUM} = v_{FB} + G \cdot v_{S,diff} \quad (4.81)$$

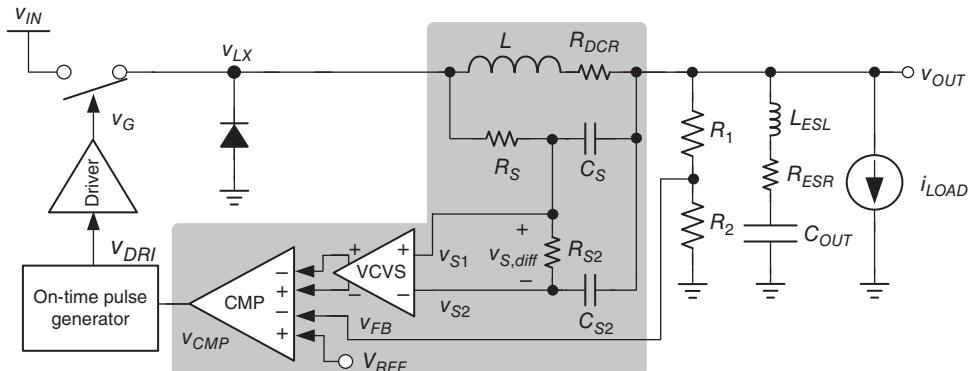
Equation (4.82) can also be re-derived from Eq. (4.66):

$$\left( R_{ESR} + G \cdot \frac{L}{R_S C_S} \right) \cdot C_{OUT} > \frac{T_{ON}}{2} \quad (4.82)$$

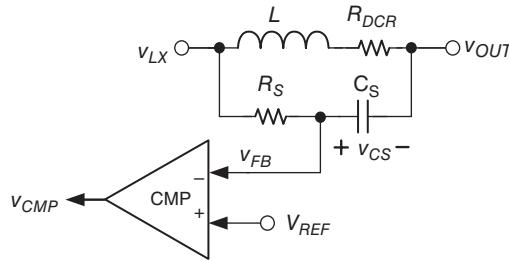
However, these two RC-filters can influence their function in actual cases. The subsequent analyses determine the suitable parameters of these resistances and capacitances to avoid analyzing and using the complex transfer function from  $i_L$  to  $v_{S,diff}$  of these two RC-filters.

First, we review the structure of the current-sensing technique with only one RC-filter, as shown in Figure 4.55. Based on the values of pole and zero in Eq. (4.75), Eq. (4.83) is utilized for pole/zero cancellation to achieve a fast transfer function:

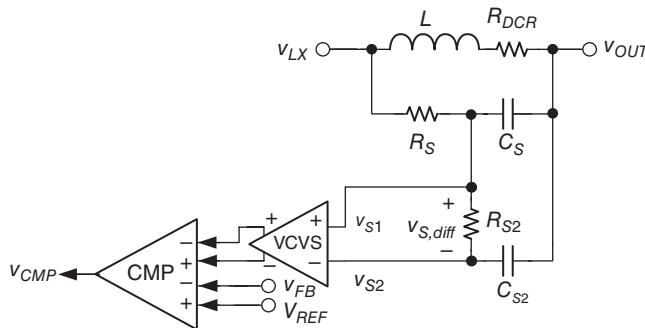
$$L/R_{DCR} = R_S C_S \quad (4.83)$$



**Figure 4.54** Current-sensing technique with two pairs of RC-filters and VCVS linear amplifiers



**Figure 4.55** Structure of the current-sensing technique with one RC-filter



**Figure 4.56** Structure of the current-sensing technique with two pairs of RC-filters

Figure 4.56 shows the structure of the current-sensing technique with two pairs of RC-filters. Given the transient response,  $R_S$  and  $C_S$  are also derived using Eq. (4.83) based on previous experience.

However, the values of  $R_{S2}$  and  $C_{S2}$  influence the aberration of pole/zero cancellation and the transient response of  $v_{S1}$  that generates the phase lead or phase delay function. Therefore, a significantly large aberration can inhibit the load transient response. Moreover, significantly large values of  $R_{S2}$  and  $C_{S2}$  further slow down the transient response of  $v_{S2}$  and inhibit the load transient response. As a result, the criteria expressed in Eqs. (4.84) and (4.85) are approximately set as follows:

$$R_{S2}C_{S2} < \frac{1}{10}R_SC_S \quad (4.84)$$

$$C_{S2} < \frac{1}{10}C_S \quad (4.85)$$

The second RC-filter, composed of  $R_{S2}$  and  $C_{S2}$ , is used to derive the function of the LPF. Considering the suitable bandwidth of the LPF, the inequality expressed in Eq. (4.86) is set as follows:

$$\frac{1}{2\pi R_{S2}C_{S2}} < \frac{f_{SW}}{4} \quad (4.86)$$

By rearranging, Eq. (4.87) can be derived from Eq. (4.86):

$$R_{S2}C_{S2} > \frac{2}{\pi} \cdot \frac{1}{f_{SW}} \quad (4.87)$$

The combination of Eqs. (4.82)–(4.86) results in Eqs. (4.88)–(4.90), which are employed to obtain the values of  $R_S$ ,  $C_S$ ,  $R_{S2}$ , and  $C_{S2}$ .

$$\left\{ \begin{array}{l} (R_{ESR} + G \cdot \frac{L}{R_S C_S}) \cdot C_{OUT} > \frac{T_{ON}}{2} \\ \frac{2}{\pi f_{SW}} < R_{S2} C_{S2} < \frac{1}{10} (R_S C_S) = \frac{1}{10} (L/R_{DCR}) \end{array} \right. \quad (4.88)$$

$$\left\{ \begin{array}{l} \frac{2}{\pi f_{SW}} < R_{S2} C_{S2} < \frac{1}{10} (R_S C_S) = \frac{1}{10} (L/R_{DCR}) \\ C_{S2} < \frac{1}{10} C_S \end{array} \right. \quad (4.89)$$

$$\left\{ \begin{array}{l} C_{S2} < \frac{1}{10} C_S \end{array} \right. \quad (4.90)$$

#### **Example 4.7: Simulation results provide four cases for comparison to validate Eq. (4.89)**

This simulation provides four cases for comparison to validate Eq. (4.89). Table 4.16 lists the basic specifications, and Table 4.17 lists the critical parameters. In this simulation,  $R_1 = 0$  k $\Omega$ ,  $R_2 = 400$  k $\Omega$ , and  $v_{OUT}$  is equal to  $v_{FB}$ . In the four cases, different values of  $R_{S2}$  and  $C_{S2}$  are obtained, whereas  $R_S$  and  $C_S$  are constant and provide perfect pole/zero cancellation to  $L$  and  $R_{DCR}$ . The result reveals that the different time constants result in different capabilities of the LPF and different levels of distortion of  $v_{S,diff}$ .

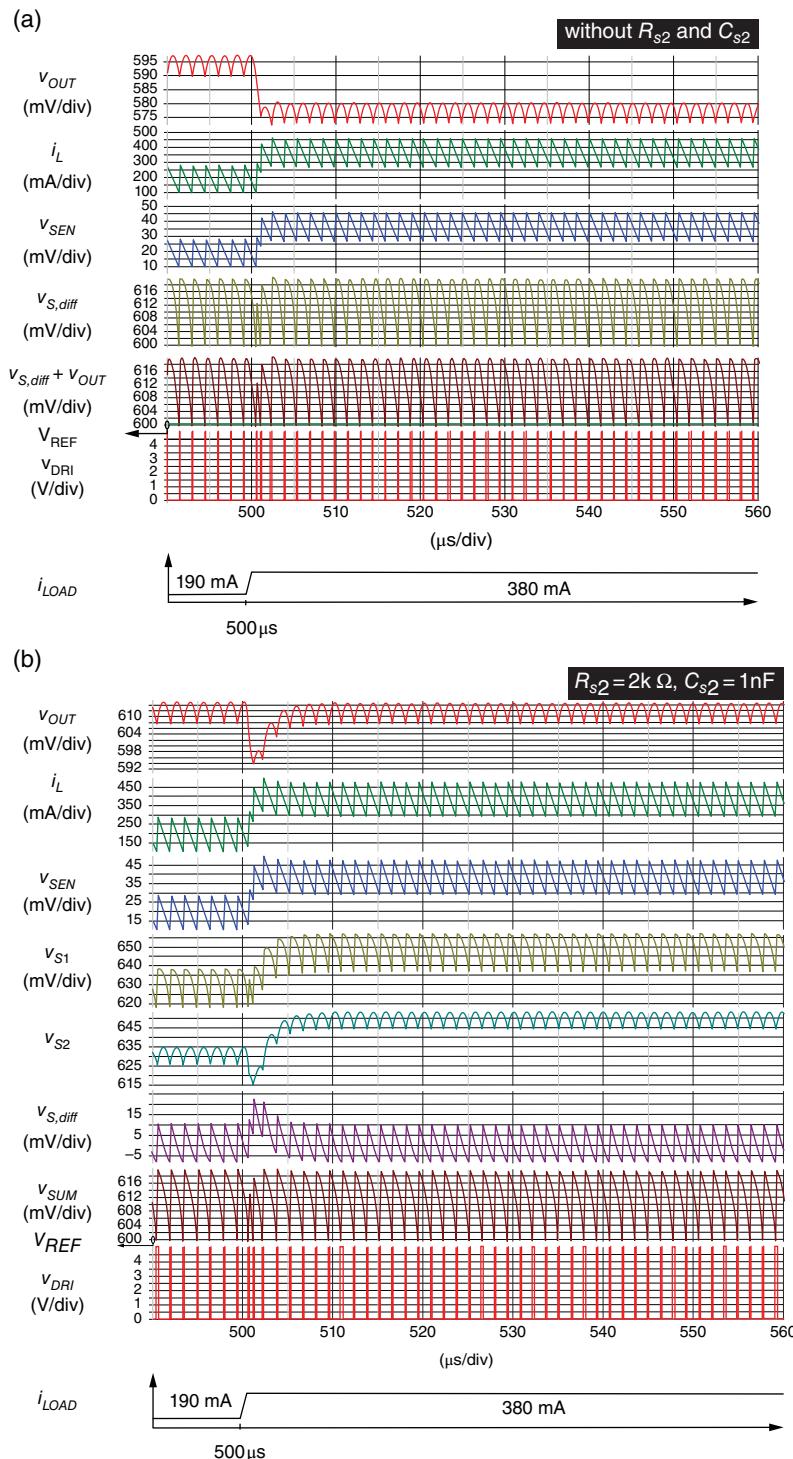
Figure 4.57 shows the waveform with transient response for the four cases. In case (a),  $R_{S2}$  and  $C_{S2}$  are absent and the structure is similar to that of type4. The  $V_{OUT}$  waveform suffers from voltage droop at different loading conditions because  $v_{SEN}$  contains the AC and DC components of  $i_L$ . In case (b),  $R_{S2}$  is 2 k $\Omega$  and  $C_{S2}$  is 1 nF based on the criterion expressed in Eq. (4.89). Therefore,  $v_{S,diff}$  exhibits a good result with only the AC component of  $i_L$ , and  $v_{OUT}$  exhibits good load regulation without extra voltage droop at different loading conditions. In

**Table 4.16** Basic specifications used in Example 4.7

$v_{IN}$	$v_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu$ H	100 m $\Omega$	4.7 $\mu$ F	0 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.17** Design parameters and characteristics of the four cases

Case	$R_{DCR}$	$R_S$	$C_S$	$R_{S2}$ (k $\Omega$ )	$C_{S2}$ (nF)	Characteristic
(a)	100 m $\Omega$	100 $\Omega$	470 nF	—	—	Has voltage droop
(b)				2	1	No voltage droop with good transient response
(c)				20	1	No voltage droop but poor transient response
(d)				0.2	1	Unstable because $v_{S,diff}$ has no AC component of $i_L$



**Figure 4.57** Load transient response (a) without  $R_{S2}$  and  $C_{S2}$ , (b) with  $R_{S2} = 2 \text{ k}\Omega$  and  $C_{S2} = 1 \text{ nF}$ , (c) with  $R_{S2} = 20 \text{ k}\Omega$  and  $C_{S2} = 1 \text{ nF}$ , and (d) with  $R_{S2} = 0.2 \text{ k}\Omega$  and  $C_{S2} = 1 \text{ nF}$

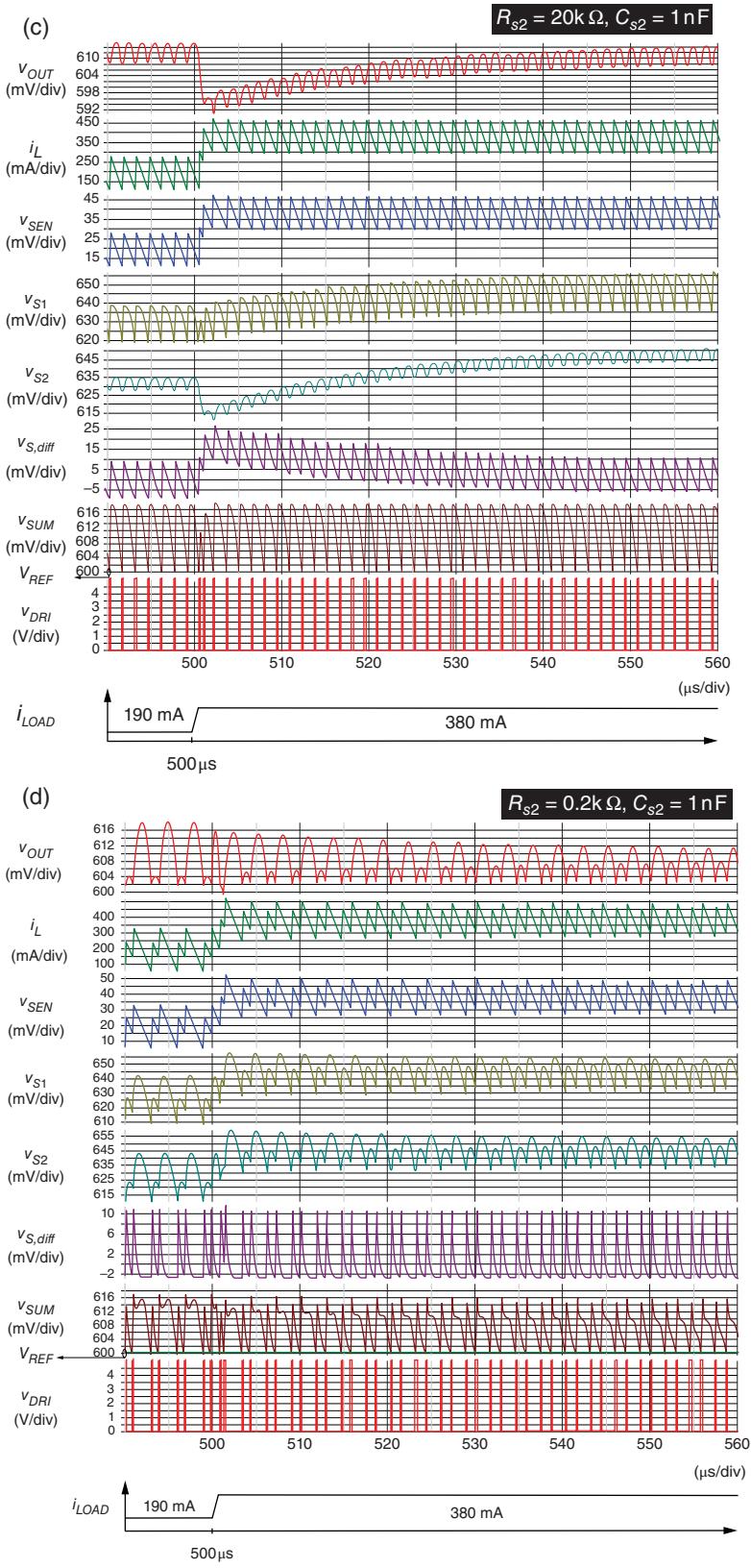


Figure 4.57 (Continued)

case (c),  $R_{S2}$  is 20 k $\Omega$  and  $C_{S2}$  is 1 nF. The condition of Eq. (4.89) holds, but the bandwidth of the values of  $R_{S2}$  and  $C_{S2}$  becomes lower than that in case (b). As a result, the transient response of  $v_{S2}$  becomes slower and still functions at steady state, although the voltage droop is removed. As a result, when the second inequality of Eq. (4.89) does not hold, the transient response becomes slower. In case (d),  $R_{S2}$  is 0.2 k $\Omega$  and  $C_{S2}$  is 1 nF. The first inequality of Eq. (4.89) does not hold, which is relative to the switching frequency. The RC-filter of  $R_{S2}$  and  $C_{S2}$  has no ability to filter out the AC component of  $i_L$  from  $v_{S2}$ . In other words, the AC component of  $i_L$  is almost removed from  $v_{S,diff}$  because  $v_{S1}$  and  $v_{S2}$  remain the AC component of  $i_L$ . As a result, the lack of current information on feedback degrades the stability when the output capacitor with low ESR is used.

**Example 4.8:** This example demonstrates Eq. (4.90) to discuss the influence of different values of  $R_{S2}$  and  $C_{S2}$

Table 4.18 lists the basic specifications. Here,  $R_1 = 0$  k $\Omega$  and  $R_2 = 400$  k $\Omega$ ,  $v_{OUT}$  is equal to  $v_{FB}$ . Table 4.19 lists the parameters for seven cases, and Figure 4.58 shows the relative waveforms.

In case (a),  $R_{S2}$  and  $C_{S2}$  are absent, and the structure is similar to that of type4. The  $v_{OUT}$  waveform suffers from voltage droop at different loading conditions because  $v_{CS}$  contains both the AC and the DC component of  $i_L$ . In other cases, the time constants of  $R_{S2}$  and  $C_{S2}$  are the same and Eq. (4.89) holds. Cases (b), (c), and (e) perform well in terms of load regulation and transient response. However, the value of  $C_{S2}$  is 10  $\mu$ F in case (d). Equation (4.90) does not hold, and the operation is unstable. In contrast, the values of  $R_{S2}$  and  $C_{S2}$  in case (f) satisfy Eqs. (4.89) and (4.90), but voltage droop occurs. In consideration of the too-large values of  $R_{S2}$  and the too-small values of  $C_{S2}$ , the leakage current of  $C_{S2}$  should be of concern. With a several mini-volt ripple of  $v_{SEN}$  across  $R_{S2}$  and  $C_{S2}$ , the current flowing through  $R_{S2}$  to  $v_{S2}$  would only be several nano-amperes. To emphasize the importance of the leakage current, the size of the leakage impedance is exaggerated to 100 M $\Omega$  in this case. Figure 4.59 shows the setting window of SIMPLIS to edit the device parameter of  $C_{S2}$ . Compared with  $R_{S2}$  of 20 M $\Omega$  and leakage

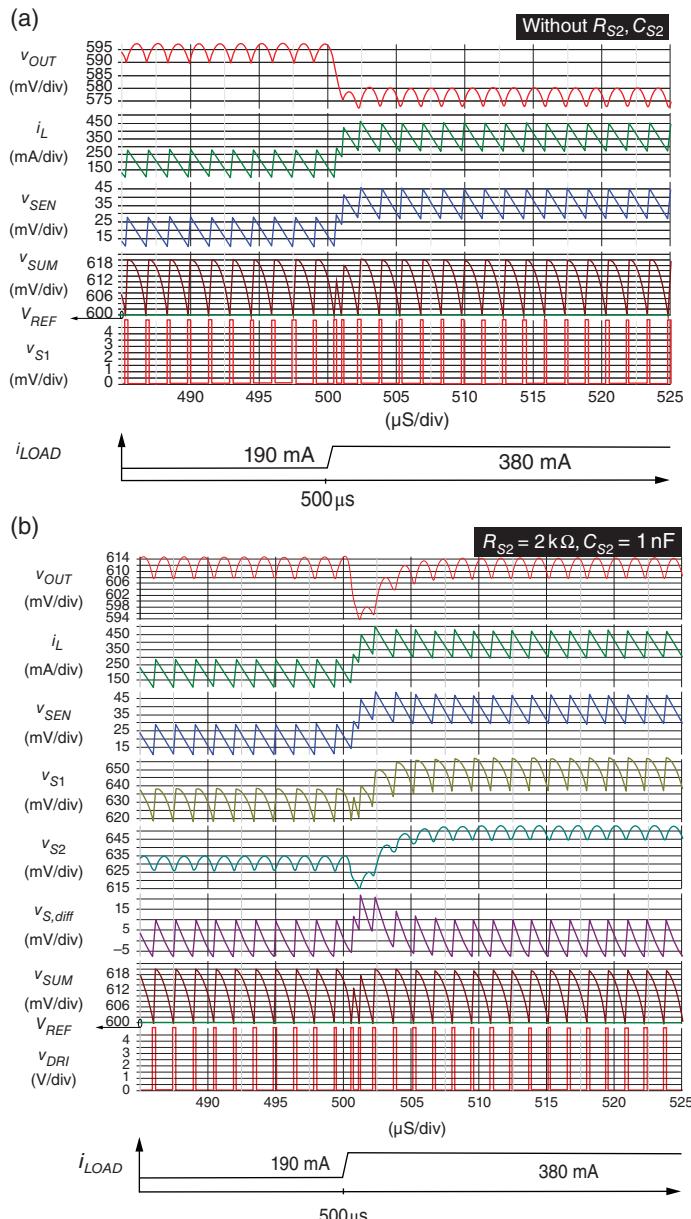
**Table 4.18** Basic specifications used in Example 4.8

$v_{IN}$	$v_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu$ H	100 m $\Omega$	4.7 $\mu$ F	0 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.19** The designing parameters and characteristics for different cases

Case	$R_{DCR}$	$R_S$	$C_S$	$R_{S2}$	$C_{S2}$	Characteristic
(a)	100 m $\Omega$	100 $\Omega$	470 nF	—	—	Voltage droop exists
(b)				2 k $\Omega$	1 nF	Voltage droop is removed
(c)				2 $\Omega$	1 $\mu$ F	Voltage droop is removed
(d)				0.2 $\Omega$	10 $\mu$ F	Unstable operation because of violation of Eq. (4.90)
(e)				2 M $\Omega$	1 pF	Voltage droop is removed
(f)				20 M $\Omega$	0.1 pF	The function of $R_{S2}$ and $C_{S2}$ is degraded by leakage current

impedance of  $100 \text{ M}\Omega$ , the leakage current is  $1/5$  of the current flowing through  $R_{S2}$ . In other words, the leakage current is  $1/4$  of the current flowing through  $C_{S2}$ . This ratio is so large that the filtering function of  $R_{S2}$  and  $C_{S2}$  is degraded. Therefore,  $v_{S2}$  extracts no DC component of  $v_{S1}$  and the droop of  $v_{OUT}$  is not removed. Last but not least, the droop of  $v_{S1}$  is caused by the droop of  $v_{OUT}$  through the conduction of  $C_{S2}$ . As a result, once the value of  $R_{S2}$  is increased for the decrease in value of  $C_{S2}$ , the leakage current should be carefully taken into consideration.



**Figure 4.58** Load transient response (a) without  $R_{S2}$  and  $C_{S2}$ , (b) with  $R_{S2} = 2 \text{ k}\Omega$  and  $C_{S2} = 1 \text{ nF}$ , (c) with  $R_{S2} = 2 \Omega$  and  $C_{S2} = 1 \mu\text{F}$ , (d) with  $R_{S2} = 0.2 \Omega$  and  $C_{S2} = 10 \mu\text{F}$ , (e) with  $R_{S2} = 2 \text{ M}\Omega$  and  $C_{S2} = 1 \text{ pF}$ , (f) with  $R_{S2} = 20 \text{ M}\Omega$  and  $C_{S2} = 0.1 \text{ pF}$

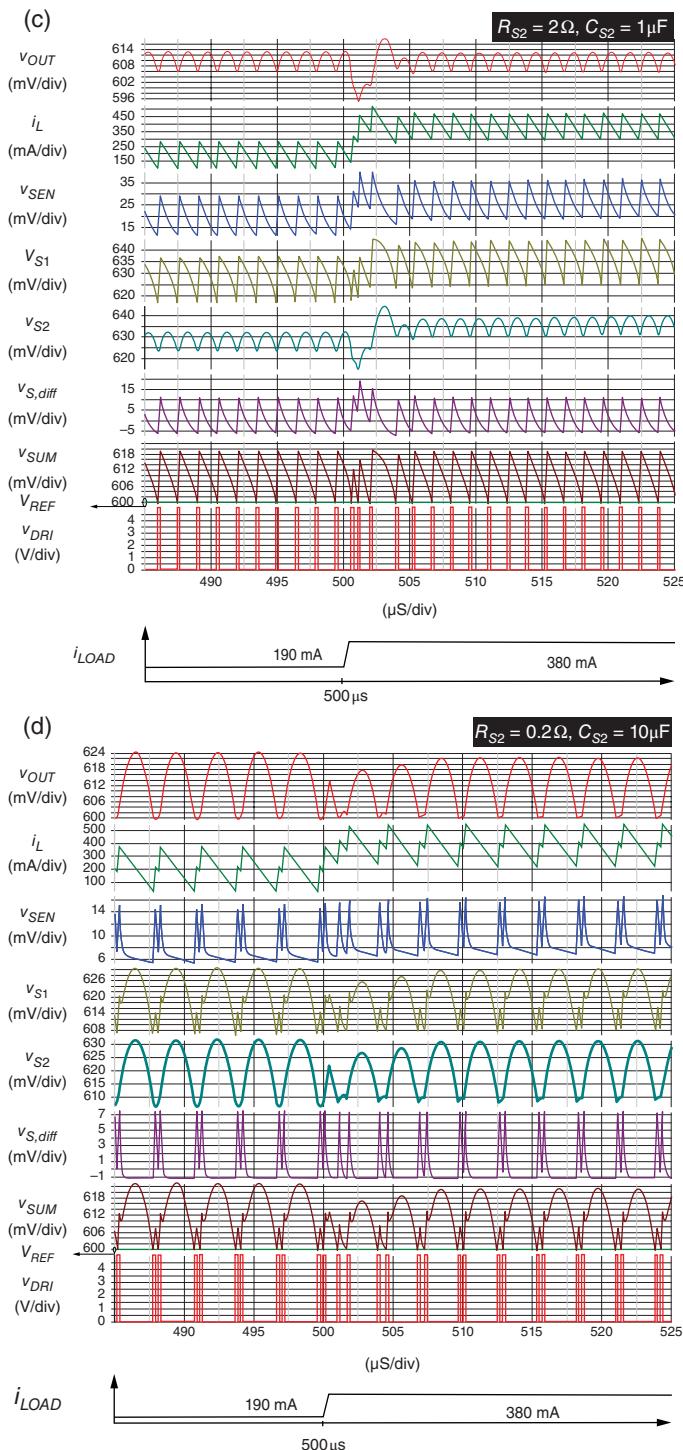


Figure 4.58 (Continued)

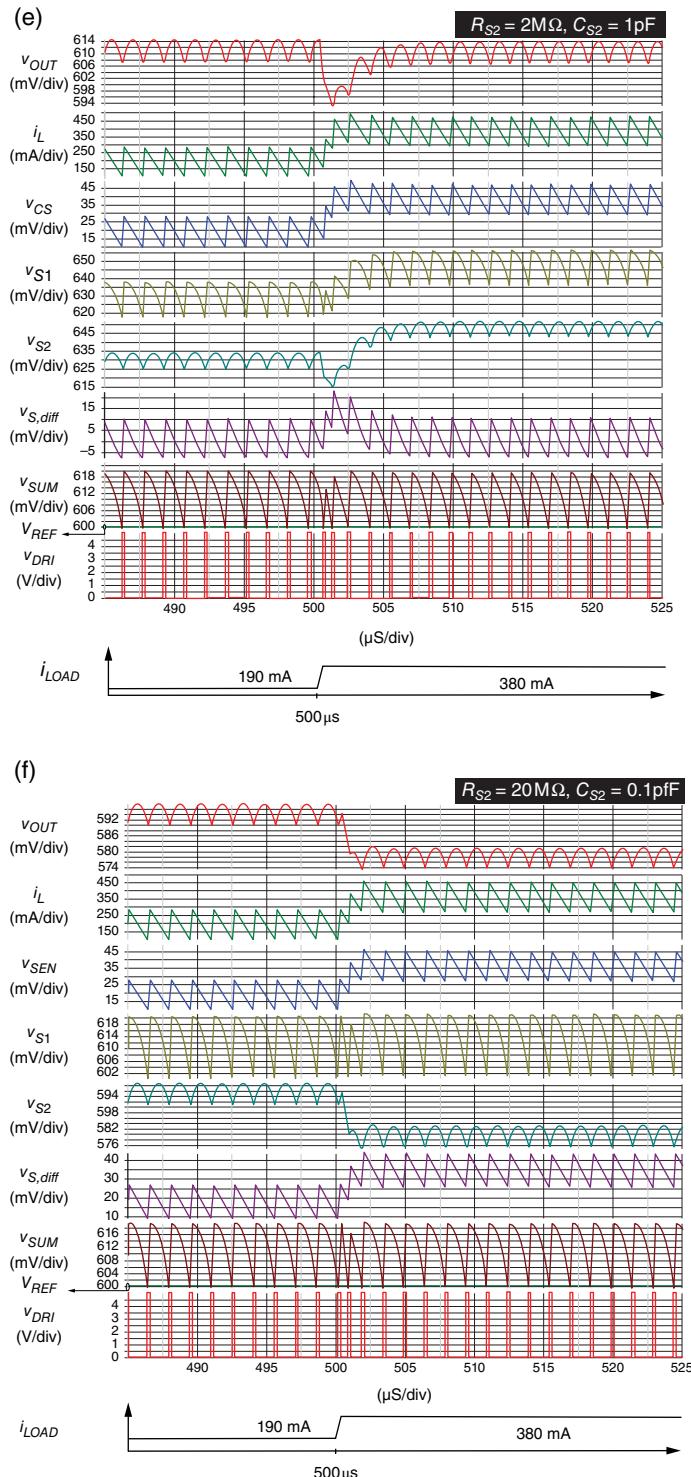
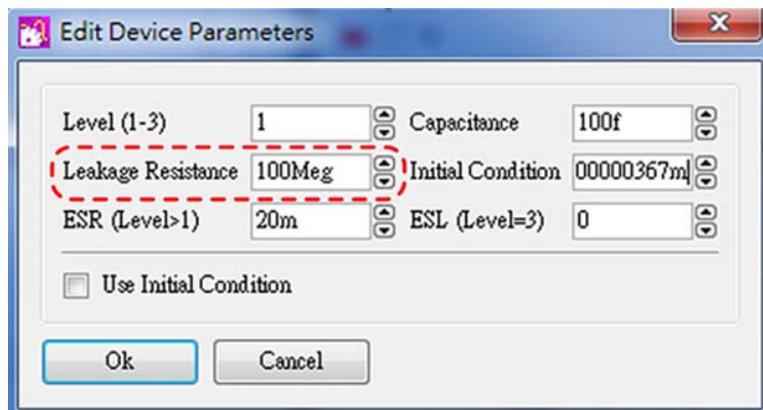


Figure 4.58 (Continued)



**Figure 4.59** SIMPLIS window to edit the device parameters of  $C_{S2}$

### SIMPLIS Setting

Figure 4.60 illustrates the setup circuit via SIMPLIS corresponding to Figure 4.52.

This circuit is composed of a comparator, on-time pulse generator, non-overlap circuit, high-side switch, low-side switch, inductor, parallel RC-filter, output capacitor, and output load. The high-side switch and low-side switch are parallel with a diode to form an equivalent MOSFET device.

Figure 4.61 provides a zoomed-in view of the partial portion of Figure 4.60. Critical devices should be set, and Figure 4.62 illustrates the setting windows for these parameters.

Figure 4.62(a) is a window to edit the device parameter of the output capacitor, whose value is  $4.7 \mu\text{F}$ . “Level” is set as “2” to activate the value setting of ESR. However, to demonstrate the parallel RC-filter function of Examples 4.7 and 4.8, the value of ESR is  $0 \text{ m}\Omega$ .

Figure 4.62(b) is a window to edit the device parameter of the inductor, whose value is  $4.7 \mu\text{H}$ . “Series Resistance” is  $R_{DCR}$ , set as  $100 \text{ m}\Omega$ .

Figure 4.62(c) is a window to edit the device parameter of the change in loading conditions. “Wave shape” is selected first as “One pulse,” then “Time/Frequency” can be set for the time of load change. In this setting, the loading condition remains at light load until the time is  $500 \mu\text{s}$ , and then changes from light to heavy load in  $2 \mu\text{s}$ . In turn, the loading condition remains at heavy load until the time is  $550 \mu\text{s}$ , and then changes from heavy to light load in  $2 \mu\text{s}$ . Besides, the value of the load change is set by adjusting the value of “Resistance load” in Figure 4.61.

Figure 4.62(d) is a window to edit the device parameters of three inputs summing the circuit. According to Eq. (4.77), the gain for  $v_{S1}$  and  $v_{S2}$  is 1 and  $-1$ , respectively, for extra  $v_{S,diff}$ . According to Eq. (4.77), the gain for  $v_{OUT}$  is 1. Besides, “Input Resistance” is set as  $1\text{G}$  to avoid the load effect.

Block (e) in Figure 4.61 includes the resistances and capacitances of a parallel RC-filter. Different values are set in Examples 4.7 and 4.8.

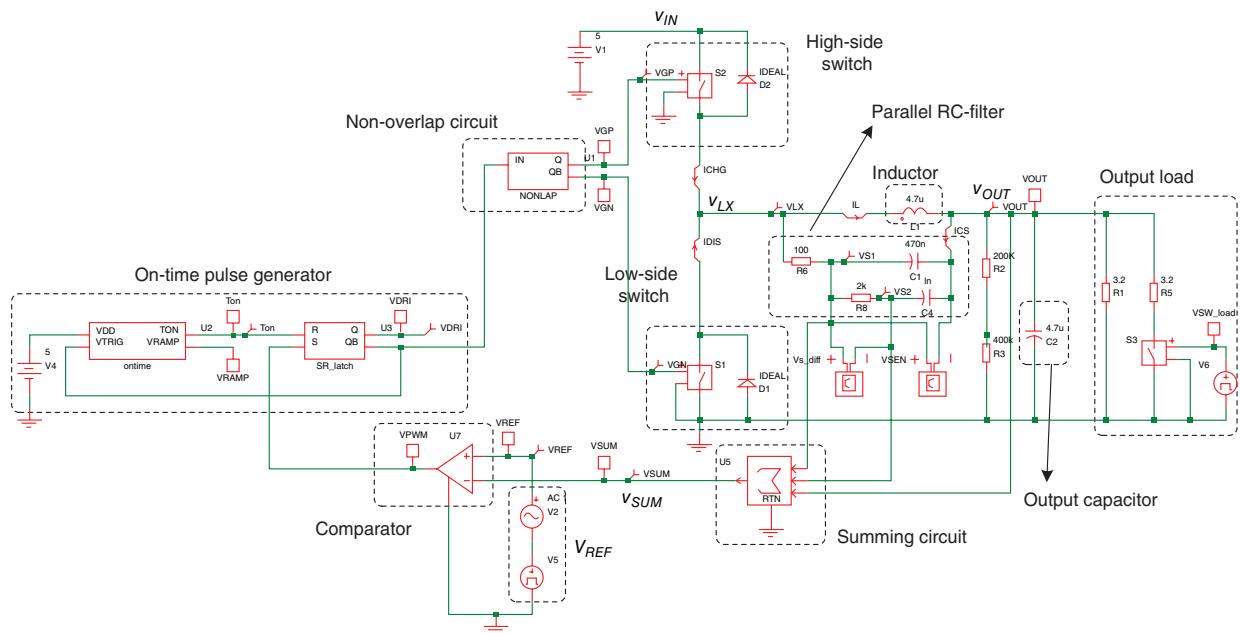
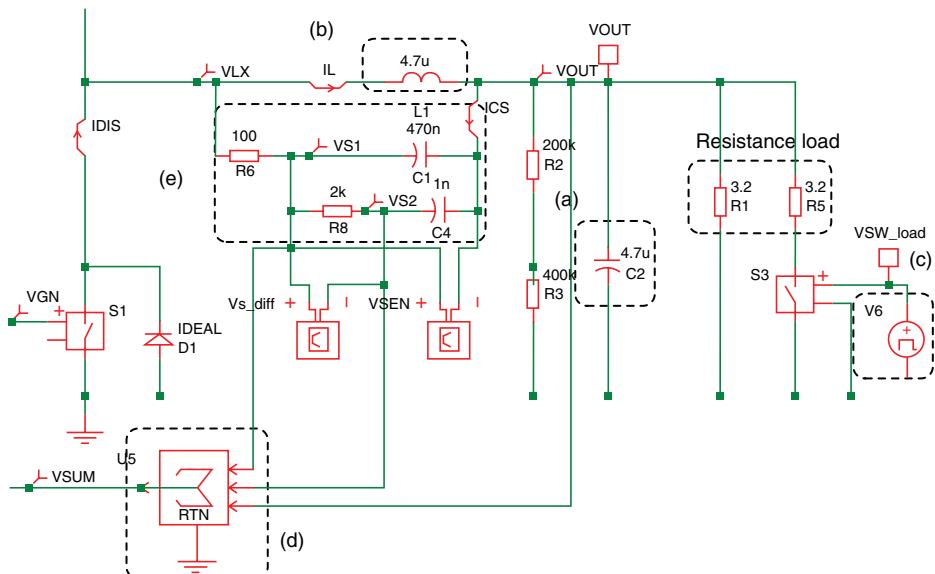
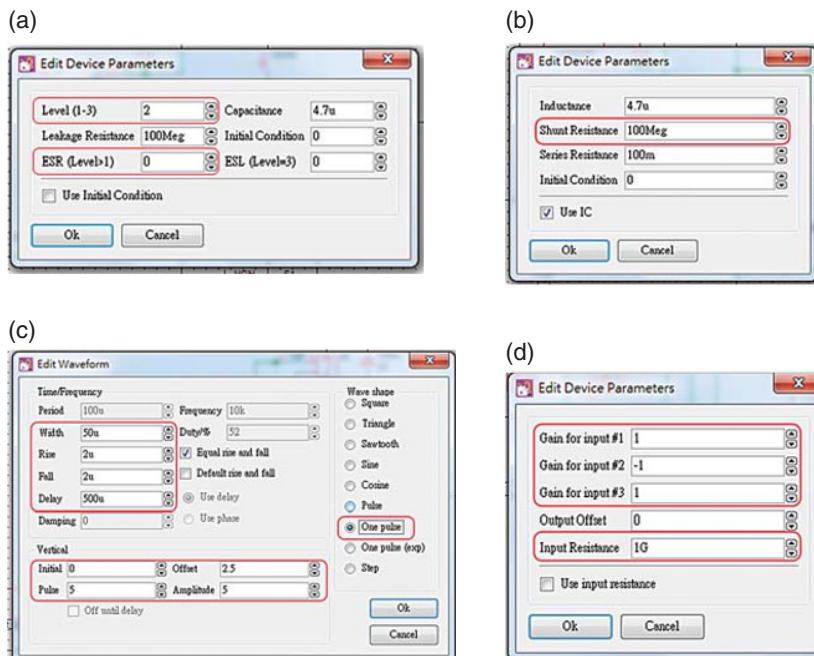


Figure 4.60 Setup circuit via SIMPLIS



**Figure 4.61** Zoom-in views of output filter, RC-filters, summing circuit, and loading



**Figure 4.62** Windows for setting device parameters. (a) Output capacitor. (b) Inductor. (c) Output load. (d) Summing circuit

**Example 4.9:** This example shows the improvement of transient response in case of using VCVS if we change the values of  $R_S$  and  $C_S$

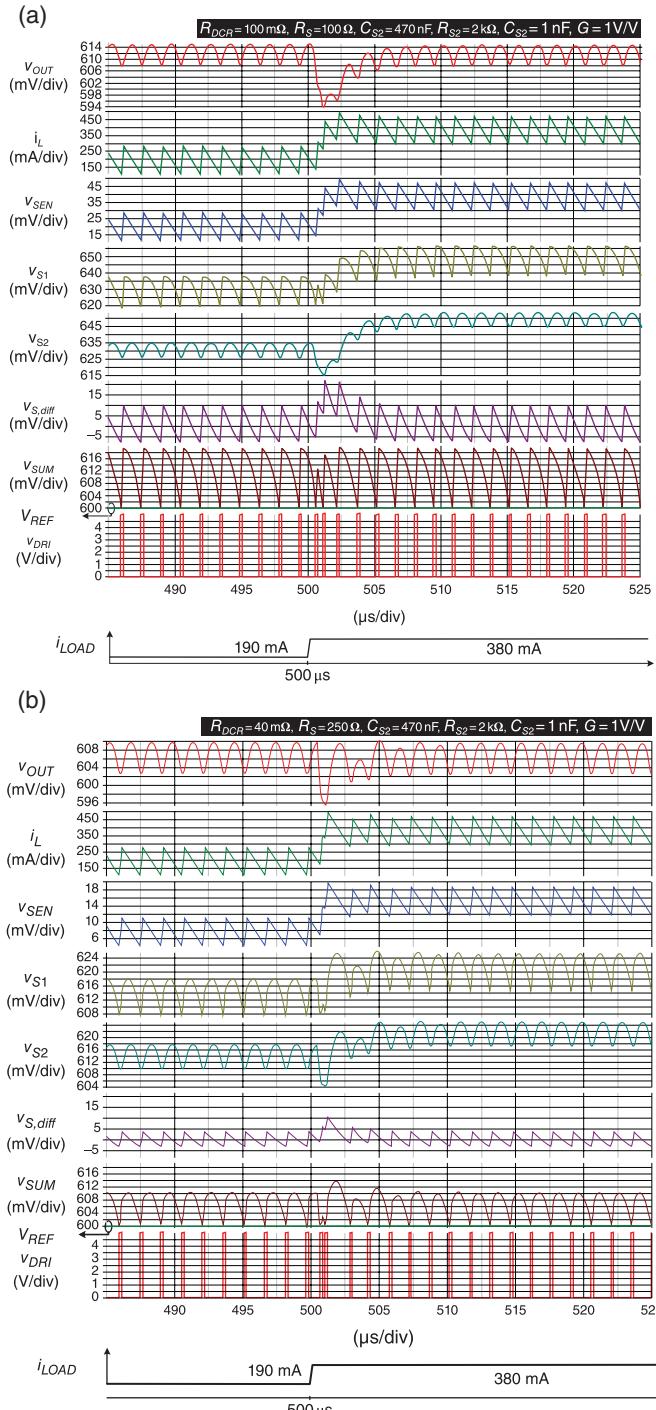
This example discusses Eq. (4.82) for use of the VCVS in Figure 4.54. When different inductors are used, the values of  $R_S$  and  $C_S$  are designed according to the value of  $R_{DCR}$  as expressed in Eq. (4.89) for good transient response. In this example we have seven cases; the same value of  $C_S$  and different values of  $R_S$  to match the different values of  $R_{DCR}$ . According to the criterion of Eq. (4.88) for stability, the increase in  $G$  is designed for smaller values of  $R_S$  and  $R_{DCR}$ . Table 4.20 lists the basic specifications. Here,  $R_1 = 0 \text{ k}\Omega$  and  $R_2 = 400 \text{ k}\Omega$ ,  $v_{OUT}$  is equal to  $v_{FB}$ . Table 4.21 lists the parameters for seven cases in which the values of  $R_{DCR}$ ,  $R_S$ , and  $G$  are different. Based on the stable operation in case (a), the waveforms of the other cases are observed in Figure 4.63. By comparing cases (a) and (b), the smaller value of  $R_S$  leads to a lower  $v_{SEN(AC),pp}$ . As a result,  $v_{SUM}$  is composed of less information on  $v_{SEN(AC)}$ , although the transient response is improved. In case (c), the much smaller value of  $R_S$  ( $20 \text{ m}\Omega$ ) is designed for  $R_{DCR}$  of  $500 \Omega$ . The  $v_{SEN(AC),pp}$  in case (c) can be expected to become smaller than

**Table 4.20** Basic specifications used in Example 4.9

$v_{IN}$	$v_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu\text{H}$	100 m $\Omega$	4.7 $\mu\text{F}$	0 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.21** The designing parameters and characteristics for different cases

Case	$R_{DCR}$ (m $\Omega$ )	$R_S$	$C_S$	$R_{S2}$	$C_{S2}$	$G$	$v_{SEN(AC),pp}$ (mV)	Characteristic
(a)	100	100 $\Omega$	470 nF	2 k $\Omega$	1 nF	1	17	
(b)	40	250 $\Omega$				1	6.8	<ul style="list-style-type: none"> <li>Smaller <math>v_{SEN(AC)}</math></li> <li>Faster transient response</li> </ul>
(c)	20	500 $\Omega$				1	3.4	<ul style="list-style-type: none"> <li>Smaller <math>v_{SEN(AC)}</math></li> <li>Fast transient response</li> <li>Worse aberration between <math>v_{SUM}</math> and <math>i_L</math></li> </ul>
(d)	20	500 $\Omega$				5	3.4	<ul style="list-style-type: none"> <li>Similar to (a) because of same <math>G \cdot v_{S,diff}</math></li> </ul>
(e)	10	1 k $\Omega$				1	1.7	<ul style="list-style-type: none"> <li>Serious aberration between <math>v_{SUM}</math> and <math>i_L</math></li> <li>Unstable because of too small value of <math>v_{SEN(AC)}</math> relative to ripple of <math>V_{FB}</math></li> </ul>
(f)	10	1 k $\Omega$				2	1.7	<ul style="list-style-type: none"> <li>Similar to (c) because of same <math>G \cdot v_{S,diff}</math></li> </ul>
(g)	10	1 k $\Omega$				4	1.7	<ul style="list-style-type: none"> <li>Similar to (b) because of same <math>G \cdot v_{S,diff}</math></li> </ul>
(h)	10	1 k $\Omega$				10	1.7	<ul style="list-style-type: none"> <li>Similar to (a) because of same <math>G \cdot v_{S,diff}</math></li> </ul>



**Figure 4.63** Load transient response with different  $v_{SEN(AC),pp}$  and  $G \cdot v_{S,diff}$  owing to different  $R_{DCR}$ ,  $R_S$ , and  $G$ . (a)  $G = 1$ ,  $R_{DCR} = 100 \text{ m}\Omega$ , and  $R_S = 100 \Omega$ . (b) Faster transient response caused by smaller  $v_{SEN(AC)}$ . (c) Worse aberration between  $v_{SUM}$  and  $i_L$ . (d) Similar to (a) because of same  $G \cdot v_{S,diff}$ . (e) Unstable because of too small value of  $v_{SEN(AC)}$  relative to ripple of  $V_{FB}$ . (f) Similar to (c) because of same  $G \cdot v_{S,diff}$ . (g) Similar to (b) because of same  $G \cdot v_{S,diff}$ . (h) Similar to (a) because of same  $G \cdot v_{S,diff}$ .

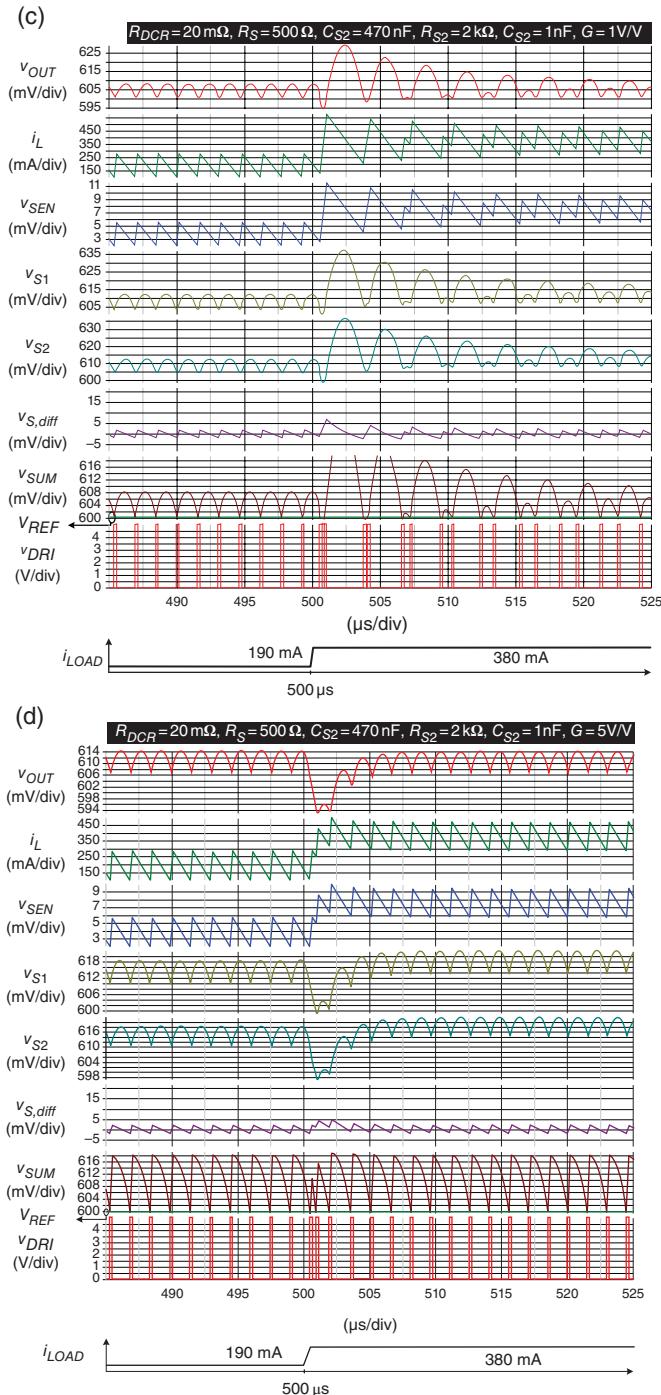


Figure 4.63 (Continued)

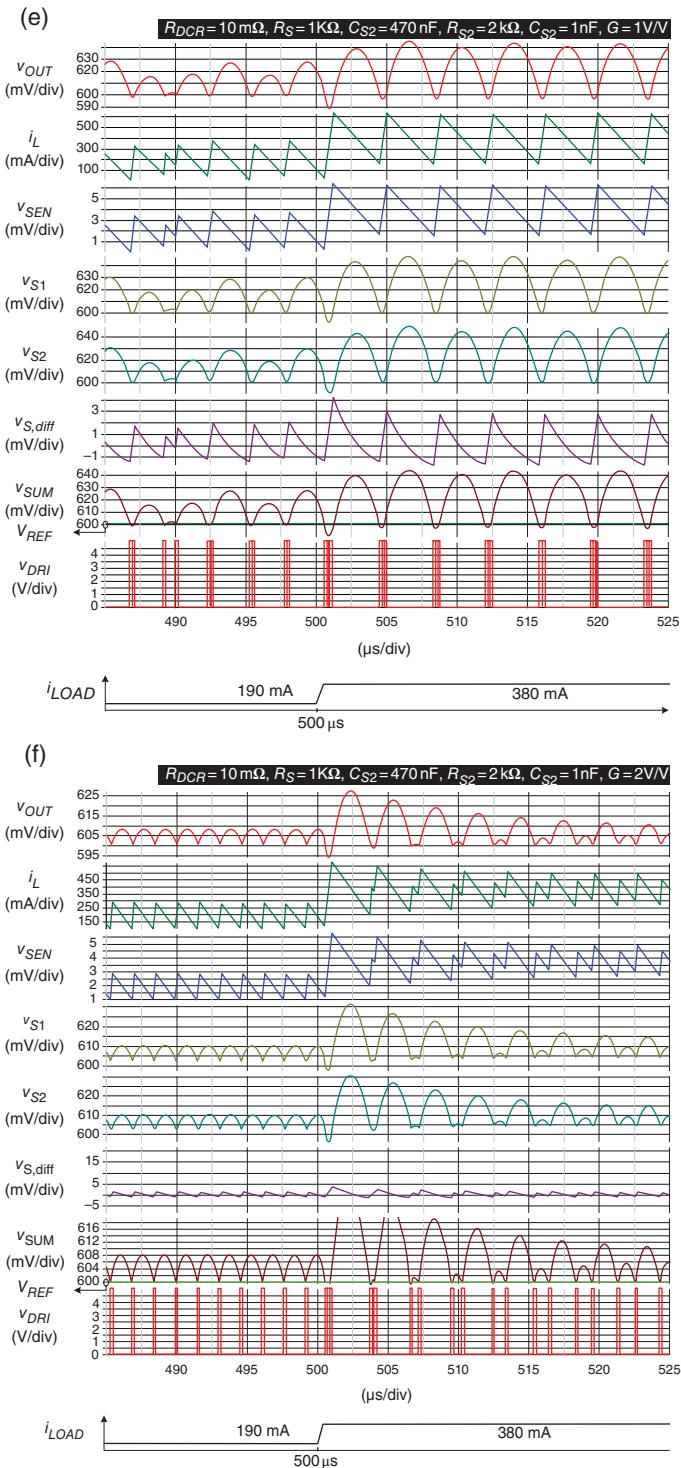


Figure 4.63 (Continued)

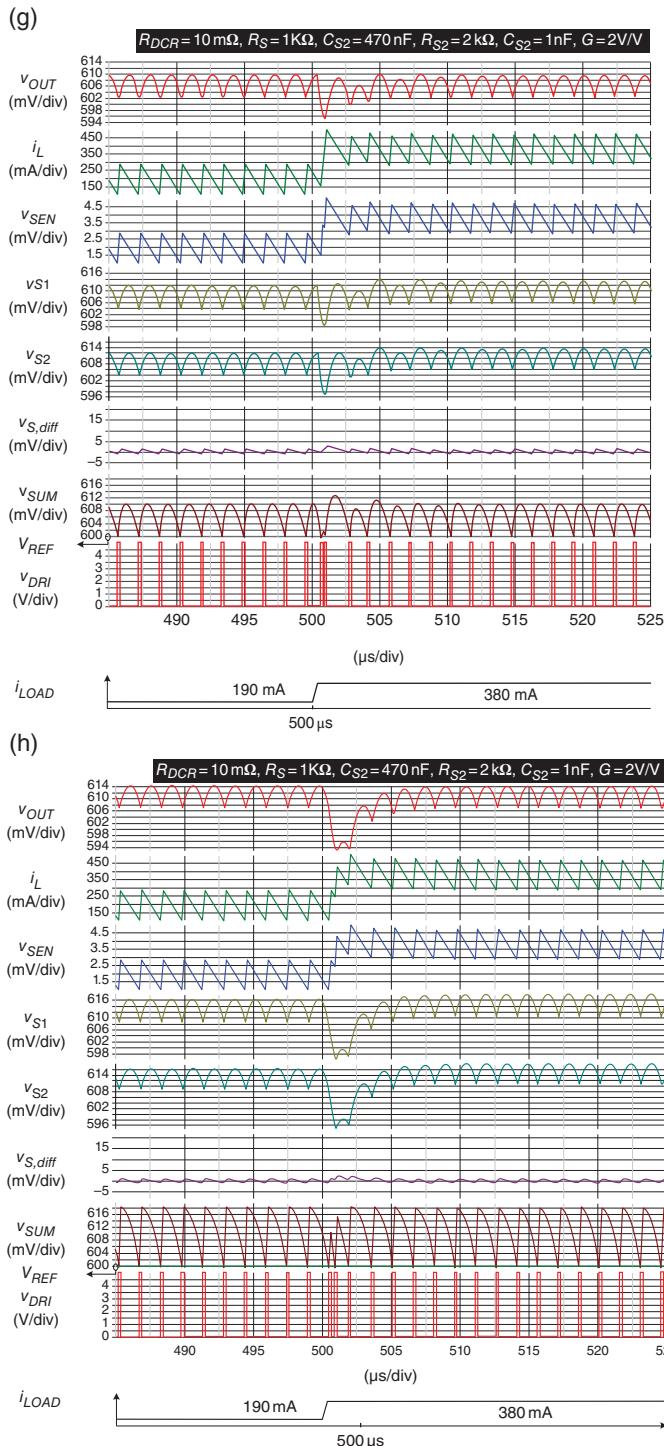


Figure 4.63 (Continued)

that in case (b). Figure 4.63(c) shows unstable operation because of an insufficient amount of information on  $v_{SEN(AC),pp}$ . In other words, the criterion in Eq. (4.88) does not hold. To stabilize the operation, the value of  $G$  is increased from 1 to 5 V/V to amplify the value of  $v_{S,diff}$  in case (d). Comparing (a) and (d),  $v_{SEN(AC),pp}$  shows a 1/5 change with a 1/5 change in the value of  $R_S$ . With the five-time change in  $G$ , the ripples of  $v_{S,diff}$  in case (a) and (d) are almost similar. Consequently, both cases perform almost similarly in terms of stable operation and transient response. The remaining cases can be analyzed similarly. The operations in cases (e) and (f) are also unstable according to the criterion. Even though the values of  $v_{SEN(AC),pp}$  are different in different cases, the final value of  $v_{S,diff}$  determines whether the operation is stable or not. Consequently, cases (a), (d), and (h) perform similarly. Cases (b) and (g) also perform similarly, while cases (c) and (f) perform similarly.

**Example 4.10:** The transient response is influenced by opposite trends among  $v_{OUT}$  and  $i_L$ .

As mentioned previously, the variations in  $v_{OUT}$  and  $i_L$  at different loading conditions exhibit opposite trends. Therefore, the transient response is inhibited. This simulation reveals that the transient response is influenced by the different values of  $G$ , resulting in a gain in amplifier  $v_{S,diff}$  because  $v_{S,diff}$  represents the AC component of  $i_L$ . Table 4.22 lists the basic specifications. In this simulation,  $R_1 = 0 \text{ k}\Omega$ ,  $R_2 = 400 \text{ k}\Omega$ , and  $v_{OUT}$  is equal to  $v_{FB}$ .

Table 4.23 lists the parameters of three cases, and Figure 4.64 shows the relative waveforms.

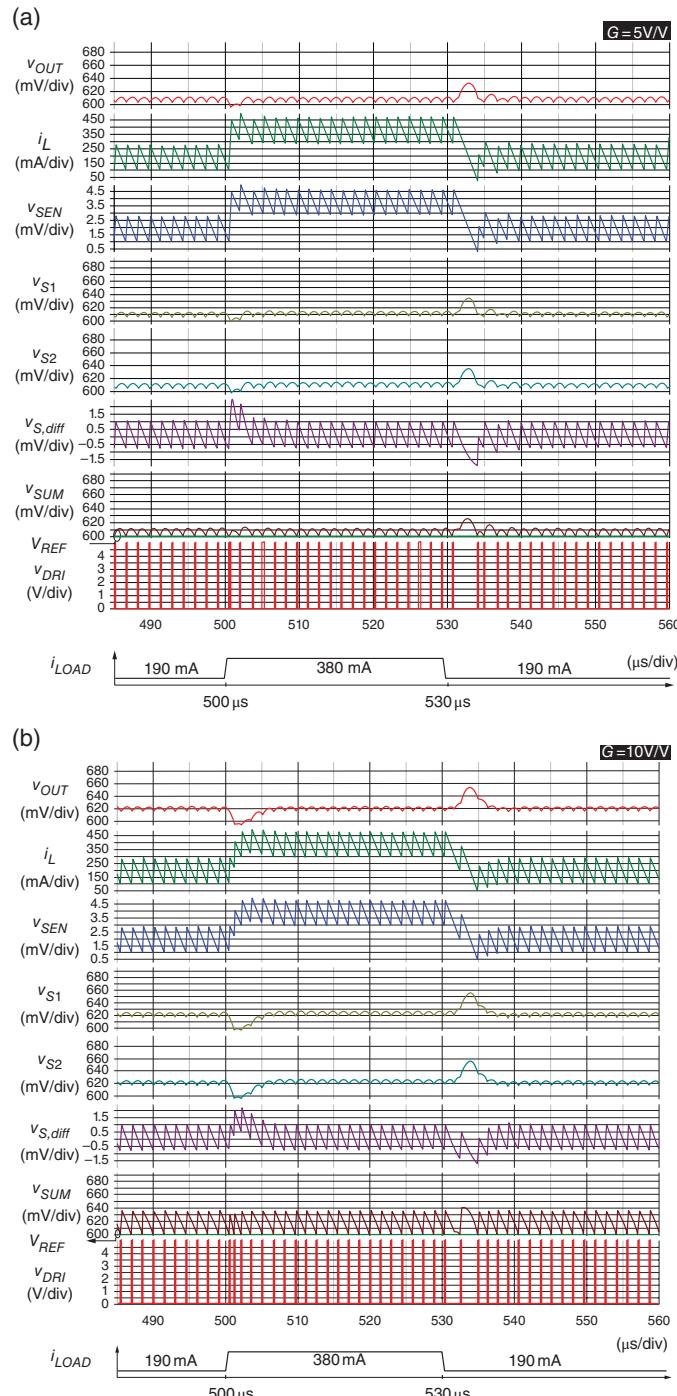
Figure 4.64(a)–(c) shows that  $v_{SEN(AC),pp}$  has the same value in all cases because of the same values of  $R_S$  and  $C_S$ . The values of  $G$  in all cases are 5, 10, and 5. The ripple of  $v_{SUM}$  has values of 12, 36, and 90 mV. The larger the ripple of  $G \cdot v_{S,diff}$ , the worse the transient response. The worst case (case (c)) shows that the converter responds to the changing load until the ratio of the variation in  $v_{OUT}$  over the ripple of  $G \cdot v_{S,diff}$  is sufficiently large. Moreover, the on-time and off-time periods are not extended during light to heavy and heavy to light loads, respectively, because that ratio is not evident. In conclusion, although the extra gain in  $G$  can enhance the stability, the ratio of the tolerated variation in  $v_{OUT}$  of the ripple of  $G \cdot v_{S,diff}$  should be carefully designed to obtain a suitable transient response.

**Table 4.22** Basic specifications used in Example 4.10

$v_{IN}$	$v_{OUT}$	$V_{REF}$	$L$	$R_{DCR}$	$C_{OUT}$	$R_{ESR}$	$L_{ESL}$	$T_{ON}$	$f_{SW}$
5 V	600 mV	600 mV	4.7 $\mu$ H	100 m $\Omega$	4.7 $\mu$ F	0 m $\Omega$	0 nH	180 ns	660 kHz

**Table 4.23** The designing parameters and characteristics

	$R_{DCR}$	$R_S$	$C_S$	$R_{S2}$	$C_{S2}$	$G$	$v_{SEN(AC),pp}$	$G \cdot v_{S,diff}$ (mV)
(a)	10 mΩ	1 kΩ	470 nF	2 kΩ	1 nF	5	1.7 mV	12
(b)						10		36
(c)						50		90



**Figure 4.64** Load transient response with different  $G \cdot v_{S,diff}$  because of different  $G$ . (a)  $G = 5$ . (b)  $G = 10$ . (c)  $G = 50$

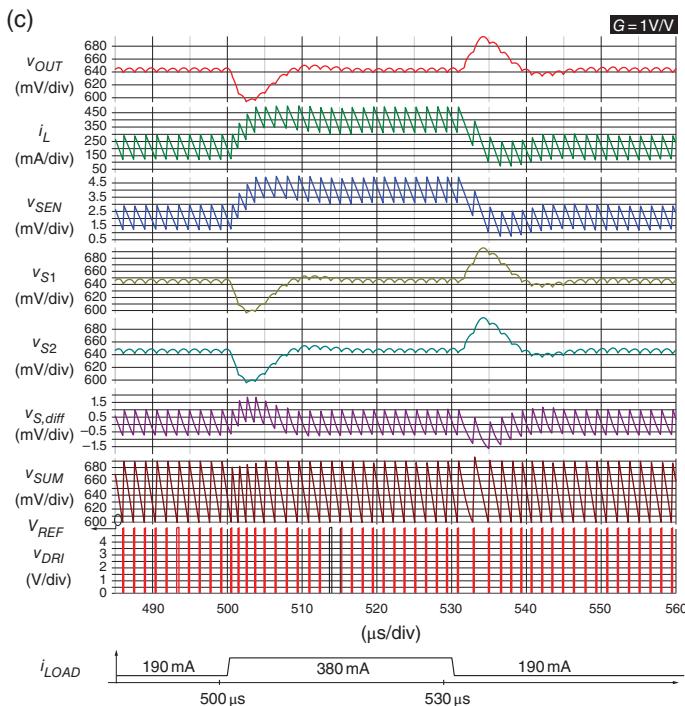


Figure 4.64 (Continued)

### SIMPLIS Setting

Figure 4.65 illustrates the setup circuit via SIMPLIS corresponding to Figure 4.54.

This circuit is composed of a comparator, on-time pulse generator, non-overlap circuit, high-side switch, low-side switch, inductor, parallel RC-filter, output capacitor, and output load. The high-side switch and low-side switch are parallel with a diode to form an equivalent MOSFET device.

Figure 4.66 provides a zoomed-in view of a partial portion of Figure 4.65. There are critical devices to be set, and Figure 4.67 illustrates the setting windows for these parameters.

Figure 4.67(a) is a window to edit the device parameter of the output capacitor, whose value is  $4.7 \mu\text{F}$ . “Level” is set as “2” to activate the value setting of ESR. To demonstrate the parallel RC-filter function of Examples 4.9 and 4.10, the value of ESR is  $0 \text{ m}\Omega$ .

Figure 4.67(b) is a window to edit the device parameter of the inductor, whose value is  $4.7 \mu\text{H}$ . “Series Resistance” is  $R_{DCR}$ , set as  $100 \text{ m}\Omega$ .

Figure 4.67(c) is a window to edit the device parameter of the change in loading conditions. “Wave shape” is first selected as “One pulse,” then “Time/Frequency” can be set for the time of load change. In this setting, the loading condition remains at light load until the time is  $500 \mu\text{s}$ , and then changes from light load to heavy load in  $2 \mu\text{s}$ . In turn, the loading condition remains at heavy load until the time is  $530 \mu\text{s}$ , and then changes from heavy load to light load in  $2 \mu\text{s}$ . Besides, the value of the load change is set by adjusting the value of “Resistance load” as labeled in Figure 4.66.

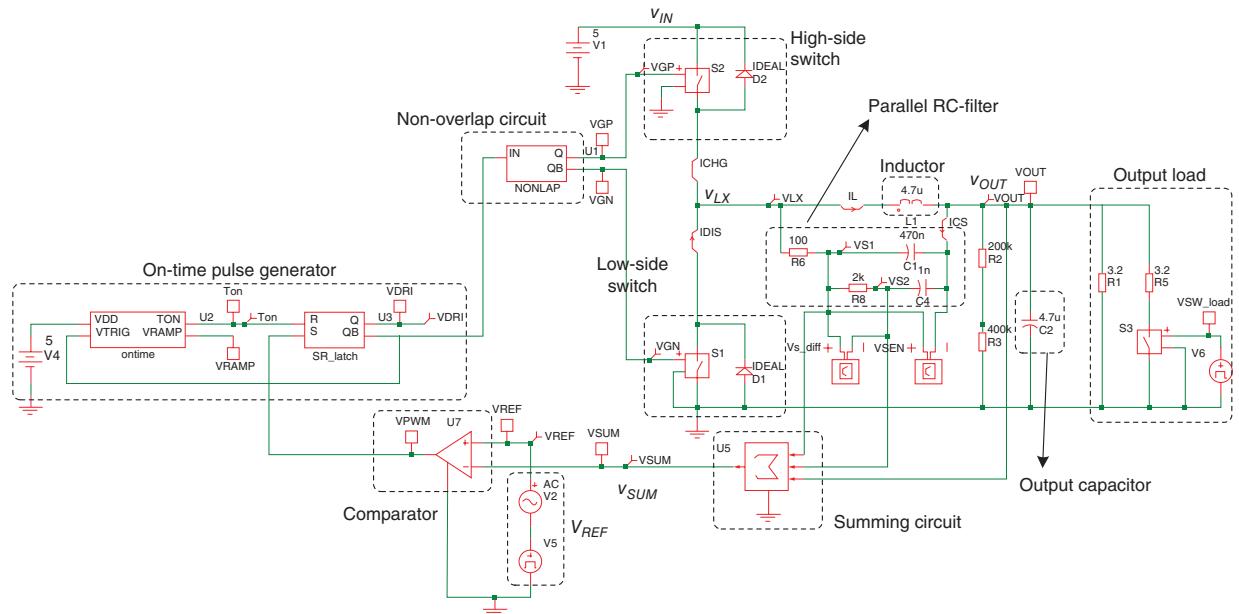
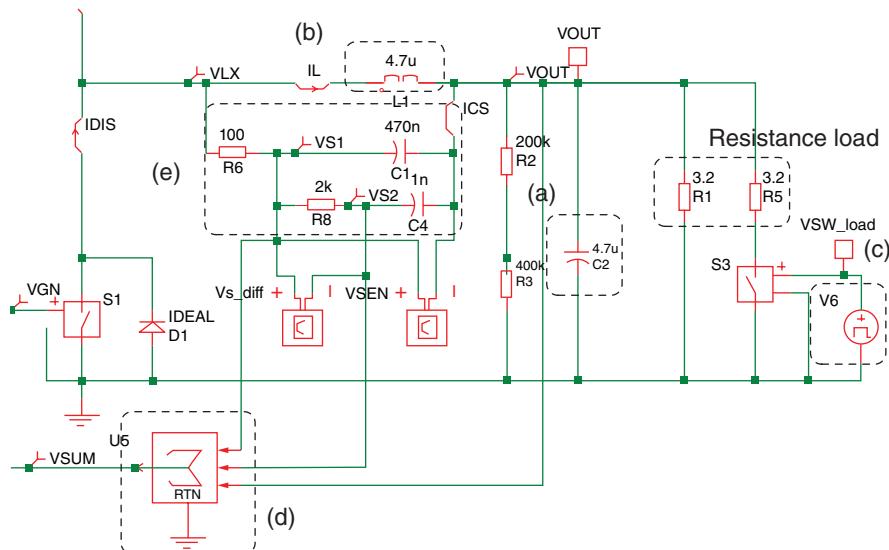
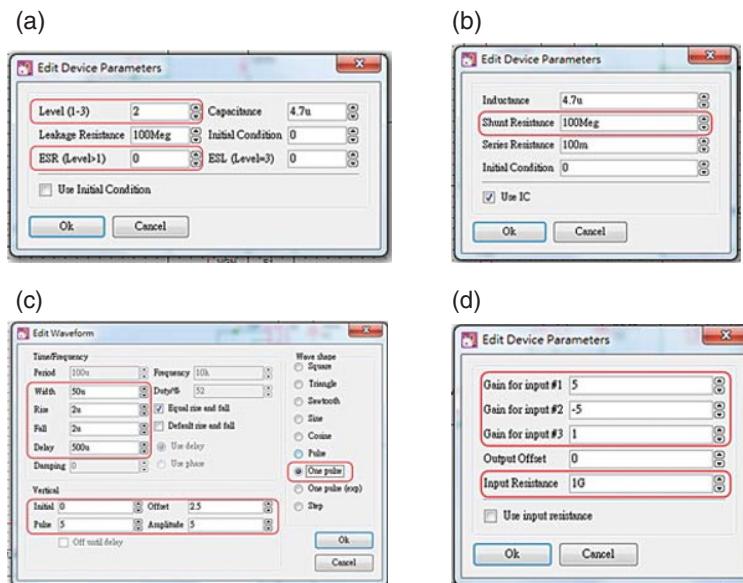


Figure 4.65 Setup circuit via SIMPLIS



**Figure 4.66** Zoom-in views of output filter, RC-filters, summing circuit, and loading



**Figure 4.67** Windows for setting device parameters. (a) Output capacitor. (b) Inductor. (c) Output load. (d) Summing circuit

Figure 4.67(d) shows the window to edit the device parameter of a three-input summing circuit. According to Eqs. (4.76) and (4.81), the extra gain of  $G$  from VCVS indicates that the gains for  $v_{S1}$  and  $v_{S2}$  are set to have opposite sign and the same value. Taking  $G = 5$ , for example, the gains for  $v_{S1}$  and  $v_{S2}$  are 5 and -5, respectively. Different values are set in

Examples 4.9 and 4.10. According to Eq. (4.77), the gain for  $v_{OUT}$  is 1. Besides, “Input Resistance” is set as 1G to avoid the load effect.

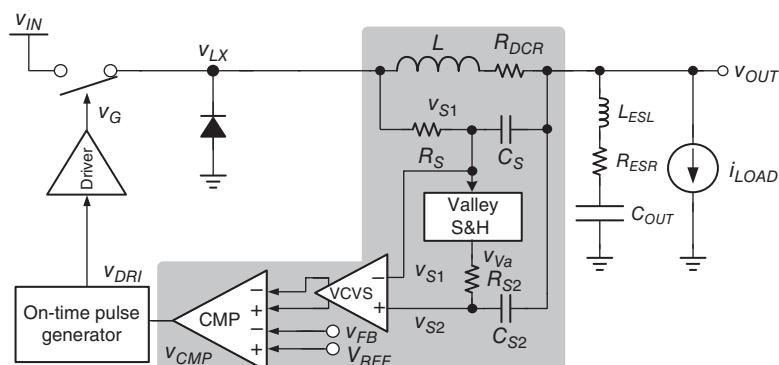
Block (e) in Figure 4.61 includes the resistances and capacitances of a parallel RC-filter. Different values are set in Examples 4.9 and 4.10.

#### 4.3.2.6 CF-type6 (Parallel RC-Filter with Accurate Regulation)

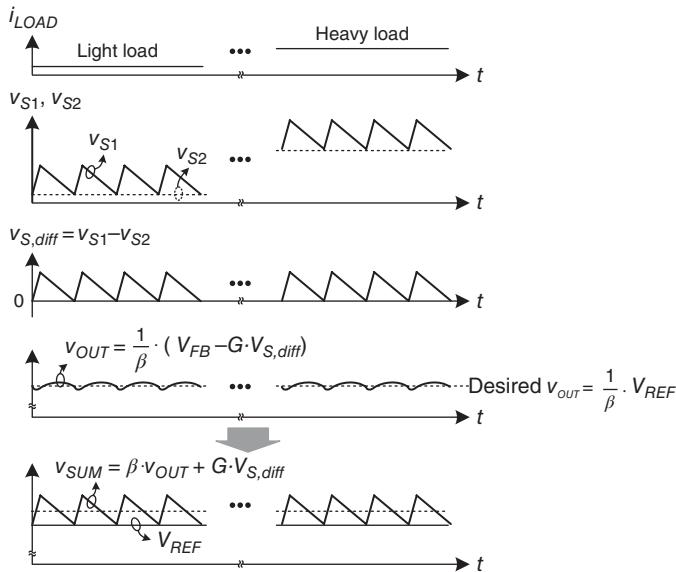
The CF-type6 is introduced in this subsection; it utilizes an extra CF path to ensure stability and achieve accurate regulation simultaneously. Figure 4.68 shows the structure of the CF-type6 modified from the structure shown in Figure 4.54. An additional valley detector is used. Figure 4.69 shows the operating waveform of the converter with CF-type6. The first RC-filter composed of  $R_S$  and  $C_S$  generates  $v_{S1}$ , which contains information from  $v_{OUT}$  and  $i_L$ . The valley detector and second RC-filter process  $V_{S1}$  to extract AC information from  $i_L$ , that is, remove the DC information from  $v_{OUT}$  and  $i_L$ . The valley sample-and-holder (S&H) uses  $v_{S1}$  to generate  $v_{VA}$ , which is equal to the valley value of  $v_{S1}$ . The second RC-filter, composed of  $R_{S2}$  and  $C_{S2}$ , processes  $v_{VA}$  to generate  $v_{S2}$ , which can also represent the valley value of  $v_{S1}$ . Afterward, the high-frequency noise can be suppressed. When  $v_{S1}$  and  $v_{S2}$  are fed into the VCVS, the differential output voltage of VCVS, that is,  $v_{S,diff2}$ , is determined, as expressed in Eq. (4.91).  $v_{S,diff}$  can represent information from the AC component of  $i_L$ .

$$v_{S,diff2} = G \cdot v_{S,diff} = G \cdot (v_{S1} - v_{S2}) \quad (4.91)$$

In the comparison of  $v_{S,diff}$  of CF-type5 shown in Figure 4.53 and  $v_{S,diff}$  of CF-type6 shown in Figure 4.68, the average  $v_{S,diff}$  of CF-type6 is not zero, whereas the valley of  $v_{S,diff}$  of CF-type6 is zero. In other words, for CF-type6, Figure 4.68 shows that the valleys of  $v_{FB}$  and  $v_{SUM}$  are equal. No voltage offset between the valleys of  $v_{FB}$  and  $V_{REF}$  is observed because the valley of  $v_{SUM}$  is regulated at  $V_{REF}$  through the comparator in the feedback loop. In the comparison of



**Figure 4.68** Current-sensing technique with two pairs of RC-filters, valley S&H, and VCVS linear amplifier



**Figure 4.69** Operating waveform showing no voltage droop and offset voltage at  $v_{OUT}$

$v_{OUT}$  of CF-type5 shown in Figure 4.53 and  $v_{OUT}$  of CF-type6 shown in Figure 4.68, the voltage droop can be removed by the extra valley S&H in CF-type6.

#### 4.3.3 Comparison of On-Time Control with an Additional Current Feedback Path

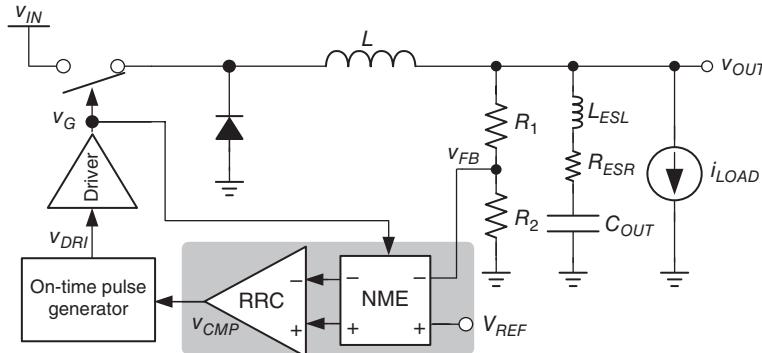
Table 4.24 lists the design issues of various types of ripple-based converters with additional CF. The voltage droop, offset voltage, and characteristics of CF-type1 to CF-type6 are compared. For the simplest method, CF-type1 can be used. However,  $R_S$  in series with the power delivery path aggravates power loss. CF-type2 is also easy to design, but the integral function of  $R_{LPF}$  and  $C_{LPF}$  slows down the transient response. CF-type3, which uses  $R_S$  and  $C_S$  in parallel with the inductor, can prevent aggravation of the transient response. The values of  $R_S$  and  $C_S$  are designed by considering pole/zero cancellation for optimum transient response. Based on the structure of CF-type3, an additional  $R_{S2}$  is added to CF-type4 to improve the flexible AVP function. The AVP features of voltage droop at different loading conditions can ensure a fast transient response. Based on the structure of CF-type3, an additional RC-filter composed of  $R_{S2}$  and  $C_{S2}$  is added to CF-type5 to remove the voltage droop of several applications that require good load regulation. However, the offset voltage still exists. Based on the structure of CF-type5, an extra valley S&H is added to CF-type6 to remove the offset voltage and ensure accurate regulation. In conclusion, a trade-off between achieving additional functions and sacrificing complex structures exists in an on-time control with additional CF path. Designers can select the most suitable structure based on the specifications listed in Table 4.25. This table lists

**Table 4.24** Characteristics of different structures

Structure	Voltage droop	Offset voltage	Characteristics
CF-type1	●	●	<ul style="list-style-type: none"> <li>• A series <math>R_S</math></li> <li>• Extra power loss because of <math>R_S</math></li> <li>• Easy to implement because of its simple structure</li> </ul>
CF-type2	●	●	<ul style="list-style-type: none"> <li>• An integral RC-filter</li> <li>• <math>R_{LPF}</math> and <math>C_{LPF}</math></li> <li>• Slow transient response because of the integral function</li> </ul>
CF-type3	●	●	<ul style="list-style-type: none"> <li>• Basic structure of parallel RC-filters</li> <li>• <math>R_{S2}</math> and <math>C_{S2}</math></li> </ul>
CF-type4	●	●	<ul style="list-style-type: none"> <li>• A parallel RC-filter and an additional <math>R_{S2}</math></li> <li>• <math>R_{S1}</math>, <math>R_{S2}</math>, and <math>C_{S1}</math></li> <li>• Voltage droop is adjustable for the AVP function</li> </ul>
CF-type5	—	●	<ul style="list-style-type: none"> <li>• Two sets of RC-filters</li> <li>• <math>R_{S1}</math>, <math>R_{S2}</math>, <math>C_{S1}</math>, and <math>C_{S2}</math></li> <li>• Voltage droop is removed to ensure good load regulation</li> </ul>
CF-type6	—	—	<ul style="list-style-type: none"> <li>• Two sets of RC-filters and an additional valley S&amp;H</li> <li>• <math>R_{S1}</math>, <math>R_{S2}</math>, <math>C_{S1}</math>, and <math>C_{S2}</math></li> <li>• Voltage droop is removed to ensure good load regulation</li> <li>• Offset voltage is removed to ensure accurate regulation</li> </ul>

**Table 4.25** Issues and results of different structures

Table	Structure	Discussing issue	Result
Table 4.8	CF-type1	Different $R_S$	Different voltage droop
Table 4.10	CF-type3	Different $C_S$	Different amplitudes of $v_{SEN}$ have an influence on stability
Table 4.12	CF-type3	Different $C_S$	Different pole locations lead to different transient responses
Table 4.14	CF-type3	Same time-constant value but different $C_S$ and $R_S$	The influence on $v_{OUT}$ and power loss of RC-filters
Table 4.17	CF-type4	Different $R_{S2}$	The capability of LPF and the different levels of distortion of $v_{S,diff}$
Table 4.19	CF-type4	Different $C_{S2}$ and $R_{S2}$	Too large $C_{S2}$ influences the time constant of $C_S$ and $R_S$ . The extra phase delay leads to unstable operation
		Same time-constant value	Too large $R_{S2}$ with small $C_{S2}$ suffers the problem of leakage current
Table 4.21	CF-type4	Different amplitude of $v_{SEN}$ and $v_{S,diff}$	Stability
Table 4.23	CF-type4	Different amplitude of $v_{S,diff}$	Transient response



**Figure 4.70** On-time control with RRC and NME to ensure stable operation even if a small  $R_{ESR}$  is used

the issues of the various techniques and simulation results of the relative simulation. These issues and results also provide important hints for design.

#### 4.3.4 Ripple-Reshaping Technique to Compensate a Small Value of $R_{ESR}$

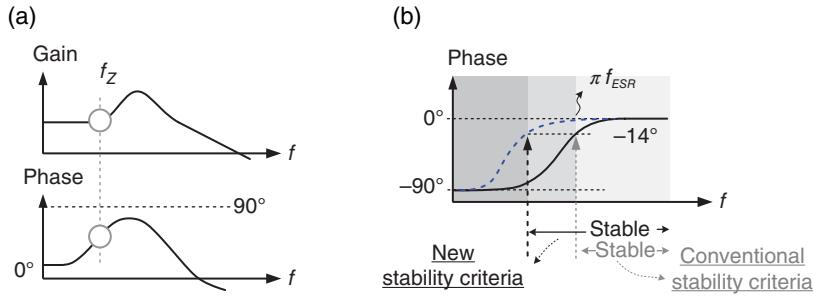
When  $R_{ESR}$  is small, extracting the inductor current ripple from the output voltage is difficult. The non-linear relationship between inductor current ripple and output voltage ripple causes sub-harmonic oscillation. Figure 4.70 shows the on-time control with ripple-reshaping technique, which includes ripple-recovered compensator (RRC) and noise margin enhancement (NME), to compensate for the small  $R_{ESR}$  effect.

The RRC technique with NME function is used to derive the ripple-reshaping function to compensate for the instability effect of a small  $R_{ESR}$ . The RRC provides a differentiation function by reversing the integration function of  $C_{OUT}$  and thus recovering the inductor current information. Moreover, the RRC determines the output DC level by comparing the feedback signal with the reference voltage. The NME is used to eliminate the ESL effect and increase the noise margin of the RRC technique.

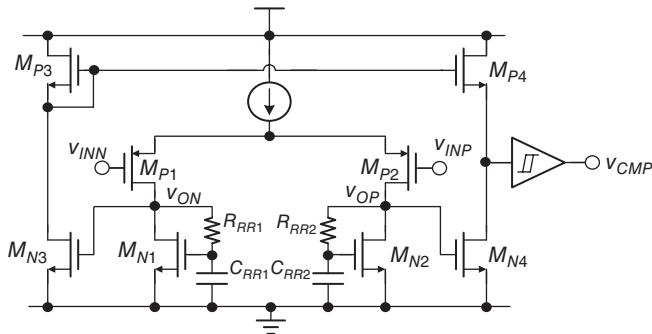
##### 4.3.4.1 RRC for Reversing the Integration Function by $C_{OUT}$

In Eq. (4.27), the conventional compensation technique utilizing  $R_{ESR}$  and  $C_{OUT}$  results in zero at the frequency of  $f_{ESR}$ . However, if  $R_{ESR}$  decreases because of the use of the MLCC, then the zero will move toward high frequencies. According to the analytical results shown in Figure 4.20, a high-frequency zero only has a slight effect on the boosting phase to increase stability. That is, the conventional compensation technique fails to stabilize the entire system. Therefore, the compensating zero generated by the RRC technique is used to boost the PM even without the ESR zero. Figure 4.71 shows that the compensating zero equivalently boosts the phase at approximately  $90^\circ$  so that the conventional stability criterion, as shown in Figure 4.20, can easily be achieved.

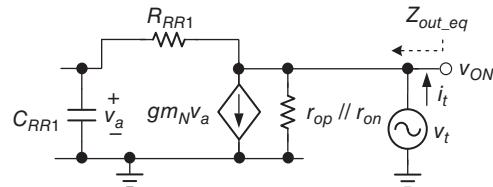
Figure 4.72 shows the circuit implementation of RRC. In the first stage of RRC, the input differential pair is composed of  $M_{P1}$  and  $M_{P2}$ , with the active load formed by N-MOSFETs



**Figure 4.71** (a) Phase lead effect caused by a zero can improve the phase margin. (b) Phase lead effect caused by the RRC technique can increase system stability when a small ESR is used



**Figure 4.72** Circuit implementation of RRC



**Figure 4.73** Small signal model of the first stage of RRC

( $M_{N1}$  and  $M_{N2}$ ), resistors ( $R_{RR1}$  and  $R_{RR2}$ ), and capacitors ( $C_{RR1}$  and  $C_{RR2}$ ). As a result, the RRC can generate a pole/zero pair to ensure phase lead compensation. By contrast, in the second stage of RRC, the analog signals ( $v_{OP}$  and  $v_{ON}$ ) are converted to the digital control signal to obtain the full swing voltage  $v_{CMP}$ .

We use the common-mode small signal half-circuit model of the first stage of RRC, as shown in Figure 4.73, to derive the pole/zero pair. One test voltage  $v_t$  is applied to the  $v_{ON}$  node, and the corresponding current  $i_t$  flows into the circuit. As such, the equivalent output impedance  $Z_{out\_eq}$  can be determined.

Kirchhoff's current law (KCL) theorem is used to express  $i_t$  as follows:

$$i_t = \frac{v_t}{r_{on}/|r_{op}|} + \frac{v_t}{R_{RR1} + \frac{1}{sC_{RR1}}} + gm_N \cdot v_a \quad (4.92)$$

When  $r_o$  caused by the channel length modulation is neglected, the output impedance  $r_{out}$  is derived using Eq. (4.93) and the transfer function is derived using Eq. (4.94), where the pole and the zero locate at  $gm_n/C$  and  $1/RC$ , respectively:

$$r_{out} = \frac{v_t}{i_t} = \frac{1 + sR_{RR1}C_{RR1}}{gm_N + sC_{RR1}} \quad (4.93)$$

$$A_{DM} = \left| \frac{v_{OP} - v_{ON}}{v_{INP} - v_{INN}} \right| = \frac{gm_P}{gm_N} \left( \frac{1 + sR_{RR1}C_{RR1}}{1 + s\frac{C_{RR1}}{gm_N}} \right) \quad (4.94)$$

Consequently, if  $R_{RR1} \gg 1/gm_N$ , then the zero locates at lower frequencies compared with those of the pole. The differential input signal ( $v_{INP} - v_{INN}$ ) will have a phase lead compared with the differential output signal ( $v_{OP} - v_{ON}$ ).  $R_{D1}$  and  $C_{D1}$  are respectively set as 500 kΩ and 5 pF to ensure that the zero locates at approximately 63.6 kHz. The frequency response is shown in Figure 4.71. The compensating zero contributes a maximum phase delay of 14° located at approximately 200 kHz. Thus, the system operates at the lowest frequency of 200 kHz without the need for any large  $R_{ESR}$ . Meanwhile, the differential structure enhances the noise immunity and decreases the jitter and EMI effects. The RRC technique ensures stability, even though the 200 μF MLCC with only 1 mΩ ESR is used as the output capacitor.

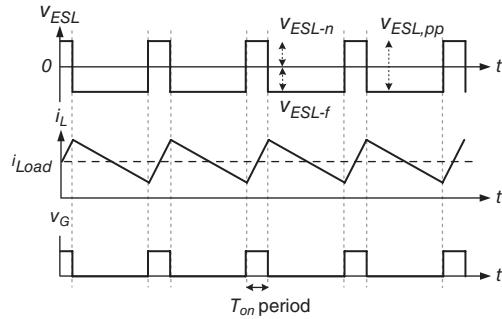
#### 4.3.4.2 NME for Tolerating $L_{ESL}$

The ESL in the output capacitor is another factor used to induce the distortion of the feedback voltage signal. The ESL effect on the output voltage ripple that influences the differential function of D-RRC expressed in Eq. (4.8) is rewritten as in Eqs. (4.95) and (4.96).

$$\text{On-time phase: } v_{ESL-n} = v_{ESL}(t) = \frac{v_{IN} - v_{OUT}}{L} \cdot L_{ESL} \quad (4.95)$$

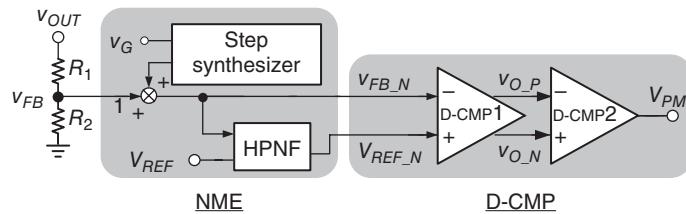
$$\text{Off-time phase: } v_{ESL-f} = v_{ESL}(t) = \frac{-v_{OUT}}{L} \cdot L_{ESL} \quad (4.96)$$

The voltage ripple caused by the ESL,  $v_{ESL}(t)$ , is constant during the on-time and off-time phases. As a result, the ESL voltage ripple forms a pulse waveform, as shown in Figure 4.74.

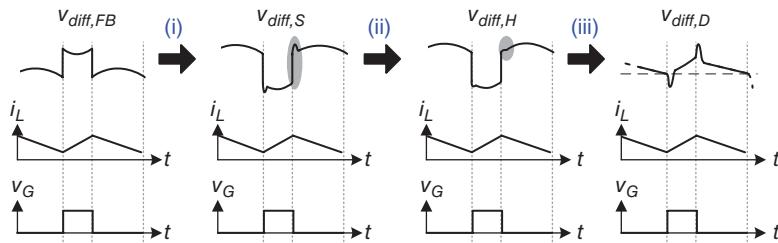


**Figure 4.74** ESL voltage ripple at the output voltage

(a)



(b)

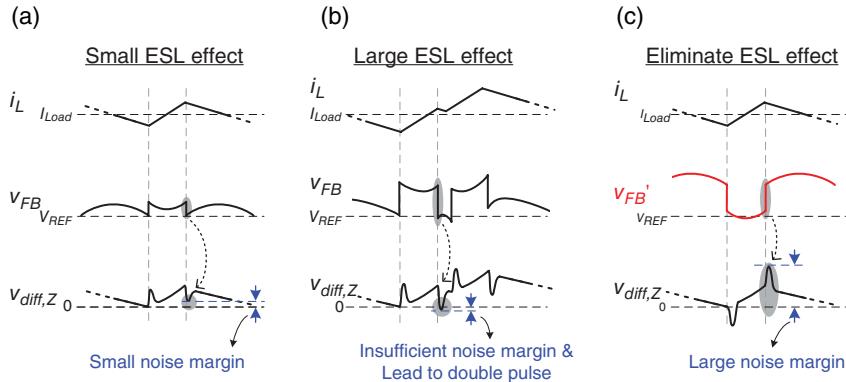


**Figure 4.75** (a) Structure of the NME circuit. (b) Detailed waveforms of each output

The peak-to-peak value is the summation of Eqs. (4.93) and (4.94):

$$v_{ESL,pp} = \frac{v_{IN}}{L} \cdot L_{ESL} \quad (4.97)$$

The voltage ripple value is proportional to  $v_{IN}$  and  $L_{ESL}$ . Generally,  $L_{ESL}$  is smaller than 1 nH. However, the ESL effect cannot be neglected if a high value of  $v_{IN}$  is commonly used to generate high power for commercial products. For example,  $v_{ESL,pp}$  is as large as 42 mV when  $v_{IN}$  is 21 V,  $L_{ESL}$  is 1 nH, and  $L$  is 2  $\mu$ H. The process of how the NME technique alleviates the ESL effect to improve D-RRC performance should be elucidated. Figure 4.75(a) shows the NME



**Figure 4.76** Function of the step generator. (a) Stable operation with a small ESL effect and without NME. (b) Unstable operation with a large ESL effect and without NME. (c) Stable operation with a large ESL effect and with NME

circuit, which consists of a step synthesizer and a high-frequency noise filter (HFNF). The differential voltage at different stages is defined as:

$$\begin{cases} v_{diff,FB} = v_{FB} - V_{REF} \\ v_{diff,S} = v_{INP} - V_{REF} \\ v_{diff,H} = v_{INP} - v_{INN} \\ v_{diff,D} = v_{OP} - v_{ON} \end{cases} \quad (4.98)$$

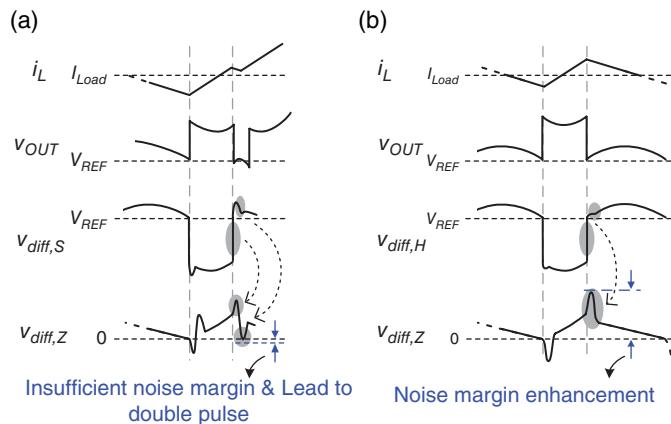
Figure 4.75(b) shows a simple waveform to illustrate the operation. Steps (i), (ii), and (iii) represent the corresponding functions of the (i) step synthesizer, (ii) HFNF, and (iii) RRC. Each function is described in detail as follows.

Figure 4.76(a), (b) indicates the necessity of NME through a comparison of the small  $L_{ESL}$  and the large  $L_{ESL}$ , respectively. In case of a small  $L_{ESL}$ , the down-stepping  $v_{ESL}$  at the beginning of the off-time period results in an undershoot of the differential signal  $v_{diff,D}$  after the D-RRC process, but without the step generator circuit. The undershoot of the differential signal  $v_{diff,D}$  may decrease to less than 0 V because of the ESL effect. Moreover, the incorrect triggering effect at the beginning of the off-time period instantly decreases the system stability. In other words, the double-pulse phenomenon will occur. Figure 4.76(c) shows the functions of NME for D-RRC when a small ESR is used. The feedback voltage signal can be modified from the ESL step to its opposite step. Thus, the feedback voltage signal can be depicted equivalently to  $v_{INP}$ . As a result, an overshoot of the differential signal  $v_{diff,D}$  at the beginning of the off-time period significantly enhances the noise margin.  $v_{diff,D}$  is reshaped and is in phase with the inductor current after the overshoot. By contrast, the undershoot of the differential signal  $v_{diff,D}$ , which is distorted drastically at the beginning of the on-time period, does not need to be considered because the on-time period is innately defined by the on-time pulse generator.

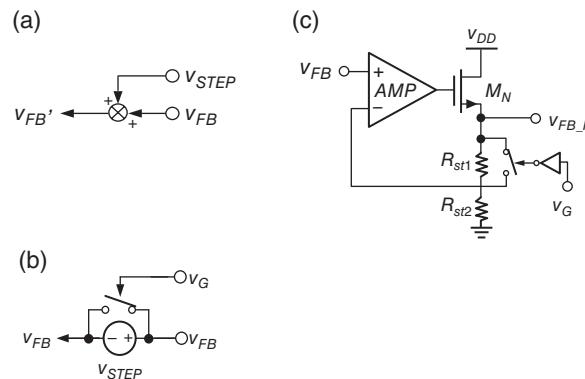
The opposite step must be generated and synchronized with the on-time period to eliminate the effect of  $v_{ESL}$ . However, the step generator has certain limitations in BW (bandwidth) and PM. If the PM is removed to obtain sufficient speed, then the differential output of the step

generator,  $v_{diff,S}$ , as shown in Figure 4.77, will lead to the double-pulse phenomenon after the D-RRC. The HPNF circuit couples the high-frequency variation from one input terminal to another terminal of the D-RRC to alleviate the defect of the step generator. Consequently,  $v_{FB}$  is pre-regulated by the NME circuit to enhance noise immunity and regulated by the D-RRC technique. The differential output signal of the D-RRC,  $v_{diff,D}$ , is reshaped from the phase delay  $v_{FB}$  and is in phase with the inductor current during the off-time period.

Finally, Figure 4.78(a) shows the implementation of the step synthesizer, with one example of how to synthesize the step waveform into the feedback signal. Figure 4.78(b) shows that the summation function is derived using a voltage source  $v_{STEP}$  and a switch, which is controlled by the gate control signal  $v_G$ . The voltage source can be generated by a capacitor. Figure 4.78(c) shows the implementation of another circuit with a buffer structure. By using the gate control signal  $v_G$ ,



**Figure 4.77** Waveforms illustrating the function of the NME and RRC techniques: (a) without HPNF and (b) with HPNF



**Figure 4.78** Implementation of the step synthesizer. (a) Concept of the step synthesizer. (b) Step synthesizer with a constant voltage source and a switch. (c) Step synthesizer with a buffer structure

the signals generated by the step synthesizer can be expressed in Eqs. (4.99) and (4.100). The magnitude of the step is equal to  $v_{FB'}(R_{st1}/R_{st2})$  and can be adjusted using  $R_{st1}$  and  $R_{st2}$ .

$$v'_{FB} = v_{FB} + v_{FB} \cdot \frac{R_{st1}}{R_{st2}}, \text{ when } v_{GP} \text{ is logic high} \quad (4.99)$$

$$v'_{FB} = v_{FB}, \text{ when } v_{GP} \text{ is logic low} \quad (4.100)$$

### 4.3.5 Experimental Result of Ripple-Reshaped Function

#### 4.3.5.1 Chip Micrograph

The on-time controlled buck converter with RRC and NME is fabricated using the UMC 0.35  $\mu\text{m}$  bipolar CMOS–DMOS (BCD) 40 V process. For applications with high conversion ratio and heavy driving current of 8 A, power MOSFETs are selected as discrete components. The high-side and low-side power MOSFETs are AOL1414 and AOL1412, respectively. The off-chip inductor and the capacitor are 1  $\mu\text{H}$  and 220  $\mu\text{F}$  (22  $\mu\text{F} \times 10$ ), respectively. Table 4.26 lists the specifications of this converter.

The nominal switching frequency is near 300 kHz. The output voltage ranges from 0.75 to 3.3 V, with the input voltage defined by the laptop adapter or the desktop power supply. In other words, the highest input voltage is 21 V. Figure 4.79 shows the chip micrograph with active silicon area measuring approximately 3.61  $\text{mm}^2$  including the test circuits. Table 4.27 describes the function of the sub-circuits.

Figure 4.80 shows the prototype of the on-time controlled buck converter with D-CAP and NME. Here, MLCCs are used as the output capacitor. The equivalent of the  $R_{ESR}$  value is calculated as nearly 1  $\text{m}\Omega$  according to the estimated output ripple ( $v_{pp}$ ) and Eq. (4.101):

$$\begin{aligned} v_{pp} &= v_{C_{OUT}} + v_{ESR} = \frac{v_{OUT}(1-D)}{8f_{SW}^2LC} + \frac{R_{ESR}v_{OUT}(1-D)}{f_{SW}L} \\ \Rightarrow R_{ESR} &= \left( v_{pp} - \frac{v_{OUT}(1-D)}{8f_{SW}^2LC} \right) \cdot \frac{f_{SW}L}{v_{OUT}(1-D)} \end{aligned} \quad (4.101)$$

**Table 4.26** Performance of the on-time controlled converter with RRC and NME techniques

Process	UMC 0.35 $\mu\text{m}$ BCD 40 V
Input voltage ( $v_{IN}$ )	5–21 V
Output voltage ( $v_{OUT}$ )	0.75–3.3 V
Supply voltage for chip ( $v_{DD}$ )	5 V
Load range ( $i_{Load}$ )	0.1–8 A
Inductor	1 $\mu\text{H}$
Output capacitor (MLCC)	220 $\mu\text{F}$ (22 $\mu\text{F} \times 10$ )
$R_{ESR}$	1 $\text{m}\Omega$
$L_{ESL}$	2.6 nH
Operation frequency	100–600 kHz
Output ripple	8–10 mV
Maximum efficiency	91%

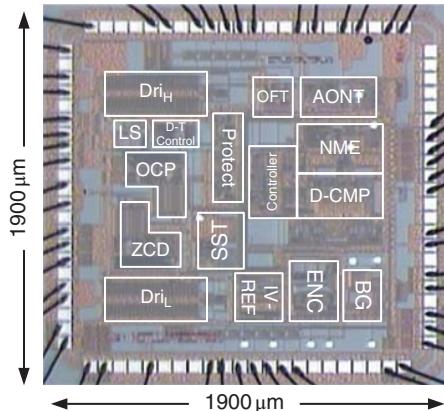


Figure 4.79 Chip micrograph

Table 4.27 Description of sub-circuits

RRC	Ripple-recovered compensator	ZCD	Zero-current detector
NME	Noise margin enhancement	OCP	Over-current protector
AONT	Adaptive on-time timer	PROTECTOR	Protect circuit
OFT	Minimum off-time timer	SST	Soft start
LS	Level shift	BG	Bandgap
D-T Control	Deadtime control	ENC	Enable controller
Dri <sub>H</sub>	High-side driver	IV-REF	Biassing current/reference voltage generator
Dri <sub>L</sub>	Low-side driver		

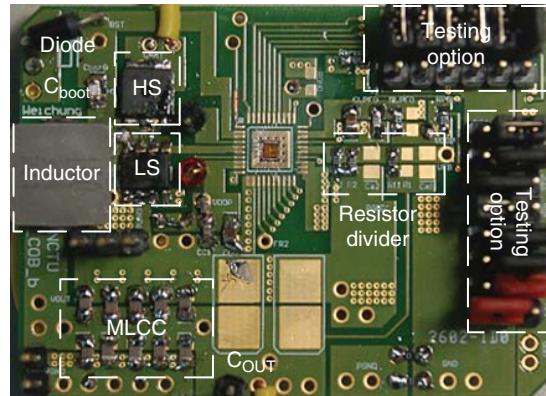
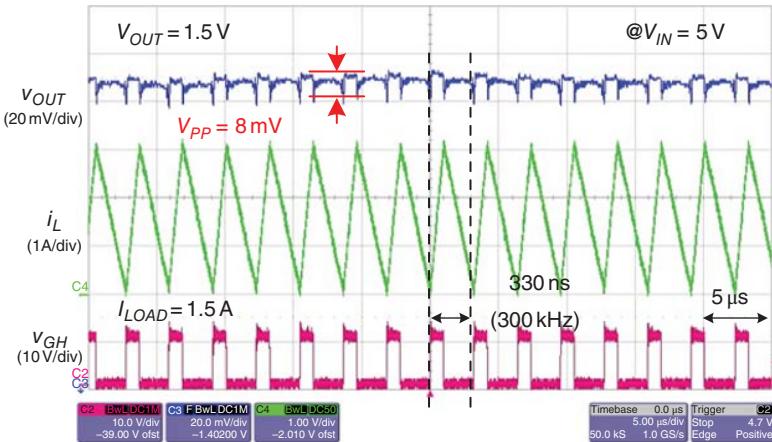


Figure 4.80 Prototype of the on-time controlled buck converter with RRC and NME

#### 4.3.5.2 Steady-State and Load Transient Response

Figure 4.81 shows the steady state of the experimental results;  $v_{IN}$  is 5 V and the output voltage  $v_{OUT}$  is 1.5 V when  $i_{Load}$  is 1.5 A and the switching frequency is 300 kHz.  $i_L$  is the inductor current.  $v_{GH}$  is the driving signal for the high-side MOSFET.  $R_{ESR}$  is approximately 1 mΩ and  $C_{OUT}$  is 220 μF (22 μF × 10) because of the use of MLCC. According to the conventional



**Figure 4.81** Waveforms in steady state with RRC and NME

stability criterion shown in Eq. (4.27), the switching frequency should be higher than 2 MHz. However, the experimental results show that the system stability is guaranteed even under a low switching frequency of 300 kHz because the RRC and NME techniques can reduce the limitation of the stability criterion. Thus, the switching loss can be significantly reduced. In particular, the voltage ripple at  $v_{OUT}$  can be smaller than 8 mV when  $v_{IN}$  is 5 V. Moreover, the output ripple and the inductor current are out of phase because of the MLCC.

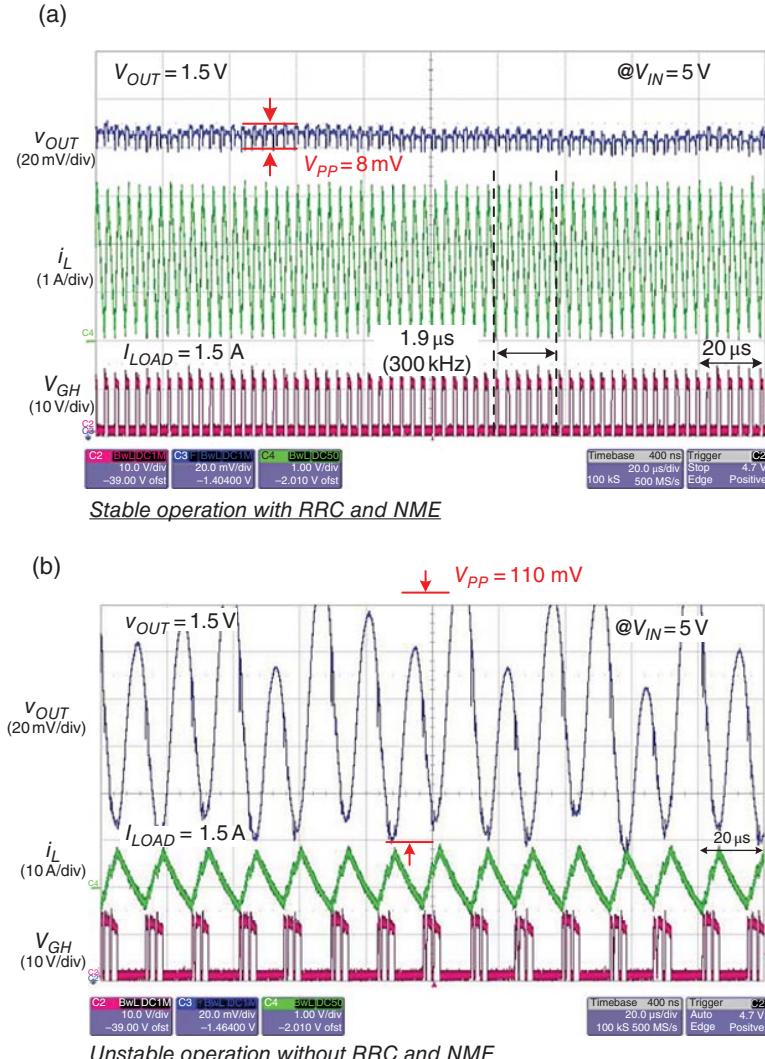
Figure 4.82 demonstrates the functions of RRC and NME when  $v_{IN}$  is 5 V and  $v_{OUT}$  is 1.5 V. Figure 4.82(a) shows the stable operation attributed to the implementation of RRC and NME. In contrast, with the external option set by the testing circuit, the sub-harmonic oscillation waveform occurs when RRC and NME are disabled, as shown in Figure 4.82(b). RRC contributes the phase lead to the feedback signal, which results in a similar performance that utilizes the output capacitor with a large ESR.

Furthermore, if  $R_{ESR}$  is approximately 1 mΩ, the effect of ESL is considerable when  $v_{IN}$  is higher than 15 V.  $v_{ESL}$  is 40 mV, as shown in Figure 4.83. The figure shows the contribution of NME if Figure 4.83(a) and (b) are compared. The system with only the RRC circuit has inadequate noise margins, such that  $v_{OUT}$  is marginally stable. Figure 4.83(c) shows the seriously unstable waveforms without the aid of the RRC–NME technique.

Figure 4.84 shows the waveforms of  $v_{OUT}$  and the inductor current  $i_L$  operating in the CCM when the load current  $i_{Load}$  steps up from 1 to 8 A, or vice versa. Here,  $v_{IN}$  is 15 V and  $v_{OUT}$  is 1.5 V. Consequently, the switching frequency is 300 kHz. Undershoot and overshoot voltages are 20 and 38 mV, respectively. The transient recovery times are 20 and 25 μs, respectively. Figure 4.85 shows the waveforms operating in the DCM at light loads. The switching frequency  $f_{SW}$  is scaled down to 78 kHz to enhance efficiency, which is an advantage of the on-time control for high efficiency at light loads. Obviously, system stability can be guaranteed when the output operates under different loading conditions because of the implementation of RRC and NME.

#### 4.3.5.3 Comparison with Other Techniques

Table 4.28 lists the comparison among prior literature in the design of constant on-time controlled DC/DC converters. The output ripple has been effectively reduced because of using the

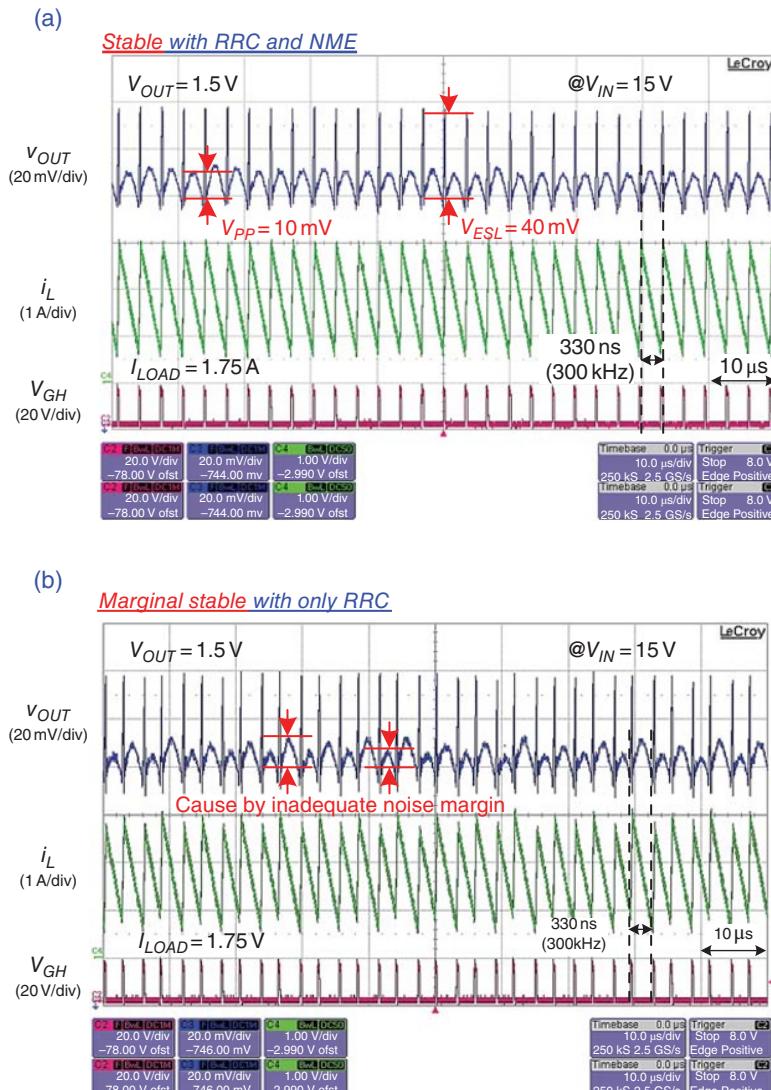


**Figure 4.82** (a) Stable waveforms attributed to the implementation of RRC and NME at  $v_{IN} = 5 \text{ V}$ ,  $v_{OUT} = 1.5 \text{ V}$ . (b) Unstable waveforms in the on-time controlled buck converter without RRC and NME at  $v_{IN} = 5 \text{ V}$ ,  $v_{OUT} = 1.5 \text{ V}$

MLCC. The system can also operate at a low switching frequency when a small ESR is used. It can demonstrate the high performance achieved by RRC and NME.

The RRC and NME conquer stability relative to the small ESR value and the large ESL effect in the COT buck converter. Even though the MLCC is used as the output capacitor, without conventional ESR compensation the RRC technique can still increase the system stability since

the compensator contributes a phase lead similar to the phase delay (PD) controller. Besides, the differential structure can benefit the noise margin to decrease the jitter and the EMI effects. In contrast, the NME technique eliminates the effect of ESL to enhance the noise immunity. Furthermore, using a reliable on-time timer with an improved linear function, the near-constant switching frequency, which is adjusted to accommodate variable input voltage, can further



**Figure 4.83** (a) Regulated waveforms attributed to the implementation of RRC and NME at  $v_{IN} = 15 \text{ V}$ ,  $v_{OUT} = 1.5 \text{ V}$ . (b) Marginal stable waveforms with RRC only at  $v_{IN} = 15 \text{ V}$ ,  $v_{OUT} = 1.5 \text{ V}$ . (c) Unstable waveforms in the on-time controlled buck converter without RRC and NME at  $v_{IN} = 15 \text{ V}$ ,  $v_{OUT} = 1.5 \text{ V}$

(c)

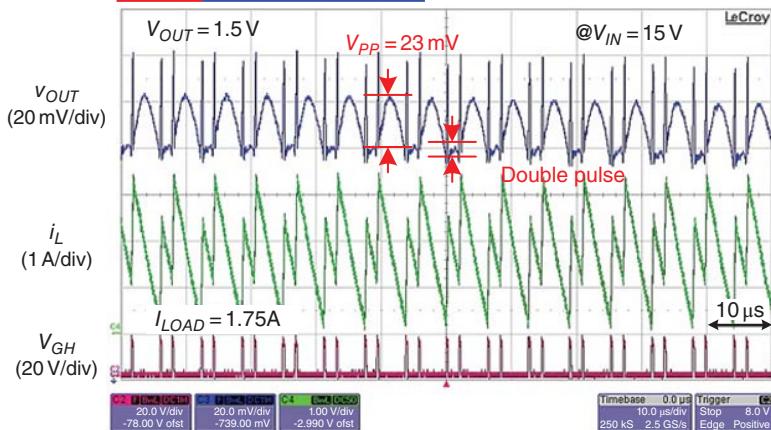
*Unstable without RRC and NME*

Figure 4.83 (Continued)

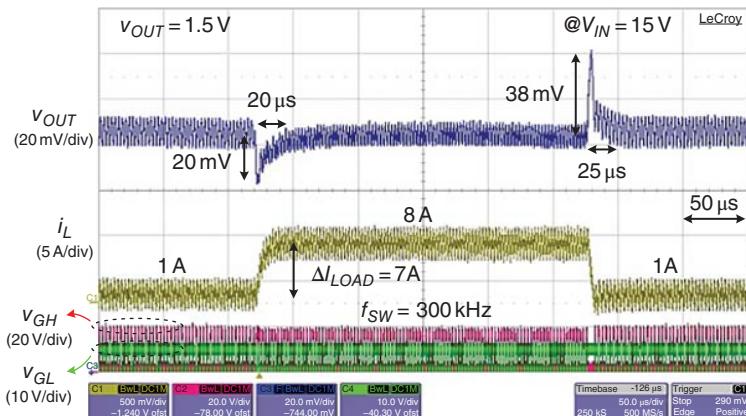
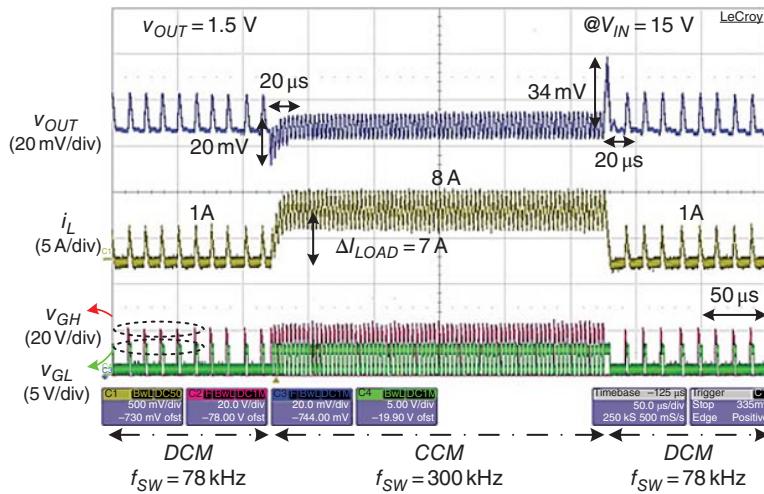


Figure 4.84 Load transient response at CCM operation with RRC and NME techniques

confirm the system stability. Owing to the MLCC with extremely small  $R_{ESR}$  value for general applications, the output ripple can be greatly reduced and thus the switching power loss can be decreased corresponding to the large  $R_{ESR}$  used to compensate conventional ripple-based control. Experiment results verify the correct and effective functions of the RRC and the NME in the strict case of small  $R_{ESR} = 1 \text{ m}\Omega$  and large  $v_{ESL} = 40 \text{ mV}$ . Without sacrificing the inherent advantages of the on-time control, RRC and NME for the MLCC applications can ensure a low ripple of 10 mV and a high efficiency of 91%.



**Figure 4.85** Load transient response at DCM operation at light loads with RRC and NME techniques

**Table 4.28** Comparison table

	This work	[2] ISSCC	[3] T-PE	[4] T-CAS II	[5] JSSC	[6] T-PE	[7] T-PE
Control method	Ripple reshape	Quasi-V2 hysteretic	Virtual inductor current	Derivative-output ripple voltage (DOR)	Pseudo type III compensation	VIC ripple	QDI
Process ( $\mu\text{m}$ )	0.35	0.35	0.35	0.35	0.35	0.18	0.35
$v_{IN}$ (V)	15	2.7–3.3	9	2.4	2.5–3.5	12	3.3
$v_{OUT}$ (V)	1.5	0.9–2.1	4.5	1.8	0.8–2.4	3.3	2
Switching frequency, $f_{SW}$ (MHz)	0.3	3	0.33	0.5	1	0.25	0.8
$L$ ( $\mu\text{H}$ )	1	2.2	90	3.3	4.7	1	4.7
$C_{CO}$ ( $\mu\text{F}$ )	220	4.4	220	4.7	4.7	286	4.7
Tolerance of minimum $R_{ESR}$ ( $\text{m}\Omega$ )	1	30	50	15	20	3	10
Minimum $\Delta v_{ripple}$ (mV)	10	12	N/A	20	10	40	10
$\Delta i_L$ (A)	7	0.45	N/A	0.45	0.5	N/A	0.49
Load range, $i_{Load}$ (A)	1–8	0.05–0.5	N/A	0.25–0.7	0.1–0.6	N/A–18	0.01–0.5
Power efficiency	91%	93%	N/A	N/A	85% up	90%	93%

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# 5

## Ripple-Based Control Technique Part II

### 5.1 Design Techniques for Enhancing Voltage Regulation Performance

#### 5.1.1 Accuracy in DC Voltage Regulation

Conventional on-time control has the advantages of fast transient response and simple compensation compared with other control techniques, such as voltage-mode control (VMC) and current-mode control (CMC). However, the inaccuracy of output voltage regulation is an inherent drawback. The expected output voltage DC level  $v_{OUT}$  expressed in Eq. (5.1) is determined using the reference voltage  $V_{REF}$  and the voltage dividers  $R_1$  and  $R_2$ :

$$v_{OUT} = V_{REF} \cdot \left( 1 + \frac{R_1}{R_2} \right) \quad (5.1)$$

In on-time controlled converters, the output voltage is regulated but with an unexpected DC offset voltage deviation. According to Figure 4.6(a), the output voltage of the on-time controlled converter is regulated at the value calculated using Eq. (5.2). The offset voltage deviation is caused by the extra term  $v_{OUT\_ripple}$ , which also represents the output voltage ripple:

$$v_{OUT} = V_{REF} \cdot \left( 1 + \frac{R_1}{R_2} \right) + \frac{1}{2} v_{OUT\_ripple} \quad (5.2)$$

As previously mentioned in Section 4.2.1, the output voltage ripple is determined by many factors, such as the inductor current ripple,  $C_{OUT}$ ,  $R_{ESR}$ , and  $L_{ESL}$ . Moreover, the output voltage

ripple is different under different operating modes, as derived using Eqs. (5.3) and (5.4) for CCM and DCM, respectively:

$$v_{pp(CCM)} \approx \frac{(1-D)}{8f_{SW}^2 LC} \cdot v_{OUT} + R_{ESR} \cdot \frac{(1-D)}{f_{SW} L} \cdot v_{OUT} + \frac{L_{ESL}}{L} \cdot v_{IN} \quad (5.3)$$

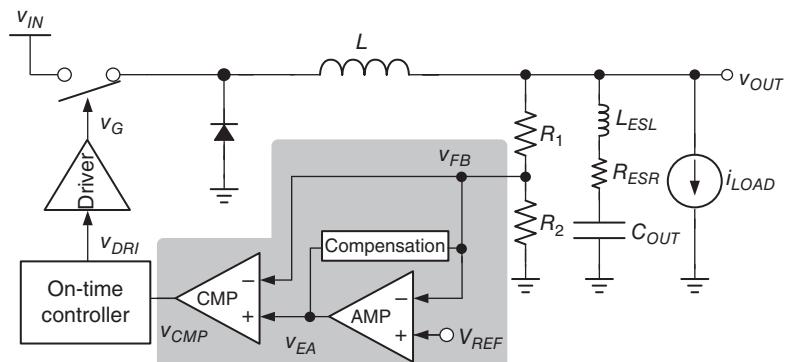
$$\begin{aligned} v_{pp(DCM)} \approx & \frac{1}{RC} \left( \frac{1}{f_{SW}} + \frac{L}{2R_{Load}(1-D)} - \sqrt{\frac{2L}{R_{Load} \cdot f_{SW} (1-D)}} \right) \cdot v_{OUT} \\ & + R_{ESR} \cdot \frac{D(1-D)}{L f_{SW}} \cdot v_{OUT} + \frac{L_{ESL}}{L} \cdot v_{IN} \end{aligned} \quad (5.4)$$

The accuracies of output voltage and load regulation are degraded because of the characteristics of the output voltage ripple when considering all parasitic effects. Therefore, the  $V^2$  structure is implemented to enhance regulation performance. The basic design method of  $V^2$  structure and other advanced techniques for high performance will be introduced in the next subsection.

### 5.1.2 $V^2$ Structure for Ripple-Based Control

#### 5.1.2.1 $V^2$ On-Time Control

Figure 5.1 shows that the  $V^2$  structure is implemented in on-time control by adding an extra output voltage feedback path. That is, the  $V^2$  structure contains two voltage feedback paths traversing directly from the output to the comparator and is used to determine the switching operation. The  $V^2$  structure is the feedback path generated by two parallel voltage paths. The first path is the original path that feeds the output voltage directly to the comparator. This path is also called the fast feedback path, because it reacts rapidly to the output voltage variation. As such, a good transient response can be derived using the  $V^2$  structure. The other path from the output to the comparator consists of one error amplifier with a compensation network. The output of the error amplifier,  $v_{EA}(t)$ , is determined by the difference voltage of  $v_{OUT}$  and  $V_{REF}$ . This path is



**Figure 5.1** Schematic of  $V^2$  on-time control

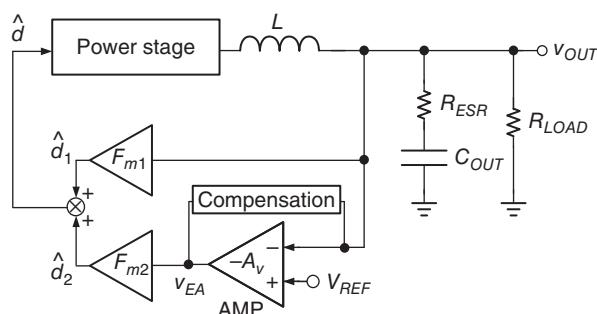
called the slow feedback path because the bandwidth is limited by the bandwidth of the error amplifier and the compensation network. Through the closed loop,  $v_{EA}(t)$  in comparison with  $V_{REF}$  reflects the error in revising the DC offset between  $v_{OUT}$  and  $V_{REF}$ . As a result, the slow feedback path can improve the output DC regulation. Simultaneously, the fast feedback path can maintain the fast transient response.

As depicted in Figure 5.1, the compensation should be well designed because the  $V^2$  structure uses the error amplifier on the feedback path. According to the superposition theory, the transfer function from the inverting terminal of the error amplifier to the output is the same as in Eq. (4.12).

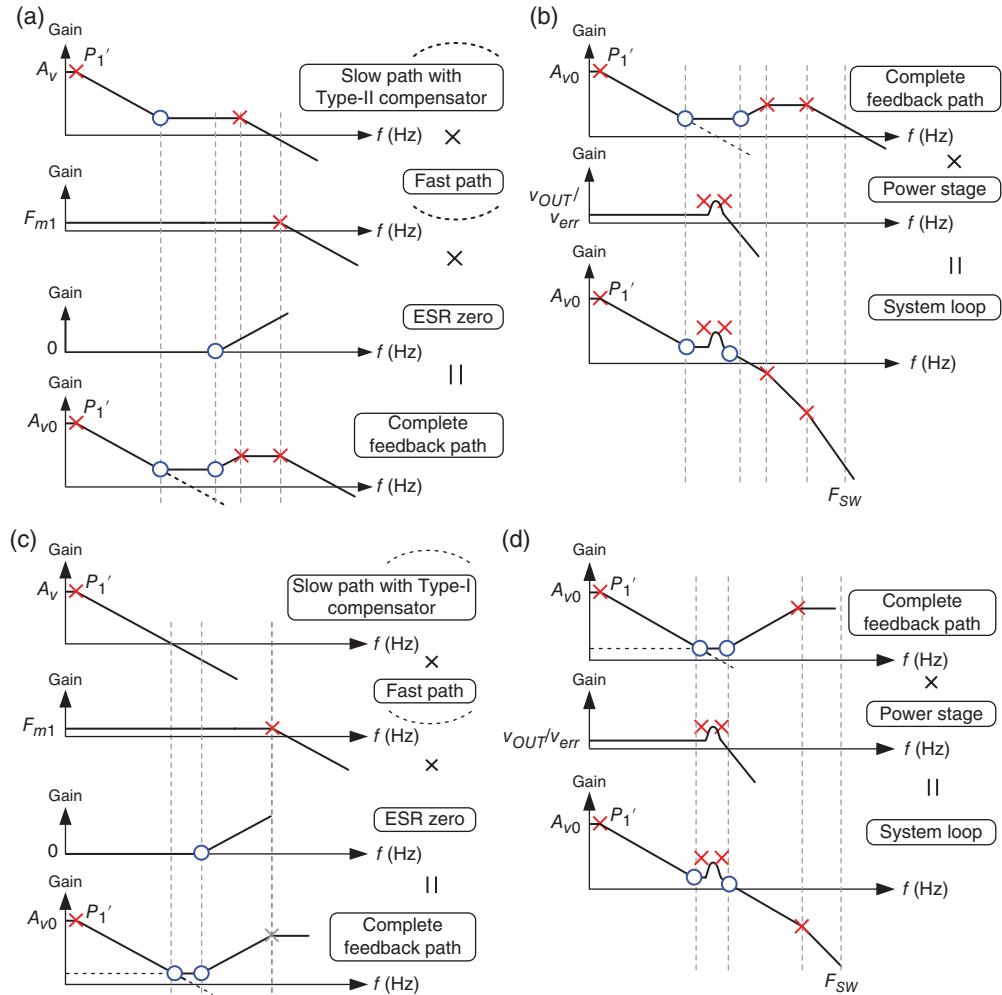
Figure 5.2 shows the small single model of a buck converter with basic  $V^2$  control. The system duty cycle  $d$  is composed of two factors,  $d_1$  and  $d_2$ , which are the controls from the fast feedback path and the slow feedback path, respectively. The transfer function of the fast feedback path is from  $v_{OUT}$  to  $d_1$ , denoted as the transfer function  $F_{m1}$ , while the slow feedback path is from  $v_{OUT}$  to  $d_2$  via the error amplifier, denoted as the transfer function  $F_{m2}$ .  $F_{m1}$  and  $F_{m2}$  stand for analog-to-digital conversion, where  $-A_v$  is the DC gain of the EA.

Similarly, according to Eq. (4.12) and if  $R_{ESR}$  is large enough, a Type-II compensator can be utilized to guarantee stability. Figure 5.3(a), (b) illustrates the frequency response to reveal the distribution of poles and zeros. In Figure 5.3(a), the slow path with Type-II compensator provides one low-frequency pole/zero pair and another high-frequency pole. In contrast, the frequency response of the fast path with the comparator has low gain and high bandwidth. To simplify the stability analysis after compensation, the zero contributed by  $R_{ESR}$  and  $C_{OUT}$  is included in the feedback path. Consequently, the frequency response of the complete feedback path can be derived as the complete waveform at the bottom of Figure 5.3(a). Figure 5.3(b) illustrates the frequency response of the system loop gain composed of the complete feedback path and the power stage. The lowest-frequency pole is set as the dominant pole. The low-frequency zero contributed by the Type-II compensator and the ESR zero, generated by  $R_{ESR}$  and  $C_{OUT}$ , can be used to cancel the complex poles derived in Eq. (4.12). Finally, the high-frequency pole is used to decade high-frequency gain and to reduce high-frequency noise. As a result, system stability can be guaranteed.

On the contrary, the Type-I compensator is another choice for all possible compensation techniques. Figure 5.3(c), (d) illustrates the frequency response to reveal the distribution of poles and zeros. In Figure 5.3(c), the Type-I compensator provides one low-frequency pole

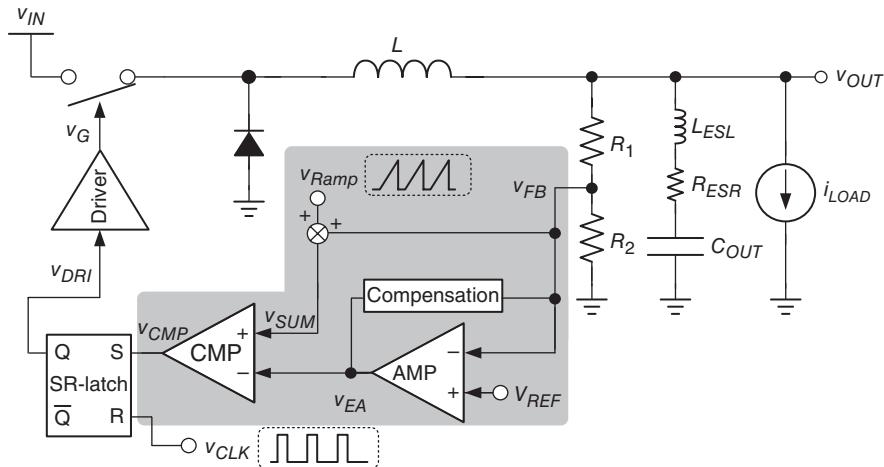


**Figure 5.2** Small single model of buck converter with the basic  $V^2$  control in a constant switching frequency



**Figure 5.3** Frequency response of (a) feedback loop with Type-II compensator, (b) system loop gain compensated by Type-II compensator, (c) feedback loop with Type-I compensator, and (d) system loop gain compensated by Type-I compensator

as the dominant pole. The ESR zero, contributed by  $R_{ESR}$  and  $C_{OUT}$ , can cancel part of the effect from the complex poles but the system still needs another zero. Thus, another architectural zero, generated by the parallel structure composed of fast and slow feedback paths, locates at a frequency near the UGF of the voltage error amplifier. Similar to the case with Type-II compensator, the complete feedback path contains one low-frequency pole and two compensation zeros. Figure 5.3(d) shows the frequency response of the system loop gain. Within the UGF, the compensated system can guarantee stability with an adequate phase margin because the system apparently performs as a one-pole system due to the cancellation of complex poles by two compensation zeros.



**Figure 5.4** Schematic of  $V^2$  constant-frequency valley-voltage control

### 5.1.2.2 $V^2$ Constant-Frequency Valley-Voltage Control

Figure 5.4 shows that the  $V^2$  structure is implemented in the constant-frequency valley-voltage control technique introduced in Section 4.1.4. The inverting input of the comparator substitutes the reference voltage  $V_{REF}$  by the EA output voltage  $v_{EA}(t)$  determined by comparing  $v_{OUT}$  and  $V_{REF}$ .  $v_{EA}(t)$  is treated as one new  $V_{REF}$  because the voltage EA revises the DC offset by the comparison result of  $v_{OUT}$  and  $V_{REF}$ . Because the error amplifier is inserted in the control loop, the compensation network is needed to increase stability. The control-to-output transfer function of the power stage can be expressed as Eq. (5.5), where  $G_{d0}$ , the DC gain of the power stage, and the LC double poles at  $\omega_0$  are shown in Eq. (5.6). The ESR zero  $\omega_{ESR}$ ,  $R_{ESR}$  and  $C_{OUT}$  can be helpful in increasing the system stability if  $\omega_{ESR}$  is less than  $3\omega_0$  at the cost of a large output voltage ripple.

$$\frac{\hat{v}_{OUT}(s)}{\hat{d}} = G_{d0} \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{1}{Q\omega_0}s + \frac{1}{\omega_0^2}s^2} \quad (5.5)$$

where

$$\omega_{ESR} = \frac{1}{R_{ESR}C_{OUT}}, \quad \omega_0 = \frac{1}{\sqrt{LC_{OUT}}}, \quad Q = R_{Load}\sqrt{\frac{C_{OUT}}{L}} \quad (5.6)$$

To analyze the stability, Figure 5.3 is also utilized to understand the small single model of a basic  $V^2$  control buck converter with constant switching frequency. Similar to the compensation skill for  $V^2$  on-time control, a Type-II compensator can be used to stabilize the  $V^2$  structure with

the assistance of a large  $R_{ESR}$ . Equation (5.7) expresses the loop-gain transfer function of the buck converter with  $V^2$  structure, where  $F_{m1} = F_{m2} = F_m$ :

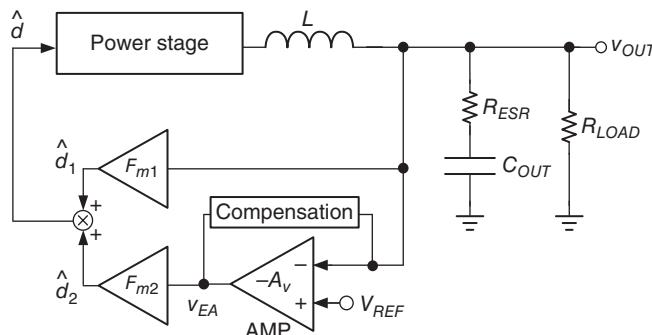
$$T(s) = G_{d0}F_mA_v \cdot \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{1}{Q\omega_0}s + \frac{1}{\omega_0^2}s^2\right)\left(1 + \frac{s}{\omega_p}\right)} \quad (5.7)$$

The Type-II compensator generates a low-frequency pole  $\omega_p$  and a zero  $\omega_z$  with gain improvement by the error amplifier.  $\omega_p$  works as the system dominant pole, while  $\omega_z$  and  $\omega_{ESR}$  cancel the effect of the complex poles at  $\omega_0$ . As a result, Type II with a large value of  $R_{ESR}$  can guarantee system stability. Alternatively, architectural parallel paths can generate a zero to replace the zero of the Type-II compensator. In other words, the compensator can be simplified to a Type-I compensator if an adequate UGF can be derived (Figure 5.5).

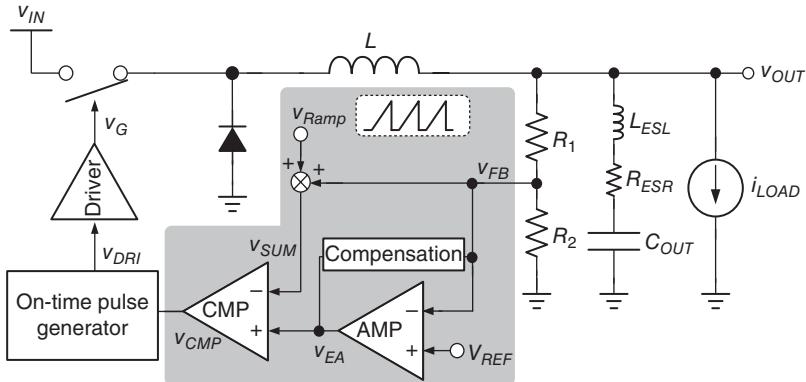
### 5.1.3 $V^2$ On-Time Control with an Additional Ramp or Current Feedback Path

An additional ramp signal or current feedback signal can increase the stability. However, the ripple of feedback voltage equivalently induces a larger DC voltage offset. Thus, the  $V^2$  structure can be implemented to maintain the stability without sacrificing the DC regulation. Figures 5.6 and 5.7 show the  $V^2$  on-time control with an additional ramp signal and an additional current feedback path, respectively.

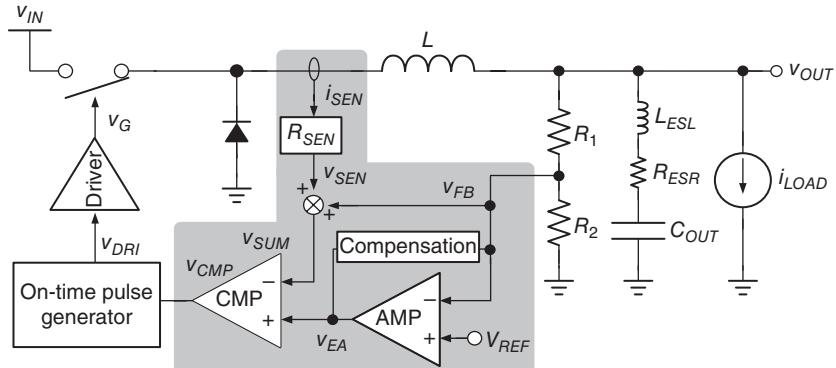
The current-sensing circuit can be determined by the approaches introduced in Section 4.3.2. With a voltage EA,  $v_{EA}$  adjusts the DC value to accurately regulate the output voltage. In other words, no matter whether the sensing voltage includes DC information or not, the DC value of  $v_{EA}$  can dynamically change corresponding to the DC value of  $v_{SUM}$  and the difference between  $v_{FB}$  and  $v_{REF}$ . If  $v_{SUM}$  includes DC information on the inductor current, the DC value of  $v_{EA}$  is almost determined by the loading conditions. One design issue that needs to be taken into consideration is that the DC value of  $v_{EA}$  would influence the operation of the amplifier. Too high or too low a value would cause the MOSFET to operate in a linear region and degrade the DC gain of the amplifier. Similar to current-mode PWM control, the loading current range is



**Figure 5.5** Small signal of basic  $V^2$  control buck converter with a constant switching frequency



**Figure 5.6**  $V^2$  on-time control with an additional ramp signal



**Figure 5.7**  $V^2$  on-time control with an additional current feedback path

somehow constrained by the DC value of the current-sensing signal because of the limited headroom voltage. In contrast, Type-I or Type-II compensator can be used with similar analysis methods in  $V^2$  on-time control to guarantee system stability.

Although the accuracy of DC regulation and stability can be guaranteed, the side effect of slow transient response caused by the additional signals is significant. According to the results of Eqs. (4.32) and (4.37), the quality factor  $Q$  in the denominator implies that the system can be more robust when the feedback signal accompanies an increasing amount of additional ramp signal or additional current ripple. However, the increasing amount of the additional signals equivalently reduces the gain to monitor the output voltage. As a result, the insensitivity to variation of output voltage degrades the transient response. To guarantee stability, the excess of extra signals scarifies the fast transient response, which is an inherent advantage of ripple-based control. Consequently, when these techniques are utilized, any over-designs should be avoided to keep the original advantages and to further achieve advanced performance.

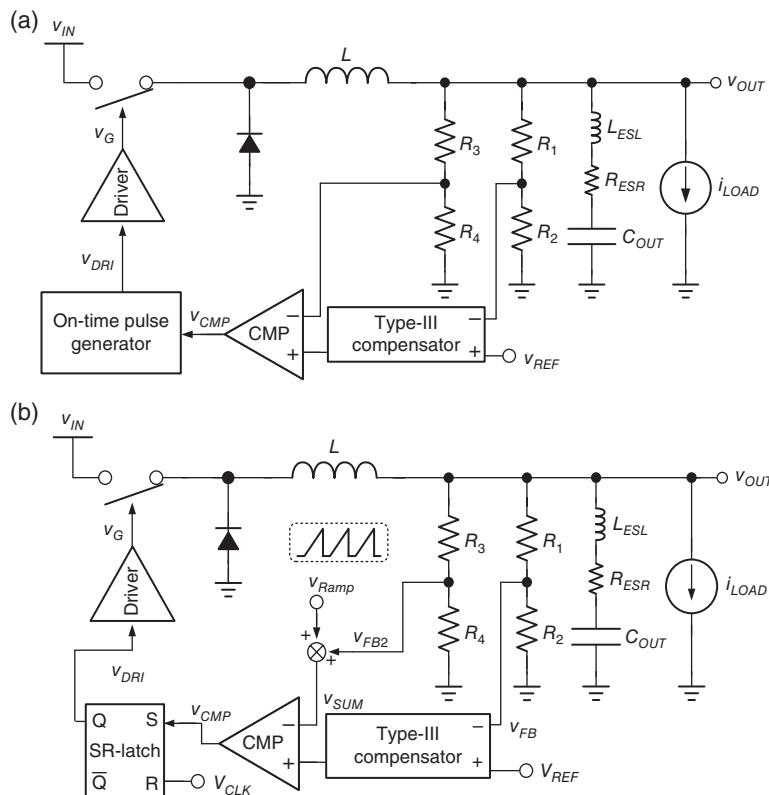
### 5.1.4 Compensator for $V^2$ Structure with Small $R_{ESR}$

#### 5.1.4.1 Type-III Compensator for Realizing $V^2$ Control with Small $R_{ESR}$

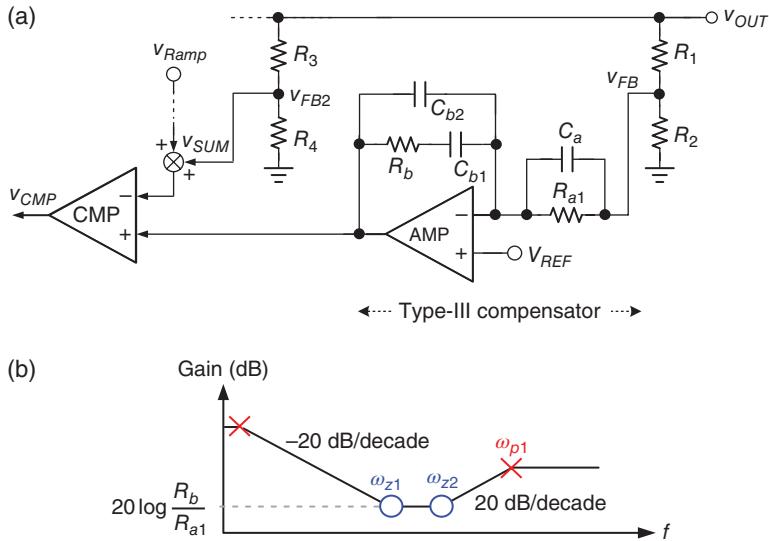
Based on the analysis in Section 5.1.2, the compensator should provide two zeros to cancel the complex poles. If the output capacitor  $C_{OUT}$  has large  $R_{ESR}$ , one of the zeros can be contributed by  $C_{OUT}$  and  $R_{ESR}$ . The other zero is contributed by the compensator on the feedback path. In case of large  $R_{ESR}$ , the Type-I and Type-II compensators are suitable candidates to guarantee stability. In contrast, if  $C_{OUT}$  contains a small  $R_{ESR}$ , the zero generated by  $R_{ESR}$  and  $C_{OUT}$  is located at high frequencies and is not useful for system stability. To cancel the complex poles at the power stage, two zeros must be provided by the compensator on the feedback path. Consequently, a Type-III compensator can be taken into consideration.

Figure 5.8(a), (b) shows that the Type-III compensator is applied to  $V^2$  on-time control and  $V^2$  constant-frequency peak-voltage control, respectively.

Figure 5.9(a) shows the structure of  $V^2$  control with Type-III compensator. Figure 5.9(b) depicts the frequency response, and the transfer function is expressed in Eq. (5.8). An error



**Figure 5.8** Type-III compensator for (a)  $V^2$  on-time control, (b)  $V^2$  constant-frequency peak-voltage control



**Figure 5.9** (a) Structure of  $V^2$  control and Type-III compensator with one pole and two zeros. (b) Frequency response

amplifier with three capacitors and two resistors to implement the Type-III compensator can generate two zeros ( $\omega_{z1}$  and  $\omega_{z2}$ ) and one pole ( $\omega_{p1}$ ), as in Eq. (5.9):

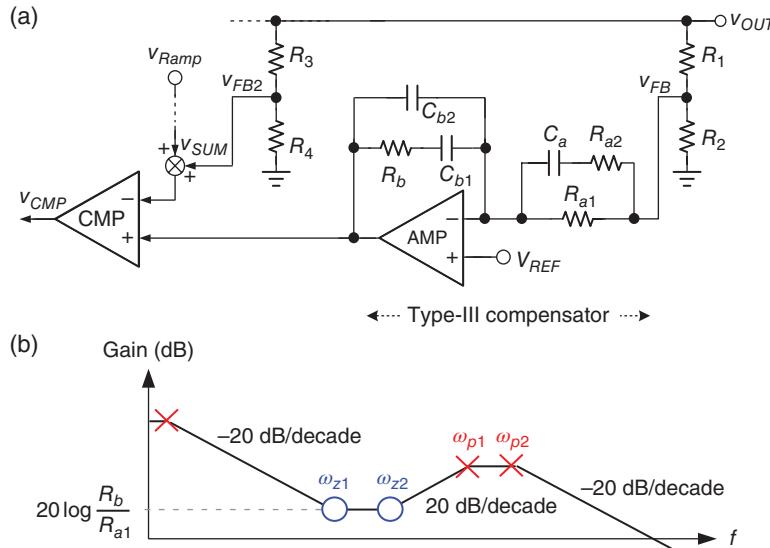
$$A(s) = -A_0 \cdot \frac{1}{s(C_{b1} + C_{b2})R_{a1}} \cdot \frac{(1 + sR_{a1}C_a)(1 + sR_bC_{b1})}{1 + sR_b \left( \frac{C_{b1} \cdot C_{b2}}{C_{b1} + C_{b2}} \right)} \quad (5.8)$$

$$\begin{aligned} \omega_0 &= \frac{1}{(C_{b1} + C_{b2})R_{a1}}, \quad \omega_{p1} = \frac{1}{R_b \left( \frac{C_{b1} \cdot C_{b2}}{C_{b1} + C_{b2}} \right)} \\ \omega_{z1} &= \frac{1}{R_{a1}C_a}, \quad \omega_{z2} = \frac{1}{R_bC_{b1}} \end{aligned} \quad (5.9)$$

Two zeros need to locate at frequencies near the complex poles, caused by the power stage. To ensure a negative feedback loop, the frequency of one of the zeros is required to be below the complex poles. Besides, according to the stability criterion of ripple-based control as in Eq. (4.27), two zeros,  $\omega_{z1}$  and  $\omega_{z2}$ , are suggested to be located at frequencies lower than 10% of the switching frequency. In contrast, the high-frequency pole,  $\omega_{p1}$ , is suggested to be located at frequencies close to the high-frequency zero due to  $R_{ESR}$  for suppressing high-frequency noise.

Figure 5.10(a) shows the structure of  $V^2$  control with Type-III compensator. Figure 5.10(b) depicts the frequency response whose transfer function is expressed in Eq. (5.10):

$$A(s) = -A_0 \cdot \frac{1}{s(C_{b1} + C_{b2})R_{a1}} \cdot \frac{(1 + s(R_{a1} + R_{a2})C_a)(1 + sR_bC_{b1})}{1 + sR_b \left( \frac{C_{b1} \cdot C_{b2}}{C_{b1} + C_{b2}} \right)(1 + sR_{a2}C_a)} \quad (5.10)$$

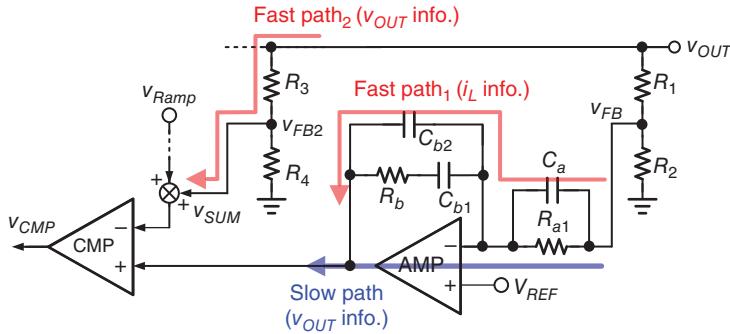


**Figure 5.10** (a) Structure of \$V^2\$ control and Type-III compensator with two poles and two zeros. (b) Frequency response

An error amplifier with three capacitors and three resistors to implement a Type-III compensator can generate two zeros ( $\omega_{z1}$  and  $\omega_{z2}$ ) and two poles ( $\omega_{p1}$  and  $\omega_{p2}$ ), as shown in Eq. (5.11). Compared with Figure 5.9, this Type-III compensator provides an additional pole,  $\omega_{p2}$ , which can benefit artifact noise suppression at high frequencies. Thus, this pole,  $\omega_{p2}$ , is typically set to half of  $f_{SW}$ , or 10 times the UGF,  $f_{UGF}$ .

$$\begin{aligned}\omega_0 &= \frac{1}{(C_{b1} + C_{b2})R_{a1}}, \quad \omega_{p1} = \frac{1}{R_b \frac{C_{b1} \cdot C_{b2}}{C_{b1} + C_{b2}}}, \quad \omega_{p2} = \frac{1}{R_{a2}C_{a1}} \\ \omega_{z1} &= \frac{1}{(R_{a1} + R_{a2})C_{a1}}, \quad \omega_{z2} = \frac{1}{R_b C_{b1}}\end{aligned}\quad (5.11)$$

To comprehensively understand the similarities and differences compared with the previous \$V^2\$ structure, the Type-III compensator in Figure 5.9(a) can also be divided equally into two parallel paths, fast path<sub>1</sub> and slow path, as shown in Figure 5.11. Through capacitors  $C_a$  and  $C_{b2}$ , this fast path provides the pass of high-frequency signals. In other words, the inductor current ripple information can be equivalently recovered by the output voltage ripple so that the inductor current can be monitored to ensure stability. On the slow feedback path through the amplifier, the offset at the output can be modified. There is another fast path (fast path<sub>2</sub>) through the voltage divider ( $R_3$  and  $R_4$ ) that can directly reflect the DC regulation of  $v_{OUT}$  so that the converter can instantly adjust the power delivery during the transient period. Consequently, the function of fast path<sub>1</sub> and fast path<sub>2</sub> is similar to the fast path in the previous \$V^2\$ structure, which can simultaneously monitor  $v_{OUT}$  for DC regulation and  $i_L$  for stability. The buck converter with



**Figure 5.11** Different signal paths feeding back from the output

$V^2$  control and small ESR can be modulated with an ensured stability. And last but not least, if the constant-frequency clock signal is applied as shown in Figure 5.8(b), an extra ramp signal is necessary to avoid the sub-harmonic oscillation.

#### 5.1.4.2 Type-III Compensator for Realizing Single Path $V^2$ Control with Small $R_{ESR}$

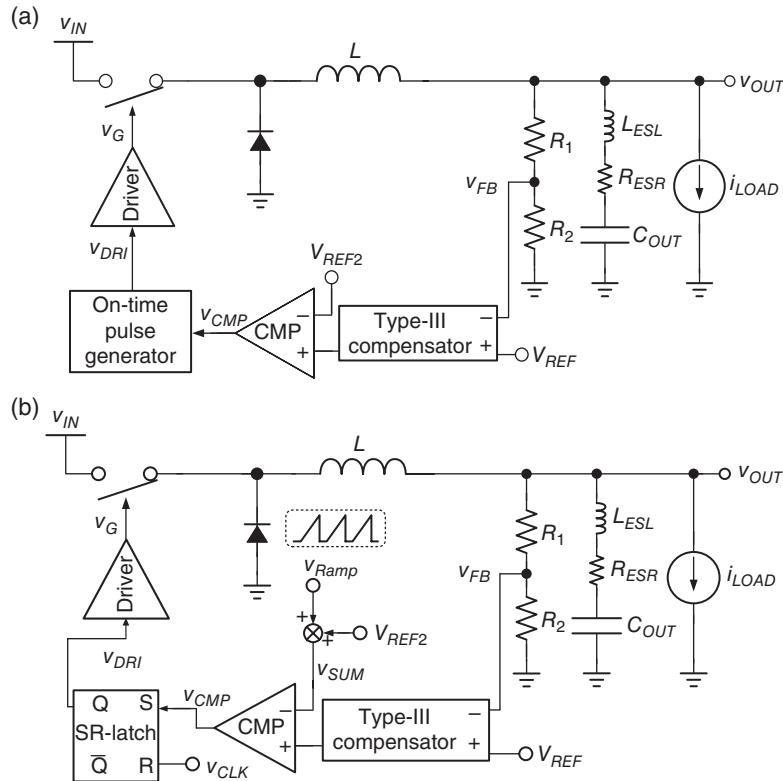
There are researches that provide simplification methods to further develop the structure of the Type-III compensator for  $V^2$  control. The direct voltage path is removed so that the feedback path can be viewed as one single way through the compensator while the ripple-based control is still established. Figure 5.12(a), (b) shows the architecture of a single feedback path for  $V^2$  on-time control and  $V^2$  constant-frequency peak-voltage control, respectively.

To understand the concept for realizing ripple-based control by a single path, let's take Figure 5.12 as an example with the help of Figure 5.13 to depict the comparator including Type-III compensator in detail. The path through the Type-III compensator includes two paths, both a fast path and a slow path. The fast path provides a function of the high-pass filter to recover the inductor current ripple information from the output voltage ripple. The slow path provides DC information to regulate  $V_{OUT}$ . According to the above analysis, this approach does work. However, the limited bandwidth of the slow path cannot instantly reflect the output voltage level. As a result, the transient response is significantly deteriorated.

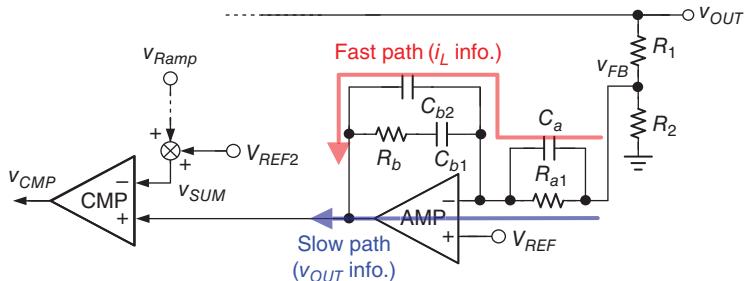
#### 5.1.4.3 Differentiator for $V^2$ Structure with Small $R_{ESR}$

The above discussion provides a Type-III compensator to guarantee stability. However, the integration becomes a challenge because large capacitors and large resistors are necessary. For this reason, it is necessary to develop other approaches that provide the same function together with the possibility of integrated compensation. We introduce some ideas to make such an integrated design more feasible.

From the aspect of ripple-based control, the inductor current ripple is difficult to extract from the voltage feedback path because the output voltage ripple is not generally dominated by the



**Figure 5.12** Type-III compensator for (a)  $V^2$  on-time control, (b)  $V^2$  constant-frequency peak-voltage control



**Figure 5.13** The comparator including Type-III compensator in detail

small  $R_{ESR}$ . The relationship between  $v_L$  and  $v_{OUT}$  is not linear. According to Eqs. (4.7)–(4.9), the output voltage can be derived as Eq. (5.12) including ESR and ESL effects:

$$v_{OUT}(t) = R_{ESR}i_L(t) + \frac{1}{C_{OUT}} \int i_L(t)dt + L_{ESL} \frac{d}{dt} i_L(t) \quad (5.12)$$

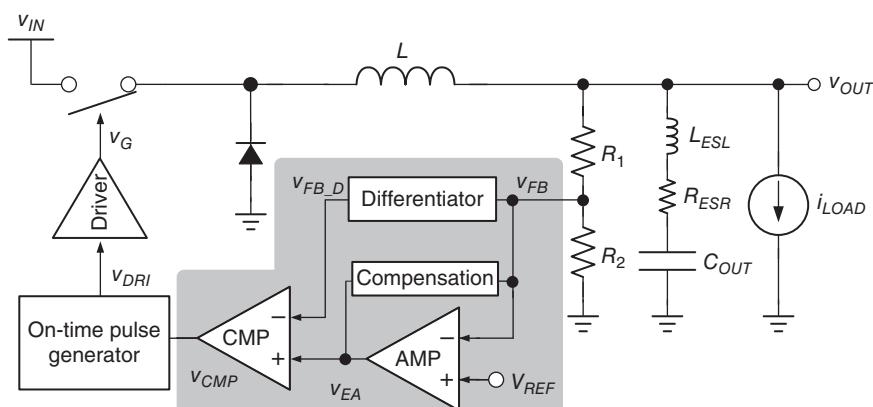
Obviously, only the first term of  $R_{ESR}$  contributes a linear function to reflect the inductor current ripple. When an output capacitor with low  $R_{ESR}$  is used, the ripple is mainly determined by the second and third terms. Besides, assuming the ESL effect is also ignored due to a small ESL value, the relationship between  $i_L$  and  $v_{OUT}$  is shown in Eq. (5.13), which expresses simply charging/discharging the output capacitor with the inductor current:

$$v_{OUT}(t) = \frac{1}{C_{OUT}} \int i_L(t) dt \quad (5.13)$$

This equation shows the non-linear relationship between  $v_{OUT}(t)$  and  $i_L(t)$ . Feeding back the output voltage to the controller will cause unstable operation due to the out-of-phase relationship between  $v_{OUT}(t)$  and  $i_L(t)$ . Therefore, the differentiator in Figure 5.14 is used in the  $V^2$  structure to derive the inductor current information though the feedback output voltage. Because the slow feedback path through the amplifier is used to enhance the accuracy, the output voltage ripple has little impact on the operation. In contrast, the fast feedback loop needs the inductor current ripple information to determine correct switching timing. It's necessary to recover the inductor current ripple from  $v_{OUT}$ .

Equation (5.14) is derived to show the inductor current ripple recovered by the signal  $v_{FB\_D}(t)$  after an ideal differentiator. In other words,  $v_{FB\_D}(t)$  is linearly proportional to  $i_L(t)$ . With the assistance of a recovery function of the differentiator, the stability issue can be analyzed as discussed in Section 4.3. Consequently, even when  $R_{ESR}$  of the output capacitor is too small, the stability can be increased by the  $V^2$  structure with an additional differentiator:

$$v_{FB\_D}(t) = v_{OUT}(t) \cdot \beta = \frac{d}{dt} \left( \frac{1}{C_{OUT}} \int i_L(t) dt \right) \cdot \beta = i_L(t) \cdot \frac{\beta}{C_{OUT}} \quad (5.14)$$



**Figure 5.14** The differentiator can be used in the  $V^2$  structure to derive the inductor current information though the feedback output voltage

where

$$\beta = \frac{R_2}{R_1 + R_2}$$

#### 5.1.4.4 Equivalent Type-III Compensator for $V^2$ Control with Small $R_{ESR}$

If  $R_{ESR}$  is not large enough in the  $V^2$  on-time control, the differentiator has the ability to extract the inductor current ripple through the fast feedback path. In other words, the zero is contributed by a differentiator to replace the equivalent ESR zero so that Eq. (4.27) holds to ensure system stability.

In contrast, because the complex poles exist at the power stage, two zeros should be provided on the feedback path, which is composed of slow and fast paths. Thus, a Type-I or Type-II compensator can be used to work on the slow feedback path. When a Type-I compensator is used, two zeros are contributed by the compensator and the architectural zero due to parallel paths. When a Type-II compensator is used, both zeros are contributed by the compensator.

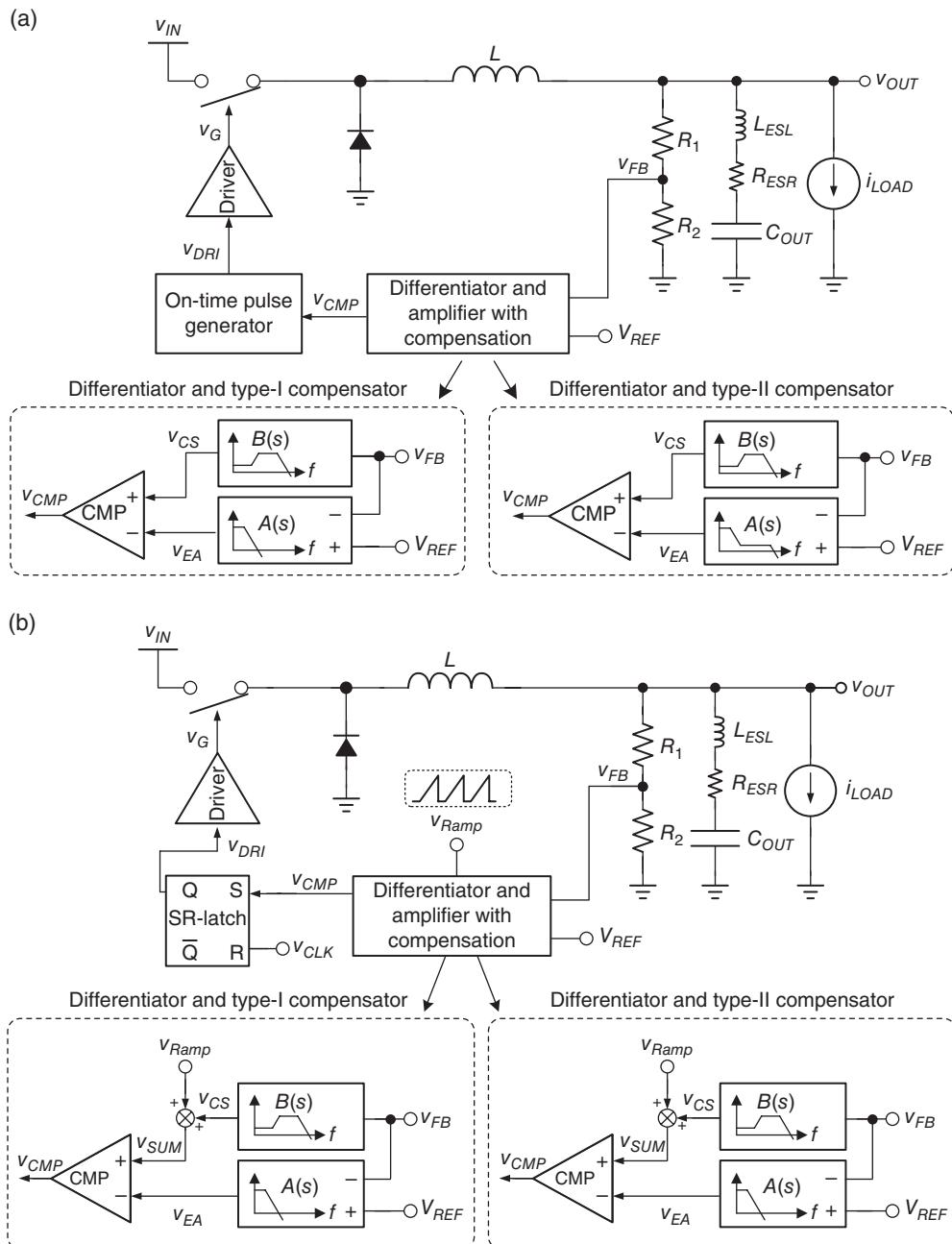
The block circuit is illustrated in Figure 5.15. The function of the differentiator is equivalent to the function of a high-pass filter. In practice, the function should be seen as a band-pass filter, expressed as  $B(s)$ , because high-frequency poles exist inherently in the circuit. The critical design issue is to ensure the zero is adequate to contribute a phase lead function for differentiation, and meanwhile to ensure that the other pole is at a high enough frequency. The transfer function of the amplifier with compensation is expressed as  $A(s)$ . Whether for on-time control as in Figure 5.15(a) or for constant-frequency peak-voltage control as in Figure 5.15(b), the system contains complex poles.

Figure 5.16(a), (c) illustrates the frequency response for the system with Type-I compensator. Figure 5.16(b), (d) illustrates the frequency response for the system with Type-II compensator. The parallel structure of  $A(s)$  and  $B(s)$  can induce two zeros, as shown in Figure 5.16(a), (b). Except for the dominant pole, the rest of the poles locate at a frequency higher than the bandwidth (BW), so it is reasonable to ignore their effects. As a result, Figure 5.16(c), (d) shows that the complex poles are compensated by two zeros for on-time control and constant-frequency peak-voltage control, respectively.

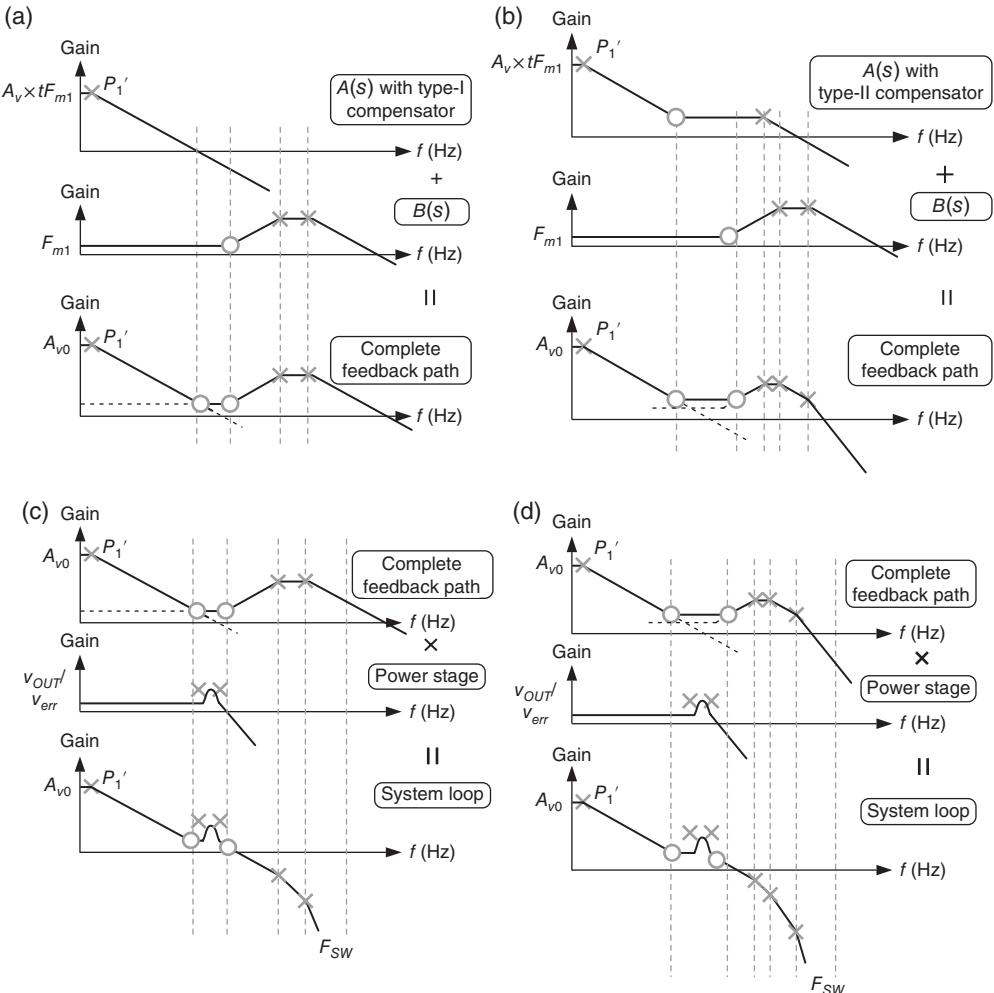
It should be noticed that the additional differentiator induces some drawbacks. On the fast feedback path, the differentiator recovers the inductor current ripple from the output voltage ripple. However, some high-frequency poles exist practically in the differentiator circuit. The bandwidth of this fast feedback path then limits the signal conduction from  $v_{OUT}(t)$  to  $v_{CS}(t)$ . Thus, the inherent fast transient response feature is drastically degraded, although the stability is increased.

#### 5.1.5 Ripple-Based Control with Quadratic Differential and Integration Technique if Small $R_{ESR}$ is Used

Through use of the differentiation function, the ripple of the feedback signal can be recovered from the distortion of  $v_{OUT}$  when a small  $R_{ESR}$  is used. In other words, the system stability can be guaranteed. Besides, the output voltage ripple and the transient dip can effectively be



**Figure 5.15** Equivalent Type-III compensator for (a)  $V^2$  on-time control, (b)  $V^2$  constant-frequency peak-voltage control

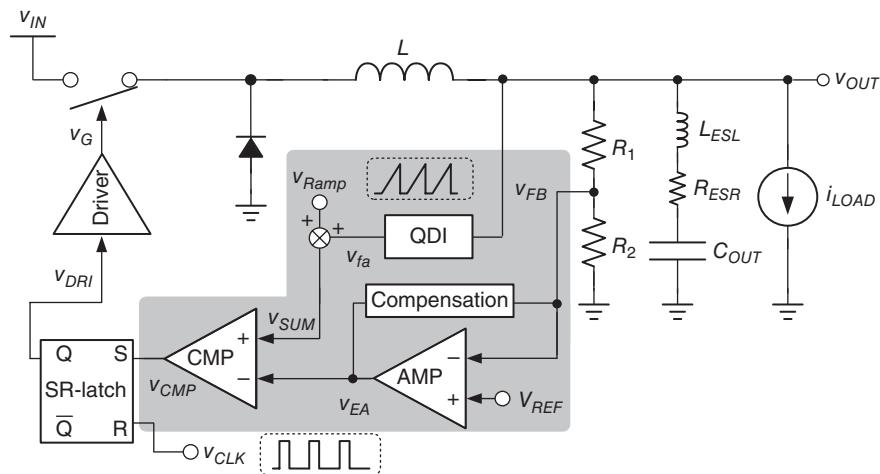


**Figure 5.16** Frequency response of (a) feedback loop with Type-I compensator, (b) feedback loop with Type-II compensator, (c) system loop with Type-I compensator, (d) system loop with Type-II compensator

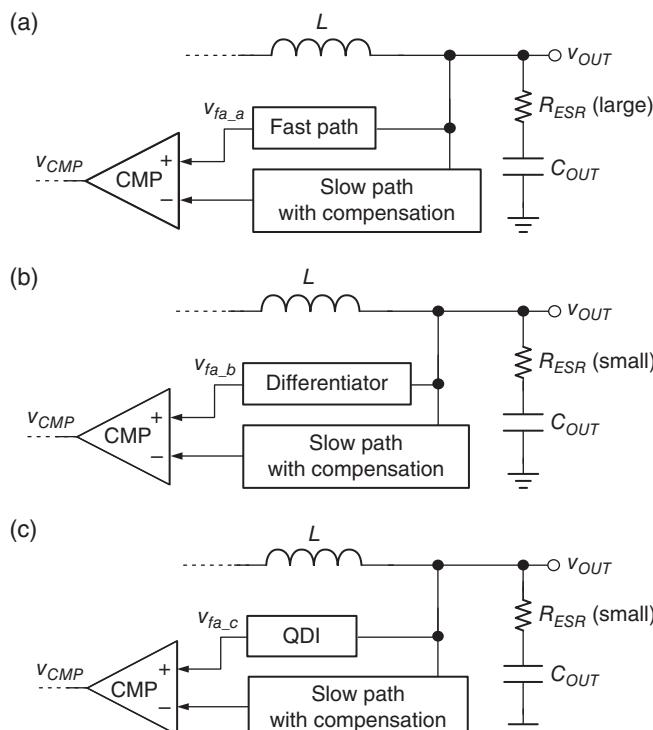
minimized. However, the existing  $R_{ESR}$  still affects the accuracy of the recovery signal. This unwilling distortion deteriorates the system stability. Furthermore, the inaccurate accuracy signal results in a worse load regulation.

The quadratic differential and integration (QDI) technique based on the  $V^2$  control buck converter improves these performances. Figure 5.17 shows the  $V^2$  control with the QDI technique. Based on the structure of  $V^2$  control, the QDI technique is inserted on the fast feedback path.

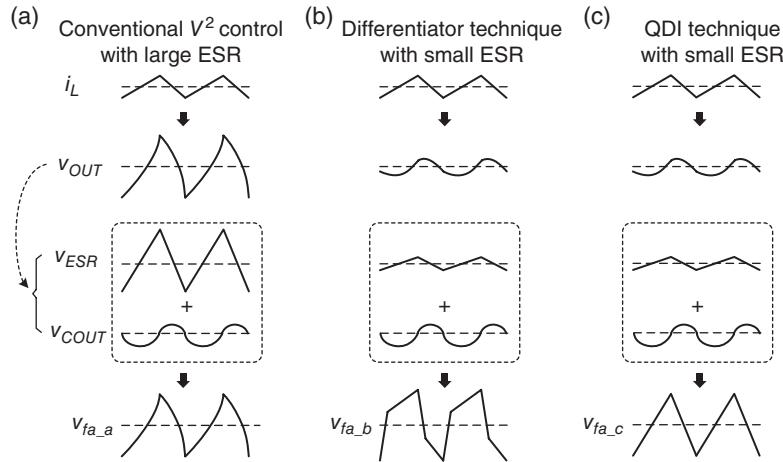
Figure 5.18 shows a simple structure for comparison between the QDI technique and previous methods, based on  $V^2$  control. Figure 5.18(a) shows the conventional  $V^2$  control with large ESR. Figure 5.18(b), (c) shows the differentiator technique with small ESR and the



**Figure 5.17**  $V^2$  control with the QDI technique



**Figure 5.18** The structures with  $V^2$  control: (a) conventional  $V^2$  control for large ESR application; (b)  $V^2$  control with differentiator technique for small ESR application; (c)  $V^2$  control with QDI technique for small ESR application



**Figure 5.19** (a) Conventional  $V^2$  control with large ESR. (b) Differentiator technique with small ESR. (c) QDI technique with small ESR

QDI technique with small ESR, respectively. The  $L_{ESL}$  on the capacitor is assumed small so that the ripple of  $L_{ESL}$  can be neglected. The signal  $v_{fa}$  ( $v_{fa\_a}$ ,  $v_{fa\_b}$ , and  $v_{fa\_c}$  for each technique) represents a signal fed into the positive input node of the comparator. Corresponding to these structures, let's observe the characteristics of operating waveforms as shown in Figure 5.19.

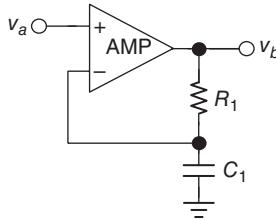
Case (a) in Figure 5.19 shows conventional  $V^2$  control with large  $R_{ESR}$ . The inductor current ripple flows into the output capacitor.  $v_{ESR}$  and  $v_{COUT}$  reflect linear and integral voltage ripples, respectively. With a large  $R_{ESR}$ ,  $v_{OUT}$  ripple reflects the high linearity of  $i_L$ . The inductor current information is converted to  $v_{fa\_a}$  through the fast feedback path. Because the ripple  $v_{fa\_a}$  keeps high linearity to  $i_L$ , the system remains stable without using any extra techniques. Cases (b) and (c) in Figure 5.19 show the techniques with small  $R_{ESR}$ . With small  $R_{ESR}$ ,  $v_{OUT}$  ripple reflects low linearity to that of  $i_L$ . To maintain stability, the differentiator is inserted on the fast path as shown in Figure 5.18, with the operating waveforms in Figure 5.19(b). By neglecting the ripple of ESL, Eq. (5.12) can be expressed as:

$$v_{OUT}(t) = R_{ESR}i_L(t) + \frac{1}{C_{OUT}} \int i_L(t)dt \quad (5.15)$$

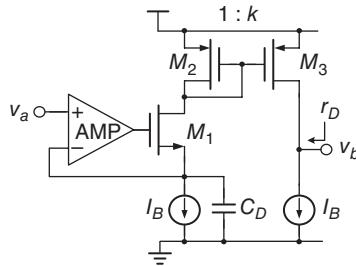
Using the conventional amplifier (AMP)-based differentiator as depicted in Figure 5.20,  $v_{fa\_b}(t)$  can be expressed in the S-domain and the time domain, respectively:

$$\frac{v_b(s)}{v_a(s)} = (sC_1R_1 + 1) \quad (5.16)$$

$$\begin{aligned} v_{fa\_b}(t) &= C_1R_1v'_{OUT}(t) + v_{OUT}(t) \\ &= R_{ESR}C_1R_1 \frac{d}{dt}i_L(t) + \frac{C_1R_1}{C_L}i_L(t) + R_{ESR}i_L(t) + \frac{1}{C_L} \int i_L(t)dt \end{aligned} \quad (5.17)$$



**Figure 5.20** Basic amplifier-based differentiator



**Figure 5.21** VCCS circuit with the differentiator function

Although the inductor current ripple factor is included in Eq. (5.17), the first and third terms still result in undesirable distortion in  $v_{fa\_b}(t)$ . In contrast, one voltage-control current-source (VCCS) circuit [1] as depicted in Figure 5.21 can perform a suitable differentiation function to eliminate the distortion and increase the accuracy.  $v_{fa\_b}(t)$  after the VCCS circuit is expressed in the S-domain and the time domain, respectively:

$$v_b(s) = skC_D r_D v_a(s) \quad (5.18)$$

$$\begin{aligned} v_{fa\_b}(t) &= kC_D r_D \left( R_{ESR} \frac{d}{dt} i_L(t) + \frac{i_L(t)}{C_{OUT}} \right) \\ &= kC_D r_D R_{ESR} \frac{d}{dt} i_L(t) + \frac{kC_D r_D}{C_{OUT}} i_L(t) \end{aligned} \quad (5.19)$$

The parameter  $k$  is the current mirror ratio and  $r_D$  is the equivalent output resistance of the VCCS circuit. By comparing Eqs. (5.19) and (5.17), it's more accurate to recover the inductor current ripple by the VCCS circuit. Without a large ESR, the second term of Eq. (5.19) provides information on the inductor current ripple. However, the first term of Eq. (5.19), which is caused by parasitic ESR, is still undesirable. From the description in Figure 5.19(b),  $v_{fa\_b}(t)$  is composed of four slopes during a switching period. The second rising stage and the fourth falling stage represent the inductor current ripple. The first rising stage and the third falling stage are caused by the ESR. In other words, a larger ESR leads to a larger distortion. As a result,  $v_{fa\_b}(t)$  still suffers from the distortion problem owing to the existing ESR of the output capacitor.

In contrast, with the assistance of the QDI technique, the unwilling ESR-related distortion is completely removed. Consequently, a more accurate ripple of  $v_{fa}$  can achieve better stability. Thus, the QDI technique is expected to recover  $v_{fa\_c}(t)$  as shown in Figure 5.19c.  $v_{fa\_c}(t)$  is then proportional to the inductor current ripple. The QDI circuit not only gets an adequate function to modulate the duty cycle, but also purifies the recovery signal to enhance the signal-to-noise ratio (SNR). As shown in Figure 5.17,  $V^2$  control with the QDI circuit contains two voltage feedback paths.

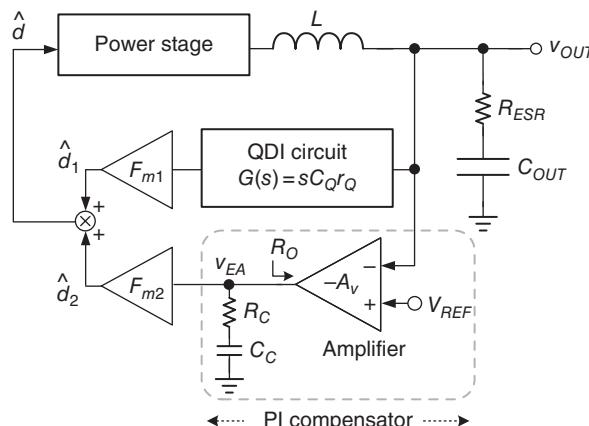
The first path, which is a slow feedback path, compares the output voltage with the reference voltage to decide the error signal. The second path, which is a fast feedback path, is handled by the QDI circuit to obtain the recovery signal and remove the dependence on the ESR. This second voltage path can still react rapidly to the output voltage variation to speed up the transient response. Therefore, a fast transient response can be achieved by the  $V^2$  control scheme with the QDI circuit without adding other fast transient techniques.

### 5.1.5.1 Stability Analysis

Figure 5.22 shows the small signal model of the  $V^2$  control with the QDI circuit, which is inserted between the output voltage node and the PWM modulator  $F_{m1}$ . The QDI circuit works as a differentiator and the transfer function is simply expressed as in Eq. (5.20), where  $C_Q$  and  $r_Q$  constitute an equivalent differential constant in the QDI circuit:

$$G_{VCCS}(s) = skC_Qr_Q \quad (5.20)$$

There are two parallel paths that contribute  $d_1$  and  $d_2$  to adjust the duty cycle  $d$  according to the output voltage. The first path for determining the factor  $d_1$  is composed of  $G_{VCCS}(s)$  and  $F_{m1}$ , which are the transfer functions of the QDI circuit and the comparator, respectively. The second path for determining  $d_2$  is composed of  $A_V(s)$  and  $F_{m2}$ , which are the transfer functions of the amplifier with Type-II compensation and the comparator, respectively. Type-II



**Figure 5.22** Small signal model of the  $V^2$  control buck converter with the QDI technique

compensation is used because the zero generated by small  $R_{SER}$  and  $C_{OUT}$  locates at high frequencies and contributes no compensation. The transfer function of the Type-II compensator is expressed as in Eq. (5.21). Equation (5.22) shows the compensation pole/zero pair, where  $R_O$  is the equivalent output impedance of the AMP:

$$A_{AMP}(s) = A_{v0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \quad (5.21)$$

$$\omega_z = \frac{1}{R_C C_C}, \omega_p = \frac{1}{R_O C_C} \quad (5.22)$$

Therefore, the output-to-duty transfer function can be derived as:

$$\frac{\hat{d}(s)}{v_{OUT}(s)} = \frac{\hat{d}_1(s) + \hat{d}_2(s)}{v_{OUT}(s)} = F_m \left( sC_Q R_Q + A_{v0} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \right) = A_{v0} F_m \left( \frac{\left(1 + \frac{s}{\omega_{zcom1}}\right) \left(1 + \frac{s}{\omega_{zcom2}}\right)}{1 + \frac{s}{\omega_p}} \right) \quad (5.23)$$

Not only can the zero be derived from Type-II compensation, but the structure of the parallel paths can also generate an additional zero. These two zeros,  $\omega_{zcom1}$  and  $\omega_{zcom2}$ , are shown as:

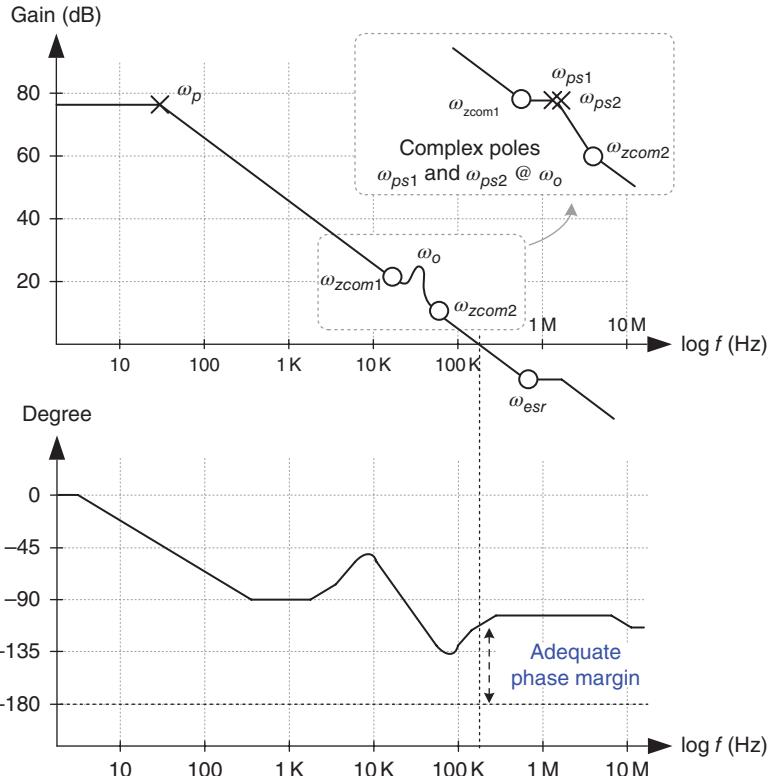
$$\omega_{zcom1}, \omega_{zcom2} = \frac{A_{v0} R_C}{2 C_Q R_Q R_O} \left( 1 \pm \sqrt{1 - \frac{4 C_Q R_Q R_O}{A_v C_C R_C^2}} \right) \quad (5.24)$$

With the transfer function of the power stage in Eq. (5.25), the transfer function of the system loop with the QDI circuit is expressed as:

$$\frac{\hat{v}_{OUT}(s)}{\hat{d}(s)} = G_{d0} \frac{\left(1 + \frac{s}{\omega_{ESR}}\right)}{\left(1 + \frac{1}{\omega_0 Q} s + \frac{1}{\omega_0^2} s^2\right)} \quad (5.25)$$

$$T_{Loop,QDI}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{d}(s)} \cdot \frac{\hat{d}(s)}{\hat{v}_{OUT}(s)} \approx A_v F_m G_{d0} \frac{\left(1 + \frac{s}{\omega_{ESR}}\right) \left(1 + \frac{s}{\omega_{zcom1}}\right) \left(1 + \frac{s}{\omega_{zcom2}}\right)}{\left(1 + \frac{1}{\omega_0 Q} s + \frac{1}{\omega_0^2} s^2\right) \left(1 + \frac{s}{\omega_p}\right)} \quad (5.26)$$

Figure 5.23 depicts the Bode plot of the  $V^2$  control buck converter with the QDI technique. The system dominant pole  $\omega_p$  is determined by the Type-II compensator. Two zeros,  $\omega_{zcom1}$  and  $\omega_{zcom2}$ , are used to cancel the effect of the complex pole from the LC filter at the output stage. With a small ESR, the zero  $\omega_{ESR}$  typically appears at very high frequencies. As a result, system stability can be guaranteed even though a small ESR is used.



**Figure 5.23** Frequency response of the  $V^2$  control buck converter with the QDI technique

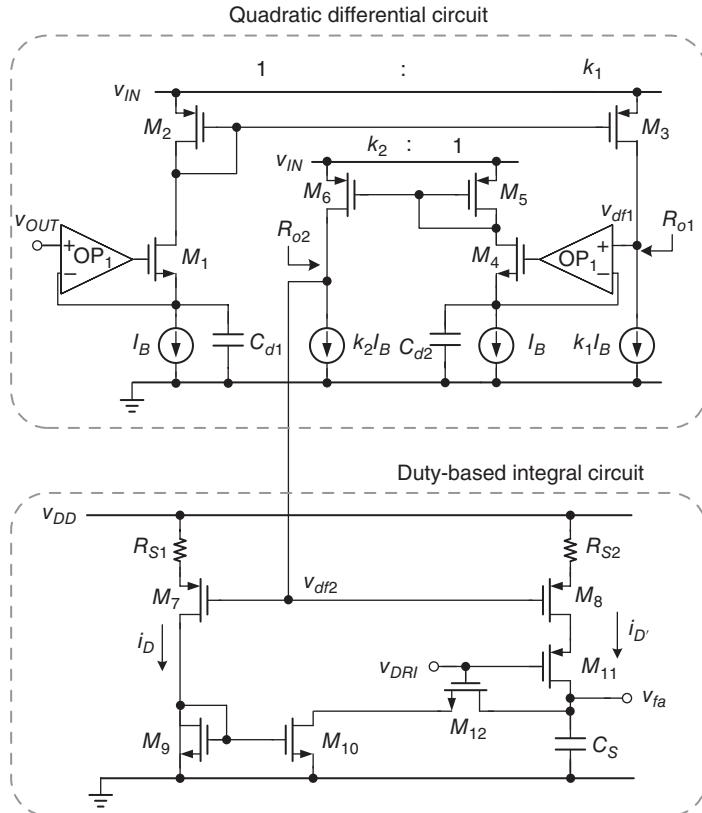
### 5.1.5.2 Circuit Implementation of QDI

Figure 5.24 shows a circuit implementation of the QDI technique including two stages, a quadratic differential circuit and a duty-based integral circuit. The quadratic differential circuit is composed of two cascaded VCCS structures. The VCCS structure can provide a differentiation function. After the first differentiation, the signal  $v_{df1}$  contains the undesirable first term in Eq. (5.27). After the second differentiation, the signal  $v_{df2}$  contains only information on the slope of the inductor current ripple, as shown in Eq. (5.28). In other words, the ESR effect is eliminated at this moment.

$$v_{df1}(t) = \frac{d}{dt} v_{OUT}(t) = \tau_1 \left( R_{ESR} \frac{d}{dt} i_L(t) + \frac{i_L(t)}{C_L} \right) \quad (5.27)$$

$$v_{df2}(t) = \frac{d}{dt} v_{df1}(t) = \tau_1 \tau_2 \left( \frac{1}{C_L} \frac{v_{IN} - v_{OUT}}{L} \right) \quad (5.28)$$

Through the integration stage,  $v_{fa(t)}$  can be expressed as in Eq. (5.29).  $v_{fa(t)}$  is purely proportional to the inductor current ripple  $i_L$ . The accuracy of  $v_s$  is then further enhanced compared with the previous results, which suffer from ESR-related distortion.



**Figure 5.24** QDI implementation circuit

$$v_{fa}(t) = \int v_{df2}(t) dt = \frac{\tau_1 \tau_2}{C_L} i_L(t) + \tau_3 \quad (5.29)$$

Here,  $\tau_1$ ,  $\tau_2$ , and  $\tau_3$  are constants generated in the procedure of differentiation and integration. As mentioned in Eq. (5.18), the transfer function of the cascaded VCCS structure can be expressed as:

$$\frac{v_{df2}(s)}{v_{OUT}(s)} = (sk_1 C_{d1} R_{O1})(sk_2 C_{d2} R_{O2}) \quad (5.30)$$

In the integral circuit, according to the PWM signal,  $V_{DRI}$ , the currents  $i_D$  and  $i_{D'}$  flow into the capacitor  $C_s$  during on-time and off-time periods, respectively, to achieve the integration function. The transfer function of the integral circuit can be derived in Eq. (5.31), where  $g_{m7}$  and  $g_{m8}$  are the transconductances of MOSFETs  $M_7$  and  $M_8$ , respectively:

$$\begin{cases} \frac{v_{fa}(s)}{v_{df2}(s)} = \frac{1}{sC_s(1/g_{m8} + R_{s1})} & \text{during on-time period} \\ \frac{v_{fa}(s)}{v_{df2}(s)} = \frac{1}{sC_s(1/g_{m7} + R_{s2})} & \text{during off-time period} \end{cases} \quad (5.31)$$

Corresponding to the transfer function of QDI as shown in Figure 5.22, the exact transfer function of the QDI circuit is shown in Eq. (5.32) with the equivalent capacitance  $C_Q$  and resistance  $R_Q$  as in Eq. (5.33):

$$G_{QDI}(s) = \frac{v_s(s)}{v_{OUT}(s)} = \frac{(sk_1 C_{d1} R_{O1})(sk_2 C_{d2} R_{O2})}{sC_s(1/g_m + R_s)} = \frac{s}{C_s(1/g_m + R_s)/k_1 k_2 C_{d1} C_{d2} R_{O1} R_{O2}} = s C_Q R_Q \quad (5.32)$$

$$C_Q = \frac{k_1 k_2 C_{d1} C_{d2}}{C_s} \text{ and } R_Q = \frac{R_{O1} R_{O2}}{1/g_m + R_s} \quad (5.33)$$

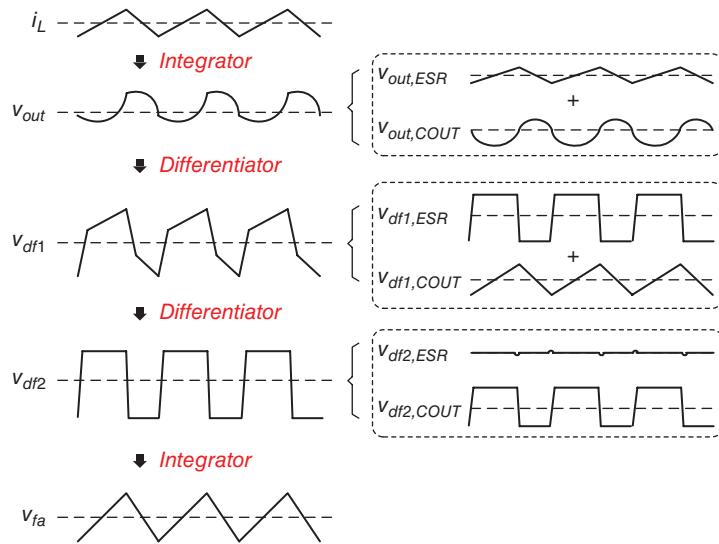
The coefficients  $k_1$  and  $k_2$  are the current mirror ratios in the two-stage VCCS structure. According to Eq. (5.32), the equation in the S-domain between  $v_{fa}(s)$  and  $v_{OUT}(s)$  is derived in Eq. (5.34), and the equation in the time domain between  $v_{fa}(t)$  and  $v_{OUT}(t)$  is then derived in Eq. (5.35):

$$v_{fa}(s) = \frac{1}{s} \cdot \frac{k_1 k_2 C_{d1} C_{d2} R_{O1} R_{O2}}{C_s(1/g_m + R_s)} \cdot s^2 \cdot v_{OUT}(s) \quad (5.34)$$

$$\begin{aligned} v_{fa}(t) &= \frac{k_1 k_2 C_{d1} C_{d2} R_{O1} R_{O2}}{C_s(1/g_m + R_s)} \int \left( \frac{d^2}{dt^2} \left( R_{ESR} i_L(t) + \frac{1}{C_L} \int i_L(t) dt \right) \right) dt \\ &\Rightarrow \begin{cases} v_{fa}(t) = \frac{k_1 k_2 C_{d1} C_{d2} R_{O1} R_{O2}}{C_s C_L (1/g_{m8} + R_{s1})} i_L(t) \propto i_L(t) & \text{during on-time period} \\ v_{fa}(t) = \frac{k_1 k_2 C_{d1} C_{d2} R_{O1} R_{O2}}{C_s C_L (1/g_{m7} + R_{s2})} i_L(t) \propto i_L(t) & \text{during off-time period} \end{cases} \end{aligned} \quad (5.35)$$

There are no ESR-dependent terms in Eq. (5.35), because the distortion caused by the ESR is eliminated by the QDI circuit. Consequently, the QDI function can recover a pure inductor current ripple from the output voltage ripple when a small ESR is used. Besides, compared with conventional current-sensing circuits, the QDI can also save much power consumption. Furthermore, the recovery function is not constrained by the load range. Therefore, large equivalent differential constants,  $C_Q$  and  $R_Q$ , can be generated without the implementation of large resistors and capacitors. Hence, the QDI circuit not only confirms the stability but also benefits the reduction in cost of the active silicon area. For example, the capacitors  $C_{d1}$  and  $C_{d2}$  have the same small value of 0.5 pF and the capacitor  $C_s$  is approximately equal to 2 pF, since the constants  $k_1$  and  $k_2$  are used to reduce the requirement of large on-chip capacitors.

Figure 5.25 depicts the operating waveform of the QDI circuit. According to Figure 5.24, the process of the QDI can be divided into three stages with the output voltage,  $v_{df1}$ ,  $v_{df2}$ , and  $v_{fa}$ . The component of the voltage cross  $R_{ESR}$  deteriorates the recovering function, as explained in Figure 5.19. By this response the voltage components from  $R_{ESR}$  and  $C_{OUT}$  are depicted for  $v_{OUT}$ ,  $v_{df1}$ , and  $v_{df2}$  to explain how to remove the influence from the voltage cross  $R_{ESR}$ . Through  $R_{ESR}$  and  $C_{OUT}$ ,  $v_{OUT}$  information is derived in  $i_L$ . Through the differentiation in the first stage of QDI,  $v_{out,ESR}$  with triangular waveform becomes  $v_{df1,ESR}$  with rectangular waveform, and  $v_{out,COUT}$  is recovered to  $v_{df1,COUT}$  with triangular waveform. Through the differentiation in the second stage of QDI,  $v_{df1,ESR}$  becomes  $v_{df2,ESR}$  with spike, and  $v_{df1,COUT}$



**Figure 5.25** Operating waveform of the QDI circuit

becomes  $v_{dif2,COUT}$  with rectangular waveform. Through the integration function in the final stage,  $v_{dif2,COUT}$  is recovered to the triangular waveform while  $v_{dif2,ESR}$  contributes almost no result to  $v_{fa}$  because the spike of  $v_{dif2,ESR}$  is composed of high-frequency elements. As a result, the QDI can benefit the recovery function without being influenced by  $R_{ESR}$ .

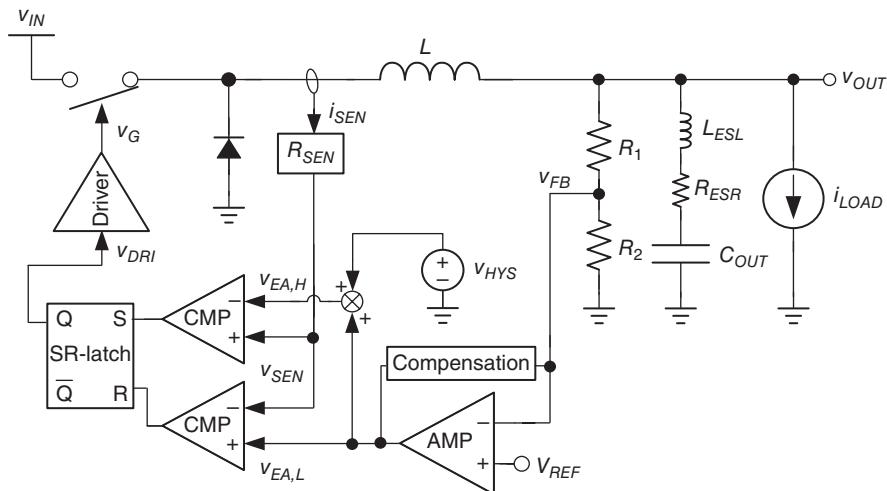
### 5.1.6 Robust Ripple Regulator (R3)

Ripple-based control has an inherent fast transient advantage. As we mentioned before, the control of the power converter includes the set and reset operations to determine the starting of the on-time and the off-time period, respectively. The COT control has the ability to adjust the off-time period. Thus, the switching frequency can be changed in case of any load change. Once the load changes from light to heavy, the shortened off-time effectively increases the switching frequency for a fast transient response. On the contrary, in case of a heavy to light load change, both the high-side and the low-side are turned off to enter the diode emulation mode and further extend the off-time period. A load-dependent switching frequency can ensure the power-saving advantage. However, if considering in detail the scenario where the load changes during the on-time period, the COT control loses its ability to dynamically adjust the on-time period since the constant on-time is calculated by the input and output voltages. Here, we can say that the pre-defined on-time limits the flexibility of the on-time period if the load changes instantly and during the on-time period. To release the constraint set by the constant on-time, some ripple-based control methods can be thought of as possible control techniques to improve the overall performance.

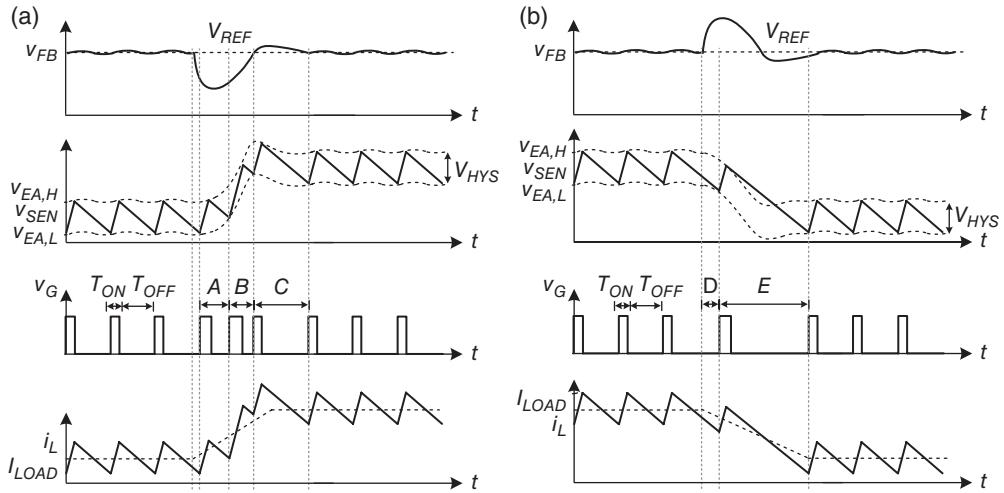
Hysteresis control methods are one possible solution to get both flexibility in modulating on-time and off-time at the same time. First of all, observing voltage-ripple-based (VRB) hysteresis can have some disadvantages. The output voltage ripple limits the allowable voltage

hysteresis window. That is to say, the smaller the hysteresis is, the smaller the noise margin is. This causes unstable operation if a small ESR value is used. Although the compensation offset voltage can be inserted in both the upper and the lower bonds to solve the unstable problem, the need for a large ESR sets the constraint of selecting the output capacitor. Furthermore, owing to the hysteresis operation, it is hard to retrieve the switching frequency and derive equally divided phases if a multiple-phase technique is needed. The advantage of the VRB hysteresis control is that the output voltage can be limited within the voltage hysteresis window and the accuracy can be ensured within a certain percentage.

In contrast, the current-ripple-based (CRB) hysteresis control can be a possible solution. The inductor current is regulated within the predefined hysteresis window, which is similar to the output voltage of the VRB regulated within the voltage hysteresis window. However, some obvious disadvantages of the CRB need to be addressed. The crucial problem is that the output voltage is floating without being regulated because there is no feedback from the output voltage. The CRB hysteresis control needs an additional voltage feedback loop to regulate the output voltage, as shown in Figure 5.26. The  $R_{SEN}$  block can sense the AC inductor current ripple. The feedback path needs to include one integrating error amplifier to improve the regulation performance of the output voltage. The output  $v_{EA,L}$  of the error amplifier can be set as the lower bond of the CRB hysteresis window. With an additional and constant value of  $V_{HYS}$  as the hysteresis window, the output voltage ripple can be kept constant without being affected by any disturbance. As we know, the changing rate of  $v_{EA,L}$  determines the transient response time of the CRB hysteresis control. Moreover, the changing rate of  $v_{EA,L}$  is completely controlled by the compensation techniques used in the converter. There is a trade-off between the fast transient response, which benefits from CRB control and the regulation accuracy, which benefits from the error amplifier. Please refer to the compensation skills in Chapter 3. Type III is recommended to let the converter behave well with high accuracy and well-regulated output voltage.



**Figure 5.26** Conventional CRB hysteresis control with additional voltage feedback for improving output voltage regulation

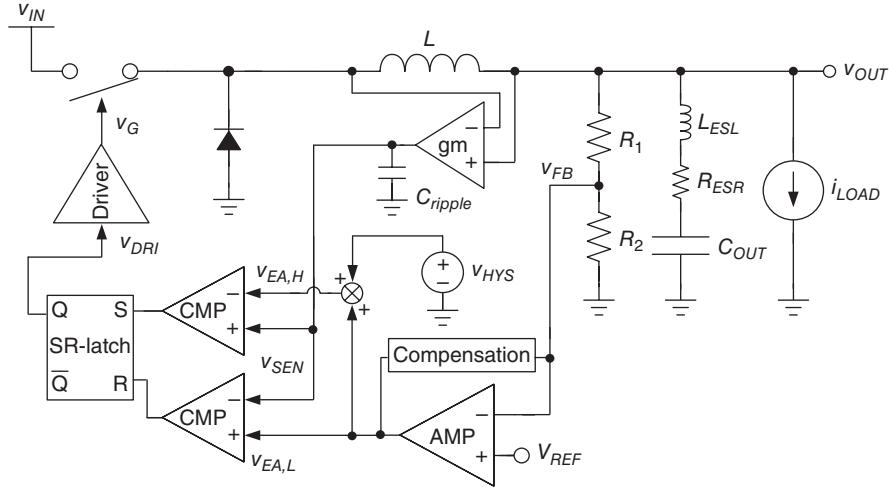


**Figure 5.27** Operating waveform at (a) light-to-heavy load transient and (b) heavy-to-light load transient

Besides, the derivation of the switching frequency through the current ripple is still difficult and thus the interleaving technique is hard to apply. Furthermore, full inductor current sensing is a challenge if the sensing method is an on-chip technique. Any switching noise may deteriorate the sensing performance and thereby cause an undesired unstable operation with increased output voltage ripples.

Figure 5.27 shows the waveform in the transient process to illustrate the fast transient. The rising and falling slopes of  $v_{SEN}$  in the on-time and off-time periods are constant, respectively. In steady state, the on-time and off-time periods are fixed, modulated by the ripple of  $v_{SEN}$  and the fixed hysteretic window. The DC level of  $v_{EA,L}$  is proportional to the loading conditions. During the transient from light to heavy load as shown in Figure 5.27(a), a dynamical increase in  $v_{EA,L}$  can adjust the on-time and off-time periods. Periods A, B, and C illustrate that the on-time period extends and the off-time period shrinks. The duty cycle enlarges and the switching frequency becomes higher, so that sufficient power can be delivered instantly to the output to recover the voltage drop. During the transient from heavy to light load as shown in Figure 5.27 (b), periods D and E illustrate that the on-time period shrinks and the off-time period extends so that the transient performance is enhanced. Consequently, compared with other methods of ripple-based control, voltage-mode hysteresis control with an extra current loop can further improve the transient response because of the lack of constraints in the fixed on-time period, off-time period, and switching frequency.

In order to get rid of the switching noise, Figure 5.28 uses one voltage-to-current converter, which is a transconductance ( $gm$ ) amplifier to generate a clean pseudo-inductor AC current ripple. One ripple capacitor  $C_{ripple}$  at the output of the  $gm$  amplifier can generate the ripple signal  $v_{SEN}$  to represent (reflect) the inductor current ripple. Owing to  $C_{ripple}$ , the switching noise can be reduced to get a noise-reduction sensing signal  $v_{CS}$ . In the frequency domain, the insertion of  $C_{ripple}$  can generate one low-frequency zero to alleviate the LC double pole effect. In other words, the whole system becomes a one-pole system. Type-I compensation



**Figure 5.28** Robust ripple regulator using the regeneration of the inductor AC current ripple as PWM signal

can be used to achieve a fast transient response at the cost of the regulation performance, because a trade-off exists between system stability and regulation performance. The transient response can be as fast as that of COT control. For highly precise output supply requirements, Type II is recommended to compensate the whole system for high performance. High low-frequency gain and high bandwidth can be guaranteed at the same time after Type-II compensation. However, the BW is still limited within 10–20% of the switching frequency and thus the transient response is still slower than that of COT control. Consequently, the conclusion is that a good transient response and excellent regulation can be achieved with the implementation in Figure 5.28.

## 5.2 Analysis of Switching Frequency Variation to Reduce Electromagnetic Interference

Table 5.1 lists the characteristics and performance of three common control methods for the DC/DC buck converter. Using ripple-based on-time control (RBOTC) [2–21] for the buck converter meets the requirements of Soc because it exhibits the best performance compared with PWM CMC and PWM VMC [11, 22–29].

A comparison of the line transient responses of each control method shows that the PWM CMC exhibits better performance than the PWM VMC because the disturbance that occurs at the input voltage directly influences the inductor current, which can be sensed from the CF path. However, the response is constrained because the duty ratio is controlled by  $v_{EA}$ , the output of the voltage error amplifier with limited bandwidth. By contrast, RBOTC exhibits a faster transient response because the duty ratio is instantly adjusted by the variation that occurs at  $v_{OUT}$ . Similarly, RBOTC exhibits a fast load transient response. Considering the load range, PWM CMC exhibits poor performance because the current-sensing range is restricted by

**Table 5.1** Characteristics of three common control methods for DC/DC buck converter

	PWM CMC	PWM VMC	RBOTC
Line transient response	Good	Poor	Excellent
Load transient response	Good	Good	Excellent
Load range	Poor	Good	Excellent
Conversion ratio range	Poor	Poor	Excellent
Conversion ratio	Poor	Good	Excellent
Quietest current	Poor	Good	Excellent
Output ripple	Excellent	Excellent	Poor (w/i SP-CAP) Excellent (w/i MLCC)
PFM at DCM for efficiency enhancement	Complex	Complex	Excellent (inherence)
Rejection of frequency variation at CCM	Excellent	Excellent	Poor

SP-CAP, specialty polymer capacitor. PFM, pulse frequency modulation.

the limited bandwidth of the current-sensing circuit. Moreover, the frequency response of PWM CMC and PWM VMC depends on the output loading conditions. As for the conversion ratio, PWM CMC exhibits poor performance because the current-sensing circuit has a limited bandwidth. Thus, an extreme duty ratio results in a short period that enables current information to be sensed. The current-sensing circuit also consumes extra power.

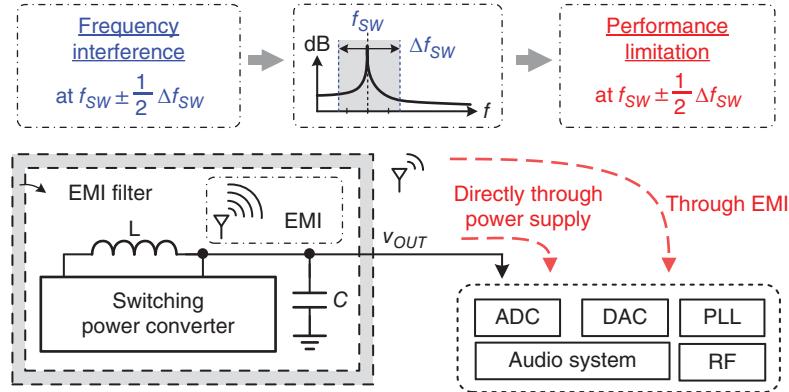
In contrast, the performance of the output ripple for RBOTC is constrained by the output capacitor for stability issue as discussed in Section 4.2. The constraint of selecting output capacitor with a large ESR is successfully overcome so that the output ripple can be further reduced if MLCCs are used [4–10, 29]. (This consideration will be introduced in detail later.)

Another constraint is that RBOTC is a clock-free architecture because of its ripple-based control architecture. As such, RBOTC suffers from severe switching frequency variation ( $\Delta f_{SW}$ ) caused by disturbances from the change in input voltage ( $v_{IN}$ ), output voltage ( $v_{OUT}$ ), and loading current ( $i_{Load}$ ).

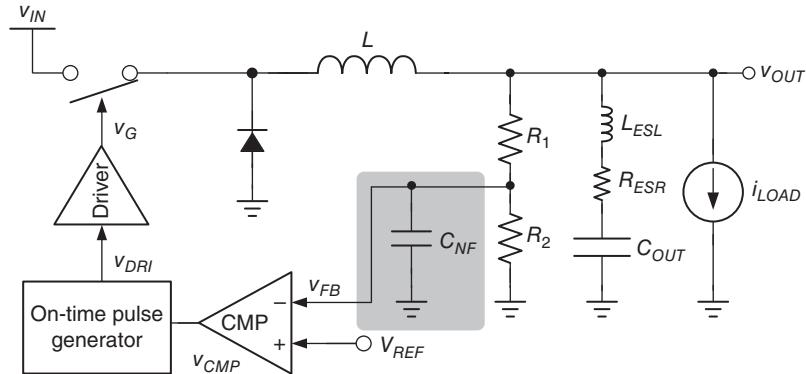
In other words, a power converter with RBOTC becomes a frequency interference source in the range of  $f_{SW} \pm 0.5\Delta f_{SW}$ , which is a disadvantage. Analog circuits, such as radio frequency, audio system, analog-to-digital (ADC) converters, digital-to-analog (DAC) converters, and phase-locked loop (PLL) circuits, are sensitive to a certain level of  $\Delta f_{SW}$  because the frequency variation degrades their performance, as shown in Figure 5.29. Given the frequency interference with surrounding circuits through EMI, a constant  $f_{SW}$  in standing wave ratios is expected because the known noise spectrum with a small  $\Delta f_{SW}$  can be utilized to design the noise-filtering circuit for low EMI.

### 5.2.1 Improvement of Noise Immunity of Feedback Signal

Ripple-based control techniques inherently lead to an unexpected frequency variation because the modulation is determined by a small output voltage ripple and the reference voltage. Consequently, on the feedback path, the feedback signal  $v_{FB}$  with low noise immunity is easily disturbed by any perturbation, possibly from parasitic capacitive or inductive coupling paths.



**Figure 5.29** Frequency interference from SWRs limits the performance of analog circuits at  $f_{SW} \pm 0.5\Delta f_{SW}$



**Figure 5.30** Noise filter on the feedback path

Increasing the quiescent current to suppress the voltage variation by coupling noise is one of the methods used to easily enhance the noise immunity. However, efficiency is sacrificed. The use of an additional ramp signal or additional inductor current information can also improve the noise immunity and enhance the stability. Several well-known techniques have recently been developed to solve these problems, and these will be introduced here.

### 5.2.2 Bypassing Path to Filter the High-Frequency Noise of the Feedback Signal

Figure 5.30 shows that a bypass capacitor  $C_{NF}$  can provide a noise-filtering path to filter out high-frequency interference at  $v_{FB}$ . However, a pole, which is constituted by  $R_1 \parallel R_2$  and  $C_{NF}$ , causes phase delay on the feedback path. The phase margin is deteriorated and the system may suffer from sub-harmonic oscillation. Selection of the noise-filtering capacitor will influence

converter stability and performance. Thus, the appropriate noise-filtering design is needed if noise immunity and system stability are considered simultaneously.

### 5.2.2.1 Feedforward Path to Enlarge the Feedback Signal

Figure 5.31 shows another approach to improve the noise immunity by adding one feedforward capacitor  $C_{FF}$  placed parallel with the feedback resistor  $R_1$ .  $C_{FF}$  provides the feedforward path for high-frequency components at  $v_{OUT}$  directly summed at  $v_{FB}$ . Specifically, the direct feedforward path equivalently increases the magnitude of the feedback voltage ripple of the feedback signal from the conventional feedback divider.

With the addition of  $C_{FF}$ , the transfer function of the output voltage to the feedback voltage is derived and expressed as follows:

$$\frac{\hat{v}_{FB}(s)}{\hat{v}_{OUT}(s)} = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + sR_1 C_{FF})}{(1 + s(R_1 \| R_2)C_{FF})} \quad (5.36)$$

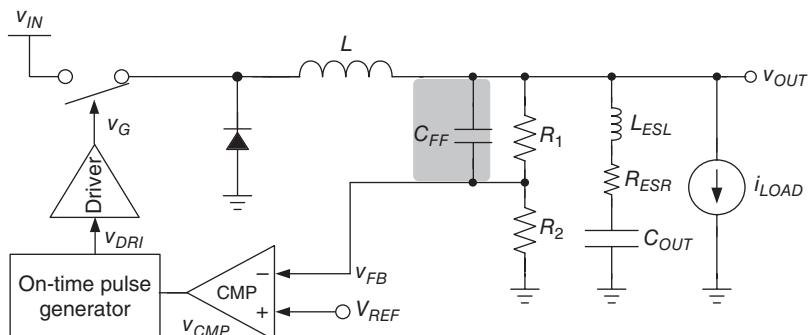
Equivalently, the feedforward capacitor contributes one pole/zero pair. The feedforward capacitor can work correctly only if the position of the pole is higher than that of zero:

$$pole = \frac{1}{(R_1 \| R_2)C_{FF}} >> zero = \frac{1}{R_1 C_{FF}} \quad (5.37)$$

Moreover, the designed zero is assumed to locate around the switching frequency to effectively conduct the inductor current ripple through the additional feedforward path, as expressed in Eq. (5.38). The transfer function of the inductor current to the feedback voltage can also be derived as in Eq. (5.40), if Eqs. (5.38) and (5.39) are substituted in Eq. (5.36):

$$(R_1 \| R_2) \cdot C_{FF} \approx R_{ESR} C_{OUT} \quad (5.38)$$

$$\frac{\hat{v}_{OUT}(s)}{\hat{i}_L(s)} \approx R_{ESR} + \frac{1}{sC_{OUT}} \quad (5.39)$$



**Figure 5.31** Additional feedforward capacitor  $C_{FF}$  improves noise immunity

$$\frac{\hat{v}_{FB}(s)}{\hat{i}_L(s)} \approx \frac{R_2}{R_1 + R_2} \cdot \frac{1 + s \left( \frac{R_1 + R_2}{R_2} \right) R_{ESR} C_{OUT}}{s C_{OUT}} \quad (5.40)$$

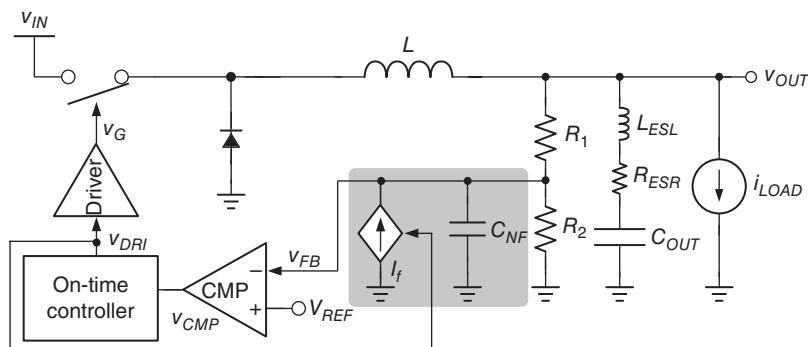
The additional zero is effectively pushed toward the origin through increasing  $R_{ESR}$  by a factor of  $(R_1 + R_2)/R_2$ . Consequently,  $C_{FF}$  not only increases the ripple of  $v_{FB}$ , but also releases the limitation of the large time constant constituted by  $R_{ESR}$  and  $C_{OUT}$ .

### 5.2.2.2 Active Controller to Enlarge the Feedback Signal (Patent-US 6958594)

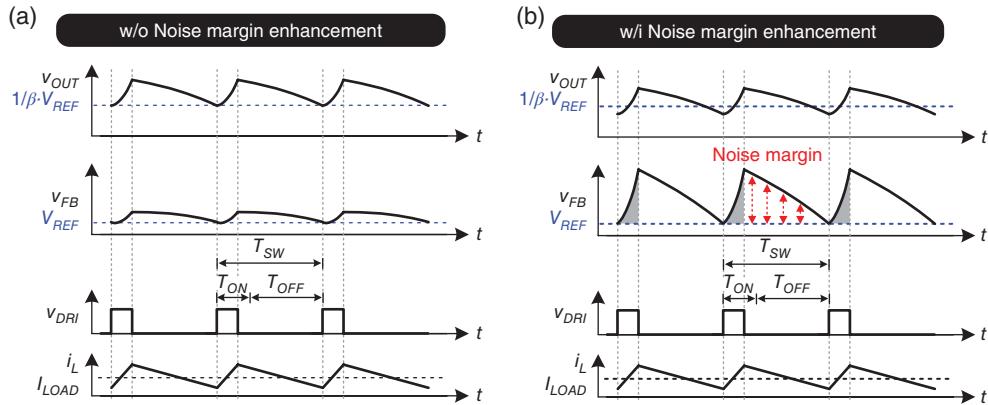
Enlarging the difference voltage between two terminals, namely  $v_{FB}$  and  $V_{REF}$ , which are the two inputs of the comparator, is important to improve noise immunity. The definition of the noise margin indicates the difference voltage between the two inputs of the comparator. If the difference voltage is large, then the converter can be free from noise interference. In Figure 5.32, one current source  $I_f$ , which is controlled by the on-time controller, is used to increase the difference voltage between two terminals of the comparator corresponding to the on-time period.

The voltage on  $C_{NF}$  is charged by the on-time controlled current source. In this study, a low input voltage indicates a large on-time value and the need for a large difference voltage. By contrast, a high input voltage has a small on-time value and a small voltage difference enhancement in this technique. Considering the adaptive ramp signal generated by the constant current source, the difference voltage between  $v_{FB}$  and  $V_{REF}$  can be enlarged inversely proportional to the input voltage. In other words, distinguishing the voltage difference between  $v_{FB}$  and  $V_{REF}$  becomes easy. Thus, the noise immunity is improved. Figure 5.33(a) shows the waveforms without NME. Thus, any noise from the coupling effects will deteriorate the regulation performance. By contrast, Figure 5.33(b) shows the advantage of enlarging the difference voltage to obtain high noise immunity, where the parameter  $\beta$  is the ratio of  $R_2$  over  $R_1 + R_2$ . A large noise margin can tolerate a large noise from the coupling effects.

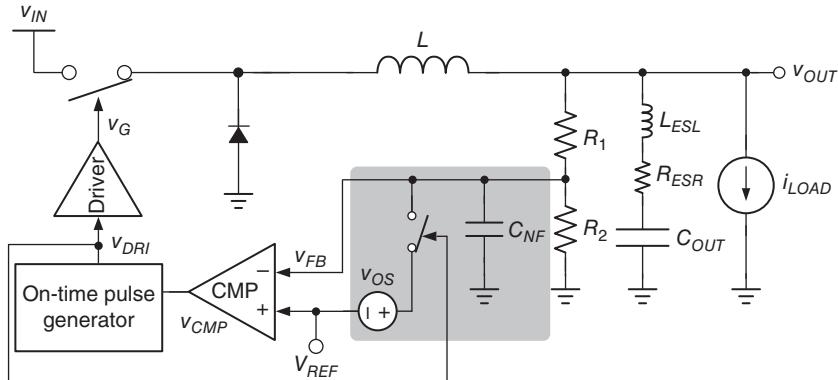
In Figure 5.33, the on-time period is relatively short to generate an adequate difference voltage under the high input voltage condition. One possible scenario may fail to ensure a sufficient difference voltage to inhibit the sub-harmonic effect. Thus, a robust and flexible method as



**Figure 5.32** Noise margin is enhanced by a constant current source



**Figure 5.33** (a) Poor noise margin and low noise immunity. (b) Noise margin is enhanced by the addition of one current source corresponding to the adaptive on-time value

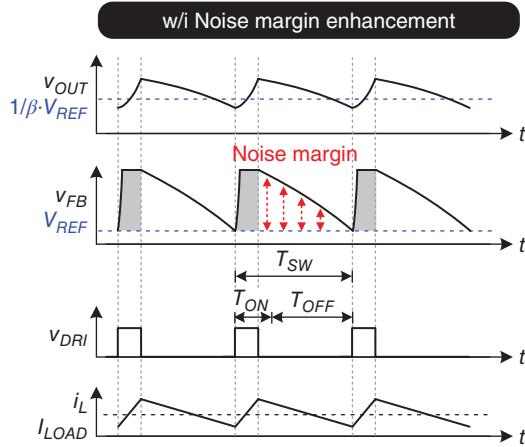


**Figure 5.34** Noise margin is enhanced by a constant DC offset voltage

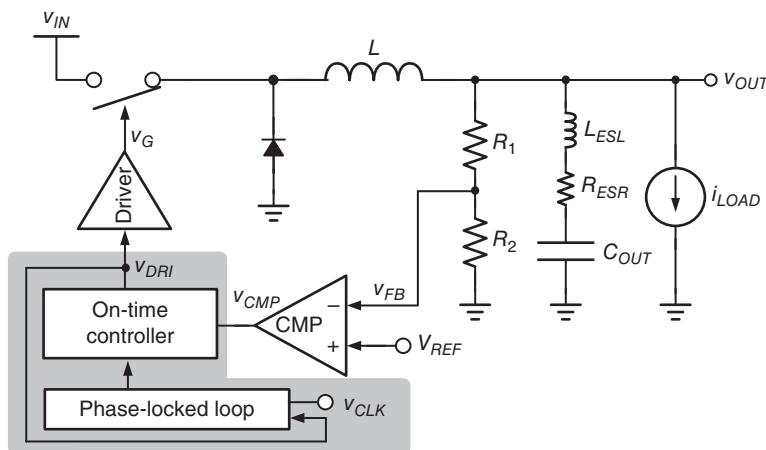
presented in Figure 5.34 can enhance the noise margin by using an additional constant offset voltage  $V_{OS}$  without being affected by the adaptive on-time period. Figure 5.35 shows the waveforms that illustrate the correct operation. Any noise will not cause large frequency variations. This phenomenon is assumed to be a pseudo-constant switching frequency control. The EMI problem can be alleviated by enhancing the noise margin. However, the additional offset voltage distorts the DC level of the feedback signal in case of the additional DC offset voltage. The offset voltage can be discharged through the resistors but can influence the DC regulation of the output voltage, which is an evident disadvantage.

### 5.2.3 Technique of PLL Modulator

The PLL modulator is applied to on-time control to maintain a constant operating frequency in steady state even under different  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$  [11, 12, 23–26]. The



**Figure 5.35** Noise margin is enhanced by the addition of one constant DC offset voltage without being affected by the adaptive on-time value



**Figure 5.36** Switching frequency of the converter can be synchronized with  $v_{CLK}$  from the Soc through the PLL modulator

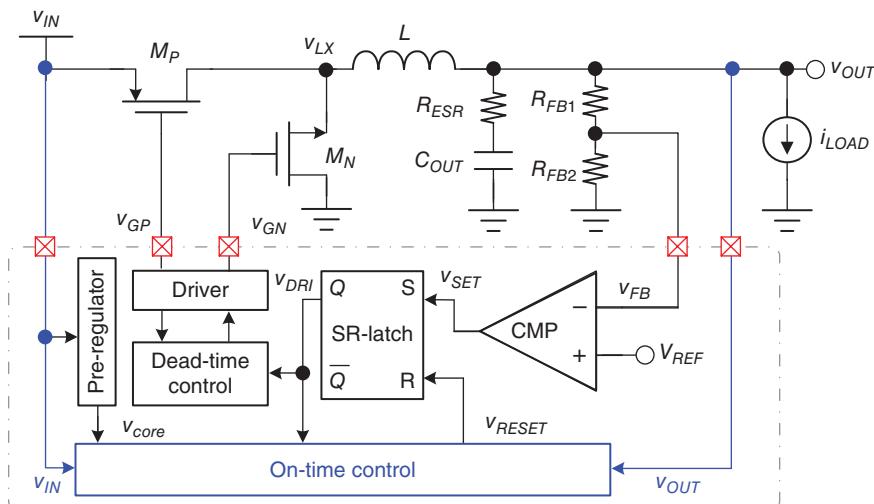
PLL modulator can control the on-time controller and adjust the corresponding on-time period based on the reference constant clock signal, which originates from the Soc, to synchronize the switching frequency without being influenced by any disturbances. By intuition, the performance can be improved significantly by the PLL modulator. However, the circuit architecture becomes complex. Thus, both the cost and the quiescent power loss increase (Figure 5.36).

### 5.2.4 Full Analysis of Frequency Variation under Different $v_{IN}$ , $v_{OUT}$ , and $i_{LOAD}$

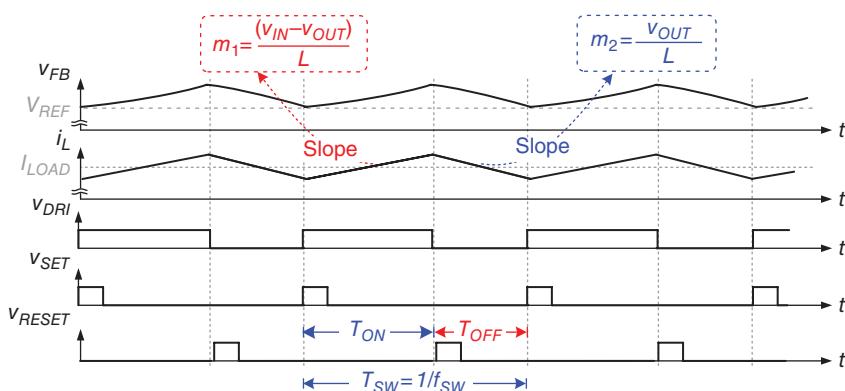
#### 5.2.4.1 Operation of On-Time Control Switching Converter

Figure 5.37 shows the conventional architecture of the DC/DC buck converter with on-time control. The pre-regulator converts the input voltage ( $v_{IN}$ ) into the core voltage ( $v_{core}$ ) to supply the controllers, which are designed by core devices. The feedback loop monitors the feedback voltage ( $v_{FB}$ ) using the voltage divider to regulate  $v_{OUT}$ . The feedback loop mainly comprises the comparator (CMP), on-time timer, and slew rate (SR)-latch.

Figure 5.38 illustrates the timing diagram in the steady state, where the inductor current  $i_L$  conforms to the principle of voltage-second balance for stable regulation. The switching cycle



**Figure 5.37** Architecture of conventional on-time controlled DC/DC buck converter



**Figure 5.38** Timing diagram of the on-time controlled DC/DC buck converter

starts at the beginning of  $T_{ON}$ , which is triggered by the setting signal  $v_{SET}$  and terminated by the resetting signal  $v_{RESET}$ .  $v_{SET}$  is the output of the CMP and reflects the energy request from the output voltage. By contrast,  $v_{RESET}$  is the output of the on-time timer to switch the on-time period to the off-time period. The operation during  $T_{ON}$  refers to the charging path to increase the inductor current.  $T_{ON}$  is triggered when  $v_{FB}$  falls below the reference voltage  $V_{REF}$ . The duty ratio  $D$  is determined by the relationship between the input voltage  $v_{IN}$  and the output voltage  $v_{OUT}$ . Consequently, the switching frequency  $f_{SW}$  in the on-time control can be determined by the pre-defined  $T_{ON}$  and its corresponding  $D$ , where  $T_{ON}$  has some constraints to ensure system stability.

#### 5.2.4.2 Analysis of Switching Frequency Variation

The switching frequency of the buck converter in the CCM is expressed as:

$$f_{SW} = D \cdot \frac{1}{T_{ON}} \quad (5.41)$$

Ideally, the slope of  $i_L$  is proportional to  $v_{IN} - v_{OUT}$  and  $-v_{OUT}$  during the on-time and off-time periods, respectively. The ideal duty ratio ( $D_{ideal}$ ) is equal to the ratio of  $v_{OUT}$  to  $v_{IN}$  in a lossless ideal case, as shown in Eq. (5.42), if  $v_{OUT}$  is well regulated:

$$D_{ideal} = \frac{v_{OUT}}{v_{IN}} \quad (5.42)$$

Similarly, the ideal on-time period  $T_{ON(ideal)}$  in the conventional architecture should be proportional to  $v_{OUT}/v_{IN}$  in Eq. (5.43) if the switching period  $T_{SW}$  ( $=1/f_{SW}$ ) is constant:

$$T_{ON(ideal)} = \frac{v_{OUT}}{v_{IN}} \cdot T_{SW} = D_{ideal} \cdot T_{SW} = \frac{D_{ideal}}{f_{SW}} \quad (5.43)$$

The switching frequency  $f_{SW}$  can then be expressed as:

$$f_{SW} = D_{ideal} \cdot \frac{1}{T_{ON(ideal)}} \quad (5.44)$$

Moreover, Eq. (5.45) expresses the actual duty ratio ( $D_{actual}$ ), which is defined as the ratio of the actual on-time period  $T_{ON(actual)}$  to  $T_{SW}$  in Eq. (5.46):

$$D_{actual} = \frac{T_{ON(actual)}}{T_{SW}} = T_{ON(actual)} \cdot f_{SW} \quad (5.45)$$

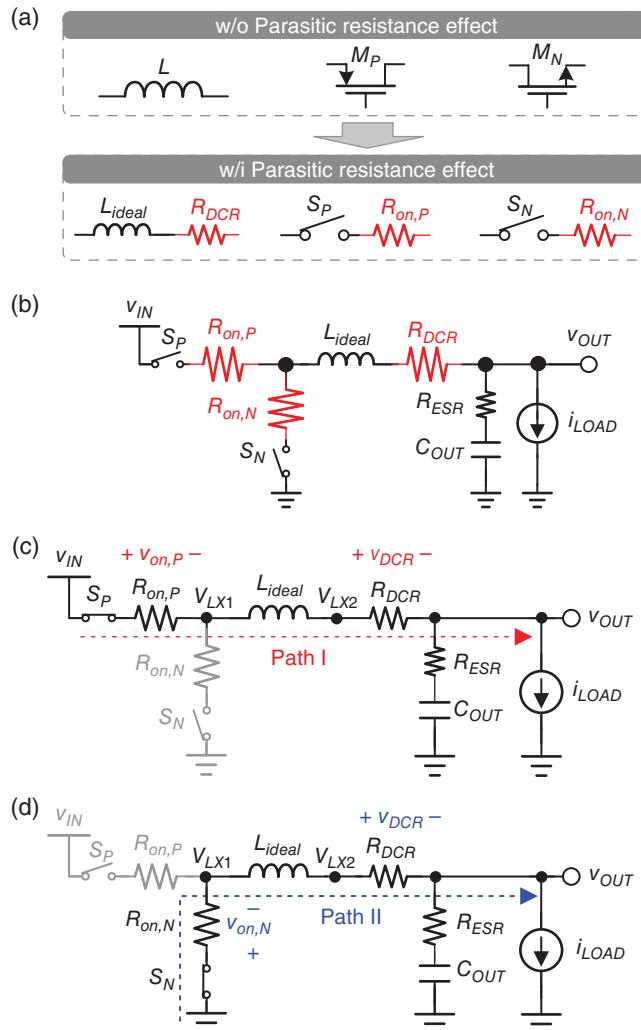
$$\text{where } T_{SW} = T_{ON(actual)} + T_{OFF(actual)} \quad (5.46)$$

Therefore, the constant switching frequency  $f_{SW}$  is expressed as:

$$f_{SW} = \frac{1}{T_{SW}} = \frac{D_{actual}}{T_{ON(actual)}} \quad (5.47)$$

$D_{actual}$  is larger than  $D_{ideal}$  because more energy should be derived from the power source if the possible power loss is considered when all parasitic effects are included.  $f_{SW}$  is also drastically perturbed by different  $v_{IN}$ ,  $v_{OUT}$ , and loading current  $i_{Load}$ , because  $T_{ON(ideal)}$  in Eq. (5.43) cannot compensate for the change in  $D_{actual}$ .

To completely analyze the influence of  $\Delta f_{SW}$ , Figure 5.39(a) is discussed with the addition of parasitic resistance, including the direct current resistance of the inductor ( $R_{DCR}$ ), as well as the on-resistance  $R_{on,P}$  and  $R_{on,N}$  of the power MOSFETs,  $M_P$  and  $M_N$ , respectively. Figure 5.39(b) shows the actual and non-ideal power stage of the buck converter if parasitic resistances are considered. Figure 5.39(c), (d) illustrates the energy delivery paths, including paths I and II,



**Figure 5.39** (a) Consideration of parasitic resistance. (b) Power stage of buck converter by considering the parasitic resistance. (c) Energy delivery path during  $T_{ON}$ . (d) Energy delivery path during  $T_{OFF}$

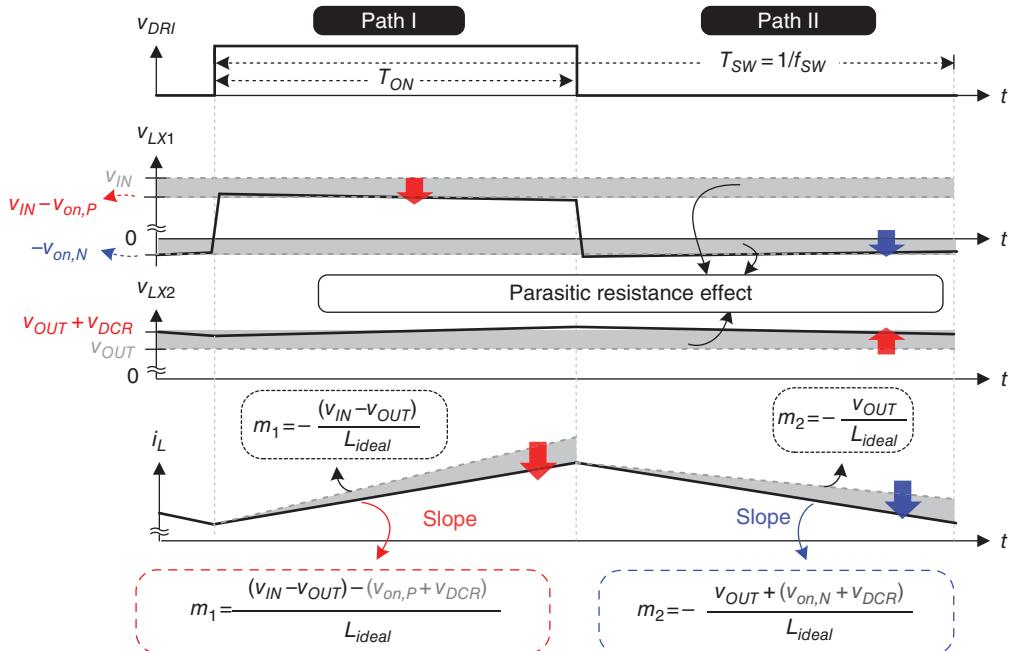
during  $T_{ON}$  and  $T_{OFF}$ , respectively. Parasitic resistances result in voltage drops,  $v_{on,P}$ ,  $v_{on,N}$ , and  $v_{DCR}$ . All voltage drops are dependent on  $i_{Load}$ , as shown:

$$\begin{cases} v_{on,P} = R_{on,P} \cdot i_{Load} \\ v_{on,N} = R_{on,N} \cdot i_{Load} \\ v_{DCR} = R_{DCR} \cdot i_{Load} \end{cases} \quad (5.48)$$

Figure 5.40 illustrates the frequency variation as a result of parasitic resistances.  $v_{on,P}$ ,  $v_{on,N}$ , and  $v_{DCR}$  lead the voltage variation across the inductor  $L$ . The waveform shows that the voltage of nodes  $v_{LX1}$  and  $v_{LX2}$  affects the cross voltage of  $L_{ideal}$ , and subsequently results in the gradual steep rising and falling of slopes with extra term  $-(v_{on,P} + v_{DCR})$  and  $v_{on,N} + v_{DCR}$ , respectively. In other words, the cross voltage of the inductor decreases and increases as  $i_L$  flows through paths I and II, respectively. The voltages of  $v_{LX1}$  and  $v_{LX2}$  with and without considering the parasitic resistance effect are listed in Table 5.2. Even if  $v_{IN}$  and  $v_{OUT}$  are not modified, the constant  $T_{ON}$  at different loading conditions results in frequency variation because different slopes of  $i_L$  occur at different loading conditions.

According to the voltage/second balance in steady state, Eqs. (5.49) and (5.50) are obtained by assuming that  $i_L$  rises and falls linearly during  $T_{ON}$  and  $T_{OFF}$ , respectively, where  $\Delta i_L$  is the peak-to-peak ripple current of  $i_L$ :

$$[(v_{IN} - v_{OUT}) - (v_{on,P} + v_{DCR})] = L_{ideal} \cdot \frac{\Delta i_L}{D_{actual} \cdot T_{SW}} \quad (5.49)$$



**Figure 5.40** Influence of parasitic resistances on  $v_{LX1}$ ,  $v_{LX2}$ , and  $i_L$  slope

**Table 5.2** Voltage across the inductor w/i and w/o considering parasitic resistances

	Ideal case: w/o parasitic resistance effect	Actual case: w/i parasitic resistance effect
	$v_{LX1}$	$v_{LX2}$
Path I	$v_{IN}$	$v_{OUT}$
Path II	$\sim$	$v_{IN} - v_{on,P}$

$$[v_{OUT} + (v_{on,N} + v_{DCR})] = L_{ideal} \cdot \frac{\Delta i_L}{(1 - D_{actual}) \cdot T_{SW}} \quad (5.50)$$

$D_{actual}$  in Eqs. (5.51) and (5.52) is derived from Eqs. (5.49) and (5.50), respectively, during  $T_{ON}$  and  $T_{OFF}$ :

$$D_{actual} = \frac{v_{OUT} + (R_{on,N} + R_{DCR}) \cdot i_{Load}}{v_{IN} - (R_{on,P} - R_{on,N}) \cdot i_{Load}} \quad (5.51)$$

$$D_{actual} = \frac{D_{ideal} + \frac{(R_{on,N} + R_{DCR}) \cdot i_{Load}}{v_{IN}}}{1 - \frac{(R_{on,P} - R_{on,N}) \cdot i_{Load}}{v_{IN}}} \quad (5.52)$$

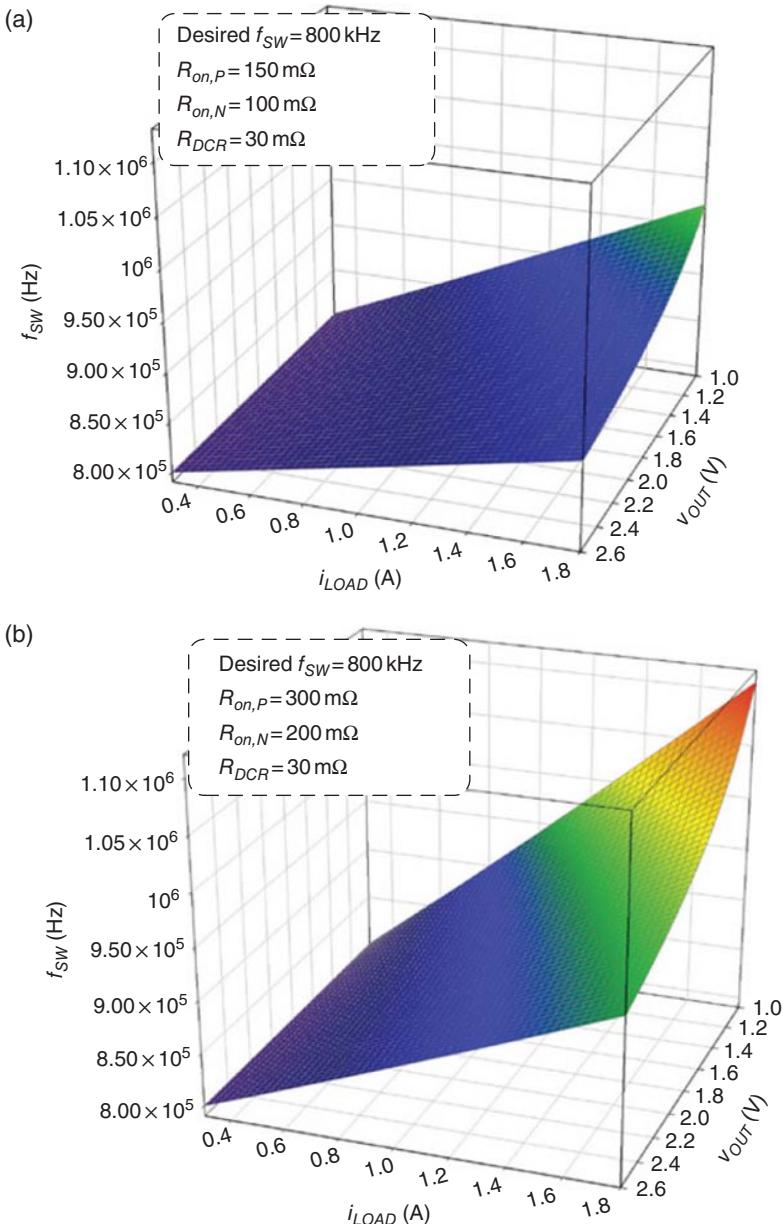
By substituting Eq. (5.52) into Eq. (5.41), the switching frequency is derived in Eq. (5.53). Compared with Eq. (5.44), Eq. (5.53) reveals that the switching frequency is dependent on several parasitic factors:

$$f_{SW} = \frac{D_{ideal} + \frac{(R_{on,N} + R_{DCR}) \cdot i_{Load}}{v_{IN}}}{1 - \frac{(R_{on,P} - R_{on,N}) \cdot i_{Load}}{v_{IN}}} \cdot \frac{1}{T_{ON(actual)}} \quad (5.53)$$

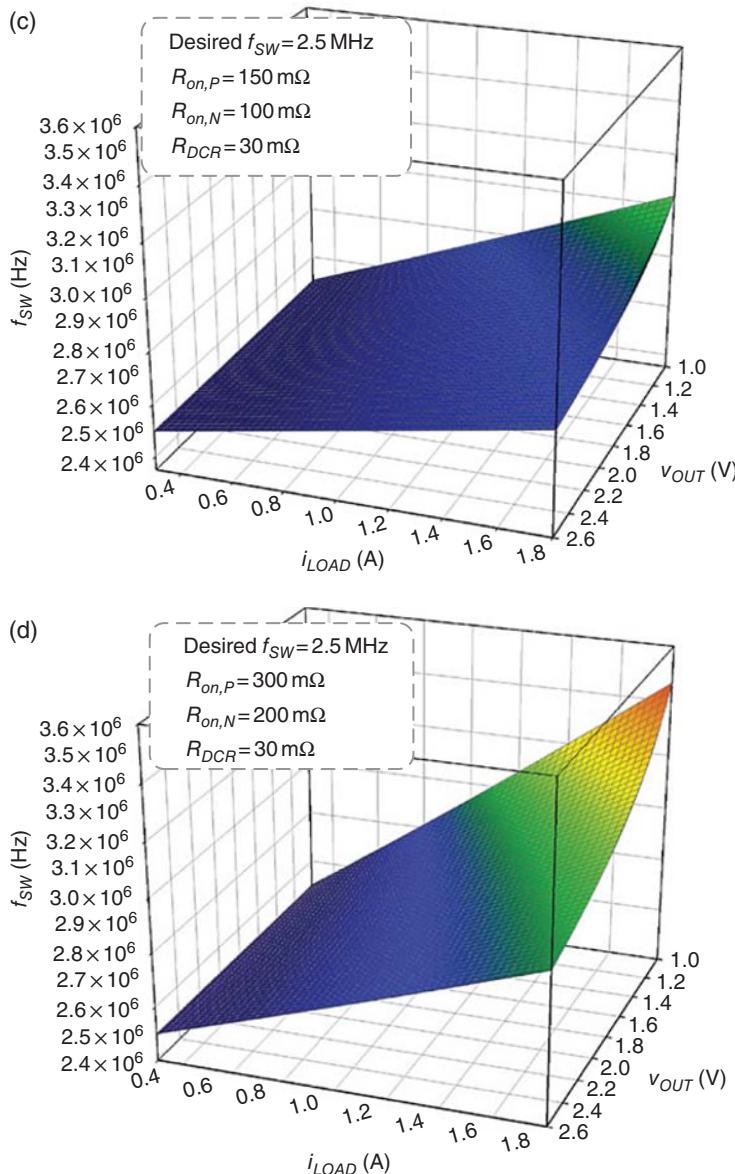
Figure 5.41 presents four cases to depict  $\Delta f_{SW}$  at different  $v_{OUT}$ ,  $v_{IN}$ , and  $i_{Load}$  according to Eq. (5.53). The desired  $f_{SW}$  is 800 kHz in cases (a) and (b), and the desired  $f_{SW}$  is 2.5 MHz in cases (c) and (d). In all these cases, the change in  $i_{Load}$  results in more significant  $\Delta f_{SW}$  when  $v_{OUT}$  is at low values. A comparison of cases (a) and (b) reveals that  $\Delta f_{SW}$  in case (b) is the worse because of the serious parasitic effect. Cases (c) and (d) also have similar results. Comparing the desired  $f_{SW}$  of 800 kHz with 2.5 MHz shows that the case with high desired  $f_{SW}$  has the worse  $\Delta f_{SW}$  at the load change from 0.3 to 1.7 A.

Figure 5.42 depicts  $\Delta f_{SW}$  with specific load changes versus the desired  $f_{SW}$  and  $v_{OUT}$ . This characteristic can also be obtained using Eqs. (5.52) and (5.53). Considering that  $v_{OUT}$ ,  $v_{IN}$ , and the parasitic resistances remain constant,  $\Delta D_{actual}$  with a certain load change remains constant. However, a high desired  $f_{SW}$  represents a short  $T_{ON(actual)}$ , and  $\Delta f_{SW}$  is amplified from  $D_{actual}$  by a large value of  $1/T_{ON(actual)}$ .

In conclusion,  $\Delta f_{SW}$  should not be neglected. A conventional  $T_{ON(ideal)}$  as in Eq. (5.43) cannot compensate for the variation in  $D_{actual}$  as in Eq. (5.52). Furthermore, Eq. (5.53) reveals that



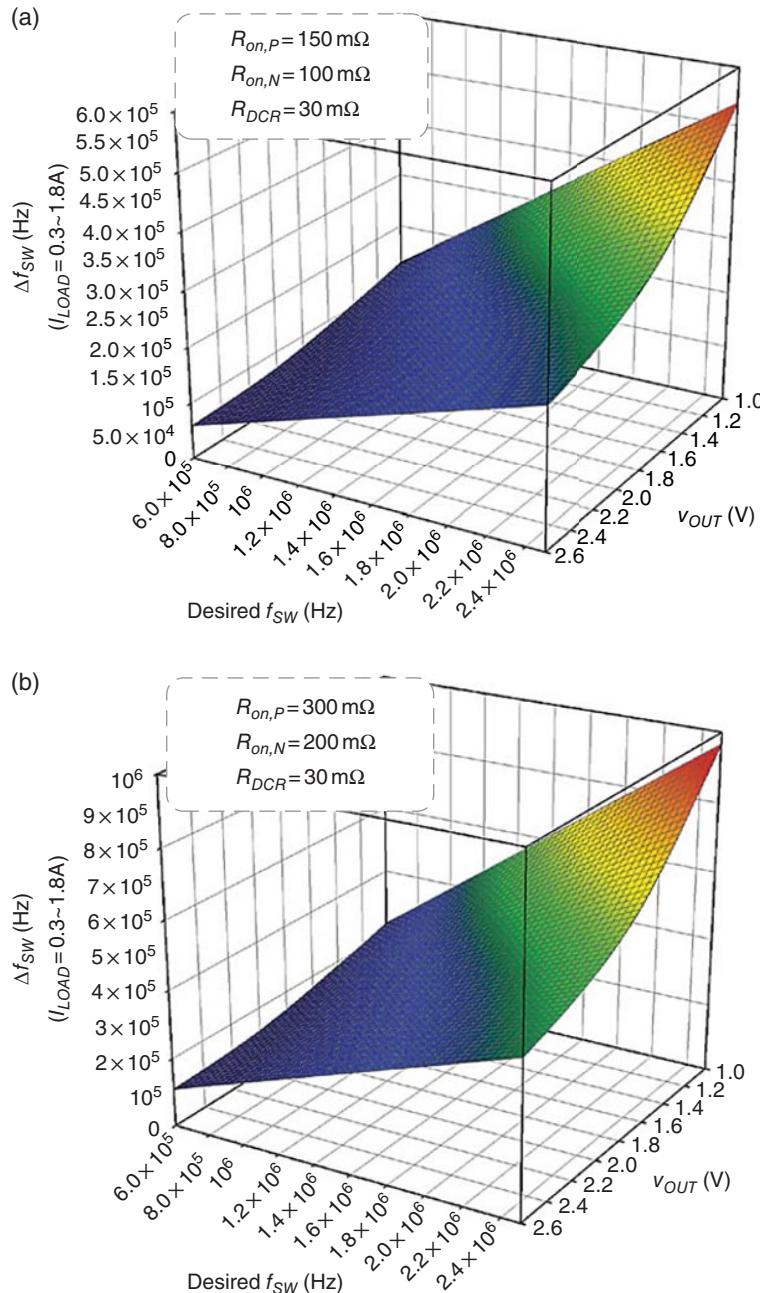
**Figure 5.41** Relationship among  $f_{SW}$ ,  $i_{Load}$ , and  $v_{OUT}$  when  $v_{IN} = 3.3 \text{ V}$ : (a) desired  $f_{SW} = 800 \text{ kHz}$ ,  $R_{on,p} = 150 \text{ m}\Omega$ ,  $R_{on,N} = 100 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$ ; (b) desired  $f_{SW} = 800 \text{ kHz}$ ,  $R_{on,p} = 300 \text{ m}\Omega$ ,  $R_{on,N} = 200 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$ ; (c) desired  $f_{SW} = 2.5 \text{ MHz}$ ,  $R_{on,p} = 150 \text{ m}\Omega$ ,  $R_{on,N} = 100 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$ ; (d) desired  $f_{SW} = 2.5 \text{ MHz}$ ,  $R_{on,p} = 300 \text{ m}\Omega$ ,  $R_{on,N} = 200 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$



**Figure 5.41** (Continued)

designing a proper  $T_{ON}$  to completely compensate for the parasitic effects is the challenge for on-time control to maintain a constant  $f_{SW}$ .

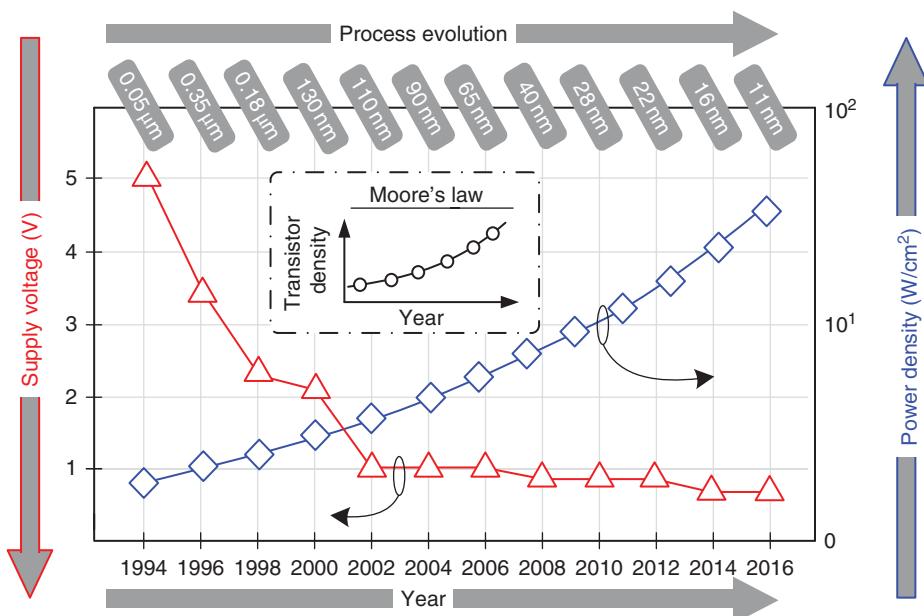
The designer should focus on reducing the frequency variation because the desired output voltage is not scaled down, and the switching does not increase significantly as in the past. However, the transistor density increases drastically for Soc applications because of the recent



**Figure 5.42** Variation of  $f_{SW}$  in load change from 0.3 to 1.8 A versus different desired  $f_{SW}$  and  $v_{OUT}$  when (a)  $R_{on,p} = 150 \text{ m}\Omega$ ,  $R_{on,N} = 100 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$  and (b)  $R_{on,p} = 300 \text{ m}\Omega$ ,  $R_{on,N} = 200 \text{ m}\Omega$ ,  $R_{DCR} = 30 \text{ m}\Omega$

advances in nanometer-scale processes. Meanwhile, the power density increases significantly, and the supply voltage is scaled down, as shown in Figure 5.43. The power density increases, although the supply voltage is scaled down from 5 V in 0.5  $\mu\text{m}$  to 0.85 V in 10 nm. The trend follows, and may even be beyond Moore's law. Consequently, power management systems or smart power converters, which feature high power and high performance, are urgently needed for today's consumer electronics. If the output voltage provided by power converters is scaled down below 1 V for circuits in the advanced process,  $f_{SW}$  will also increase to several megahertz for compact size and small output ripple. Predicting the variation of the switching frequency does not influence the Soc performance of some filters, and thus the reduction in switching frequency variation is expected.

Although Eq. (4.3) is a roughly derived result, understanding intuitively why the switching frequency varies in different  $v_{IN}$  and  $v_{OUT}$  is useful. However,  $D_{actual}$  is determined not only by  $v_{IN}$  and  $v_{OUT}$ , but also by  $i_{Load}$  and parasitic resistances, as shown in Eq. (5.51). Specifically, Eq. (5.51) manifests that the power MOSFET, inductor, and load range should be selected carefully and specified according to the tolerance of frequency variation. To release the frequency variation, a conventional  $T_{ON}$  as derived in Eq. (5.43) cannot compensate for  $D_{actual}$  in Eq. (5.51). Furthermore, this equation reveals the proper design of  $T_{ON}$  to compensate for completely parasitic facts, which is a challenge for on-time control with constant switching frequency. The following subsections will introduce useful techniques to maintain a constant switching frequency by considering the cases under different  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$ .



**Figure 5.43** Trends of supply voltage and power density with the evolution of process technology

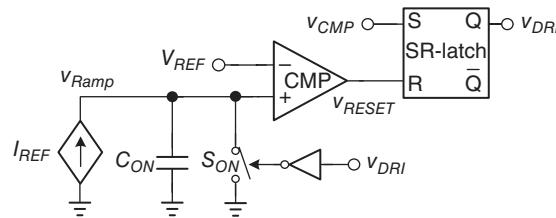
### 5.2.5 Adaptive On-Time Controller for Pseudo-Constant $f_{SW}$

#### 5.2.5.1 Fixed On-Time Controller (Fixed $T_{ON}$ )

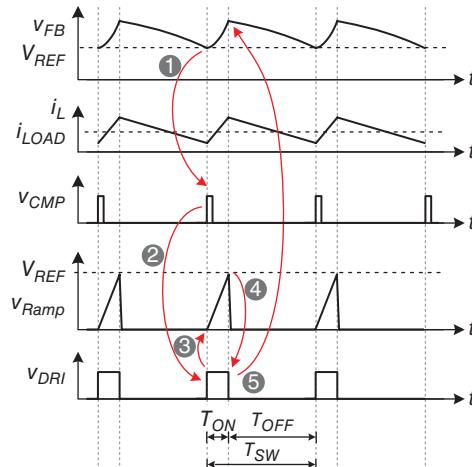
Figure 5.44 shows the fundamental structure of the basic fixed on-time controller to realize the fixed pulse of one on-time period. The current  $I_{REF}$  charges  $C_{ON}$  to increase  $v_{Ramp}$  from zero to  $V_{REF}$ .  $T_{ON}$  can be derived as in Eq. (5.44), with its characteristics proportional to  $V_{REF}$  and inversely proportional to  $I_{REF}$ .  $T_{ON}$  can be adjusted by different  $C_{ON}$ ,  $I_{REF}$ , and  $V_{REF}$ :

$$T_{ON} = \frac{C_{ON}}{I_{REF}} \cdot V_{REF} \quad (5.54)$$

Figure 5.45 illustrates the operating waveforms. The switching period  $T_{SW}$  is defined as a period that starts when  $v_{FB}$  falls below  $V_{REF}$  and terminates when the next switching starts again. At the beginning of  $T_{SW}$ , the on-time phase is triggered when  $v_{FB}$  falls below  $V_{REF}$ .  $v_{DRI}$  is set high from low. In the initial condition of the on-time pulse,  $v_{Ramp}$  is reset to zero by the switch  $S_{ON}$  controlled by the signal  $v_{DRI}$ . Thereafter, the current source starts to charge  $C_{ON}$



**Figure 5.44** Model of the basic constant on-time controller



**Figure 5.45** Waveforms to illustrate the operation of the on-time controller

with an increasing signal  $v_{Ramp}$  during the  $T_{ON}$  period. Third, when  $v_{Ramp}$  reaches the upper threshold,  $V_{REF}$ , the comparator output,  $v_{DRI}$ , is set from high to low and the  $T_{ON}$  period is terminated. Meanwhile,  $v_{Ramp}$  is reset to zero by  $v_{DRI}$  and prepared to trigger in the next period.

In this design, the switching frequency varies with different  $v_{IN}$  and  $v_{OUT}$ . The following topics examine the analyses and different methods to pursue the constant switching frequency independent of operating conditions, such as  $v_{IN}$ ,  $v_{OUT}$ ,  $i_{Load}$ , and the characteristics of components in the power stage.

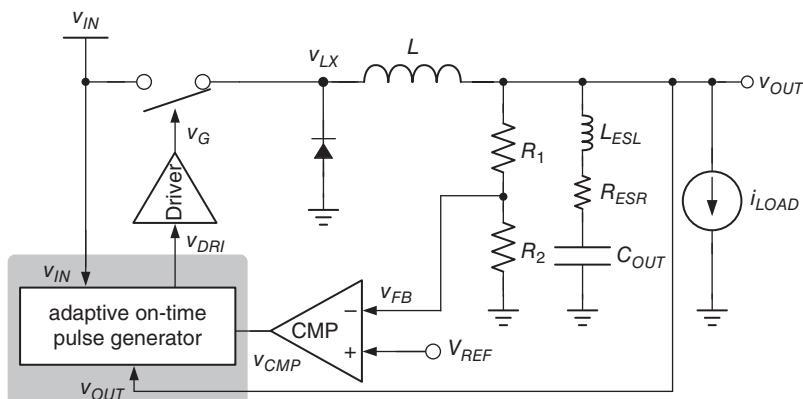
### 5.2.5.2 Adaptive On-Time Controller Utilizing Information on $v_{IN}$ and $v_{OUT}$

In Eq. (4.3), the switching frequency is determined by three factors,  $T_{ON}$ ,  $v_{IN}$ , and  $v_{OUT}$ . A constant  $T_{ON}$  implies that the switching frequency varies at different  $v_{IN}$  and  $v_{OUT}$ . For example, this situation may occur if  $v_{IN}$  is provided by a battery in portable applications. When the electronic device continues to operate and the power from the battery is consumed for some time, the voltage level of the battery continuously decreases, and then  $v_{IN}$  decreases. This situation shows an approach to eliminate the switching frequency variation. The value of  $T_{ON}$  is adjusted according to the input voltage  $v_{IN}$  and the output voltage  $v_{OUT}$  in the adaptive on-time pulse generator. According to Eq. (4.3),  $T_{ON}$  is inversely proportional to  $v_{IN}$  while it is proportional to  $v_{OUT}$ , as expressed in Eq. (5.55) (Figure 5.46):

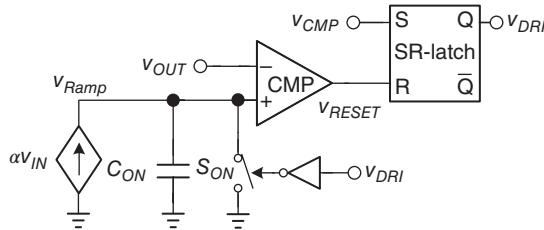
$$T_{ON} \propto \frac{v_{OUT}}{v_{IN}} \quad (5.55)$$

As a result, Eq. (5.56) shows that a pseudo-constant switching frequency can be achieved, such that the switching frequency is not affected by the variations of  $v_{IN}$  and  $v_{OUT}$ :

$$f_{SW(new)} \propto \frac{v_{OUT}}{v_{IN} \cdot \left( \frac{v_{OUT}}{v_{IN}} \right)} = \text{constant} \quad (5.56)$$



**Figure 5.46** The adaptive on-time is adjusted by  $v_{IN}$  and  $v_{OUT}$



**Figure 5.47** Model of the basic adaptive on-time control to obtain a pseudo-constant switching frequency

Figure 5.47 shows the basic structure of the adaptive on-time pulse generator to realize the pseudo-constant switching frequency in Eq. (5.55). The charging current source, which is equal to  $\alpha \cdot v_{IN}$ , is used to charge the capacitor  $C_{ON}$ , where  $\alpha$  is a constant value.

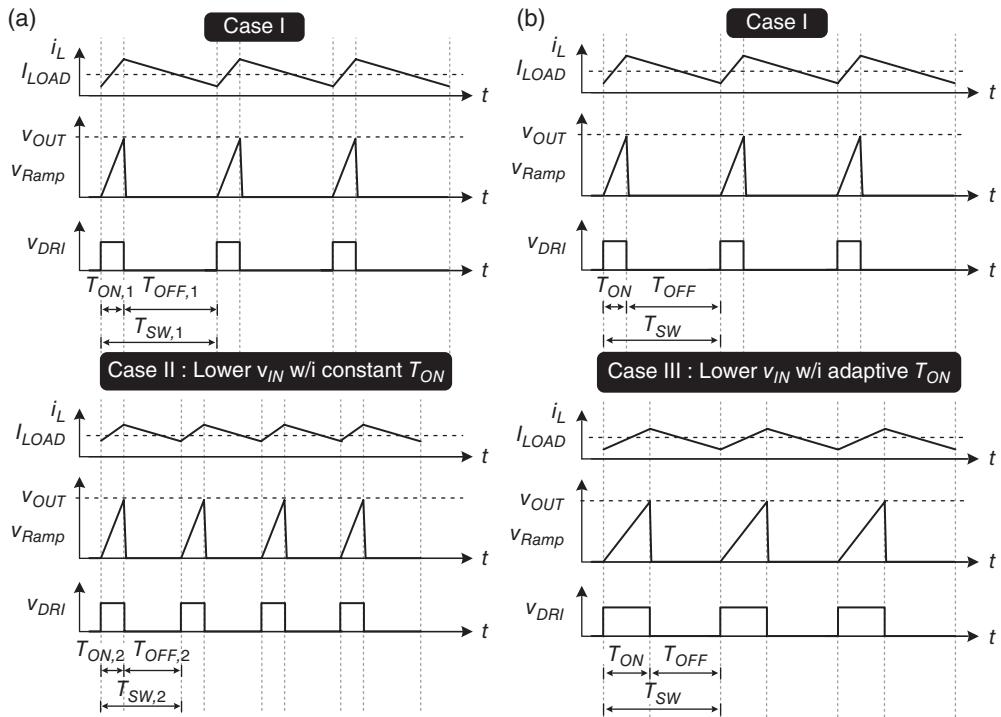
Assuming that  $v_{Ramp}$  ramps up linearly, the increase or decrease in  $v_{OUT}$  results in the charging time as  $v_{Ramp}$  increases or decreases because the upper threshold voltage is  $v_{OUT}$ . By contrast, a different  $v_{IN}$  results in different charging currents of  $C_{ON}$  and in different rising speeds at  $v_{Ramp}$ . In other words, increasing/decreasing  $v_{IN}$  causes a faster or slower rising speed at  $v_{Ramp}$ , and then changes the charging time as  $v_{Ramp}$  decreases or increases. Consequently,  $T_{ON}$  is derived as Eq. (5.57) with its characteristics proportional to  $v_{OUT}$  and inversely proportional to  $v_{IN}$ :

$$T_{ON} = \frac{C_{ON}}{\alpha} \cdot \frac{v_{OUT}}{v_{IN}} \quad (5.57)$$

The basic adaptive on-time control can maintain a pseudo-constant switching frequency  $f_{SW}$  by adjusting the on-time value corresponding to the varying  $v_{IN}$  and  $v_{OUT}$ .

Figure 5.48(a), (b) describes the different cases by comparing between constant and adaptive on-time. If we use case I as reference, when  $v_{IN}$  decreases, we observe different results in case II with constant on-time and case III with adaptive on-time. The duty cycle changes because the decrease in  $v_{IN}$  eases the decreasing slope of  $i_L$ . If  $T_{ON}$  remains constant, as shown in case II, then  $T_{OFF}$  will shrink accordingly and cause a short switching period  $T_{SW}$ . In other words, at heavy loads,  $f_{SW}$  can increase because of the constant  $T_{ON}$ . The  $f_{SW}$  variation is summarized in Table 5.3. By contrast, the on-time value can adjust dynamically according to  $v_{IN}$  and  $v_{OUT}$ , such that  $f_{SW}$  remains constant at different  $v_{IN}$  and  $v_{OUT}$  conditions. Case III shows that  $f_{SW}$  remains constant because of the dynamic  $T_{ON}$  when  $v_{IN}$  decreases. As shown in Figure 5.47, decreasing  $v_{OUT}$  creates a short time for  $v_{Ramp}$  to rise to the upper threshold,  $v_{OUT}$ , such that  $T_{ON}$  extends. Consequently, the desired  $T_{ON}$  for constant  $T_{SW}$  under different  $v_{IN}$  and  $v_{OUT}$  is summarized in Table 5.3.

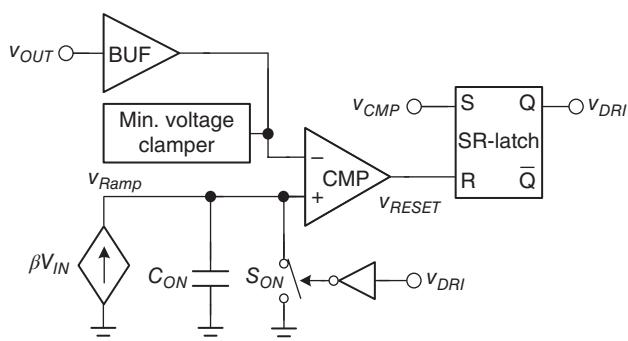
In this work, the start-up operation should be considered carefully. When the converter is triggered from the shut-down situation, the initial value of  $v_{OUT}$  is zero. This zero value makes the on-time pulse extremely short, because  $v_{Ramp}$  rises quickly to  $v_{OUT}$  whenever  $C_{ON}$  is charged. As a result,  $C_{OUT}$  in the output stage is difficult to charge because the on-time period is extremely short, although  $v_{CMP}$  remains high to represent the need for energy replenishment. For this reason, the complete circuit design, as shown in Figure 5.49, will utilize the minimum



**Figure 5.48** Characteristics of frequency change under different  $v_{IN}$  in comparison with (a) constant  $T_{ON}$  and (b) adaptive  $T_{ON}$

**Table 5.3** Characteristics of the summarized variation in on-time control

Condition	Duty variation ( $\Delta D$ )	Switching frequency variation ( $\Delta f_{SW}$ ) with constant $T_{ON}$	Desired $T_{ON}$ for constant $f_{SW}$
$v_{IN} \downarrow$	$\uparrow$	$\downarrow$	$\uparrow$
$v_{IN} \uparrow$	$\downarrow$	$\uparrow$	$\downarrow$
$v_{OUT} \downarrow$	$\downarrow$	$\uparrow$	$\downarrow$
$v_{OUT} \uparrow$	$\uparrow$	$\downarrow$	$\uparrow$



**Figure 5.49** Model of the basic adaptive on-time control with buffer and minimum voltage clamp

voltage clamper to control the minimum voltage of the minus input of CMP, and thus ensure that the minimum on-time value during start-up is adequate. Moreover,  $v_{OUT}$  will be fed into CMP through a buffer (BUF) because  $v_{OUT}$  contains switching noise.

In contrast, it's also an important design issue to discuss how to implement the charging current circuit, which is proportional to  $v_{IN}$ . The following examples give the reader the circuit implementation for reference.

### 5.2.5.3 Circuit Implementation (1)

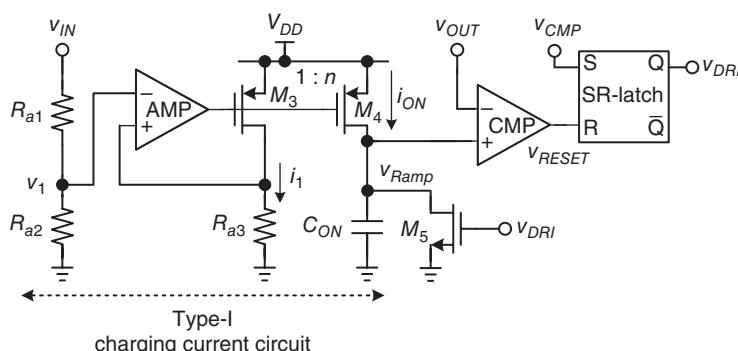
Figure 5.50 shows the circuit implementation of the Type-I charging current circuit for the model in Figure 5.47. Considering that the value of  $v_{IN}$  may be higher than the normal voltage of core devices in the process,  $v_{IN}$  is often fed first into voltage dividers to scale down its value. The voltage divider is composed of  $R_{ON}$  and  $R_{a1}$ .  $v_1$  is proportional to  $v_{IN}$ :

$$v_1 = v_{IN} \cdot \frac{R_{a2}}{R_{a1} + R_{a2}} \quad (5.58)$$

The amplifier with negative feedback then converts  $i_1$  from  $v_1$  and  $R_{a3}$ . Given the current mirror ratio of  $n$  between  $M_3$  and  $M_4$ ,  $i_{ON}$  can be derived as in Eq. (5.59). In other words, the charging current  $i_{ON}$  is proportional to  $v_{IN}$ :

$$i_{ON} = n \cdot \frac{v_1}{R_{a3}} = v_{IN} \cdot \left( n \cdot \frac{R_{a2}}{(R_{a1} + R_{a2}) \cdot R_3} \right) \quad (5.59)$$

To adjust the on-time period for the user, the designer can set  $R_{a1}$ ,  $R_{a2}$ , or  $R_{a3}$  as a discrete component for replacement with a specific value. The weakness of this circuit is that the voltage divider has a trade-off between silicon area and quiescent current. The amplifier with negative feedback also consumes extra silicon area for adequate compensation. Additionally, the operating range of  $v_{IN}$  is limited by the consideration of the input common-mode range of the amplifier.



**Figure 5.50** Implementation of Type-I charging current circuit

### 5.2.5.4 Circuit Implementation (2)

Figure 5.51 shows the implementation of the Type-II charging current circuit. This circuit uses a self-bias current structure composed of  $R_{ON}$  and  $M_1$  to generate  $i_1$ . The current is mirrored by ratios  $n$  and  $m$ , and then generates  $i_{ON}$  as expressed in Eq. (5.60). The factor  $v_{GS}$  deteriorates the linearity between  $i_{ON}$  and  $v_{IN}$ :

$$i_{ON} = mn \cdot \frac{v_{IN} - v_{GS}}{R_{ON}} \quad (5.60)$$

However, when  $v_{IN}$  is much higher than  $v_{GS}$ ,  $v_{GS}$  can be neglected and Eq. (5.60) can be simplified as:

$$i_{ON} \approx m \cdot n \cdot \frac{v_{IN}}{R_{ON}} \quad (\text{when } v_{IN} \gg v_{GS}) \quad (5.61)$$

In this design,  $R_{ON}$  can be set as a discrete component and replaced by an adequate value for the desired on-time period. The value of  $R_{ON}$  sacrifices no cost of the silicon area, such that the quiescent current is easily reduced and power loss is saved.

### 5.2.5.5 Adaptive On-Time Controller with Information on $v_{LX}$ and $v_{OUT}$

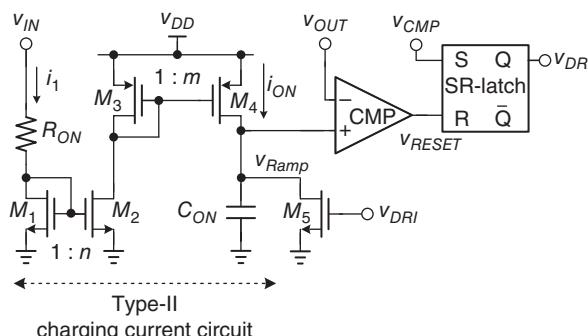
Figure 5.52 shows the structure of the adaptive on-time pulse generator to alleviate the switching frequency variation caused by different loading conditions, as derived in Eq. (5.13).

Compared with the previous structure depicted in Figure 5.47, the voltage-controlled current source in Figure 5.52 depends on  $v_{LX}$ , which is the node connected to the high-side switch and the inductor. Through the on-resistance of the high-side switch,  $v_{LX}$ , as expressed in Eq. (5.62), changes with different loading conditions  $i_{Load}$  during the on-time period:

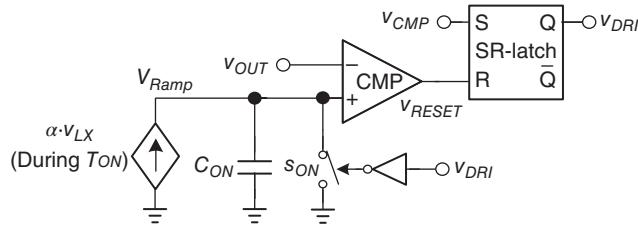
$$v_{LX} = v_{IN} - i_L(t) \cdot R_{ON} \quad (5.62)$$

To simplify the analysis,  $i_L(t)$  is replaced by the average inductor current, which is equal to  $I_{Load}$ :

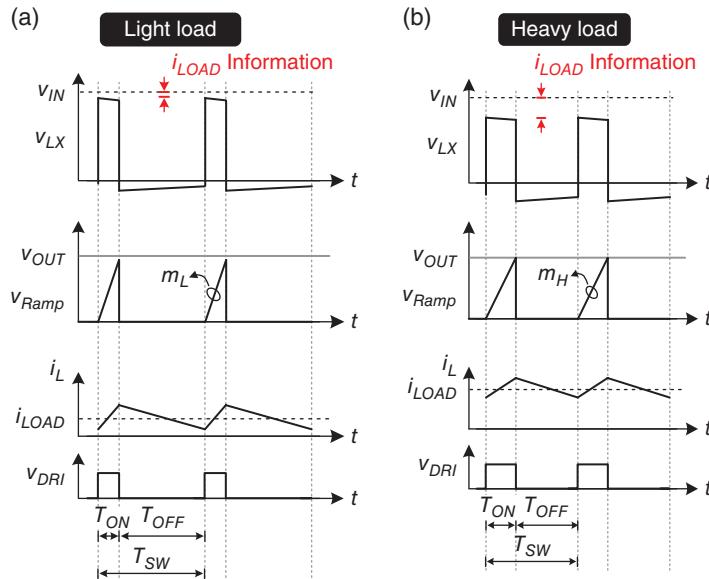
$$v_{LX} = v_{IN} - I_{Load} \cdot R_{ON} \quad (5.63)$$



**Figure 5.51** Implementation of Type-II charging current circuit



**Figure 5.52** Structure of adaptive on-time controller with the addition of  $v_{LX}$  information



**Figure 5.53** Waveforms illustrate the load current affecting the  $v_{Ramp}$  slope value (a) at light loads and (b) at heavy loads

Then,  $T_{ON}$  is derived in Eq. (5.64) and adjusted by  $v_{OUT}$ ,  $v_{IN}$ , and  $I_{Load}$ :

$$T_{ON} = \frac{C_{ON}}{\alpha} \cdot \frac{v_{OUT}}{v_{IN} - I_{Load} \cdot R_{ON}} \quad (5.64)$$

As a result, if  $I_{Load}$  increases, then the  $T_{ON}$  period will increase according to the change in  $I_{Load}$ , such that the loading effect on duty can be eliminated. According to Eq. (5.13), although the factor of  $I_{Load}$  cannot be calibrated completely, the switching frequency variation can be more or less alleviated.

Figure 5.53 illustrates the operating waveforms for the adaptive on-time controller with the addition of  $v_{LX}$  information. As expressed in Eq. (5.62),  $I_{Load}$  information can be included via

$v_{LX}$  as the derived equation in Eq. (5.63). Compared with different loading conditions, the voltage level of  $v_{LX}$  during the on-time period is lower at heavy loads, and then produces  $v_{Ramp}$  with a smaller slope, or  $m_H < m_L$ . As a result,  $v_{Ramp}$  spends a long time to ramp up to  $v_{OUT}$ , such that  $T_{ON}$  can be extended slightly at heavy loads. This approach is the simplest to apply to compensate for the frequency variation in  $I_{Load}$ .

### 5.2.5.6 Circuit Implementation (3)

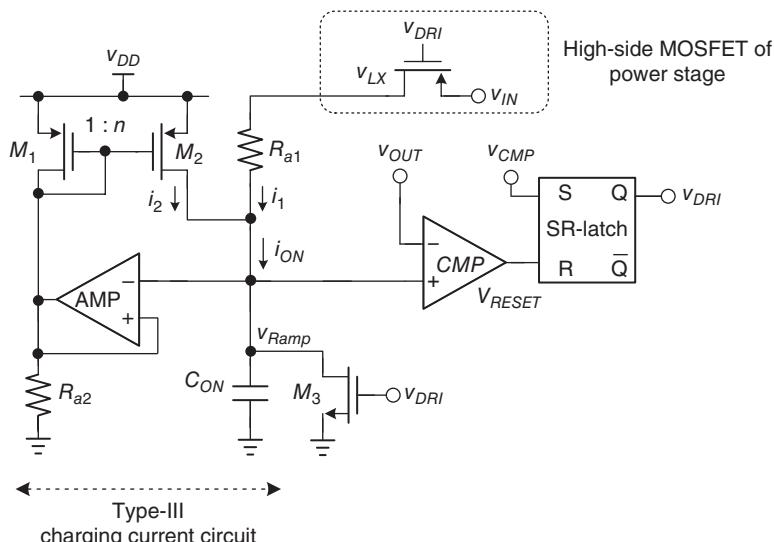
Figure 5.54 shows an adaptive on-time controller. The charging current  $i_{ON}$  includes both  $i_1$  and  $i_2$ , as expressed in Eq. (5.65). When the value of  $R_{a1}$  is equal to the value of  $R_{a2}/n$ , the second factor is eliminated, such that  $i_{ON}$  is completely proportional to  $v_{IN}$ :

$$I_{ON} = i_1 + i_2 = \left( \frac{v_{LX} - v_{Ramp}}{R_{q1}} \right) + \left( n \cdot \frac{v_{Ramp}}{R_{q2}} \right) = \frac{v_{LX}}{R_{q1}} + v_{Ramp} \cdot \left( -\frac{1}{R_{q1}} + \frac{n}{R_{q2}} \right) \quad (5.65)$$

As a result, the charging current  $i_{ON}$  flows into  $C_{ON}$ , and the on-time period is determined as expressed in Eq. (5.66), which is similar to Eq. (5.64):

$$T_{ON} = \frac{C_{ON}}{i_1 + i_2} \cdot v_{OUT} = C_{ON} \cdot R_{a1} \cdot \frac{v_{OUT}}{v_{LX}} \quad (5.66)$$

The value of  $R_{a1}$  equal to the value of  $R_{a2}/n$  can be achieved by good layout matching skills on the same chip without the influence of process variation. However, the on-time period is difficult to adjust to the desired switching frequency. Although  $R_{a1}$  and  $R_{a2}$  can be designed as discrete components, additional components require high costs and PCB area.



**Figure 5.54** Adaptive on-time controller to obtain a reliable switching frequency without the influence of the variation in input voltage  $v_{IN}$

According to Eq. (1.3),  $f_{SW}$  remains constant regardless of the variation from  $v_{OUT}$  and  $v_{IN}$  and  $i_{Load}$ . Compared with prior studies that utilize  $v_{IN}$  instead of  $v_{LX}$ , this work provides an accurate and linear solution to correctly minimize the variation of the switching frequency. Therefore, the approach can work as a PWM operation with constant switching frequency, although the internal clock is absent. Furthermore, by directly comparing the connection of  $R_{ON}$  to the nodes  $v_{IN}$  and  $v_{LX}$  in the previous design, which causes  $i_{ON}$  to flow continuously, a switch can be used to cut the current flowing path to prevent more power loss during the off-time period. However, this switch should be a high-voltage device if  $v_{IN}$  is higher than the normal voltage of core devices. In other words, the silicon area cost is higher. By contrast, when  $R_{ON}$  is connected to  $v_{LX}$ , the high-side switch can be utilized to generate  $i_{ON}$  only at the on-time period.  $v_{Ramp}$  is always lower than  $v_{OUT}$ . The advantages of this design include avoiding high-voltage damage caused by  $v_{IN}$  and wasteful power consumption. Moreover, the number of high-voltage devices can be reduced to minimize the cost.

### 5.3 Optimum On-Time Controller for Pseudo-Constant $f_{SW}$

$v_{IN}$ ,  $v_{OUT}$ , and the load current  $i_{Load}$  will influence the value of  $f_{SW}$ . Generally,  $f_{SW}$  increases if  $i_{Load}$  increases. For EMI consideration, the suppression of the frequency variation caused by  $i_{Load}$  is also expected. This section introduces the detailed analysis and importance of  $f_{SW}$ .

The previous literature proposed several techniques to alleviate variation because of the clock-free architecture RBOTC. An extra external clock or PLL is utilized at the expense of circuit complexity, silicon area, and cost [11, 12, 23–26]. By contrast, the techniques use  $v_{IN}$  and  $v_{OUT}$  information to generate adaptive on-time and maintain constant  $f_{SW}$  at different  $v_{IN}$  and  $v_{OUT}$  [7, 17, 29]. However, the performance remains constrained, and these works cannot ensure constant  $f_{SW}$  at different loading conditions because practical parasitic resistances are not considered. Although the load current information is applied by replacing  $v_{IN}$  with  $v_{LX}$ , the improvement in  $\Delta f_{SW}$  is not effective [7]. A previous technique also applies load information to revise the on-time period, but the compensation values are not analyzed. Deciding on the amount of compensation accurately is difficult [17] because once overcompensation occurs,  $\Delta f_{SW}$  deteriorates. Furthermore, deriving the quantitative  $\Delta f_{SW}$  analysis, the information of  $v_{OUT}$ ,  $v_{IN}$ , and  $i_{Load}$  is insufficient because the assumption conditions are not suitable [17].

The literature in [29] utilized the RC network to sense  $i_L$  and adjust the adaptive on-time for pseudo-constant  $f_{SW}$ . However, the assumption of equal on-resistance value at both high- and low-side power MOSFETs is necessary but it is suitable because maintaining this assumption is difficult. Many resistors and the DCR of the inductor should also be matched exactly, which increases the design difficulty.

The reduction in  $\Delta f_{SW}$  needs to suitably control the on-time; alleviating  $\Delta f_{SW}$  also reduces EMI problems. Consequently, the quantitative analysis is complete and provides the predicting correction technique (PCT) to modulate an adaptive on-time for constant  $f_{SW}$  under different conditions, including  $v_{IN}$ ,  $v_{OUT}$ , and wide-range  $i_{Load}$ . The complete parasitic resistances of each component are considered without any assumption or simplification. Only the driving signal of the high-side power MOSFET ( $v_{GP}$ ) is necessary to achieve constant  $f_{SW}$  in the on-time circuit. This technique significantly reduces the complexity compared with those in previous works, which require additional  $v_{IN}$ ,  $v_{OUT}$ ,  $v_{LX}$ , current-sensing circuit, and parasitic resistance of components of the power stage.

### 5.3.1 Algorithm for Optimum On-Time Control

To completely compensate for  $\Delta f_{SW}$  using this approach, Eq. (5.67) is derived by rearranging Eqs. (5.49) and (5.50):

$$\begin{aligned} v_{IN} D_{actual} &= v_{OUT} + D_{actual} \cdot (R_{on,P} \cdot i_{Load}) \\ &\quad + (1 - D_{actual}) \cdot (R_{on,N} \cdot i_{Load}) + R_{DCR} \cdot i_{Load} \end{aligned} \quad (5.67)$$

An equivalent output voltage ( $v_{OUT,eq}$ ) is defined by  $v_{OUT}$  and  $\Delta v_{par}$ , as expressed in Eq. (5.68), in which  $\Delta v_{par}$  in Eq. (5.69) represents the voltage variation when the parasitic effects are considered:

$$v_{OUT,eq} = v_{OUT} + \Delta v_{par} \quad (5.68)$$

$$\Delta v_{par} = R_{par} \cdot i_{Load} \quad (5.69)$$

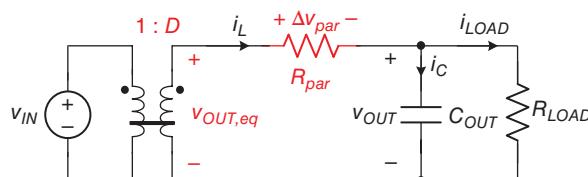
The parasitic effects are a series of parasitic equivalent resistances ( $R_{par}$ ), as expressed in Eq. (5.70):

$$R_{par} = D_{actual} \cdot R_{on,P} + (1 - D_{actual}) \cdot R_{on,N} + R_{DCR} \quad (5.70)$$

$v_{OUT,eq}$  is then expressed by  $D_{actual}$  in Eq. (5.71):

$$v_{OUT,eq} = D_{actual} \cdot v_{IN} \quad (5.71)$$

Figure 5.55 illustrates the average model for the power stage of the buck converter. All parasitic resistances are considered, and these parasitic effects are revealed by the equivalent ratio of the ideal transformer and the series of parasitic equivalent resistances  $R_{par}$  in Eq. (5.70). Instead of using  $v_{OUT}$  in the conventional design,  $v_{OUT,eq}$  can be synthesized by the optimum on-time. This work utilizes  $v_{IN}$  and  $v_{OUT,eq}$  to generate the optimum  $T_{ON}$  according to Eqs. (5.41) and (5.71). The solution to effectively alleviate  $\Delta f_{SW}$  can be realized at different  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$  conditions.



**Figure 5.55** Average model for the power stage of the buck converter when all parasitic resistances are considered

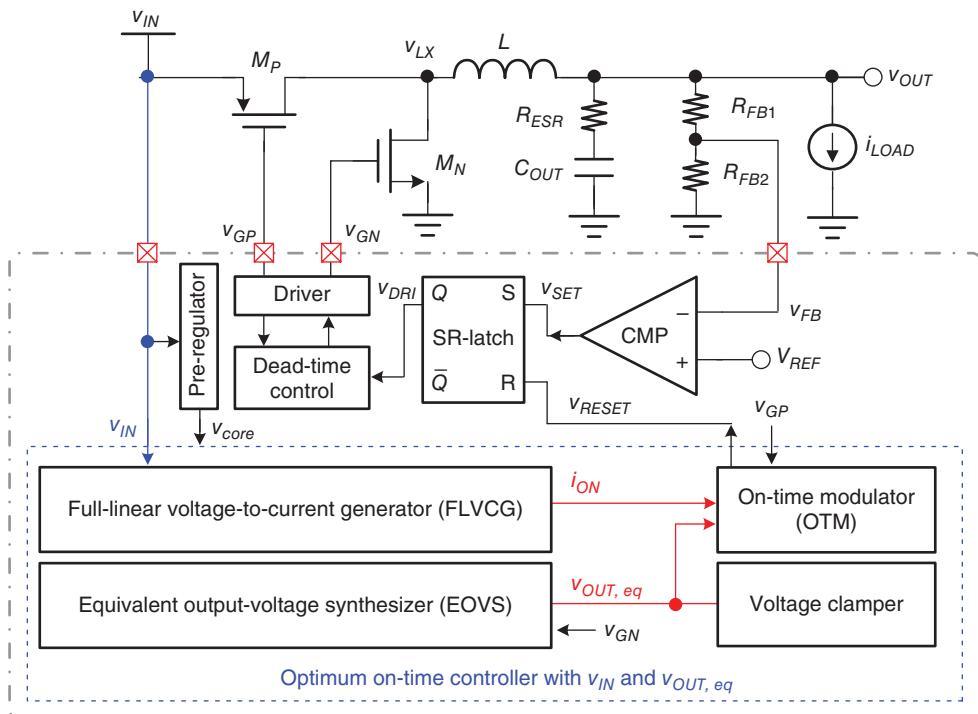
### 5.3.2 Type-I Optimum On-Time Controller with Equivalent $V_{IN}$ and $V_{OUT,eq}$

#### 5.3.2.1 Architecture and Operation of Converter

The optimum on-time controller is implemented in the DC/DC buck converter as shown in Figure 5.56. This optimum on-time controller can achieve a thorough solution to predict an adequate  $T_{ON}$  and obtain a nearly constant  $T_{SW}$ . The calibration includes all the changes in  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$ . The optimum on-time controller technique includes the fully linear voltage-to-current generator (FLVCG), equivalent output-voltage synthesizer (EOVS), on-time modulator (OTM), and voltage clamer.

The FLVCG circuit converts  $v_{IN}$  into the current  $i_{ON}$  and obtains a linear relationship with  $v_{IN}$ . The EOVS circuit modulates  $v_{OUT,eq}$  by  $v_{IN}$  and the driving signal  $v_{GP}$ . The OTM circuit outputs  $v_{RESET}$  to determine  $T_{ON}$  by  $i_{ON}$  and  $v_{OUT,eq}$ . According to Eq. (5.41),  $T_{ON}$  is designed as the value proportional to  $D_{actual}$ . Although numerous factors determine  $D_{actual}$  in Eq. (5.51), the PCT circuit uses  $v_{IN}$  and  $v_{GP}$  to generate an optimum  $T_{ON}$ , and thus compensate for  $D_{actual}$  without using any extra complex current-sensing circuits. Obtaining the on-resistance information of the power MOSFET and  $R_{DCR}$  of the inductor is also unnecessary.

Based on Eqs. (5.41) and (5.45), the optimum  $T_{ON}$  must be the value proportional to  $D_{actual}$ . Although various factors determine  $D_{actual}$  in Eq. (5.51), the optimum on-time controller can only use  $v_{IN}$  and  $v_{GP}$  to generate the optimum  $T_{ON}$  and compensate for  $D_{actual}$  to achieve the



**Figure 5.56** Architecture of the optimum on-time controlled buck converter using  $v_{IN}$  and  $v_{OUT,eq}$

pseudo-constant  $f_{SW}$ . In other words,  $v_{OUT}$  and  $v_{LX}$  are unnecessary for  $v_{IN}$  and  $v_{GP}$ . According to Eq. (5.71), FLVCG converts  $v_{IN}$  into the current ( $i_{ON}$ ), which is linear to  $v_{IN}$ . EOVS modulates  $v_{OUT,eq}$  by  $v_{IN}$  and the driving signal  $v_{GP}$ . Then, OTM determines  $T_{ON}$  by  $i_{ON}$  and  $v_{OUT,eq}$ .

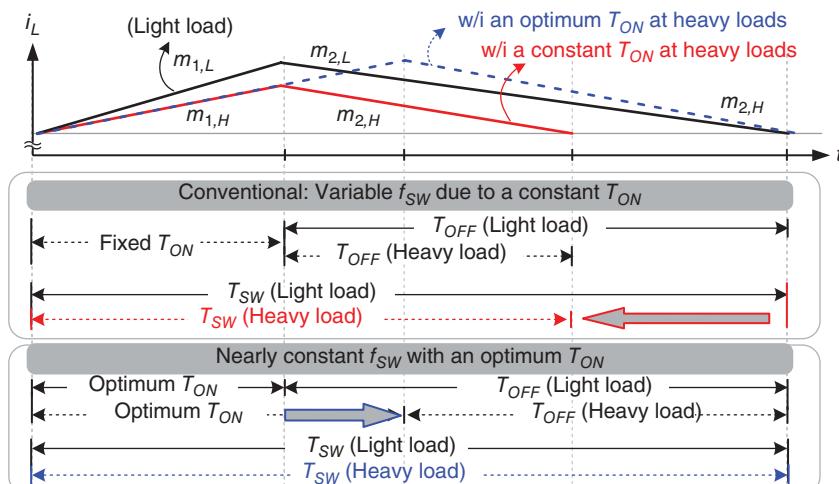
When  $v_{OUT,eq}$  is directly realized by Eqs. (5.68) and (5.69), the complex current-sensing circuit is required because  $v_{OUT,eq}$  includes many parasitic on-resistances. To reduce the complexity,  $v_{OUT,eq}$  is synthesized by  $v_{IN}$  and  $v_{GP}$  according to Eq. (5.71). Consequently,  $T_{ON}$  is expressed as in Eq. (5.72) to achieve a pseudo-constant  $f_{SW}$ :

$$T_{ON} = \frac{v_{OUT\_eq}}{v_{IN}} \cdot T_{SW} = \frac{(D_{actual} \cdot v_{IN})}{v_{IN}} \cdot T_{SW} = \frac{D_{actual}}{f_{SW}} \quad (5.72)$$

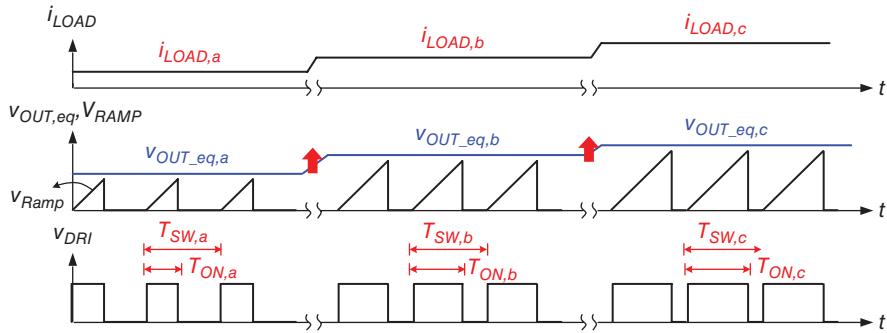
Compared with the constant  $T_{ON}$  and the optimum  $T_{ON}$ , Figure 5.57 explains that the variable  $D_{actual}$  at different loading conditions has some effects on  $\Delta f_{SW}$ . Slopes  $m_{1,L}$  and  $m_{2,L}$  rise and fall at light loads, respectively. Slopes  $m_{1,H}$  and  $m_{2,H}$  rise and fall at heavy loads, respectively. Increasing  $i_{Load}$  results in a smaller  $m_{1,H}$  than  $m_{1,L}$  and a larger  $m_{2,H}$  than  $m_{2,L}$ . As a result,  $T_{ON}$  is required to increase adequately at heavy loading conditions to maintain a constant  $f_{SW}$  at heavier loading conditions because of the expanding duty ratio, and vice versa.

The optimum on-time controller provides an adaptive  $T_{ON}$ , which is proportional to  $D_{actual}$  to compensate for the change in  $D_{actual}$  obtaining a nearly constant  $f_{SW}$ , as shown in Eq. (5.45). Without any complex sensing circuits, the optimum on-time controller generates  $v_{OUT,eq}$  as an equivalent  $v_{OUT}$  proportional to  $D_{actual}$  and  $v_{IN}$ . By contrast,  $v_{Ramp}$  is a rising voltage with a slope value proportional to  $v_{IN}$ .  $T_{ON}$  is also determined by the period when  $v_{Ramp}$  starts to rise until its value is equal to  $v_{OUT,eq}$ . Consequently,  $T_{ON}$  can be expressed as in Eq. (5.73), in which the on-time capacitor  $C_{ON}$  is constant to obtain a nearly constant  $f_{SW}$ .

Figure 5.58 and Table 5.4 illustrate that the optimum on-time controller can modulate the adequate  $v_{OUT,eq}$  and  $v_{Ramp}$ . Different loading conditions reflect the corresponding  $D_{actual}$  with



**Figure 5.57** Variable  $f_{SW}$  with fixed  $T_{ON}$  and fixed  $f_{SW}$  with optimum  $T_{ON}$  at different load currents



**Figure 5.58** Operating waveforms of the optimum on-time controlled buck converter in case of increasing output loading current

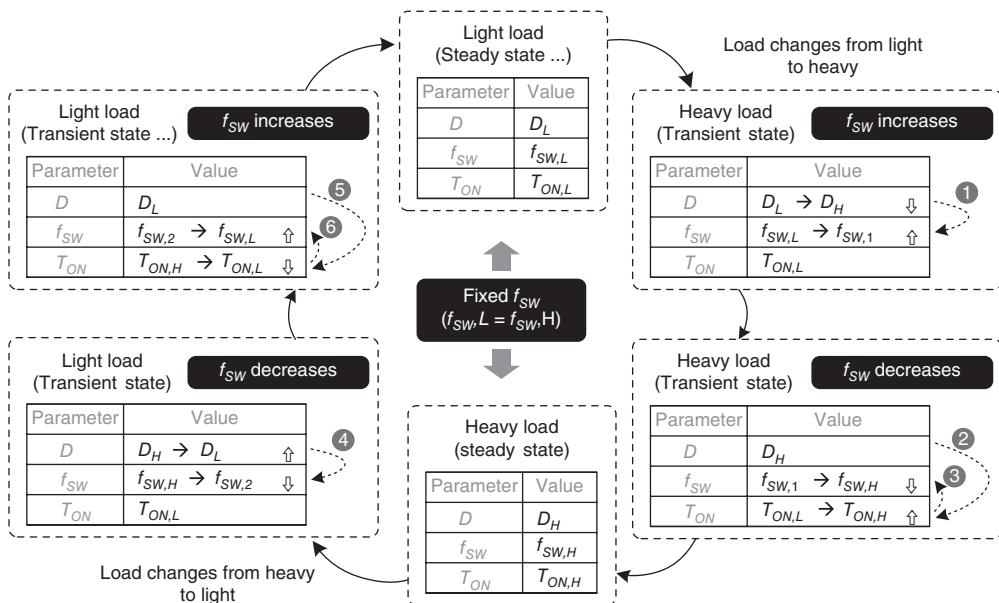
**Table 5.4** Relationship of the values in different loading conditions

$i_{Load}$	$i_{Load,a} < i_{Load,b} < i_{Load,c}$
$D_{actual}$	$D_a < D_b < D_c$
$v_{OUT,eq}$	$v_{OUT,eq,a} < v_{OUT,eq,b} < v_{OUT,eq,c}$
$T_{ON}$	$T_{ON,a} < T_{ON,b} < T_{ON,c}$
$T_{SW}$	$T_{SW,a} > T_{SW,b} > T_{SW,c}$
$f_{SW}$	$f_{SW,a} < f_{SW,b} < f_{SW,c}$

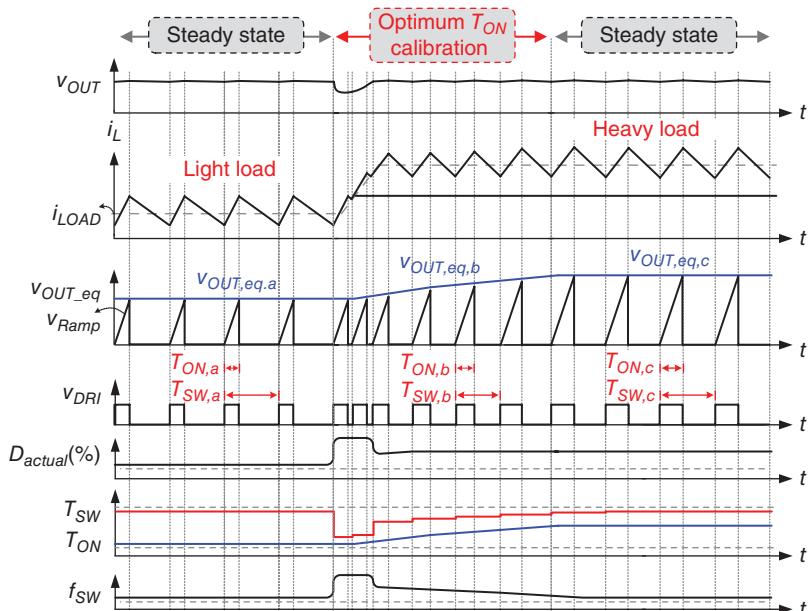
certain  $v_{OUT}$  and  $v_{IN}$  because of parasitic resistance effects. Figure 5.58 includes three cases with loading conditions  $i_{Load,a}$ ,  $i_{Load,b}$ , and  $i_{Load,c}$ , where  $i_{Load,a} < i_{Load,b} < i_{Load,c}$ . A large  $i_{Load}$  expands  $D_{actual}$ , as shown in Eq. (5.51). Consequently, PCT predicts and generates a high  $v_{OUT,eq}$  to generate a long  $T_{ON}$ . By contrast, a low  $v_{OUT,eq}$  generates  $T_{ON}$  when  $D_{actual}$  shrinks at a small  $i_{Load}$ .

Figure 5.59 explains the method to recover the constant  $f_{SW}$  during the load transient. In light-load steady state, the values of  $D$ ,  $f_{SW}$ , and  $T_{ON}$  are  $D_L$ ,  $f_{SW,L}$ , and  $T_{ON,L}$ , respectively. In heavy-load steady state, the values of  $D$ ,  $f_{SW}$ , and  $T_{ON}$  are  $D_H$ ,  $f_{SW,H}$ , and  $T_{ON,H}$ , respectively. Comparing the light and heavy loads reveals that the expected result achieves an  $f_{SW,L}$  equal to  $f_{SW,H}$  to obtain a constant switching frequency. Now, we observe the change of  $D$ ,  $f_{SW}$ , and  $T_{ON}$  if a light-to-heavy load transient is used as an example. When the load current changes from light to heavy,  $f_{SW}$  increases temporarily because  $D$  decreases and  $T_{ON}$  is not changed. In other words,  $f_{SW,1}$  is larger than  $f_{SW,L}$ , and  $D_H$  is less than  $D_L$ . Meanwhile, the optimum on-time controller adjusts  $T_{ON}$  to obtain a large value according to the increasing duty,  $D_H$ . In other words,  $T_{ON,H}$  is larger than  $T_{ON,L}$ . As a result, the shorter  $T_{ON}$  can modify  $f_{SW}$  to  $f_{SW,H}$  from the increasing value,  $f_{SW,1}$ , in which  $f_{SW,1}$  is larger than  $f_{SW,H}$ . Finally, the system enters into heavy-load steady state. According to Eqs. (5.47) and (5.71),  $T_{ON}$  adjusted by the optimum on-time controller can achieve an  $f_{SW,L}$  equal to  $f_{SW,H}$ . By contrast, the procedure is similar, although the load current changes from heavy to light.

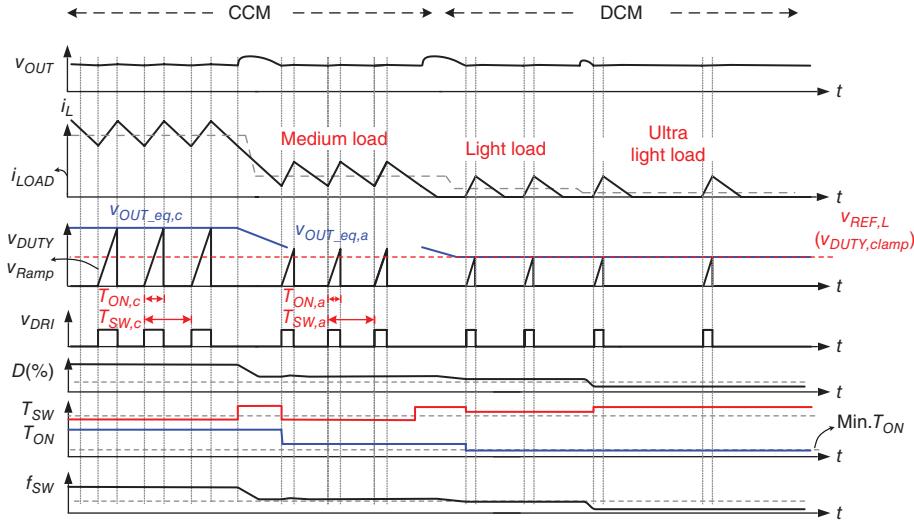
Figure 5.60 illustrates the timing diagram of the optimum on-time controller in any load current change. The EOVS circuit modulates  $v_{OUT,eq}$  as  $v_{OUT,eq,a}$  and  $T_{ON}$  as  $T_{ON,a}$  in light



**Figure 5.59** Operation of the optimum on-time controlled buck converter can keep  $f_{sw}$  constant when the output loading changes



**Figure 5.60** Timing diagram of the optimum on-time controlled buck converter to obtain a nearly constant switching frequency during light-to-heavy load transient



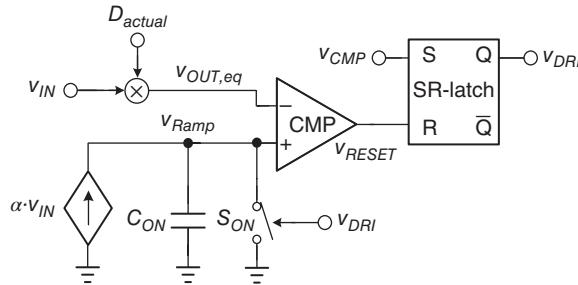
**Figure 5.61** Timing diagram of the optimum on-time controlled buck converter to obtain a nearly constant switching frequency during heavy-to-light load transient

loads. If the load current changes from light to heavy,  $T_{SW}$  will decrease because  $T_{ON}$  is too short to provide adequate energy to manage the heavy loading conditions. In this period, the switching frequency is not constant temperately. Immediately, the optimum on-time controller processes  $T_{ON}$  calibration to adjust  $T_{ON}$ . According to  $v_{IN}$  and a large  $D_{actual}$  value, which reflect the information on parasitic effects and loading condition, the EOVS circuit obtains a large  $v_{OUT,eq}$  corresponding to an optimum value  $v_{OUT,eq,c}$ . Subsequently, the OTM circuit expands  $T_{ON}$  to increase the effective value of  $T_{SW}$ .  $f_{SW}$  is regulated back to its value equivalent to that of light loads. Finally,  $f_{SW}$  is nearly constant without being affected by any disturbance.

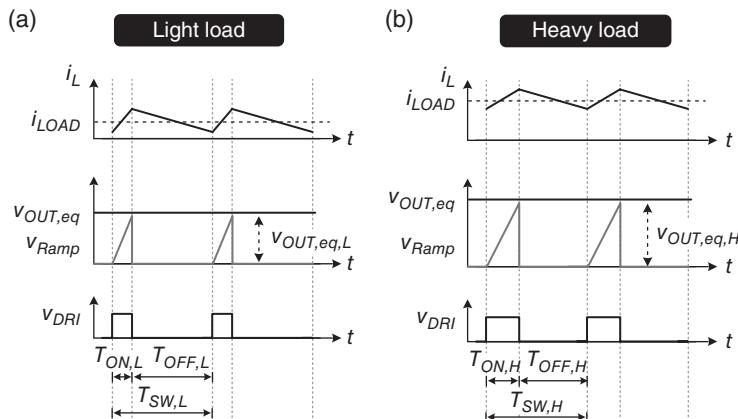
The voltage level of  $v_{OUT,eq}$  will be very high or low during the start-up period. An extreme load transient or DCM operation occurs because  $v_{OUT,eq}$  is synthesized by  $v_{GP}$ . According to Eqs. (5.68) and (5.69), this window range is designed to tolerate  $v_{OUT,eq}$ . Consequently, the voltage clamp in Figure 5.56 is used to ensure the voltage level of  $v_{OUT,eq}$  is within the adequate range. As shown in Figure 5.61, this technique thus achieves a pseudo-constant  $f_{SW}$  in the CCM. The on-time period is adjusted to a small value when the decreasing loading current results in a large  $D_{actual}$ . In the DCM, the voltage clamp limits the minimum on-time period, such that the inherent advantage to reduce  $f_{SW}$  is maintained for high efficiency.

### 5.3.2.2 Model

Figure 5.62 shows the structure to generate the adaptive on-time period with the calibration. The structure also alleviates the variation from the variations of  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$  to obtain a small  $f_{SW}$  variation. By multiplying  $D_{actual}$  and  $v_{IN}$ ,  $v_{OUT,eq}$  is obtained to represent the output information.  $D_{actual}$  represents the practical value when parasitic components are considered.



**Figure 5.62** Structure of advanced adaptive on-time period with  $v_{OUT,eq}$  for load calibration



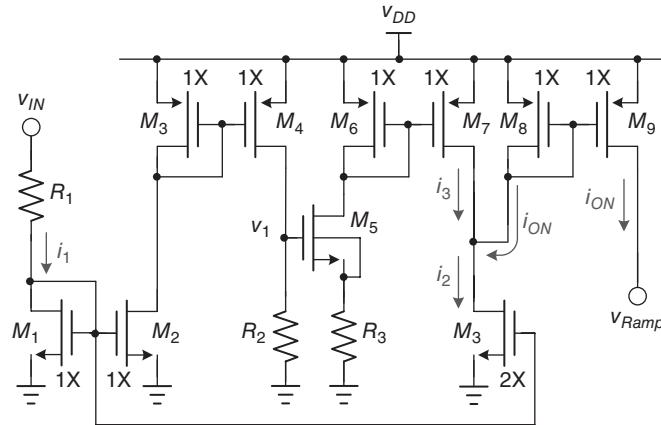
**Figure 5.63** Operating waveforms illustrate the adaptive on-time period with the calibration: (a) at light loads; (b) at heavy loads

The comparator then determines  $T_{ON}$ , as shown in Eq. (5.73), which is proportional to  $D_{actual}$ :

$$T_{ON} = \frac{C_{ON}}{\alpha} \cdot \frac{v_{OUT\_eq}}{v_{IN}} = \frac{C_{ON}}{\alpha} \cdot \frac{D_{actual} \cdot v_{IN}}{v_{IN}} \propto D_{actual} \quad (5.73)$$

Consequently, the pseudo-constant  $f_{SW}$  can be achieved by substituting Eq. (5.73) into Eq. (5.47). Figure 5.63 illustrates the operating waveforms for the on-time control with equivalent  $v_{OUT}$  information. According to Eq. (5.51), different loading conditions lead to different duty cycles. As defined in Eq. (5.45), the ratios of  $T_{ON}$  and  $T_{SW}$  reflect the duty cycle. In case of an increasing loading current, a large duty cycle leads to a high  $v_{OUT,eq}$ . In other words,  $v_{OUT,eq,L}$  is less than  $v_{OUT,eq,H}$ , such that  $T_{ON}$  is extended.

Moreover, Eq. (5.73) shows that  $T_{ON}$  is proportional to  $D_{actual}$ , which contains  $v_{OUT}$  and  $v_{IN}$  information according to Eq. (5.51). This  $T_{ON}$  also compensates for the variation of  $v_{OUT}$  and  $v_{IN}$ , implying that the frequency variation caused by different  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$  conditions can be alleviated by the modified  $T_{ON}$ .



**Figure 5.64** Implementation of the fully linear voltage-to-current generator

### 5.3.2.3 Circuit Implementation

Figure 5.64 shows the FLVCG circuit, which is implemented by core devices and low-voltage MOSFETs and is supplied by  $v_{DD}$ . Although  $v_{IN}$  is higher beyond the voltage level for core devices, the structure of the resistor  $R_1$  and the diode-connected MOSFET  $M_1$  benefits from not using a high-voltage MOSFET.  $i_1$  and  $i_2$  are generated by  $v_{IN}$ , as shown in Eq. (5.74), but  $i_1$  is not completely linear to  $v_{IN}$  because of  $v_{GS,M1}$ , which represents the gate-to-source voltage of MOSFET  $M_1$ :

$$i_1 = \frac{1}{2}i_2 = \frac{v_{IN} - v_{GS,M1}}{R_1} \quad (5.74)$$

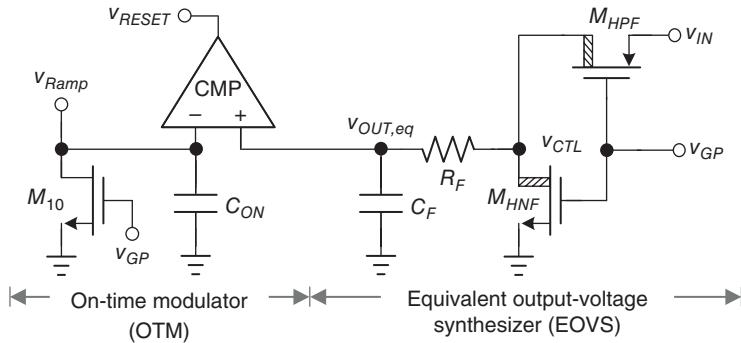
To compensate for the unexpected  $v_{GS,M1}$ ,  $M_5$  forms the source-generation structure to generate the compensated current  $i_3$ , as expressed in Eq. (5.75).  $v_{GS,M1}$  and  $v_{GS,M5}$  are nearly equal by setting  $M_1$  and  $M_5$  with the same aspect ratio and removing the body effect. Consequently,  $i_3$  is composed of  $v_{GS,M5}$  and derived in Eq. (5.76):

$$i_3 = \frac{v_1 - v_{GS,M5}}{R_3} = \frac{i_1 R_2 - v_{GS,M5}}{R_3} \quad (5.75)$$

$$i_3 = \frac{R_2 v_{IN} - (R_1 + R_2) v_{GS,M1}}{R_1 R_3} \quad (5.76)$$

Conducting  $i_2$  and  $i_3$  into the node by opposite directions generates  $i_{ON}$ , as derived in Eq. (5.77):

$$i_{ON} = i_2 - i_3 = \frac{(2R_3 - R_2)v_{IN} + (R_1 + R_2 - 2R_3)v_{GS,M1}}{R_1 R_3} \quad (5.77)$$



**Figure 5.65** Implementation of an equivalent output-voltage synthesizer and an optimum on-time synthesizer

With equal values of  $2R_1$ ,  $2R_2$ , and  $R_3$ , the current  $i_{ON}$  is obtained, as shown in Eq. (5.78). Consequently,  $i_{ON}$  is converted from  $v_{IN}$  by FLVCG and is proportional to  $v_{IN}$ . Then, the current  $i_{ON}$  is used to charge into  $C_{ON}$ , such that  $v_{Ramp}$  increases the voltage, and the increase in rate is proportional to  $v_{IN}$ :

$$i_{ON} = \frac{3}{2} \frac{v_{IN}}{R_1} \quad (5.78)$$

By contrast, Figure 5.65 shows the implementation of EOVS and OTM. All devices are implanted with low voltage, except for  $M_{HPF}$  and  $M_{HNF}$ , which are high-voltage MOSFETs because of  $v_{IN}$  and  $v_{GP}$ . The right portion is EOVS and structured by  $M_{HPF}$ ,  $M_{HNF}$ ,  $R_F$ , and  $C_F$ . The signals  $v_{IN}$  and  $v_{GP}$  control EOVS to produce  $v_{OUT,eq}$ . Signal  $v_{OUT,eq}$  is expressed as Eq. (5.71) because  $v_{GP}$  drives the signal to control the high-side power MOSFET  $M_P$ , and the duty of  $v_{GP}$  is equal to the ratios of  $T_{ON}$  and  $T_{SW}$ .

When  $v_{Ramp}$  and  $v_{OUT,eq}$  are compared,  $T_{ON}$  is determined by the OTM according to the duration when  $v_{Ramp}$  is below  $v_{OUT,eq}$ . Consequently,  $T_{ON}$  is proportional to  $D_{actual}$ , which is derived as Eq. (5.79) using  $v_{OUT,eq}$ ,  $C_{ON}$ , and  $i_{ON}$ :

$$T_{ON} = \frac{C_{ON} \cdot v_{OUT,eq}}{I_{ON}} = \frac{2}{3} C_{ON} \cdot R_1 \cdot \frac{v_{IN} \cdot D_{actual}}{v_{IN}} \propto D_{actual} \quad (5.79)$$

Substituting Eq. (5.79) into Eq. (5.47) yields a thoroughly constant  $T_{SW}$  because of the independence of  $v_{IN}$ ,  $v_{OUT}$ ,  $D_{actual}$ ,  $i_{Load}$ , and the parasitic resistances. The ripple of  $v_{OUT,eq}$  is also derived approximately in Eq. (5.80). For example, to ensure the ripple is small enough in this work,  $C_F$  is 1 pF and  $R_F$  is 5 MΩ when  $v_{IN}$  is 3.3 V,  $v_{OUT}$  is 1.05 V, and  $f_{SW}$  is 2.5 MHz:

$$v_{OUT,eq,pp} = T_{ON} \cdot \frac{v_{IN}}{R_F \cdot C_F} \quad (5.80)$$

### 5.3.3 Type-II Optimum On-Time Controller with Equivalent $V_{DUTY}$

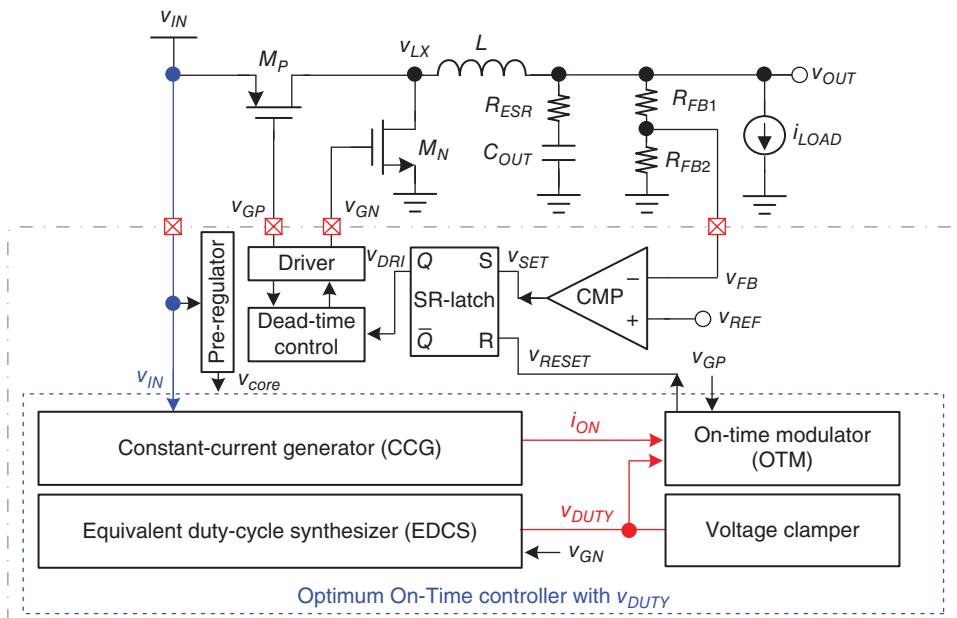
#### 5.3.3.1 Architecture and Operation of Converter

In addition to the optimum on-time controller with  $v_{OUT,eq}$  and  $v_{IN}$ , as depicted in Figure 5.56, the optimum on-time controller can be modified as shown in Figure 5.66. This modified optimum on-time controller comprises the constant-current generator (CCG), EDCS, OTM, and voltage clamer. This controller further removes the need for information on  $v_{IN}$ . In other words,  $v_{GP}$  is the only necessary information.

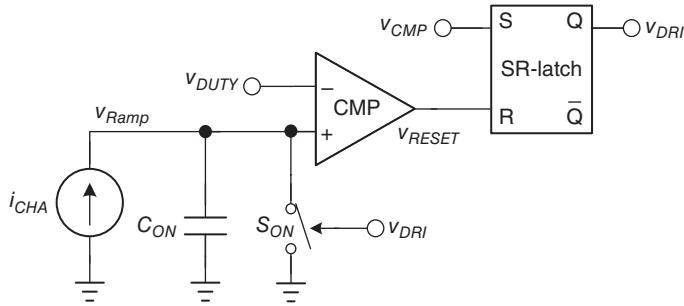
The CCG block generates the constant current  $i_{ON}$ , which is independent of variations of  $v_{IN}$ ,  $v_{OUT}$ , and  $i_{Load}$ . The EDCS circuit modulates the equivalent duty-cycle voltage ( $v_{DUTY}$ ) by driving the signal  $v_{GP}$ . The OTM circuit outputs  $v_{RESET}$  to determine the on-time period by  $i_{ON}$  and  $v_{DUTY}$ . Similar to the operation and performance of the optimum on-time controller in Figure 5.66, this optimum on-time controller achieves constant  $f_{SW}$  without the need for extra complex current-sensing circuits and the detection of the on-resistance of the power MOSFET and  $R_{DCR}$  of the inductor.

#### 5.3.3.2 Model

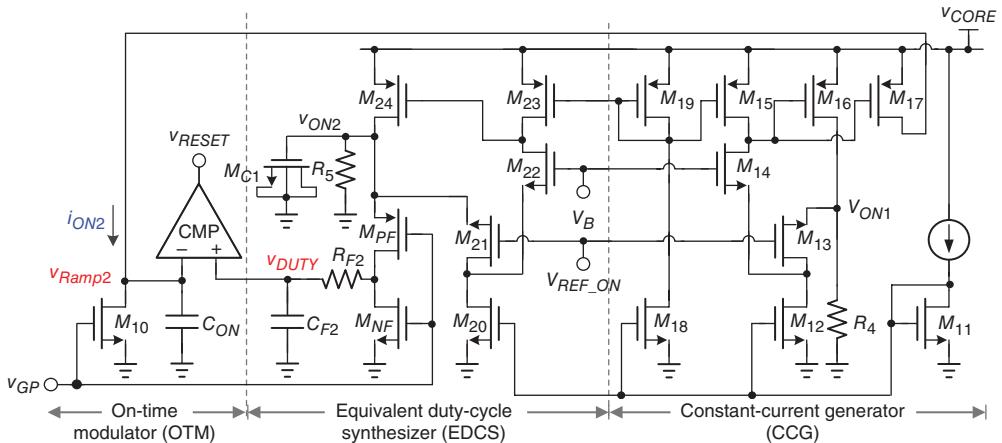
According to Eq. (5.47),  $T_{ON}$  can be designed directly by  $D$  information instead of  $v_{IN}$  and  $v_{OUT}$  information, such that the frequency variation can be compensated. With a similar structure, the current,  $i_{CHA}$ , is used to charge the on-time capacitor  $C_{ON}$  to reach an upper bound and determine the value of  $T_{ON}$ .  $i_{CHA}$  should be constant and be independent of any perturbation from



**Figure 5.66** Architecture of the optimum on-time controlled buck converter using  $V_{DUTY}$



**Figure 5.67** Structure of Type-II optimum on-time controller with  $v_{DUTY}$



**Figure 5.68** Implementation of Type-II optimum on-time controller including OTM, EDCS, and CCG

$v_{IN}$ ,  $v_{OUT}$ ,  $i_{Load}$ , and so on. The upper bound is set by an equivalent duty,  $v_{DUTY}$ , whose value is proportional to  $D$  information (Figure 5.67):

$$T_{ON} = \frac{C_{ON} \cdot v_{DUTY}}{i_{ON}} = \frac{C_{ON} (k \cdot D_{actual})}{i_{ON}} \propto D_{actual} \quad (5.81)$$

where  $k = \text{constant}$

### 5.3.3.3 Circuit Implementation

Figure 5.68 provides another circuit implementation to realize the optimum  $T_{ON}$  with  $i_{CH4}$  and  $v_{DUTY}$ . The complexity of CCG is reduced compared with that of FLVCG, and the new EDCS removes the need for high-voltage MOSFETs. Furthermore, only one control signal  $v_{GP}$  is needed.  $V_{REF\_ON}$  is a reference voltage with constant value, and  $v_B$  is a voltage to bias  $M_{22}$

and  $M_{14}$ . In the CCG of the right portion,  $M_{13}$  is a voltage follower to determine  $v_{ON1}$  from  $V_{REF\_ON}$ . Then,  $R_4$  and  $M_{13}-M_{17}$ , which are structured by negative feedback, determine the current of  $M_{17}$  as the value

$$i_{ON} = \frac{V_{REF\_ON} + v_{GS13}}{R_4} \quad (5.82)$$

In the EDCS of the middle portion,  $M_{21}$  is the voltage follower to determine  $v_{ON2}$  from  $V_{REF\_ON}$ . Then, MOSFETs  $M_{21}-M_{24}$ , which are structured by negative feedback, provide the driving capability to regulate  $v_{ON2}$  as the value

$$v_{ON2} = V_{REF,ON} + v_{GS,M21} \quad (5.83)$$

$R_5$  and  $M_{C1}$  are used to bias  $M_{24}$  and assist the regulation.  $v_{GP}$  then utilizes  $M_{PF}$ ,  $M_{NF}$ ,  $R_{F2}$ , and  $C_{F2}$  to generate  $v_{DUTY}$ :

$$v_{DUTY} = v_{ON2} \cdot D_{actual} \quad (5.84)$$

Consequently, the OTM in the left portion uses  $v_{DUTY}$  and  $i_{ON2}$  to determine  $T_{ON}$ :

$$T_{ON} = i \frac{C_{ON} \cdot v_{DUTY}}{I_{ON2}} = C_{ON} \cdot \frac{(V_{REF\_ON} + v_{GS,M21}) \cdot D_{actual}}{(V_{REF\_ON} + v_{GS,M13}) \cdot \frac{1}{R_4}} \propto D_{actual} \quad (5.85)$$

The optimum  $T_{ON}$  proportional to  $D_{actual}$  can be obtained because  $V_{REF\_ON}$ ,  $v_{GS21}$ ,  $v_{GS13}$ , and  $C_{ON}$  are constant.

### 5.3.4 Frequency Clammer

Figure 5.69 shows the voltage clammer, including lower-bound and upper-bound clamps. When  $v_{OUT,eq}$  is lower than the lower-bound voltage  $V_{REF,L}$ ,  $M_{30}$  and  $M_{31}$  can drive  $M_{32}$  to clamp  $v_{OUT,eq}$  at the voltage level of  $V_{REF,L}$ . By contrast, when  $v_{OUT,eq}$  is higher than the upper-bound voltage  $V_{REF,H}$ ,  $M_{35}$  and  $M_{36}$  can drive  $M_{37}$  to clamp  $v_{OUT,eq}$  at the voltage level of  $V_{REF,H}$ . In other words, the swing range of  $v_{OUT,eq}$  ensures the window between  $V_{REF,L}$  and  $V_{REF,H}$ . Moreover, MOSFETs  $M_{31}$ ,  $M_{32}$ ,  $M_{36}$ , and  $M_{37}$  can be off and have no influence on  $v_{OUT,eq}$  when  $v_{OUT,eq}$  is within the window.

### 5.3.5 Comparison of Different On-Time Controllers

Table 5.5 compares the various on-time controllers. A comparison of the structures in Figures 5.62 and 5.67 demonstrates that the structure in Figure 5.62 is more complex because the charging current should be dependent on  $V_{IN}$  information to calibrate the variation of  $v_{OUT,eq}$ . By contrast, the structure in Figure 5.67 only requires the driving signal information, such that the structure becomes simpler. The circuit implementation in Figure 5.64 for the structure in Figure 5.62 should carefully consider the accuracy of resistors and the current mirror, as

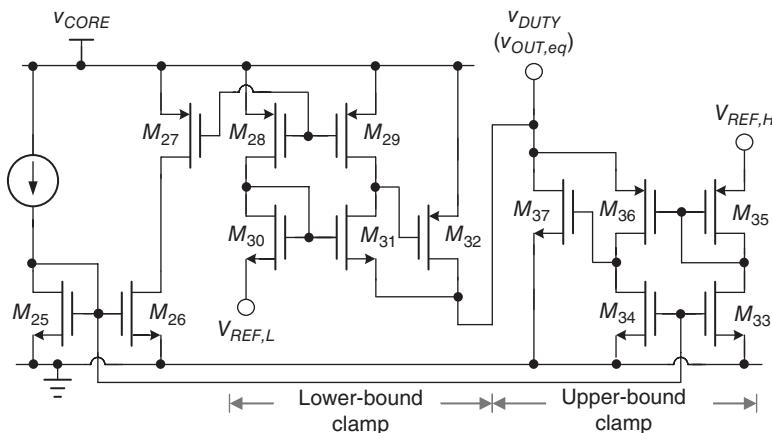


Figure 5.69 Voltage clamer

Table 5.5 Comparison of different on-time controllers

	Fixed $T_{ON}$	Basic adaptive $T_{ON}$ with $v_{IN}$ and $v_{OUT}$	Adaptive $T_{ON}$ with $v_{LX}$ and $v_{IN}$	Type-I optimum $T_{ON}$ with $v_{OUT,eq}$ and $v_{IN}$	Type-II optimum $T_{ON}$ with $v_{DUTY}$
Structure	Figure 5.44	Figure 5.47	Figure 5.52	Figure 5.62	Figure 5.67
Circuit implantation		Type I in Figure 5.50 Type II in Figure 5.51 Type III in Figure 5.54 FLVCG in Figure 5.64		Figure 5.65	Figure 5.68
Required information	$v_{DRI} (v_{GP})$	$v_{IN}$ $v_{OUT}$	$v_{LX}$ $v_{OUT}$	$v_{IN}$ $v_{OUT}$	$v_{DRI} (v_{GP})$
		$v_{DRI} (v_{GP})$	$v_{DRI} (v_{GP})$	$v_{DRI} (v_{GP})$	
Design issue		<ul style="list-style-type: none"> <li>• Matching issue should be designed carefully</li> <li>• Charging current should be fully linear to <math>v_{IN}</math></li> <li>• High-voltage devices are needed because of the use of <math>v_{IN}</math></li> </ul>			
Flexibility	Poor	Charging current dependent on $v_{IN}$ is difficult to achieve			Excellent
$\Delta f_{SW}$ by $v_{IN}$ and $v_{OUT}$	Poor	Good	Good	Excellent	Excellent
$\Delta f_{SW}$ by $i_{Load}$	Poor	Poor	Good	Excellent	Excellent

well as the issue of body effect. Owing to the mismatch value, Eq. (5.78) is difficult to achieve and causes a large variation in switching frequency. The desired switching frequency is also difficult to adjust. On the contrary, the circuit implemented in Figure 5.68 for the structure in Figure 5.67 provides more flexible and robust performance. The desired switching frequency can be adjusted by the value of  $R_4$ , which is a discrete component. The switching frequency variation is more independent of the process variation or mismatch problem. This structure reduces the required information on  $v_{OUT}$  and  $v_{IN}$ . It can release strict design considerations, including the matching design of the resistor and the current mirror, high linearity between  $v_{IN}$  and charging current, and use of high-voltage devices.

### 5.3.6 Simulation Result of Optimum On-Time Controller

The on-time control DC/DC converter is simulated in the UMC 28 nm CMOS process. In simulation results, Type-I PCT is implemented to demonstrate and observe the different fixed  $v_{OUT}$  in conventional constant on-time control and variable  $v_{OUT,eq}$  in the optimum on-time control. Figure 5.70 demonstrates the function of the PCT for the desired  $f_{SW} = 800$  kHz. The specifications are  $v_{IN} = 3.3$  V,  $v_{OUT} = 1.05$  V,  $L = 2.2$   $\mu$ H, and  $C_{OUT} = 4.7$   $\mu$ F. The parasitic effects are also considered, in which  $R_{on,P}$  and  $R_{on,N}$  are 150 and 100 m $\Omega$ , respectively, and the  $R_{DCR}$  of the inductor is 30 m $\Omega$ . The waveforms include  $v_{OUT}$ ,  $i_L$ ,  $v_{Ramp}$ ,  $v_{OPT}$ , and  $v_{GP}$ . With conventional on-time control,  $\Delta f_{SW}$  is approximately 76 kHz when the  $i_{Load}$  change is 1.5 A. By contrast, the PCT ensures that the  $f_{SW}$  variation is lower than 3 kHz. Particularly,  $v_{OUT,eq}$  increases as  $i_{Load}$  increases to achieve optimum  $T_{ON}$ .

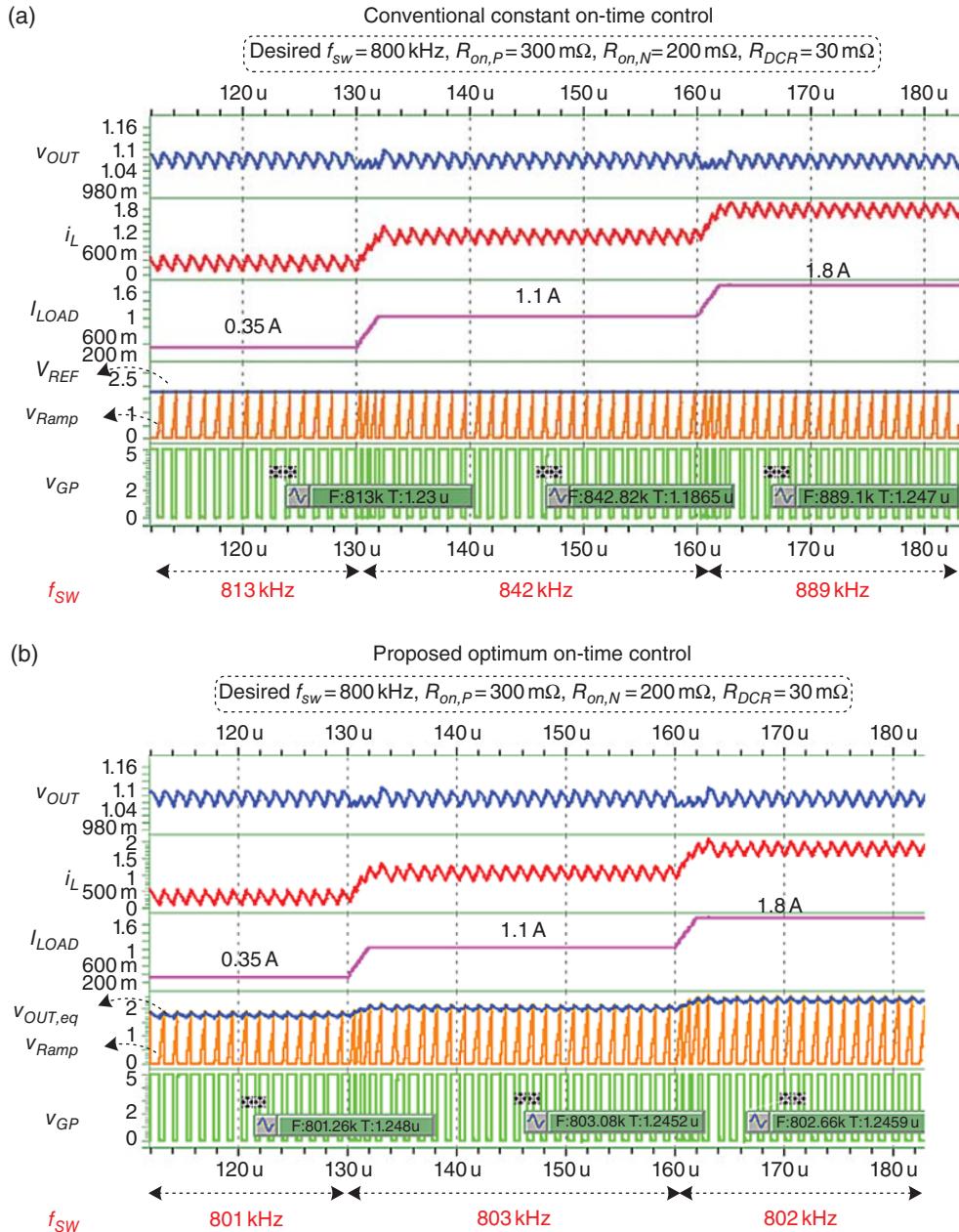
Figure 5.71 demonstrates the function of the PCT if the desired  $f_{SW}$  is 2.5 MHz, where  $L$  is 1  $\mu$ H. Under the same parameters of parasitic effects, the performance comparison is shown in Figure 5.70. In conventional on-time control,  $\Delta f_{SW}$  is approximately 410 kHz when the  $i_{Load}$  change is 1.5 A. By contrast, the PCT ensures that  $\Delta f_{SW}$  is lower than 4 kHz.

Table 5.6 shows the performance of the simulation result. By comparing Figures 5.70(a) and 5.71(a) with the conventional constant on time, the higher desired  $f_{SW}$  results in a larger  $\Delta f_{SW}$ , which is consistent with the analysis result. The PCT benefits ultra-low  $\Delta f_{SW}$ , as shown in both.

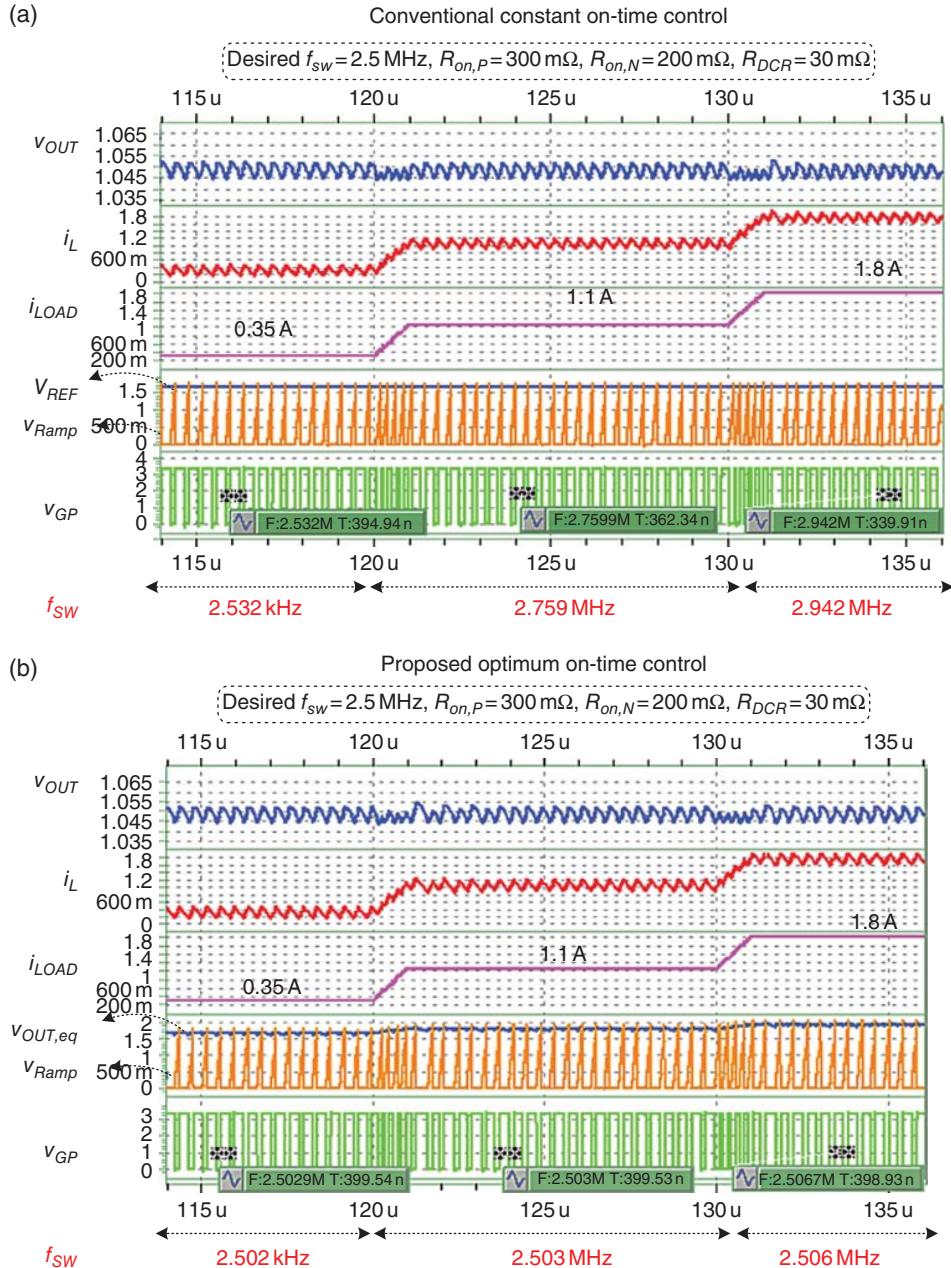
Figure 5.72 shows the performance of the simulation result with the desired  $f_{SW} = 800$  kHz.  $f_{SW}$  is nearly constant, although the parasitic effect is more serious when  $R_{on,P}$  is 300 m $\Omega$  and  $R_{on,N}$  is 200 m $\Omega$ . The performance of the  $f_{SW}$  variation is defined by  $\Delta f_{SW}/f_{SW}$  and  $\Delta f_{SW}/\Delta i_{Load}$ . The PCT has a performance of 0.375%  $\Delta f_{SW}/f_{SW}$  and 2 kHz/A  $\Delta f_{SW}/\Delta i_{Load}$ . By contrast, conventional on-time has  $\Delta f_{SW}/f_{SW}$  of more than 9.5% and  $\Delta f_{SW}/\Delta i_{Load}$  of more than 50 kHz/A.

### 5.3.7 Experimental Result of Optimum On-Time Controller

The Type-II optimum on-time controlled buck converter is fabricated by UMC 28 nm CMOS technology. The specifications include  $v_{IN} = 3.3$  V,  $v_{OUT} = 1.05$  V,  $L = 1$   $\mu$ H,  $C_{OUT} = 4.7$   $\mu$ F, and  $f_{SW} = 2.5$  MHz. The results show  $R_{on,P}$  and  $R_{on,N}$  are 300 and 200 m $\Omega$ , respectively.  $R_{DCR}$  of the inductor is 30 m $\Omega$ . Figure 5.73 shows the waveforms of the conventional on-time controller when  $i_{Load}$  changes from 1.7 to 0.3 A, and vice versa. The on-time period remains constant at different loading conditions in the conventional design. However, the change in slopes of



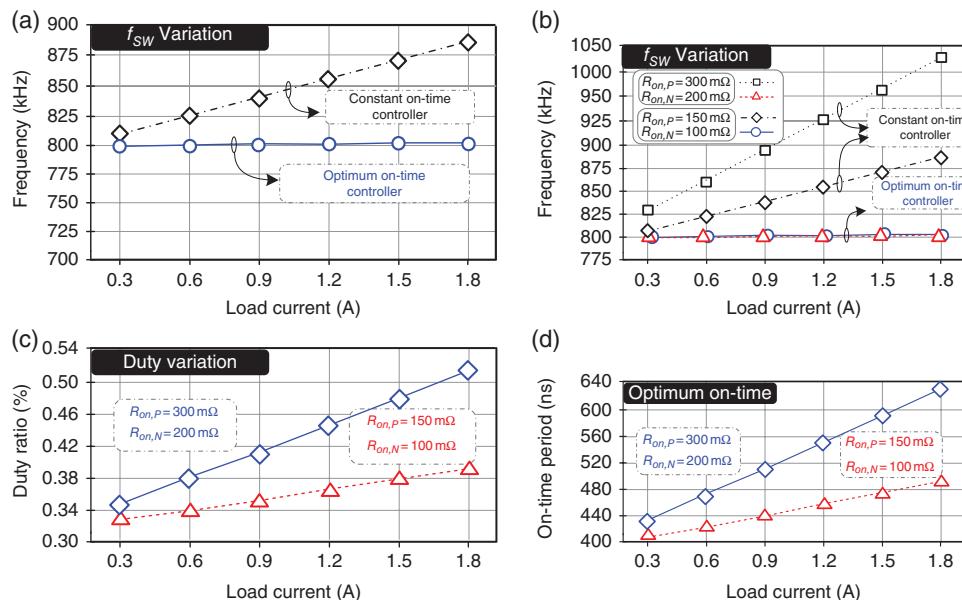
**Figure 5.70** Simulation result of converter with desired  $f_{sw} = 800 \text{ kHz}$ . (a) Constant on-time control. (b) Optimum on-time control with PCT



**Figure 5.71** Simulation result of the converter with desired  $f_{sw}=2.5$  MHz. (a) Constant on-time control. (b) Optimum on-time control with PCT

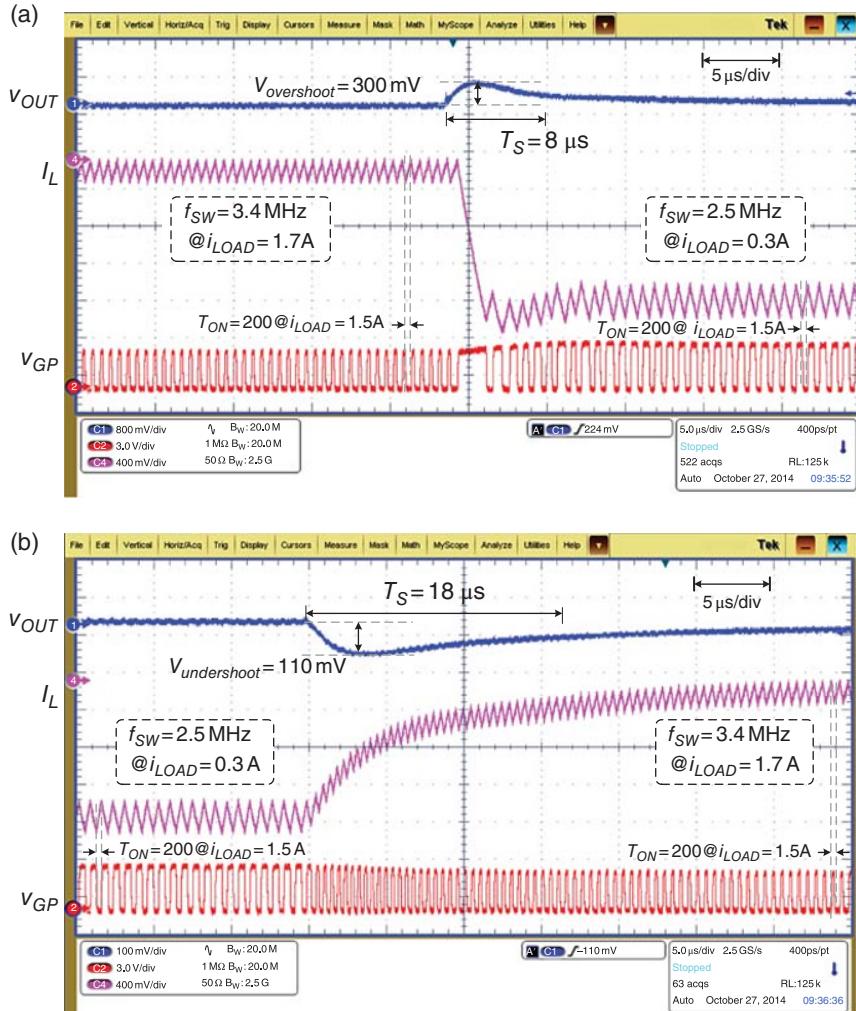
**Table 5.6** Comparison table of conventional COT converter and the COT converter with PCT technique

Control method	Constant on-time		Optimum on-time	
$v_{IN}$ (V)	3.3		3.3	
$v_{OUT}$ (V)	1.05		1.05	
$L$ ( $\mu$ H)	1		2.2	
$C_{OUT}$ ( $\mu$ F)	4.7		4.7	
$\Delta i_{Load}$ (A)	1.5		1.5	
Desired $f_{SW}$	800 kHz	2.5 MHz	800 kHz	2.5 MHz
$\Delta f_{SW}$ (kHz)	76	410	3	4
$\Delta f_{SW}/f_{SW}$ (%)	9.5	16.4	0.375	0.16
$\Delta f_{SW}/\Delta i_{Load}$ (kHz/A)	50.6	273.3	2	2.6

**Figure 5.72** Switching frequency variation during different load conditions

$i_L$  and  $D_{actual}$  is due to the parasitic effects.  $f_{SW}$  is 2.5 and 3.4 MHz when  $i_{Load}$  is 0.3 and 1.7 A, respectively. The  $f_{SW}$  variation is approximately 0.9 MHz for a 1.4 A change in  $i_{Load}$ .

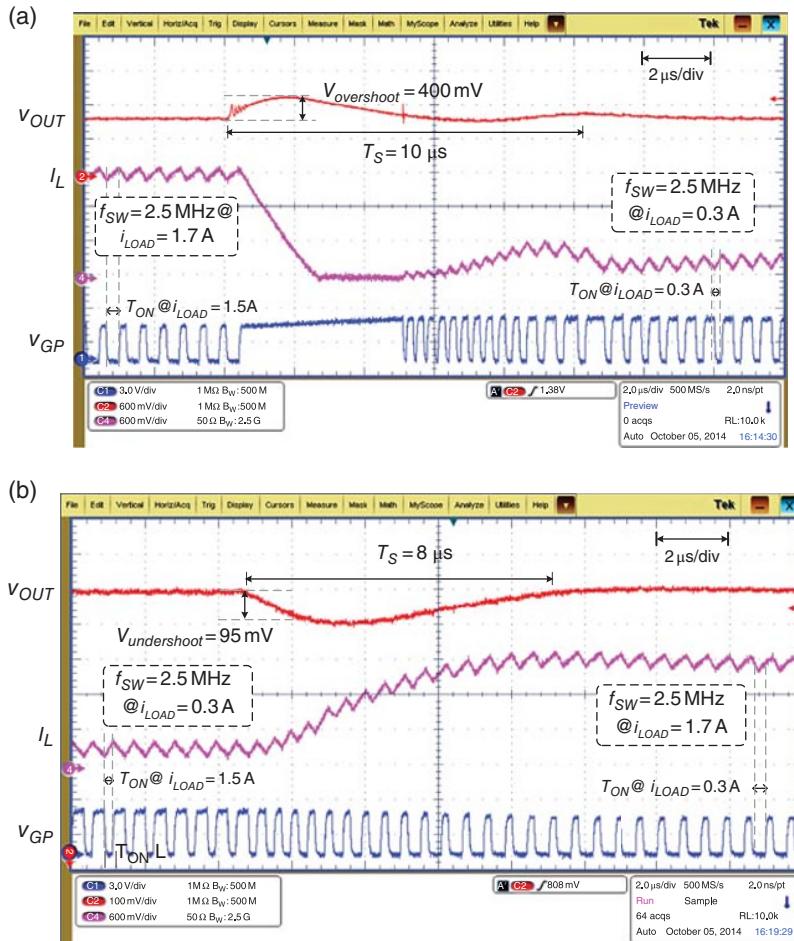
By contrast, Figure 5.74 demonstrates the function of the optimum on-time controller. Figure 5.75 provides the zoomed-in waveforms in steady state. Although the slopes of  $i_L$  and  $D_{actual}$  continue to change at different loading conditions because of the parasitic effects,



**Figure 5.73** Frequency variation in constant on-time controlled buck converter when  $i_{Load}$  changes (a) from heavy to light load and (b) from light to heavy load

$f_{SW}$  is nearly constant at 2.5 MHz during adjustable on-time periods.  $T_{ON}$  is 170 ns and the duty cycle is 0.35 at light loads, whereas  $T_{ON}$  is adjusted to 210 ns and its duty cycle is 0.52 at heavy loads.  $\Delta f_{SW}$  is approximately 8 kHz when the change in  $i_{Load}$  is 1.4 A.

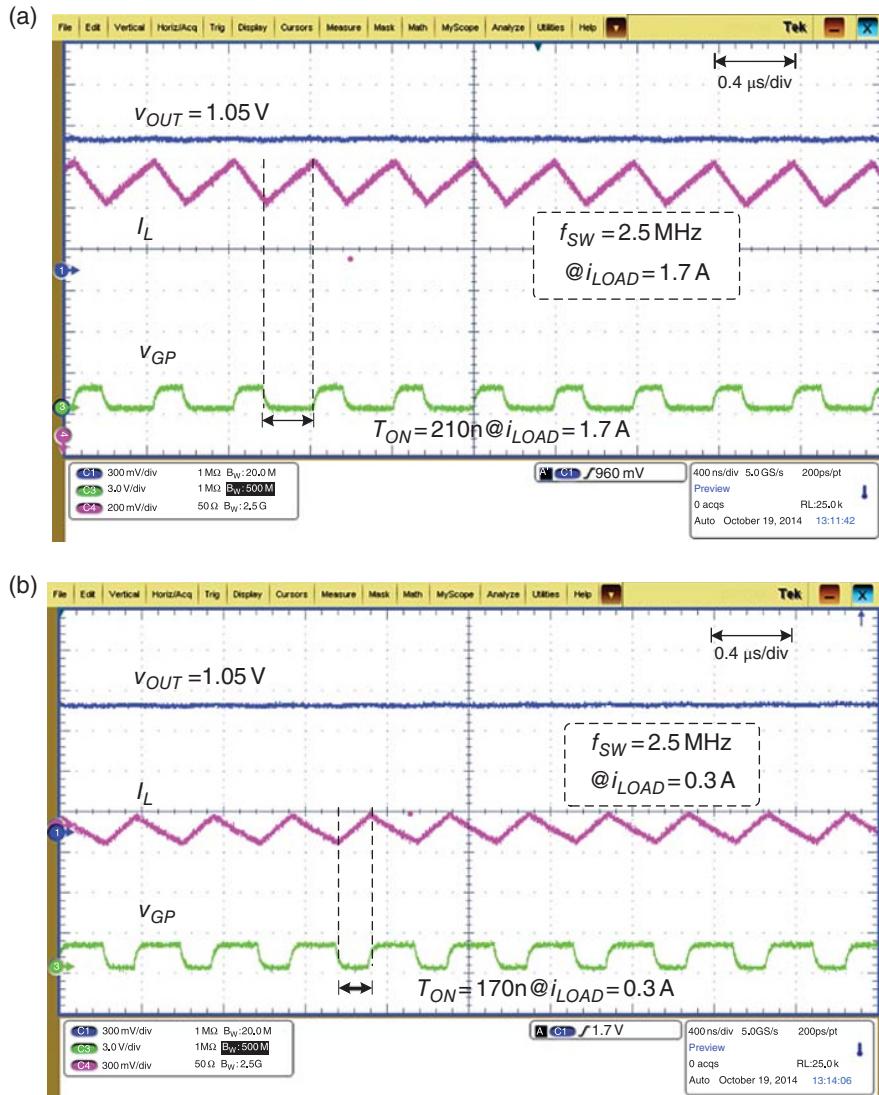
Table 5.7 shows the comparison of prior methods. The performance of  $f_{SW}$  variation is indicated by  $\Delta f_{SW}/f_{SW}$  and  $\Delta f_{SW}/\Delta i_{Load}$ . The designs in [11, 12, 25] achieve good performance at  $\Delta f_{SW}/f_{SW}$  and  $\Delta f_{SW}/\Delta i_{Load}$ , but the extra clock signal and complex PLL-based loop should be employed. The design in [17, 29] also reduces the complexity of the controller, and these



**Figure 5.74** Pseudo-constant frequency in optimum on-time controlled buck converter when  $i_{Load}$  changes (a) from heavy to light load and (b) from light to heavy load

designs remove the need for an extra clock signal and achieve adaptive on-time, but the performance of  $\Delta f_{SW}$  in these designs is withdrawn.

Figure 5.76 shows the performance, which includes the constant on-time control, optimum on-time control, LCC [17], and SLCC [29]. The design in [17] using current sensing performs with  $\Delta f_{SW}/f_{SW}$  of 9.5% and  $\Delta f_{SW}/\Delta i_{Load}$  of 129 kHz/A. The design in [29] utilizes the RC network, but the  $f_{SW}$  changes from 600 to 800 kHz when the load changes from 200 to 900 mA. According to the measured transient waveforms,  $\Delta f_{SW}/f_{SW}$  is 25% and  $\Delta f_{SW}/\Delta i_{Load}$  is 285.7 kHz/A. By contrast, the optimum on-time controller ensures that the  $f_{SW}$  variation is lower than 8 kHz when  $f_{SW}$  is 2.5 MHz. Although the parasitic effects are severe,  $f_{SW}$  is nearly

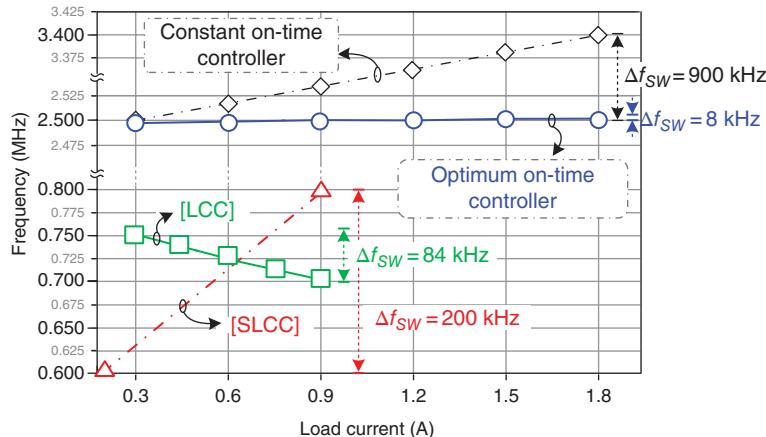


**Figure 5.75** Steady state of the optimum on-time controlled buck controller: (a)  $i_{Load} = 1.7 \text{ A}$ ; (b)  $i_{Load} = 0.3 \text{ A}$

constant, in which  $R_{on,P}$  and  $R_{on,N}$  are 300 and 200 mΩ, respectively. The optimum on-time controller has good performances in  $\Delta f_{SW}/f_{SW} = 0.32\%$  and  $\Delta f_{SW}/\Delta i_{Load} = 5.7 \text{ kHz/A}$  at  $f_{SW} = 2.5 \text{ MHz}$ . In this work, the peak efficiency is 89%, which is dominated by the on-resistance of the power stage. The values of these on-resistances are designed larger than that

**Table 5.7** Comparison table of state-of-the-art COT converters

Control method	PLL-based [15]	PLL-based [12]	PLL-based [11]	DADC [13]	LCC (load sensing) [17]	SLCC [29]	Constant on-time	Optimum on-time
$v_{IN}$	3 V	2.7–4.5 V	2.5 V	2.7–3.3 V	3.3 V	2.7–3.6 V	3.3 V	3.3 V
$v_{OUT}$	1.8 V	2 V	0.7–1.8 V	0.9–2.1 V	1.2 V	1–1.2 V	1.05 V	1.05 V
$L$	4.7 $\mu$ H	4.7 $\mu$ H	1–5 $\mu$ H	2.2 $\mu$ H	4.7 $\mu$ H	N/A	1 $\mu$ H	1 $\mu$ H
$C_{out}$	4.7 $\mu$ F	10 $\mu$ F	10 $\mu$ F	4.4 $\mu$ F	8.9 $\mu$ F	N/A	4.7 $\mu$ F	4.7 $\mu$ F
$R_{on,P}$	N/A	N/A	N/A	N/A	N/A	N/A	300 m $\Omega$	300 m $\Omega$
$R_{on,N}$							200 m $\Omega$	200 m $\Omega$
$R_{DCR}$							30 m $\Omega$	30 m $\Omega$
$f_{SW}$	1 MHz	1 MHz	1 MHz	3 MHz	750 kHz	800 kHz	2.5 MHz	2.5 MHz
$\Delta f_{SW}$	15 kHz	2 kHz	5 kHz	100 kHz	84 kHz	200 kHz	900 kHz	8 kHz
$\Delta f_{SW}/f_{SW}$	1.5%	0.2%	0.5%	3.3%	11.2%	25%	36%	0.32%
$\Delta i_{Load}$	0.25 A	0.4 A	0.6 A	0.45 A	0.65 A	700 mA	1.4 A	1.4 A
$\Delta f_{SW}/\Delta i_{Load}$	60 kHz/A	5 kHz/A	8 kHz/A	222.2 kHz/A	129 kHz/A	285.7 kHz/A	642.8 kHz/A	5.7 kHz/A
Extra $V_{CLK}$	Required	Required	Required	Not required	Not required	Not required	Not required	Not required
Maximum efficiency	95%	95.5%	93%	93%	87%	88.2%	89%	89%



**Figure 5.76** Switching frequency variation during different loading conditions

of the general design to demonstrate the performance of the optimum on-time controller. Although the power stage contains serious parasitic effects, the optimum on-time controller can achieve pseudo-constant  $f_{SW}$ , which has a competitive performance for the design applied by PLL.

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# 6

# Single-Inductor Multiple-Output (SIMO) Converter

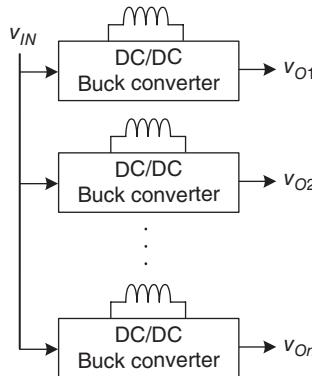
## 6.1 Basic Topology of SIMO Converters

Conventionally,  $n$  parallel DC/DC buck converters are most commonly used to generate  $n$  supplying voltages  $v_{O1}–v_{On}$ , as illustrated in Figure 6.1. High power efficiency is achieved through distributive voltage/current levels because of the inherent characteristics of the DC/DC buck converter. However, this topology requires  $n$  inductors and  $n$  buck converter chips on the PCB, and the volume and cost of tablets and/or portable devices are largely increased. To suppress the volume of the power management unit (PMU),  $n$  parallel low dropouts (LDOs) are cascaded after one DC/DC buck converter as shown in Figure 6.2, because only one inductor, one buck converter chip, and  $n$  small LDO chips are required. Nevertheless, large dropout voltages across the LDOs occur when the corresponding output voltage is low, which deteriorates the power efficiency, and the charge in the battery runs out in a short time. The solution in Figure 6.2 is not efficient for tablets or portable devices.

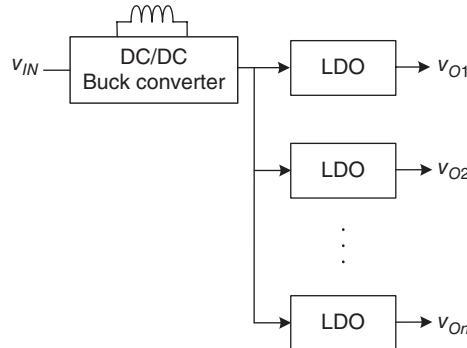
Instead, a SIMO DC/DC converter is able to simultaneously generate  $n$  supply voltages, as shown in Figure 6.3, by adopting only one inductor and one SIMO converter chip [1, 2]. The advantages are that the PCB area and cost are largely suppressed.  $v_{O1}–v_{On}$  can be well regulated by properly allocating the energy stored in the inductor to each output voltage. Therefore, SIMO DC/DC converters are more attractive in applications that need multiple supply voltages.

### 6.1.1 Architecture

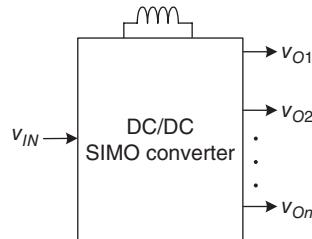
The simplified architecture of a SIMO converter, which can be divided into power stage and controller, is illustrated in Figure 6.4. Similar to DC/DC buck converters, the high-side power MOSFET  $M_H$ , low-side power MOSFET  $M_L$ , and inductor  $L$  control acquire energy from the input source  $v_{IN}$  and store the energy in the inductor. In SIMO converters,  $n$  additional switches



**Figure 6.1**  $n$  supply voltages are generated by  $n$  parallel DC/DC buck converters



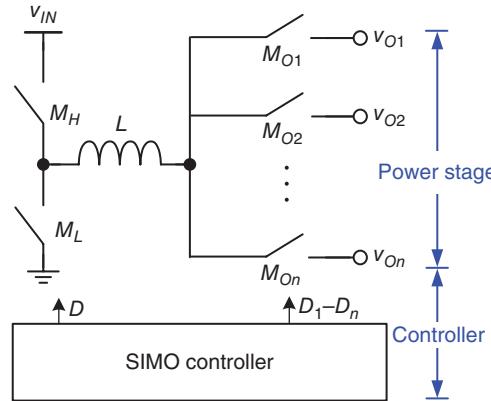
**Figure 6.2**  $n$  supply voltages are generated by cascading one DC/DC buck converter and  $n$  parallel LDOs



**Figure 6.3**  $n$  supply voltages are generated by one SIMO converter

are adopted to appropriately allocate the stored energy to  $n$  outputs  $v_{O1}–v_{On}$ . Therefore,  $n$  different voltage levels can be generated to meet the requirements of a variety of applications.

A SIMO controller must control the turning on/off periods of all the switches. The duty cycle control signals  $D$ ,  $(1 - D)$ , and  $D_1–D_n$  must be generated to control the power switches  $M_H, M_L$



**Figure 6.4** Simplified architecture of the SIMO converter.

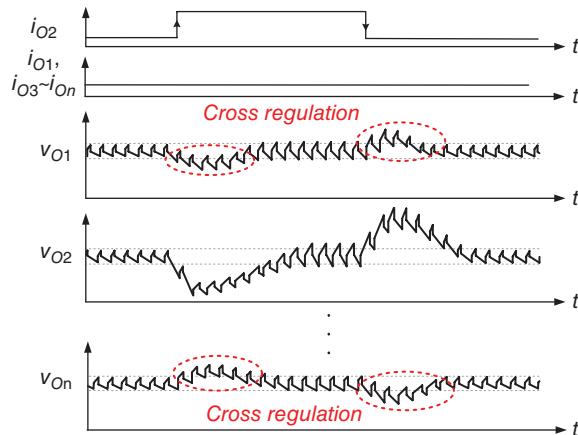
and the output switches  $M_{O1}$ – $M_{On}$ , respectively, for the voltage regulation of each output. The SIMO converter design is divided into two parts: the power stage and the controller design. At the power stage,  $2n$  paths are formed by the combinations of  $M_H$ ,  $M_L$ , and  $M_{O1}$ – $M_{On}$ . Thus, different arrangements of the energy path sequence are realized for different design targets [3]. Moreover, additional auxiliary switches can also be included to improve the performance of SIMO converters, especially for high power-conversion efficiency. Most importantly, selecting an adequate power switch control method considering high power-conversion efficiency is crucial. As we know, trade-off designs exist among the performance of SIMO converters. The power switch control method in controller designs can determine the duty cycles of all the switches in a pre-designed energy path sequence or load-dependent energy path sequence. How to choose control methods, such as the ripple- and error-based control, is discussed below.

### 6.1.2 Cross Regulation

Since all outputs share only one inductor with each other in the SIMO converter, interference among them occurs only occasionally. Accumulated or insufficient energy in a single inductor causes the phenomenon of cross regulation in SIMO converters [4]. As depicted in Figure 6.5, when the load current variation occurs at  $v_{O2}$ , while  $i_{O1}$  and  $i_{O3}$ – $i_{On}$  remain constant,  $v_{O2}$  naturally results in undershoot and overshoot at heavy and light loads, which are similar to a transient response in a single-output buck converter. However, unintended voltage variations also occur in  $v_{O1}$  and  $v_{O3}$ – $v_{On}$ . These unintended voltage variations at victim outputs without any load variations are called “cross regulation.” Cross regulation can be defined as the ratio of voltage variation at the output without any load variations to load current variation at a certain output, as expressed in Eq. (6.1):

$$\text{Cross regulation} = \frac{\Delta v_{Oj}}{\Delta i_{Ok}} (\text{mV/mA}), j \neq k \quad (6.1)$$

An instantaneous load current variation in a certain output breaks the steady-state balanced energy delivery sequence of the SIMO converter. The stored energy in the inductor no longer



**Figure 6.5** Cross-regulation phenomenon in SIMO converters

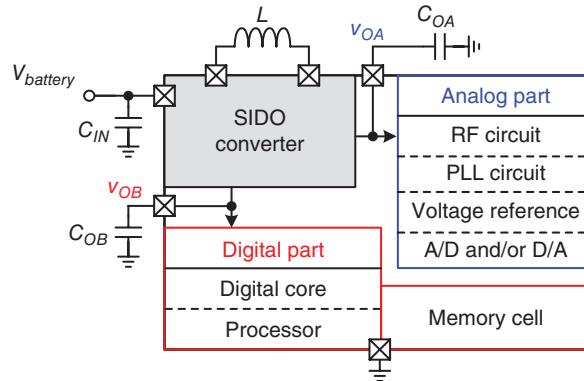
satisfies the instantaneous energy demand or release. Raising or pulling the inductor current level to its new balanced level within a short period is impossible because of limited bandwidth. Therefore, voltage variations occur at all outputs and cause cross regulation at victim outputs. Although the voltage variation can be recovered through the feedback loop of each output, the settling time becomes longer than that in the single-output buck converter because the chain reaction among all the outputs prolongs the recovery time. The design challenge in SIMO converters is to minimize cross regulation and enhance supply quality in the PMU.

## 6.2 Applications of SIMO Converters

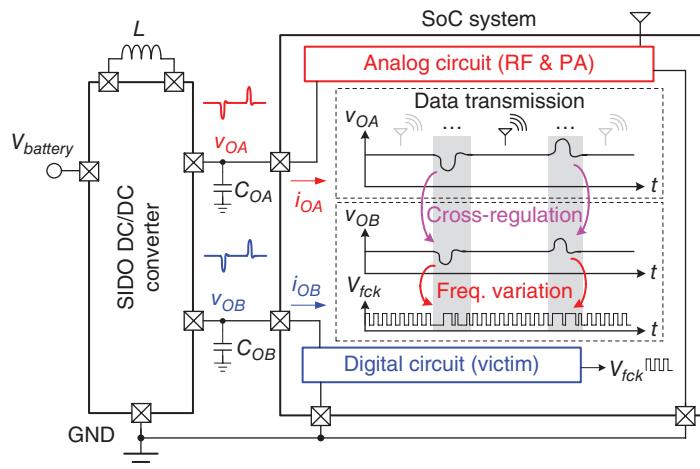
SIMO converters are widely used to minimize the size of PMUs in different applications. These applications can be classified into Soc and portable electronic systems. Soc integrates the whole system in a single chip to achieve high integrations. Advanced processes are usually adopted, such as the 65 nm or 28 nm CMOS process. Portable electronic systems, for instance tablet applications, require a large driving capability and constitute the whole system in a PCB board.

### 6.2.1 System-on-Chip

If the sub-modules in a Soc can simply be classified into analog and digital circuits, then the simplified single-inductor dual-output (SIDO) converter can provide suitable and independent supply voltages to these sub-modules. However, if the demanded supply voltage range is wide, then the SIMO converter may be more suitable than the SIDO converter. Similarly, the reduction of one inductor is area efficient, and the PCB area is effectively reduced because a conventional PMU requires more than two off-chip inductors to generate dual switching regulator (SWR) output voltages [5–7]. Low output voltage ripple, minimized cross regulation, and high power-conversion efficiency are essential design issues for one SIDO converter. Figure 6.6 shows the SIDO step-down converter in the Soc integration. The embedded power switches



**Figure 6.6** Simple illustration of the SIDO step-down converter in the SoC integration, which can provide distinct analog and digital power supplies to the analog and digital parts, respectively



**Figure 6.7** Detailed description of the transient cross-regulation effect in the SIDO converter and the performance deterioration in SoC applications

in the SIDO converter can deliver energy from  $V_{battery}$  to both off-chip capacitors  $C_{OA}$  and  $C_{OB}$  through an off-chip inductor. Therefore, the SIDO converter generates two output voltages,  $v_{OA}$  and  $v_{OB}$ , to supply the analog and digital parts, respectively. In particular, the PMU implemented by the SIDO converter in the Soc system can be properly guaranteed. However, several design challenges in the SIDO or SIMO converters should be prudently considered to prevent the deterioration of the Soc performance. The well-known design challenge is the reduction of cross regulation. When any one of the outputs undergoes a sudden loading current change, cross regulation occurs at the rest of the outputs because the accumulated inductor current occurs in the single off-chip inductor.

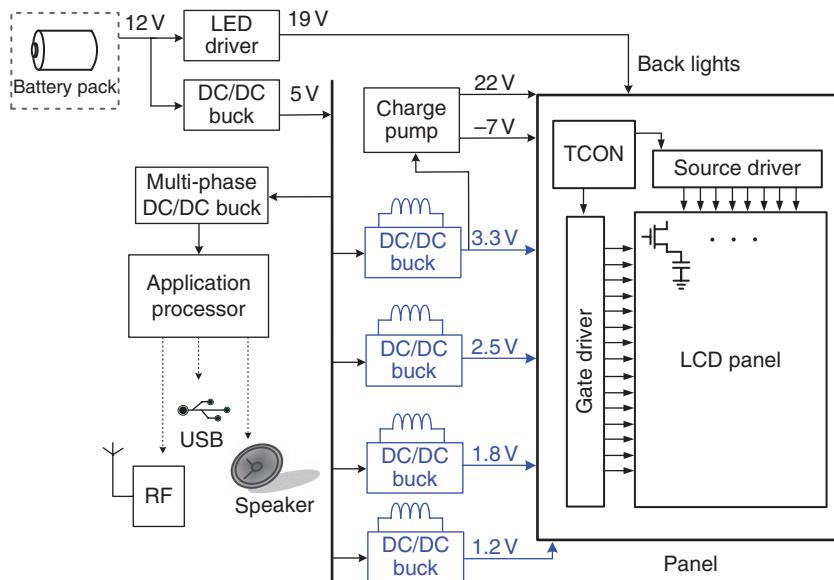
The transient cross regulation in the SIDO converter affects the PMU and the performance of the powered circuits in Soc applications. Figure 6.7 shows the transient cross regulation effect

of the step-down SIDO converter in Soc applications. The analog supply voltage source  $v_{OA}$  powers the RF and PA circuits, whereas the digital supply voltage source  $v_{OB}$  supplies the digital circuits. During the data transmission period, a large power requirement causes a sudden loading current increase at  $i_{OA}$ , thereby resulting in an expected voltage drop at  $v_{OA}$ . Simultaneously,  $v_{OB}$  is also affected by the voltage variation even under constant loading condition. The reason is that only one inductor is disturbed and used to deliver energy to the loading change at  $i_{OA}$ . The unexpected sudden voltage variation at  $v_{OB}$  degrades the performance of the digital circuits in Soc. Transient cross regulation varies the frequency of the signal  $V_{fck}$  and even induces abnormal operation in the system processor or other digital circuits. Therefore, how to minimize cross regulation in the SIDO converter becomes a necessary research topic.

### 6.2.2 Portable Electronics Systems

With the development of commercial portable electronics, small volume, light weight, and long usage time have become urgent requirements for consumers. The PMU has a pivotal role in portable electronics because the sub-circuits of different function blocks all require a high-quality voltage supply to ensure their performance. A low-cost PMU with a small PCB area is desirable to minimize the cost of portable electronics [34, 37].

The typical architecture of a commercial tablet is illustrated in Figure 6.8 [4, 8, 9]. Except for the LED driver, which supplies the backlights and a pair of positive/negative supply voltages for the gate driver, the panel requires several supply voltages with different levels, which are implemented by several DC/DC buck converters in commercial tablets. Here, four DC/DC buck converter chips with four inductors form the power solutions of this panel, which requires



**Figure 6.8** Typical architecture of commercial tablet and its power management unit

four different output voltages ranging from 1.2 to 3.3 V. The timing control unit (TCON) requires three supply voltages of 3.3, 1.8, and 1.2 V, while the gate driver and source driver demand voltages of 2.5 and 1.8 V, respectively. Using four individual buck converters, the performance requirements of each circuit block can easily be satisfied by separately designed converters.

However, the disadvantage of adopting four individual DC/DC buck converters is the large PCB area occupation. Multiple inductors dramatically increase the cost as well. The main concern here is how to design a PMU such that a small volume, light weight, and long usage time are achieved and no flicker effect occurs on the display in commercial tablets.

## 6.3 Design Guidelines of SIMO Converters

### 6.3.1 Energy Delivery Paths

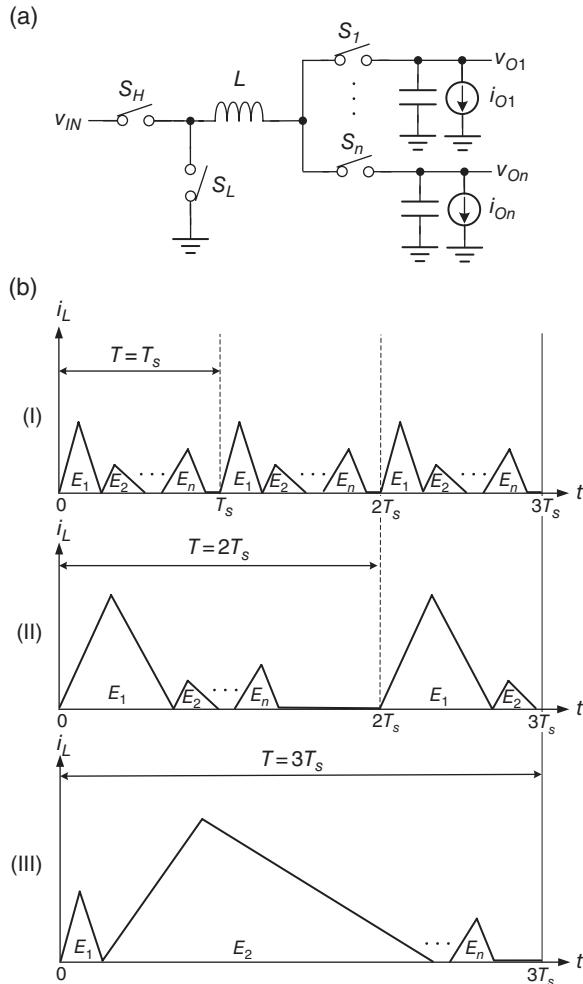
Energy delivery arrangements at the power stage are highly related to the performance of SIMO converters, especially in consideration of cross regulation. Thus, energy delivery schemes need to be considered carefully in order to guarantee adequate energy supply for multiple outputs, so as to minimize cross regulation. Additionally, the DC level of the inductor current has to be sufficient to meet the total loading conditions of all outputs. Some prior representative designs for SIMO converters are discussed and compared as follows.

#### 6.3.1.1 Constant-Charge Auto-Hopping (CCAH)

A simple method of minimizing cross regulation in SIMO converters is to separate the energy delivery of each output using zero inductor current. Therefore, the DCM control method can ensure the return of the inductor current to zero at the end of each PWM switching cycle. Cross regulation can effectively be reduced, but the other converter performances are sacrificed because of the limited DCM bandwidth.

Based on the DCM operation, CCAH aims to minimize cross regulation with unbalanced loads at  $v_{O1}-v_{On}$  [10]. Figure 6.9 shows the topology and operating waveforms. Figure (b) shows that in case I the energies requested by each output, which are indicated by  $E_1-E_n$ , respectively, are close to one another. The energy stored in the inductor  $L$  is sequentially allocated to  $v_{O1}-v_{On}$ . At  $t = 0$ , which is the start of a switching cycle, energy  $S_1$  is on and  $S_2-S_n$  are off to transfer energy to  $v_{O1}$ . Until the inductor current reaches zero, which indicates that the energy transferred to  $v_{O1}$  is sufficient,  $S_2$  is on and  $S_1$  and  $S_3-S_n$  are off to transfer energy to  $v_{O2}$ . When all the outputs obtain sufficient energy, all the switches  $S_H$ ,  $S_L$ , and  $S_1-S_n$  are turned off with zero inductor current. The energy allocation resumes at  $t = T_s$ . With DCM control, the transference of energy is ordered with the switching period  $T = T_s$ . The zero current region, which exists inherently in DCM control, can act as a buffer region to address energy variations during the transient and minimize cross regulation.

When an unbalanced load occurs (i.e., large load current difference between outputs), CCAH adjusts the switching period to  $n$  times  $T_s$  based on load condition  $T = kT_s$ , where  $k$  is an integer. Using the constant charge concept, the average energy transferred to each output remains constant regardless of switching frequency. In case II, when the energy requested by  $v_{O1}$  is considerably large, the time of  $E_1$  is significantly extended to obtain enormous energy. This process delays the energy attainment of the other outputs; thus, the energy allocation sequence cannot



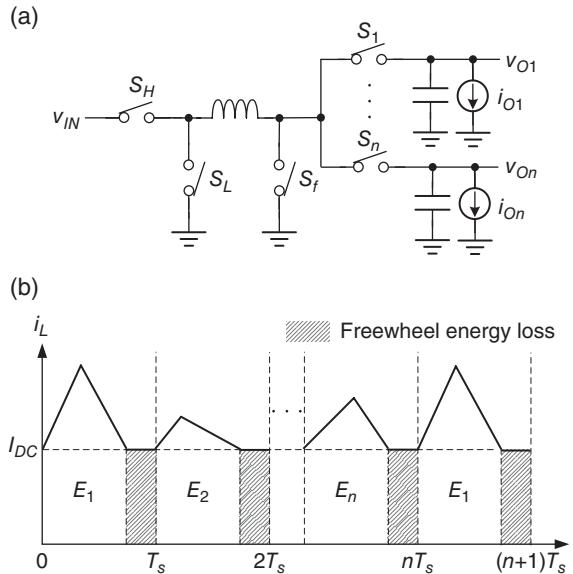
**Figure 6.9** Constant-charge auto-hopping: (a) topology; (b) operating waveforms

be achieved in a switching frequency. Therefore, CCAH extends the switching frequency to  $2T_s$  in case II. Case III shows that CCAH also extends the switching frequency to  $3T_s$  when  $E_2$  is considerably large.

Even CCAH can adapt to a wide range of loads and unbalanced loads, thereby delaying the energy attainment results in cross regulation. The switching frequency decreases with an increase in load current. Obvious disadvantages are large switching power loss at light loads and large ripple at heavy loads.

### 6.3.1.2 Pseudo-Continuous-Conduction Mode (PCCM)

The PCCM operation in [11] forces the inductor current back to the predefined DC level  $I_{DC}$  at the end of each PWM switching cycle. A non-zero inductor current can have advantages, including improved driving capability, lower output voltage ripples than that of the DCM, and higher bandwidth if compensated by Type II compensator.



**Figure 6.10** Pseudo-continuous conduction mode: (a) topology; (b) operating waveforms

Figure 6.10(a) shows a brief illustration of the classic PCCM control method in SIMO DC/DC buck converters. Except for the switches  $S_H$ ,  $S_L$ , and  $S_1-S_n$ , which are required in the basic topologies of SIMO converters in Figure 6.4, a freewheel switch  $S_f$  in Figure 6.10(a) is additionally adopted to achieve PCCM operation. The operating waveforms of the inductor current are depicted in Figure 6.10(b). In the first switching cycle (from 0 to  $T_s$ ), energy  $E_1$  is allocated to  $v_{O1}$  through  $(S_H, S_1)$  and  $(S_L, S_1)$  for inductor current charging and discharging, respectively. When the inductor current returns to  $I_{DC}$ ,  $S_L$  and  $S_f$  form the freewheel path until the switching cycle ends, and a constant inductor current level can be maintained by the shorted inductor because of the freewheel switch. Next,  $v_{O2}-v_{On}$  obtain energies  $E_2-E_n$  in the subsequent switching cycles in sequence. After  $n$  switching cycles, energy is allocated to  $v_{O1}$  again.

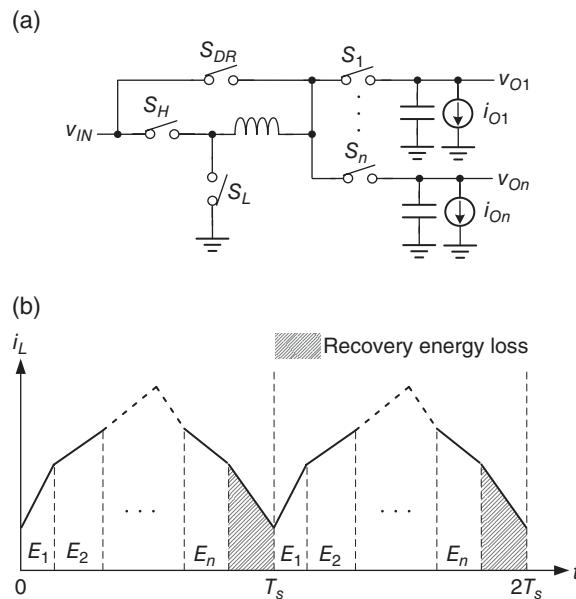
The insertion of a freewheel period to separate each output can be viewed as an energy buffer. Once the load current at one of the  $n$  outputs varies, the extension or compression of the freewheel period can achieve the voltage regulation of the load-varied output without affecting the other outputs. Therefore, cross regulation can be eliminated if a sufficient freewheel period can be maintained. In addition, the insertion of a freewheel period can simplify the compensation network. The system order is reduced from two (in voltage-mode control) to one that is similar to that of the DCM operation because the inductor current is reset to a predefined DC level in each switching period. The compensation for the PCCM operation becomes simpler. A Type II or PI compensator can be used to increase system stability.

Unfortunately, some inherent disadvantages that exist in PCCM are not suitable for battery-powered applications. The first crucial and obvious disadvantage is the high conduction power loss during the freewheel period. To ensure regulation,  $I_{DC}$  is always higher than the total loading current of all the outputs because no energy is transferred to the outputs in freewheel periods. During freewheel periods, the multiplication of the square of a high-value  $I_{DC}$  and the turn-on resistances of  $S_L$  and  $S_f$  causes large conduction loss and greatly degrades power

efficiency. Although a large freewheeling power switch can alleviate conduction power loss, a large silicon area occupation drastically increases the cost. For heavy load current endurance and low on-resistance, an unlimited increase in the area of  $S_f$  is impossible. Moreover, the design of the energy buffer region becomes more complicated in the PCCM if an adaptive and adequate  $I_{DC}$  is dynamically adjusted according to load conditions. If  $I_{DC}$  is too low, a large voltage ripple and unregulated problems may occur. If  $I_{DC}$  is too high, a large conduction power loss deteriorates the power conversion efficiency. The second fatal disadvantage is the large output voltage ripple. The output voltage ripple characteristic of the PCCM is similar to that of DCM because the peak inductor current is determined by the loading current. In particular, the output voltage ripple increases drastically at heavy loads. The efficiency deterioration in the PCCM makes it unsuitable in tablets or battery-powered applications.

### 6.3.1.3 Adaptive Energy Recovery Control (AERC)

To simultaneously achieve low cross regulation and suppress freewheel power loss, the AERC technique is proposed in [12]. Instead of freewheel duration, an energy recovery duration is constructed in the AERC technique. The AERC creates an energy recovery duration, which is the feedback controlled by the load-dependent duty. This recovery duration is responsible for decoupling the sub-channels and behaves similarly to a buffer region in the transient condition. As illustrated in Figure 6.11(a), the switch  $S_{DR}$  is introduced to form an energy recovery path. The operating waveforms are illustrated in Figure 6.11(b). At the beginning of a switching cycle, energy is allocated to each output in sequence. After all the outputs obtain adequate energy, the energy recovery duration is activated in the remaining switching cycle. The



**Figure 6.11** Adaptive energy recovery control: (a) topology; (b) operating waveforms

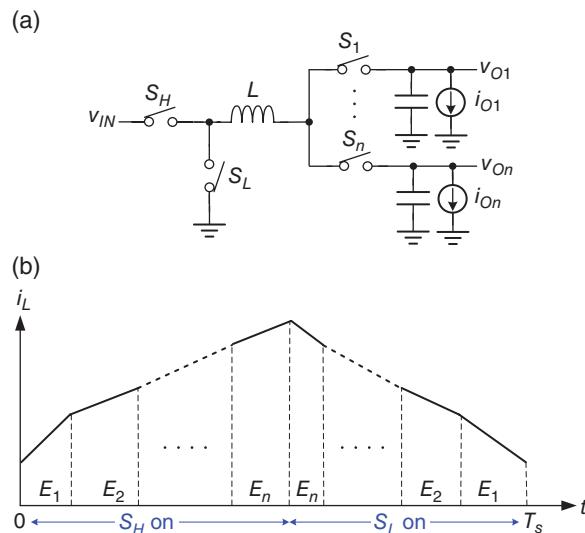
inductor current flows through  $S_L$ ,  $L$ , and  $S_{DR}$  back to the input source for energy recovery. In other words, sufficient energy stored in the inductor can face any sudden load changes from all the outputs.

Both the energy recovery duration in AERC and the freewheel duration in PCCM act as energy buffer regions to minimize cross regulation. The decision of the DC inductor level in AERC is not required, in contrast to the PCCM technique. Under different loading conditions, the energy recovery duration is automatically determined once the energy allocations in all the outputs are complete. Although energy can be recovered back to the input source for energy reuse, the turn-on resistance of  $S_L$  and  $S_{DR}$  still causes large conduction power loss. Thus, the problem of deteriorated power-conversion efficiency still cannot be solved by such an active energy recovery technique. In other words, the AERC technique can ensure controller stability and reduce cross regulation at the cost of power-conversion efficiency.

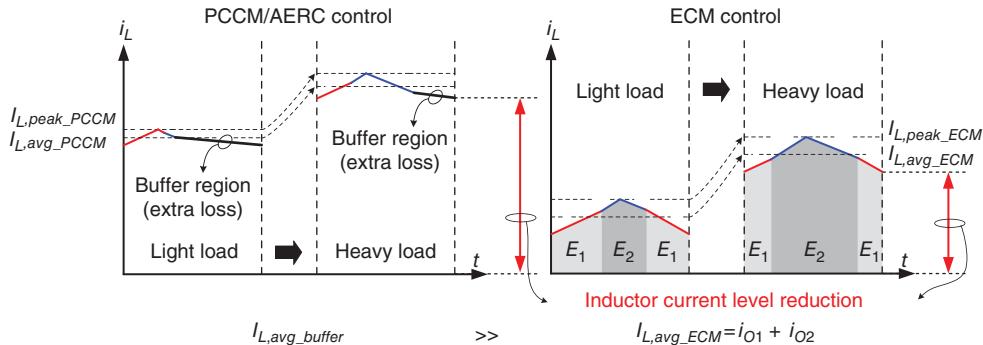
#### 6.3.1.4 Energy-Conservation Mode (ECM) Control

From the above discussions, inserting an energy buffer into the energy control sequence can minimize cross regulation at the cost of power efficiency. However, high efficiency for long usage time in portable and wearable electronics is especially important. The ECM control removes the buffer region and rearranges the energy paths according to all the output loading conditions. Thus, high efficiency and low cross regulation can be achieved concurrently because the freewheel stage is deleted [13, 14].

Figure 6.12(a) illustrates the topology of the ECM-controlled SIMO converter, which does not include extra switches in the basic SIMO converter shown in Figure 6.4. As mentioned earlier, this topology contains  $2n$  energy paths, which include  $n$  inductor charging paths



**Figure 6.12** ECM control: (a) topology; (b) operating waveforms



**Figure 6.13** Comparison of the PCCM/AERC and ECM controls in a two-output DC/DC converter

through the high-side switch  $S_H$ , and  $n$  inductor discharging paths through the low-side switch  $S_L$ . By combining these paths with all positive and negative slopes in one switching cycle, the inductor current waveform of ECM control is created, as illustrated in Figure 6.12(b). When  $S_H$  is on and  $S_L$  is off, the inductor current is charged, and the energy is allocated from the first to the last output in sequence. When  $S_H$  is off and  $S_L$  is on, the inductor current is discharged, and the energy is allocated from the last to the first output in sequence. From another point of view, the ECM control method uses the superposition of  $n$  inductor currents in different current levels. The energy levels  $E_1-E_n$  are superposed from the bottom to the top layer to construct the inductor current waveform.

Taking a two-output DC/DC converter, that is, a SIDO converter as an example, Figure 6.13 clearly compares the energy loss in PCCM/AERC with that in ECM control. In PCCM or AERC control, the buffer region not only causes extra loss but also largely increases the inductor current level. The increase in current level results in a large conduction power loss in all the power switches of the SIMO converters and further degrades power efficiency. By contrast, ECM control simultaneously removes the buffer region and reduces the inductor current level. Obviously, the average inductor current level in PCCM/AERC,  $I_{L,avg\_buffer}$ , is much higher than that in ECM control,  $I_{L,avg\_ECM}$ . The advantage of ECM control is that  $I_{L,avg\_ECM}$  is equal to the total load current. In other words, increasing the inductor current is not necessary, and conduction power loss can be reduced.

### 6.3.1.5 Buck and Boost SIMO Converter

Figure 6.14 shows the structure of the SIDO converter, which achieves dual buck and boost outputs with one single inductor utilization. In order to minimize the number of power switches to obtain silicon cost saving, the energy delivery paths for dual outputs must be arranged carefully. There are three main power switches and one freewheel switch in the power stage. Both of the output conditions can be fed back to the controller by the EAs. The full-range current-sensing circuit is used to derive the complete inductor current information to achieve duty cycle modulation with the charge-reservation methodology. The control logic can generate the control signals for the power switches. This technique implements similar current-mode control for