

Operational Amplifiers-Based Compensators

The operational amplifier, commonly abbreviated as *op amp*, represents the basis of the closed loop system (see [1, 2]). Its function, in a feedback system, is to amplify the error detected between a fixed and stable reference level (e.g., a current or a voltage) and the monitored state variable (e.g., an output voltage or a current). Besides its monitoring purposes, the op amp lends itself very well to building the compensation stage. Its role is to shape the loop gain transfer function $T(s)$ of the system we need to stabilize by compensating the plant deficiencies such as lack of gain, phase lag, and resonating peaks. By wiring passive components such as capacitors and resistors across the op amp, we will build a transfer function $G(s)$, which, once inserted in the return path, will adjust the loop gain crossover frequency to the targeted value and provide the necessary phase and gain margins [3]. In this section, we will cover the previously introduced three basic types, 1, 2, and 3, plus some extra configurations where an isolated feedback is necessary—in offline power converters, for instance. Figure 5.1 shows the typical nonisolated configuration on the left, whereas the isolated version appears on the right side.

Nonisolated structures are often found in so-called point of load (POL) regulators where a voltage is locally created by decreasing or increasing an available dc rail (12 V to 5 V, for instance). As source and load share a common ground, the converter is said to be nonisolated. If you now plan to power a DVD player or simply a cell phone from a mains outlet, unless you want to reiterate Luigi Galvani experiments and risk a lethal electric shock, it is strongly advised to isolate the output ground (touched by the end user) from the live wire. The high-frequency power transformer performs this isolation task by having primary and secondary sides physically separated. However, the output monitoring data must be returned to the control section—the pulse width modulator—usually placed on the nonisolated side. As shown in the right side of Figure 5.1, an optocoupler is used in the wide majority of cases to return this output voltage error information. Other means to convey the information exist, such as high-frequency low-power transformers or even piezoelectric devices. They will not be described here. As the optocoupler is one of the most important elements in an isolated power supply, an appendix is entirely dedicated to this device in the end of this chapter.

Let's start with the simplest compensating structure, type 1.

5.1 Type 1: An Origin Pole

Type 1 is the typical compensator found in circuits where no phase boost at the selected crossover frequency is necessary. Also called an integrator, it includes a single

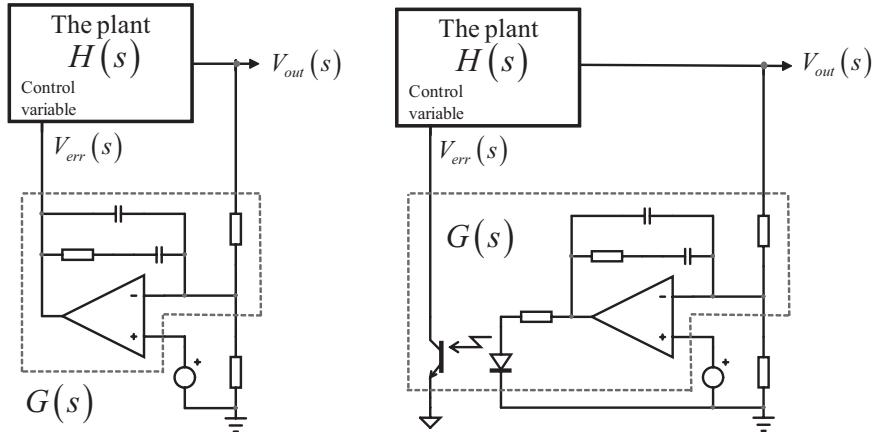


Figure 5.1 The basic op amp configuration and its isolated counterpart.

pole at the origin and offers a permanent phase lag of 270° or a phase lead of 90° . The simplest form of the compensator appears in Figure 5.2.

Throughout the text, the transfer function of the op amp-based circuit $G(s)$ is defined by

$$G(s) = \frac{V_{err}(s)}{V_{out}(s)} \quad (5.1)$$

In this type 1 configuration, you derive G by dividing the capacitor impedance by the upper resistor R_1 :

$$G(s) = \frac{V_{err}(s)}{V_{out}(s)} = -\frac{Z_f}{Z_i} = -\frac{\frac{1}{sC_1}}{R_1} = -\frac{1}{sC_1R_1} \quad (5.2)$$

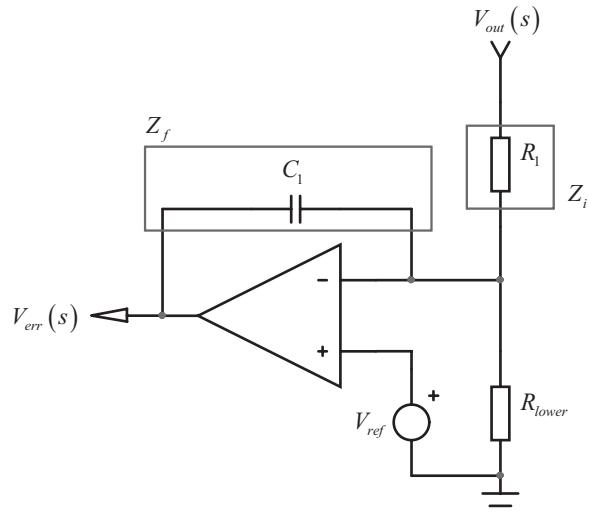


Figure 5.2 A capacitor C_1 connected across the output and the inverting input of the op amp creates an origin pole together with the upper resistor R_1 .

In which we unveil the so-called 0-dB crossover pole angular frequency:

$$\omega_{po} = \frac{1}{R_1 C_1} \quad (5.3)$$

As we explained before, (5.2) features an origin pole for $s = 0$. However, the time constant of (5.3) can be seen as a gain, pushing up or down the -1 slope. When the frequency reaches the value defined by (5.3), the gain of the type 1 compensator is 1 or 0 dB—hence its name, the 0-dB crossover pole.

By reworking (5.2) with (5.3), we obtain the following form:

$$G(s) = -\frac{\frac{1}{s}}{\frac{\omega_{po}}{\omega}} \quad (5.4)$$

The magnitude of (5.4) is given by

$$|G(j\omega)| = \left| j \frac{\omega_{po}}{\omega} \right| = \sqrt{\left(\frac{\omega_{po}}{\omega} \right)^2} = \frac{\omega_{po}}{\omega} \quad (5.5)$$

Whereas the argument of this simple integrator is obtained via

$$\arg G(j\omega) = \arg \left(0 + j \frac{\omega_o}{\omega} \right) = \tan^{-1}(\infty) = \frac{\pi}{2} \quad (5.6)$$

also equal to $\frac{\pi}{2} - 2\pi = -\frac{3\pi}{2}$ or -270° .

According to (5.5), to adjust the gain or the attenuation we want at a certain frequency, our crossover choice, for instance, we just need to calculate where to position the 0-dB crossover pole f_{po} .

5.1.1 A Design Example

Let us assume we want to compensate a gain deficiency G_{fc} of -20 dB at a 1-kHz frequency. To do that, we will define the position at which the 0-dB crossover pole must be located so that the magnitude of $G(s)$ is exactly 20 dB when the frequency reaches 1 kHz. A 20-dB gain translates to

$$G = 10^{\frac{-G_{fc}}{20}} = 10 \quad (5.7)$$

According to (5.5), to attenuate the input signal by 20 dB at 1 kHz, we must place the 0-dB crossover pole at

$$f_{po} = f_c G = 10 f_c = 10 \text{ kHz} \quad (5.8)$$

Assuming the upper resistor R_1 is $10 \text{ k}\Omega$, then capacitor C_1 can be easily calculated according to (5.3):

$$C_1 = \frac{1}{2\pi R_1 f_{po}} = \frac{1}{6.28 \times 10k \times 10k} = 1.6 \text{ nF} \quad (5.9)$$

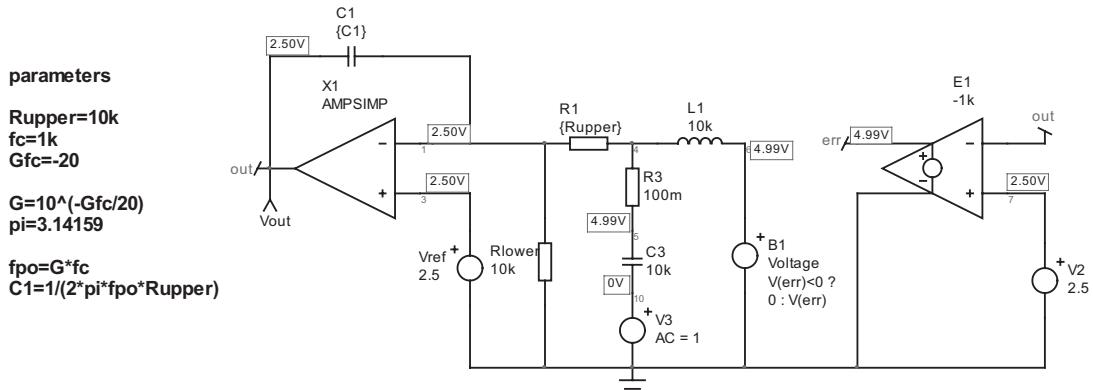


Figure 5.3 The automated simulation of the type 1 example.

The SPICE simulation of such a compensator appears in Figure 5.3.

As you can see in the schematic, the operating points have been reflected and show that the op amp output is well biased, away from its lower or upper stops. This situation is obtained thanks to the voltage-controlled voltage source E_1 , which automatically biases the type 1 network (here a 5-V output) to make the op amp work within its linear region ($V_{err} = 2.5$ V). In case you change the op amp and replace this model by another one, or adopt a different upper resistor value, the bias point will automatically adjust to the value imposed by V_2 . No further tweak is necessary. The L_1/C_3 network (also labeled LoL/CoL in other fixtures) makes this auto-adjustment possible: when SPICE calculates the dc point—the circuit bias point—it shorts the inductors and opens

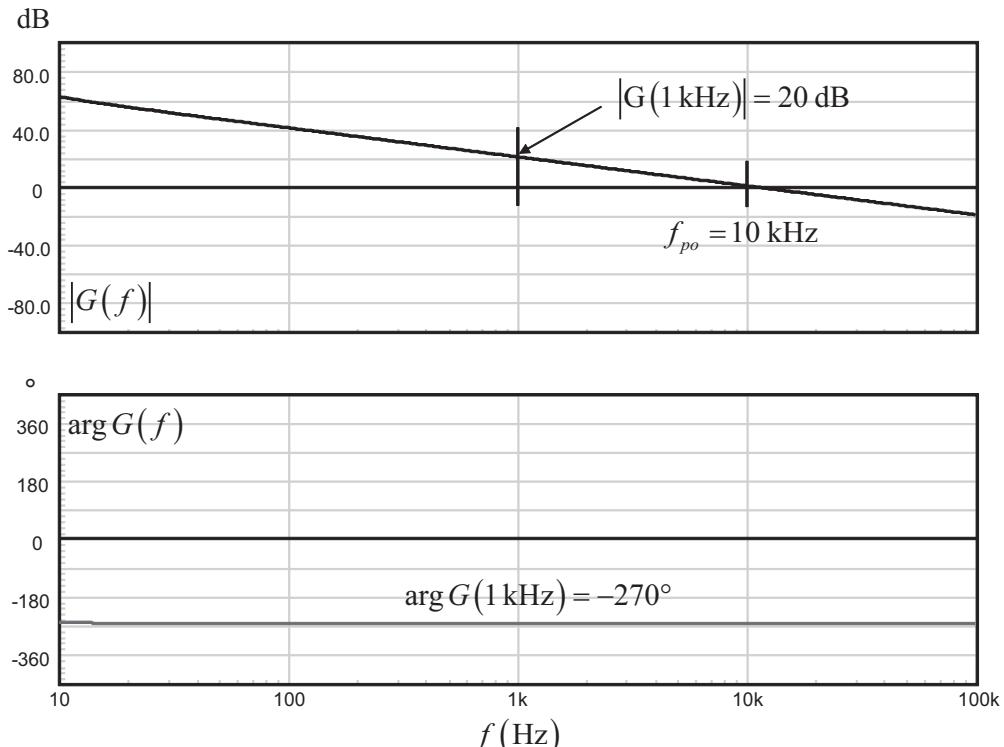


Figure 5.4 the resulting plot shows a +20-dB gain at 1 kHz, as expected.

all the capacitors. As L_1 is a short circuit and C_3 is off, the loop is closed and E_1 adjusts to have the *out* node equal to 2.5 V. Once the ac simulation starts, L_1 being of high value, it blocks the modulation while it easily passes through C_3 . This way, any change in the circuit leads to a new bias point calculation every time you start the simulation.

The simulation results appear in Figure 5.4 and confirm the right gain at 1 kHz: +20 dB. The phase is permanently lagging at 270°. Please note that most simulators are displaying the phase with a 2π modulo:

$$\theta = \frac{\pi}{2} \pm k2\pi \quad (5.10)$$

If $k = 0$, then the displayed angle will be $\pi/2$ or 90°. To ease the representation, we purposely added -360° to the phase curve in order to offer a more common value of -270° .

Please see Appendix C in Chapter 4 for explanations on phase display in simulators.

5.2 Type 2: An Origin Pole, plus a Pole/Zero Pair

Offering an origin pole, one zero, and one higher frequency pole, the type 2 compensator provides a phase boost up to 90°. Its electrical configuration appears in Figure 5.5. The transfer function is obtained by calculating the impedance offered by the network placed in the op amp feedback path, Z_f , and dividing it by the upper resistor, R_1 :

$$\frac{Z_f}{Z_i} = \frac{\left(\frac{1}{sC_1} + R_2 \right) \frac{1}{sC_2}}{\left(\frac{1}{sC_1} + R_2 \right) + \frac{1}{sC_2}} \quad (5.11)$$

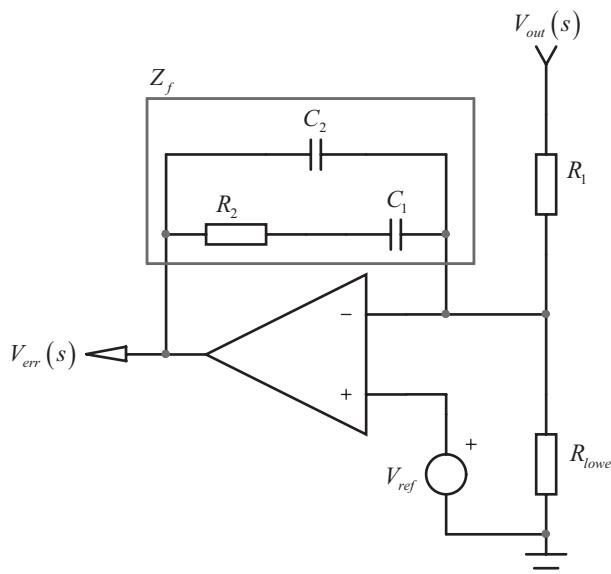


Figure 5.5 By adding an extra pole/zero pair to type 1, type 2 offers a possible phase boost up to 90°.

Developing and rearranging (5.11), we have

$$G(s) = -\frac{Z_f}{Z_i} = -\frac{1 + sR_2C_1}{sR_1(C_1 + C_2)\left(1 + sR_2\left[\frac{C_1C_2}{C_1 + C_2}\right]\right)} \quad (5.12)$$

From there, we can factor sR_2C_1 and have the equation fit a more common format:

$$G(s) = -\frac{R_2}{R_1} \frac{C_1}{C_1 + C_2} \frac{1 + 1/sR_2C_1}{\left(1 + sR_2\left[\frac{C_1C_2}{C_1 + C_2}\right]\right)} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.13)$$

where

$$G_0 = \frac{R_2}{R_1} \frac{C_1}{C_1 + C_2} \quad (5.14)$$

$$\omega_z = \frac{1}{R_2C_1} \quad (5.15)$$

$$\omega_p = \frac{1}{R_2 \frac{C_1C_2}{C_1 + C_2}} \quad (5.16)$$

In these definitions, ω_z and ω_p are known because of the phase boost we want for our converter (see Chapter 4 on compensation strategies). To adjust the cross-over point, that is to say provide the exact gain or attenuation at the selected cross-over frequency f_c , we need to extract R_2 from (5.13). Thanks to its right-side form, we can express the magnitude of (5.13) at the crossover frequency f_c involving the pole and zero, independently from the passive elements that fix them:

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_z}{f_c}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_p}\right)^2}} \quad (5.17)$$

By substituting C_1 and C_2 extracted from (5.15) and (5.16) into (5.17) and then solving for R_2 , we obtain the following value:

$$R_2 = \frac{R_1 f_p G}{f_p - f_z} \frac{\sqrt{\left(\frac{f_c}{f_p}\right)^2 + 1}}{\sqrt{\left(\frac{f_z}{f_c}\right)^2 + 1}} \quad (5.18)$$

where G represents the needed magnitude at the crossover frequency as defined by (5.7). The rest of the component values come out easily:

$$C_1 = \frac{1}{2\pi R_2 f_z} \quad (5.19)$$

$$C_2 = \frac{C_1}{2\pi f_p C_1 R_2 - 1} \quad (5.20)$$

A possibility exists to simplify these formulas. In a lot of practical cases, the capacitance value of C_2 is much smaller than that of C_1 . As a result, if we now consider $C_2 \ll C_1$, the overall transfer function simplifies to

$$G(s) \approx -\frac{R_2}{R_1} \frac{1/s R_2 C_1 + 1}{(1 + s R_2 C_2)} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.21)$$

Following the same path as before, we can extract the component values we are looking for:

$$G_0 = \frac{R_2}{R_1} \quad (5.22)$$

$$\omega_p = \frac{1}{R_2 C_2} \quad (5.23)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (5.24)$$

$$R_2 = R_1 G \quad (5.25)$$

$$C_2 = \frac{1}{2\pi f_p R_2} \quad (5.26)$$

$$C_1 = \frac{1}{2\pi R_2 f_z} \quad (5.27)$$

The argument of a type 2 configuration where an origin pole and a zero/pole pair cohabit is given by

$$\arg G(\omega) = \arg\left(-1 + j\frac{\omega_z}{\omega}\right) - \arg\left(1 + j\frac{\omega}{\omega_p}\right) \quad (5.28)$$

The numerator complex number lies in quadrant II; we need to add π to correct the angle returned by \tan^{-1} (see Appendix 4C for a refresher on complex numbers):

$$\arg G(f) = \pi - \tan^{-1}\left(\frac{f_z}{f}\right) - \tan^{-1}\left(\frac{f}{f_p}\right) \quad (5.29)$$

In dc, because of the origin pole and the op amp inversion, the phase lags by

$$\lim_{f \rightarrow 0} \arg G(f) = \pi - \tan^{-1}(\infty) - \tan^{-1}(0) = \pi - \frac{\pi}{2} = \frac{\pi}{2} \text{ or } -\frac{3\pi}{2} \quad (5.30)$$

As seen in Chapter 4, the phase boost at the crossover frequency f_c is $\arg G(f_c) - \frac{\pi}{2}$. Otherwise expressed, the phase boost of a type 2 compensator is

$$\text{boost} = \pi - \tan^{-1}\left(\frac{f_z}{f_c}\right) - \tan^{-1}\left(\frac{f}{f_p}\right) - \frac{\pi}{2} = \left[\frac{\pi}{2} - \tan^{-1}\left(\frac{f_z}{f_c}\right)\right] - \tan^{-1}\left(\frac{f_c}{f_p}\right) \quad (5.31)$$

The term $\frac{\pi}{2} - \tan^{-1}\left(\frac{f_z}{f_c}\right)$ is simply $\tan^{-1}\left(\frac{f_c}{f_z}\right)$ so

$$\text{boost} = \tan^{-1}\left(\frac{f_c}{f_z}\right) - \tan^{-1}\left(\frac{f_c}{f_p}\right) \quad (5.32)$$

5.2.1 A Design Example

Let's assume we need to provide a 15-dB gain at a selected 5-kHz frequency together with a phase boost of 50°. Where do we place our pole and zero pair? As we have detailed in the pole-zero section, the pole can be placed at the following location:

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 5k = 13.7 \text{ kHz} \quad (5.33)$$

As the phase peaks at the geometric mean between the pole and the zero, this latter is placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{(5k)^2}{13.7k} \approx 1.8 \text{ kHz} \quad (5.34)$$

Applying the design equations (5.18) through (5.20), we can calculate the component values we need, considering the upper resistor R_1 fixed to 10 kΩ in this example:

$$R_2 = \frac{R_1 f_p G}{f_p - f_z} \frac{\sqrt{\left(\frac{f_c}{f_p}\right)^2 + 1}}{\sqrt{\left(\frac{f_z}{f_c}\right)^2 + 1}} = 64.8 \text{ k}\Omega \quad (5.35)$$

$$C_1 = \frac{1}{2\pi R_2 f_z} = 1.3 \text{ nF} \quad (5.36)$$

$$C_2 = \frac{C_1}{2\pi f_p C_1 R_2 - 1} = 206 \text{ pF} \quad (5.37)$$

The SPICE simulation of the type 2 compensator appears in Figure 5.6 and makes use of the automated bias point adjustment previously described. The ac sweep results are given in Figure 5.7 and confirm our calculations.

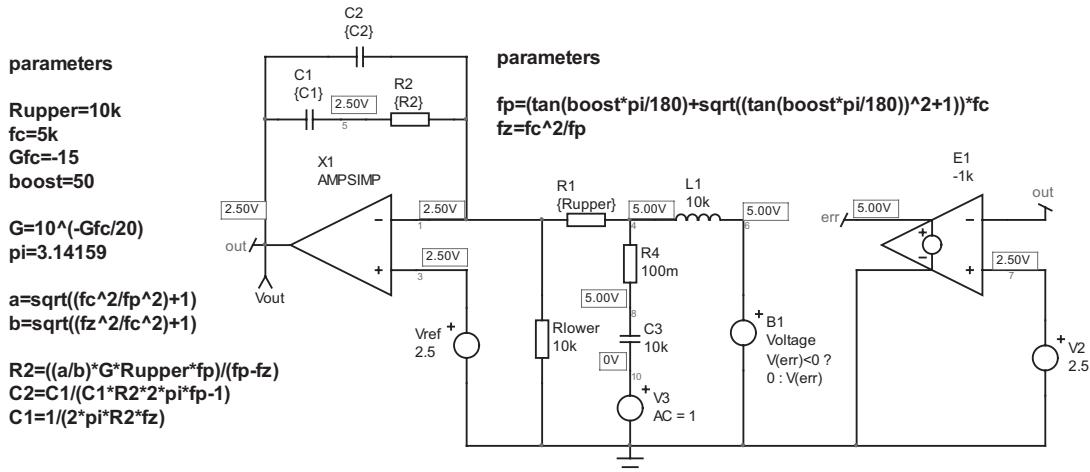


Figure 5.6 In this test fixture, the E_1 source automatically adjusts the bias point of the compensator to place the op amp output within its regulation range (2.5 V). Should you change the divider network, the bias point would automatically be recomputed.

In this particular example, as we deal with a rather high crossover frequency, the simplified formulas given by (5.25) through (5.27) would give almost similar results because C_2 is small compared to C_1 . In case the crossover frequency would be much lower, in the vicinity of a few tens of hertz as with a PFC, for instance, then you might need to use the full formulas to obtain the exact gain and phase boost you are looking for.

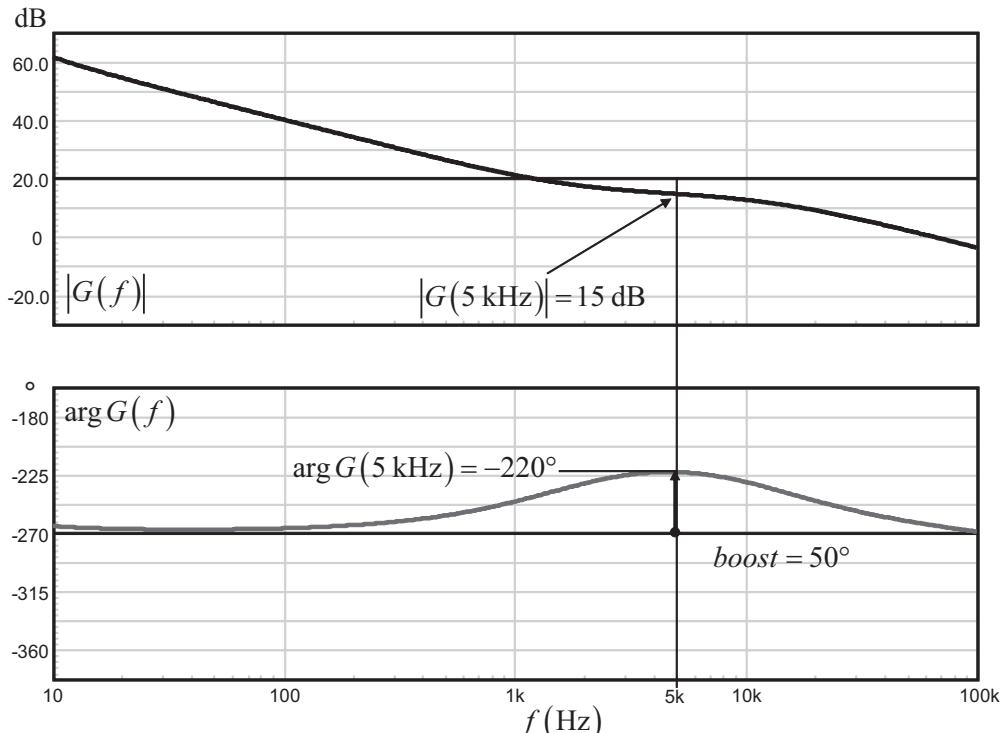


Figure 5.7 The Bode plot confirms the right 50° phase boost and the gain at the selected 5-kHz crossover frequency.

5.3 Type 2a: An Origin Pole plus a Zero

There are applications where the high-frequency pole on the op amp is not necessary. For instance, if you associate the op amp with an optocoupler, you might want to place the pole after the optocoupler to improve the noise immunity of the whole chain. Figure 5.8 shows you the adopted configuration in its simplest form. This is a PI compensator.

Following the previous design derivation method, we quickly obtain the transfer function:

$$G(s) = -\frac{R_2 + \frac{1}{sC_1}}{R_1} = -\frac{1 + sR_2C_1}{sR_1C_1} = -\frac{1 + s/\omega_z}{s/\omega_{po}} \quad (5.38)$$

We can factor s/ω_z and rearrange the equation:

$$G(s) = -\frac{s}{\omega_z} \frac{\omega_{po}}{s} \left(1 + \frac{\omega_z}{s} \right) = -G_0 \left(1 + \frac{\omega_z}{s} \right) \quad (5.39)$$

From which the zero, the 0-dB origin pole and the mid-band gain can be extracted:

$$\omega_z = \frac{1}{R_2 C_1} \quad (5.40)$$

$$\omega_{po} = \frac{1}{R_1 C_1} \quad (5.41)$$

$$G_0 = \frac{\omega_{po}}{\omega_z} = \frac{R_2}{R_1} \quad (5.42)$$

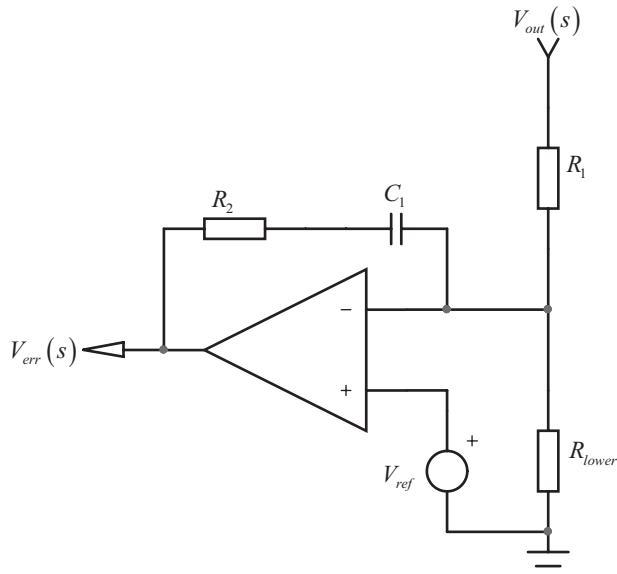


Figure 5.8 Type 2a does not implement the high-frequency pole.

As the frequency increases, C_1 becomes a short circuit and the gain reduces to a ratio of resistors as expressed by

$$\lim_{s \rightarrow \infty} |G(s)| = G_0 = \frac{R_2}{R_1} \quad (5.43)$$

The argument is calculated using (5.39). Because of the negative sign on G_0 (the inverting configuration), we are in quadrant II, and π must be added to the arctangent result:

$$\arg G(j\omega) = 180^\circ + \arg\left(1 - j \frac{\omega_z}{\omega}\right) = 180^\circ + \tan^{-1}\left(-\frac{\omega_z}{\omega}\right) = 180^\circ - \tan^{-1}\left(\frac{\omega_z}{\omega}\right) \quad (5.44)$$

When ω reaches infinity, the right term is 0, and we have the phase of a simple inverter. When displayed under the SPICE graphical viewer, it can show up as 180° or -180° , as both angles are similar.

5.3.1 A Design Example

Suppose we need to compensate a circuit whose gain excess at a 10-Hz crossover frequency is 20 dB. The needed phase boost to stabilize the device is 45° . How do we place our zero and the 0-dB crossover pole to meet these criteria? We know that in dc, the argument of the inverting type 2a is 90° . The phase boost is thus

$$\text{boost} = \arg G(j\omega_c) - 90^\circ \quad (5.45)$$

If we substitute (5.44) in the previous equation, we have

$$\text{boost} = 180^\circ - \tan^{-1}\left(\frac{\omega_z}{\omega_c}\right) - 90^\circ = 90^\circ - \tan^{-1}\left(\frac{\omega_z}{\omega_c}\right) \quad (5.46)$$

Solving for ω_z and converting to f_z , we have

$$f_z = f_c \tan\left(\frac{\pi}{2} - \text{boost}\right) = 10 \cdot \tan(90^\circ - 45^\circ) = 10 \text{ Hz} \quad (5.47)$$

We have the zero position, where do we place the 0-dB crossover pole now? From (5.38), we calculate the magnitude at the selected crossover frequency:

$$|G(f_c)| = \frac{\sqrt{1 + \left(\frac{f_c}{f_z}\right)^2}}{f_c} f_{po} \quad (5.48)$$

We will now place the 0-dB crossover pole to realize an attenuation G of -20 dB at 10 Hz. From (5.48), we have

$$f_{po} = \frac{G \cdot f_c}{\sqrt{1 + \left(\frac{f_z}{f_c}\right)^2}} = \frac{10^{\frac{-20}{20}} \times 10}{\sqrt{1 + \left(\frac{10}{10}\right)^2}} = \frac{1}{\sqrt{2}} \approx 0.7 \text{ Hz} \quad (5.49)$$

The simulation circuit appears in Figure 5.9.

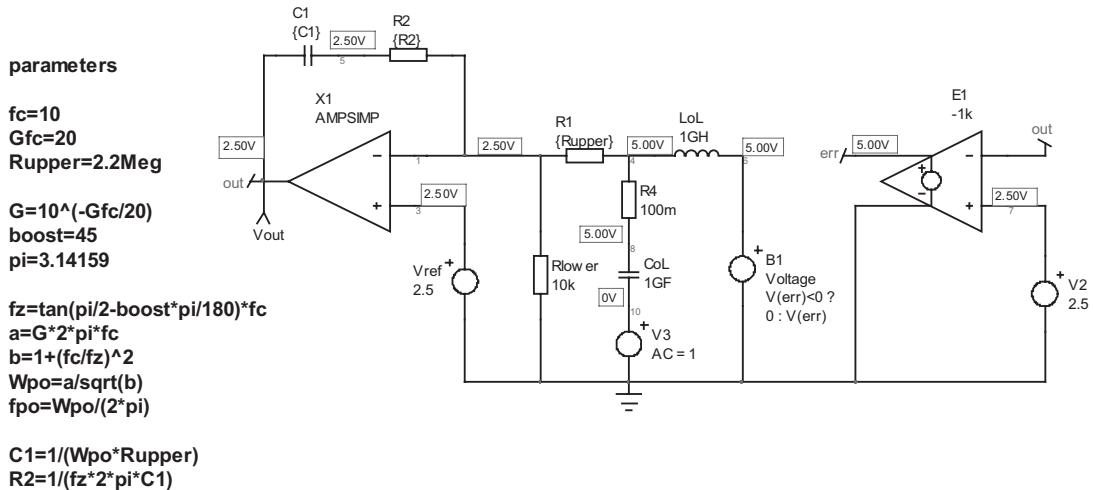


Figure 5.9 The automated simulation circuit for the type 2a compensator.

The ac simulation are given in Figure 5.10 and confirm the validity of our equations.

5.4 Type 2b: Some Static Gain plus a Pole

There are some applications where a simple proportional compensation combined with a gain rolloff is the adequate solution. In this situation, type 2b can be

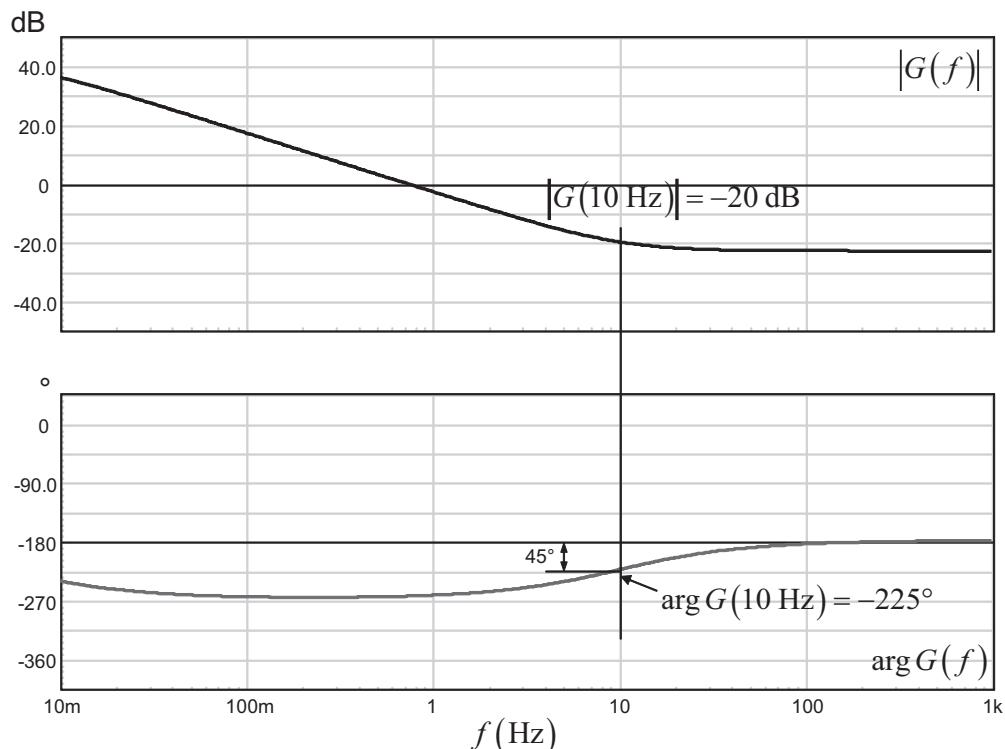


Figure 5.10 The simulations results confirm the 10-Hz zero and the phase lag up to 180°.

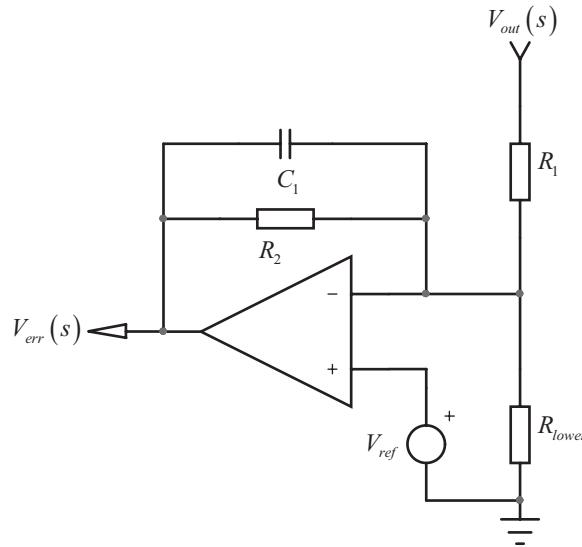


Figure 5.11 Type 2b inserts a pole together with some static gain.

envisioned. Its architecture appears in Figure 5.11. The transfer function equation is straightforward:

$$G(s) = -\frac{\frac{1}{sC_1}R_2}{\frac{1}{sC_1} + R_2} \frac{1}{R_1} = -\frac{R_2}{R_1} \frac{1}{1 + sR_2C_1} = -G_0 \frac{1}{1 + s/\omega_p} \quad (5.50)$$

with

$$G_0 = \frac{R_2}{R_1} \quad (5.51)$$

and

$$\omega_p = \frac{1}{R_2C_1} \quad (5.52)$$

At high-frequency, the gain goes to

$$\lim_{s \rightarrow \infty} |G(s)| = 0 \quad (5.53)$$

In dc, the gain reaches a plateau, also called the static gain:

$$\lim_{s \rightarrow 0} |G(s)| = G_0 \quad (5.54)$$

The argument of type 2b is derived as follows:

$$\arg G(j\omega) = \pi - \tan^{-1} \left(\frac{\omega}{\omega_p} \right) \quad (5.55)$$

At dc, when the capacitor is considered an open circuit, the argument is that of a simple inverter and is 180° or -180° . When the frequency increases toward infinity, the phase reaches

$$\lim_{s \rightarrow \infty} \arg G(s) = \pi - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) = \pi - \tan^{-1}(\infty) = \pi - \frac{\pi}{2} = \frac{\pi}{2} \text{ or } -270^\circ \quad (5.56)$$

5.4.1 A Design Example

Let's assume a 50-dB static gain is needed, followed by a pole installed at 10 kHz. R_1 is supposed to be $10 \text{ k}\Omega$. Using (5.54), we have

$$R_2 = R_1 10^{\frac{50}{20}} = 10k \times 316 \approx 3.2 \text{ M}\Omega \quad (5.57)$$

The capacitor is obtained using (5.52):

$$C_1 = \frac{1}{2\pi R_2 f_p} = \frac{1}{6.28 \times 3.2M \times 10k} = 4.7 \text{ pF} \quad (5.58)$$

The simulator has been fed with these calculated values and the commented results show up in Figure 5.12.

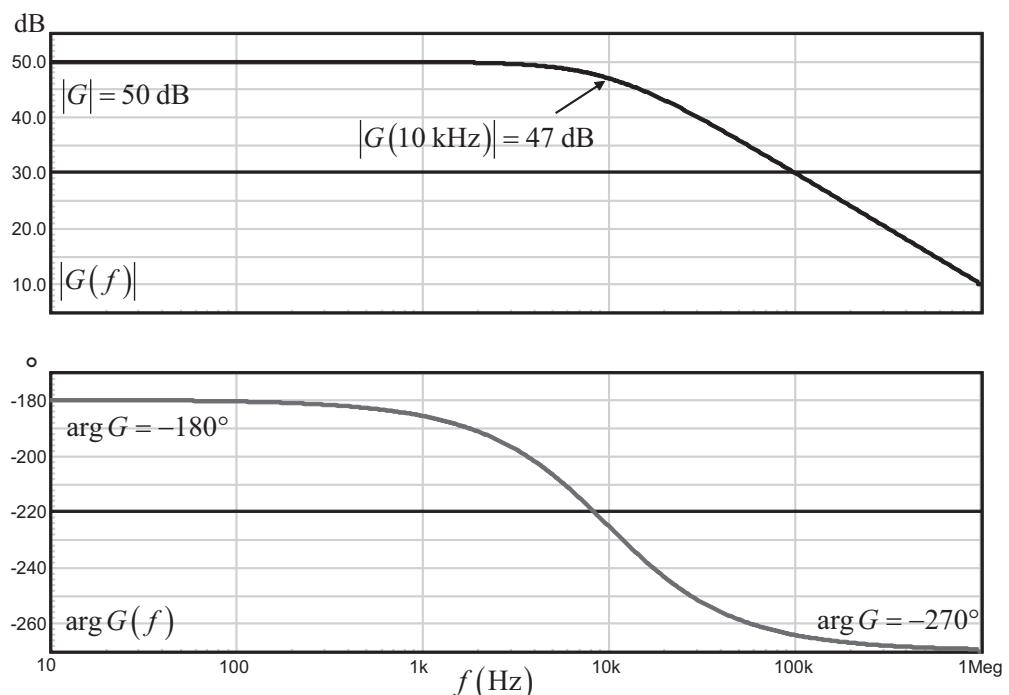


Figure 5.12 The phase starts from 180° down to 90° or from -180° down to -270° ; this is the type 2a argument over frequency.

5.5 Type 2: Isolation with an Optocoupler

In the majority of offline applications (e.g., ac-dc adapters), the secondary side information is carried back to the primary via an opto-isolator, also known as an optocoupler. This element plays an important role, and you must understand how it works to successfully stabilize a converter that uses one. The simplified representation of an opto-isolator appears in Figure 5.13. In a nutshell, the set of parameters needed to stabilize a loop are the following ones:

- *Current transfer ratio (CTR)*: this is the amount of current I_C flowing in the collector when the LED is forward biased by a current I_F . Its definition is simply

$$\text{CTR} = \frac{I_C}{I_F} \quad (5.59)$$

- C_{opto} : this is the equivalent parasitic capacitor seen across the collector and the emitter of the device. It actually sets the pole frequency f_{pole} inherent to the optocoupler when wired in either a common collector (R_{pulldown}) or common emitter (R_{pullup}) configuration:

$$f_{\text{pole}} = \frac{1}{2\pi C_{\text{opto}} R_{\text{pullup}}} \quad (5.60)$$

- You cannot get rid of that pole but you can shift it by adding an extra capacitor across the optocoupler collector-emitter terminals.
- V_f : this is the LED forward voltage. It usually equals roughly 1 V and stays rather constant given the low forward currents in play.
- $V_{CE,sat}$: this is the minimum voltage appearing across the collector-emitter junction when the LED is forward biased. It obviously depends on the collector current and the LED biasing level. In general, this saturation voltage is in the vicinity of 300 mV.

The equivalent simplified schematic we have used appears next and shows the presence of the parasitic capacitor, which, when combined with the pull-up resistor,

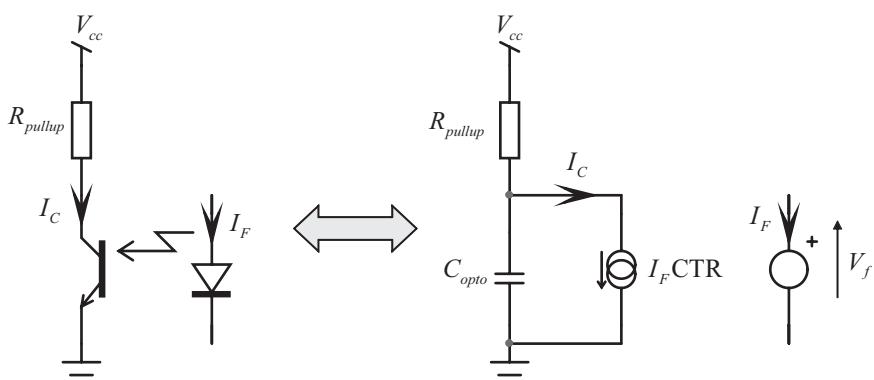


Figure 5.13 The simplified ac model of the optocoupler that we will use in the following lines.

introduces a pole. Any capacitor connected from the collector to ground will be supplemental to the parasitic capacitor already present. This is something to keep in mind for future calculations.

There are basically three possible ways to connect an optocoupler to the op amp output. They appear in Figure 5.14. In the first option, noted (a), an op amp directly drives the optocoupler LED with a simple resistor in series with the op amp output.

The second option (b) shows the optocoupler LED wired as a pull-up load. Please note that in this configuration, the LED current not only depends on the op amp output but also on the observed voltage, V_{out} in this case. Finally, solution (c) is a variation of (b) in the sense that the LED current now solely depends on the op amp output current. We will explore these configurations in several design examples.

In solution (a), the op amp output is made of $V_{out}(s)G(s)$ alone, and the optocoupler chain provides an additional gain block, featuring a pole brought by C_{opto} combined with the pull-up resistor. A type 2 compensator already features one pole. If we directly cascade another stage also exhibiting a pole within our frequency zone of interest, we will surely degrade the op amp transfer function and, in particular, the phase boost we are looking for. For that reason, why not getting rid of the pole in the op amp chain (like with a type 2a) and only keep the pole brought by the optocoupler? This would ensure the inclusion of the optocoupler in the calculation chain, thus accounting for its effects (on the pole but also on the gain with its CTR). We know that the optocoupler pole can be shifted by adding an extra capacitor from collector to ground, a capacitor that will also help improve

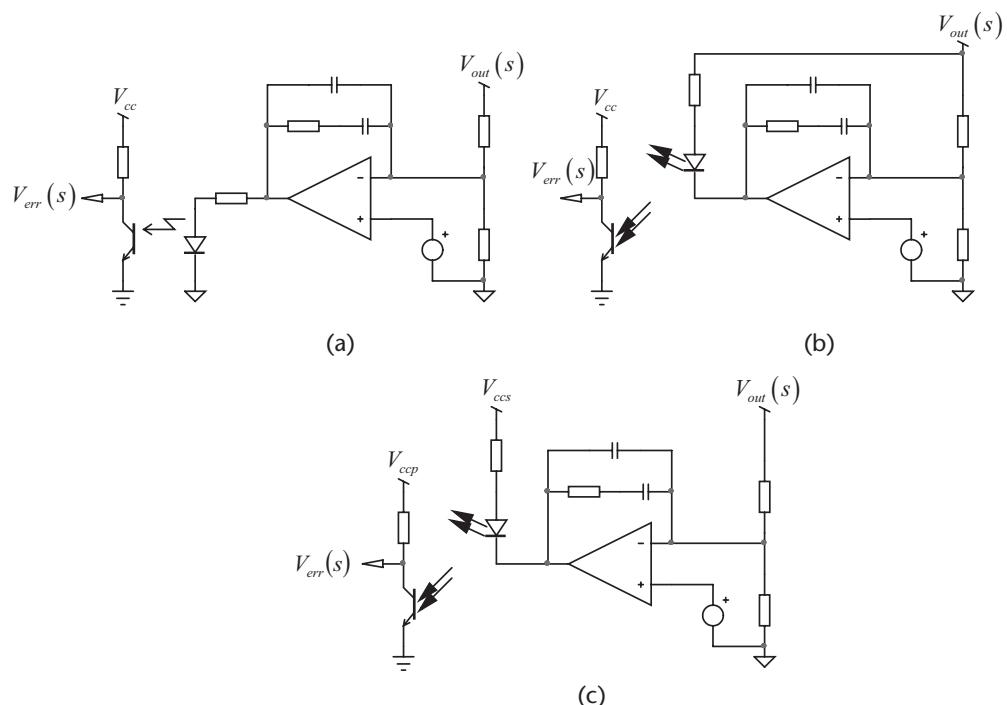


Figure 5.14 Three possibilities exist to wire an op amp output to an optocoupler.

the noise immunity. Indeed, the connection from the optocoupler to the feedback pin of the considered controller is often long and subject to noise pickup. Adding an extra capacitor for the pole and placing it exactly between the feedback pin and the controller ground (close to the integrated circuit) is the best way to avoid spurious noise injection. This is the adopted scheme for all our compensation examples featuring an optocoupler.

5.5.1 Optocoupler and Op Amp: the Direct Connection, Common Emitter

The type 2 compensator connected to the optocoupler appears in Figure 5.15. The current flowing through the LED is made of a dc component (the bias point) and an ac component. In ac and neglecting the diode dynamic resistance, the LED current is simply the op amp output voltage divided by the LED series resistor R_{LED} :

$$I_{LED}(s) = \frac{V_{op}(s)}{R_{LED}} \quad (5.61)$$

Note the position of C_2 that has moved on the nonisolated optocoupler side. C_2 represents the total capacitance on the collector node, including C_{opto} .

The ac output voltage $V_{err}(s)$ is generated by the collector current flowing in the loading network consisting of the pull-up resistor in parallel with the total capacitance seen from the collector to ground, C_2 . The capacitor, C_2 , as explained, will be the combination of the added external capacitor C_{col} (placed close to the controller feedback pin) and the optocoupler parasitic element, C_{opto} . They both appear in parallel:

$$C_2 = C_{opto} \parallel C_{col} \quad (5.62)$$

Now, as the LED current expression is known, we can easily link it to the output voltage with the help of (5.59). Please note the presence of the minus sign given the inversion brought by the common-emitter configuration:

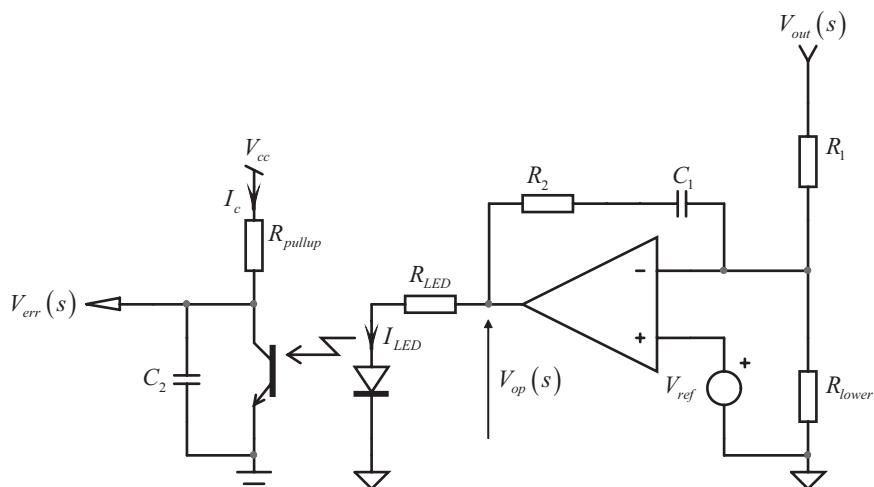


Figure 5.15 The op amp is directly driving the LED via a series resistor. Note the position of C_2 that has moved on the non-isolated optocoupler side. C_2 represents the total capacitance on the collector node, including C_{opto} .

$$V_{err}(s) = -I_{LED}(s)\text{CTR}(R_{pullup} \parallel C_2) = -V_{op}(s) \frac{R_{pullup}}{R_{LED}} \frac{1}{1 + sR_{pullup}C_2} \text{CTR} \quad (5.63)$$

The op amp solely contributes to a type 2a transfer function already seen with (5.38). Therefore, combining (5.63) with (5.38) and rearranging, we have

$$G(s) = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \frac{1 + 1/sR_2C_1}{1 + sR_{pullup}C_2} = G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.64)$$

where

$$G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} = G_1 G_2 \quad (5.65)$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (5.66)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.67)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (5.68)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (5.69)$$

It is important to note that the negative sign has disappeared since two inverting circuits are in series, the op amp and the optocoupler in a common-emitter arrangement. This polarity can fit certain types of controllers, but it has to be checked before adopting this configuration.

In (5.65), the mid-band gain is actually composed of two terms: the optocoupler network ($G_1 = R_{pullup}\text{CTR}/R_{LED}$) cascaded with the op amp contribution ($G_2 = R_2/R_1$). The optocoupler network features elements usually imposed or fixed by the controller and the optocoupler. This is the case for the pull-up resistor and the CTR. One adjustment variable for the mid-band gain can therefore be the LED resistor. However, this resistor has a limit beyond which the proper bias point is no longer ensured. When the op amp output is to its highest level (VOH), the current injected in the LED and seen on the collector multiplied by CTR has to be sufficiently strong to bring the collector to the saturation voltage, $V_{CE,sat}$ (≈ 300 mV, depending on R_{pullup} and the V_{cc} level). If not, the output voltage on the collector will limit the dynamics of the allowed feedback signal, hampering the converter operation in some conditions. As a result, an upper limit for R_{LED} has to be derived. The maximum current in the collector is equal to

$$I_{C,\max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}} \quad (5.70)$$

Reflected back to the LED, it becomes

$$I_{LED,\max} = \frac{I_{c,\max}}{\text{CTR}_{\min}} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}\text{CTR}_{\min}} \quad (5.71)$$

This current must be reached when the op amp delivers its maximum output voltage at a given supply level:

$$I_{LED,\max} = \frac{\text{VOH} - V_f}{R_{LED}} \quad (5.72)$$

As both (5.71) and (5.72) must be equal, we can extract the maximum value of the LED resistor:

$$R_{LED,\max} = \frac{R_{pullup}(\text{VOH} - V_f)\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} \quad (5.73)$$

5.5.2 A Design Example

We want to reuse the compensation parameters already exposed in the type 2 design example: a 15-dB gain at 5 kHz together with a 50° phase boost at this point. Equations (5.33) and (5.34) recommended we place a pole at 13.7 kHz and a zero at 1.8 kHz, respectively. Suppose we have the following parameters:

- $\text{VOH} = 10 \text{ V}$; the op amp maximum output voltage.
- $V_f = 1 \text{ V}$; the LED forward voltage.
- $V_{CE,sat} = 0.3 \text{ V}$; the optocoupler saturation voltage.
- $V_{cc} = 5 \text{ V}$; the pull-up V_{cc} level.
- $R_{pullup} = 1 \text{ k}\Omega$; the optocoupler pull-up resistor.
- $\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.
- $R_1 = 10 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.
- $f_{opto} = 15 \text{ kHz}$; the optocoupler pole that has been characterized with R_{pullup} .

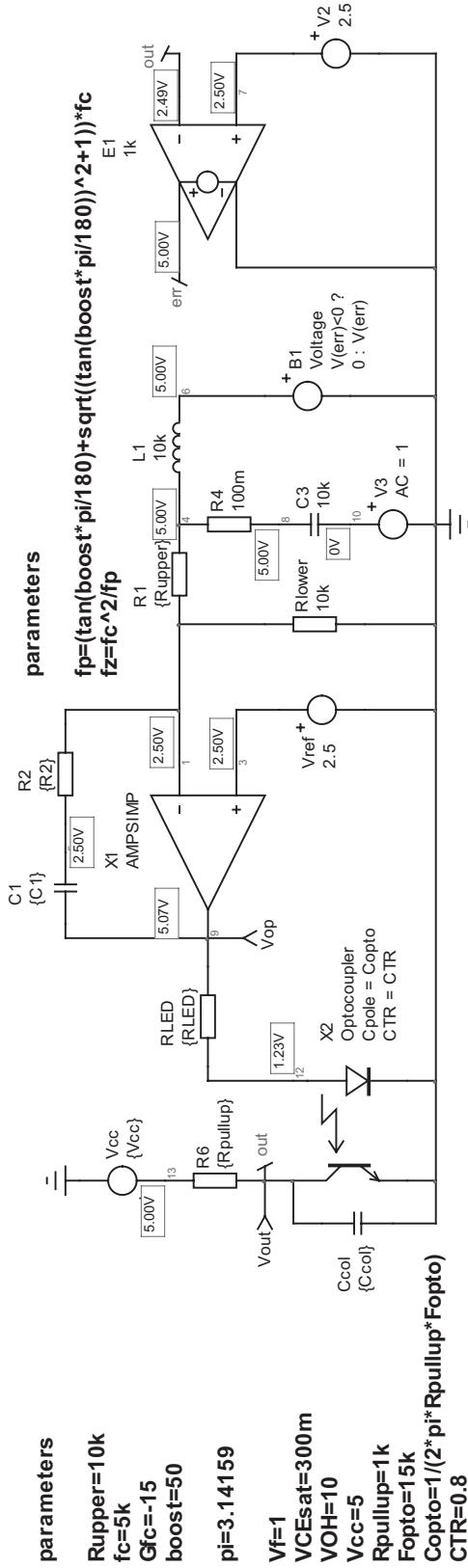
With these elements on hand, let us calculate with (5.73) the maximum LED series resistor we can select:

$$R_{LED,\max} = \frac{R_{pullup}(\text{VOH} - V_f)\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} = \frac{1k(10 - 1)}{5 - 0.3} 0.8 = 1.5 \text{ k}\Omega \quad (5.74)$$

Adopting a 20 percent safety margin and choosing a normalized value, we finally have $R_{LED} = 1.2 \text{ k}\Omega$. With this resistor now known, we can evaluate the gain brought by the optocoupler chain alone and defined by

$$G_1 = \frac{R_{pullup}}{R_{LED}} \text{CTR}_{\min} = \frac{1k}{1.2k} 0.8 = 0.666 \quad (5.75)$$

Given the needed 15-dB gain G at the crossover point (5 kHz), the second gain G_2 is simply



$$R_{max} = ((V_{OH} - V_f) / (V_{cc} - V_{CEsat})) * R_{pullup} * CTR$$

$$R_{LED} = R_{max} * 0.8$$

$$G = 10^{(-G_f/20)}$$

$$G1 = R_{pullup} * CTR / R_{LED}$$

$$G2 = G_f G_1$$

$$R2 = G2 * R_{upper}$$

$$C2 = 1 / (2 * pi * f_p * R_{pullup})$$

$$C_{col} = C2 - Copto$$

$$C1 = 1 / (2 * pi * R2 * f_z)$$

Figure 5.16 The ac simulation of the type 2 compensator directly driving the optocoupler.

$$G_2 = \frac{G}{G_1} = \frac{10^{\frac{15}{20}}}{0.666} = 8.44 \quad (5.76)$$

From (5.67) we can immediately extract the value of R_2 :

$$R_2 = R_1 G_2 = 10k \times 8.44 = 84.4 \text{ k}\Omega \quad (5.77)$$

The zero depends on R_2 , which [due to (5.68)], leads to C_1 :

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 1.8k \times 84.4k} \approx 1 \text{ nF} \quad (5.78)$$

The pole is obtained thanks to C_2 , the total capacitance seen across the optocoupler collector to ground. For a 13.7-kHz location and a 1-k Ω pull-up resistor, we have

$$C_2 = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 1k \times 13.7k} = 11.6 \text{ nF} \quad (5.79)$$

As explained, C_2 is actually made of the external capacitor C_{col} that we will place in parallel with the internal optocoupler parasitic capacitor C_{opto} . Given the characterized optocoupler pole at 15 kHz, the parasitic capacitor is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6 \text{ nF} \quad (5.80)$$

As the total capacitance is 11.6 nF, the added capacitor C_{col} is simply the difference between (5.79) and (5.80):

$$C_{col} = C_2 - C_{opto} = 11.6n - 10.6n = 1 \text{ nF} \quad (5.81)$$

Sometimes, this capacitor can be negative, meaning that the optocoupler pole position limits the placement of the high-frequency pole. In this case, try to reduce the crossover frequency and compute the pole position until (5.81) gives a minimum capacitance of 100 pF. Try also to change the crossover frequency where less phase boost is needed. This capacitor, placed across the feedback and the ground pins, very close to the controller, will not only play its ac stabilization role but will also ensure a good noise immunity.

Figure 5.16 depicts the simulation template that we used for this example.

Further to a simulation, the results appear in Figure 5.17 and show the correct values at 5 kHz. Please note that the phase lag of the whole chain is now 90° and no longer 270° since $G(s)$ does not reverse the input signal owing to the optocoupler configuration.

5.5.3 Optocoupler and Op Amp: The Direct Connection, Common Collector

In some cases, because the control law polarity is not suitable, the direct connection with the optocoupler wired in a common-emitter configuration does not work. An

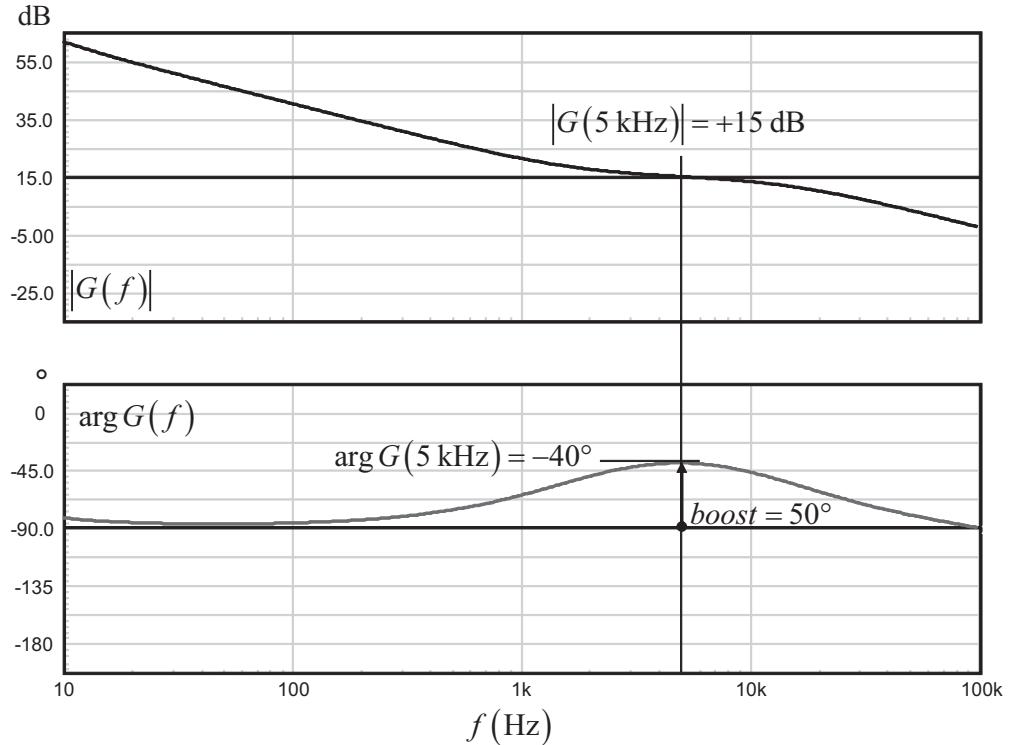


Figure 5.17 The simulation results show an excellent agreement between the input data and the final results.

option consists of placing the optocoupler loading resistor in the emitter rather than in the collector: common collector versus common emitter. This option appears in Figure 5.18.

The transfer function is exactly the same as in (5.64), except that the minus sign is coming back and R_{pullup} is replaced by $R_{pulldown}$:

$$G(s) = -\text{CTR} \frac{R_{pulldown}}{R_{LED}} \frac{R_2}{R_1} \frac{1 + 1/sR_2C_1}{1 + sR_{pulldown}C_2} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.82)$$

where:

$$G_1 = \text{CTR} \frac{R_{pulldown}}{R_{LED}} \quad (5.83)$$

$$G_1 = \text{CTR} \frac{R_{pulldown}}{R_{LED}} \quad (5.84)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.85)$$

$$\omega_z = \frac{1}{R_2C_1} \quad (5.86)$$

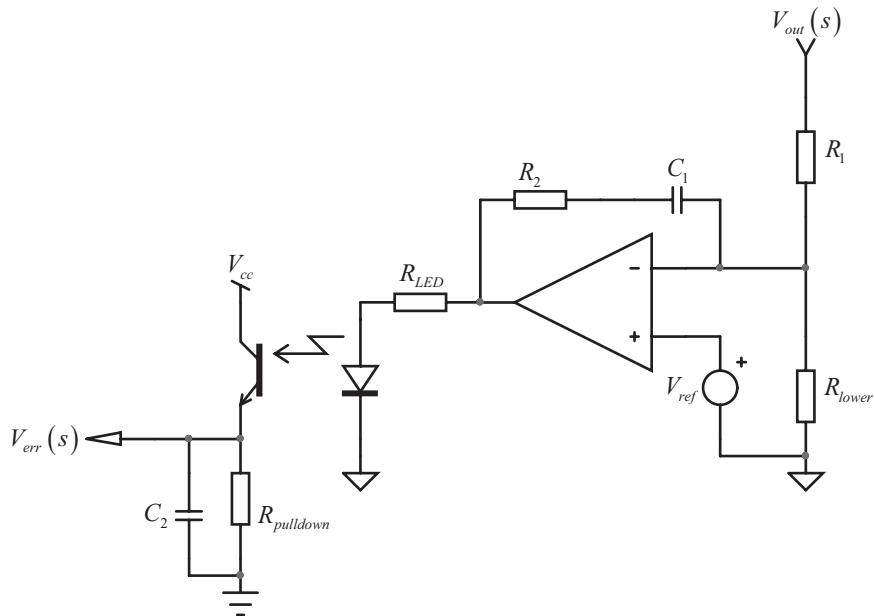


Figure 5.18 The loading resistor is now in the emitter of the optocoupler, rather than its collector, restoring the negative sign to $G(s)$.

$$\omega_p = \frac{1}{R_{pulldown}C_2} \quad (5.87)$$

The design methodology exposed in the previous design example remains the same. The maximum LED resistor now depends upon the pull-down resistor:

$$R_{LED,max} = \frac{R_{pulldown}(V_{OH} - V_f)CTR_{min}}{(V_{cc} - V_{CE,sat})} \quad (5.88)$$

5.5.4 Optocoupler and Op Amp: The Direct Connection Common Emitter and UC384X

Within the power supply controllers, the UC384X still occupies an important part of modern designs: low cost, flexibility, and ease of availability are among its characteristics. Despite the presence of an internal op amp, it is easy to connect it to one of the previous secondary-side type 1 or type 2 configurations. Indeed, in most cases, it is easier and more effective to have the intelligence—the reference and the compensator—placed on the secondary side and feed the information back to the primary side via an optocoupler. This is what Figure 5.19 suggests. In this example, the op amp is wired as a unity gain inverter, bringing the right polarity from the optocoupler collector. Make sure the op amp resistors are sufficiently high compared to R_{pullup} —otherwise, both the gain and the pole position will be affected. The design procedure exposed in the previous lines is unchanged, given the unity gain of the UC384X op amp configuration. Please note that this configuration requires an auxiliary supply on the secondary side to power the op amp independently from V_{out} ; otherwise, the converter cannot start up.

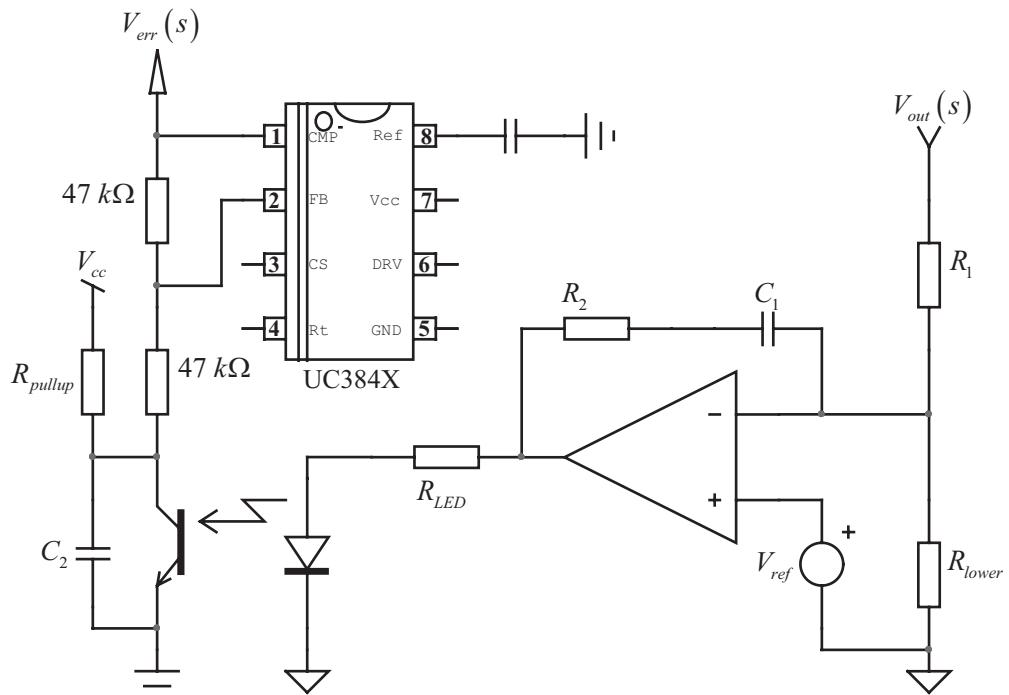


Figure 5.19 Connecting our type 2 chain to a UC384X controller is an easy exercise.

5.5.5 Optocoupler and Op Amp: Pull Down with Fast Lane

New generation controllers, such as the NCP120X from ON Semiconductor, offer a simple feedback pin internally pulled up by a resistor. To reduce the power flow, the feedback level must decrease as shown in Figure 5.20.

If we take the op amp example from Figure 5.15, for instance, we find the polarity is not correct: when the output voltage V_{out} approaches the target, V_{op} decreases. This leads to an increase of V_{err} , rather than the opposite needed by Fig-

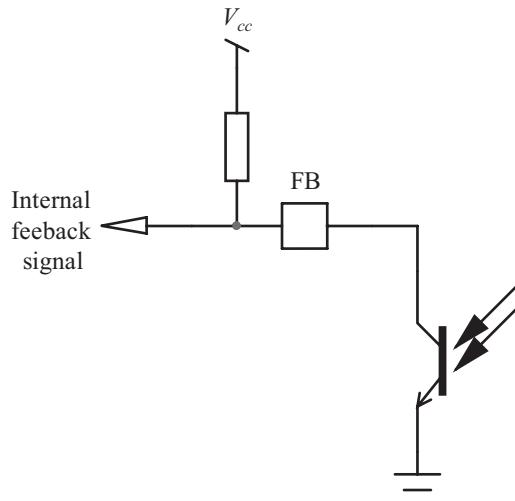


Figure 5.20 Most modern PWM controllers feature a feedback input that must be pulled down to reduce the peak current setpoint.

ure 5.20. Rather, it is more effective to arrange the op amp in a different manner, as proposed by Figure 5.21.

In this configuration, the LED current is now dependent on the op amp output voltage $V_{op}(s)$ as well as directly on the converter output voltage, $V_{out}(s)$. When C_1 is a short circuit at high frequency, the op amp output is ac flat (there is no coming through modulation, since C_1 is a short), and its dc output maintains the bias point at the right level. Therefore, if V_{out} is modulated, it is not seen at the op amp output. However, if V_{out} is modulated, since the cathode of the LED is now fixed by the op amp output, there is an ac current flowing in the LED:

$$I_{LED}(s) = \frac{V_{out}(s)}{R_{LED}} \quad (5.89)$$

This characteristic, also seen with the TL431, is imputed to the so-called *fast lane*, meaning that V_{out} has a direct access to the LED current without passing through the op amp. This particular arrangement leads to the following equation:

$$I_{LED}(s) = \frac{V_{out}(s) - V_{op}(s)}{R_{LED}} \quad (5.90)$$

The op amp output is that of a type 1 compensator already described by (5.2). By substituting $V_{op}(s)$ of (5.2) in (5.90), we have

$$I_{LED}(s) = \frac{V_{out}(s) + \left(V_{out}(s) \frac{1}{sR_1C_1} \right)}{R_{LED}} = \frac{V_{out}(s)}{R_{LED}} \left(1 + \frac{1}{sR_1C_1} \right) = \frac{V_{out}(s)}{R_{LED}} \left(\frac{1 + sR_1C_1}{sR_1C_1} \right) \quad (5.91)$$

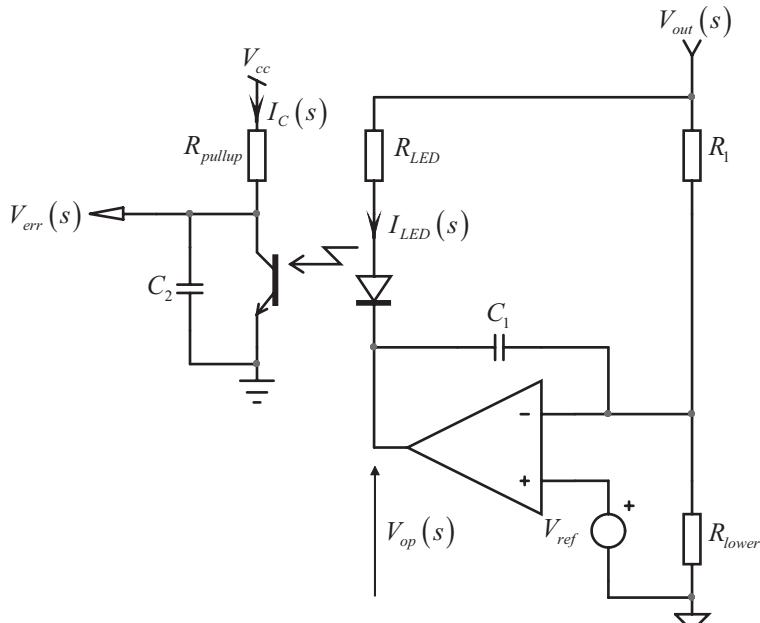


Figure 5.21 The LED drive is no longer ground referenced but directly hooked to the monitored output, creating another ac path. Despite C_1 alone across the op amp, we really have a type 2 configuration with a pole/zero pair.

In this equation, we can see the effect of the fast lane. Rather than having a simple type 1 as Figure 5.21 suggests at first glance, we have an origin pole and a zero: a type 2a! To finish our type 2 configuration, we can add a high-frequency pole as we did before across the collector-emitter of the optocoupler.

$$V_{err}(s) = -I_C(s)(R_{pullup} \parallel C_2) = -I_C(s)R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \quad (5.92)$$

Substituting (5.91) multiplied by the optocoupler CTR (to get the collector current) in (5.92), we have

$$G(s) = -\frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{1 + sR_1C_1}{sR_1C_1(1 + sR_{pullup}C_2)} \quad (5.93)$$

By factoring sR_1C_1 in the numerator, we obtain

$$G(s) = -\frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{1 + \frac{1}{sR_1C_1}}{1 + sR_{pullup}C_2} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.94)$$

This is our complete type 2 error amplifier, where

$$G_0 = \frac{R_{pullup}}{R_{LED}} \text{CTR} \quad (5.95)$$

$$\omega_p = \frac{1}{R_{pullup}C_2} \quad (5.96)$$

$$\omega_z = \frac{1}{R_1C_1} \quad (5.97)$$

$$C_2 = \frac{1}{2\pi f_p R_{pullup}} \quad (5.98)$$

$$C_1 = \frac{1}{2\pi R_1 f_z} \quad (5.99)$$

In the circuit presented in Figure 5.21, the maximum LED current is linked to the minimum op amp output swing V_{OL} , the converter output voltage V_{out} , and the LED series resistor. Again, as explained in the previous design example, the LED resistor features an upper value limit to ensure that the optocoupler collector can always bring $V_{err}(s)$ to ground. Otherwise, the loop might have a regulation problem if its dynamics are hampered in some way. The maximum collector current is given by

$$I_{C,\max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}} \quad (5.100)$$

Reflected back to the LED, it becomes

$$I_{LED,\max} = \frac{I_{C,\max}}{\text{CTR}_{\min}} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}\text{CTR}_{\min}} \quad (5.101)$$

The LED current depends on the series resistor value of course, but also on V_{out} and the minimum op amp output voltage VOL:

$$I_{LED,max} = \frac{V_{out} - V_f - VOL}{R_{LED}} \quad (5.102)$$

Equating (5.101) and (5.102), we can extract the LED resistor limit:

$$R_{LED,max} = \frac{R_{pullup}(V_{out} - V_f - VOL)CTR_{min}}{(V_{cc} - V_{CE,sat})} \quad (5.103)$$

In light of (5.95), we can see that the mid-band gain is adjusted by calculating the LED resistor value. Unfortunately, as confirmed by (5.103), there is an upper limit for this resistor. An upper limit for the LED resistor implies a lower limit for the mid-band gain:

$$G_0 \geq \frac{R_{pullup}}{R_{LED,max}} CTR \quad (5.104)$$

This is the tragedy inherent to the fast lane presence, also affecting the TL431 circuitry. If you'd like to attenuate at the selected crossover frequency rather than amplify, you are stuck with a minimum gain imposed by (5.104). Let us see the implications with a design example.

5.5.6 A Design Example

For the sake of simplicity, we will reuse the compensation parameters already exposed in the type 2 design example, slightly changed for the gain: a 5-dB amplification at 5-kHz together with a 50° phase boost at this point. Equations (5.33) and (5.34), respectively, recommended we place a pole at 13.7 kHz and a zero at 1.8 kHz. Suppose we have the following parameters:

$VOL = 0.2$ V; the op amp minimum output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$V_{out} = 5$ V; the monitored output voltage.

$R_{pullup} = 1\text{ k}\Omega$; the optocoupler pull-up resistor.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 10\text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 15$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

With these elements on hand, let us calculate with (5.103) the maximum LED series resistor we can use:

$$R_{LED,max} = \frac{R_{pullup}(V_{out} - V_f - VOL)CTR_{min}}{(V_{cc} - V_{CE,sat})} = \frac{1k(5 - 1 - 0.2)}{5 - 0.3} 0.8 \approx 647 \Omega \quad (5.105)$$

When working with (5.95) to adjust the mid-band gain, we will have to select a LED resistor value below what (5.105) recommends. Let's see what (5.95) suggests when we extract R_{LED} out of it:

$$R_{LED} = \frac{R_{pullup}}{G_0} \text{CTR}_{\min} = \frac{1k}{\frac{5}{10^{20}}} 0.8 = 450 \Omega \quad (5.106)$$

We are below 647Ω by ≈ 30 percent, so it is safe to select that resistor value. The next component is the zero capacitor C_1 . Dependent upon the upper resistor R_1 , its calculation is straightforward:

$$C_1 = \frac{1}{2\pi f_z R_1} = \frac{1}{6.28 \times 1.8k \times 10k} = 8.8 \text{ nF} \quad (5.107)$$

The pole is realized with the pull-up resistor and the compound capacitor C_2 equal to C_{col} and C_{opto} in parallel:

$$C_2 = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 1k \times 13.7k} = 11.6 \text{ nF} \quad (5.108)$$

Given the extracted optocoupler pole of 15 kHz, the parasitic capacitor C_{opto} is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6 \text{ nF} \quad (5.109)$$

As the total capacitance is 11.6 nF, the added capacitor C_{col} is simply the difference between (5.108) and (5.109):

$$C_{col} = C_2 - C_{opto} = 11.6n - 10.6n = 1 \text{ nF} \quad (5.110)$$

We are now all set and can start a simulation to verify our calculations. This is what appears in Figure 5.22, showing the proper operating points.

The Bode plot response of the previous compensation circuit is shown in Figure 5.23.

Equation (5.104) teaches us that the gain cannot be smaller than

$$G_0 \geq 20 \log_{10} \left(\frac{1k}{647} 0.8 \right) = 1.84 \text{ dB} \quad (5.111)$$

Should we need a 0-dB gain at 5 kHz rather than the adopted 5 dB, we would violate (5.105), and the loop could not properly bias the LED and the optocoupler. This is the inherent limitation of the fast lane and can often be a problem where attenuation rather than gain are needed. To get rid of this issue, why not trying to suppress the fast lane?

5.5.7 Optocoupler and Op Amp: Pull-Down with Fast Lane, Common Emitter, and UC384X

Given the return of the negative sign in the transfer equation of our compensator, we can connect this circuit to either a NCP120X type of controller or a UC384X. The

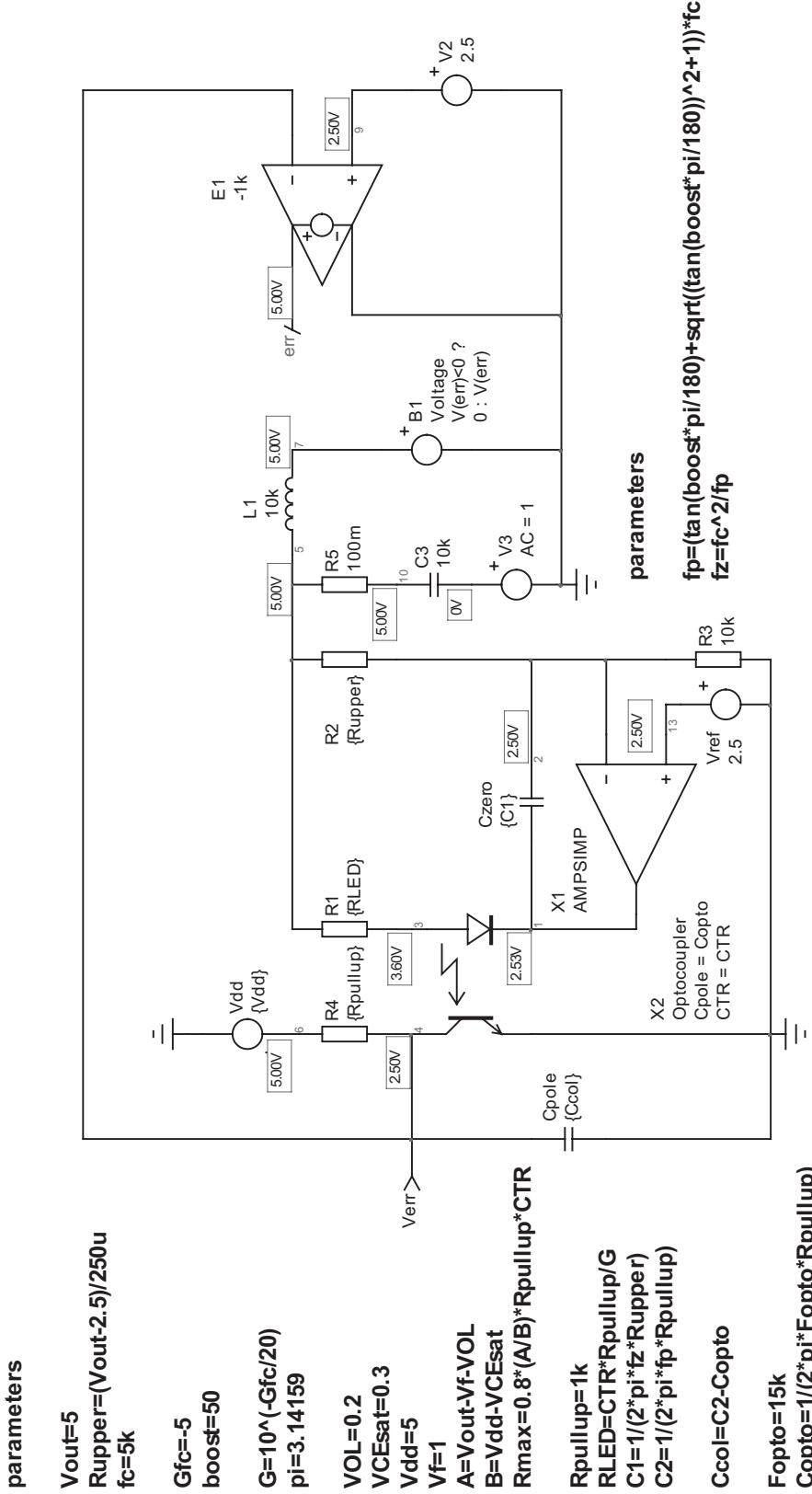


Figure 5.22 The simulation fixture shows a type 2 associating an op amp and an optocoupler. This time, the op amp drives the LED from its cathode rather than its anode as seen before.

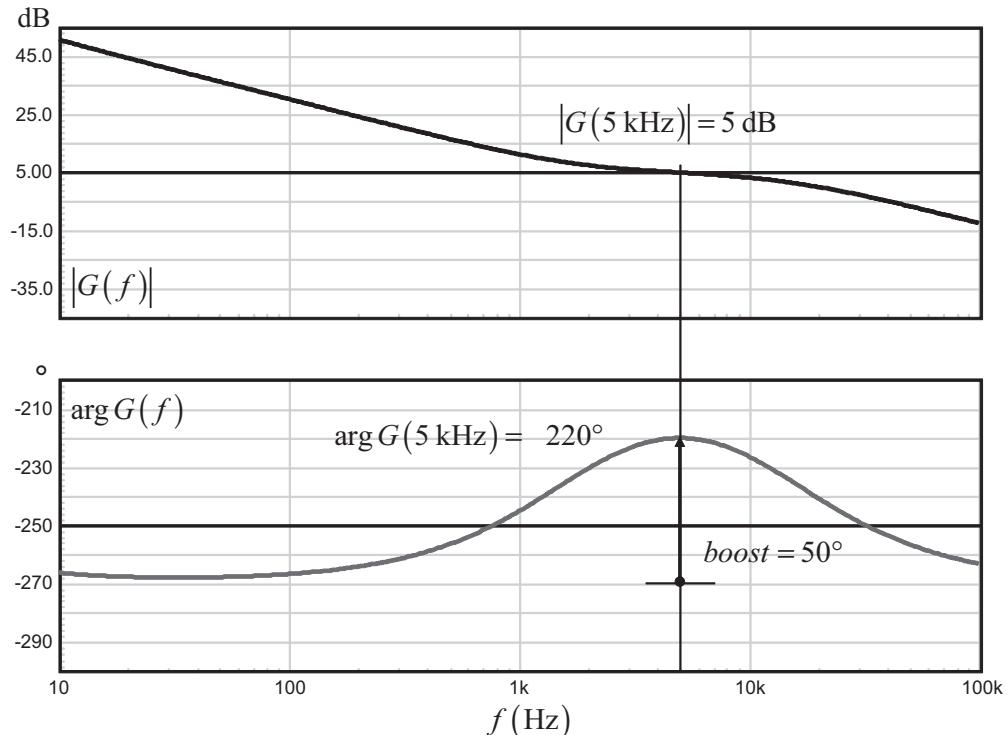


Figure 5.23 The Bode plot response of the type 2 return chain confirms the 5-dB gain at 5 kHz with the right phase boost.

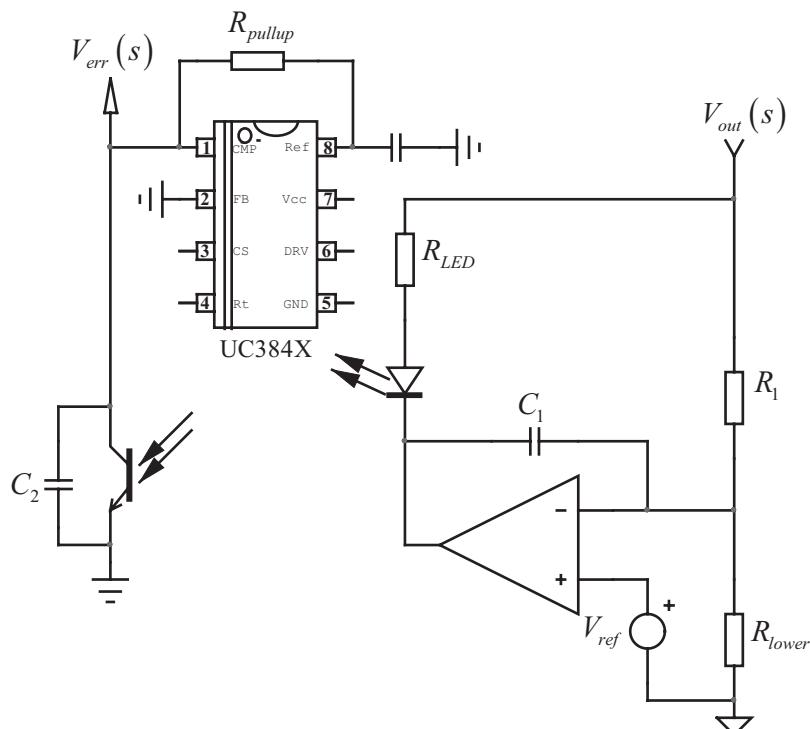


Figure 5.24 The UC384X can also be implemented without using its internal operational amplifier. A simple pull-up resistor to the 5-V reference is enough to drive it from the optocoupler collector.

error amplifier inside this chip cannot deliver more than 1 mA. Therefore, a solution is to hook its output (pin 1, CMP) to the 5-V reference voltage via a pull-up resistor and ground the feedback input (pin 2, FB). Then, connect the optocoupler collector to pin 1 and you are all set! This configuration is described in Figure 5.24.

The design procedure is the same that we just have seen in the previous design example.

Compared to what was shown in Figure 5.19, when V_{out} is absent at startup, the op amp does not impose a current into the LED and the optocoupler collector is high, naturally imposing the maximum peak current: the converter can start without problems, even if the op amp is not supplied at the beginning.

5.5.8 Optocoupler and Op Amp: Pull Down Without Fast Lane

In applications where more flexibility is needed in the choice of the compensated crossover gain, a solution consists in suppressing the fast lane. The fast lane actually comes from a direct ac relationship between the LED current and the monitored variable. To get rid of it, either connect the LED anode to a regulated dc voltage, independent from the output level, or isolate it via a Zener diode and a capacitor. This is what Figure 5.25 suggests. This solution is actually very close to the direct LED drive disclosed in Figure 5.15, except that we now drive the optocoupler diode cathode. Also, as we will see, the error signal polarity is now compatible with pull-down feedback inputs such as the one already presented in Figure 5.20. A similar regulation architecture is found on the popular NCP120X series from ON Semiconductor, for instance. Capitalizing on what has already been derived, we can immediately express the LED ac current:

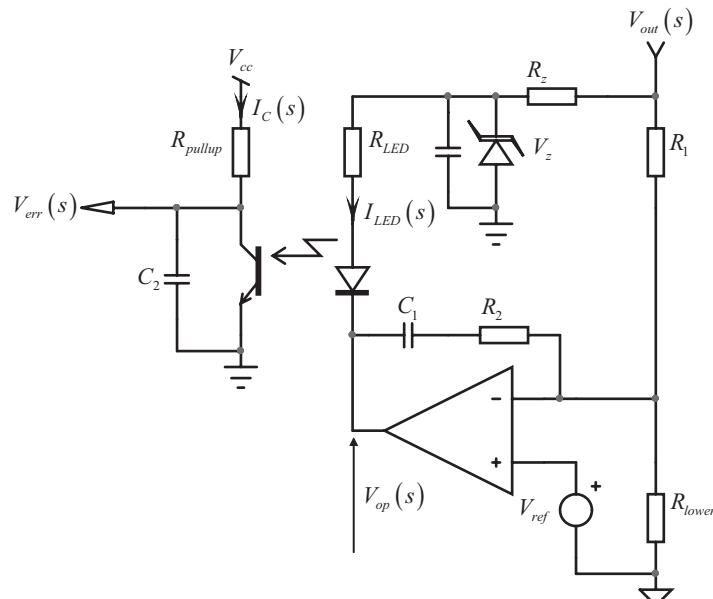


Figure 5.25 By inserting an ac-decoupling network between the output voltage and the LED anode, it becomes possible to get rid of the fast lane.

$$I_{LED}(s) = -\frac{V_{op}(s)}{R_{LED}} \quad (5.112)$$

The op amp ac output $V_{op}(s)$ is that of a type 2a whose expression was derived in (5.39):

$$\frac{V_{op}(s)}{V_{out}(s)} = -\frac{R_2 + \frac{1}{sC_1}}{R_1} = -\frac{1 + sR_2C_1}{sR_1C_1} = -\frac{sR_2C_1}{sR_1C_1} \left(\frac{1}{sR_2C_1} + 1 \right) = -\frac{R_2}{R_1} \left(1 + \frac{1}{sR_2C_1} \right) \quad (5.113)$$

The second stage is made of the optocoupler path and classically involves the pull-up resistor and the capacitor from collector to ground, C_2 :

$$V_{err}(s) = -I_{LED}(s)R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \text{CTR} \quad (5.114)$$

Combining (5.112), (5.113), and (5.114), we obtain the complete transfer function:

$$G(s) = -\text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \frac{1 + 1/sR_2C_1}{1 + sR_{pullup}C_2} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (5.115)$$

where

$$G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} = G_1 G_2 \quad (5.116)$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (5.117)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.118)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (5.119)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (5.120)$$

As we have shown before, the LED resistor must be sized to let the optocoupler properly pull the feedback node down to ground. A sufficient current must therefore flow through R_{LED} to let the op amp fully control the feedback voltage. However, the limit on the LED resistor fixes only one gain expression, G_1 , but as we have a type 2a with the op amp, we can freely set R_2 without limitation at all. The equation for $R_{LED,\max}$ is similar to the one already derived:

$$R_{LED,\max} = \frac{R_{pullup}(V_Z - V_f - \text{VOL})\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} \quad (5.121)$$

In this expression, V_Z represents the Zener voltage derived from the output voltage. This voltage must also be carefully selected. If too low, you limit the voltage excursion over the op amp output, and if too high, you reduce the ac decoupling effects you are looking for—that is to say, ac-separating the LED anode voltage from

the output voltage $V_{out}(s)$. Setting the Zener voltage around two thirds of the output voltage looks like a reasonable choice.

Once the LED resistor has been selected, we need to calculate the Zener diode biasing resistor R_Z . This resistor supplies the current not only for the LED branch but also for the Zener diode to make it operate far enough from its knee (the lower its dynamic impedance, the better ac isolation from V_{out} it provides). The LED maximum current is actually reached when the feedback voltage V_{FB} (or V_{err}) is pulled down to $V_{CE,sat}$. In this case, the LED current is simply

$$I_{LED,max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}CTR_{min}} \quad (5.122)$$

The Zener dropping resistor R_Z is therefore immediately derived through

$$R_Z = \frac{V_{out} - V_Z}{I_{LED,max} + I_{Zbias}} \quad (5.123)$$

Substituting (5.122) in (5.123), we obtain

$$R_Z = \frac{(V_{out} - V_Z)R_{pullup}CTR_{min}}{V_{cc} - V_{CE,sat} + I_{Zbias}R_{pullup}CTR_{min}} \quad (5.124)$$

5.5.9 A Design Example

Let's assume we still want the same crossover frequency of 5 kHz associated with a 50° phase boost, but rather than amplifying at this frequency, we want a -10-dB attenuation. The variables are as follows:

$VOL = 0.2$ V; the op amp minimum output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$R_{pullup} = 1$ kΩ; the optocoupler pull-up resistor.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$V_{out} = 12$ V; the converter output voltage.

$R_1 = 38$ kΩ; the upper resistor in the resistor bridge observing the output variable.

$V_{out} = 12$ V; the monitored output voltage.

$f_{opto} = 15$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

$V_Z = 8.2$ V; the Zener diode breakdown voltage.

$I_{Zbias} = 1$ mA; the Zener diode bias current.

With these elements on hand, let us calculate with (5.121) the maximum LED series resistor we can select:

$$R_{LED,max} = \frac{R_{pullup}(V_Z - V_f - VOL)CTR_{min}}{(V_{cc} - V_{CE,sat})} = \frac{1k \times (8.2 - 1 - 0.2) \times 0.8}{5 - 0.3} \approx 1.2 \text{ k}\Omega \quad (5.125)$$

Adopting a 20 percent safety margin and choosing a normalized value, we finally have $R_{LED} = 910 \Omega$. With its resistor now known, we can evaluate the gain brought by the optocoupler chain alone defined by

$$G_1 = \frac{R_{pullup}}{R_{LED}} \text{CTR}_{\min} = \frac{1k}{910} 0.8 = 0.88 \quad (5.126)$$

Given the needed -10 -dB attenuation at the crossover point (5 kHz), the second gain G_2 is simply

$$G_2 = \frac{10^{\frac{-10}{20}}}{0.88} = 0.328 \quad (5.127)$$

From (5.118) we can immediately extract the value of R_2 :

$$R_2 = R_1 G_2 = 38k \times 0.328 \approx 12.5 \text{ k}\Omega \quad (5.128)$$

The zero depends on R_2 , which, after (5.34) and (5.119), leads to C_1 :

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 1.8k \times 12.5k} \approx 7 \text{ nF} \quad (5.129)$$

The pole is obtained owing to C_2 , the total capacitance seen across the optocoupler collector to ground. For a 13.7-kHz upper pole location—see (5.33) and (5.120)—and a 1-k Ω pull-up resistor, we have

$$C_2 = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 1k \times 13.7k} = 11.6 \text{ nF} \quad (5.130)$$

As explained, C_2 is actually made of an external capacitor C_{col} in parallel with the internal optocoupler parasitic capacitor C_{opto} . Given the extracted optocoupler pole of 15 kHz, the parasitic capacitor is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6 \text{ nF} \quad (5.131)$$

As the total capacitance is 11.6 nF, the added capacitor C_{col} is simply the difference between (5.130) and (5.131):

$$C_{col} = C_2 - C_{opto} = 11.6n - 10.6n = 1 \text{ nF} \quad (5.132)$$

The ac design is finished, so let's see what resistance value we can select for R_Z . Applying (5.124), we have

$$R_Z = \frac{(V_{out} - V_Z) R_{pullup} \text{CTR}_{\min}}{V_{cc} - V_{CE,sat} + I_{Zbias} R_{pullup} \text{CTR}_{\min}} = \frac{(12 - 8.2) \times 1k \times 0.8}{5 - 0.3 + 1m \times 1k \times 0.8} = 552 \Omega \quad (5.133)$$

We can also apply a safety margin on this value and select a 470- Ω resistor. This design is now over, and we can feed our simulator with these values. This is what Figure 5.26 shows you with the proper bias point values.

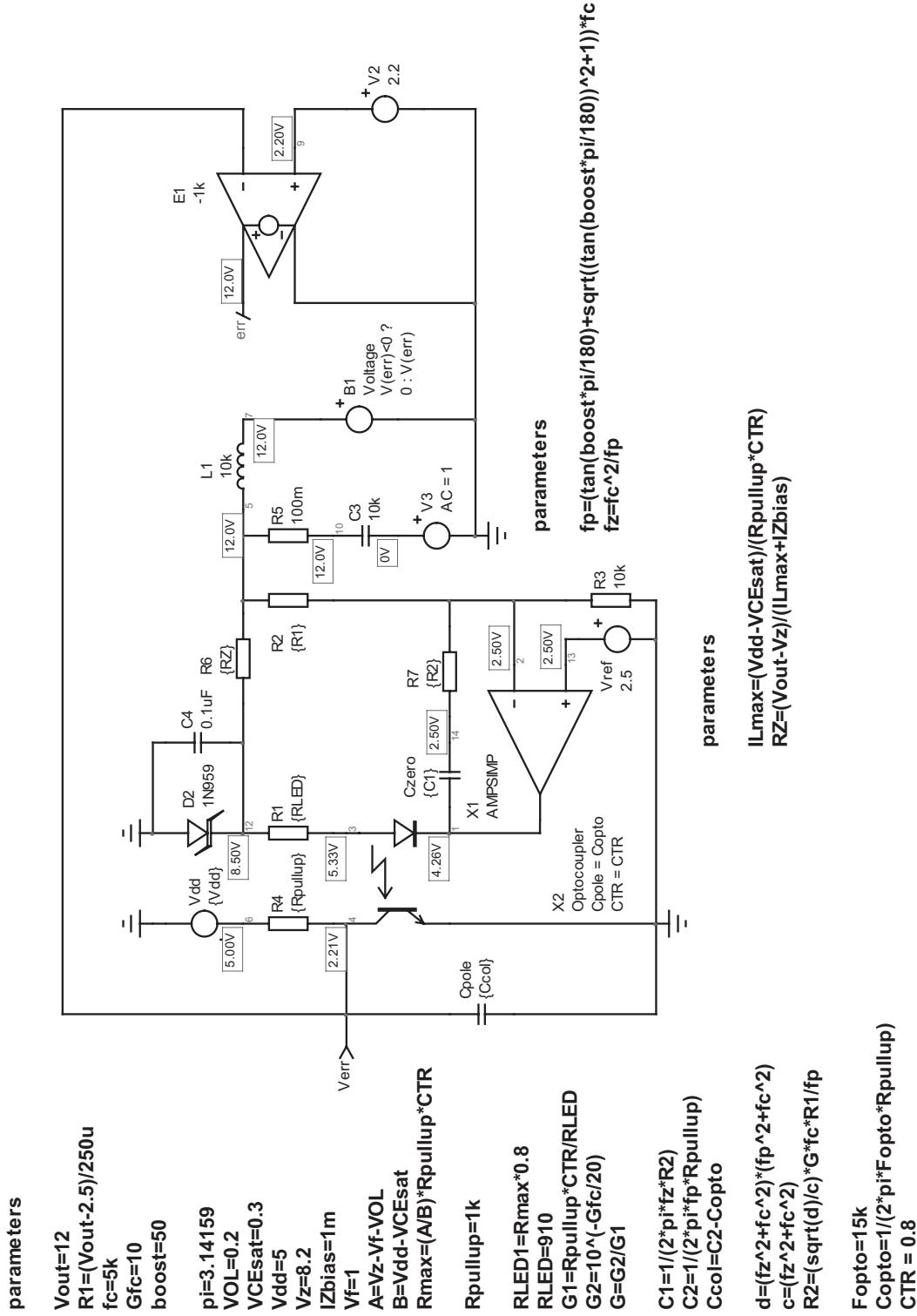


Figure 5.26 An ac simulation test fixture for the type 2 compensator where the fast lane on the secondary side has been removed.

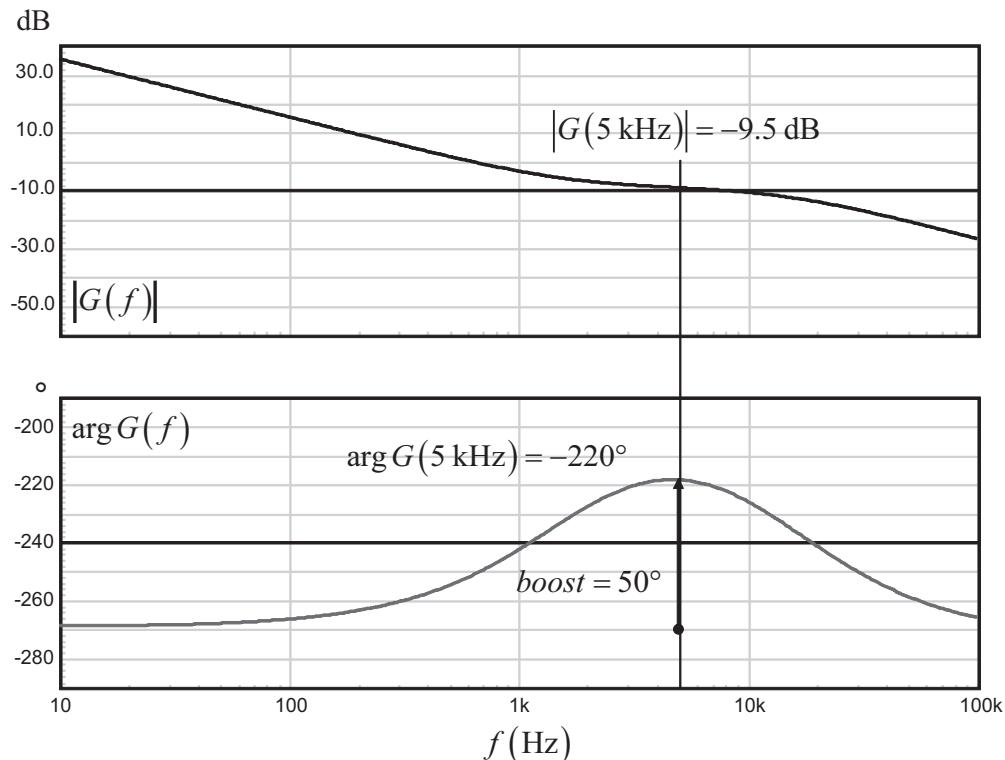


Figure 5.27 The ac sweep shows the attenuation slightly less than our initial target of -10 dB . This is linked to the LED dynamic resistor and the imperfect ac decoupling provided by the Zener network.

The ac simulation results appear in Figure 5.27 and show a slight discrepancy between the -10-dB target and the -9.5-dB result read on the graph. This is mainly linked to the imperfect decoupling brought by the Zener network. If this dispersion between the target and the result is considered too wide, it can easily be compensated by increasing the attenuation/gain target by the observed difference. We increase the attenuation target to -10.5 dB in this case.

In this example, we have shown a Zener-based network. It could of course be replaced by a linear regulator, either integrated or using a bipolar transistor. We could even think of an auxiliary winding dedicated to this purpose. With this latter, the designer must ensure the lack of ac coupling between the auxiliary voltage feeding the optocoupler LED and the regulated rail (Figure 5.28).

5.5.10 Optocoupler and Op Amp: A Dual-Loop Approach in CC-CV Applications

In certain applications, it is necessary to control the output voltage V_{out} or the delivered current I_{out} and ensure one of them remains constant. This is called a constant-current constant-voltage converter (CC-CV). Even in pure CC applications, a voltage-loop is always present to prevent output voltage runaways in light-load conditions. Widely used in notebook or cell-phone chargers, their typical

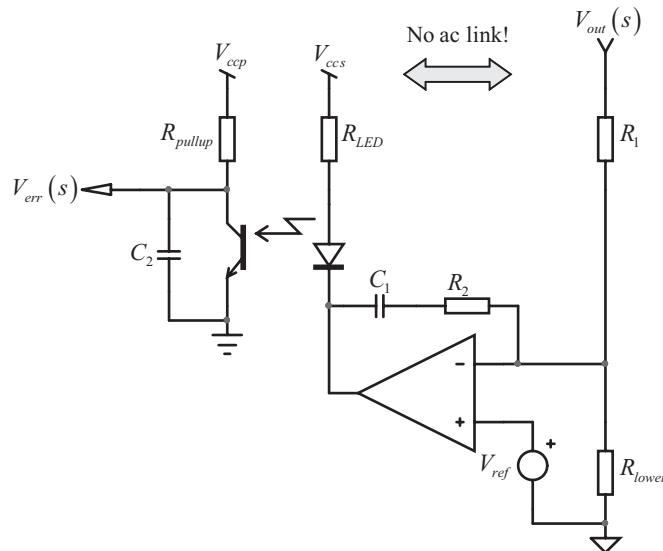


Figure 5.28 The Zener-based network can be replaced by a dc source, which must be ac-decoupled from V_{out} .

output characteristic appears in Figure 5.29: one control section operates at a time, either the voltage loop or the current loop.

The voltage implementation requires a sensing network made of two resistors similar to those used in the previous examples. The current regulation loop needs a sensing element, usually a few resistors, plus a low-voltage reference voltage.

Figure 5.30 portrays the typical secondary side of a CC-CV control circuitry, where the sensing ground is actually the converter output ground. Please note the insertion of a sense resistor in series with the secondary-side winding. The voltage developed across this element is, however, negative when referenced to the load ground (see the sensed voltage arrow in Figure 5.30). Since the reference voltage, usually a 2.5-V source, is linked to the output ground, a means has to be found to authorize the current loop implementation. A zoom of this portion appears in Figure 5.31.

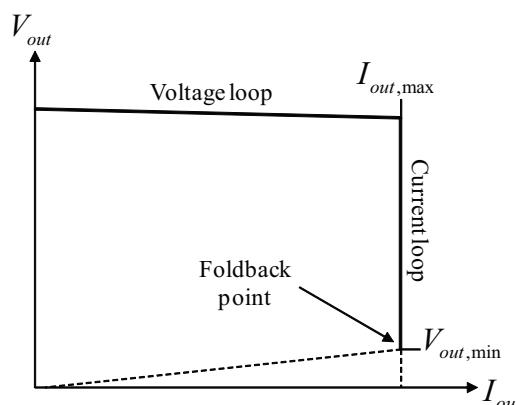


Figure 5.29 This is the typical charging profile of a CC-CV converter.

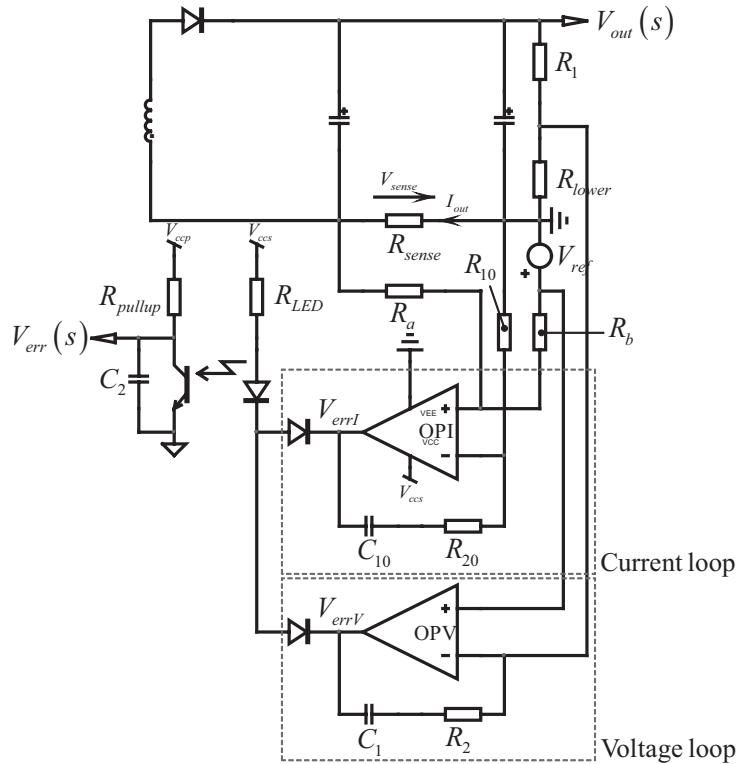


Figure 5.30 A typical charger secondary-side architecture showing both loops and their respective elements.

The trick is to sum the negative voltage across R_{sense} with a portion of the reference voltage so that the noninverting pin of the op amp reaches 0 when the current reaches the imposed limit. To analyze such a system, the best is to use the superposition theorem. The voltage on the noninverting pin is thus the sum of the voltage obtained when V_{ref} is shorted to ground and the voltage obtained once V_{sense}

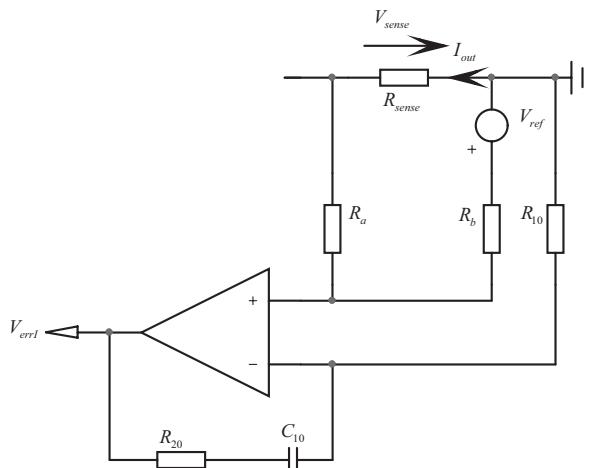


Figure 5.31 The zoomed current loop structure confirms a reference voltage connected to the output ground.

is shorted to ground. As the op amp will strive to maintain 0 V between both of its input pins, we have

$$V(+) = V_{ref} \frac{R_a}{R_a + R_b} + V_{sense} \frac{R_b}{R_a + R_b} = 0 \quad (5.134)$$

Solving for V_{sense} :

$$V_{sense} = -V_{ref} \frac{R_a}{R_b} \quad (5.135)$$

When referenced to the ground, $V_{sense} = -R_{sense}I_{out}$. We can thus extract the output current setpoint:

$$I_{out} = V_{ref} \frac{R_a}{R_{sense}R_b} \quad (5.136)$$

By selecting R_{sense} to minimize the losses but also to maintain a sufficient voltage drop for noise immunity (≈ 100 mV), R_a and R_b can be further calculated.

A CC-CV regulation circuit works by activating either the current loop if I_{out} is greater than the current setpoint, or the voltage loop, to maintain V_{out} within the target. When the voltage loop is active, the OPV op amp leads the regulation, while the op amp checking the current, OPI, keeps its output high, having its associated series diode blocked: the current regulation block is silent. When the current loop starts to detect that the current exceeds the limit imposed by (5.136), the OPI op amp pulls the optocoupler LED down and the output voltage goes down. The voltage-loop op amp OPV detects this event and increases its output, trying to force the converter to release more energy. As the two op amps outputs are wired in a logical OR configuration via series diodes, the output that pulls the most current out of the diodes leads: the current loop now regulates, V_{out} drops, op amp OPV naturally increases its output, and the voltage-loop diode blocks.

A typical example of such an application is a battery charger: when you connect a discharged battery to the converter, the output current is limited and kept constant as the battery voltage starts to increase. In this mode, the current loop leads. As the voltage increases and approaches the target, the voltage loop takes over and regulates the output level to a safe value.

The principle is depicted by the simplified sketch offered in Figure 5.32, where the switch pictures the action of the two diodes. As you can see, the ac signal coming out of either op amps crosses a common block $G_1(s)$ made of the optocoupler and its associated passive elements. Its transfer function has already been derived several times:

$$G_1(s) = \frac{V_{err}(s)}{V_{op}(s)} = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{1}{1 + sR_{pullup}C_2} \quad (5.137)$$

Therefore, if you have decided to compensate the voltage loop according to certain criterion, $G_1(s)$ will be shaped to satisfy them. Unfortunately, this block will also affect the transfer function of the current loop when made active. Therefore, there are chances that the high-frequency pole purposely introduced by $R_{pullup}C_2$ for the voltage loop does not suit the compensation strategy you want for the current loop. However, the loops we want to compensate are almost identical in phase

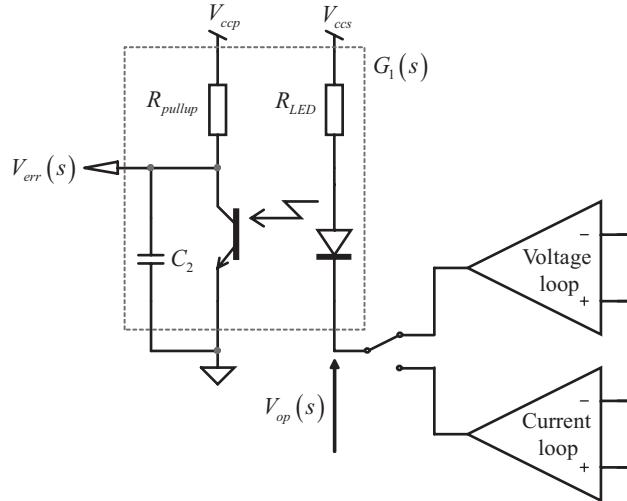


Figure 5.32 A CC-CV regulator features two loops, separately activated via a network of diodes, represented by a two-position switch. In ac, both loops cross a common block noted $G_1(s)$.

response at a given operating point. This is because the output current is the output voltage divided by the load resistor and transformed into a voltage by R_{sense} . We can show that the current loop ac response $H_i(s)$ is that of the voltage loop $H_v(s)$ scaled down by the sense resistor R_{sense} and the load resistor R_{load} :

$$H_i(s) = H_v(s) \frac{R_{sense}}{R_{load}} \quad (5.138)$$

A few iterations will thus be necessary to select a high-frequency pole that matches the voltage-loop requirements but also that of the current loop. We will see that in the design example. Capitalizing on the type 2a equation (5.39), the two separate transfer function expressions can be written the following ways:

$$G_v(s) = \frac{V_{err}(s)}{V_{out}(s)} = -G_l(s) \frac{R_2}{R_1} \left(1 + \frac{R_2 C_1}{s} \right) = -G_l G_{2v} \frac{1 + \omega_{zv}/s}{1 + s/\omega_p} \quad (5.139)$$

$$G_i(s) = \frac{V_{err}(s)}{V_{sense}(s)} = -G_l(s) \frac{R_{20}}{R_{10}} \left(1 + \frac{R_{20} C_{10}}{s} \right) = -G_l G_{2i} \frac{1 + \omega_{zi}/s}{1 + s/\omega_p} \quad (5.140)$$

in which we have

$$G_l = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (5.141)$$

$$G_{2v} = \frac{R_2}{R_1} \quad (5.142)$$

$$G_{2i} = \frac{R_{20}}{R_{10}} \quad (5.143)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (5.144)$$

$$\omega_{zv} = \frac{1}{R_2 C_1} \quad (5.145)$$

$$\omega_{zi} = \frac{1}{R_{20} C_{10}} \quad (5.146)$$

As expected, the high-frequency pole ω_p is common to both transfer functions. Once fixed for the first compensated loop, the designer will have to adjust the zero for the second loop in order to meet the required phase boost. Please note that we purposely adopted a control scheme where the fast lane has been suppressed: the LED anode is connected to an auxiliary voltage V_{ccs} . Furthermore, this auxiliary voltage, V_{ccs} , needs to be maintained when V_{out} collapses to zero; otherwise, the regulation would be lost with consequences depending on the control scheme. A few solutions helping to solve this problem will be further presented.

5.5.11 A Design Example

We have a discontinuous conduction mode (DCM) flyback converter operated in current-mode control, which delivers a 12 V output voltage. We want to set the constant current section to a maximum current of 1 A.

First, let us calculate the resistive network R_a , R_b , and R_{sense} of Figure 5.31. To arbitrarily limit the power dissipation to 100 mW on the sensing resistor, we can quickly derive its value:

$$R_{sense} = \frac{P_{sense}}{I_{out}^2} = \frac{0.1}{1} = 100 \text{ m}\Omega \quad (5.147)$$

Then, if the reference voltage in our integrated circuit is 2.5 V, we can fix one of the two resistors R_a or R_b and select the other one. If R_a is arbitrarily fixed to 2 k Ω and the sensing shunt is 100 m Ω , then according to (5.136), R_b equals

$$R_b = V_{ref} \frac{R_a}{R_{sense} I_{out}} = 2.5 \frac{2k}{0.1 \times 1} = 50 \text{ k}\Omega \quad (5.148)$$

To compensate the loops, we need open-loop plots of the converter we have designed, observing either the output voltage, $H_v(s)$, or the voltage image of the output current, $H_i(s)$. The results appear in Figure 5.33.

We have purposely selected two different crossover frequencies for the voltage and current loops, 1 kHz and 400 Hz, respectively, but equal values would also work. Let's tackle the voltage loop compensation first using the following data:

$V_{OL} = 0.2 \text{ V}$; the op amp minimum output voltage.

$V_f = 1 \text{ V}$; the LED forward voltage.

$V_{CE,sat} = 0.3 \text{ V}$; the optocoupler saturation voltage.

$V_{ccp} = 5 \text{ V}$; the primary-side pull-up V_{cc} level.

$V_{ccs} = 8.2 \text{ V}$; the secondary-side V_{cc} level.

$R_{pullup} = 20 \text{ k}\Omega$; the optocoupler pull-up resistor given by the selected controller.

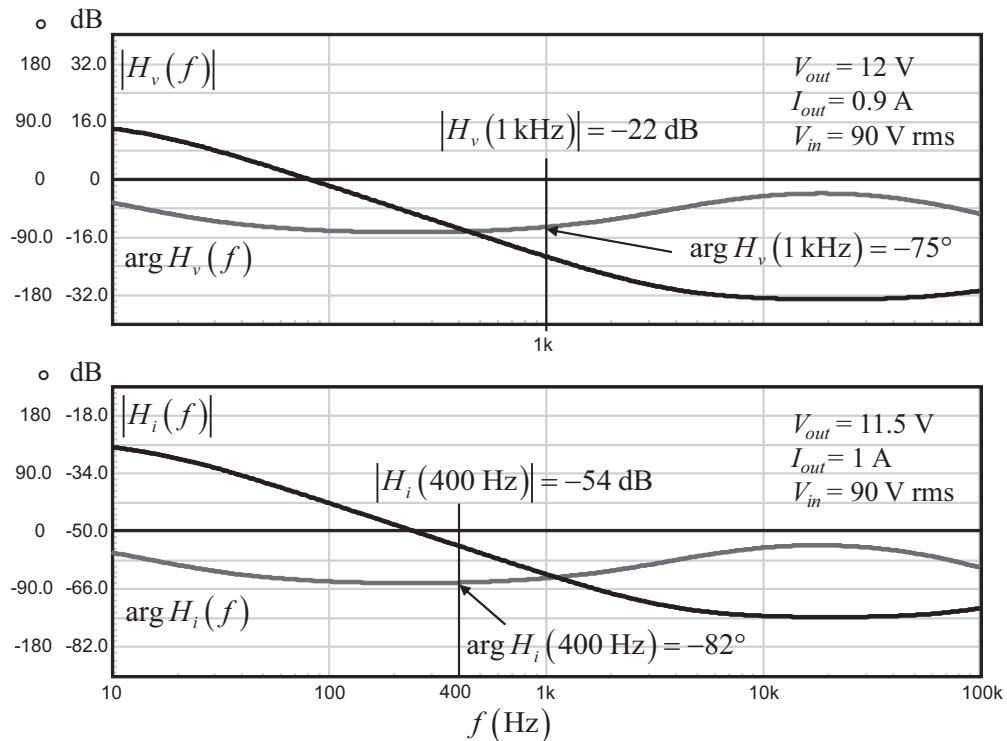


Figure 5.33 The output voltage and output current open-loop gains of a flyback converter operated in the DCM.

$\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.

$V_{out} = 12\text{ V}$; the converter output voltage.

$R_1 = 38\text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$R_{10} = 1\text{ k}\Omega$; the resistor sensing the output current and connected to ground.

$f_{opto} = 6\text{ kHz}$; the optocoupler pole that has been characterized with R_{pullup} .

We first start by working the G_1 block, made of the optocoupler element. The maximum LED resistor value is computed using (5.121):

$$R_{LED,\max} = \frac{R_{pullup}(V_{ccp} - V_f - \text{VOL})\text{CTR}_{\min}}{(V_{ccp} - V_{CE,sat})} = \frac{20k \times (8.2 - 1 - 0.2) \times 0.8}{5 - 0.3} \approx 23.8\text{ k}\Omega \quad (5.149)$$

Given the $20\text{-k}\Omega$ pull-up resistor on the primary and its associated small pull-down current ($235\text{ }\mu\text{A}$), we have plenty of margin on the LED resistor selection. Let's adopt a $10\text{-k}\Omega$ value. Following (5.141) the gain brought by G_1 is thus

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} = 0.8 \frac{20k}{10k} = 1.6 \approx 4.1\text{ dB} \quad (5.150)$$

For a 1-kHz crossover frequency, we need to lift up the gain curve by $G_v = 22\text{ dB}$ (see Figure 5.33). As G_1 already equals 4.1 dB , G_{2v} will need to be

$$G_{2v} = G_v - G_1 = 22 - 4.1 = 17.9 \text{ dB} \quad (5.151)$$

Given a 38-k Ω resistor value for the upper resistor bridge divider, using (5.142) we have

$$R_2 = R_1 10^{\frac{G_{2v}}{20}} = R_1 10^{\frac{17.9}{20}} = 38k \times 7.85 = 298 \text{ k}\Omega \quad (5.152)$$

The phase lag of $H_v(s)$ is -75° at 1 kHz. For a 60° phase margin, we will need to extract the phase boost using the following formula, already seen in Chapter 4:

$$\arg H(f_c) - [270^\circ - \text{boost}] = -360^\circ + \varphi_m \quad (5.153)$$

The necessary phase boost thus amounts to

$$\text{boost} = -360^\circ + \varphi_m - \arg H(f_c) + 270^\circ = -90 + 60 + 75 = 45^\circ \quad (5.154)$$

To satisfy this required boost at a 1-kHz crossover frequency, the pole will be placed at the following location:

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.4 \times 1k = 2.4 \text{ kHz} \quad (5.155)$$

Given a crossover frequency placed at the geometric mean between the zero and pole, the zero will be placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{1k \times 1k}{2.4k} \approx 416 \text{ Hz} \quad (5.156)$$

We can now calculate capacitor C_1 to be placed in series with R_2 using (5.145):

$$C_1 = \frac{1}{2\pi R_2 f_z} = \frac{1}{6.28 \times 298k \times 416} \approx 1.3 \text{ nF} \quad (5.157)$$

Implementing (5.144), the capacitor taking place over the optocoupler collector is found to be

$$C_2 = \frac{1}{2\pi f_p R_{pullup}} = \frac{1}{6.28 \times 2.4k \times 20k} = 3.3 \text{ nF} \quad (5.158)$$

We know that the optocoupler parasitic capacitor C_{opto} contributes to C_2 :

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} = 1.3 \text{ nF} \quad (5.159)$$

We thus need to add a small extra capacitor C_{col} whose value is

$$C_{col} = C_2 - C_{opto} = 3.3n - 1.3n = 2 \text{ nF} \quad (5.160)$$

The voltage loop is now fully compensated. Let's take a look at the current loop now. Looking back to Figure 5.33, the gain deficiency is 54 dB at 400 Hz ($G_i =$

54 dB), together with a phase lag of 82° . According to (5.150), we need to provide an additional gain of

$$G_{2i} = G_i - G_1 = 54 - 4.1 = 49.9 \text{ dB} \quad (5.161)$$

Using (5.143), we can immediately calculate the series resistor R_{20} by arbitrarily affecting to R_{10} a value of $1 \text{ k}\Omega$:

$$R_{20} = R_{10} 10^{\frac{G_{2i}}{20}} = R_{10} 10^{\frac{49.9}{20}} = 1k \times 312 = 312 \text{ k}\Omega \quad (5.162)$$

For a phase lag of 82° (see Figure 5.33), how much phase boost must we provide to reach a phase margin of 60° :

$$\text{BOOST} = -360^\circ + \varphi_m - \arg H(f_c) + 270^\circ = -90 + 60 + 82 = 52^\circ \quad (5.163)$$

We know that a pole already exists, given by the presence of the pull-up resistor and capacitor C_2 . For the voltage loop stability purposes, this pole is currently

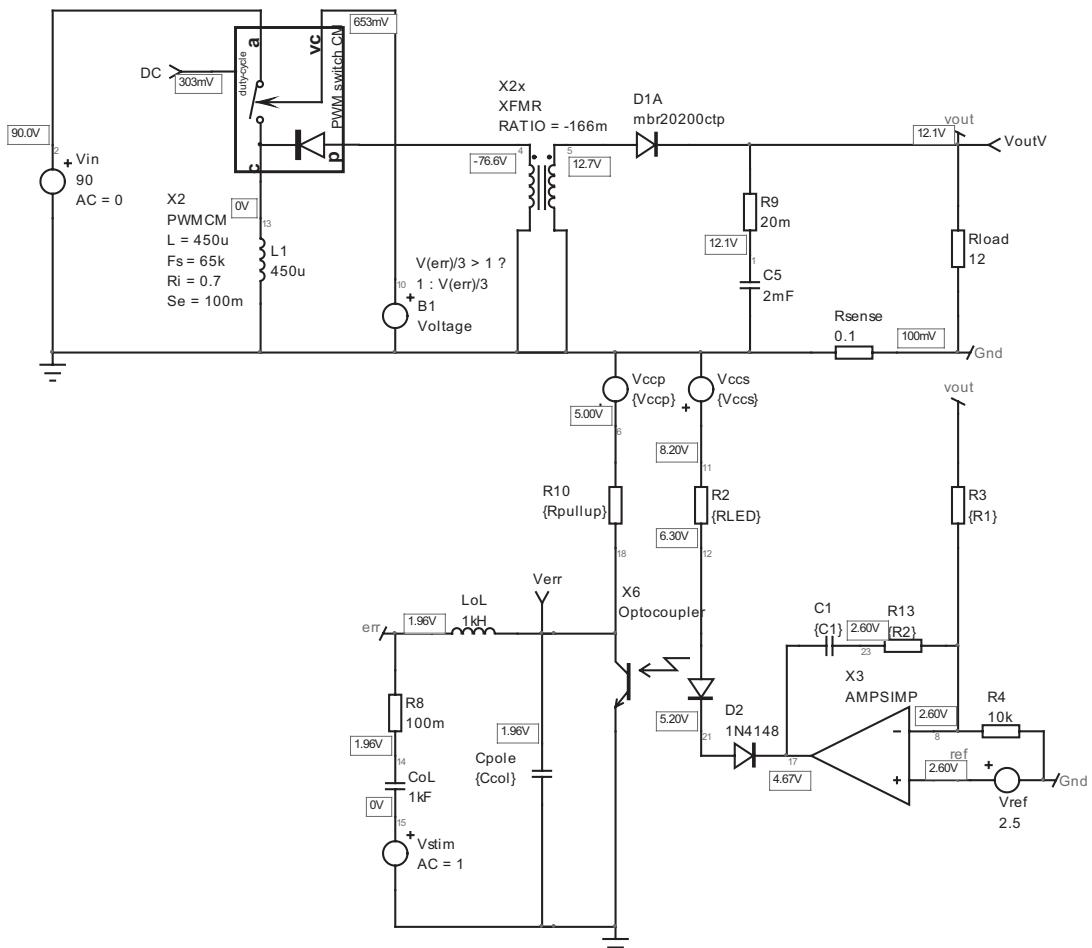


Figure 5.34 A simulation template helps us to check the final ac response once all components have been calculated. Here the voltage loop chain is not represented.

present at a 2.4-kHz frequency, as explained by (5.155). Where to place the zero in order to boost the phase by 52° at 400 Hz? As already explained in Chapter 4, we have

$$f_z = \frac{f_c}{\tan\left(\text{boost} + \tan^{-1}\left(\frac{f_c}{f_p}\right)\right)} = \frac{400}{\tan\left(52 + \tan^{-1}\left(\frac{400}{2.4k}\right)\right)} = 217 \text{ Hz} \quad (5.164)$$

Now using (5.146), we obtain

$$C_{20} = \frac{1}{2\pi f_z R_{20}} = \frac{1}{6.28 \times 217 \times 312k} = 2.35 \text{ nF} \quad (5.165)$$

That's it! We are all set now and can feed our simulation templates with the previously calculated values. This is what Figure 5.34 and Figure 5.35 show you.

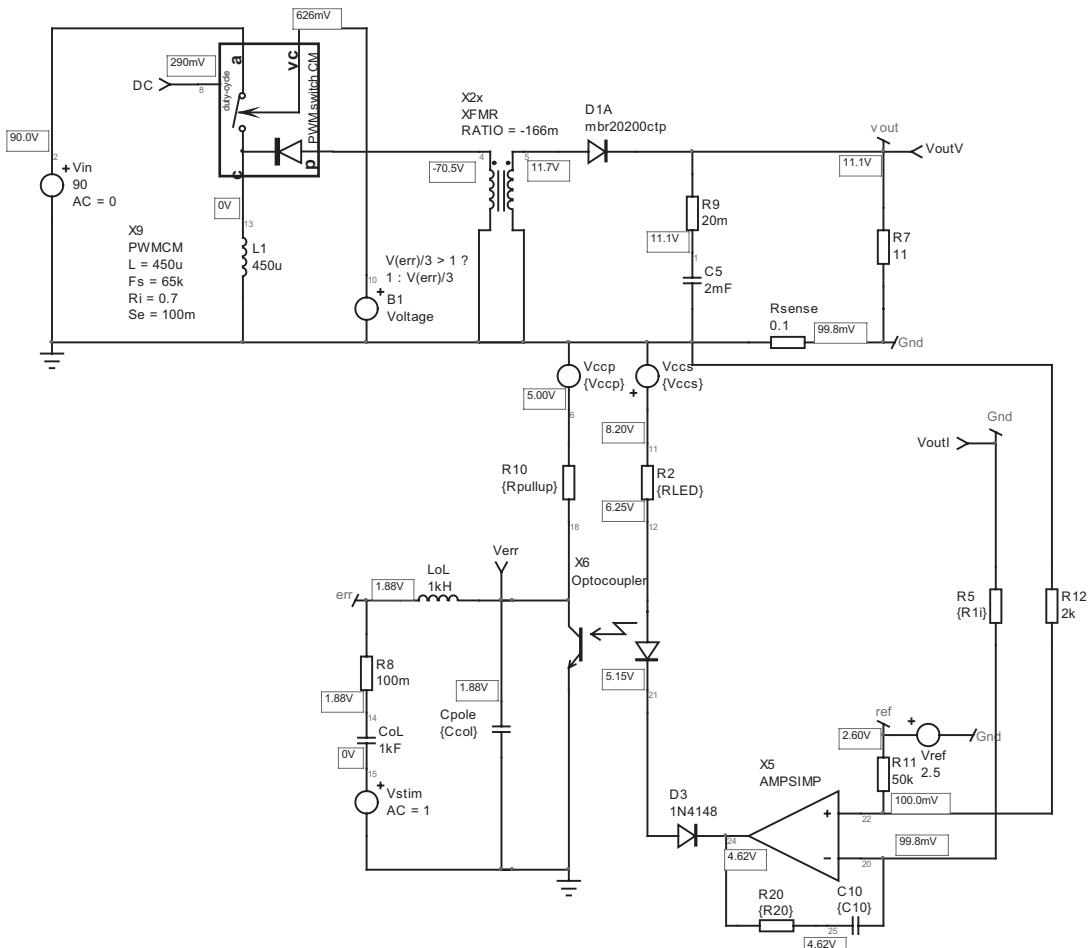


Figure 5.35 The current loop chain where the load is adjusted to consume 1 A, but V_{out} is slightly below the regulation point: this is the maximum output power.

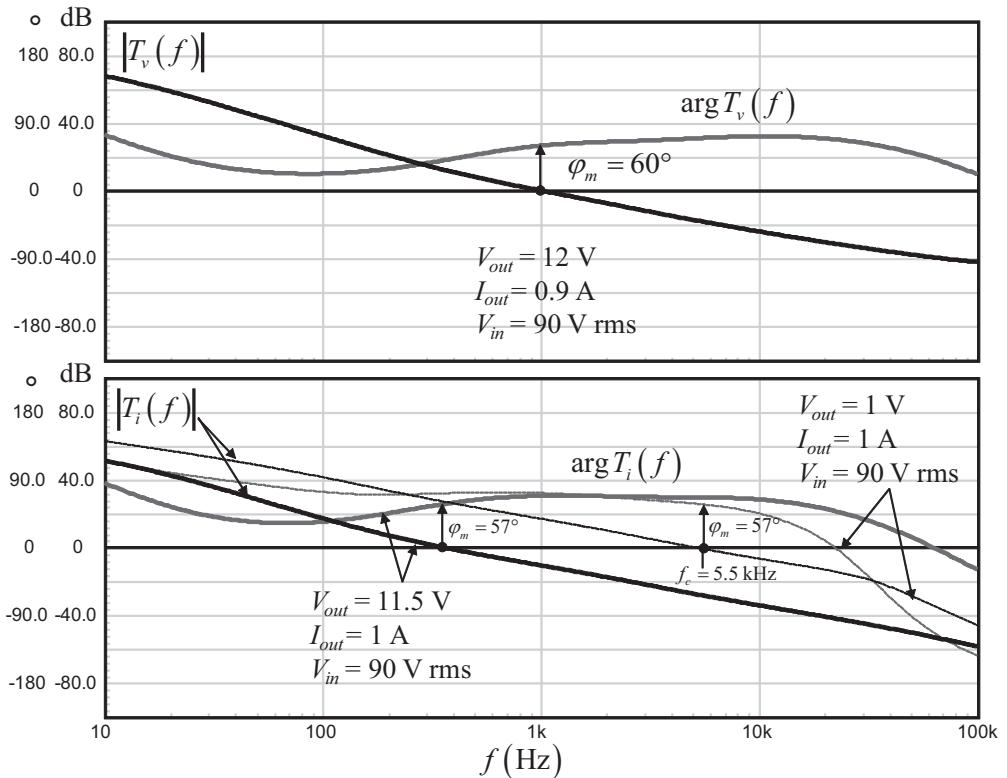


Figure 5.36 The loop gain response of both voltage and current lanes confirm the good choice of the compensation elements.

The complete open loop gain response for both chains appears in Figure 5.36 and confirms the pertinence of our compensation choices.

When the load resistance decreases in the constant-current section, the denominator of (5.138) goes down and the overall gain increases. As you can see in Figure 5.36, the loop gain of the current loop increases and extends the crossover to 5.5 kHz with a comfortable phase margin. The fact that we selected a lower bandwidth for the current loop compared to that of the voltage loop has naturally pushed the voltage-loop high-frequency pole away, leaving the current loop phase flat beyond 400 Hz. Thanks to this flat area and despite an increase in the crossover frequency, the phase margin in the current loop remains excellent.

We can now test the output voltage evolution versus the output current. This is what Figure 5.37 shows: we swept the output current while monitoring the output voltage. In the simulation tool, we simply replaced the load by a variable resistor and recorded both the output current and voltage. The graph testifies for an excellent transition between the two loops as I_{out} reaches 1 A.

There are several dedicated controllers for this type of constant-current/constant-voltage operation. ON Semiconductor offers the MC33341 or the NCP4300. One can also use a dual op amp like the LM358 to which a TL431 voltage reference is associated.

Whatever solution is used, you need to make sure the V_{cc} of these circuits always remains sufficient when V_{out} drops. Otherwise, troubles may occur when the

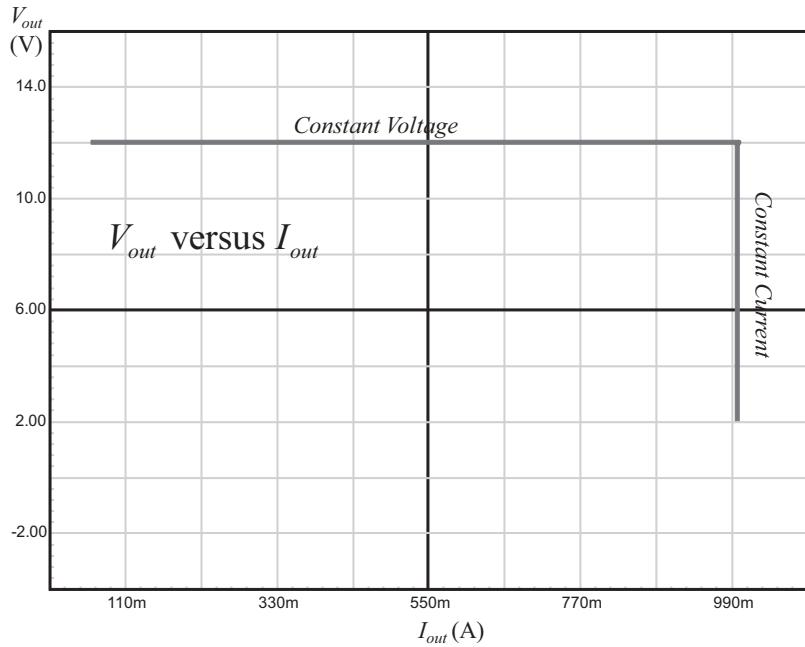


Figure 5.37 The output characteristics show a perfectly stable transition when I_{out} reaches 1A.

output voltage passes below the minimum operating voltage of these op amps. In a flyback converter application, one solution is to rotate the secondary-side rectifier as proposed in Figure 5.38 and observe that its cathode now swings to

$$V_k = V_{out} + NV_{in} \quad (5.166)$$

Therefore, when the output voltage disappears, NV_{in} is always there and supplies the op amp chain all the way down to a 0 V output. Unfortunately, the term NV_{in} can be significantly higher than the output voltage, in particular at the highest input line level. To cope with this large excursion, a simple regulator is implemented with a bipolar transistor Q_1 placed after a peak rectifying circuit (D_3C_1). To avoid an extra power dissipation when V_{out} is still present, let's say above 8 V, the Zener diode is selected such that Q_1 and D_1 are blocked when V_{out} is above 8 V. If we select an 8.2-V Zener diode, the voltage at D_1 cathode is roughly $8.2 - 2V_f \approx 6.9$ V. When V_{out} plunges below this value, D_2 blocks and the regulator supplies the op amp chain. If the Zener voltage is sufficiently well decoupled from V_{out} , it can be used to supply the LED current chain and become the V_{ccs} point in Figure 5.30. R_z in this case will supply the bipolar base current plus the LED bias current.

5.6 The Type 2: Pole and Zero are Coincident to Create an Isolated Type 1

There are cases where no phase boost is necessary, just a high dc gain and a simple -1 -slope to force a gain rolloff as the frequency increases. This is a simple integrator,

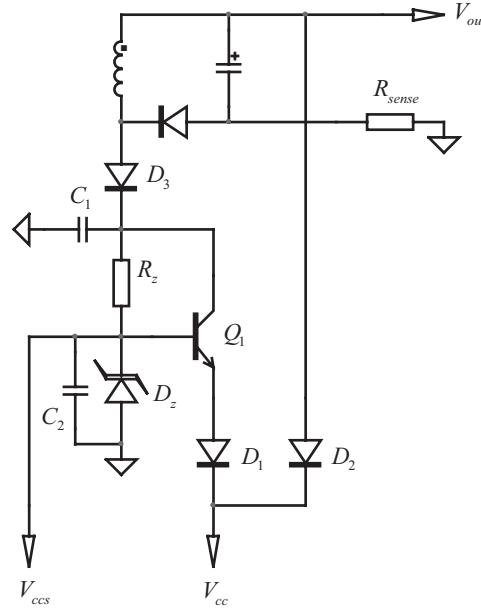


Figure 5.38 The rotation of the rectifier offers an easy means to self-supply the circuit despite the collapsing output voltage.

already identified as being a type 1 (see Section 5.1). An isolated type 2, in which both pole and zero coincide, can quickly be transformed into a type 1 compensator. However, we have seen before that the op amp pulling the LED cathode to ground (see Figure 5.21) is affected by a fast lane and sees its possible gain choices limited as shown with (5.104). The main offender in that case is the LED resistor, which combines a role in the bias point but also in the mid-band gain definition. However, in a type 1 configuration, there is no such thing as mid-band gain: the 0-dB crossover pole f_{po} is selected to force a crossover at the desired frequency f_c . To unveil the 0-dB crossover pole frequency, we will rearrange the original isolated type 2 definition given by (5.93):

$$G(s) = -\frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{1 + sR_1C_1}{sR_1C_1(1 + sR_{pullup}C_2)} = -\left(\frac{1}{s \frac{R_1R_{LED}}{R_{pullup}\text{CTR}} C_1} \right) \left(\frac{sR_1C_1 + 1}{1 + sR_{pullup}C_2} \right) \quad (5.167)$$

This equation can be put under the following form where the mid-band gain definition disappears:

$$G(s) = -\frac{1}{s/\omega_{po}} \frac{1 + s/\omega_z}{1 + s/\omega_p} \quad (5.168)$$

In this expression, we have

$$\omega_{po} = \frac{1}{\frac{R_1R_{LED}}{R_{pullup}\text{CTR}} C_1} \quad (5.169)$$

$$\omega_p = \frac{1}{R_{pullup}C_2} \quad (5.170)$$

$$\omega_z = \frac{1}{R_1C_1} \quad (5.171)$$

As both the pole and the zero are placed at a similar location, (5.170) and (5.171) must be equal:

$$\frac{1}{R_{pullup}C_2} = \frac{1}{R_1C_1} \quad (5.172)$$

Solving for C_1 :

$$C_1 = C_2 \frac{R_{pullup}}{R_1} \quad (5.173)$$

Now, substituting (5.173) into (5.169) and solving for C_2 , we find

$$C_2 = \frac{\text{CTR}}{2\pi f_{po} R_{LED}} \quad (5.174)$$

In the previous expression, the selection of R_{LED} will be dictated by bias considerations only, still using (5.103) for this purpose:

$$R_{LED,\max} = \frac{R_{pullup}(V_{out} - V_f - \text{VOL})\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} \quad (5.175)$$

The position of f_{po} depends on the wanted gain at crossover. Using (5.7) and (5.8), we can easily find its position:

$$f_{po} = f_c G \quad (5.176)$$

Once C_2 is found, (5.173) will lead to the value of C_1 . That's it—we have our type 1 in a pull-down type. Time to see a design example.

5.6.1 A Design Example

Suppose we need to create an attenuation of -20 dB at a 100-Hz crossover frequency without any phase boost. The design parameters are the following ones:

- $\text{VOL} = 0.2$ V; the op amp minimum output voltage.
- $V_f = 1$ V; the LED forward voltage.
- $V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.
- $V_{cc} = 5$ V; the primary-side pull-up V_{cc} level.
- $R_{pullup} = 20$ k Ω ; the optocoupler pull-up resistor.
- $\text{CTR}_{\min} = 0.3$; the minimum optocoupler current transfer ratio.
- $V_{out} = 12$ V; the converter output voltage.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 6 \text{ kHz}$; the optocoupler pole that has been characterized with R_{pullup} .

The maximum LED resistor value is computed using (5.175):

$$R_{LED,max} = \frac{R_{pullup}(V_{out} - V_f - VOL)CTR_{min}}{(V_{cc} - V_{CE,sat})} = \frac{20k \times (12 - 1 - 0.2) \times 0.3}{5 - 0.3} \approx 13.8 \text{ k}\Omega \quad (5.177)$$

Applying a design margin, we chose a 10-k Ω value. Now, applying (5.7) and (5.176), we first determine the position of the 0-dB crossover pole f_{po} :

$$f_{po} = f_c G = 100 \times 10^{-\frac{20}{20}} = 10 \text{ Hz} \quad (5.178)$$

Placing a pole at 10 Hz implies a fairly large capacitor value for C_2 using (5.174):

$$C_2 = \frac{CTR}{2\pi f_{po} R_{LED}} = \frac{0.3}{6.28 \times 10 \times 10k} = 477 \text{ nF} \quad (5.179)$$

C_1 comes easily with (5.173):

$$C_1 = C_2 \frac{R_{pullup}}{R_1} = 477n \times \frac{20k}{38k} = 251 \text{ nF} \quad (5.180)$$

parameters

```
Vout=12
Rupper=(Vout-2.5)/250u
fc=100
```

```
Gfc=20
```

```
G=10^(-Gfc/20)
pi=3.14159
```

```
VOL=0.2
```

```
VCEsat=0.3
```

```
Vdd=5
```

```
Vf=1
```

```
A=Vout-Vf-VOL
```

```
B=Vdd-VCEsat
```

```
Rmax=(A/B)*Rpullup*CTR
```

```
RLED=10k
```

```
Rpullup=20k
```

```
C2=CTR/(2*pi*fpo*RLED)
```

```
C1=C2*Rpullup/Rupper
```

```
Ccopt=C2-Copto
```

```
Fopto=6k
```

```
Copto=1/(2*pi*fopto*Rpullup)
```

```
CTR = 0.3
```

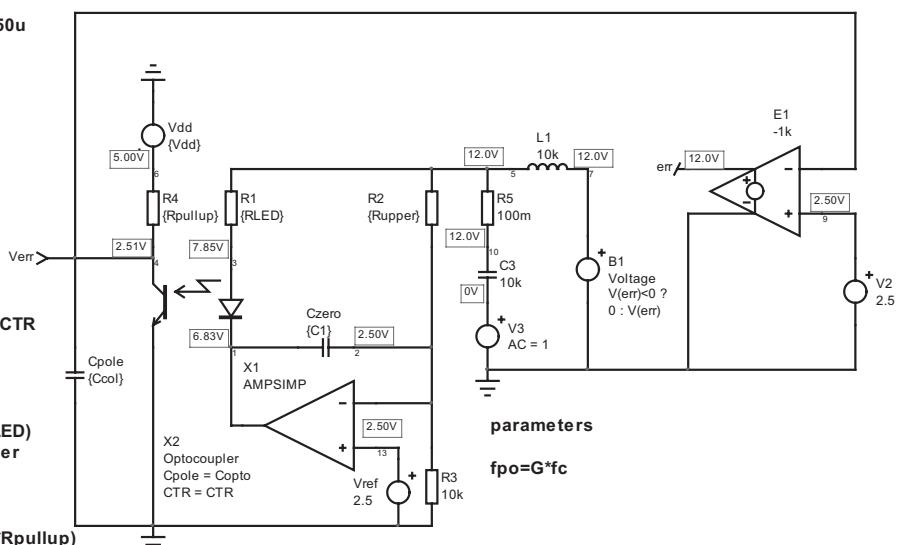


Figure 5.39 The isolated type 1 is formed by making the pole and the zero coincide. The LED resistor is calculated for bias purposes only.

The optocoupler parasitic capacitance is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} = 1.3 \text{ nF} \quad (5.181)$$

Subtracted from C_2 , the final capacitor C_{col} will be 475 nF or a normalized 0.47 μF . Now that we are all set, we can simulate the structure as demonstrated by Figure 5.39.

The results appear in Figure 5.40 and confirm the 20-dB attenuation at 10 Hz.

5.7 The Type 2: A Slightly Different Arrangement

In some cases, when the selected crossover frequency is low, with the help of their large values, the charging times of C_2 and C_1 create a natural soft-start effect: the error amplifier output slowly rises up and limits the power-on stress such as peak power dissipation in the switches. In a power factor corrector (PFC) circuit, it usually contributes to calm down the output overshoot. However, in a classical type 2 configuration, the charging capacitor is split between C_2 and C_1 , with a resistor R_2 in series for C_1 . In some high-power converters, the soft-start duration might not be long enough, despite large capacitor values. How could we keep the same crossover frequency and fully capitalize on the presence of these large capacitors? Thanks to a discussion initiated by my colleague Mr. Jim Young from ON Semiconductor, I found that a different arrangement was possible. Before unveiling it, let's understand the phenomenon in play at start-up.

At power up, as no output voltage exists on the converter output, the op amp pushes its output to the maximum. However, it quickly finds a limit as the voltage on its inverting pin immediately builds up to the reference voltage present on its noninverting input. This is because with both capacitors being discharged, the op amp output current crosses them and enters the divider bridge, imposing a “regulated” voltage on the inverting pin as any op amp should do. Therefore, rather than immediately delivering the full control to the control pin, the error voltage slowly rises, depending on the capacitor values and the current authorized by the resistors

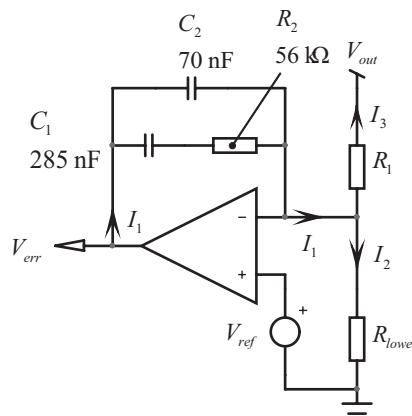


Figure 5.40 These ac results show the correct attenuation value at 100 Hz.

bridge. Figure 5.41 shows how the various currents split in the circuit during the startup sequence as V_{out} is null.

From this representation, we can write a few simple electrical laws:

$$I_2 = I_1 - I_3 = \frac{V_{ref}}{R_{lower}} \quad (5.182)$$

$$I_3 = \frac{V_{ref} - V_{out}}{R_1} \quad (5.183)$$

By substituting (5.183) into (5.182) and solving for the charging current $i_1(t)$, we have

$$i_1(t) = \frac{V_{ref}}{R_{lower}} + \frac{V_{ref} - v_{out}(t)}{R_1} \quad (5.184)$$

At startup, as $v_{out}(t)$ is zero, this equation can be arranged as

$$I_1 = \frac{V_{ref}}{R_{lower}} + \frac{V_{ref}}{R_1} = \frac{V_{ref}}{R_{lower} \parallel R_1} \quad (5.185)$$

In PFCs, R_1 is much larger than R_{lower} and the charging current simplifies to

$$I_1 \approx \frac{V_{ref}}{R_{lower}} \quad (5.186)$$

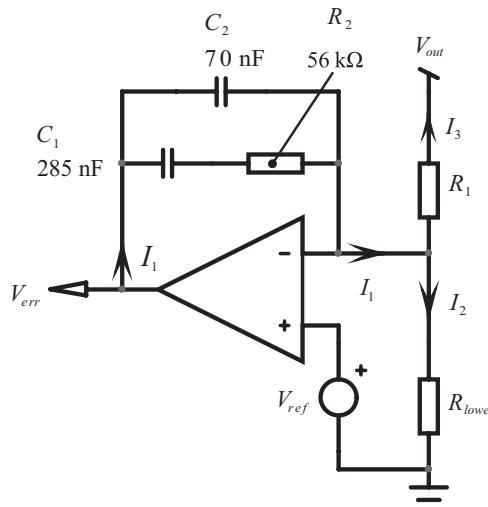


Figure 5.41 The op amp output voltage rise is not limited by the op amp output current capability but rather by the reference pin and the bottom resistor R_{lower}

This current splits between C_2 and C_1 , this latter being in series with the resistor R_2 . The current has the choice between a short-circuit (C_2 is discharged) and a resistive path (C_1 discharged plus R_2), and most of the charging current flows within C_2 , which is quickly charged by the current defined by (5.185). Powering Figure 5.41 configuration gives a linearly rising waveform, as Figure 5.42 confirms. It takes 1.2 ms before the converter can deliver its full power after the power-on sequence. For some PFC, this natural delay is not enough and cannot tame the output overshoot.

In the previous equations, the presence of R_2 prevents the current from immediately charging C_1 . Why not change the configuration where C_2 would stay alone, and have the R_2C_1 network go over the upper resistor R_1 ? This is exactly what Figure 5.43 suggests.

The set of equations differs a little from what has been previously derived, but the spirit remains the same:

$$\frac{Z_f}{Z_i} = \frac{\frac{1}{sC_2}}{\left(\frac{1}{sC_1} + R_2\right) \| R_1} \quad (5.187)$$

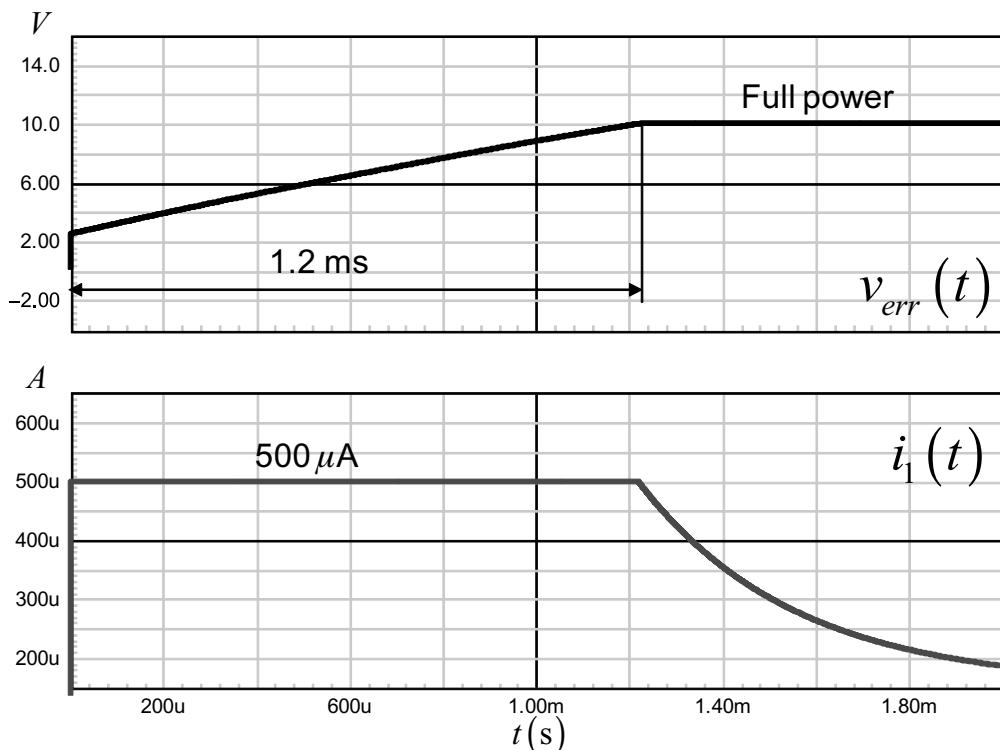


Figure 5.42 Despite a large capacitive value across the op amp (C_1 and C_2) value, the 500- μ A charging current quickly brings the op amp output voltage up to its maximum level.

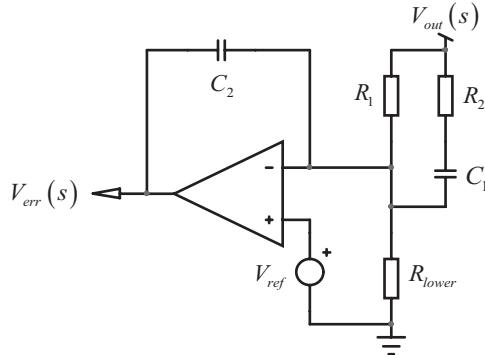


Figure 5.43 By moving the RC network across the upper resistor, the charging time is increased, providing additional free soft-start.

Developing and rearranging (5.187), we have

$$G(s) = -\frac{C_1(R_1 + R_2)}{R_1 C_2} \frac{\left(1 + \frac{1}{s(R_1 + R_2)C_1}\right)}{1 + sR_2 C_1} \quad (5.188)$$

In the previous equation, the pole, zero, and mid-band gain are immediately identified:

$$G_0 = \frac{R_1 + R_2}{R_1} \frac{C_1}{C_2} \quad (5.189)$$

$$\omega_z = \frac{1}{(R_2 + R_1)C_1} \quad (5.190)$$

$$\omega_p = \frac{1}{R_2 C_1} \quad (5.191)$$

From the previous definition, we can extract the component values we are looking for:

$$C_1 = \frac{1}{2\pi f_z (R_1 + R_2)} \quad (5.192)$$

$$C_2 = \frac{1}{2\pi f_z G_0 R_1} \quad (5.193)$$

$$R_2 = \frac{R_1 f_z}{f_p - f_z} \quad (5.194)$$

In (5.16), we have seen that the pole position was dependent upon R_2 but also the sum of C_1 and C_2 . As in (5.191) the pole location now solely depends on C_2 , for a similar pole position imposed in either Figure 5.5 or in Figure 5.43, C_2 in the

second case will be much larger than in the first. Therefore, as the entire current defined by (5.185) will cross it at startup, we can expect a longer charging time than with the traditional type 2 configuration.

To verify this assumption, we have assembled a front-end power factor corrector averaged circuit whose return loop is made either by the classical type 2 approach (Figure 5.5) or by the rearranged configuration as in Figure 5.43. The schematic of the test fixture appears in Figure 5.44.

In this example, we have automated the calculations of the type 2 classical (R_2 , C_2 , and C_1) definitions and the proposed variation (R_{20} , C_{20} , and C_{10}). Then, we performed a startup sequence followed by a load step transition imposed by the output switch X_4 . The pole and zero are, respectively, positioned at 61 Hz and 6.5 Hz. For the first case, Figure 5.5, C_1 equals 148 nF and C_2 is 16 nF. As expected, for a similar pole position, the second configuration (Figure 5.43) leads to a C_2 value of 154 nF, the sum of the previous C_1-C_2 values.

The waveforms collected in both configurations appear in Figure 5.45. The first configuration shows a rather fast output voltage rise $v_{out1}(t)$, affected by a 30-V overshoot. On the bottom of the simulation shot, the error voltage exhibits a sharp transition with almost no delay: the power is pushed to the maximum right after power-on. On the contrary, when the second configuration is tested, the output voltage settlement is much smoother and the overshoot is gone. This is testified by the observation of the error amplifier output showing an improved soft-start effect, due to the charging of the large capacitor C_2 , now alone across the op amp output and inverting input. The transient response implemented shortly after the startup period shows similar responses with either options, confirming similar ac loop gain and phase.

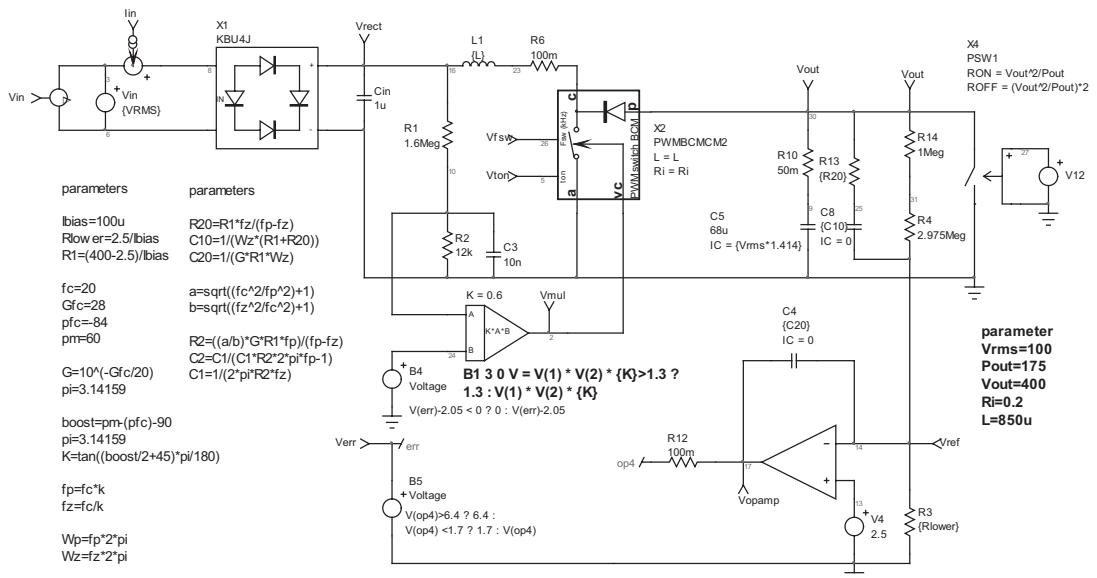


Figure 5.44 A classical PFC preconverter powered by a peak-current-mode controller, the MC33262.

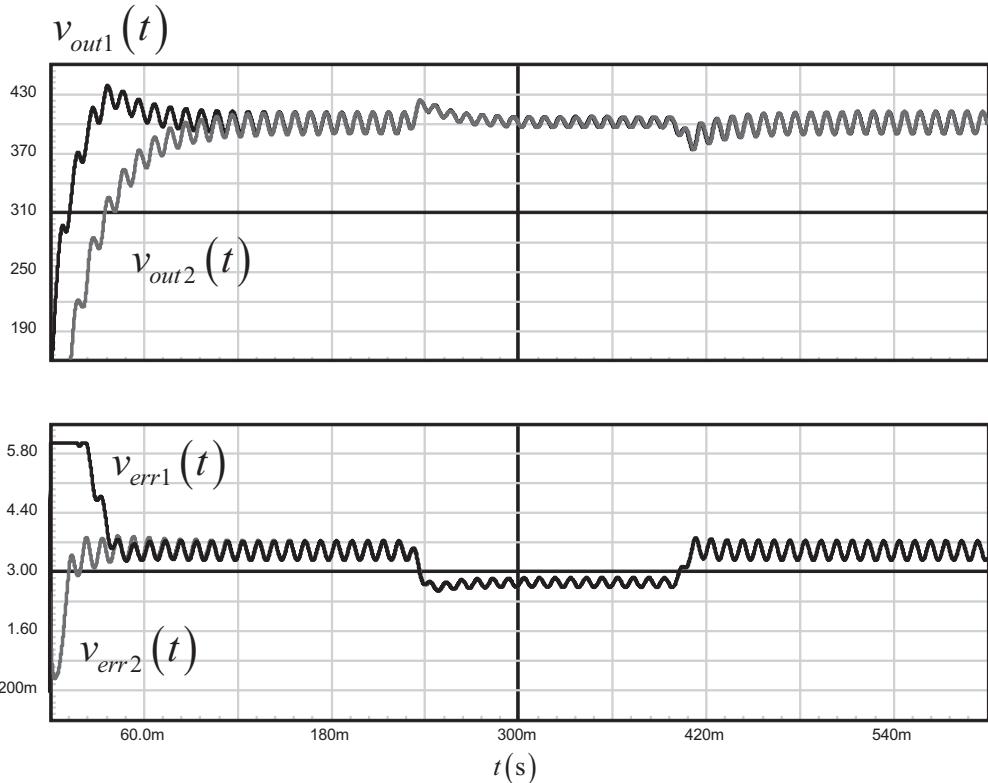


Figure 5.45 The results show the absence of overshoot in the adopted type 2 variation but a similar transient response, implying that both compensators position the poles and zeros at the exact same place.

5.8 The Type 3: An Origin Pole, a Pole/Zero Pair

The type 3 compensator is used when more than 90° of phase boost are necessary. By adding another zero/pole pair to the type 2 circuit, the type 3 can theoretically boost the phase up to 180° . Its architecture appears in Figure 5.46. The derivation of its transfer function does not really change; the principle remains the same: calculate the equivalent impedance Z_f placed across the op amp, and divide it by that of Z_i to further rearrange the equation:

$$Z_f = \left(\frac{1}{sC_1} + R_2 \right) \frac{1}{sC_2} \Big/ \left(\frac{1}{sC_1} + R_2 \right) + \frac{1}{sC_2} \quad (5.195)$$

$$Z_i = \left(\frac{1}{sC_3} + R_3 \right) R_1 \Big/ \left(\frac{1}{sC_3} + R_3 \right) + R_1 \quad (5.196)$$

Then, when dividing (5.195) by (5.196), we have

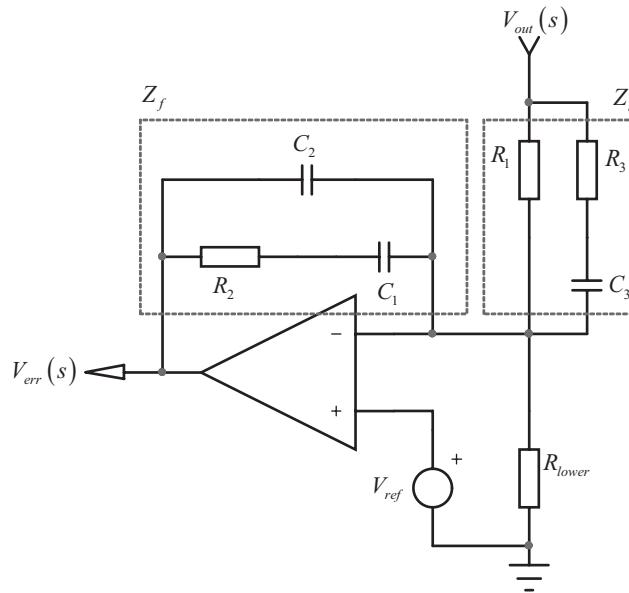


Figure 5.46 The type 3 compensator can boost the phase up to 180°.

$$\frac{Z_f}{Z_i} = G(s) = \frac{\left(\frac{1}{sC_1} + R_2\right)\frac{1}{sC_2}}{\left(\frac{1}{sC_3} + R_3\right)R_1} \Bigg/ \frac{\left(\frac{1}{sC_1} + R_2\right) + \frac{1}{sC_2}}{\left(\frac{1}{sC_3} + R_3\right) + R_1} \quad (5.197)$$

By factoring sR_2C_1 , we obtain a more familiar expression:

$$G(s) = -\frac{R_2C_1}{R_1(C_1 + C_2)} \frac{\frac{1}{sR_2C_1} + 1}{1 + sR_2 \frac{C_1C_2}{C_1 + C_2}} \frac{sC_3(R_1 + R_3) + 1}{sR_3C_3 + 1} \quad (5.198)$$

This expression can be put under the normalized form:

$$G(s) = -G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right) \left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)} \quad (5.199)$$

where

$$G_0 = \frac{R_2}{R_1} \frac{C_1}{C_1 + C_2} \quad (5.200)$$

$$\omega_{z_1} = \frac{1}{R_2C_1} \quad (5.201)$$

$$\omega_{z_2} = \frac{1}{(R_1 + R_3)C_3} \quad (5.202)$$

$$\omega_{p_1} = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \quad (5.203)$$

$$\omega_{p_2} = \frac{1}{R_3 C_3} \quad (5.204)$$

In the previous expressions, we have two zeros and two poles. They both can be coincident or spread apart of each other's. The design of such a compensator starts with the value of the series resistor R_2 . To find it, we must derive the magnitude of $G(s)$ via its definition in (5.199):

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} = \frac{R_2 C_1}{R_1 (C_1 + C_2)} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (5.205)$$

By extracting C_1 and C_2 from (5.201) and (5.203), substituting them into (5.205) then solving for R_2 , we have

$$R_2 = \frac{GR_1 f_{p_1}}{f_{p_1} - f_{z_1}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (5.206)$$

The rest of the elements comes out easily:

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad (5.207)$$

$$C_2 = \frac{C_1}{2\pi f_{p_1} C_1 R_2 - 1} \quad (5.208)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_{upper} f_{p_2} f_{z_2}} \quad (5.209)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} \quad (5.210)$$

In most of the applications, capacitor C_2 is much smaller than C_1 , and resistor R_3 is also smaller than R_1 . Therefore, the transfer equation (5.198) simplifies to

$$G(s) \approx -\frac{R_2}{R_1} \frac{\frac{1}{sR_2C_1} + 1}{1 + sR_2C_2} \frac{sC_3R_1 + 1}{sR_3C_3 + 1} = -G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right) \left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)} \quad (5.211)$$

where

$$G_0 = \frac{R_2}{R_1} \quad (5.212)$$

$$\omega_{z_1} = \frac{1}{R_2C_1} \quad (5.213)$$

$$\omega_{z_2} = \frac{1}{R_1C_3} \quad (5.214)$$

$$\omega_{p_1} = \frac{1}{R_2C_2} \quad (5.215)$$

$$\omega_{p_2} = \frac{1}{R_3C_3} \quad (5.216)$$

The magnitude expression of the simplified type 3 now becomes

$$|G(f_c)| = \frac{R_2}{R_1} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (5.217)$$

From which the value of R_2 can also be extracted:

$$R_2 = G R_1 \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (5.218)$$

In (5.218) and (5.206), the term G represents the needed gain or attenuation at the selected crossover frequency and already defined by (5.7).

The expression of a type 3 configuration can be put under the following simple form:

$$G(s) = \frac{N(s)}{D(s)} \quad (5.219)$$

The argument of (5.219) is thus

$$\arg G(s) = \arg N(s) - \arg D(s) \quad (5.220)$$

In other words,

$$\arg N(j\omega) = \arg\left(-1 + j\frac{\omega_{z_1}}{\omega}\right) + \arg\left(1 + j\frac{\omega}{\omega_{z_2}}\right) \quad (5.221)$$

$$\arg D(j\omega) = \arg\left(1 + j\frac{\omega}{\omega_{p_1}}\right) + \arg\left(1 + j\frac{\omega}{\omega_{p_2}}\right) \quad (5.222)$$

Subtracting (5.222) from (5.221), we have

$$\arg G(j\omega) = \arg\left(-1 + j\frac{\omega_{z_1}}{\omega}\right) + \arg\left(1 + j\frac{\omega}{\omega_{z_2}}\right) - \arg\left(1 + j\frac{\omega}{\omega_{p_1}}\right) - \arg\left(1 + j\frac{\omega}{\omega_{p_2}}\right) \quad (5.223)$$

Solving the above leads to

$$\arg G(f) = \pi - \tan^{-1}\left(\frac{f_{z_1}}{f}\right) + \tan^{-1}\left(\frac{f}{f_{z_2}}\right) - \tan^{-1}\left(\frac{f}{f_{p_1}}\right) - \tan^{-1}\left(\frac{f}{f_{p_2}}\right) \quad (5.224)$$

In dc, because of the origin pole and the op amp inversion, the phase lags by

$$\lim_{f \rightarrow 0} \arg G(f) = \pi - \tan^{-1}(\infty) + \tan^{-1}(0) - 2\tan^{-1}(0) = \pi - \frac{\pi}{2} = \frac{\pi}{2} \text{ or } -270^\circ \quad (5.225)$$

The phase boost at the crossover frequency f_c , is simply $\arg G(f_c) - \frac{\pi}{2}$. In other words, for our type 3 compensator, the phase boost alone is

$$boost = \frac{\pi}{2} - \tan^{-1}\left(\frac{f_{z_1}}{f_c}\right) + \tan^{-1}\left(\frac{f_c}{f_{z_2}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p_1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p_2}}\right) \quad (5.226)$$

In the previous expression, the term $\frac{\pi}{2} - \tan^{-1}\left(\frac{f_{z_1}}{f_c}\right)$ is simply $\tan^{-1}\left(\frac{f_c}{f_{z_1}}\right)$ so

$$boost = \tan^{-1}\left(\frac{f_c}{f_{z_1}}\right) + \tan^{-1}\left(\frac{f_c}{f_{z_2}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p_1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p_2}}\right) \quad (5.227)$$

It is important to note that in the previous formulas, the poles and zeros can be coincident or not; you can equally apply the given definitions by having $f_{p_1} = f_{p_2}$ / $f_{z_1} = f_{z_2}$ or $f_{p_1} \neq f_{p_2}$ / $f_{z_1} \neq f_{z_2}$.

5.8.1 A Design Example

In this example, we will design a type 3 compensator providing a 10-dB attenuation at 5 kHz together with a 145° phase boost. First, let us translate the 10-dB attenuation into a unit less value:

$$G = 10^{-\frac{10}{20}} = 316m \quad (5.228)$$

The next step is to place the poles and zeros to offer the desired 145° local boost at 5 kHz. From the previous chapters, we know how to position a double pole in relationship to the crossover frequency and the required phase boost:

$$f_{p_{1,2}} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{5k}{\tan\left(45 - \frac{145}{4}\right)} = \frac{5k}{154m} \approx 32.5 \text{ kHz} \quad (5.229)$$

The double zero is classically defined by remembering that the peak in phase boost occurs at the geometric mean between the double coincident pole/zero pair:

$$f_{z_{1,2}} = \frac{f_c^2}{f_{p_{1,2}}} = \frac{25k}{32.5k} \approx 769 \text{ Hz} \quad (5.230)$$

From (5.206), we can calculate the value of R_2 , assuming an upper resistor R_1 of 10 kΩ.

$$R_2 = \frac{316m \times 10k \times 32.5k}{32.5k - 769} \frac{\sqrt{1 + \left(\frac{5k}{32.5k}\right)^2} \sqrt{1 + \left(\frac{5k}{32.5k}\right)^2}}{\sqrt{1 + \left(\frac{769}{5k}\right)^2} \sqrt{1 + \left(\frac{5k}{769}\right)^2}} = 498 \Omega \quad (5.231)$$

The rest of the elements comes out easily:

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} = \frac{1}{6.28 \times 769 \times 498} = 416 \text{ nF} \quad (5.232)$$

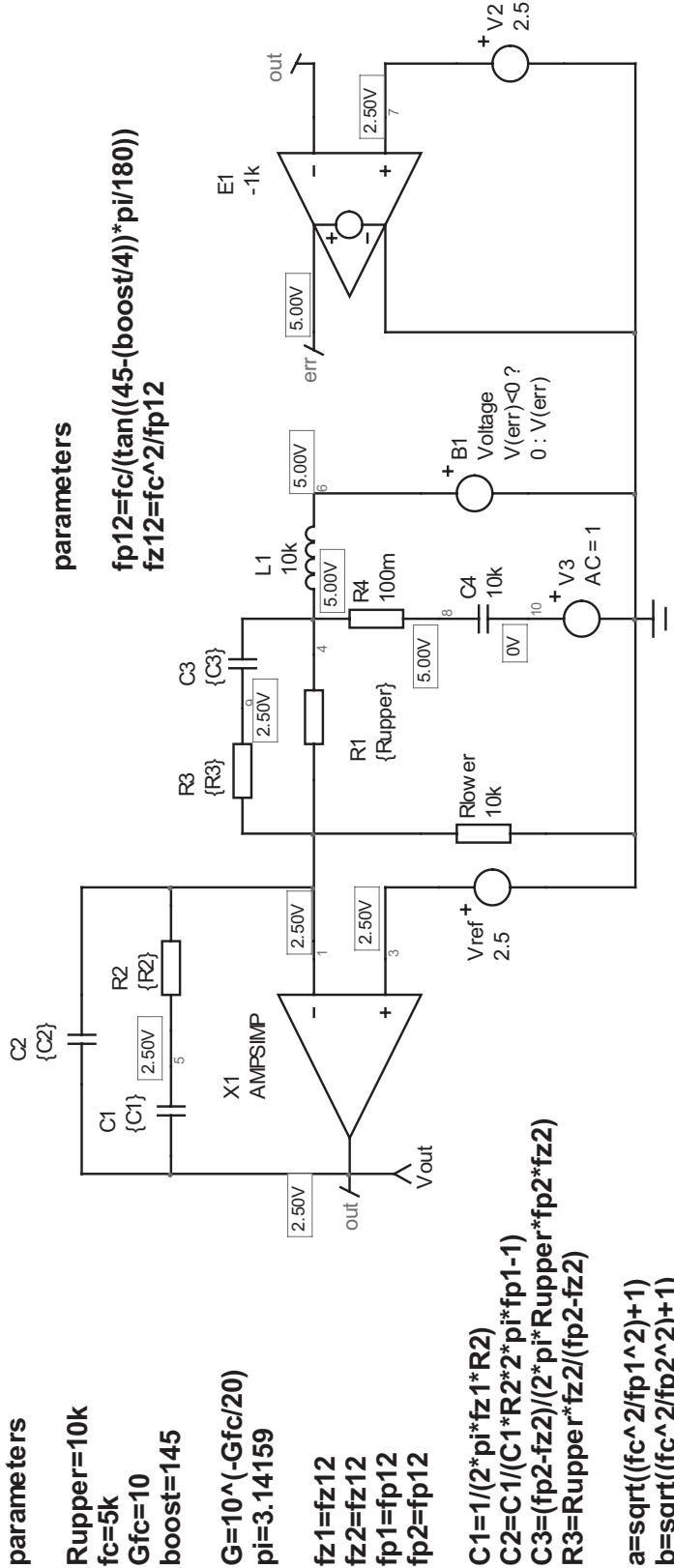
$$C_2 = \frac{C_1}{2\pi f_{p_1} C_1 R_2 - 1} = \frac{416n}{6.28 \times 32.5k \times 416n \times 498 - 1} = 10 \text{ nF} \quad (5.233)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_{upper} f_{p_2} f_{z_2}} = \frac{32.5k - 769}{6.28 \times 10k \times 32.5k \times 769} = 20 \text{ nF} \quad (5.234)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} = \frac{10k \times 769}{32.5k - 769} = 242 \Omega \quad (5.235)$$

As usual, we have captured an automated type 3 simulation fixture as shown in Figure 5.47.

In the simulation examples, the poles and zeros are coincident, but nothing would prevent us from entering separate values for each of them. The simulation results appear in Figure 5.48 and confirm our calculations.



$$\begin{aligned}
 C1 &= 1/(2 * \pi * fz1 * R2) \\
 C2 &= C1 * (C1 * R2 * 2 * \pi * fp1 - 1) \\
 C3 &= (fp2 * fz2) / (2 * \pi * Rupper * fp2 * fz2) \\
 R3 &= Rupper * fz2 / (fp2 - fz2)
 \end{aligned}$$

$$\begin{aligned}
 a &= \sqrt{(fc^2 / fp1^2) + 1} \\
 b &= \sqrt{(fc^2 / fp2^2) + 1} \\
 c &= \sqrt{(fz1^2 / fc^2) + 1} \\
 d &= \sqrt{(fc^2 / fz2^2) + 1}
 \end{aligned}$$

$$R2 = ((a * b * (c * d)) / (fp1 - fz1)) * Rupper * G * fp1$$

Figure 5.47 An automated type 3 simulation fixture calculates the component values for us.

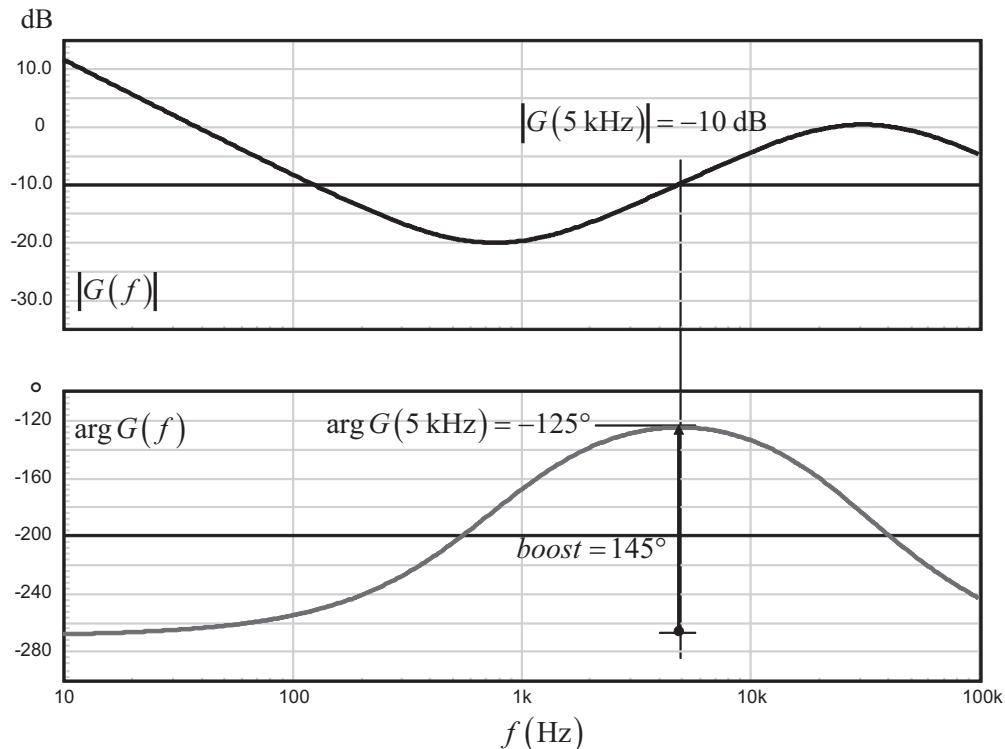


Figure 5.48 The ac simulation results of the type 3 compensator, confirming the 10-dB attenuation at 5 kHz.

5.9 The Type 3: Isolation with an Optocoupler

The isolated type 3 finds application in converters where a large phase boost is needed. This is the case for the voltage-mode buck-derived converters such as forward or push-pull types. The resonant poles must be damped, and the designer usually places a double zero right at the resonant peak to force a crossover with a -1 -slope. Let's discover the various ways of wiring a type 3 with an optocoupler.

5.9.1 Optocoupler and Op Amp: The Direct Connection, Common Collector

The type 3 compensator is often used in voltage-mode forward converters, where the peaking of the LC network requires the placement of a double zero at the resonant frequency. Therefore, in isolated versions, it requires a connection to an opto-isolator, ending up again in various possible configurations. The first one is the direct link of the op amp output to the LED anode, as already discovered in the type 2 section. Such a configuration appears in Figure 5.49.

The type 3 compensator around the op amp has been transformed into a kind of type 3a, where the second pole brought by C_2 has been removed and moved to the optocoupler block. This change helps to include the optocoupler in the loop and

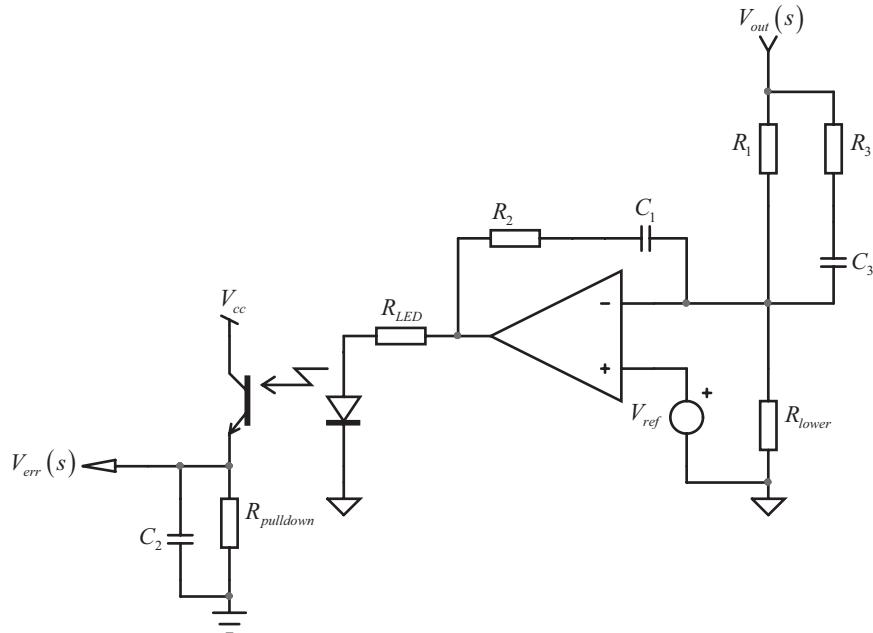


Figure 5.49 The op amp output of a type 3 configuration can directly drive the LED anode of the optocoupler.

also improves the noise immunity at the chain end. From the previous studies, it is possible to derive the compensator gain as follows:

$$G(s) = -\text{CTR} \frac{R_{\text{pulldown}}}{R_{\text{LED}}} \frac{R_2}{R_1} \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_3C_3} \frac{1 + sC_3[R_1 + R_3]}{1 + sR_{\text{pulldown}}C_2} = -G_1 G_2 \frac{\left(1 + \frac{\omega_{z1}}{s}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (5.236)$$

where

$$G_1 = \text{CTR} \frac{R_{\text{pulldown}}}{R_{\text{LED}}} \quad (5.237)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.238)$$

$$\omega_{z1} = \frac{1}{R_2 C_1} \quad (5.239)$$

$$\omega_{z2} = \frac{1}{(R_1 + R_3)C_3} \quad (5.240)$$

$$\omega_{p1} = \frac{1}{R_3 C_3} \quad (5.241)$$

$$\omega_{p_2} = \frac{1}{R_{pulldown} C_2} \quad (5.242)$$

The definition for R_2 derived in (5.218) is still valid for this architecture:

$$R_2 = \frac{G}{G_1} R_1 \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (5.243)$$

In the previous expression, the term G/G_1 accounts for the optocoupler presence and its own network gain G_1 as described in (5.237). G is the total necessary gain or attenuation at crossover as described by (5.7). The rest of the element values is found using a system of equations involving (5.243), (5.239), (5.240), and (5.241):

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad (5.244)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pulldown}} \quad (5.245)$$

$$C_3 = \frac{f_{p_1} - f_{z_2}}{2\pi R_{upper} f_{p_1} f_{z_2}} \quad (5.246)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_1} - f_{z_2}} \quad (5.247)$$

5.9.2 A Design Example

Suppose we want to create an isolated 10-dB amplification at 1 kHz, together with a 110° phase boost at this frequency. The design parameters are the following ones:

$V_{OH} = 10$ V; the op amp maximum output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$R_{pulldown} = 1$ kΩ; the optocoupler pull-up resistor.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 10$ kΩ; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 15$ kHz; the optocoupler pole that has been characterized with $R_{pulldown}$.

Given the 110° phase boost at 1 kHz, we first assume to place coincident poles and zeros at a place to be determined. Capitalizing on what has already been derived, we will place a pole pair at the following position:

$$f_{p_{1,2}} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{1k}{315m} \approx 3.2 \text{ kHz} \quad (5.248)$$

The double zero will be located at

$$f_{z_{1,2}} = \frac{f_c^2}{f_p} = \frac{1k}{3.2k} \approx 312 \text{ Hz} \quad (5.249)$$

Then, with the pole and zero position being defined, we carry on by defining the upper limit for the LED resistor. This resistor ensures that the feedback voltage will always be able to swing up to a voltage close to $V_{cc} - V_{CE,sat}$, despite the minimum CTR of the optocoupler and the op amp output upper stop. This equation has already been derived in (5.73):

$$R_{LED,\max} = \frac{R_{pulldown}(V_{OH} - V_f)\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} = \frac{1k(10 - 1)}{5 - 0.3} \cdot 0.8 = 1.5 \text{ k}\Omega \quad (5.250)$$

Adopting a 20 percent safety margin and choosing a normalized value, we finally adopt $R_{LED} = 1.2 \text{ k}\Omega$. With this resistor known, we can evaluate the gain brought by the optocoupler chain alone and defined by

$$G_1 = \frac{R_{pulldown}}{R_{LED}} \text{CTR}_{\min} = \frac{1k}{1.2k} \cdot 0.8 = 0.666 \quad (5.251)$$

Thanks to (5.243), the value for R_2 is obtained:

$$R_2 = \frac{G}{G_1} R_1 \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} = \frac{10^{\frac{10}{20}}}{0.666} 10k \frac{\sqrt{1 + \left(\frac{1k}{3.2k}\right)^2} \sqrt{1 + \left(\frac{1k}{3.2k}\right)^2}}{\sqrt{1 + \left(\frac{312}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{312}\right)^2}} \approx 15 \text{ k}\Omega \quad (5.252)$$

We are now ready to evaluate the rest of the components using (5.244) through (5.247):

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} = \frac{1}{6.28 \times 312 \times 15k} = 34 \text{ nF} \quad (5.253)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pulldown}} = \frac{1}{6.28 \times 3.2k \times 1k} \approx 50 \text{ nF} \quad (5.254)$$

$$C_3 = \frac{f_{p1} - f_{z2}}{2\pi R_1 f_{p1} f_{z2}} = \frac{3.2k - 312}{6.28 \times 10k \times 3.2k \times 312} \approx 46 \text{ nF} \quad (5.255)$$

$$R_3 = \frac{R_1 f_{z2}}{f_{p1} - f_{z2}} = \frac{10k \times 312}{3.2k - 312} = 1.08 \text{ k}\Omega \quad (5.256)$$

The capacitor put across the optocoupler, in total, must equal 50 nF (C_2). The optocoupler pole is located at 15 kHz. Given a pull-down resistor of 1 k Ω , we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pulldown}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6 \text{ nF} \quad (5.257)$$

When subtracted from (5.254), you obtain the value for C_{col} , the final capacitor installed across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 50n - 10.6n \approx 39 \text{ nF} \quad (5.258)$$

We are all set now. We can capture Figure 5.49, automate its bias point with a simple op amp, E_1 , and then run a simulation. This what we propose in Figure 5.50.

The ac results appear in Figure 5.51 and agree very well with the calculations.

5.9.3 Optocoupler and Op Amp: The Direct Connection, Common Emitter

There are some cases where the control law polarity does not suit the converter control circuitry, and the direct connection of the op amp to the optocoupler does not work. As we already introduced with the type 2 configuration, an option consists of placing the optocoupler loading resistor in the collector rather than in the emitter (see Figure 5.52).

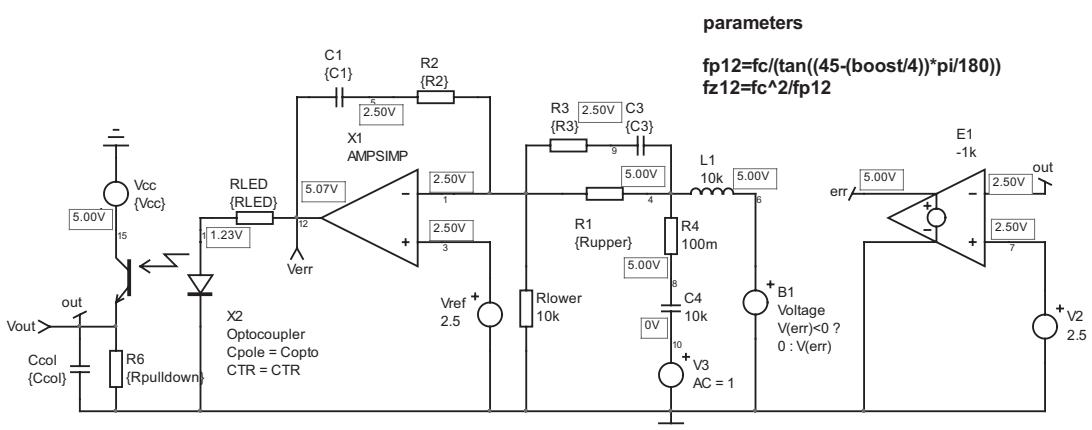


Figure 5.50 The simulation fixture includes an automated bias point adjustment. The elements are also automatically computed (not shown here).

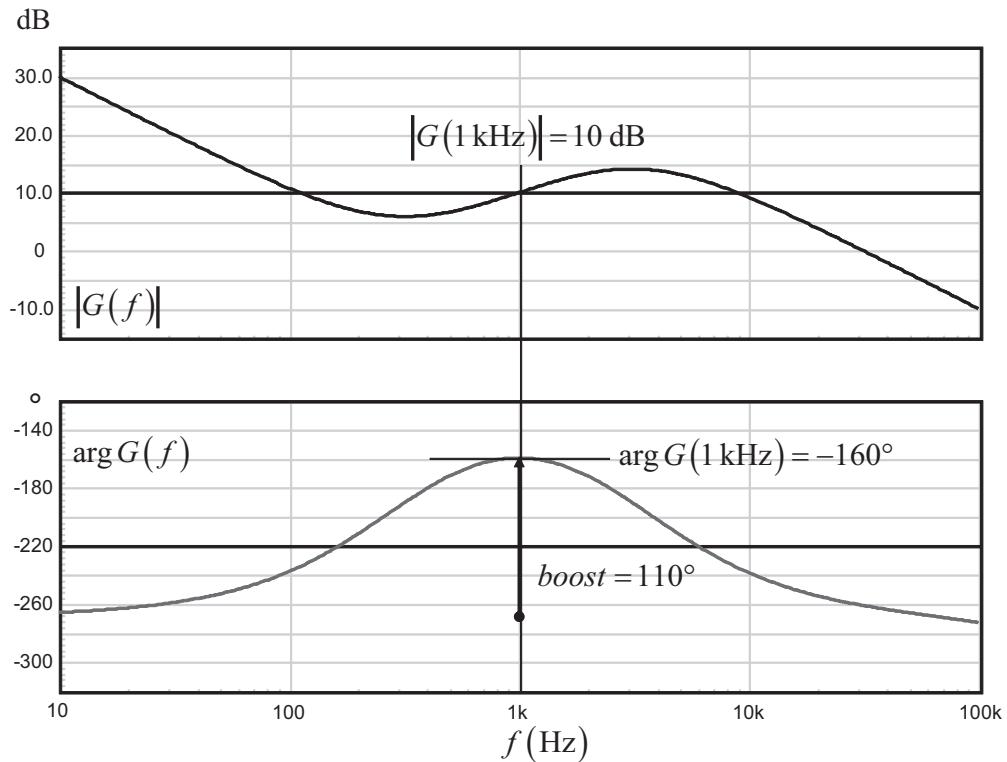


Figure 5.51 The result is excellent: the 10-dB line transition occurs right at 1 kHz, and the phase is boosted by 110°.

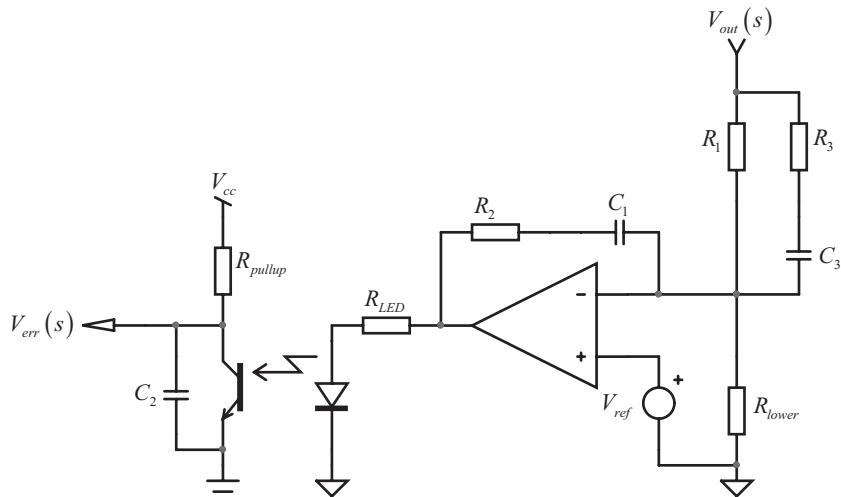


Figure 5.52 By placing the loading resistor in the collector rather than in the emitter, the compensation polarity is changed.

The transfer function is almost similar to that of (5.236), except that the negative sign is gone and the second pole depends on the pull-up resistor:

$$G(s) = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_3C_3} \frac{1 + sC_3[R_1 + R_3]}{1 + sR_{pulldown}C_2} = G_1 G_2 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right) \left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)} \quad (5.259)$$

where

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (5.260)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.261)$$

$$\omega_{z_1} = \frac{1}{R_2 C_1} \quad (5.262)$$

$$\omega_{z_2} = \frac{1}{(R_1 + R_3)C_3} \quad (5.263)$$

$$\omega_{p_1} = \frac{1}{R_3 C_3} \quad (5.264)$$

$$\omega_{p_2} = \frac{1}{R_{pullup} C_2} \quad (5.265)$$

The design methodology exposed in the previous design example remains valid for this type of arrangement.

5.9.4 Optocoupler and Op Amp: The Direct Connection, Common Emitter, and UC384X

The architecture already offered with the type 2 does not change for a type 3 configuration. The UC384X op amp is simply wired as an inverter. As its input impedance is that of the resistor connected to the optocoupler collector, it must be sufficiently high compared to the pull-up resistor. Otherwise, the resistor will change the pole location imposed by C_2 and R_{pullup} . Figure 5.53 depicts a type 3 driving an UC384X controller.

As we already pointed out, this type of control works if the op amp is powered from an auxiliary source already present at startup. Otherwise, the full bias of the LED at power-on (which pushes V_{err} to the maximum) will not occur, preventing the converter from starting up.

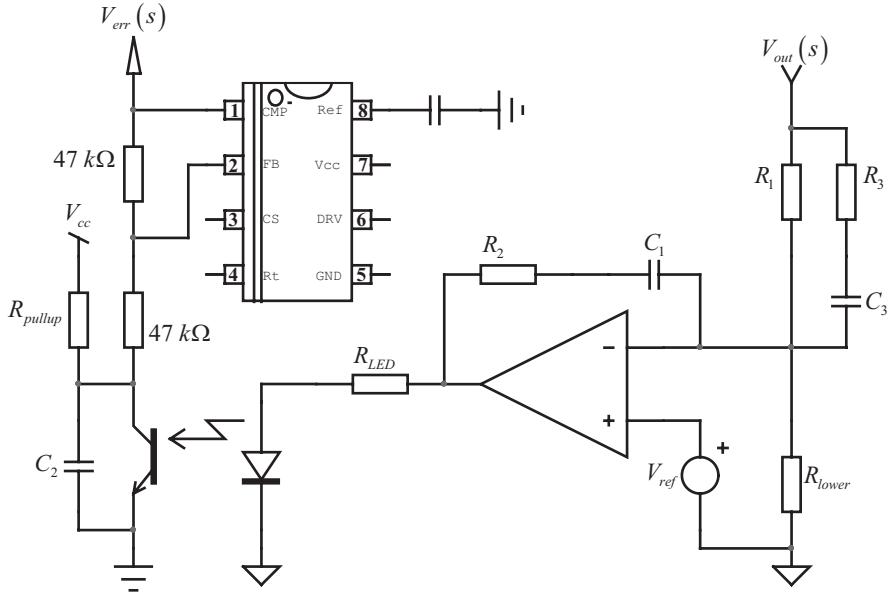


Figure 5.53 The UC384X can be used with a type 3 architecture. Wired as a follower, it does not perturb the chain.

5.9.5 Optocoupler and Op Amp: Pull-Down with Fast Lane

As introduced in Figure 5.20, some controllers do only accept the optocoupler wired in a common-collector configuration. In this case, the op amp must drive the LED in a pull-down association, pulling the LED cathode to ground. The application circuit appears in Figure 5.54. As we described in the type 2 section, the

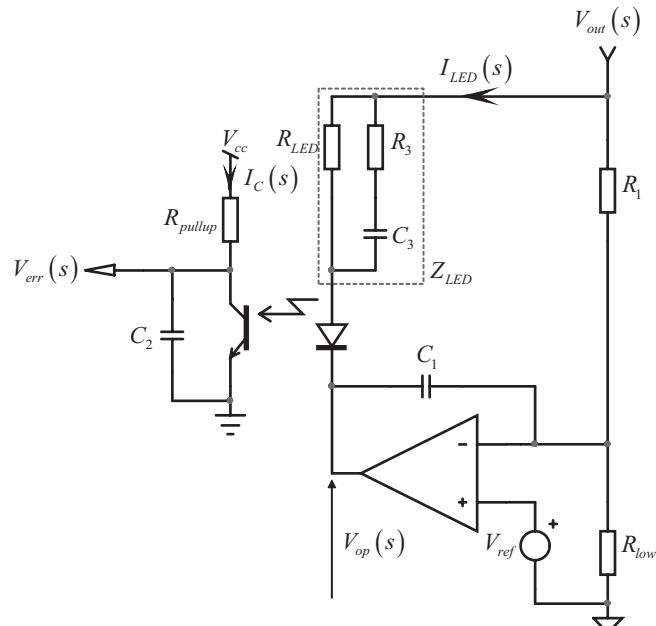


Figure 5.54 The application circuit of the op amp driving the optocoupler LED in a pull-down configuration.

pull-down configuration induces a fast-lane effect we have to deal with. This is the reason the network R_3C_3 must take place across the LED resistor and no longer across R_1 . We will see in a moment how it affects the design flexibility.

Following the description of the type 2 configuration in Section 5.5.5, the LED ac current is defined by

$$I_{LED}(s) = \frac{V_{out}(s) - V_{op}(s)}{Z_{LED}} = (V_{out}(s) - V_{op}(s)) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)} \quad (5.266)$$

The output voltage of the op amp is simply that of a type 1 compensator:

$$V_{op}(s) = -\frac{1}{sC_1R_1}V_{out}(s) \quad (5.267)$$

Substituting (5.267) into (5.266), we obtain

$$\begin{aligned} I_{LED}(s) &= \left(V_{out}(s) + V_{out}(s) \frac{1}{sR_1C_1} \right) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)} \\ &= V_{out}(s) \left(\frac{1 + sR_1C_1}{sR_1C_1} \right) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)} \end{aligned} \quad (5.268)$$

Rearranging the previous, we have

$$I_{LED}(s) = V_{out}(s) \left(\frac{1 + sR_1C_1}{sR_1C_1} \right) \frac{s(R_{LED} + R_3)C_3 + 1}{R_{LED}(sC_3R_3 + 1)} \quad (5.269)$$

Now realizing that the error voltage $V_{err}(s)$ is linked to the LED current by the optocoupler CTR, we have

$$V_{err}(s) = -I_{LED}(s)R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \text{CTR} \quad (5.270)$$

Substituting (5.269) into (5.270) and rearranging, we obtain the transfer function we are looking for:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{1 + 1/sR_1C_1}{1 + sR_{pullup}C_2} \frac{sC_3(R_{LED} + R_3) + 1}{1 + sC_3R_3} = -G_0 \frac{1 + \omega_{z1}/s}{1 + s/\omega_{p1}} \frac{1 + s/\omega_{z2}}{1 + s/\omega_{p2}} \quad (5.271)$$

In this equation, we can identify poles, zeros, and a static gain;

$$G_0 = \frac{R_{pullup}}{R_{LED}} \text{CTR} \quad (5.272)$$

$$\omega_{z1} = \frac{1}{R_1 C_1} \quad (5.273)$$

$$\omega_{z2} = \frac{1}{(R_{LED} + R_3)C_3} \quad (5.274)$$

$$\omega_{p1} = \frac{1}{R_{pullup}C_2} \quad (5.275)$$

$$\omega_{p2} = \frac{1}{R_3 C_3} \quad (5.276)$$

The magnitude of (5.271) is given by

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} = \frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (5.277)$$

Then, combining (5.277), (5.273), (5.274), and (5.276) and solving for R_{LED} , R_3 , C_1 , C_2 , and C_3 , we can extract the definitions we need to design the compensator:

$$R_{LED} = \frac{R_{pullup}}{G} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (5.278)$$

$$C_3 = \frac{f_{p2} - f_{z2}}{2\pi R_{LED} f_{p2} f_{z2}} \quad (5.279)$$

$$R_3 = \frac{f_{z2} R_{LED}}{f_{p2} - f_{z2}} \quad (5.280)$$

$$C_1 = \frac{1}{2\pi f_{z1} R_1} \quad (5.281)$$

$$C_2 = \frac{1}{2\pi R_{pullup} f_{p2}} \quad (5.282)$$

In the previous equations, G is the gain or the attenuation as defined by (5.7). The limiting factor here is, again, the LED resistor. This resistor must be sized to ensure that enough current can cross the LED to bring the error voltage down to the optocoupler $V_{CE,sat}$ level. This LED resistor still obeys (5.103) derived for the type 2 with the LED configured in a pull-down drive:

$$R_{LED,max} = \frac{R_{pullup}(V_{out} - V_f - VOL)CTR_{min}}{(V_{cc} - V_{CE,sat})} \quad (5.283)$$

As this resistor also fixes the gain or the attenuation at the selected crossover frequency, it can be seen as a limiting factor for the possible gain selections. If we combine (5.277) and (5.283), we can solve for the minimum gain below which the system cannot go:

$$|G_{min}| = \frac{V_{cc} - V_{CE,sat}}{V_{out} - V_f - VOL} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (5.284)$$

This G_{min} term illustrates the crossover gain below which the compensator cannot be designed. For instance, should you find a G_{min} of 5 dB with (5.284), you could simply not select a crossover frequency where you need to amplify by 3 dB. It would not work. However, 6 dB would. Changing the optocoupler CTR or R_{pullup} would not help to modify the result. Actually, (5.284) is made of two terms: the first one (involving VOL , V_{out} , and so on) corresponds to the minimum biasing conditions needed to operate the compensator. The second term involves the poles and zeros position—in other words, the needed phase boost. You can therefore see G_{min} as another limit for the maximum phase boost you can ask for a selected gain. We can derive an equation linking G_{min} and the phase boost you want. The result appears next:

$$G_{min}(boost) = 20 \log_{10} \left(\frac{V_{cc} - V_{CE,sat}}{V_{out} - V_f - VOL} \sqrt{\cot^2 \left(\frac{boost}{4} - 45 \right)} \right) \quad (5.285)$$

If we consider the following standard values for the first term of the expression, we can plot (5.285), sweeping the phase boost between 0 and 180°:

$VOL = 0.2$ V; the op amp maximum output voltage.

$V_{out} = 12$ V; the regulated output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

The result appears in Figure 5.55 and shows a gain starting from a minimum value (a null phase boost when both poles and zeros are coincident) and going up as the required phase boost increases. Therefore, when using this type of compensator,

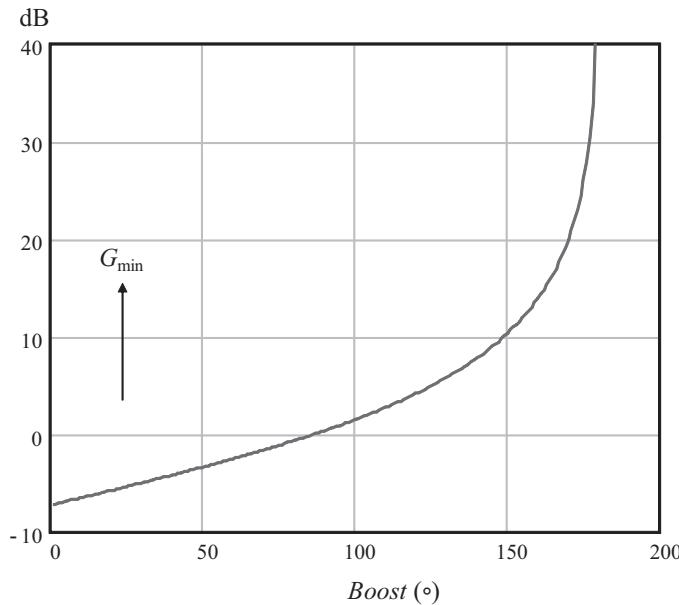


Figure 5.55 The minimum gain is dependent on the wanted phase boost.

it will be important to choose a crossover frequency where the needed gain and phase boost do not conflict with (5.284).

5.9.6 A Design Example

In this example, we want to cross over at a 1-kHz frequency with a 10-dB amplification. The needed phase boost is 120°. The component list appears next and does not change.

$V_{OL} = 0.2$ V; the op amp minimum output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$V_{out} = 12$ V; the converter output voltage.

$R_{pullup} = 1 \text{ k}\Omega$; the optocoupler pull-up resistor.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 15$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

Given the needed 120° phase boost at 1 kHz, we first assume to place coincident poles and zeros at a place to be determined. Capitalizing on what has already been derived, we will place a pole pair at the following position:

$$f_{p1,2} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{1k}{268m} \approx 3.7 \text{ kHz} \quad (5.286)$$

The double zero will be located at

$$f_{z_{1,2}} = \frac{f_c^2}{f_p} = \frac{1k}{3.7k} \approx 270 \text{ Hz} \quad (5.287)$$

Then, with the pole and zero position defined, we proceed by defining the upper limit for the LED resistor. This resistor ensures that the feedback voltage will always be able to deliver a voltage close to $V_{CE,sat}$, despite the minimum CTR of the optocoupler and the op amp output minimum swing. This equation has already been derived in (5.103):

$$R_{LED,\max} = \frac{R_{pullup}(V_{out} - V_f - VOL)\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} = \frac{1k \times (12 - 1 - 0.2)}{5 - 0.3} \times 0.8 = 1.8 \text{ k}\Omega \quad (5.288)$$

We now have to check whether the 120° phase boost at the selected 10-dB gain are compatible with the LED biasing conditions. Using (5.285), we have

$$G_{\min} = 20 \log_{10} \left(\frac{5 - 0.3}{12 - 1 - 0.2} \sqrt{\cot^2 \left(\frac{120}{4} - 45 \right)} \right) = 20 \log_{10} (435m \times 3.73) \approx 4.2 \text{ dB} \quad (5.289)$$

Since we want 10 dB, we are well above what (5.289) recommends, and we can thus continue with the design process. Applying the formulas we derived for R_2 , C_2 , C_3 , and R_3 , we have

$$R_{LED} = \frac{1k}{10^{20}} 0.8 \sqrt{1 + \left(\frac{270}{1k} \right)^2} \sqrt{1 + \left(\frac{1k}{270} \right)^2} \sqrt{1 + \left(\frac{1k}{3.7k} \right)^2} \sqrt{1 + \left(\frac{1k}{3.7k} \right)^2} = 944 \Omega \quad (5.290)$$

$$C_3 = \frac{3.7k - 270}{6.28 \times 3.7k \times 944 \times 270} \approx 580 \text{ nF} \quad (5.291)$$

$$R_3 = \frac{270 \times 944}{3.7k - 270} = 74 \Omega \quad (5.292)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_1} = \frac{1}{6.28 \times 270 \times 38k} = 15.6 \text{ nF} \quad (5.293)$$

$$C_2 = \frac{1}{2\pi R_{pullup} f_{p_2}} = \frac{1}{6.28 \times 1k \times 3.7k} = 43 \text{ nF} \quad (5.294)$$

The capacitor across the optocoupler, in total, must equal 43 nF. The optocoupler pole is located at 15 kHz. Given a pull-up resistor of 1 k Ω , we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6 \text{ nF} \quad (5.295)$$

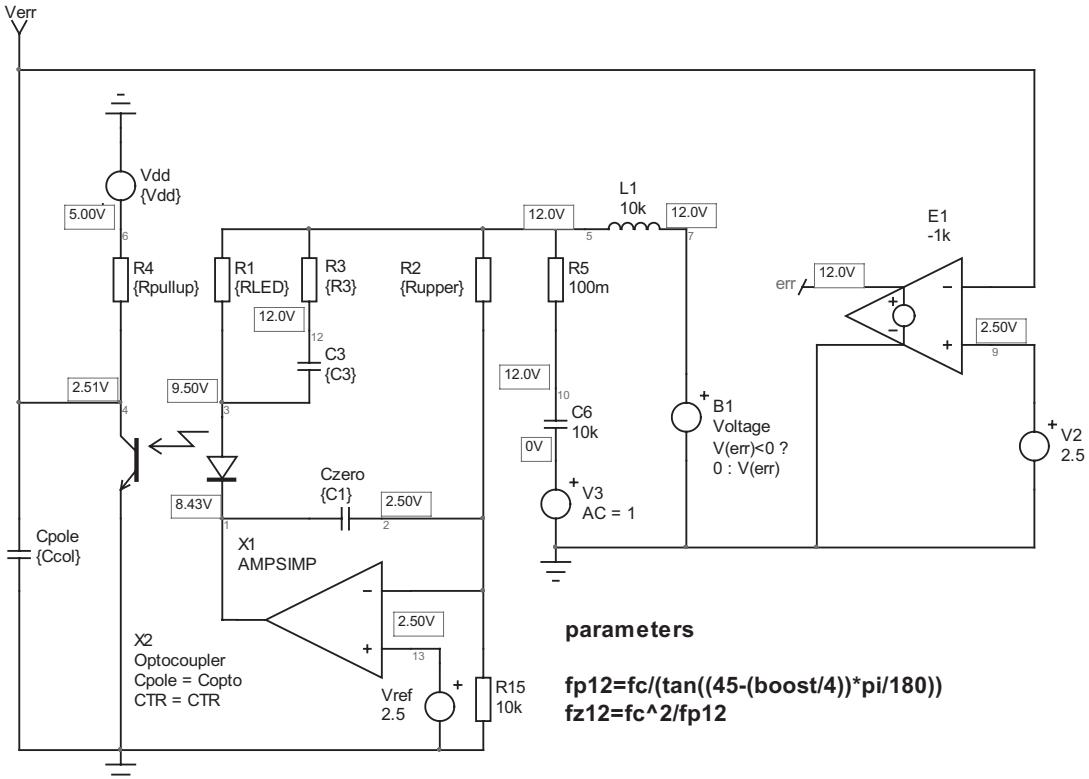


Figure 5.56 The bias-point-automated simulation template helps to test the calculated parameters for all our components.

When subtracted from (5.294), you obtain the value for C_{col} , the final capacitor installed across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 43n - 10.6n \approx 32 \text{ nF} \quad (5.296)$$

The design is done now, and we can start the simulation as proposed by Figure 5.56. The parameter calculations are fully automated and we can change the needed boost or crossover gain on the fly and check if the results match our wishes. The simulation results appear in Figure 5.57 and confirm the design methodology we have adopted.

5.9.7 Optocoupler and Op Amp: Pull Down without Fast Lane

The fast lane presence really hampers the design, as it introduces another limiting variable. The problem comes from the access of $V_{out}(s)$ to the error path via the LED connection. To get rid of this problem, we must provide an ac isolation between the LED current and the regulated output variable. This is the solution already introduced in Figure 5.25 and updated in Figure 5.58.

Observing Figure 5.58 reveals the presence of a type 3a kind of compensator where the high-frequency pole has moved on the optocoupler. Let us write the

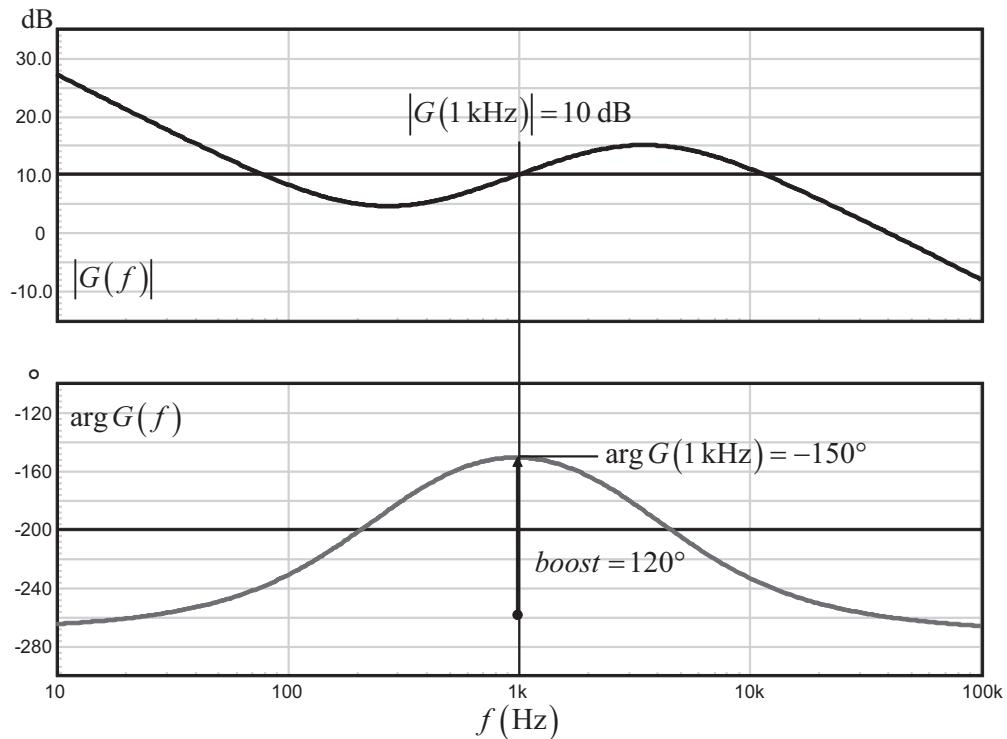


Figure 5.57 The simulation results confirm the correct phase boost as well as the perfect 10-dB crossover gain.

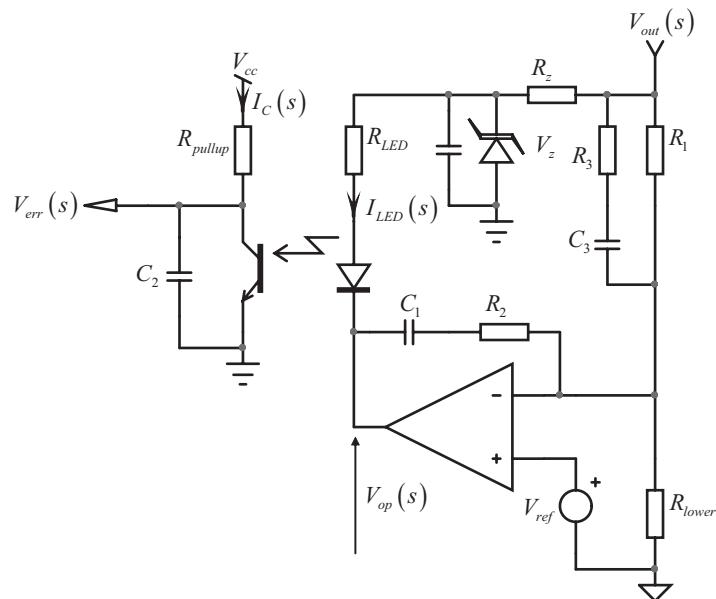


Figure 5.58 To get rid of this problem, we will apply the technique already seen in the type 2 section where the LED is ac-decoupled from V_{out} via a Zener diode.

output voltage of the op amp, $V_{op}(s)$, by deriving the impedance definitions for Z_i and Z_f ,

$$Z_f = \left(\frac{1}{sC_1} + R_2 \right) \quad (5.297)$$

$$Z_i = \left(\frac{1}{sC_3} + R_3 \right) R_1 \Big/ \left(\frac{1}{sC_3} + R_3 + R_1 \right) \quad (5.298)$$

By dividing (5.297) by (5.298) and factoring sR_2C_1 , we obtain the transfer function of the op amp alone:

$$\frac{V_{op}(s)}{V_{out}(s)} = -\frac{R_2}{R_1} \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_3C_3} (1 + sC_3(R_1 + R_3)) \quad (5.299)$$

With the op amp output driving the LED current, the error signal is thus that of the op amp translated by a gain brought by the optocoupler. We have already seen this in (5.114):

$$V_{err}(s) = -I_{LED}(s)R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \text{CTR} \quad (5.300)$$

The ac LED current being $-V_{op}(s)/R_{LED}$, the final transfer function definition pops up immediately:

$$\frac{V_{op}(s)}{V_{out}(s)} = -\frac{R_2}{R_1} \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{1 + \frac{1}{sR_2C_1}}{1 + sR_3C_3} \frac{1 + sC_3(R_1 + R_3)}{1 + sR_{pullup}C_2} \quad (5.301)$$

This expression can be put under the normalized form:

$$G(s) = -G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right) \left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)} \quad (5.302)$$

where

$$G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} = G_1 G_2 \quad (5.303)$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (5.304)$$

$$G_2 = \frac{R_2}{R_1} \quad (5.305)$$

$$\omega_{z_1} = \frac{1}{R_2 C_1} \quad (5.306)$$

$$\omega_{z_2} = \frac{1}{2\pi C_3(R_1 + R_3)} \quad (5.307)$$

$$\omega_{p_1} = \frac{1}{2\pi R_3 C_3} \quad (5.308)$$

$$\omega_{p_2} = \frac{1}{R_{pullup} C_2} \quad (5.309)$$

The magnitude of (5.302) is given by

$$|G(f_c)| = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \sqrt{\frac{1 + \left(\frac{f_{z_1}}{f_c}\right)^2}{1 + \left(\frac{f_c}{f_{p_1}}\right)^2}} \sqrt{\frac{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (5.310)$$

Then, combining and solving for R_{LED} , R_3 , C_2 , C_1 , and C_3 , we can extract the definitions we are looking for:

$$R_2 = \frac{GR_1R_{LED}}{R_{pullup}\text{CTR}} \sqrt{\frac{1 + \left(\frac{f_c}{f_{p_1}}\right)^2}{1 + \left(\frac{f_{z_1}}{f_c}\right)^2}} \sqrt{\frac{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (5.311)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} \quad (5.312)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad (5.313)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pullup}} \quad (5.314)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_1 f_{p_2} f_{z_2}} \quad (5.315)$$

With the fast lane being removed, the LED resistor no longer plays a role in the pole/zero positions. Its value now solely depends on acceptable bias conditions to give the error voltage the necessary swing, despite unavoidable dispersions on the optocoupler CTR. The formula derived in the type 2 case is still valid:

$$R_{LED,\max} = \frac{R_{pullup}(V_Z - V_f - \text{VOL})\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} \quad (5.316)$$

In this expression, the V_Z term represents the selected Zener level obtained from the output. As discussed in Section 5.5.8, we recommend a Zener voltage equal to two-thirds of the output voltage. This tradeoff offers a limited voltage loss across the dropping resistor and ensures a good ac decoupling between the Zener voltage and the monitored output. Considering a Zener biasing current I_{Zbias} , the dropping resistor can be computed using an equation already derived:

$$R_Z = \frac{(V_{out} - V_Z)R_{pullup}\text{CTR}_{\min}}{V_{cc} - V_{CE,sat} + I_{Zbias}R_{pullup}\text{CTR}_{\min}} \quad (5.317)$$

All component values are now attached to a design formula; it is time for the design example!

5.9.8 A Design Example

In this example, we have to crossover at a 5-kHz frequency where a -10 -dB attenuation is needed. At the crossover point, the phase must be boosted by 150° . The parameter list appears next and does not change.

$\text{VOL} = 0.2$ V; the op amp minimum output voltage

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$V_{out} = 12$ V; the converter output voltage.

$R_{pullup} = 1 \text{ k}\Omega$; the optocoupler pull-up resistor.

$\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 15$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

Given the needed 150° phase boost at 5 kHz, we first assume we should place co-incident poles and zeros at a location to be determined. Capitalizing on what has already been derived, we will place a pole pair at the following position:

$$f_{p1,2} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{5k}{131m} \approx 38 \text{ kHz} \quad (5.318)$$

The double zero will be located at

$$f_{z1,2} = \frac{f_c^2}{f_p} = \frac{25k}{38k} \approx 660 \text{ Hz} \quad (5.319)$$

As usual, let us pick a LED resistance that fits our bias requirements using (5.316):

$$R_{LED,\max} = \frac{R_{pullup}(V_Z - V_f - \text{VOL})\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat})} = \frac{1k \times (8.2 - 1 - 0.2)}{5 - 0.3} \times 0.8 = 1.2 \text{ k}\Omega \quad (5.320)$$

Applying a 20 percent design margin, we select a $910\ \Omega$ resistor. For a 12 V output, we have selected an 8.2 V Zener diode. Considering a 1-mA bias current for this component, we can now calculate the associated dropping resistor using (5.317):

$$R_Z = \frac{(V_{out} - V_Z)R_{pullup}CTR_{min}}{V_{cc} - V_{CE,sat} + I_{Zbias}R_{pullup}CTR_{min}} = \frac{(12 - 8.2) \times 1k \times 0.8}{5 - 0.3 + 1m \times 1k \times 0.8} = 552\ \Omega \quad (5.321)$$

The type 3 passive elements are calculated using equations (5.311) through (5.315):

$$R_2 = \frac{10^{-\frac{10}{20}} \times 910}{1k \times 0.8} \sqrt{\frac{1 + \left(\frac{5k}{38k}\right)^2}{1 + \left(\frac{660}{5k}\right)^2}} \sqrt{\frac{1 + \left(\frac{5k}{38k}\right)^2}{1 + \left(\frac{5k}{660}\right)^2}} = 1.8\ k\Omega \quad (5.322)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} = \frac{38k \times 660}{38k - 660} = 671\ \Omega \quad (5.323)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} = \frac{1}{6.28 \times 660 \times 1.8k} = 134\ nF \quad (5.324)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pullup}} = \frac{1}{6.28 \times 38k \times 1k} = 4.2\ nF \quad (5.325)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_1 f_{p_2} f_{z_2}} = \frac{38k - 660}{6.28 \times 38k \times 38k \times 660} = 6.2\ nF \quad (5.326)$$

We know that the total capacitor connected across the optocoupler that forms C_2 is actually made of the optocoupler parasitic pole C_{opto} and the added capacitor C_{col} . The optocoupler pole is located at 15 kHz. Given a pull-up resistor of $1\ k\Omega$, we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 15k \times 1k} = 10.6\ nF \quad (5.327)$$

When subtracted from (5.325), you obtain the value for C_{col} , the final capacitor installed across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 4.2n - 10.6n \approx -6.4\ nF \quad (5.328)$$

This is a negative capacitor value, meaning that the second pole is entirely fixed by the optocoupler at 15 kHz rather than the expected one at 38 kHz. To ensure the presence of an extra capacitor across the optocoupler for an improved noise immunity, we can see that we do not have too many choices:

1. Reduce the crossover frequency until the added capacitor becomes positive again. Shoot for a value above 100 pF, placed very close to the controller. In

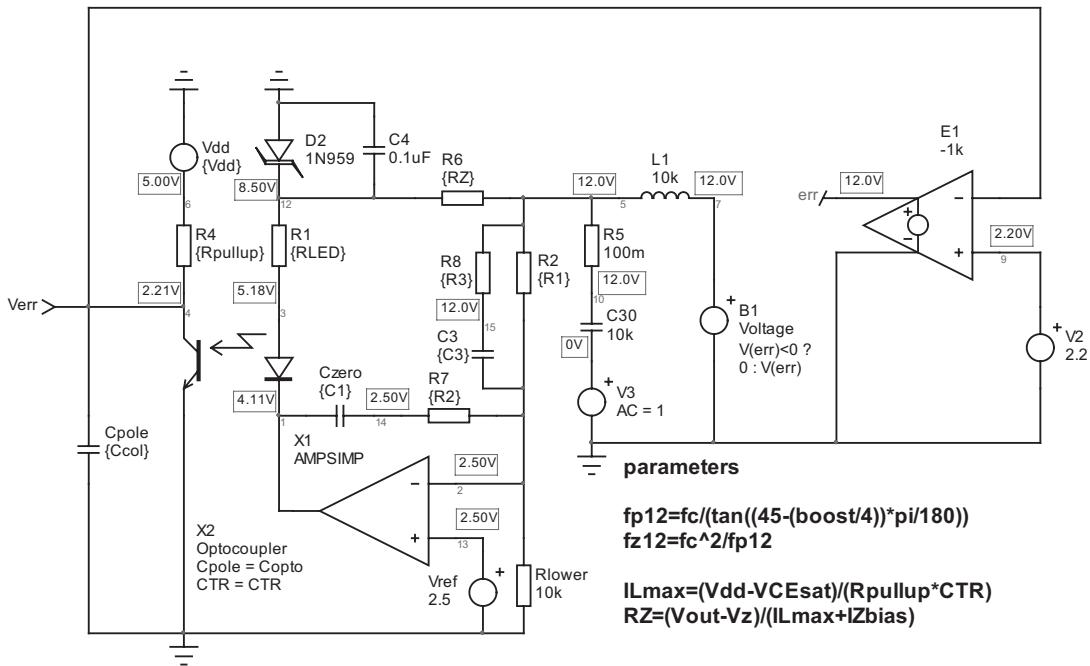


Figure 5.59 The type 3 featuring the Zener diode no longer shows the gain limit inherent to the fast lane.

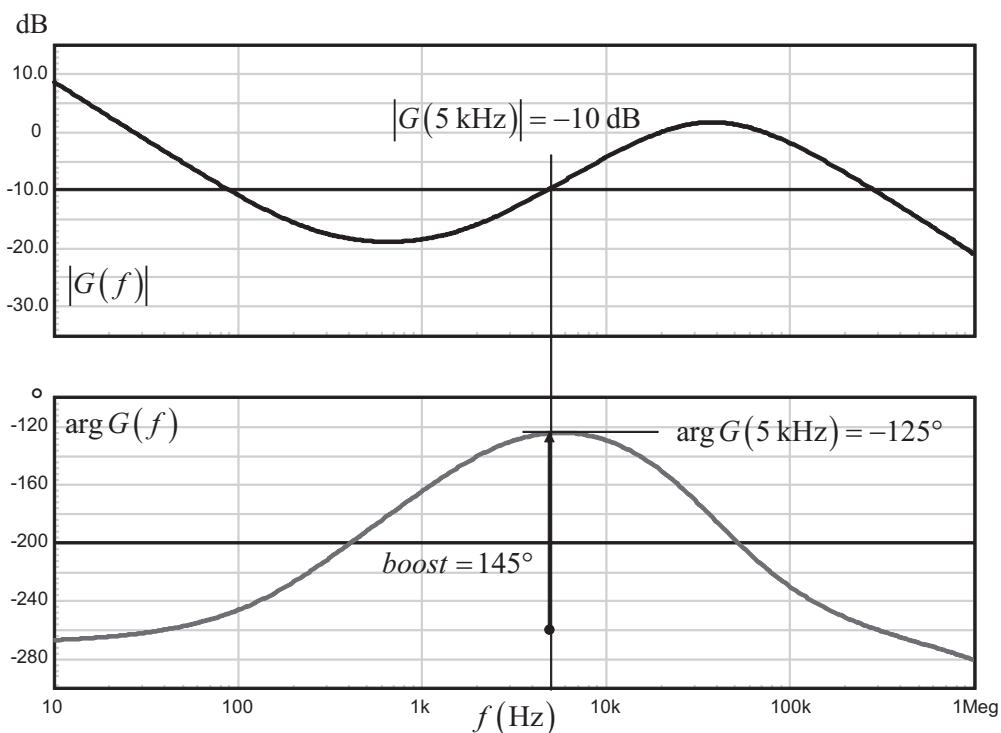


Figure 5.60 The simulation results of the type 3 compensator based on an op amp where the fast lane has been deactivated.

our example, reducing the crossover frequency to 1.8 kHz induces an extra capacitor value of 1 nF.

2. Adopt a faster optocoupler whose pole when associated with the selected pull-up resistor is beyond the high-frequency pole selected for the compensator. Another solution consists of using a cascode configuration.

Having these elements on hand, it is time for a simulation, as proposed by Figure 5.59.

The ac results show that the phase boost is slightly less than what was expected, mainly due to the mismatch in the second high-frequency pole that lead us to ignore C_{col} since the optocoupler pole fixes the second pole entirely (see Figure 5.60).

5.10 Conclusion

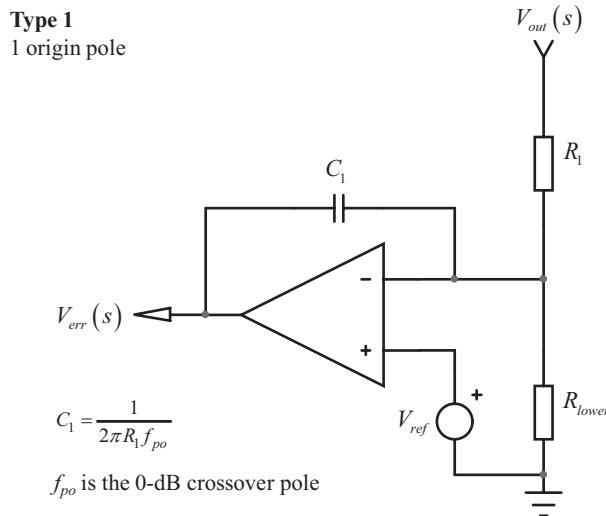
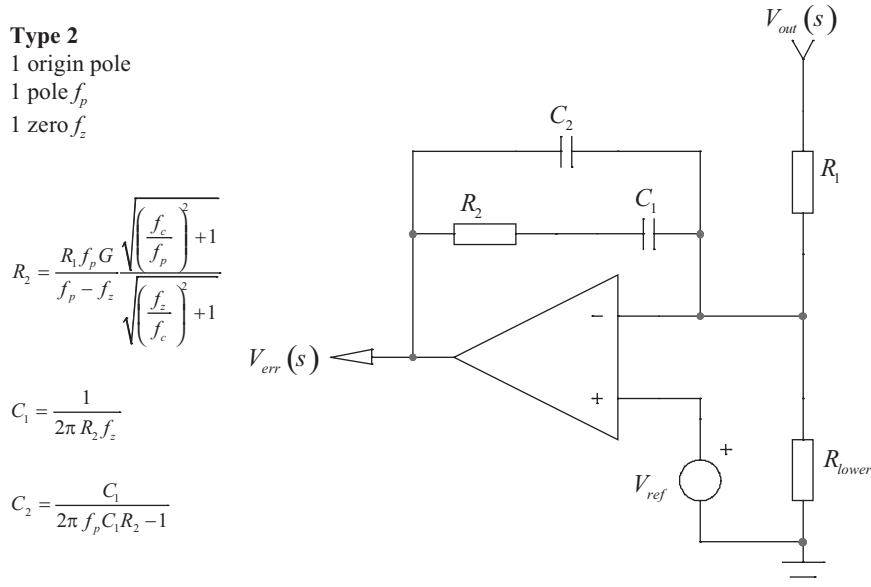
Op amp used in control loop can be wired in a lot of different ways. We believe this chapter covers most of the possible structures you will use during your design analysis. Whether you stabilize nonisolated dc-dc converters or ac-dc power supplies with an optocoupler, you should find the structure that suits your needs. If not, you have all the analysis examples that will help you derive the set of expressions you need. Finally, to let you strengthen your knowledge in the field of operational amplifiers and their usage in the power electronics field, [1–4] should put you on the right track.

References

- [1] Mancini, R., “Op Amps for Everyone,” Texas-Instruments Application note SLOD006b, August 2002.
- [2] Carter, B., “Handbook of Operational Amplifier Functions,” Texas-Instruments Application note SBOA092A, October 2001.
- [3] Basso, C., *Switch Mode Power Supplies: SPICE Simulations and Practical Designs*, New York: McGraw-Hill, 2008.
- [4] Mamano, B., “Isolating the Control Loop,” Unitrode application note SLUP090, SEM700, 1990.

Appendix 5A: Summary Pictures

The following pictures summarize the component definitions associated with the structures described in the chapter.

**Figure 5.61** The type 1.**Figure 5.62** The type 2.

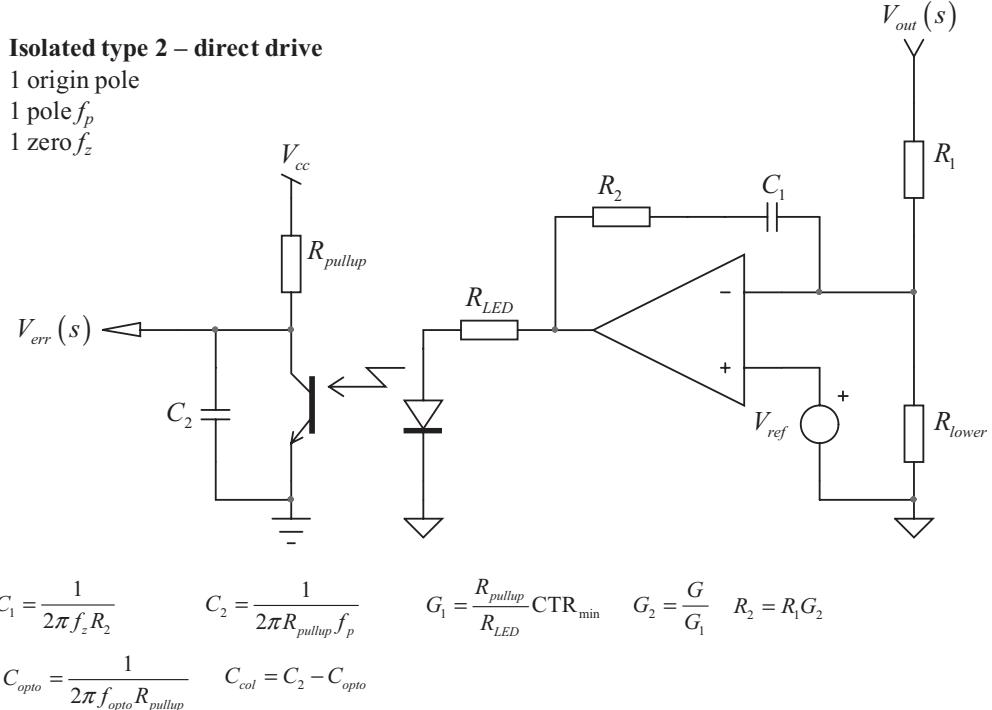
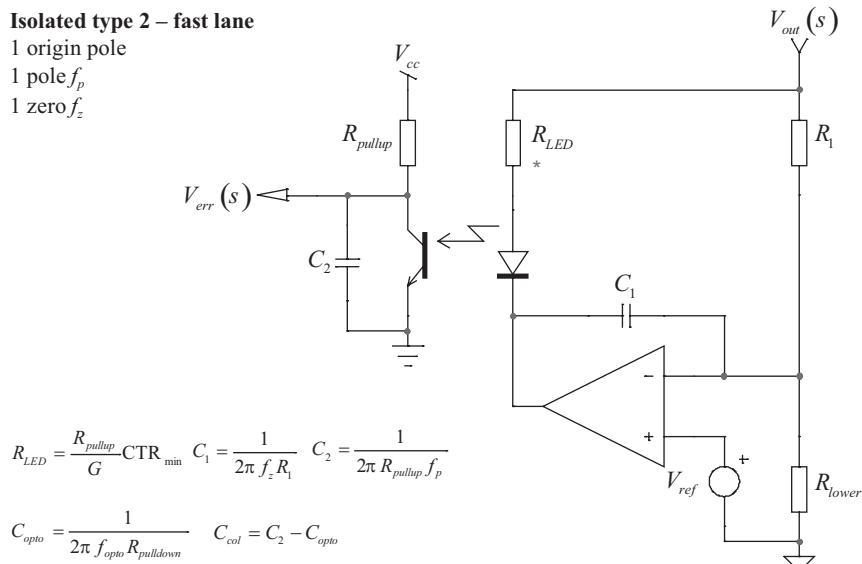


Figure 5.63 An isolated type 2, direct optocoupler connection.

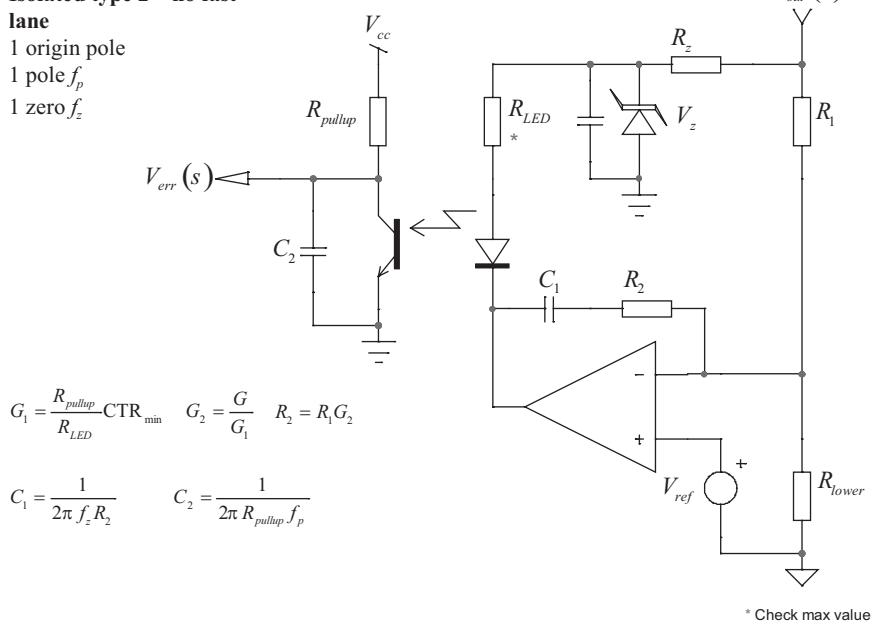


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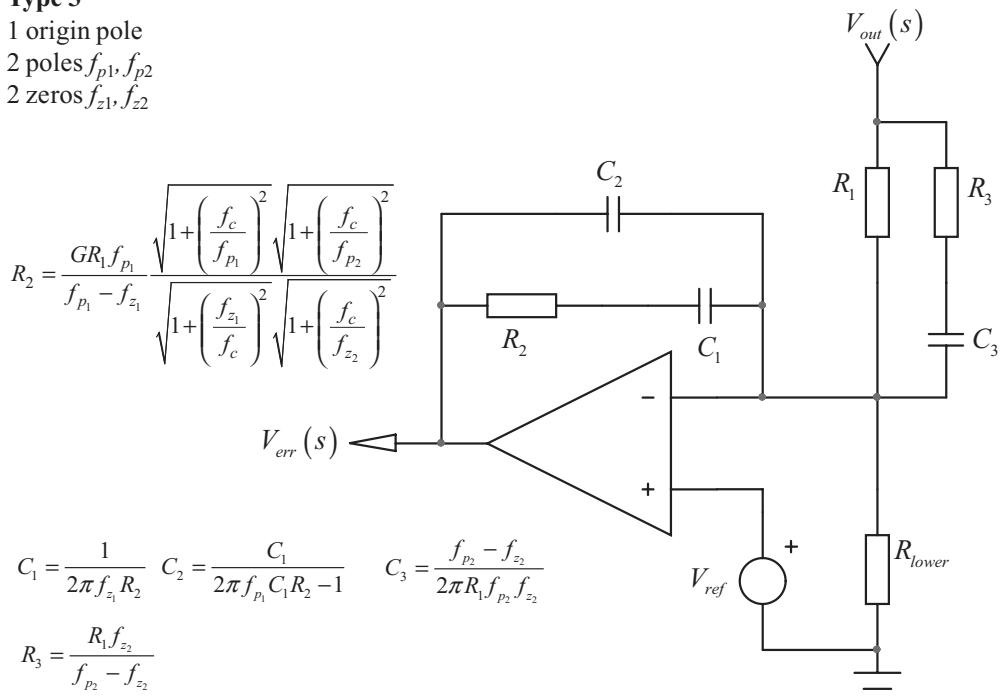
Figure 5.64 An isolated type 2 with fast lane.

Isolated type 2 – no fast lane

- 1 origin pole
- 1 pole f_p
- 1 zero f_z

**Figure 5.65** An isolated type 2 without fast lane.**Type 3**

- 1 origin pole
- 2 poles f_{p1}, f_{p2}
- 2 zeros f_{z1}, f_{z2}

**Figure 5.66** The type 3.

Isolated type 3

1 origin pole

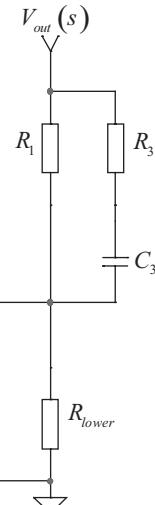
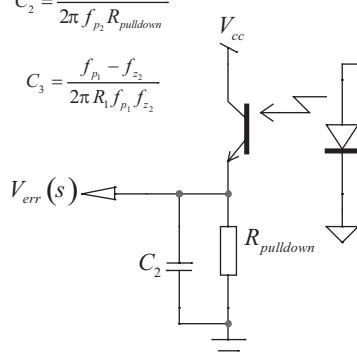
2 poles f_{p1}, f_{p2} 2 zeros f_{z1}, f_{z2}

$$R_2 = \frac{G}{G_1} R_1 \sqrt{\frac{1 + \left(\frac{f_c}{f_{p1}}\right)^2}{1 + \left(\frac{f_{z_1}}{f_c}\right)^2}} \sqrt{\frac{1 + \left(\frac{f_c}{f_{p2}}\right)^2}{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad G_1 = \text{CTR} \frac{R_{\text{pulldown}}}{R_{\text{LED}}}$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2}$$

$$C_2 = \frac{1}{2\pi f_{p2} R_{\text{pulldown}}}$$

$$C_3 = \frac{f_{p_1} - f_{z_2}}{2\pi R_1 f_{p_1} f_{z_2}}$$



$$R_3 = \frac{R_1 f_{z_2}}{f_{p_1} - f_{z_2}} \quad C_{\text{opto}} = \frac{1}{2\pi f_{\text{opto}} R_{\text{pulldown}}} \quad C_{\text{col}} = C_2 - C_{\text{opto}}$$

Figure 5.67 An isolated type 3, direct optocoupler connection.**Isolated type 3 – fast lane**

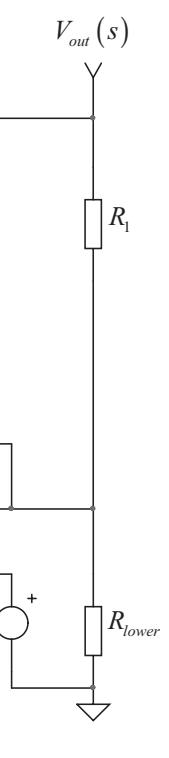
1 origin pole

2 poles f_{p1}, f_{p2} 2 zeros f_{z1}, f_{z2}

$$R_{\text{LED}} = \frac{R_{\text{pullup}}}{G} \text{CTR} \sqrt{\frac{1 + \left(\frac{f_{z_1}}{f_c}\right)^2}{1 + \left(\frac{f_c}{f_{p_1}}\right)^2}} \sqrt{\frac{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_{\text{LED}} f_{p_2} f_{z_2}} \quad C_1 = \frac{1}{2\pi f_{z_1} R_1} \quad R_3 = \frac{f_{z_2} R_{\text{LED}}}{f_{p_2} - f_{z_2}}$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{\text{pullup}}} \quad C_{\text{opto}} = \frac{1}{2\pi f_{\text{opto}} R_{\text{pullup}}} \quad C_{\text{col}} = C_2 - C_{\text{opto}}$$



* Check max value

Figure 5.68 An isolated type 3 with fast lane.

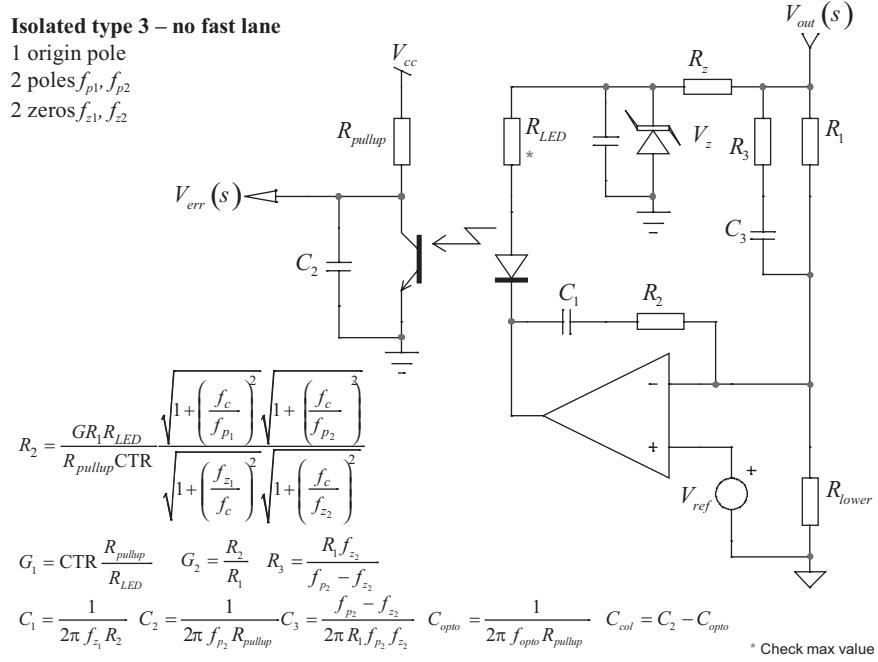


Figure 5.69 An isolated type 3, no fast lane.

Appendix 5B: Automating Components Calculations with k Factor

The k factor is a technique introduced by Dean Venable and described in [1]. Basically, it uses the formulas already derived in Chapter 4 that dictate the positions of the single or double pole/zero pair. Dean Venable's idea was then to include his k factor definition into the calculation of the R and C elements of any compensator. At that time, he only covered op amp-based circuits, and that is the limit of his analysis. The nice thing for beginners, however, is that you do not manipulate poles, zeros, or the 0-dB crossover pole position, as these values do not appear in the component definitions. The drawback of the method is that crossover is always placed at the geometric means of the poles and zeros positions: you cannot split them to cope with your particular design. This is the reason that in this book, we preferred manually placing individual poles and zeros for the best flexibility, whether or not you want coincident poles/zeros.

For the sake of explanation, but also because the method is popular, we will show how component values for op amp-based compensators were derived using the k factor method next.

Type 1

The type 1 does not need particular development, as we do not place a pole or a zero but rather a 0-dB origin pole. We can also think of the type 1 as a type 2 compensator where the poles and zeros would be made coincident. In that case, k as defined by

$$k = \tan\left(\frac{\text{boost}}{2} + \frac{\pi}{4}\right) \quad (5.329)$$

would simply be 1, as the phase boost in a type 1 is 0. The formulas given in the beginning of this chapter are those that Dean Venable derived in his paper: (5.7), (5.8), and (5.9).

Type 2

The type 2 from Figure 5.5 requires a little bit of algebraic efforts to unveil the value of k in the design formulas we have. The position of the pole, the zero, and the mid-band gain G for an op amp-based type 2 are the following:

$$G = \frac{R_2}{R_1} \frac{C_1}{C_1 + C_2} \quad (5.330)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (5.331)$$

$$\omega_p = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \quad (5.332)$$

The relationship from Chapter 4 that links the pole and zero position with the crossover point is

$$\omega_p = k \cdot \omega_c \quad (5.333)$$

$$\omega_z = \frac{\omega_c}{k} \quad (5.334)$$

From (5.330), we can extract the value of R_2 :

$$R_2 = \frac{G \cdot R_1(C_1 + C_2)}{C_1} \quad (5.335)$$

A similar value can be obtained if we equate (5.332) and (5.333), and then solve for R_2 . We should obtain

$$R_2 = \frac{C_1 + C_2}{C_1 C_2 \omega_c k} \quad (5.336)$$

Now, equating (5.335) and (5.336), we can extract the value of C_2 :

$$\frac{G \cdot R_1(C_1 + C_2)}{C_1} = \frac{C_1 + C_2}{C_1 C_2 \omega_c k} \quad (5.337)$$

Given the simplifications by $(C_1 + C_2)$ and C_1 , it becomes

$$C_2 = \frac{1}{\omega_c G \cdot k \cdot R_1} = \frac{1}{2\pi f_c G \cdot k \cdot R_1} \quad (5.338)$$

Now, if we equate (5.331) and (5.334), we obtain another definition for R_2 :

$$R_2 = \frac{k}{C_1 \omega_c} \quad (5.339)$$

This definition is similar to that given in (5.336); we can now solve for C_2 :

$$\frac{k}{C_1 \omega_c} = \frac{C_1 + C_2}{C_1 C_2 \omega_c k} \quad (5.340)$$

We find

$$C_1 = C_2(k^2 - 1) \quad (5.341)$$

R_2 was already derived in (5.339) and equals

$$R_2 = \frac{k}{2\pi f_c C_1} \quad (5.342)$$

In these formulas, G is the gain/attenuation needed at the selected crossover frequency f_c .

Type 3

The type 3 was introduced in Figure 5.46. The positions of the poles and zeros pairs have been derived in this chapter. If we consider coincident poles and zeros, we have

$$\omega_{z_{1,2}} = \frac{1}{R_2 C_1} = \frac{1}{(R_1 + R_3) C_3} \quad (5.343)$$

$$\omega_{p_{1,2}} = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} = \frac{1}{R_3 C_3} \quad (5.344)$$

The crossover gain G involves the poles/zeros positions and is given by

$$G = \frac{R_2}{R_1} \frac{C_1}{C_1 + C_2} \frac{\sqrt{1 + \left(\frac{\omega_{z_{1,2}}}{\omega_c}\right)^2} \sqrt{1 + \left(\frac{\omega_c}{\omega_{z_{1,2}}}\right)^2}}{1 + \left(\frac{\omega_c}{\omega_{p_{1,2}}}\right)^2} \quad (5.345)$$

The relationship from Chapter 4 that links the pole and zero position is still

$$\omega_{p_{1,2}} = k \cdot \omega_c \quad (5.346)$$

$$\omega_{z_{1,2}} = \frac{\omega_c}{k} \quad (5.347)$$

In (5.345), we can substitute the poles and zeros definitions in (5.346) and (5.347), and rewrite the expression as follows:

$$G = \frac{R_2 C_1 k^2 \sqrt{\frac{k^2 + 1}{k^2}}}{R_1(C_1 + C_2) \sqrt{k^2 + 1}} = \frac{C_1 R_2 k}{R_1(C_1 + C_2)} \quad (5.348)$$

As (5.343) and (5.347) are similar, we can extract the value of R_2 that we will substitute in (5.348):

$$R_2 = \frac{k}{\omega_c C_1} \quad (5.349)$$

$$G = \frac{k^2}{R_1 \omega_c (C_1 + C_2)} \quad (5.350)$$

Now, if we equate (5.346) and the second term of (5.344), then substitute R_2 by its definition in (5.349), we have

$$\omega_c k = \frac{\omega_c (C_1 + C_2)}{k C_2} \quad (5.351)$$

Solving for C_1 , we obtain

$$C_1 = C_2(k^2 - 1) \quad (5.352)$$

Now that we have a link between C_1 and C_2 , we can replace C_1 in (5.350) by its definition in (5.352). Then, solving for C_2 , we obtain

$$C_2 = \frac{1}{2\pi f_c R_1 G} \quad (5.353)$$

Let's have a look at R_2 already given by (5.349). We can keep this value (equal to that of Dean Venable) or use (5.352) and (5.353) to develop it further:

$$R_2 = \frac{k}{\omega_c C_2 (k^2 - 1)} = \frac{R_1 G \cdot k}{(k^2 - 1)} \quad (5.354)$$

R_3 and C_3 require a few more lines. From (5.344), we extract R_3 :

$$R_3 = \frac{C_1 C_2 R_2}{C_3 (C_1 + C_2)} \quad (5.355)$$

From (5.343), we get R_2 :

$$R_2 = \frac{C_3(R_1 + R_3)}{C_1} \quad (5.356)$$

and we substitute its definition in (5.355). We obtain

$$R_3 = \frac{C_2(R_1 + R_3)}{C_1 + C_2} \quad (5.357)$$

Solving for R_3 , gives

$$R_3 = \frac{C_2 R_1}{C_1} \quad (5.358)$$

From (5.352), we can define C_2/C_1 :

$$\frac{C_2}{C_1} = \frac{1}{k^2 - 1} \quad (5.359)$$

R_3 is now fully defined by

$$R_3 = \frac{R_1}{k^2 - 1} \quad (5.360)$$

C_3 is obtained by using (5.344) and (5.346):

$$\omega_c k = \frac{1}{R_3 C_3} \quad (5.361)$$

Thus,

$$C_3 = \frac{1}{2\pi f_c R_3 k} \quad (5.362)$$

We are all set! The difference in these equations with those derived by Dean Venable is the k value that we kept similar to that of the type 2 definition. Mr. Venable purposely squared the right term of (5.329):

$$k_{Venable} = \left[\tan\left(\frac{\text{boost}}{2} + \frac{\pi}{4}\right) \right]^2 \quad (5.363)$$

and thus uses \sqrt{k} instead in all his equations. Final results are obviously similar. The following figures give a summary of the k factor components definitions in the three different compensator types.

Reference

- [1] Venable, D., "The k Factor: A New Mathematical Tool for Stability Analysis and Synthesis," *Proceedings of Powercon 10*, 1983, pp. 1–12.

f_c is the crossover frequency

G is the gain/attenuation at crossover

$$C_1 = \frac{1}{2\pi f_c R_l G}$$

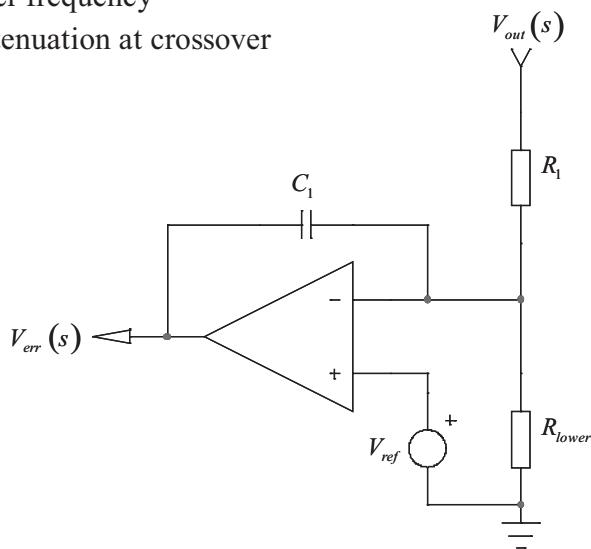


Figure 5.70 The type 1 is a simple compensator featuring an origin pole.

f_c is the crossover frequency

G is the gain/attenuation at crossover

$$k = \tan\left(\frac{\text{boost}}{4} + \frac{\pi}{4}\right)$$

$$C_2 = \frac{1}{2\pi f_c G \cdot k \cdot R_l}$$

$$C_1 = C_2 (k^2 - 1)$$

$$R_2 = \frac{k}{2\pi f_c C_1}$$

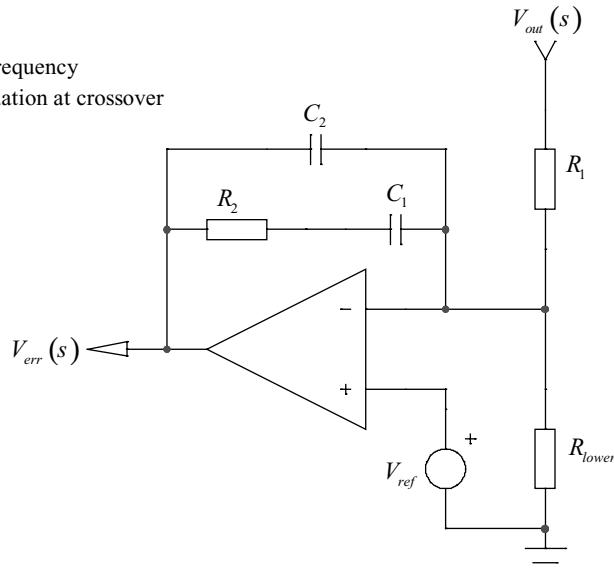


Figure 5.71 The type 2 compensator using components definitions involving the k factor.

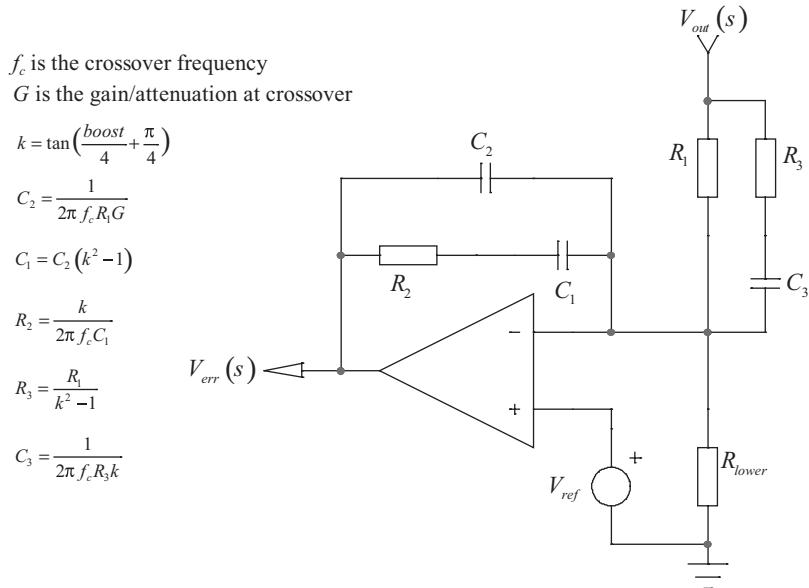


Figure 5.72 The type 3 compensator featuring the components definitions involving the k factor.

Appendix 5C: The Optocoupler

In isolated structures, the secondary-side information has to be conveyed across an isolation barrier to reach the nonisolated primary side. Several methods exist to cross that barrier, but the most popular uses an optical component called the optocoupler. Throughout the examples, we learned that the device affects the transfer function through several parameters, such as its current transfer ratio and transmission pole. Despite the care you will put in the selection of poles/zeros placement to build phase and gain margins, the insertion of the optocoupler can ruin your efforts if you do not realize its impact on the final transfer function. Knowing how to extract the optocoupler parameters and understand how they can change is vital to designing robust and reliable converters.

Transmitting Light

An optocoupler is made of a bipolar transistor and a gallium arsenide (GaAs) LED element. Encapsulated into a plastic package, it can provide galvanic isolation from 2.5 kV to 6 kV between a transformer-isolated secondary side and the primary side of a converter. The term galvanic comes after Luigi Galvani, an Italian scientist who studied the effects of electricity on muscles in the 18th century.

There are several manufacturing techniques related to the optocouplers. Reference [1] reviews the assembly techniques in great detail. Among them, the planar technique consists of laying the diode and transistor in the same plane and wire bonding them to a common leadframe. Figure 5.73 shows a simplified view of a planar optocoupler, where a silicone dome reflects the LED beam to further route it to the transistor collector-base junction. The photons emitted by the beam light are collected by the base of the transistor and give rise to a collector current. As no

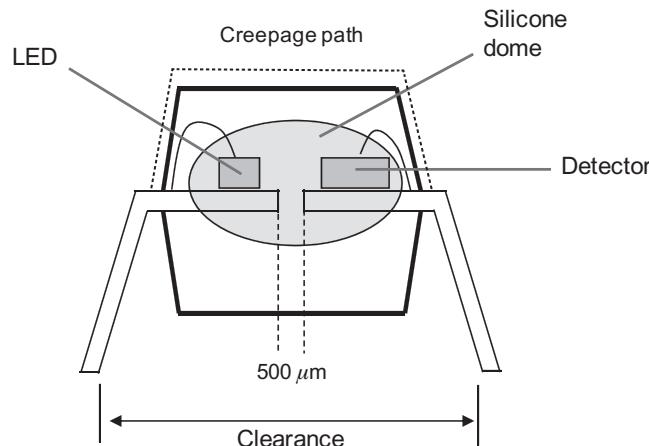


Figure 5.73 A simplified representation of an optocoupler construction.

electrical contact exists between the LED and transistor connections, the isolation is naturally created.

Current Transfer Ratio

The collector current I_c flowing in the transistor depends on the quantity of photons emitted by the LED. As the light intensity directly depends on the LED biasing current I_F , we have a relationship between both currents. This is the current transfer ratio (CTR), defined as follows:

$$\text{CTR}(\%) = \frac{I_c}{I_F} 100 \quad (5.364)$$

The CTR is affected by a lot of external parameters: temperature, LED current, transistor gain dispersions, and so on. Figure 5.74 portrays the effect of the LED forward current on the optocoupler CTR. You can see the wide variations of these parameters, as the LED current changes. The characterized element is a CEL PS2913 optocoupler.

In modern consumer power supplies, where every milliwatt counts in the no-load standby power performance, the LED driving current is reduced down to a few hundreds of microamperes. As a result, the CTR collapses and can suffer from wide lots-to-lots dispersions. For a given optocoupler, a CTR range of 60–120 percent is not an uncommon value when the LED is biased in the vicinity of a few milliamperes. This number shrinks to less than 30 percent typically when operated at a $300\text{-}\mu\text{A}$ LED current, showing a division by 4 or a -12-dB attenuation when used in a gain chain!

In isolated ac-dc converters featuring an optocoupler in the return path and regardless of the implementation (op amp, TL431, and so on), the CTR plays a role in the gain expression. Usually, this mid-band gain compensates the gain deficiency of the output stage at a frequency where you want to cross over. If you ran your compensation calculations based on the highest CTR of 120 percent, you may experience a strong error in the crossover frequency if the CTR barely reaches

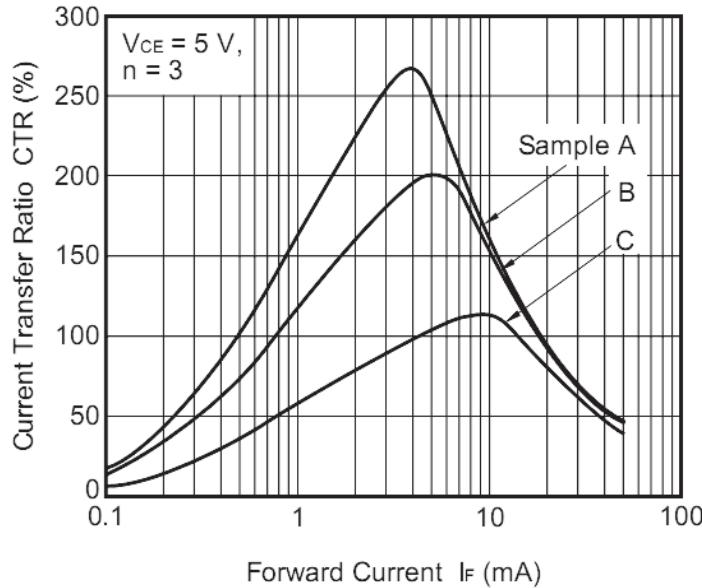


Figure 5.74 The CTR changes widely in relationship to the LED current.

30 percent at some point. In theory, the designer strives to ensure that the loop gain magnitude $|T(s)|$ passes the 0-dB axis with a -1 -slope in order to keep the phase lag at this point under control. If the loop gain experiences a 12-dB reduction because the CTR jumps from 120 percent down to 30 percent, the crossover frequency reduces by a factor of four: you initially had 1 kHz, and you end up with 250 Hz! If the available phase margin is limited in this new crossover area, the converter can experience instability problems and will fail at final test. It is thus the designer's duty to understand the CTR variations of the device he or she selected and realize that unavoidable production dispersions can degrade the phase margin at crossover.

The Optocoupler Pole

The photons emitted by the LED are collected by the collector-base area of the bipolar transistor found in the optocoupler. To maximize the collected flux, the concerned area is purposely enlarged to the detriment of the parasitic capacitance between the collector and the base. Associated to the transistor gain β , the Miller equivalent capacitor can severely hamper the compensator phase margin when used in compensator circuits. To understand the impact of this element, a typical operating configuration—regardless of the compensator type, op amp, TL431, and so on—appears in Figure 5.75. In this approach, the compensation strategy recommends that you add a capacitor between the control pin of the considered controller (labeled FB in the picture) and ground. This is C_{col} , which introduces a pole equal to

$$f_p = \frac{1}{2\pi R_{pullup}C_{col}} \quad (5.365)$$

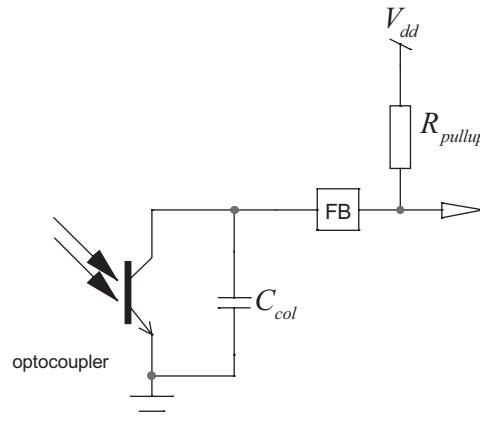


Figure 5.75 The optocoupler collector is often connected to a pull-up resistor where a stabilizing capacitor C_{col} brings a pole.

When you now connect the optocoupler to the control pin, you add its parasitic collector-emitter capacitor. This capacitor shows up in Figure 5.76, where a simplified, low-frequency, small-signal version of the optocoupler is proposed. As you can observe, this capacitor also couples with the pull-up resistor (or the pull down in a common-collector configuration) and introduces a pole at a frequency f_{opto} :

$$f_{opto} = \frac{1}{2\pi R_{pullup} C_{opto}} \quad (5.366)$$

Now, when the optocoupler capacitor couples to capacitor C_{col} you already have in place, the new pole is shifted to

$$f_p = \frac{1}{2\pi R_{pullup} (C_{col} + C_{opto})} \quad (5.367)$$

If this parasitic capacitor is large compared to C_{col} , you understand how it can distort the compensation strategy you shot for. Therefore, once the optocoupler capacitor is known, it must be subtracted from the needed capacitor you want (often

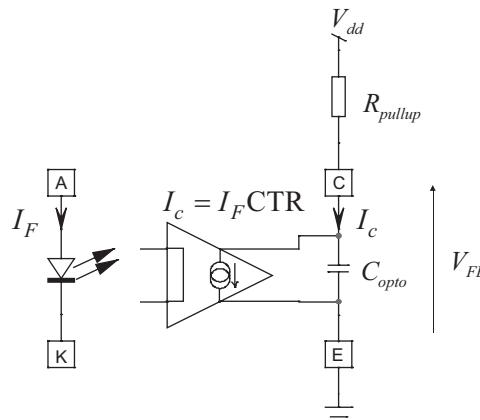


Figure 5.76 The simplified small-signal model of the optocoupler.

referred to as C_2 in the compensators) to make sure the sum of C_{opto} and C_{col} gives the right value:

$$C_{col} = C_2 - C_{opto} \quad (5.368)$$

Sometimes, it happens that C_{opto} is larger than the desired C_2 and (5.368) returns a negative value. The solution is to explore a new pole/zero combination, probably via the reduction of the selected crossover frequency. We recommend that C_{col} is at least 100 pF and placed close to the controller feedback pin. It greatly improves the immunity to spurious noises, as the feedback pin is usually high impedance and far from the optocoupler terminals.

Extracting the Optocoupler Pole

There are several ways to know the optocoupler pole position: you can read the data sheet and look for frequency response curves or timing diagrams, but the best way, in my opinion, is to set up a quick test fixture and ac sweep the optocoupler alone. That way, you know that the dc conditions and the component selection exactly match your converter implementation.

Figure 5.77 describes the way the optocoupler can be wired to unveil its pole position. The V_{bias} source fixes the dc operation point of this common-emitter configuration. You will tweak it to bring the optocoupler collector around $V_{dd}/2$ (for instance, 2 V if $V_{dd} = 5$ V), ensuring enough voltage dynamics when the ac sweep will begin. Please note that both R_{pullup} and R_{LED} can share a similar value, bringing the low frequency ac gain to the CTR value in this case. R_{bias} can be selected around a few kΩ.

The easiest way to ac sweep the circuit uses a network analyzer that will compute $20\log_{10} \frac{V(B)}{V(A)}$. The Bode plot will thus immediately appear in the computer screen. Looking for the -3-dB deviation from the low-frequency flat plateau will

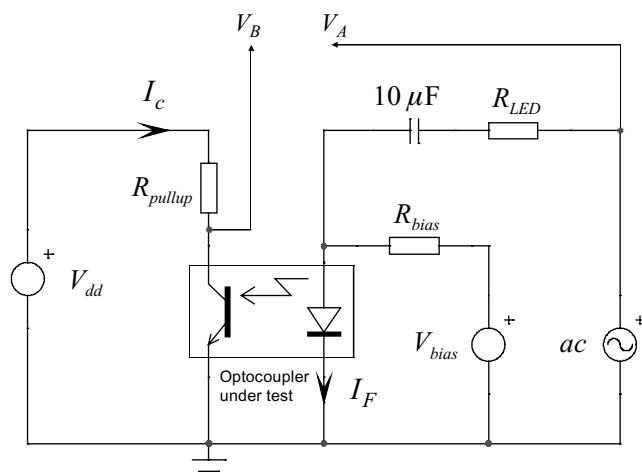


Figure 5.77 A simple test fixture biases the collector in the linear region and ac modulate the LED current.

indicate the pole position. This is what Figure 5.78 shows where the pole lies at 10 kHz. For this particular test, carried over a SFH615A-2, the pull-up resistor was set to $4.7\text{ k}\Omega$, imposing a maximum collector current around a milliampere from a 5-V V_{dd} bias source. Changing this resistor to $15\text{ k}\Omega$ rolled the pole back to 3 kHz. With a 10-kHz pole and according to (5.366), the optocoupler capacitor is 3.4 nF. In Figure 5.78, as you can see, changing the dc operating point (different V_{ce} voltages) does not affect the pole position. Please note that the optocoupler features a second pole at higher frequency. We did not account for its presence in our simplified first-order model. It must be added if you target high crossover frequencies.

Without using a network analyzer, it is still possible to find the pole position. Use a sinusoidal function generator for the ac source and observe the collector voltage with an oscilloscope at, let's say, a 100-Hz frequency. Make sure the modulation is small enough to avoid distorting the observed signal. Tweak and offset the oscilloscope vertical channel to have the signal centered at the dc collector voltage, thus equally covering the five divisions up and down from the middle of the screen. Then, change the frequency and increase it until the modulation peak amplitude drops to around 3.5 divisions (total 7 divisions peak to peak). This point corresponds to a -3-dB drop from the reference point at 100 Hz: this is the pole frequency. Figure 5.79 shows an oscilloscope shot captured during a 1-kHz pole extraction following the previous procedure.

Watch for the LED Dynamic Resistance

In equations where the fast lane is involved, the overall gain expression depends only on the following terms: the optocoupler CTR, the pull-up resistor, and the LED series resistor—see (5.66), for instance. The LED series resistor is bounded by dc operating conditions imposed by the diode forward voltage ($\approx 1\text{ V}$) and the TL431 minimum operating voltage (2.5 V). As a result, in low output voltage applications

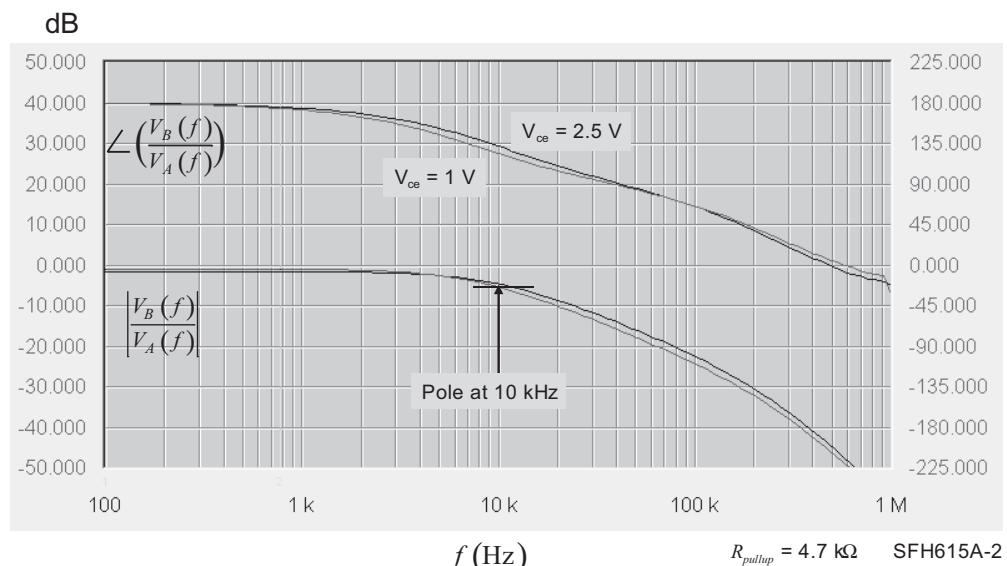


Figure 5.78 Looking at the point where the gain deviates from the low-frequency plateau by -3 dB indicates a 10-kHz pole presence.

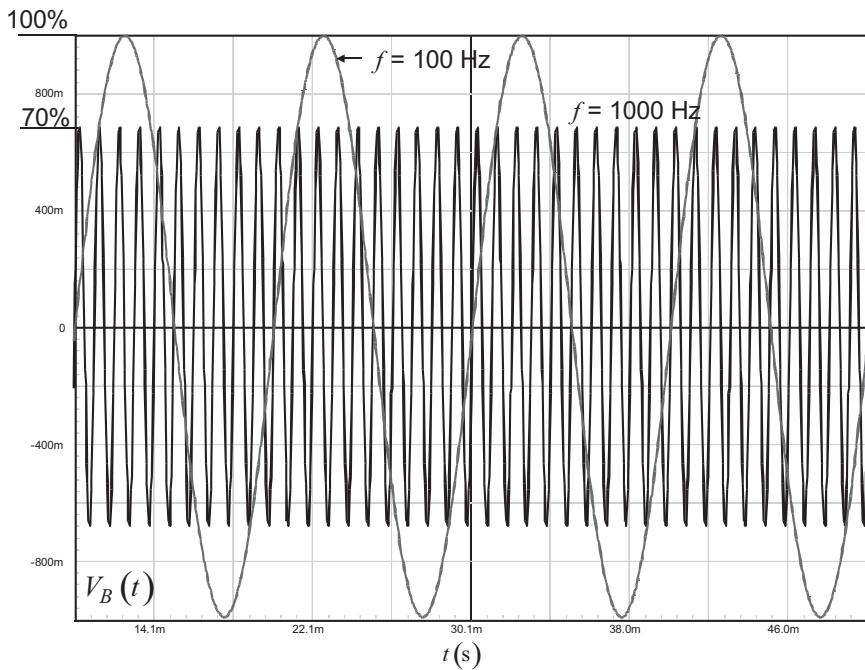


Figure 5.79 The pole extraction is straightforward with a simple oscilloscope—here, find a 1-kHz pole position.

(e.g., 5 V), this resistor can be of low value, in the vicinity of the hundred ohms. In that case, the LED dynamic resistance R_d can no longer be neglected. Furthermore, the bias resistor R_{bias} commonly installed over the LED derives a portion of the feedback current and also affects the total gain. Figure 5.80 portrays the simplified ac schematic, highlighting the elements around the LED. These small effects are often overlooked, but they can explain gain discrepancies observed in certain cases. A few equations can help us to formalize the role played by these elements and un-

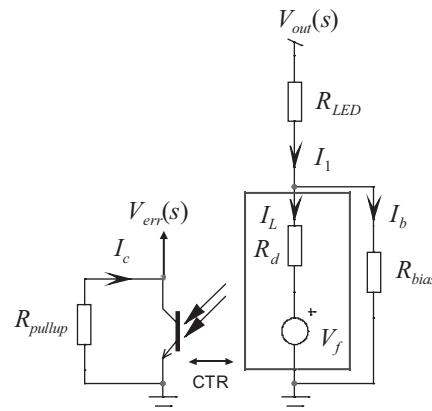


Figure 5.80 The full gain chain includes the LED series resistor and the bias generator. Both of them can affect the gain.

derstand how they interact with each other. The feedback voltage depends on the pull-up resistor and the current in it:

$$V_{err}(s) = -I_c(s)R_{pullup} = -I_L(s)R_{pullup}\text{CTR} \quad (5.369)$$

The full ac current I_1 splits between the LED and the bias resistor R_{bias} . However, the LED current, alone, participates in the feedback chain. Therefore, the bias resistor “steals” away current from the loop. Ac wise (V_f is constant and equal to 0 in ac), the LED current is expressed by

$$I_L(s) = I_1(s) \frac{R_{bias}}{R_{bias} + R_d} = \frac{V_{out}(s)}{R_{LED} + R_{bias} \parallel R_d} \frac{R_{bias}}{R_{bias} + R_d} \quad (5.370)$$

Substituting (5.370) in (5.369), we can extract the transfer function of the optocoupler chain alone:

$$\frac{V_{err}(s)}{V_{out}(s)}|_{s=0} = -\frac{R_{pullup}\text{CTR}}{R_{LED} + R_{bias} \parallel R_d} \frac{R_{bias}}{R_{bias} + R_d} \quad (5.371)$$

In this expression, both R_d and R_{bias} play a role. R_{bias} is often set to 1 kΩ in order to provide the necessary milliampere current for the TL431 biasing current. If R_d is small compared to this value, less ac current will be diverted by R_{bias} and the gain chain will not suffer from its presence. On the contrary, if R_d becomes nonnegligible, the whole chain undergoes a gain reduction. What dynamic resistance value does an optocoupler LED exhibit?

Figure 5.81 shows the characterization of such a device at different bias currents and operating temperatures. As expected, the dynamic resistance varies depending on the operating current, like any diode would do. The dynamic resistance is extracted by looking at the curve in the vicinity of the operating point and computed as the voltage variation obtained by a small current change around the considered bias region:

$$R_d = \frac{\Delta V_f}{\Delta I_d} \quad (5.372)$$

From Figure 5.81, a dynamic resistance of $\approx 160 \Omega$ is calculated with a $300-\mu\text{A}$ collector current. This is the case with modern PWM controllers that strive to reduce the consumed power in no-load conditions by hosting a high value internal pull-up resistor (usually between 10 and 20 kΩ). When the pull-up resistor is lowered to impose a 1-mA forward current ($R_{pullup} = 1 \text{ k}\Omega$), the dynamic resistance drops to $\approx 40 \Omega$. Applying (5.371) to a 5-V converter featuring the following element values— $R_{LED} = 150 \Omega$, CTR = 0.3, $R_{pullup} = 20 \text{ k}\Omega$ —we can compute the gain for various LED dynamic resistances:

$$\begin{aligned} G_1|_{R_d=0 \Omega} &\approx 32 \text{ dB} \\ G_2|_{R_d=40 \Omega} &\approx 30 \text{ dB} \\ G_3|_{R_d=160 \Omega} &\approx 25 \text{ dB} \end{aligned} \quad (5.373)$$

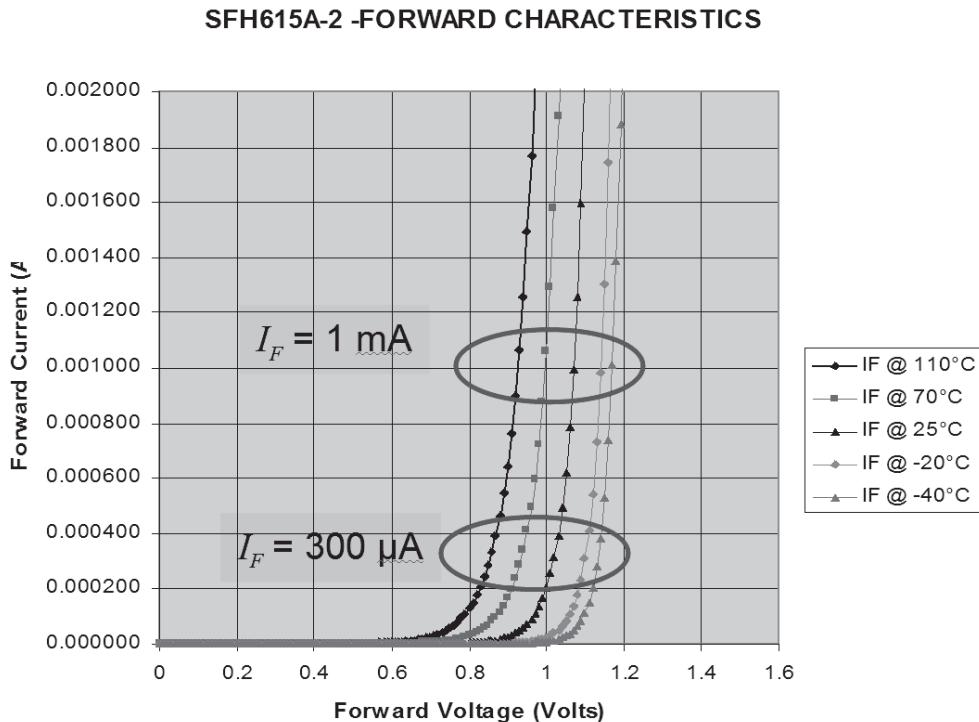


Figure 5.81 The LED dynamic resistance depends on its operating forward current.

As you can see, there is 7-dB gain difference from a calculation assuming a zero dynamic resistance and the reality of a LED operated at a low forward current. Again, a 7-dB difference in the mid-band gain can engender a crossover frequency mismatch of 2.2: you shoot for a 1-kHz crossover point and you end up below 500 Hz!

Good Design Practices

We have seen how the CTR, the LED dynamic resistance, and the parasitic pole can influence the optocoupler response. The key element to improving any of these offenders depends on the performance you are looking for. If an extremely low standby power is important while you are charging batteries (a notebook adapter, for instance), a wide bandwidth is probably not mandatory. Therefore, you can cope with a rather high pull-up resistor and a low collector current. The correspondingly low CTR value associated with a low frequency optocoupler pole will not hurt the performance in the end, as long as their natural variations are well accounted for in the design cycle. On the contrary, if time response and bandwidth are the key elements of your specifications, then make sure a low pull-up resistor value is selected (1 k Ω , for instance) to extend the optocoupler pole well beyond your crossover point and also reduce the LED dynamic resistance. You must, however, keep in mind that the optocoupler lifetime strongly depends on the LED forward current. As the optocoupler ages, the flow of emitted photons weakens and the transmission chain suffers. Operating the LED at a low current counteracts this aging process, at the expense of poor dynamic characteristics though. Some optocou-

plers compensate the LED deficiencies linked to its age, temperature, and so on. The IL300 from Vishay is one of them: a sensor monitors the LED light and modulates its operating current to keep the emitted flux constant. Please refer to the data sheet of this product for more information.

There are numerous industry-standard optocouplers manufactured by Sharp, Vishay, and CEL. Among these vendors, the PC817 and the SFH615 series are very popular. You find them in many notebook adapters and offline power supplies for TVs, DVD players, and so on. If you plan to design a high-bandwidth converter, optocouplers exhibiting high current transfer ratios (CTRs) are not recommended. To maximize the current transfer, the manufacturer will purposely grow the transistor area collecting the LED photons. By doing this, all the associated parasitic capacitances are increased, and switching times suffer. On the contrary, selecting low CTR devices will ensure a smaller internal transistor, naturally pushing away its inherent Miller capacitor.

Sometimes, when an optocoupler cannot be used, a magnetic link between the primary and secondary sides is the way to go. Reference [5] explores this solution in detail.

At the end, once the design is frozen, regardless of the isolation means, it is your duty to explore all the possible element variations with temperature and lots-to-lots dispersions in order to keep enough phase margin in all possible cases. Applying these rules is part of the recipe for a seamless mass production.

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Operational Transconductance Amplifier–Based Compensators

An operational transconductance amplifier (OTA) is a voltage-controlled current source circuit [1] affected by a transconductance factor, g_m , defined as

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}} \quad (6.1)$$

where ΔI_{out} is the amplifier output current change corresponding to a voltage change ΔV_{in} applied to its inputs.

In dc, the output current is obtained by multiplying the voltage difference ε between the noninverting pin and the inverting pin by the transconductance factor:

$$\varepsilon = V_{(+)} - V_{(-)} \quad (6.2)$$

$$I_{out} = \varepsilon g_m \quad (6.3)$$

The symbol for such an amplifier appears in Figure 6.1. You can see the transconductance value, g_m , expressed in amperes per volts or Siemens, in the international system unit. The symbols “mhos” and the reversed omega symbol \mathfrak{O} are no longer in use. Suppose the g_m in the example is $200 \mu\text{S}$; if you apply 1 V across the OTA inputs, it will deliver $200 \mu\text{A}$, inducing 200 mV across a $1\text{-k}\Omega$ resistor loading the output.

The output voltage is found using (6.3), noting that, as the inverting pin is grounded, $\varepsilon = V_{in}$:

$$V_{out} = I_{out} R_1 = V_{in} g_m R_1 \quad (6.4)$$

From this equation, the gain is simply

$$\frac{V_{out}}{V_{in}} = R_1 g_m \quad (6.5)$$

Due to this expression, we can see that by replacing R_1 with a complex network made of resistors and capacitors, we have a means to introduce poles and zeros, exactly as we did with the op amp approach.

OTAs are not very popular as standalone amplifiers. However, you often find them in power factor correction (PFC) controllers. The absence of virtual ground allows the inverting pin voltage to be used as a means to detect an overvoltage condition on the converter output. Also, designwise, they take much less die space than their op amp counterparts. Let's see the first simple OTA compensator circuit, the type 1.

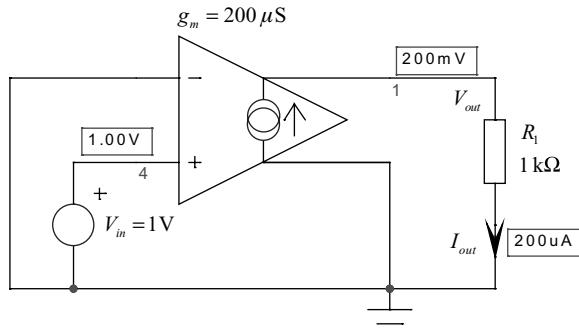


Figure 6.1 A voltage-controlled current source makes the simplest OTA. It converts the voltage measured between its inputs into an output current.

6.1 The Type 1: An Origin Pole

A type 1 circuit built on an OTA appears in Figure 6.2. The resistor of Figure 6.1 is replaced with a capacitor, C_1 . The voltage on the inverting pin is now the converter output voltage V_{out} undergoing the voltage division brought by R_1 and R_{lower} :

$$V_{(+)}(s) - V_{(-)}(s) = V_{out}(s) \frac{R_{lower}}{R_{lower} + R_1} \quad (6.6)$$

The amplifier output voltage $V_{err}(s)$ is the output current multiplied by C_1 impedance:

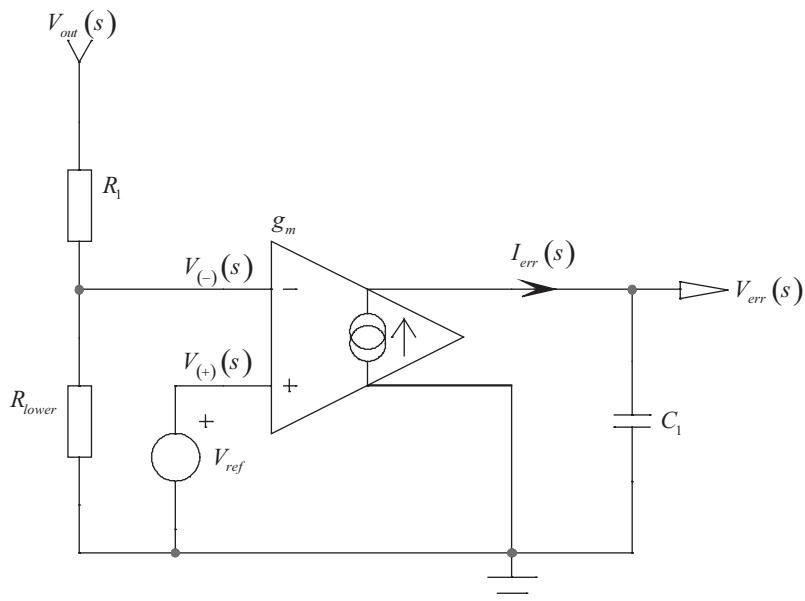


Figure 6.2 A type 1 with an OTA requires a simple capacitor connected from the output to ground.

$$V_{err}(s) = I_{err}(s) \frac{1}{sC_1} = g_m \frac{1}{sC_1} [V_{(+)}(s) - V_{(-)}(s)] \quad (6.7)$$

Substituting (6.6) into (6.7) and considering $V_{(+)}(s) = 0$ gives

$$V_{err}(s) = -g_m \frac{1}{sC_1} \frac{R_{lower}}{R_{lower} + R_1} V_{out}(s) \quad (6.8)$$

Rearranging this equation leads us to the transfer function we are looking for:

$$G(s) = \frac{V_{err}(s)}{V_{out}(s)} = -\frac{1}{sC_1 \frac{R_{lower} + R_1}{g_m R_{lower}}} = -\frac{1}{s R_{eq} C_1} \quad (6.9)$$

where the equivalent resistor is defined as

$$R_{eq} = \frac{R_{lower} + R_1}{g_m R_{lower}} \quad (6.10)$$

Equation (6.9) can be put under the familiar form

$$G(s) = -\frac{1}{\frac{s}{\omega_{po}}} \quad (6.11)$$

In which the 0-dB crossover pole definition follows

$$\omega_{po} = \frac{1}{R_{eq} C_1} = \frac{g_m R_{lower}}{(R_{lower} + R_1) C_1} \quad (6.12)$$

The biggest change compared to the op amp approach can be seen in (6.12), where the divider network and the OTA g_m parameter now enter into the equations. Regarding the divider network, in the op amp case, thanks to the virtual ground effect, both pins were at a similar potential and the ac contribution of the lower resistor R_{lower} was nonexistent. In an OTA, we do not have a local feedback from V_{err} to the inverting pin, hence the absence of virtual ground. Therefore, we cannot ignore R_{lower} any longer, as confirmed by (6.6). The OTA g_m parameter can vary depending on the care put in the integrated circuit design. Its natural variation affects the position of the 0-dB crossover pole. These details are important, and you must check how the variation in g_m changes the 0-dB crossover pole for your application. It is time for a detailed design example.

6.1.1 A Design Example

Let's assume we want a compensator transfer function with an attenuation of 25 dB at 20 Hz. For a front-end PFC regulating a 400-V output with a 2.5-V reference voltage, the upper resistor R_1 could be 4 MΩ with a lower resistor of 25 kΩ. We have selected an OTA with a 100-μS transconductance. According to formulas derived in the op amp section type 1 example, the 0-dB crossover pole is chosen depending on the required attenuation/gain and the frequency at which it occurs:

$$f_{po} = f_c G = 20 \times 10^{-\frac{25}{20}} = 1.1 \text{ Hz} \quad (6.13)$$

To place the crossover pole at this frequency, we calculate the capacitor value according to (6.12):

$$C_1 = \frac{g_m R_{lower}}{2\pi(R_{lower} + R_1)f_{po}} = \frac{100\mu \times 25k}{6.28 \times (25k + 4Meg) \times 1.1} \approx 90 \text{ nF} \quad (6.14)$$

With all the components known, we can run the simulation using the test circuit shown in Figure 6.3.

Please note that the OTA model is really the simplest possible model, a voltage-controlled current source. A more complex model would feature an upper and lower voltage clamp levels (given by the supply of the controller) plus a maximum output current limit. However, these extra components do not affect the ac response of the whole loop, and we can stay with the simplest representation.

The simulation results are delivered in Figure 6.4 and confirm our calculations. The phase lag is permanently set to 270°, which is normal for an integrator.

6.2 The Type 2: An Origin Pole plus a Pole/Zero Pair

The type 2 circuit has already been presented in the op amp section and also appears in [2]. It combines a pole zero/pair plus an origin pole for a high dc gain. The implementation using an OTA appears in Figure 6.5.

The voltage delivered by the OTA is its output current I_{err} multiplied by the loading impedance Z_L :

$$V_{err}(s) = I_{err}(s)Z_L(s) \quad (6.15)$$

The loading impedance Z_L is derived by associating two paralleled networks:

$$Z_L(s) = \left(R_2 + \frac{1}{sC_1} \right) \parallel \frac{1}{sC_2} = \frac{\left(R_2 + \frac{1}{sC_1} \right) \frac{1}{sC_2}}{\left(R_2 + \frac{1}{sC_1} \right) + \frac{1}{sC_2}} \quad (6.16)$$

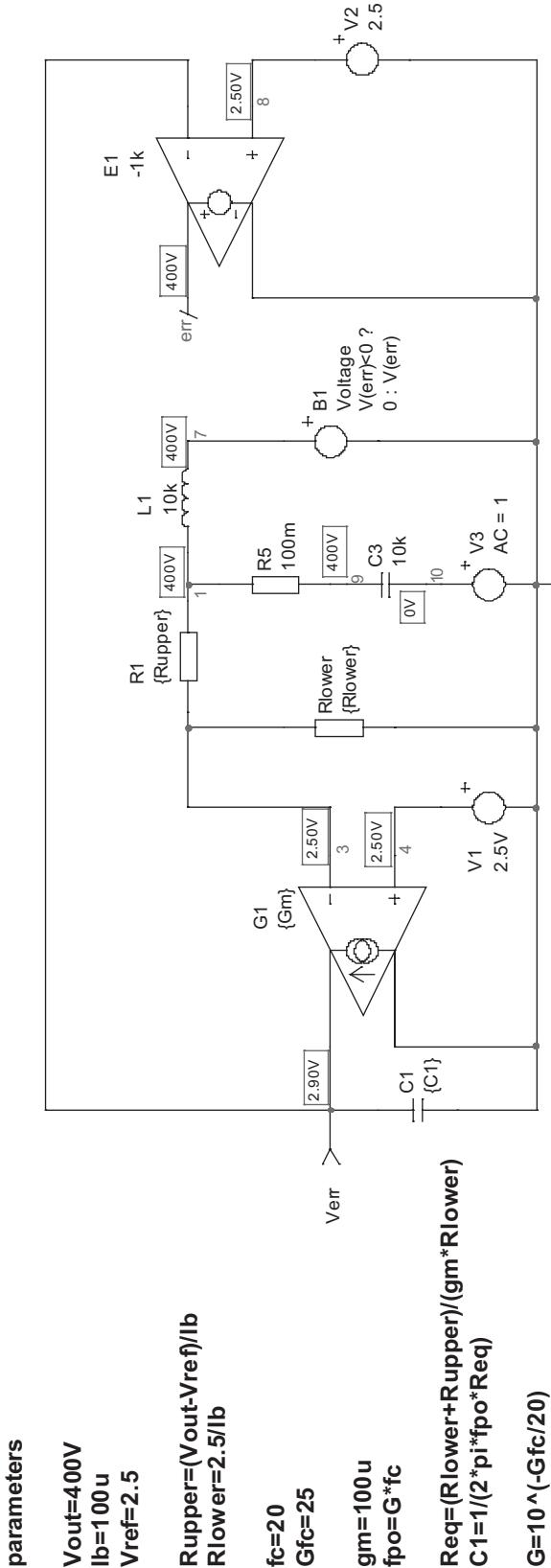
The current flowing in this network is the voltage present at the OTA inverting pin multiplied by the OTA transconductance g_m :

$$I_{err}(s) = -g_m V_{out}(s) \frac{R_{lower}}{R_{lower} + R_1} \quad (6.17)$$

Substituting (6.17) and (6.16) into (6.15), we have

$$G(s) = \frac{V_{err}(s)}{V_{out}(s)} = -g_m \frac{R_{lower}}{R_{lower} + R_1} \frac{\left(R_2 + \frac{1}{sC_1} \right) \frac{1}{sC_2}}{\left(R_2 + \frac{1}{sC_1} \right) + \frac{1}{sC_2}} \quad (6.18)$$

Rearranging (6.18), we obtain



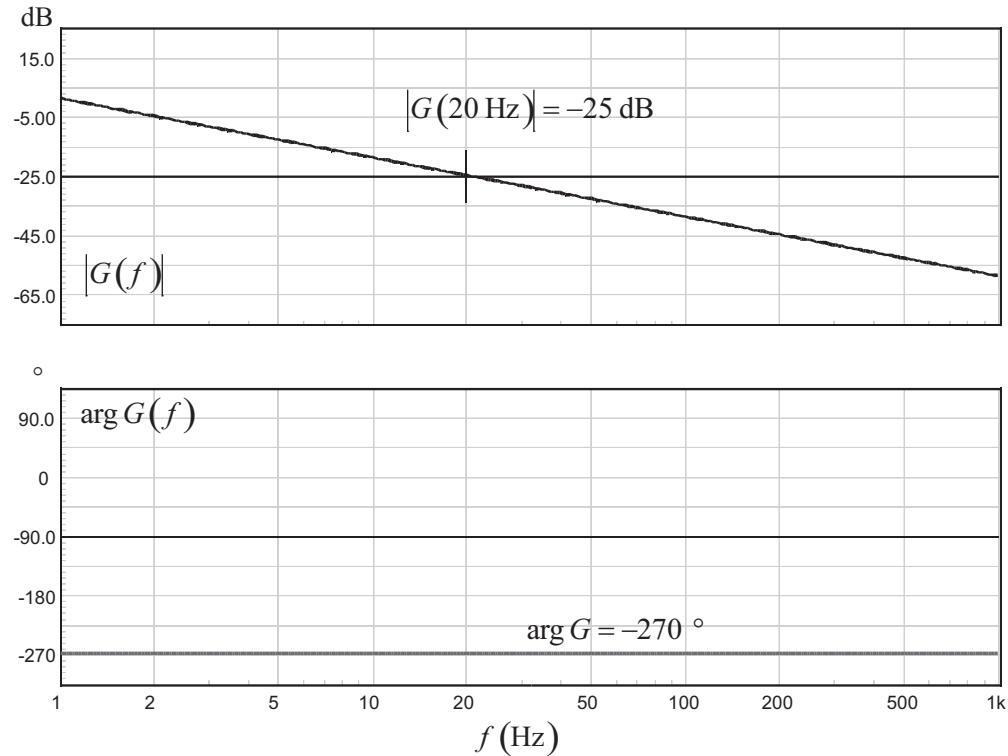


Figure 6.4 The ac results show the classical type 1 response, an integrator with a high dc-gain, crossing the -25-dB axis at 20 Hz.

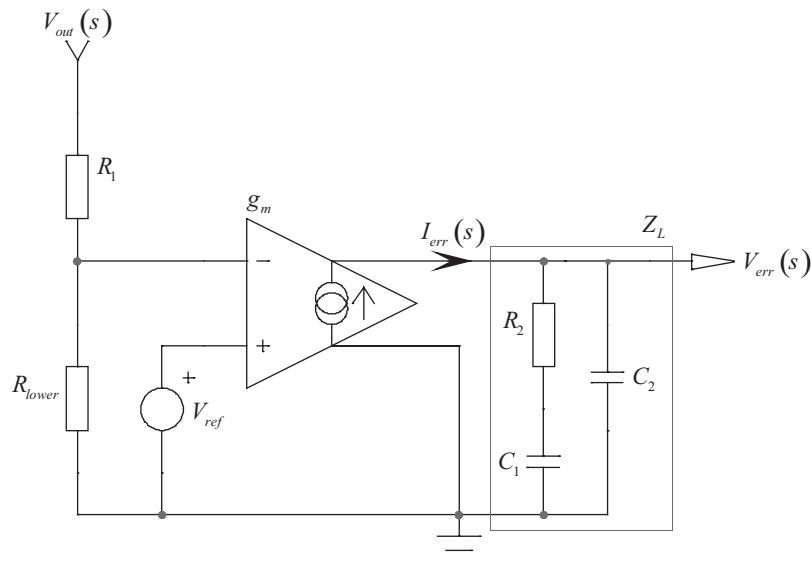


Figure 6.5 The type 2 with an OTA requires the addition of a RC network across the output capacitor C_2 .

$$G(s) = -\frac{R_{lower}g_m}{R_{lower} + R_1} \frac{1 + sR_2C_1}{s(C_1 + C_2) \left(1 + sR_2 \frac{C_1C_2}{C_1 + C_2} \right)} \quad (6.19)$$

If we now factor sR_2C_1 , we can easily unveil the poles and zeros definitions we are looking for:

$$G(s) = -\frac{R_{lower}g_m}{R_{lower} + R_1} \frac{R_2C_1}{C_1 + C_2} \frac{1 + \frac{1}{sR_2C_1}}{\left(1 + sR_2 \frac{C_1C_2}{C_1 + C_2} \right)} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (6.20)$$

In this equation, we can identify the three pertinent terms:

$$G_0 = \frac{R_{lower}}{R_{lower} + R_1} \frac{g_m R_2 C_1}{C_1 + C_2} \quad (6.21)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (6.22)$$

$$\omega_p = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \quad (6.23)$$

To extract each individual value, we have to derive the magnitude of (6.20) at the crossover frequency f_c :

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_z}{f_c} \right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_p} \right)^2}} \quad (6.24)$$

Now combining (6.21), (6.22), (6.23), and (6.24), we find the following parameters:

$$R_2 = \frac{f_p G}{f_p - f_z} \frac{(R_{lower} + R_1)}{R_{lower} g_m} \frac{\sqrt{1 + \left(\frac{f_c}{f_p} \right)^2}}{\sqrt{1 + \left(\frac{f_z}{f_c} \right)^2}} \quad (6.25)$$

$$C_1 = \frac{1}{2\pi f_z R_2} \quad (6.26)$$

$$C_2 = \frac{R_{lower} g_m}{2\pi f_p G (R_{lower} + R_1)} \frac{\sqrt{1 + \left(\frac{f_z}{f_c} \right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_p} \right)^2}} \quad (6.27)$$

In these expressions, as usual, G represents the gain or attenuation you are looking for at the selected crossover frequency f_c .

In some cases, the capacitor C_2 is much smaller than C_1 . Consequently, the gain equation greatly simplifies:

$$G(s) \approx -\frac{R_2 R_{lower} g_m}{R_{lower} + R_1} \frac{1 + \frac{1}{s R_2 C_1}}{(1 + s R_2 C_2)} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (6.28)$$

Assuming a pole/zero pair and a crossover frequency placed at the geometric mean of the pole/zero position ($f_c = \sqrt{f_p f_z}$), the component expressions are updated to

$$R_2 = \frac{G(R_{lower} + R_1)}{R_{lower} g_m} \quad (6.29)$$

$$C_1 = \frac{1}{2\pi f_z R_2} \quad (6.30)$$

$$C_2 = \frac{1}{2\pi f_p R_2} \quad (6.31)$$

Having all these elements on hand, we can proceed with a design example.

6.2.1 A Design Example

Let's re-use the type 1 OTA design example where we need to provide a 25-dB attenuation at 20 Hz. This time, we want a phase boost of 50°. Again, we assume we stabilize a PFC regulating at a 400 V output, featuring an upper resistor R_1 of 4 MΩ with a lower resistor R_{lower} of 25 kΩ. The selected OTA offers a 199-μS transconductance and the reference voltage is 2.5 V.

Where do we place our pole and zero pair? As we have detailed in the pole zero section, the pole can be placed at the following location:

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 20 = 54.8 \text{ Hz} \quad (6.32)$$

As the phase peaks at the geometric mean between the pole and the zero, this latter is placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{400}{54.8} \approx 7.3 \text{ Hz} \quad (6.33)$$

Applying the design definitions available from (6.25) through (6.27), we find

$$G = 10^{\frac{G_f c}{20}} = 10^{\frac{-25}{20}} = 0.056 \quad (6.34)$$

$$R_2 = \frac{54.8 \times 0.056}{54.8 - 7.3} \times \frac{25k + 4Meg}{25k \times 100\mu} \times \frac{\sqrt{\left(\frac{20}{54.8}\right)^2 + 1}}{\sqrt{\left(\frac{7.3}{20}\right)^2 + 1}} = 104 \text{ k}\Omega \quad (6.35)$$

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 7.3 \times 104k} = 211 \text{ nF} \quad (6.36)$$

$$C_2 = \frac{25k \times 100\mu}{6.28 \times 54.8 \times 56m \times (25k + 4Meg)} \times \frac{\sqrt{\left(\frac{7.3}{20}\right)^2 + 1}}{\sqrt{\left(\frac{20}{54.8}\right)^2 + 1}} = 32 \text{ nF} \quad (6.37)$$

The simulation schematic featuring automated calculations appears in Figure 6.6.

The results of such a simulation appears in Figure 6.7 and show the -25-dB transition occurring at 20 Hz, as expected. The boost in phase is also 50°, as required.

6.3 Optocoupler and OTA: A Buffered Connection

An OTA coupled to an optocoupler is not a very common architecture. To the author's knowledge, applications where OTAs directly drive an optocoupler are mainly those found in cell phone chargers, where the secondary-side controller hosts a dual OTA whose outputs directly bias the optocoupler LED. This is the case for the MC33341 (ON Semiconductor) or the TLE-4305 (Infineon). With this latter, the designer couples the output of the OTA to the LED via an NPN transistor wired in a common-collector configuration. Should you try to drive the LED directly from the OTA, you would end up in low-gain type of compensator, without having the ability to benefit from an origin pole. The proposed configuration appears in Figure 6.8.

In this example, the output voltage divided by the resistive bridge biases the non-inverting pin of the OTA rather than its inverting pin. This is to maintain the correct polarity on the optocoupler collector (i.e., an error voltage going down as V_{out} increases). The ac current circulating in the LED is nothing other than the buffered OTA voltage divided by the LED series resistor, R_{LED} . However, R_{LED} is not the only ohmic path crossed by this current. We have a series combination of the transistor dynamic base resistor b_{11} or r_π with the LED dynamic resistor R_d . For the sake of simplicity we will ignore them, but they obviously will affect the precision of our calculations at the end. Let's start with the voltage seen on the OTA output, $V_{op}(s)$:

$$V_{op}(s) = V_{out}(s) \frac{R_{lower}}{R_{lower} + R_1} g_m \left(R_2 + \frac{1}{sC_1} \right) \quad (6.38)$$

In ac, this voltage is found on the transistor emitter and forces a LED current equal to

$$I_{LED}(s) = \frac{V_{op}(s)}{R_{LED}} = V_{out}(s) \frac{R_{lower}}{(R_{lower} + R_1)R_{LED}} g_m \left(R_2 + \frac{1}{sC_1} \right) \quad (6.39)$$

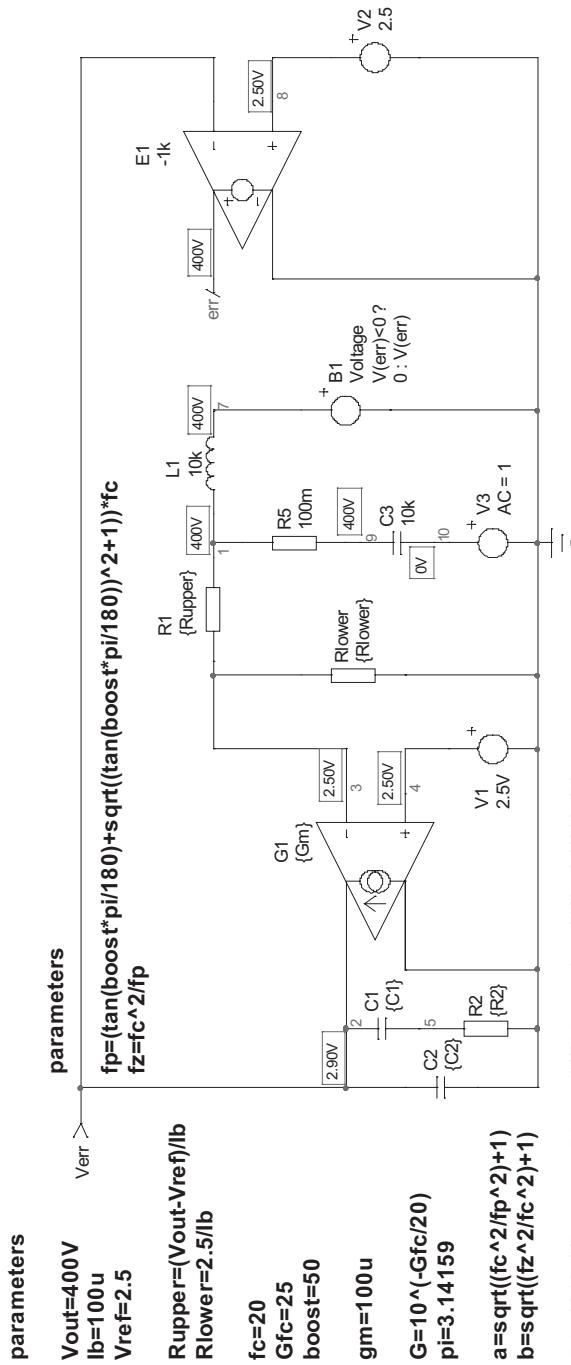


Figure 6.6 The type 2 OTA with automated calculations on the left side of the figure.

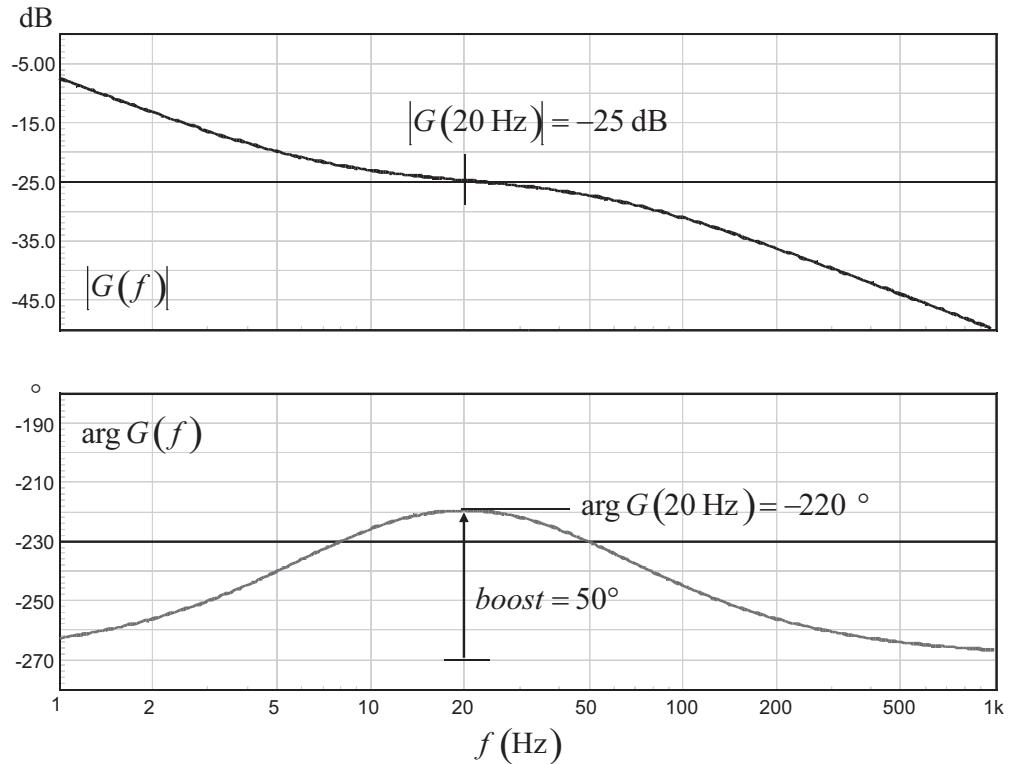


Figure 6.7 The ac simulation plots of the type 2 built with an OTA confirm the calculated results.

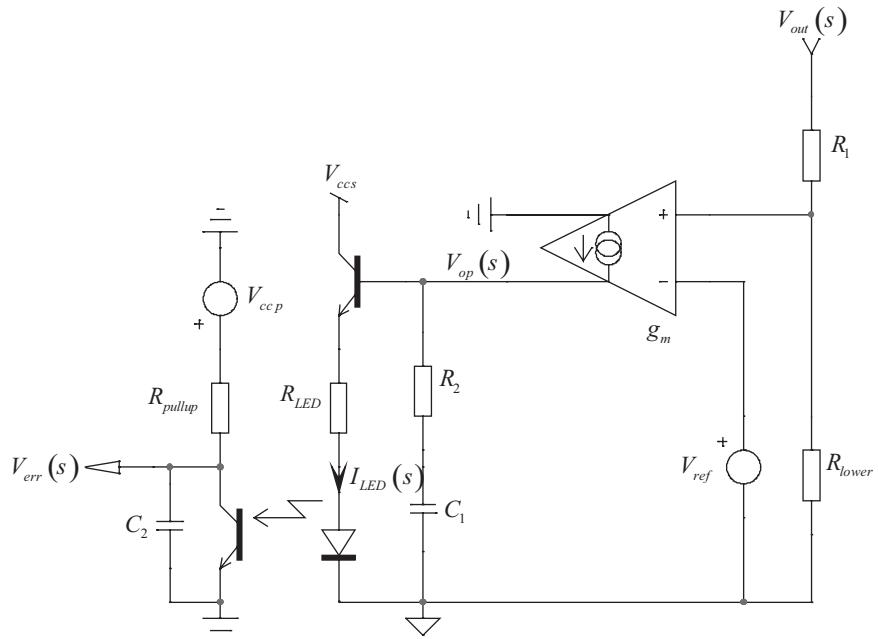


Figure 6.8 An OTA driving an optocoupler is not very common. It is sometimes found in CC-CV controllers such as the MC33341 or the TLE-4305. Please note the OTA inputs polarity as we connect the resistive divider to the noninverting pin.

When going through the optocoupler, this LED current undergoes its current transfer ratio action before crossing R_{pullup} in parallel with C_2 , further generating the error voltage, $V_{err}(s)$:

$$V_{err}(s) = -V_{out}(s) \frac{R_{lower} R_{pullup}}{(R_{lower} + R_1) R_{LED}} g_m \text{CTR} \left(R_2 + \frac{1}{sC_1} \right) \frac{1}{1 + sR_{pullup}C_2} \quad (6.40)$$

By rearranging this equation, we can derive the complete compensator transfer function:

$$G(s) = \frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{lower}}{R_{lower} + R_1} \frac{g_m R_{pullup} R_2 \text{CTR}}{R_{LED}} \frac{1 + 1/sR_2C_1}{1 + sR_{pullup}C_2} \quad (6.41)$$

We can put it under a more familiar form as follows:

$$G(s) = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (6.42)$$

Where we can identify

$$G_0 = \frac{R_{lower}}{R_{lower} + R_1} \frac{g_m R_{pullup} R_2 \text{CTR}}{R_{LED}} \quad (6.43)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (6.44)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (6.45)$$

The OTA is a current generator but still, its upper output voltage capability, VOH, is limited by its dc supply. This imposes a design constraint on the LED resistor. The voltage across the OTA must be high enough to let the optocoupler collector pull the feedback pin to ground. Based on the exercise already done in the op amp section, the LED resistor must be smaller than:

$$R_{LED} \leq \frac{R_{pullup} \text{CTR}_{\min} (\text{VOH} - V_{BE} - V_f)}{V_{ccp} - V_{CE,sat}} \quad (6.46)$$

In some circuits, the LED resistor is internally fixed and you will need to check if it complies with the recommended value in (6.46).

6.3.1 A Design Example

Let us try to stabilize the voltage loop of a converter operated in CC-CV. We assume a 10-dB gain at 1 kHz together with a 50° phase boost are required at this point. Suppose we have the following parameters:

$\text{VOH} = 5 \text{ V}$; the OTA maximum output voltage.

$V_f = 1 \text{ V}$; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{BE} = 0.65$ V; the OTA bipolar transistor base-emitter voltage.

$V_{ccp} = 5$ V; the pull-up V_{cc} level on the primary side.

$V_{ccs} = 5$ V; the V_{cc} power supply level on the secondary side.

$R_{pullup} = 20 \text{ k}\Omega$; the optocoupler pull-up resistor.

$g_m = 1 \text{ mS}$; the OTA transconductance value.

$\text{CTR}_{\min} = 0.3$; the minimum optocoupler current transfer ratio.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$R_{lower} = 10 \text{ k}\Omega$; the lower resistor in the resistor bridge observing the output variable.

$f_{opto} = 6 \text{ kHz}$; the optocoupler pole that has been characterized with R_{pullup} .

With these elements on hand, let us calculate with (6.46) the maximum acceptable LED series resistor we can select:

$$R_{LED,\max} = \frac{R_{pullup} \text{CTR} (\text{VOH} - V_{BE} - V_f)}{V_{ccp} - V_{CE,sat}} = \frac{20k \times 0.3 \times (5 - 0.65 - 1)}{5 - 0.3} = 4.3 \text{ k}\Omega \quad (6.47)$$

The adopted integrated circuit, the TLE-4305, includes a 1-kΩ resistor in series with the transistor emitter, so we are safe. Now, let's see where to place the poles and zeros to obtain the 50° phase boost we need at the selected 1-kHz crossover frequency:

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 1k = 2.74 \text{ kHz} \quad (6.48)$$

Since the phase peaks at the geometric mean between the pole and the zero, the latter is placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{1k^2}{2.74k} \approx 365 \text{ Hz} \quad (6.49)$$

To properly adjust the mid-band gain, we need to evaluate the value of R_2 . Starting from (6.42), we can extract the magnitude of the compensator and then solve for the resistor value. Following this option, we have

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_z}{f_c}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_p}\right)^2}} \quad (6.50)$$

Substituting G_0 from (6.43) in (6.50) and solving for R_2 , we have

$$R_2 = \frac{G(R_{lower} + R_1)R_{LED}}{R_{lower}R_{pullup}g_m \text{CTR}} \frac{\sqrt{1 + \left(\frac{f_c}{f_p}\right)^2}}{\sqrt{1 + \left(\frac{f_z}{f_c}\right)^2}} \quad (6.51)$$

In this equation, G corresponds to the gain/attenuation required at the cross-over frequency. Here, we need a 10-dB gain:

$$G = 10^{\frac{Gf_c}{20}} = 10^{\frac{10}{20}} = 3.16 \quad (6.52)$$

If we introduce this value in (6.51), we find R_2 equals $2.5\text{ k}\Omega$. The capacitors values for C_1 and C_2 are straightforward, owing to (6.44) and (6.45):

$$C_1 = \frac{1}{2\pi R_2 f_z} = \frac{1}{6.28 \times 2.5k \times 365} = 174 \text{ nF} \quad (6.53)$$

The total capacitor needed to form the pole at 2.74 kHz with the pull-up resistor is found to be

$$C_2 = \frac{1}{2\pi f_p R_{pullup}} = \frac{1}{6.28 \times 2.74k \times 20k} = 2.9 \text{ nF} \quad (6.54)$$

We know that this value is actually made of an external capacitor placed in parallel with the parasitic capacitor of the optocoupler:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} = 1.3 \text{ nF} \quad (6.55)$$

As a result, C_{col} is evaluated to

$$C_{col} = C_2 - C_{opto} = 2.9n - 1.3n = 1.6 \text{ nF} \quad (6.56)$$

We now have everything on hand. The test fixture appears in Figure 6.9 and shows correct operating bias points for a 12-V output. Please note the presence of clamping diodes D_1 and D_2 that limits the upper and lower excursion of the voltage-controlled current source during the bias point calculation.

The ac results appear in Figure 6.10 and show a slight discrepancy between the target (10 dB of gain) and the obtained result. This is mainly due to the cumulative effects of the dynamic resistors from the base-emitter junction (b_{11} or r_π) and from the LED diode. The 1.5-dB error can easily be compensated by increasing the target by 1.5 dB, thus shooting for 11.5 dB. The boost of 50° is well respected, though.

6.4 The Type 3: An Origin Pole and a Pole/Zero Pair

By combining an RC network across the upper resistor R_1 , it is possible to build a type 3 with an OTA. However, we will soon learn that the implication of the divider network plays a harmful role in the final transfer function. The proposed implementation appears in Figure 6.11. To obtain the transfer function, we must evaluate the input and loading impedances, noted Z_i and Z_L , respectively.

We know that the output current of the OTA depends on the voltage difference developed between its inputs. In ac, the voltage on the inverting pin depends on the divider network. Therefore,

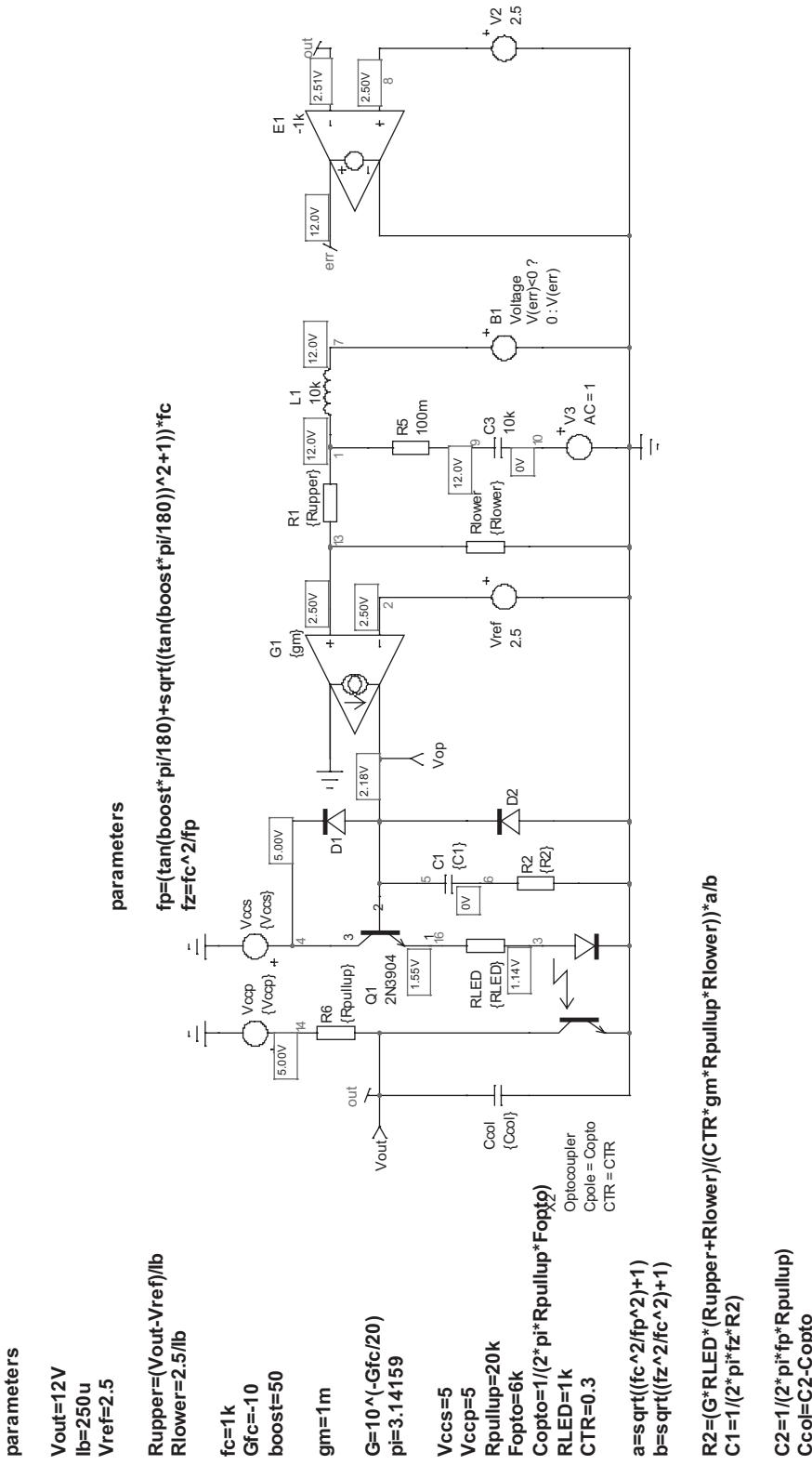


Figure 6.9 The test fixture includes the OTA driving the optocoupler LED via a NPN transistor.

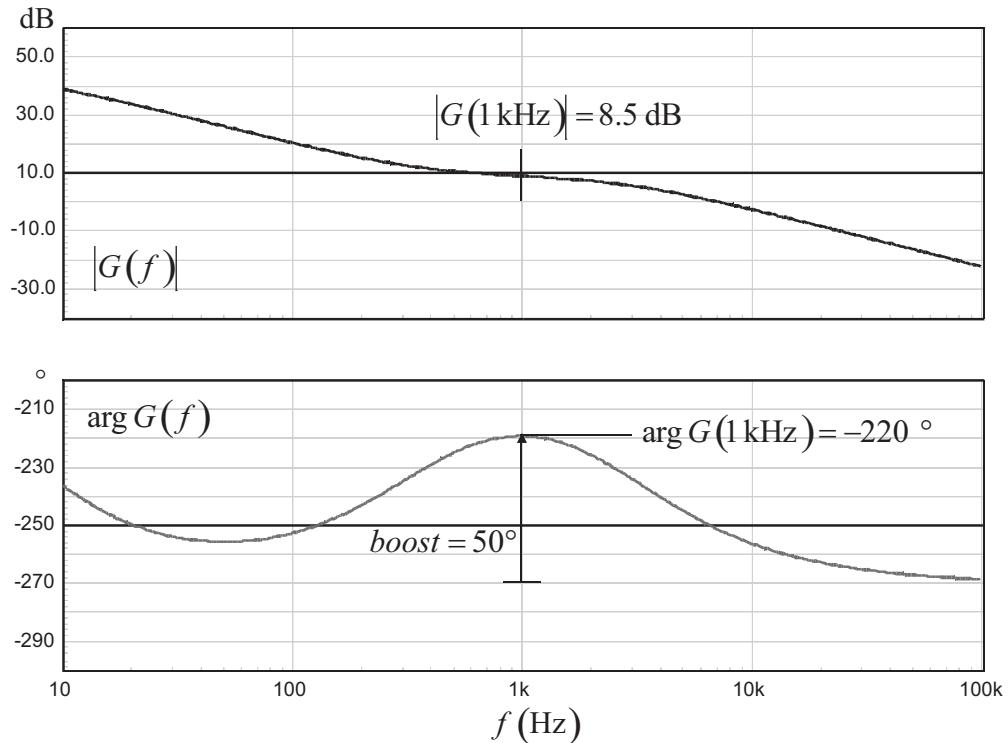


Figure 6.10 The ac sweep confirms the phase boost amplitude at 1 kHz, but we miss the target by 1.5 dB. This is because of the dynamic resistors offered by the bipolar transistors and the LED.

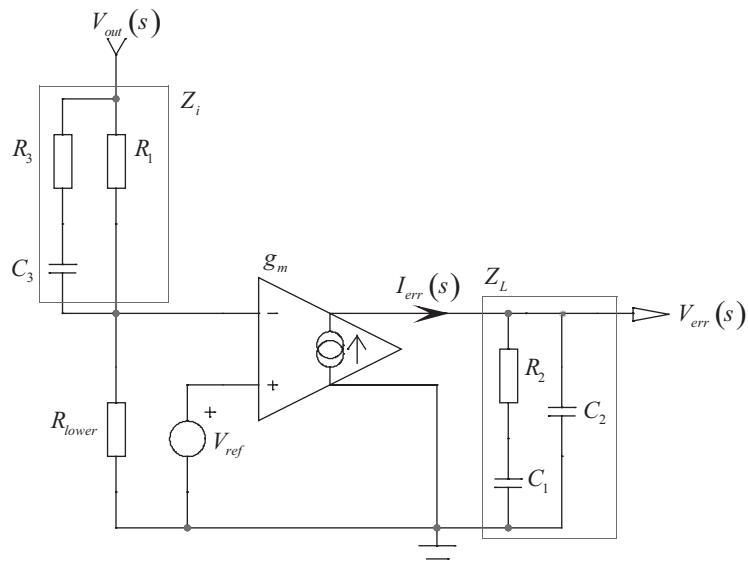


Figure 6.11 A type 3 can be built with an OTA; however, it is less flexible than with an op amp-based solution.

$$I_{err}(s) = -g_m V_{out}(s) \frac{R_{lower}}{R_{lower} + Z_i(s)} \quad (6.57)$$

The complex impedance $Z_i(s)$ can be calculated as follows:

$$Z_i(s) = \frac{\frac{sR_3C_3 + 1}{sC_3} R_1}{\frac{sR_3C_3 + 1}{sC_3} + R_1} = \frac{\frac{sR_3C_3 + 1}{sC_3} R_1}{\frac{sR_3C_3 + 1}{sC_3} + \frac{sR_1C_3}{sC_3}} = R_1 \frac{sR_3C_3 + 1}{sC_3(R_3 + R_1) + 1} \quad (6.58)$$

We can now update (6.57):

$$I_{err}(s) = -g_m V_{out}(s) \frac{R_{lower}}{R_{lower} + \frac{R_1(sR_3C_3 + 1)}{sC_3(R_3 + R_1) + 1}} \quad (6.59)$$

Rearranging this equation gives

$$I_{err}(s) = -g_m V_{out}(s) \frac{R_{lower}}{R_{lower} + R_1} \frac{sC_3(R_3 + R_1) + 1}{sC_3 \left(\frac{R_{lower}R_1}{R_{lower} + R_1} + R_3 \right) + 1} \quad (6.60)$$

As the OTA output current flows in a complex network Z_L , we can calculate its equivalent impedance and get the transfer function immediately:

$$Z_L(s) = (R_2 + C_1) \parallel C_2 = \frac{\left(R_2 + \frac{1}{sC_1} \right) \frac{1}{sC_2}}{\left(R_2 + \frac{1}{sC_1} \right) + \frac{1}{sC_2}} \quad (6.61)$$

Since $V_{out}(s) = I_{err}(s) Z_L(s)$, we simply multiply (6.60) by (6.61) and obtain

$$G(s) = -g_m \frac{R_{lower}}{R_{lower} + R_1} \frac{sC_3(R_3 + R_1) + 1}{sC_3 \left(\frac{R_{lower}R_1}{R_{lower} + R_1} + R_3 \right) + 1} \frac{\left(R_2 + \frac{1}{sC_1} \right) \frac{1}{sC_2}}{\left(R_2 + \frac{1}{sC_1} \right) + \frac{1}{sC_2}} \quad (6.62)$$

Developing and arranging (6.62) leads to

$$G(s) = -\frac{R_{lower} g_m}{R_{lower} + R_1} \frac{sC_3(R_3 + R_1) + 1}{\left[sC_3 \left(\frac{R_{lower}R_1}{R_{lower} + R_1} + R_3 \right) + 1 \right] \left[s(C_1 + C_2) \left(1 + sR_2 \frac{C_1C_2}{C_1 + C_2} \right) \right]} \quad (6.63)$$

Factoring $1 + sR_2C_1$, we have

$$G(s) = -\frac{R_{lower}}{R_{lower} + R_1} \frac{g_m R_2 C_1}{C_1 + C_2} \left[\frac{1 + 1/sR_2 C_1}{sC_3 \left(\frac{R_{lower} R_1}{R_{lower} + R_1} + R_3 \right) + 1} \right] \left[\frac{sC_3(R_3 + R_1) + 1}{1 + sR_2 \frac{C_1 C_2}{C_1 + C_2}} \right] \quad (6.64)$$

This expression can be put in the normalized form:

$$G(s) = -G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right) \left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right) \left(1 + \frac{s}{\omega_{p_2}}\right)} \quad (6.65)$$

where

$$G_0 = \frac{R_{lower}}{R_{lower} + R_1} \frac{g_m R_2 C_1}{C_1 + C_2} \quad (6.66)$$

$$\omega_{z_1} = \frac{1}{R_2 C_1} \quad (6.67)$$

$$\omega_{z_2} = \frac{1}{(R_1 + R_3) C_3} \quad (6.68)$$

$$\omega_{p_1} = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \quad (6.69)$$

$$\omega_{p_2} = \frac{1}{\left(\frac{R_{lower} R_1}{R_{lower} + R_1} + R_3 \right) C_3} \quad (6.70)$$

From these values, we need to extract the design expressions that will let us calculate the passive component values. We first need the magnitude of G at the selected crossover frequency:

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} = \frac{R_{lower} g_m}{R_{lower} + R_1} \frac{R_2 C_1}{C_1 + C_2} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (6.71)$$

Then, by using (6.67), (6.68), (6.69), (6.70), and (6.71), we can solve for R_2 , R_3 , C_1 , C_2 and C_3 :

$$R_2 = \frac{G(R_1 + R_{lower}) f_{p_1}}{R_{lower} g_m (f_{p_1} - f_{z_1})} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (6.72)$$

$$R_3 = \frac{R_1^2 f_{z_2} - R_1 R_{lower} (f_{p_2} - f_{z_2})}{(f_{p_2} - f_{z_2})(R_1 + R_{lower})} \quad (6.73)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad (6.74)$$

$$C_2 = \frac{C_1}{2\pi C_1 R_2 f_{p_1} - 1} \quad (6.75)$$

$$C_3 = \frac{1}{2\pi(R_1 + R_3)f_{z_2}} \quad (6.76)$$

We can try to simplify these equations a little bit by recognizing that very often $C_2 \ll C_1$; however, the final equations will still remain quite complex. In fact, the equation defining R_3 , (6.73), can become negative, simply meaning that the needed distance between the second pole and the second zero cannot be achieved. To determine what the limit is, let us observe the sign of (6.73) by checking its numerator. Since R_1 can be factorized and is always positive, we can exclude it from the sign study. Therefore, we have

$$R_1 f_{z_2} - R_{lower} (f_{p_2} - f_{z_2}) > 0 \quad (6.77)$$

Solving this equation leads to

$$\frac{f_{p_2}}{f_{z_2}} < \frac{R_1}{R_{lower}} + 1 \quad (6.78)$$

The right term once multiplied by the reference voltage V_{ref} gives the targeted output voltage. Capitalizing on this remark, we have

$$\frac{f_{p_2}}{f_{z_2}} < \frac{V_{out}}{V_{ref}} \quad (6.79)$$

In other words, when the output voltage is large relative to the reference voltage, for instance, a 48-V output and a 2.5-V reference voltage, we have the ability to spread both the second pole and zero by a ratio of around 19, opening possibilities for the phase boost selection. Unfortunately, for a lower output voltage (e.g., a 5-V output with a 2.5-V reference), you cannot have more than a ratio of 2 between the second pole and the second zero, drastically limiting the total available phase boost. This limits the type 3 implementation with an OTA.

Let's try to derive the phase boost brought by a pole and a zero distant by a certain ratio r :

$$\frac{f_p}{f_z} = r \quad (6.80)$$

We know that the phase boost peaks at the geometric mean between the pole and the zero, and this is where the crossover frequency is usually placed. Otherwise stated, we have

$$f_c = \sqrt{f_p f_z} \quad (6.81)$$

Now, as the pole and the zero are linked by (6.80), a new relationship between the crossover frequency and the pole/zero pair can be derived:

$$f_c = f_z \sqrt{r} = \frac{f_p}{\sqrt{r}} \quad (6.82)$$

A transfer function featuring a pole and a zero obeys the following form:

$$G(s) = \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}} \quad (6.83)$$

The phase boost at the crossover angular frequency ω_c or the frequency f_c brought by such pole/zero arrangement is found by subtracting the denominator argument to that of the numerator:

$$\text{boost} = \tan^{-1} \frac{\omega_c}{\omega_z} - \tan^{-1} \frac{\omega_c}{\omega_p} = \tan^{-1} \frac{f_c}{f_z} - \tan^{-1} \frac{f_c}{f_p} \quad (6.84)$$

If we now substitute the crossover frequency definition given by (6.82) into (6.84), we find that the pole and zero absolute locations disappear and only the ratio between them, r , remains

$$\text{boost} = \tan^{-1} \frac{f_z \sqrt{r}}{f_z} - \tan^{-1} \frac{f_p}{\sqrt{r} f_p} = \tan^{-1} \sqrt{r} - \tan^{-1} \frac{1}{\sqrt{r}} \quad (6.85)$$

To arrange this expression, we need to use a known trigonometric relationship:

$$\tan^{-1} \frac{1}{r} + \tan^{-1} r = \frac{\pi}{2} \quad (6.86)$$

From (6.86), we can extract the definition of $\tan^{-1} 1/r$:

$$\tan^{-1} \frac{1}{r} = \frac{\pi}{2} - \tan^{-1} r \quad (6.87)$$

If we substitute this expression into (6.85), we have

$$\text{boost} = \tan^{-1} \sqrt{r} - \frac{\pi}{2} + \tan^{-1} \sqrt{r} = 2 \tan^{-1} \sqrt{r} - \frac{\pi}{2} \quad (6.88)$$

Using the previous formula, we now have a means to predict the phase boost peak brought by a pole/zero pair depending on the distance between them. We consider that the peak occurs at the geometric mean. In a type 3 compensator, we have two pole/zero pairs. The first one involves the impedance loading of the OTA. This first pair is not affected by any limit implying that the pole and zero can be spread up to a maximum of 90° phase boost. On top of this phase boost, you add

the second pole/zero pair; however, it is limited in spread by (6.79). The total phase boost will thus be 90° plus the one brought by the second pole/zero pair. Assume we have the two converters, one delivering 48 V and the second 5 V from a 2.5-V reference voltage. With the first one, given the ratio of 19 between V_{out} and V_{ref} , we could obtain an extra phase boost from the second pole/zero pair of

$$boost_{48V} = 2 \tan^{-1} \sqrt{19} - 90^\circ = 64^\circ \quad (6.89)$$

bringing the total available phase boost to $90 + 64 = 154^\circ$. On the contrary, for the 5-V converter, given the ratio of 2.5 between V_{out} and V_{ref} , the extra phase boost would be limited to

$$boost_{5V} = 2 \tan^{-1} \sqrt{2.5} - 90^\circ = 25^\circ \quad (6.90)$$

This would not allow a phase boost larger than $90^\circ + 25^\circ = 115^\circ$.

6.4.1 A Design Example

We want to stabilize a 19-V power supply obtained from a 2.5-V reference voltage. The ratio between the output voltage and the reference is $19/2.5 = 7.6$. To obtain this voltage from a 2.5-V reference voltage, we have R_1 equal to $66 \text{ k}\Omega$ and R_{lower} is $10 \text{ k}\Omega$. Looking at (6.79), the pole and zero distance cannot be larger than

$$\frac{f_{p_2}}{f_{z_2}} < 7.6 \quad (6.91)$$

From (6.88), we can check what maximum phase boost we can expect from the second pole/zero pair position:

$$boost_{19V} = 2 \tan^{-1} \sqrt{7.6} - 90^\circ = 50^\circ \quad (6.92)$$

In other words, the maximum phase boost we will get from the OTA wired in the type 3 configuration will have to stay smaller than

$$boost_{max} = 90^\circ + 50^\circ = 140^\circ \quad (6.93)$$

When selecting the crossover frequency, you will have to account from the previous value to make sure the phase boost at the selected crossover point will be realizable (e.g., less than 140°). Let's assume we want 130° at a 1-kHz crossover frequency, a point where the loop needs a 15-dB of amplification. G , in this case, is simply

$$G = 10^{\frac{15}{20}} = 10^{\frac{15}{20}} = 5.6 \quad (6.94)$$

Knowing that we can get 50° from the second pole/zero pair, we are going to spread the first pole/zero pair to reach 80° so that the sum of both phase boosts gives us the 130° we are looking for. To obtain the 80° phase boost from the pole f_{p1} and the zero f_{z1} , we will place them at a certain distance from the 1-kHz crossover frequency. This distance is calculated by extracting r from (6.88):

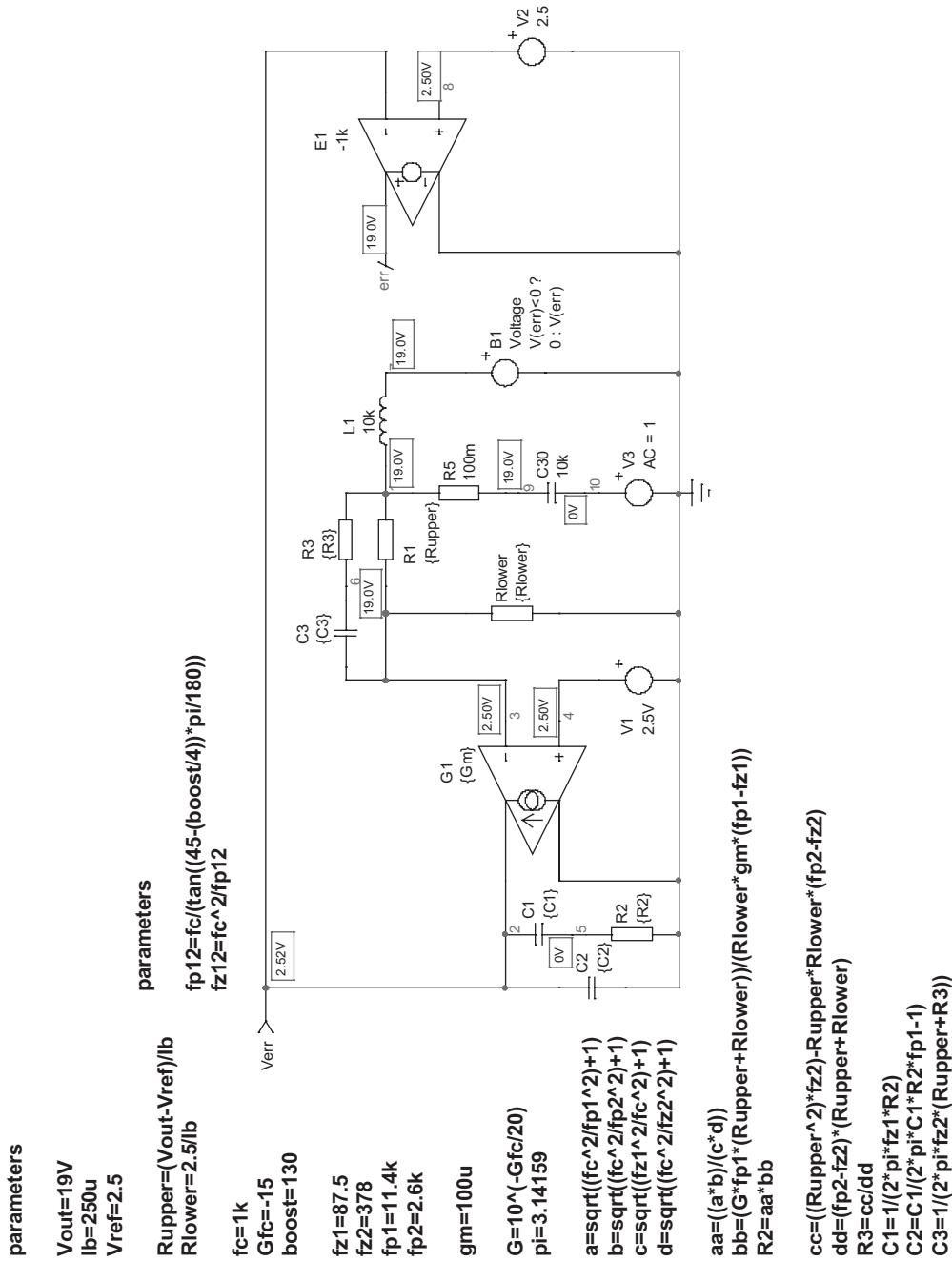


Figure 6.12 The OTA wired in a type 3 configuration is less flexible than its op amp counterpart.

$$r = \left[\tan\left(\frac{boost}{2} + \frac{\pi}{4}\right) \right]^2 \approx 130 \quad (6.95)$$

By rearranging (6.82), we can easily extract the first pole and the first zero positions in relationship to the crossover frequency f_c :

$$f_{z_1} = \frac{f_c}{\sqrt{r}} = \frac{1k}{\sqrt{130}} = 87.5 \text{ Hz} \quad (6.96)$$

$$f_{p_1} = f_c \sqrt{r} = 1k \times \sqrt{130} = 11.4 \text{ kHz} \quad (6.97)$$

From (6.91), we know that the distance between the second pole and zero have to be less than 7.6 (7 is used for safety margin). Positioned in relation to the 1-kHz crossover frequency, they have to be placed at the following positions:

$$f_{z_2} = \frac{f_c}{\sqrt{r}} = \frac{1k}{\sqrt{7}} = 378 \text{ Hz} \quad (6.98)$$

$$f_{p_2} = f_c \sqrt{r} = 1k \times \sqrt{7} = 2.6 \text{ kHz} \quad (6.99)$$

Applying (6.72) to (6.76), we find the following values for the passive elements placed around the OTA:

$$C_1 = 11.2 \text{ nF}$$

$$C_2 = 86 \text{ pF}$$

$$C_3 = 6.3 \text{ nF}$$

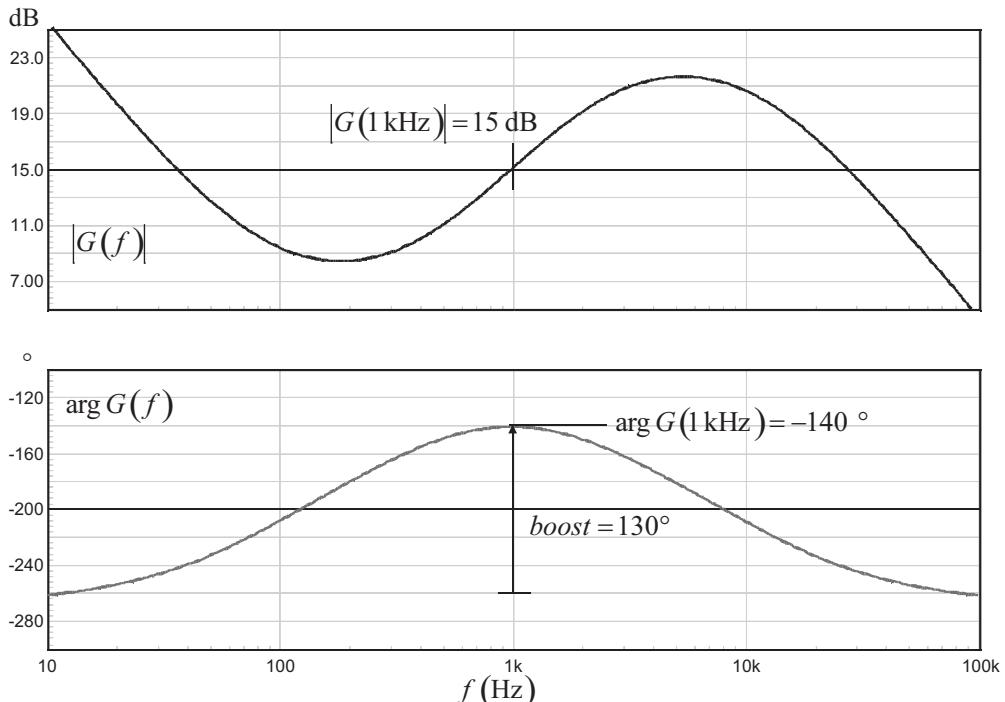


Figure 6.13 The ac response of the type 3 OTA confirms the realization of the desired phase boost.

$$R_2 = 163 \text{ k}\Omega$$

$$R_3 = 1.05 \text{ k}\Omega$$

The test fixture appears in Figure 6.12, where the automation of the component values resides on the left side of the schematic. The bias point confirms the 19-V input setpoint. Once the ac sweep has been performed, the results appear in Figure 6.13.

6.5 Conclusion

An OTA does not offer the same design flexibility as an op amp does. However, as explained, IC designers like the structure because of the small semiconductor die size it requires. The lack of virtual ground makes the lower side divider resistor enter the equations and requires attention when deriving poles and zeros placement. Depending on the ratio between the output and the reference voltages, it can hamper the second pole/zero pair placement in a type 3 configuration. For this reason, the OTA is rarely used in these configurations and must remain a designer choice for type 2 or 1 applications.

Appendix 6A: Summary Pictures

Figures 6.14 through 6.16 summarize the component definitions associated with the structures described in the chapter.

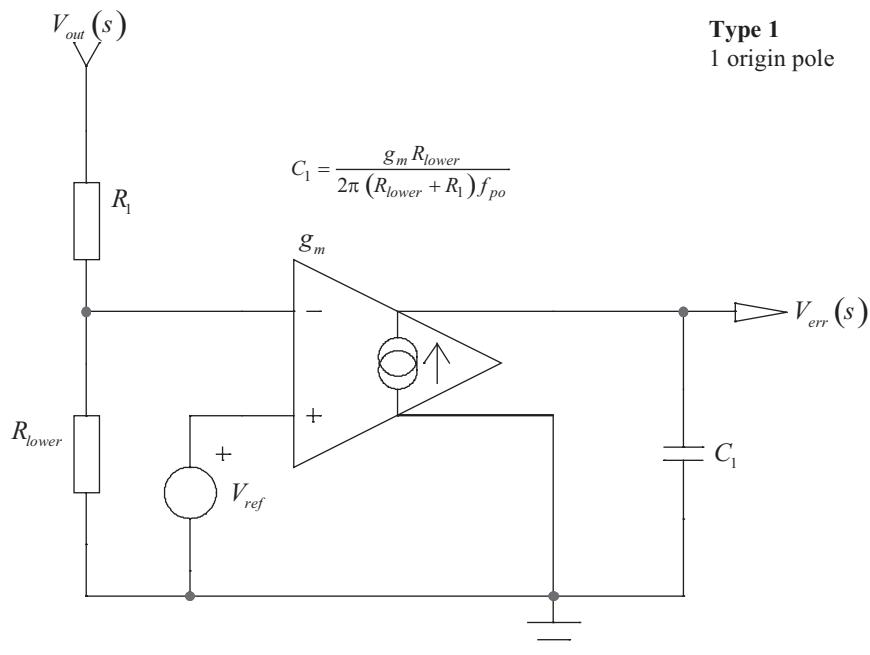


Figure 6.14 The type 1.

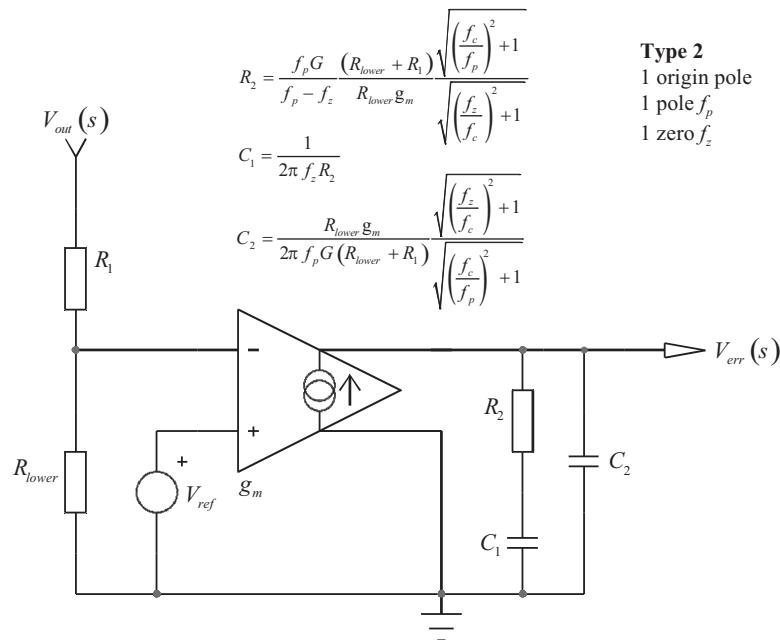


Figure 6.15 The type 2.

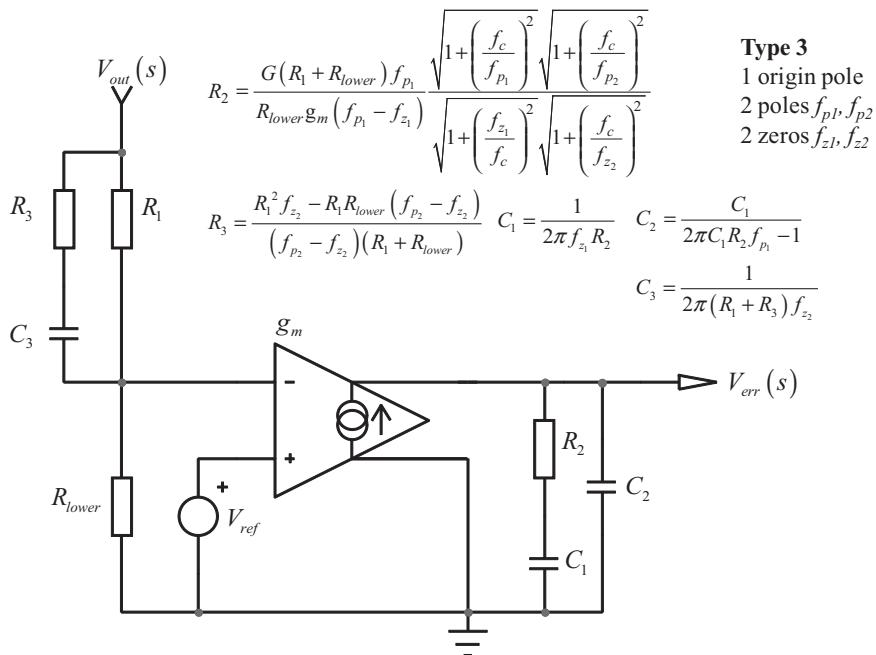


Figure 6.16 The type 3.

References

- [1] Gratz, A., "Operational Transconductance Amplifiers," <http://synth.stromeko.net/diy/OTA.pdf>.
- [2] Bassi, C., Switch Mode Power Supplies: SPICE Simulations and Practical Designs, New York: McGraw-Hill, 2008.

TL431-Based Compensators

The technical literature on loop control abounds with design examples of compensators implementing an operational amplifier (op amp). If the op amp certainly represents a possible way to generate an error signal, the industry choice for this function has been different for many years: almost all consumer power supplies involve a TL431 placed on the isolated secondary side to feed the error back to the primary side via an optocoupler. Despite its similarities with its op amp cousin, the design of a compensator around a TL431 requires a good understanding of the device operation. The introduction explores the internal structure of the device and details how its biasing conditions affect the loop performance. Then, the classical type 1, 2, and 3 structures associated with an optocoupler are explored in detail.

7.1 A Bandgap-Based Component

The TL431 equivalent architecture appears in Figure 7.1. It combines an open-collector op amp with a precise 2.5-V reference voltage. When the voltage present on the reference pin R exceeds the internal reference level, the bipolar transistor starts to conduct and a current is sunk between the cathode and anode pins. The TL431 is a self-contained op amp plus reference voltage device. As any active element, it needs a minimum voltage to operate as well as a certain amount of consumed current. For the TL431, this latter is called the bias current and must be set to at least 1 mA, as explained later. The same remark applies for the supply voltage, which cannot be lower than 2.5 V across the cathode and the anode of the component.

Figure 7.2 shows the internal schematic of a TL431 made in a bipolar technology. This circuitry was analyzed with the kind help of Mr. Kadanka, an integrated circuit designer at ON Semiconductor in the Czech Republic. The bias points are coming from a simple simulation setup where the device was used as a reference voltage [1]. This configuration implies a connection between its reference point *ref* and the cathode *k*, while the anode *a* is grounded, making the device behave as an active 2.5-V Zener diode.

In classical loop-control configuration, the TL431 observes a fraction of the output voltage seen by its *ref* pin and converts it into an output current sunk between the cathode and the anode. As such, the device can be considered as a transconductance amplifier. The TL431 internal reference circuit works around a popular structure called a *bandgap*. The description of a bandgap is outside the scope of this book but basically the principle consists of balancing the negative temperature coefficient of a junction (a transistor V_{BE}) by a thermal voltage, V_T , affected by a positive temperature coefficient. When summed together, these voltages nicely compensate to form a temperature-compensated reference voltage.

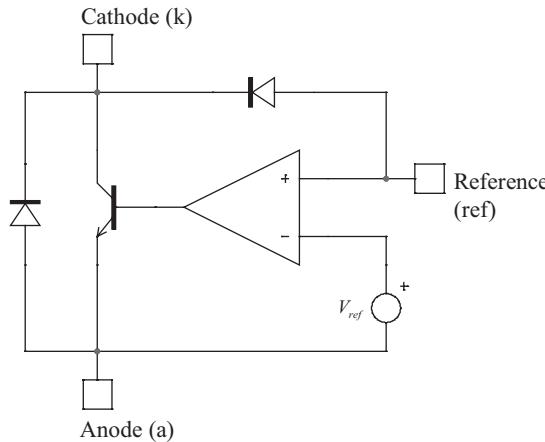


Figure 7.1 The equivalent circuit of a TL431 combines an op amp with a bipolar transistor.

To simplify the analysis, we will assume that the current gain β of all transistors used in the TL431 is very high, implying negligible base currents. The secret of operating the TL431 lies in the subtle equilibrium imposed by Q_9 and Q_1 : when conditions are met (e.g., V_{out} reached its target and V_{ref} equals 2.5 V), both Q_9 and Q_1 share the same current I_1 : V_{ka} remains constant. Any modification in this condition (for instance, brought by a setpoint variation or an increased output power demand

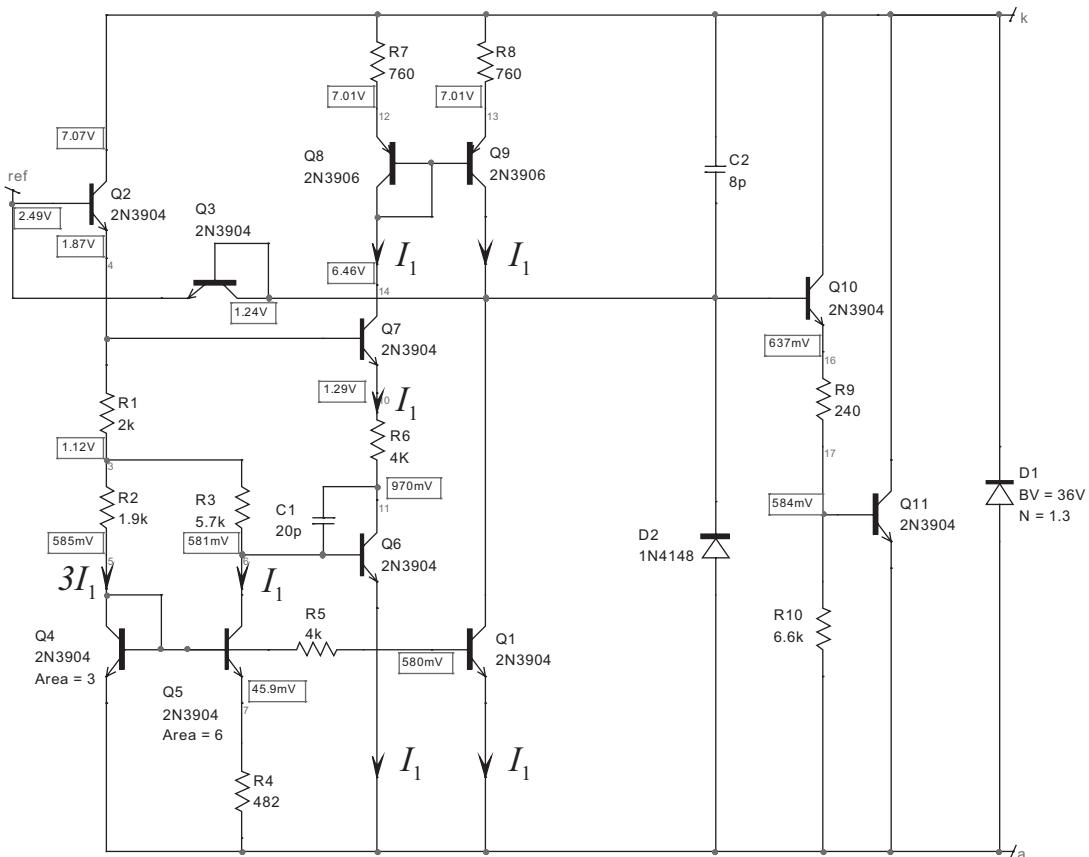


Figure 7.2 The internal schematic of a typical TL431 from ON Semiconductor where bias points in voltage and current have been captured at the equilibrium.

on the regulated converter) will either force either Q_9 to source more current or Q_1 to increase the current it sinks, changing the bias of the output darlington configuration made around Q_{10} and Q_{11} . This action brings V_{ka} down or up, respectively, and forces a current variation in the LED diode attached to the TL431 cathode (e.g., in an opto-isolated power supply application).

At the equilibrium, if we neglect the base currents, the current mirror brought by Q_8 and Q_9 duplicates I_1 , which also circulates in Q_7 and Q_6 . Because of the current mirror arrangement between Q_1 and Q_4 , the same current but scaled up by a ratio of 1 to 3 flows in Q_4 as well. This is confirmed by identical voltage drops across R_2 and R_3 (≈ 530 mV), also featuring a 1 to 3 ratio (1.9 k Ω and 5.7 k Ω):

$$I_{C,Q_5} = \frac{I_{C,Q_4}}{3} = I_{C,Q_1} = I_1 \quad (7.1)$$

Q_7 is wired in a cascode configuration and helps to shield Q_6 voltage bias against the variations on the k terminal that would otherwise be duplicated minus a V_{BE} on Q_6 collector.

In Figure 7.1, the bandgap is made by associating transistors Q_4 and Q_5 together with the emitter resistor R_4 . The *area* parameter on both devices indicates that Q_4 is “equivalent” to three transistors in parallel, whereas Q_5 is made of six paralleled transistors. Otherwise stated, the emitter size of the transistor Q_5 is twice that of transistor Q_4 given respective *area* parameters of 6 and 3. Therefore, not only the current densities J in their emitters are linked ($J_4 = 6J_5$), but their saturation currents I_S are also affected by this relationship:

$$I_{S,Q_5} = 2I_{S,Q_4} \quad (7.2)$$

7.1.1 The Reference Voltage

Now, it is interesting to calculate how the 2.5-V reference is actually established in the TL431. To do so, we need to start with current values flowing through Q_4 and Q_5 . Capitalizing on the equilibrium, we know that I_1 circulates in Q_1 and $3I_1$ in Q_4 (7.1), but due to the ratio of resistors R_2 and R_3 , I_1 also naturally flows in Q_5 . We can write the following equation for voltage difference between base terminals of Q_4, Q_5 and the anode terminal:

$$V_{BE4} = V_{BE5} + I_1 R_4 \quad (7.3)$$

The base-emitter voltage of a bipolar transistor can be calculated from its collector current I_C according to

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \quad (7.4)$$

where $V_T = \frac{kT}{q} \approx 25$ mV at a 27°C room temperature or 300 Kelvin. In this equation, I_S is the transistor saturation current (directly proportional to its emitter size), k is the Boltzmann constant (1.38×10^{-23}), and q is the electron charge equal to 1.601×10^{-19} C.

We know from (7.2) that the saturation current of Q_5 is twice the saturation current of Q_4 . We can therefore update and substitute (7.4) in (7.3):

$$V_T \ln\left(\frac{3I_1}{I_S}\right) = V_T \ln\left(\frac{I_1}{2I_S}\right) + R_4 I_1 \quad (7.5)$$

Rearranging and factoring V_T gives

$$V_T \left[\ln\left(\frac{3I_1}{I_S}\right) - \ln\left(\frac{I_1}{2I_S}\right) \right] = R_4 I_1 \quad (7.6)$$

We know that $\ln a - \ln b = \ln\left(\frac{a}{b}\right)$; therefore,

$$V_T \ln\left(\frac{3I_1}{I_S} \cdot \frac{2I_S}{I_1}\right) = V_T \ln 6 = R_4 I_1 \quad (7.7)$$

From which we can extract the value of the current I_1 :

$$I_1 = \frac{V_T \ln 6}{R_4} \quad (7.8)$$

Based on the value of R_4 , which is 482Ω , we can calculate the value of I_1 :

$$I_1 = \frac{26m \times 1.79}{482} \approx 97 \mu A \quad (7.9)$$

Knowing this current, the drop over the collector loads R_2 and R_3 can quickly be derived by ohm's law:

$$V_{R_2} = V_{R_3} = 3R_2 I_1 = R_3 I_1 = 1.9k \times 97\mu A = 5.7k \times 97\mu A = 553 \text{ mV} \quad (7.10)$$

which is not far away from the bias point calculated by SPICE and reflected in Figure 7.2. As R_1 is crossed by the sum of the currents flowing into Q_4 ($3I_1$) and Q_5 (I_1), its voltage drop is simply

$$V_{R_1} = 4R_1 I_1 = 2k \times 4 \times 97\mu A = 776 \text{ mV} \quad (7.11)$$

Finally, if we stack up all the voltages we have calculated and assume transistors V_{BE} of 580 mV, we obtain the reference level we look for:

$$V_{ref} = V_{R_1} + V_{R_2} + V_{BE2} + V_{BE4} = 0.553 + 0.776 + 0.58 + 0.58 = 2.49 \text{ V} \quad (7.12)$$

This is the value displayed in Figure 7.1 over the *ref* node.

The frequency compensation of the TL431 is performed by the capacitors C_1 , C_2 , and the resistor R_6 . For those interested, [2] details design information for bandgap-based circuits.

7.1.2 The Need for Bias Current

We explained that the condition for equilibrium is reached when V_{ref} equals 2.49 V. Now, if the voltage applied on the *ref* node changes (for instance, increases), the voltage change is propagated on the emitter of Q_2 and forces a current variation in R_1 . This change will now be seen on Q_4 and Q_5 currents, conveying the information to Q_1 and Q_6 , respectively. To that respect, you could see Q_1 and Q_6 working as a differential amplifier. However, as more current flows in Q_4 , its path will naturally offer a larger gain to activate Q_1 , sinking more current to ground than Q_6 does: V_{ka} is pulled down.

We could analytically calculate the transconductance gain of the TL431 but it is easier to deduce it from the characterization curve shown in Figure 7.3. From this curve, we can read a dc gain of 55 dB. This value, together with the 230- Ω pull-up resistor used for characterization implies a transconductance value of

$$g_m = \frac{10^{\frac{55}{20}}}{230} = 2.44 \text{ A/V} \quad (7.13)$$

As the caption details, the cathode current was set to 10 mA during the measurement. A traditional Zener diode needs some substantial bias current to make it operate far away from its knee. Otherwise, the dynamic impedance exhibited by the diode is affected, and the Zener voltage depends on the injected current. Despite being a kind of active Zener diode, the TL431 makes no exception to that particular rule: you need to inject current in its cathode to get the best from the device. We have run simulations on the transistor-level TL431 model to check where the knee sharpens. This is what appears in Figure 7.4.

In this drawing, we can identify a region below which the transconductance of the device is low, with values in the vicinity of 30 mA/V or 30 mS. As the cathode current increases, the transconductance improves and reaches up to 1 A/V. As more current is injected, values up to what is given by (7.13) are obtained.

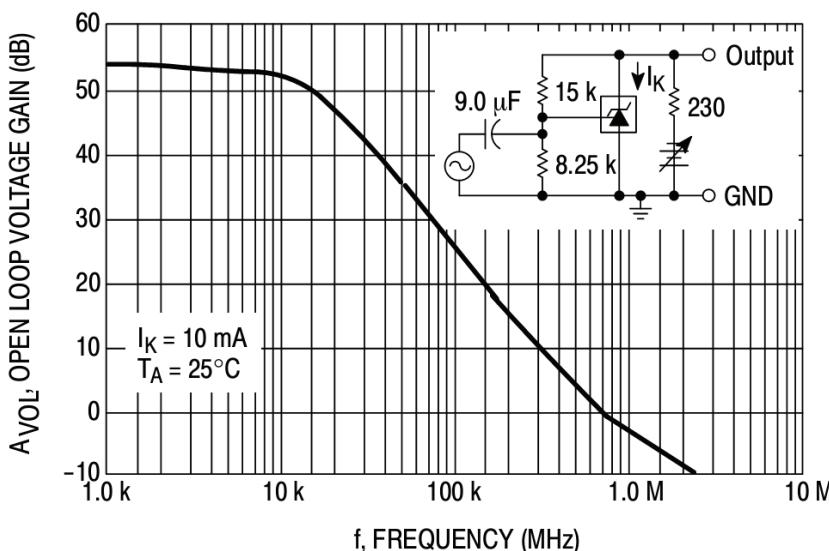


Figure 7.3 The ac test is carried upon a TL431 loaded by a 230- Ω resistor. The injected current is around 10 mA.

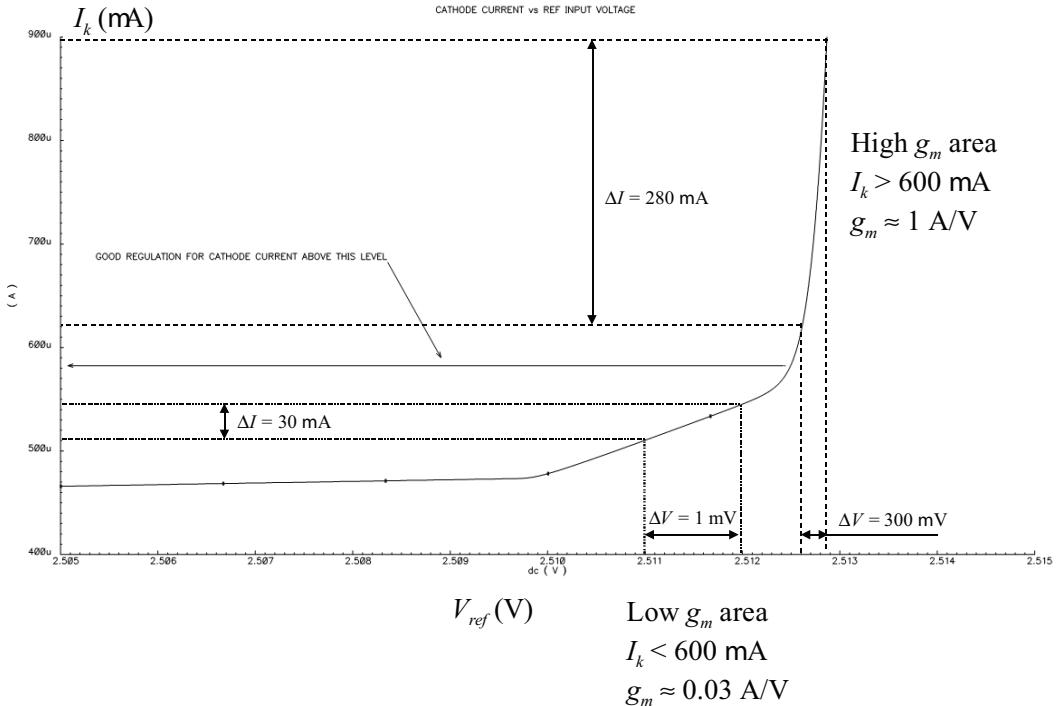


Figure 7.4 From this figure, we can clearly see the appearance of the knee below a $600\text{-}\mu\text{A}$ injected current. Below this value, the transconductance parameter g_m is rather poor.

One way to inject more current is described in Figure 7.5, where a simple resistor connected in parallel with the optocoupler LED increases the current injected in the TL431. As the LED forward drop is around 1 V, a paralleled $1\text{-k}\Omega$ resistor forms a simple 1-mA generator, which sums up with the feedback current flowing through the LED. Please note that decreasing the LED series resistor R_{LED} does not change the TL431 current, as this current is imposed by the primary-side feedback current I_C , reflected in the LED by the optocoupler current transfer ratio (CTR). Changing R_{LED} value affects the mid-band gain but not the TL431 bias as the system operates in a closed-loop form. We will see that effect later.

Finally, what current shall we inject in the TL431? The specifications state a 1-mA minimum current, and one study claims a minimum of 5 mA to obtain decent performance [3]. What value must thus be selected? Well, besides the open-loop gain that is affected by the bias current, the consumption on the output voltage also plays a role in the selection. When you chase every tens of mW to stay below a 100-mW input power for an ac-dc adapter, you understand that you cannot afford to lose precious power in a bias current that is useless in no-load conditions. High-volume notebook adapters deal with a 1-mA extra bias current on top of the natural feedback current seen in the LED. The total bias in the TL431 is thus in the vicinity of 1.5 mA, and experience shows that it is often good enough to reach adequate performance without sacrificing the standby power.

To demonstrate this fact, we have built a simple test fixture where a compensator was assembled and a bias resistor wired as suggested by Figure 7.5. The

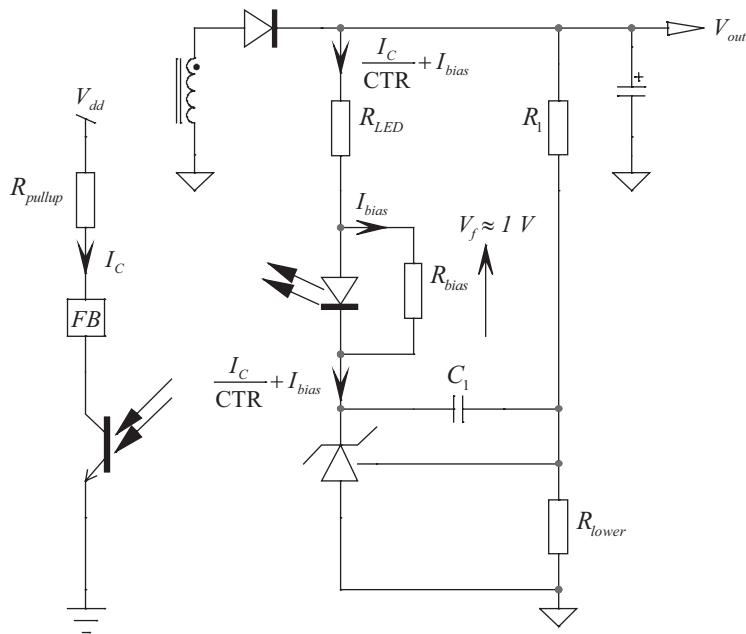


Figure 7.5 A simple resistor in parallel with the optocoupler LED creates a free current source generator.

collector current reflected through its CTR in the LED established to around $300 \mu\text{A}$. We captured a plot without added bias current, letting these $300 \mu\text{A}$ only flow in the TL431. Then, a $1\text{-k}\Omega$ resistor was put across the optocoupler LED to increase the bias current in the TL431 to roughly 1.3 mA . As one can immediately see in Figure 7.6, the open loop gain nicely benefited from this added bias current.

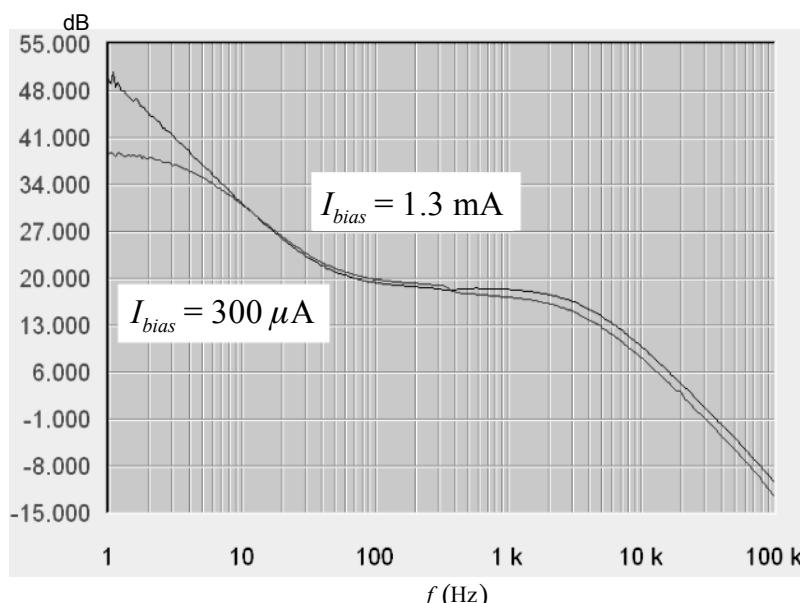


Figure 7.6 The dc gain of the TL431 clearly benefits from an added bias current.

7.2 Biasing the TL431: The Impact on the Gain

This is something we discussed in Chapter 5, but it makes sense to come back to it in this chapter because the TL431 needs an extra bias current to operate. As illustrated in Figure 7.5, the 1-mA bias is ensured by paralleling a resistor with the optocoupler LED. The compensator works by ac modulating the current circulating in the LED and transmitting it to the collector side via the optocoupler CTR. However, as the bias resistor is paralleled with the LED, it naturally steals away current, which returns to the TL431 but does not participate to the ac transfer since it is diverted from the LED. A simplified schematic appears in Figure 7.7. The V_f source illustrates the voltage drop of the LED but it does not play a role in ac as it is constant. This schematic involves the bias resistor and the LED dynamic resistor, R_d . From this representation, we can derive a few equations to show the impact of the bias current resistor.

The error voltage V_{err} is created from the circulation of the collector current in the pull-up resistor R_{pullup} :

$$V_{err}(s) = -I_c(s)R_{pullup} \quad (7.14)$$

The collector current is linked to that of the LED via the optocoupler current transfer ratio (CTR):

$$I_c(s) = I_{LED}(s)\text{CTR} \quad (7.15)$$

By substituting (7.15) in (7.14), we have

$$V_{err}(s) = -I_{LED}(s)R_{pullup}\text{CTR} \quad (7.16)$$

The LED current is actually the main current I_1 , from which the bias current I_{bias} is removed. As we identify a resistive current divider, we have

$$I_{LED}(s) = I_1(s) \frac{R_{bias}}{R_{bias} + R_d} \quad (7.17)$$

The ac current I_1 (therefore ignoring the 1-V LED forward drop) is equal to

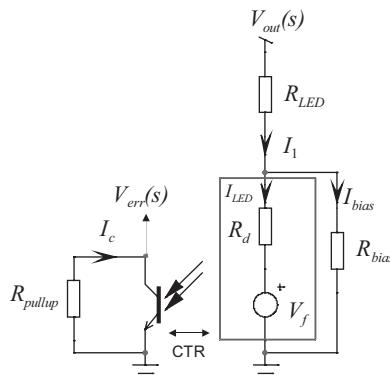


Figure 7.7 The bias resistor steals away current from the LED ac modulation.

$$I_1(s) = \frac{V_{out}(s)}{R_{LED} + R_{bias} \parallel R_d} \quad (7.18)$$

Using (7.17) and (7.18), we have

$$I_{LED}(s) = \frac{V_{out}(s)}{R_{LED} + R_{bias} \parallel R_d} \frac{R_{bias}}{R_{bias} + R_d} \quad (7.19)$$

Finally, by updating (7.16) and rearranging the result, we obtain the transfer function including all resistive paths:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup}CTR}{R_{LED} + R_{bias} \parallel R_d} \frac{R_{bias}}{R_{bias} + R_d} \quad (7.20)$$

In most of the cases, the LED dynamic resistor R_d is considered very small and (7.20) simplifies to

$$\frac{V_{err}(s)}{V_{out}(s)} \approx -\frac{R_{pullup}CTR}{R_{LED}} \quad (7.21)$$

The question now relates to the value of R_d . The dynamic resistor of a diode is linked to its operating current I_F . When operated far from the knee, the dynamic resistor is usually small. However, as the operating point shifts toward the knee, at low bias currents, R_d increases significantly. This is what happens when the pull-up resistor on the primary side is of high values in order to maintain a low-level of standby power. A small current in the LED is enough to vary the feedback level V_{err} and the dynamic resistor suffers.

To know what values we are talking about, we have performed the LED characterization of a popular optocoupler, the SFH615A-2. The results, collected at different temperatures, appear in Figure 7.8. With a $300\text{-}\mu\text{A}$ bias current, the dynamic resistor, $\Delta V_f / \Delta I_f$, is found to be 158Ω . If the bias current increases to 1 mA , the resistor drops to 38Ω . To check the impact of these values on the gain chain derived in (7.20), let's assume the following configuration:

$R_{pullup} = 20 \text{ k}\Omega$; the pull-up resistor loading the optocoupler collector.

$R_d = 158 \Omega$; the LED dynamic resistor.

$CTR = 0.3$; the optocoupler CTR.

$R_{LED} = 1 \text{ k}\Omega$; the LED series resistor.

$R_{bias} = 1 \text{ k}\Omega$; the bias resistor placed in parallel with the LED.

The approximate gain expression where both the dynamic resistor and the bias action are neglected is

$$|G(s)| = \frac{20k \times 0.3}{1k} = 6 \text{ or } 15.6 \text{ dB} \quad (7.22)$$

Using the full expression, this gain value becomes

$$|G(s)| = \frac{20k \times 0.3}{1k + \frac{1k \times 158}{1k + 158}} \times \frac{1k}{1k + 158} = 5.28 \times 0.86 = 4.55 \text{ or } 13.2 \text{ dB} \quad (7.23)$$

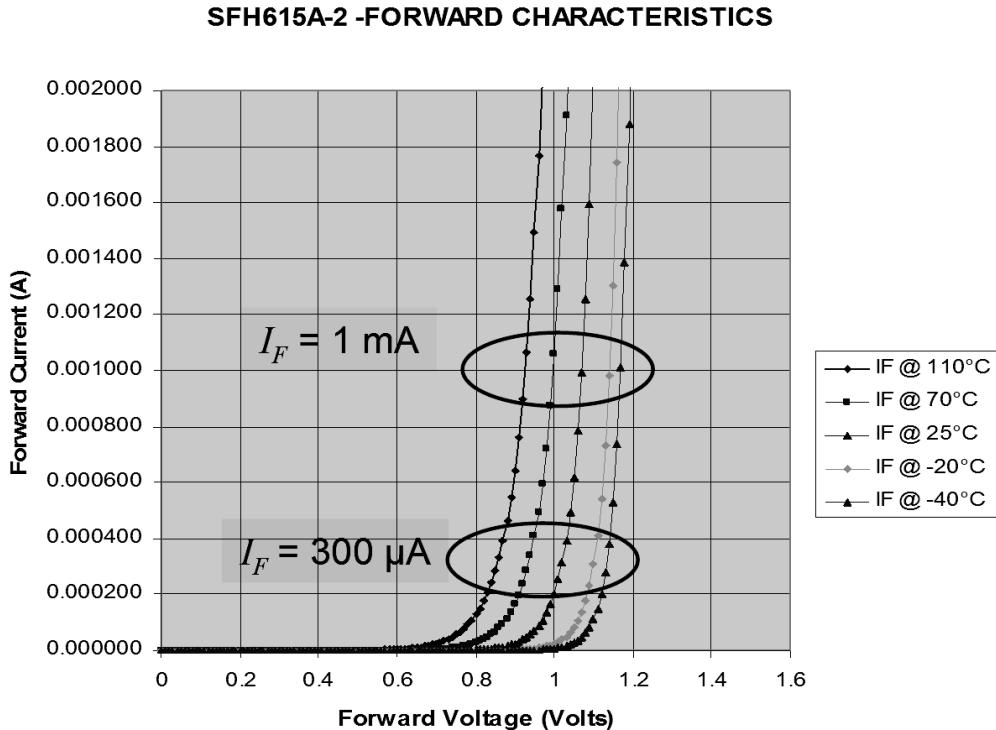


Figure 7.8 The dynamic resistor of the LED shows significant variations depending on where the operating point is.

Comparing both expressions, we can see a 2.4-dB difference. It's not a big number, but it can explain why the crossover frequency point is sometimes missed by a few decibels. To avoid this problem and extend the optocoupler bandwidth, you should force a sufficient static current in the LED by selecting low pull-up resistors on the primary side. In some cases, where the no-load standby power counts, you cannot use low R_{pullup} values, and the gain chain will be affected. When measuring the final open-loop response, it can explain the slight discrepancy you see between the computed crossover point and the final result.

7.3 Biasing the TL431: A Different Arrangement

If the parallel resistor eases the extra bias current generation for the TL431, we have just seen that it has an impact on the loop since it deviates current from the LED path. The nice thing, however, is that no calculations are required, and a simple 1-k Ω resistor placed across the LED terminals does the job perfectly. For those of you who do not like this technique because of its impact on the loop, another means exists via the direct connection of the bias resistor from the TL431 to V_{out} . This option, shown in Figure 7.9, does not affect the LED current.

The LED current depends on the current circulating in the optocoupler collector. This current is maximum when the collector is close to ground and is minimum when the collector is close to the V_{cc} point. The maximum feedback level, $V_{FB,max}$, occurs when the output power demand is high. In a peak-current mode controller,

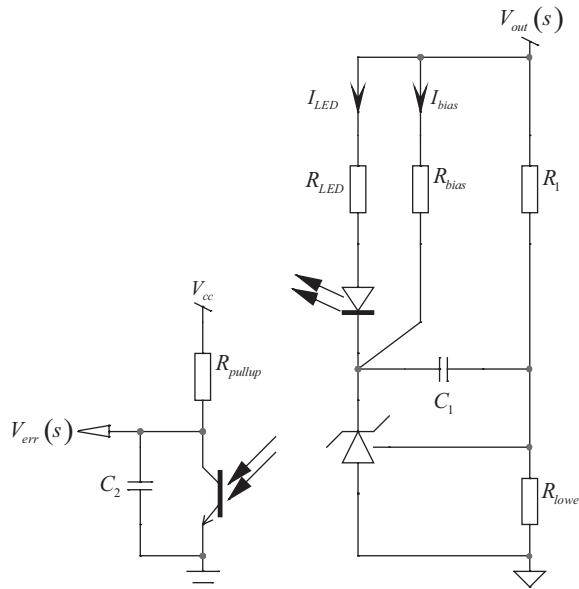


Figure 7.9 The extra resistor connected to the output voltage does not steal away current from the loop path.

the feedback voltage drives the peak current setpoint imposed to the storage inductor. This setpoint varies in relationship to the output power demand and the input voltage conditions. For safety reasons, the maximum current setpoint is internally limited to a certain value, in case the control loop would run away. In offline ac-dc controllers, this maximum setpoint is usually 1 V, safely limiting the current excursion in the sense resistor, and the inductor, to $1/R_{sense}$. To improve the voltage dynamics across the optocoupler collector and the immunity to noise, a divide-by-3 circuit is installed between the feedback pin and the peak current setpoint. Therefore, the feedback voltage will vary between 3 V (maximum power demand) and few hundred of millivolts at low power. Sometimes, one or two diodes are inserted in series with the feedback pin to offer a real 0 V setpoint when the optocoupler collector reaches its saturation level (≈ 300 mV). Such a configuration appears in Figure 7.10.

The collector current, and thus the error voltage, is controlled by the current circulating in the optocoupler LED. This current also flows in the TL431 and contributes to its bias point. This is I_{LED} in Figure 7.9. The minimum bias current occurs when the optocoupler CTR peaks at its maximum and the power demand is the highest. In that case, the feedback voltage is almost 3 V, assuming a common-emitter circuitry close to that in Figure 7.10 is implemented. Suppose we have the following parameters:

$V_{cc} = 5$ V; the pull-up resistor upper terminal voltage.

$R_{pullup} = 20$ k Ω ; the collector pull-up resistance.

$R_{LED} = 1$ k Ω ; the LED series resistance.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1$ mA; the wanted bias current in the TL431.

CTR = 30 percent to 120 percent; the optocoupler CTR variations.

$V_{FB,max} = 3$ V; the feedback voltage at maximum power.

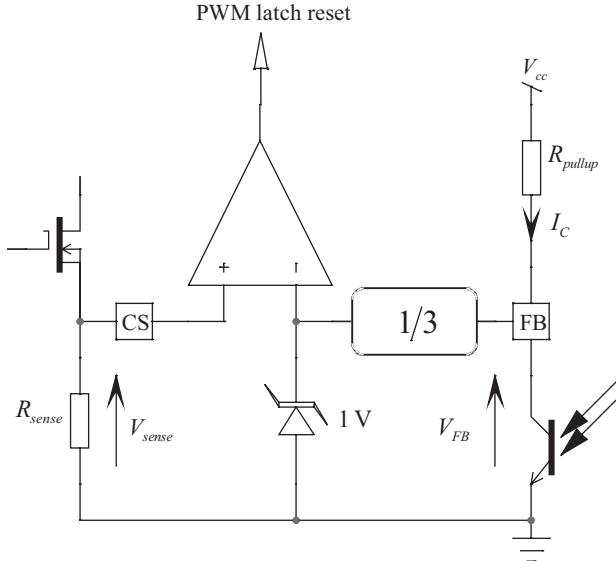


Figure 7.10 The internal circuitry of a peak current mode controller.

The minimum LED current in that case is simply

$$I_{LED,\min} = \frac{V_{cc} - V_{FB,\max}}{R_{pullup} \text{CTR}_{\max}} = \frac{5 - 3}{20k \times 1.2} \approx 83 \mu\text{A} \quad (7.24)$$

As we can see, we are far away from the minimum bias current of 1 mA required in the TL431 data sheet. This is the purpose of the extra resistor R_{bias} shown in Figure 7.9—to provide this extra current. To derive a resistance value for R_{bias} , we first need to know the voltage across it. This voltage is that across the LED series resistance R_{LED} to which the LED forward drop V_f is added. If we divide this voltage by the needed bias current, we have our resistor value:

$$R_{bias} = \frac{R_{LED} I_{LED,\min} + V_f}{I_{bias}} = \frac{\frac{V_{cc} - V_{FB,\max}}{R_{pullup} \text{CTR}_{\max}} R_{LED} + V_f}{I_{bias}} \quad (7.25)$$

If we use the previous parameters, for a 1-mA bias current, the extra resistor value must be

$$R_{bias} = \frac{83 \mu\text{A} \times 1k + V_f}{1\text{mA}} = 1083 \Omega \quad (7.26)$$

This value is not far away from what a parallel resistor would give. However, this configuration has the following advantages:

1. As no ac current is stolen from the LED path, the presence of this resistor does not affect the loop gain, even in presence of large LED dynamic resistors.
2. To cope with the TL431 biasing requirements, the LED series resistor upper limit is bounded. If you add a bias resistor across the LED, to form the 1-mA bias generator, this upper limit is affected and it brings another

burden in the calculation process (see the following). On the contrary, when the bias resistor is directly connected to the output voltage, this drawback disappears.

3. Our experience shows that this configuration slightly reduces the output overshoot at startup. This is because the bias current is immediately present as V_{out} rises up. When using the 1-kΩ resistor in parallel with the LED, the bias current only occurs when the TL431 forces the LED conduction.

7.4 Biasing the TL431: Component Limits

The TL431 requires a minimum current to operate in favorable conditions. On the other side, it also needs a minimum voltage to deliver its performance. This minimum voltage is equal to the internal reference value and cannot be lower than 2.5 V. Figure 7.5 portrays a typical TL431 arrangement where the optocoupler collector pulls the feedback pin down as the LED current increases. The series resistor R_{LED} is there to limit the maximum LED current but also to fix the compensator mid-band gain as we will see in a few lines. Unfortunately, because of the biasing conditions imposed by the TL431 (minimum operating voltage of 2.5 V and the necessity to inject 1 mA at least), there is an upper limit on this resistor value. Let us derive this limit with a few equations. First, what is the maximum collector current on the optocoupler output necessary to bring the feedback voltage close to ground, actually the optocoupler saturation voltage $V_{CE,sat}$?

$$I_{C,max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}} \quad (7.27)$$

To circulate in the pull-up resistor, this current needs the photons emitted by the internal LED and collected by the transistor base area. The collector current I_C is linked to the LED current I_F by the current transfer ratio (CTR). In our case, to cover unavoidable dispersions, we need to use the minimum value of this CTR parameter. Looking at Figure 7.5 in more detail, we can see that the total current flowing through R_{LED} also includes the additional bias current brought by R_{bias} , provided we have adopted the bias generator featuring the 1-kΩ resistor across the LED. Therefore, (7.27) can be used to derive another equation:

$$I_{R_{LED},max} = \frac{I_{C,max}}{\text{CTR}_{\min}} + I_{bias} = \frac{V_{cc} - V_{CE,sat} + I_{bias}R_{pullup}\text{CTR}_{\min}}{R_{pullup}\text{CTR}_{\min}} \quad (7.28)$$

The LED current depends not only on the output voltage, but also on the forward drop of the diode itself and the minimum operating voltage acceptable for the TL431:

$$I_{R_{LED},max} = \frac{V_{out} - V_f - V_{TL431,min}}{R_{LED}} \quad (7.29)$$

By equating (7.28) and (7.29) then solving for $R_{LED,max}$, we have the maximum value this resistor cannot exceed:

$$R_{LED,\max} \leq \frac{V_{out} - V_f - V_{TL431,\min}}{V_{cc} - V_{CE,sat} + I_{bias}CTR_{\min}R_{pullup}} R_{pullup} CTR_{\min} \quad (7.30)$$

In the previous equations, we have

V_{out} , the output voltage

I_{bias} , the TL431 biasing current when the optocoupler LED is paralleled with a resistor (usually 1 kΩ for a 1-mA bias)

$V_{TL431,\min}$, the minimum voltage the TL431 can go down to (2.5 V)

V_f , the optocoupler LED forward drop (≈ 1 V)

CTR_{\min} , the minimum optocoupler current transfer ratio

$V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current)

V_{cc} , the bias voltage where the pull-up resistor is connected to on the primary side

From the previous line, we can see that the dc operating conditions fix the upper excursion value of the LED series resistor. As we will later see, R_{LED} not only plays a role in dc, but also in the mid-band gain expression, hampering the TL431 application range. The fast lane is guilty . . .

7.5 The Fast Lane Is the Problem

Already discussed in the op amp section, it is interesting to come back on this typical characteristic of the TL431 configuration. In Figure 7.5, neglecting the bias current, the LED current is imposed by the voltage present on the output voltage, the diode forward drop, and the level on the TL431 cathode:

$$I_{LED} = \frac{V_{out} - V_f - V_{TL431}}{R_{LED}} \quad (7.31)$$

This current is actually made of two terms: a dc and ac current. The dc current fixes the operating point and corresponds to an output voltage equal to the assigned target. The ac current superimposes on the dc value and modulates the voltage on the FB node, $V_{err}(s)$. In this mode, the LED forward drop V_f no longer plays a role (it is constant and its derivative term is therefore null), and (7.31) can be updated as follows:

$$I_{LED}(s) = \frac{V_{out}(s) - V_{TL431}(s)}{R_{LED}} = \frac{V_{out}(s)}{R_{LED}} - \frac{V_{TL431}(s)}{R_{LED}} \quad (7.32)$$

In Figure 7.5, we can see a capacitor C_1 across the TL431 feedback path. At high frequencies, this capacitor becomes a short circuit and the ac voltage across the TL431 imputed to the output voltage variations sensed by R_1/R_{lower} goes to 0. However, as indicated by (7.31), the dc point is maintained and the converter keeps delivering the right output voltage V_{out} . In a classical configuration, because the feedback capacitor is a short circuit, we would suppose that the ac output of the whole system, $V_{err}(s)$, would also go down to zero.

Unfortunately, the LED ac current is made of two voltage terms, as indicated by (7.32): the one imposed by the TL431 (which is null at high frequencies because of C_1) but also that directly imposed by the output voltage. Mathematically, this fact can be expressed through the following equation:

$$\lim_{s \rightarrow \infty} I_{LED}(s) = \frac{V_{out}(s)}{R_{LED}} \quad (7.33)$$

As a result, despite a TL431 ac output being null, there is still a path from the output to the control via the optocoupler LED: this is the *fast lane* effect. Figure 7.11 shows a simplified representation of the system where the TL431 is replaced by a simple Zener diode, testifying for the disappearance of the ac link with V_{out} through the divider network. If V_{out} is modulated, then the LED current is also modulated and the perturbation propagates to the output, $V_{err}(s)$. In the light of (7.33), we can see that R_{LED} not only fixes the dc bias, but also interacts in the gain definition. This fact leads to situations where the selection of the LED series resistor based on gain/attenuation needs is not compatible with what (7.30) dictates. At this point, another solution will have to be found: the fast lane must be disabled.

7.6 Disabling the Fast Lane

If the fast lane represents the problem, we must find a way to get rid of it. How? By cutting the ac link between the observed variable (V_{out}) and the LED series resistor. This can be done by identifying in the board another dc source (e.g., 12 V), fully ac isolated from the observed variable. The output of a linear regulator will do perfectly, for instance, perhaps from another winding if necessary. Another solution consists of biasing a separated Zener-based network supplied by the output voltage we observe. If the Zener is properly biased and its voltage around two-thirds of V_{out} (to build enough ac isolation), then experience shows that it is a valid solution. This solution appears in Figure 7.12.

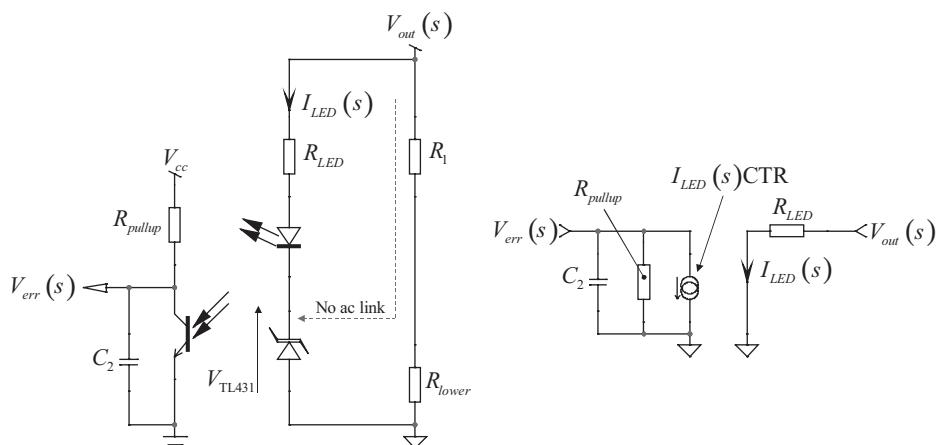


Figure 7.11 The fast lane is created because the LED current not only depends on the internal op amp ac output but also on the observed output voltage. The right side of the picture represents the equivalent ac small-signal model at high frequencies when the internal op amp ac output is zero.

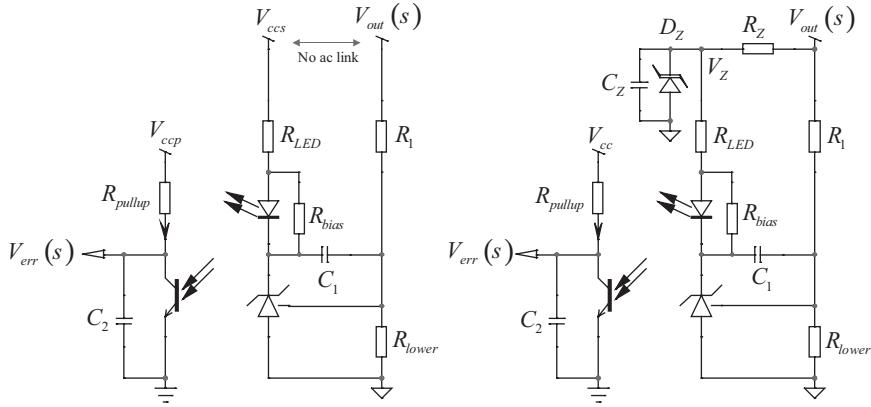


Figure 7.12 A solution is to hook the series resistor R_{LED} to a separate dc point, V_{ccs} , or build ac isolation from V_{out} via a Zener-based network.

The LED maximum value does not change from that derived in (7.30) except that V_{out} is replaced by the Zener voltage or V_{ccs} if you adopt Figure 7.12 left-side option:

$$R_{LED,max} \leq \frac{V_Z - V_f - V_{TL431,min}}{V_{ccp} - V_{CE,sat} + I_{bias}CTR_{min}R_{pullup}} R_{pullup}CTR_{min} \quad (7.34)$$

The bias resistor R_Z requires a design equation, since its role is to bias the Zener diode, but also to provide the TL431 operating current (feedback and bias currents). The Zener diode bias current I_{Zbias} has been selected so that the diode operates far enough from its knee where it will exhibit the lowest dynamic impedance and, thus, the best ac isolation from V_{out} . The LED maximum current is actually reached when the feedback voltage V_{FB} is pulled down to $V_{CE,sat}$. In this case, the LED current is simply

$$I_{LED,max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}CTR_{min}} \quad (7.35)$$

To this operating feedback current, we must add the 1-mA (or more) extra current I_{bias} brought by R_{bias} placed across the optocoupler LED. The Zener dropping resistor R_Z is therefore immediately derived through

$$R_Z = \frac{V_{out} - V_Z}{I_{LED,max} + I_{bias} + I_{Zbias}} \quad (7.36)$$

Substituting (7.35) in (7.36), we obtain

$$R_Z = \frac{(V_{out} - V_Z)R_{pullup}CTR_{min}}{(V_{cc} - V_{CE,sat}) + (I_{Zbias} + I_{bias})R_{pullup}CTR_{min}} \quad (7.37)$$

In the previous equation, we have the following variables:

V_{out} , the output voltage

I_{bias} , the TL431 biasing current when the optocoupler LED is paralleled with a resistor (usually 1 kΩ for a 1-mA bias)

- I_{Zbias} , the Zener diode biasing current
- CTR_{\min} , the minimum optocoupler current transfer ratio
- $V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current)
- V_{cc} , the bias where the pull-up resistor is connected to on the primary side

A 100-nF capacitor will be paralleled with the Zener diode to improve the filtering capabilities of the network. We are now all set to detail the design methods for the types 1, 2, and 3 using a TL431 regulator.

7.7 The Type 1: An Origin Pole, Common-Emitter Configuration

The type 1 is used to compensate power converters where no phase boost is necessary. The phase lag of a type 1 amplifier, whatever its construction (op amp, OTA, or TL431) is permanently flat to 270° . A type 1 can be built with a TL431 following the Figure 7.13 schematic:

In this circuit, the LED resistor is selected following (7.30) while the pole and zero are made coincident to cancel one another. This way, we create a simple integrator whose 0-dB crossover pole can be easily adjusted. If we neglect the LED dynamic resistor R_d , we can draw a simplified small-signal diagram from Figure 7.13. It appears in Figure 7.14.

The ac current circulating in the LED depends on V_{out} and the voltage on the internal op amp output terminal:

$$I_{LED}(s) = \frac{V_{out}(s) - V_{TL431}(s)}{R_{LED}} \quad (7.38)$$

The voltage output of the TL431 is a simple integrator and obeys the following transfer function:

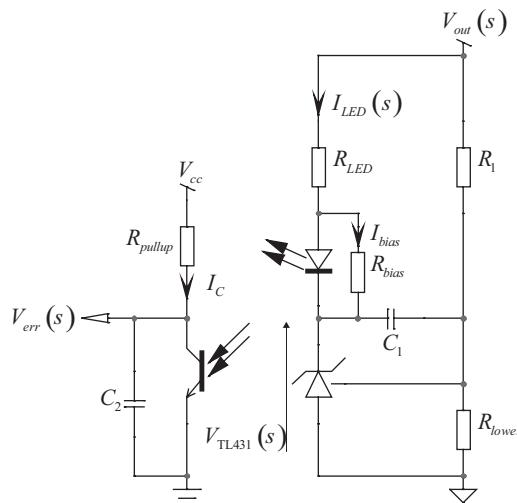


Figure 7.13 A type 1 built with a TL431 uses a type 2 configuration where the pole and zero have been made coincident.

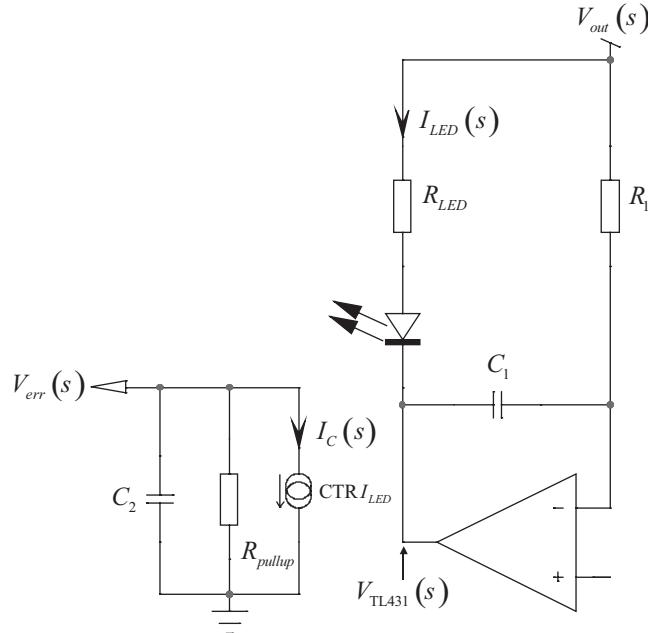


Figure 7.14 The small-signal version of the TL431 network reveals an integrator followed by a pole.

$$V_{TL431}(s) = -V_{out}(s) \frac{\frac{1}{sC_1}}{R_1} = -V_{out}(s) \frac{1}{sR_1C_1} \quad (7.39)$$

Substituting (7.39) into (7.38), we have

$$I_{LED}(s) = \frac{V_{out}(s) + V_{out}(s) \frac{1}{sR_1C_1}}{R_{LED}} = \frac{V_{out}(s)}{R_{LED}} \left(1 + \frac{1}{sR_1C_1} \right) = V_{out}(s) \left(\frac{1 + sR_1C_1}{sR_{LED}R_1C_1} \right) \quad (7.40)$$

The previous expression shows the effect of the fast lane. By inspecting Figure 7.14, we would expect the presence of a simple integrator, given the position of \$C_1\$. However, as confirmed by (7.40), a zero clearly appears in the numerator of the expression. To build a type 1, we will then need to find a way to neutralize this zero by another pole. Let us carry on with the derivation. The output voltage, \$V_{err}(s)\$, is simply the collector current \$I_C(s)\$ circulating in a network made of the pull-up resistor and the capacitor \$C_2\$:

$$V_{err}(s) = -I_C(s) \frac{\frac{1}{sC_1}}{R_{pullup} + \frac{1}{sC_1}} = -I_C(s) R_{pullup} \frac{1}{1 + sR_{pullup}C_1} \quad (7.41)$$

We know that the collector current links to the LED current via the CTR:

$$I_C(s) = I_{LED}(s) \text{CTR} \quad (7.42)$$

By substituting (7.40) into (7.42), updating and rearranging (7.41), we have

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{1}{s \frac{R_{LED}R_1}{R_{pullup}CTR} C_1} \left(\frac{1+sR_1C_1}{1+sR_{pullup}C_2} \right) \quad (7.43)$$

This equation can be put under a more familiar form such as

$$G(s) = -\frac{1}{s/\omega_{po}} \frac{1+s/\omega_z}{1+s/\omega_p} \quad (7.44)$$

where

$$\omega_{po} = \frac{R_{pullup}CTR}{R_{LED}R_1C_1} \quad (7.45)$$

$$\omega_z = \frac{1}{R_1C_1} \quad (7.46)$$

$$\omega_p = \frac{1}{R_{pullup}C_2} \quad (7.47)$$

To form a real type 1, we need to neutralize the zero and the pole to keep the 0-dB crossover pole alone. Therefore, (7.46) and (7.47) must be equal:

$$\frac{1}{R_1C_1} = \frac{1}{R_{pullup}C_2} \quad (7.48)$$

From the previous, we can extract the value of C_2 :

$$C_2 = \frac{R_1C_1}{R_{pullup}} \quad (7.49)$$

From (7.45) we obtain a value for C_1 :

$$C_1 = \frac{R_{pullup}CTR}{2\pi R_{LED}R_1f_{po}} \quad (7.50)$$

Substituting C_1 definition into (7.49), we have an expression for C_2 :

$$C_2 = \frac{CTR}{2\pi f_{po}R_{LED}} \quad (7.51)$$

The 0-dB crossover pole location must now be selected so that the magnitude G at the crossover frequency f_c exactly compensates the gain excess or deficiency read on the power stage Bode plot. The transfer function of an integrator obeys the following formula, in which ω_{po} represents the 0-dB crossover pole:

$$G(s) = \frac{1}{\frac{s}{\omega_{po}}} \quad (7.52)$$

From the previous equation, we can calculate the magnitude of $G(s)$ at the crossover frequency:

$$|G(f_c)| = \frac{f_{po}}{f_c} \quad (7.53)$$

We can now extract the 0-dB crossover pole location and feed (7.50)/(7.51) to get C_1 and C_2 , respectively:

$$f_{po} = G \cdot f_c \quad (7.54)$$

7.7.1 A Design Example

Let us assume we want to compensate a 12-V power stage exhibiting a gain excess G_f of 25 dB at a 20-Hz frequency. This could be the case for a single-stage flyback converter, for instance. To reach this goal, we will define the position at which the 0-dB crossover pole must be located so that the magnitude of $G(s)$ is exactly -25 dB when the frequency reaches 20 Hz. These 25 dB of attenuation translate to

$$G = 10^{\frac{-G_f}{20}} = 10^{\frac{-25}{20}} = 56.2\text{m} \quad (7.55)$$

Applying (7.54), the 0-dB crossover pole must be placed at

$$f_{po} = G \cdot f_c = 0.0562 \times 20 = 1.12 \text{ Hz} \quad (7.56)$$

The single-stage flyback converter uses elements exhibiting the following values:

- $V_{out} = 12 \text{ V}$; the output voltage.
- $V_f = 1 \text{ V}$; the LED forward voltage.
- $I_{bias} = 1 \text{ mA}$; the TL431 biasing current when the optocoupler LED is paralleled with a resistor.
- $V_{TL431,min} = 2.5 \text{ V}$; the minimum operating voltage of the TL431.
- $V_{CE,sat} = 0.3 \text{ V}$; the optocoupler saturation voltage.
- $V_{cc} = 5 \text{ V}$; the pull-up V_{cc} level.
- $R_{pullup} = 10 \text{ k}\Omega$; the optocoupler pull-up resistor.
- $\text{CTR}_{min} = 0.5$; the minimum optocoupler current transfer ratio.
- $R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.
- $f_{opto} = 10 \text{ kHz}$; the optocoupler pole that has been characterized with R_{pullup} .

Based on these values, we can immediately calculate the maximum LED series resistor via (7.30):

$$R_{LED,max} \leq \frac{12 - 1 - 2.5}{5 - 0.3 + 1m \times 0.5 \times 10k} 10k \times 0.5 \leq 4.4 \text{ k}\Omega \quad (7.57)$$

Adopting a 20 percent derating factor, the final series resistor for the LED is 3.5 kΩ.

The capacitors calculations can now be undertaken:

$$C_1 = \frac{R_{pullup} \text{CTR}}{R_{LED} R_1 2\pi f_{po}} = \frac{10k \times 0.5}{3.5k \times 38k \times 1.12 \times 6.28} = 5.3 \mu\text{F} \quad (7.58)$$

$$C_2 = \frac{R_1 C_1}{R_{pullup}} = \frac{5.3\mu \times 38k}{10k} = 20.3 \mu F \quad (7.59)$$

Given the optocoupler pole position value (10 kHz) with regard to the second pole (0.8 Hz), we can neglect its action on the compensator. The simulation schematic appears in Figure 7.15.

The ac response of the compensator appears in Figure 7.16 and confirms the target we set. The attenuation at 20 Hz is exactly 25 dB as expected. There is no phase boost; we knew it from the start.

7.8 The Type 1: Common-Collector Configuration

Wiring the optocoupler in a common-collector configuration does not change the operating bias point, but the transfer function loses its minus sign:

$$\frac{V_{err}(s)}{V_{out}(s)} = \frac{1}{s \frac{R_{LED} R_1}{R_{pulldown} CTR} C_1} \left(\frac{1 + sR_1 C_1}{1 + sR_{pulldown} C_2} \right) \quad (7.60)$$

The calculations carried in the previous example are still valid, with R_{pullup} being replaced by $R_{pulldown}$.

7.9 The Type 2: An Origin Pole plus a Pole/Zero Pair

The type 2 configuration is the most popular configuration of the TL431 used in a compensator application. The application circuit does not change from that proposed in Figure 7.13. Therefore, the transfer function already derived for the type 1 remains valid. However, it is our interest to slightly rearrange it to make the mid-band gain appear:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup} CTR}{s R_{LED} R_1 C_1} \left(\frac{1 + sR_1 C_1}{1 + sR_{pullup} C_2} \right) \quad (7.61)$$

By factoring $sR_1 C_1$ in the numerator, we recognize a classical type 2 transfer function:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup} CTR}{R_{LED}} \left(\frac{1 + 1/sR_1 C_1}{1 + sR_{pullup} C_2} \right) \quad (7.62)$$

This equation can be put under the form

$$G(s) = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (7.63)$$

parameters**Vout=12****Vf=1****VTL431=2.5****VCEsat=300mV****Vdd=5****Ibias=1mA**

$$a = (V_{out} - V_f - V_{TL431}) * R_{pullup} * CTR$$

$$b = (V_{dd} - V_{CEsat} + Ibias * R_{pullup}) * CTR$$

$$R_{max} = a/b$$

$$R1 = (V_{out} - 2.5) / 250\mu$$

$$fc = 20$$

$$Gfc = 25$$

$$G = 10^{\lambda} (-Gfc/20)$$

$$\pi = 3.14159$$

$$Fpo = G * fc$$

$$R_{pullup} = 10k\Omega$$

$$RLED = R_{max} * 0.8$$

$$C1 = C2 * R_{pullup} / R1$$

$$C2 = CTR / (2 * \pi * Fpo * RLED)$$

$$C_{col} = C2 - C_{opto}$$

$$F_{opto} = 10k\Omega$$

$$C_{opto} = 1 / (2 * \pi * F_{opto} * R_{pullup})$$

X2
Optocoupler

Cpole = Copo

CTR = CTR

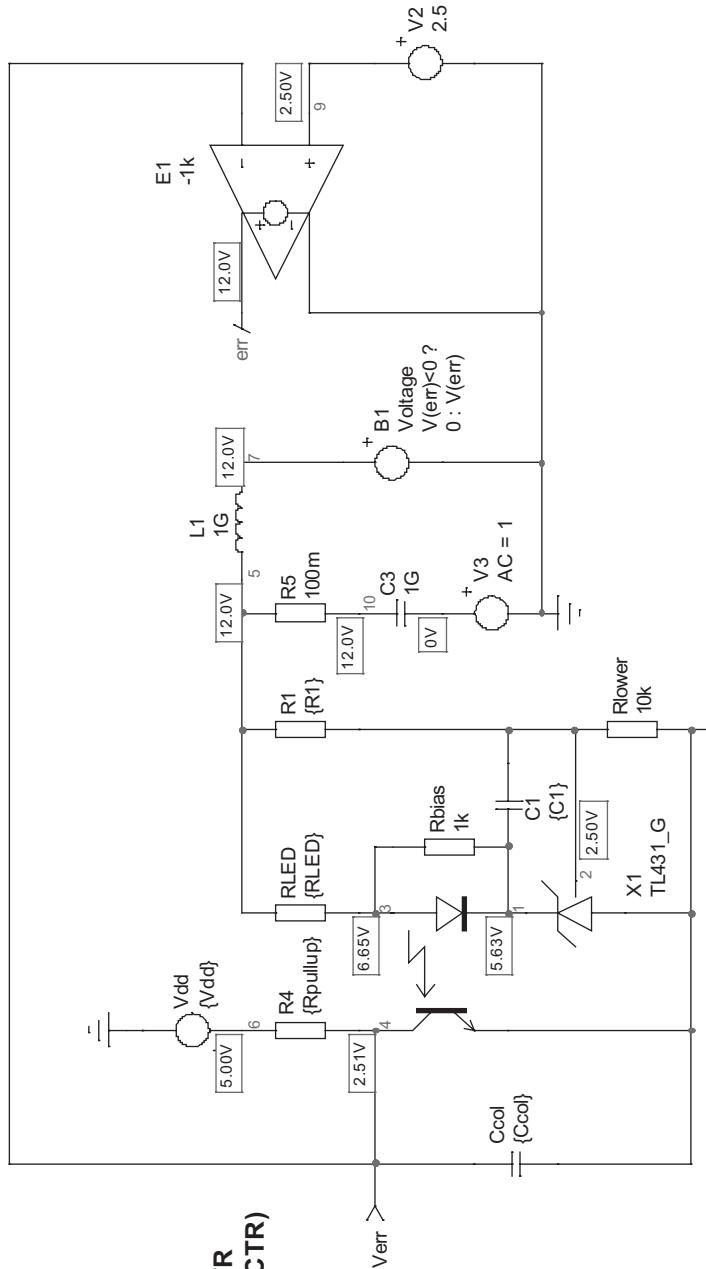


Figure 7.15 The type 1 configuration schematic implementing a TL431 does not cause any calculation difficulties.

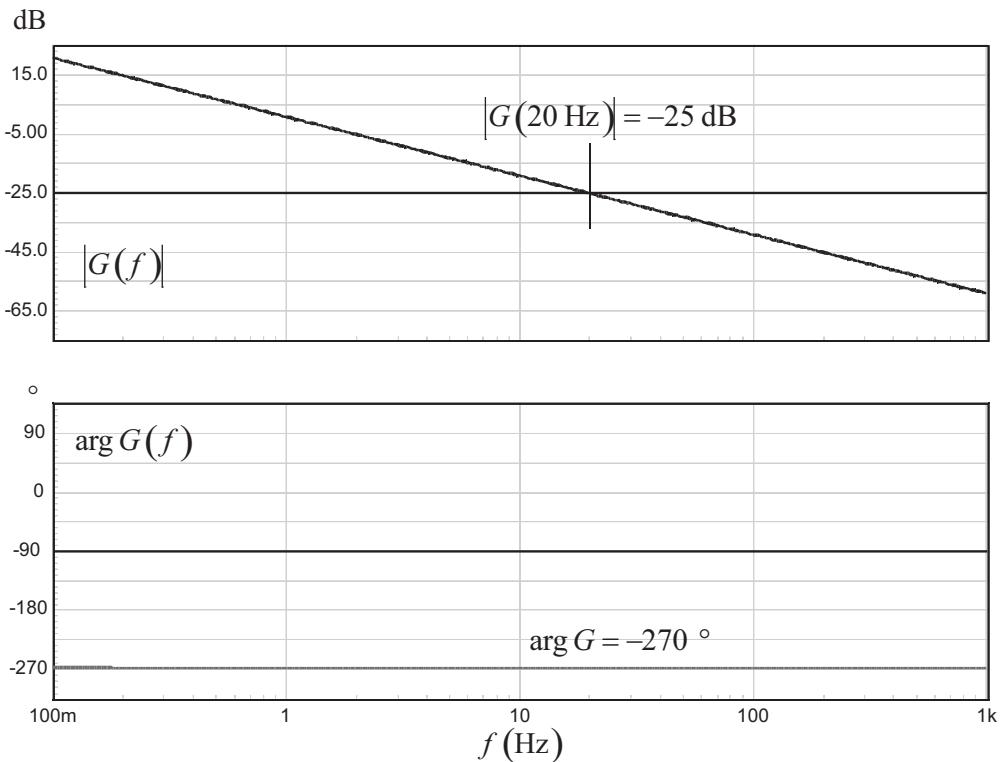


Figure 7.16 The ac response confirms the right attenuation at the selected 20-Hz crossover point.

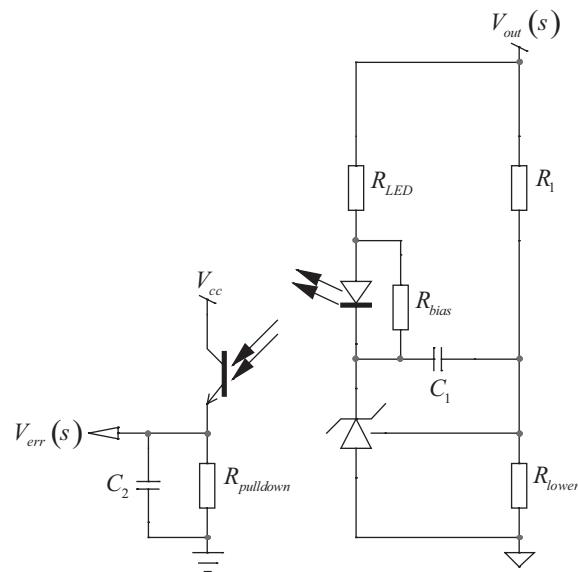


Figure 7.17 The common-collector configuration changes the signal polarity.

where

$$G_0 = \frac{R_{pullup} \text{CTR}}{R_{LED}} \quad (7.64)$$

$$\omega_z = \frac{1}{R_1 C_1} \quad (7.65)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (7.66)$$

The expression for the mid-band gain, (7.64), requires some clarifications, though. We can see that the equation includes the LED resistor whose upper limit is bounded by (7.30). This means that the flexibility of choosing any gain or attenuation value for G_0 is hampered by the upper limit for R_{LED} . Again, this is an effect of the fast lane and there is nothing we can do to counteract this effect. Suppose (7.30) gives an upper limit of 860Ω , together with a pull-up resistor of $20 \text{ k}\Omega$ and a CTR of 30 percent. In this case, the minimum gain imposed by G_0 is

$$G_0 > \text{CTR} \frac{R_{pullup}}{R_{LED,\max}} > 0.3 \frac{20}{0.860} > 7 \text{ or } \approx 17 \text{ dB} \quad (7.67)$$

This means that you can only select a crossover frequency on the $H(s)$ Bode plot where the needed amplification is at least 17 dB. Should the selected point require a 10-dB gain, you could simply not use the TL431 with the selected pull-up and LED resistor values.

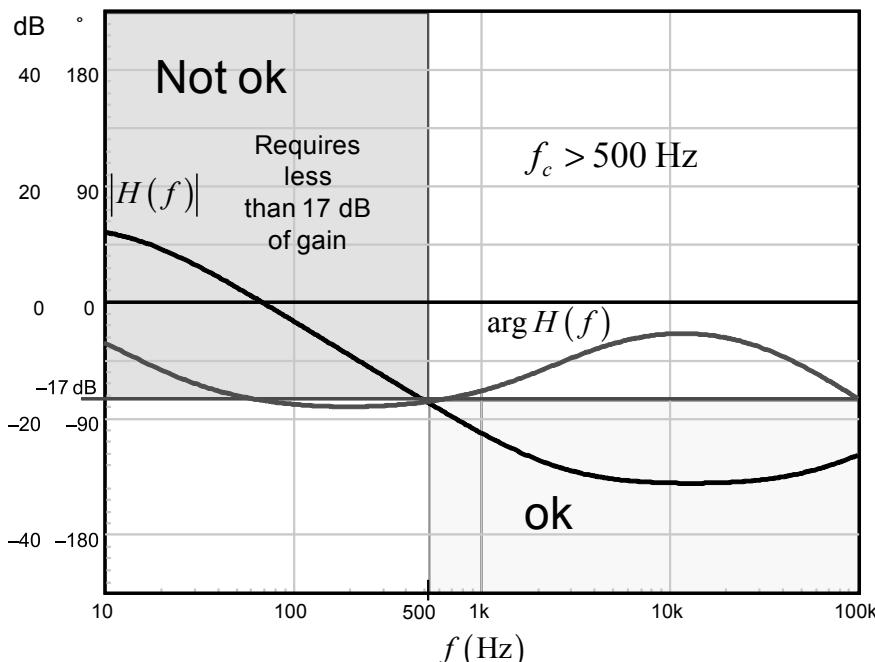


Figure 7.18 The TL431 configuration with the fast lane imposes a certain gain below which you simply cannot use the compensator. In the figure, the gain selection has to be greater than 17 dB.

Figure 7.18 shows the considered Bode plot and the possible working area. In this region, the type 2 built with the TL431 and operated with the resistors ($860\ \Omega$ for R_{LED} and $20\ k\Omega$ for R_{pullup}) would work. However, as you can see, a crossover frequency below 500 Hz could not be accepted simply because you would need a gain below the minimum of 17 dB imposed by (7.67). What if you really need to cross over below 500 Hz? Well, if the phase lag is less than 45° at the considered point, you can use a type 1 and freely select the needed gain/attenuation, regardless of the LED series resistor. Otherwise, you need to get rid of the fast lane, as we will see in a few lines. First, let's study a design example of a type 2 configuration with a TL431.

7.9.1 A Design Example

Let's assume we need to compensate a 19-V output converter whose gain deficiency at 1 kHz is -15 dB. Given the phase margin we shoot for, we will boost the phase by 50° at 1 kHz. Where do we place our pole and zero pair? As we have detailed in the pole-zero section, the pole can be placed at the following location:

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 1k = 2.74\ \text{kHz} \quad (7.68)$$

As the phase peaks at the geometric mean between the pole and the zero, this latter is placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{1k^2}{2.74k} \approx 365\ \text{Hz} \quad (7.69)$$

The converter uses components that exhibit the following characteristics:

$V_{out} = 19$ V; the output voltage.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1$ mA; the TL431 biasing current when the optocoupler LED is parallelled with a resistor.

$V_{TL431} = 2.5$ V; the minimum operating voltage of the TL431.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$R_{pullup} = 20\ k\Omega$; the optocoupler pull-up resistor.

$\text{CTR}_{\min} = 0.3$; the minimum optocoupler current transfer ratio.

$R_1 = 66\ k\Omega$; the upper element in the resistor bridge observing the output variable.

$f_{opto} = 6$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

From these values, we can first check the maximum allowable LED series resistor:

$$R_{LED,\max} \leq \frac{19 - 1 - 2.5}{5 - 0.3 + 1m \times 0.3 \times 20k} 20k \times 0.3 \leq 8.7\ k\Omega \quad (7.70)$$

Then, let's translate the 15-dB gain into a decimal value and check if the corresponding LED resistor value complies with (7.70):

$$G = 10^{\frac{-Gf_c}{20}} = 10^{\frac{15}{20}} = 5.6 \quad (7.71)$$

From (7.64), we can extract the LED resistor:

$$R_{LED} = \frac{R_{pullup} \text{CTR}}{G} = \frac{20k \times 0.3}{5.6} = 1071 \Omega \quad (7.72)$$

This resistor is well below the limit imposed by (7.70); we are safe. The first capacitor C_1 is found using (7.65) together with the 365-Hz zero we want to position:

$$C_1 = \frac{1}{2\pi f_z R_1} = \frac{1}{6.28 \times 365 \times 66k} = 6.6 \text{ nF} \quad (7.73)$$

We know that the pole capacitor C_2 is actually made of an extra capacitor C_{col} that we will place in parallel with the collector-emitter parasitic capacitor from the optocoupler:

$$C_2 = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 20k \times 2.74k} = 2.9 \text{ nF} \quad (7.74)$$

Given the characterized optocoupler pole at 6 kHz, its parasitic capacitor is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} = 1.3 \text{ nF} \quad (7.75)$$

As the total capacitance is 2.9 nF, the added capacitor C_{col} is simply the difference between (7.74) and (7.75):

$$C_{col} = C_2 - C_{opto} = 2.9n - 1.3n = 1.6 \text{ nF} \quad (7.76)$$

We are now all set and can proceed with the simulation schematic. It appears in Figure 7.19.

The automated calculation section on the left side helps to adjust the pole/zero pair on the fly in case some adjustments are further needed. The ac results appear in Figure 7.20.

We can see a slight gain mismatch that can be explained by the combined action of the LED dynamic resistor and the bias resistor. If necessary, it can be manually compensated by asking for a gain slightly higher than what is needed at 1 kHz. Practically, it will have no effect on the final loop performance.

7.10 The Type 2: Common-Emitter Configuration and UC384X

The popular UC384X lends itself very well to the implementation of a TL431 compensation network. Its internal op amp features a maximum output current capability of 1 mA: if you try to pull more current out of its pin, the op amp output collapses. Taking advantage of this, we can get rid of the op amp by wiring a pull-up resistor from its output to the 5-V reference voltage. With a maximum output current capability beyond 20 mA, we have enough headroom to select the pull-up resistor of our choice. Figure 7.21 shows the adopted configuration. The transfer function is that described by (7.62).

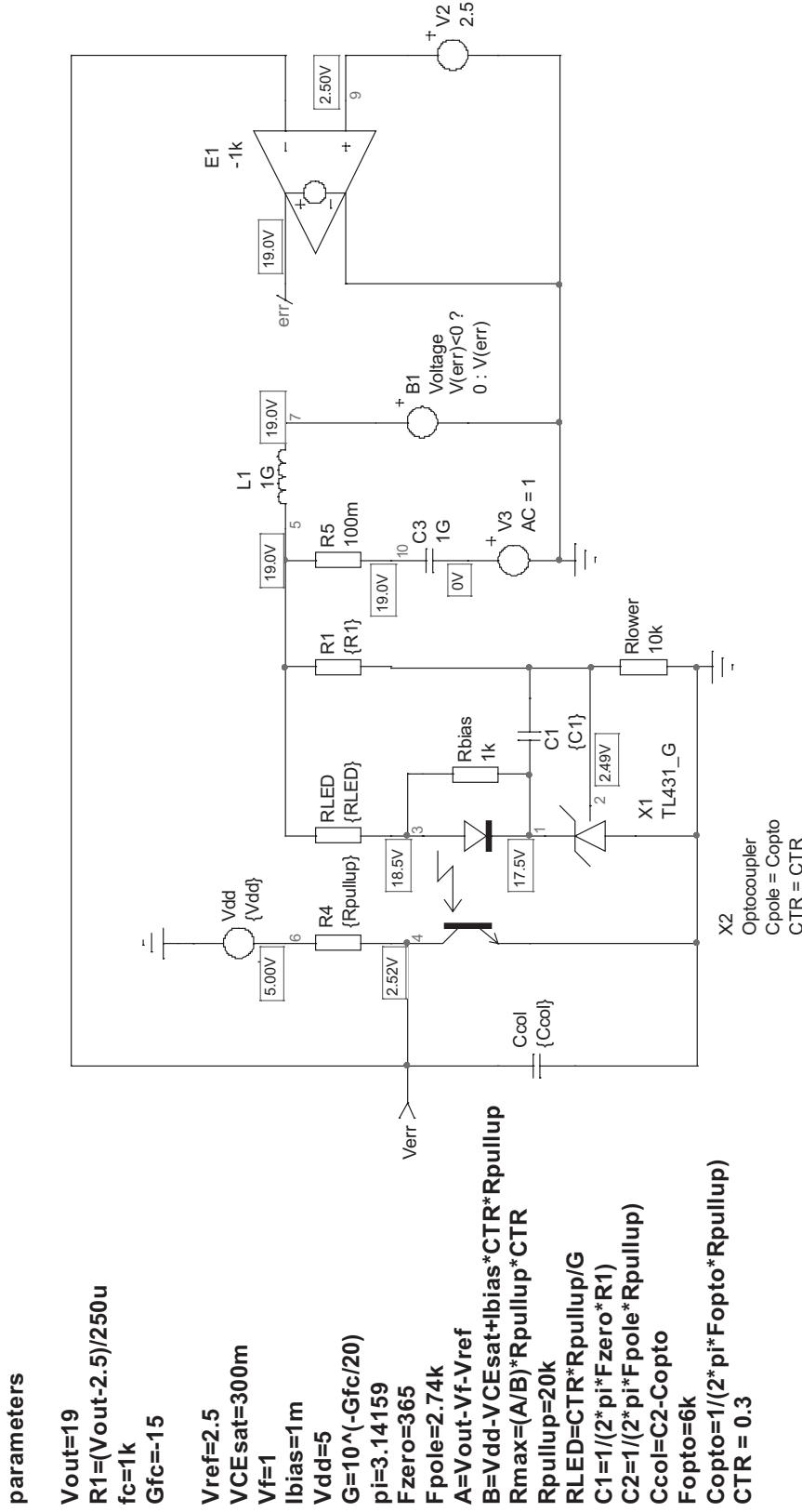


Figure 7.19 The simulation schematic of the TL431 wired in a type 2 configuration.

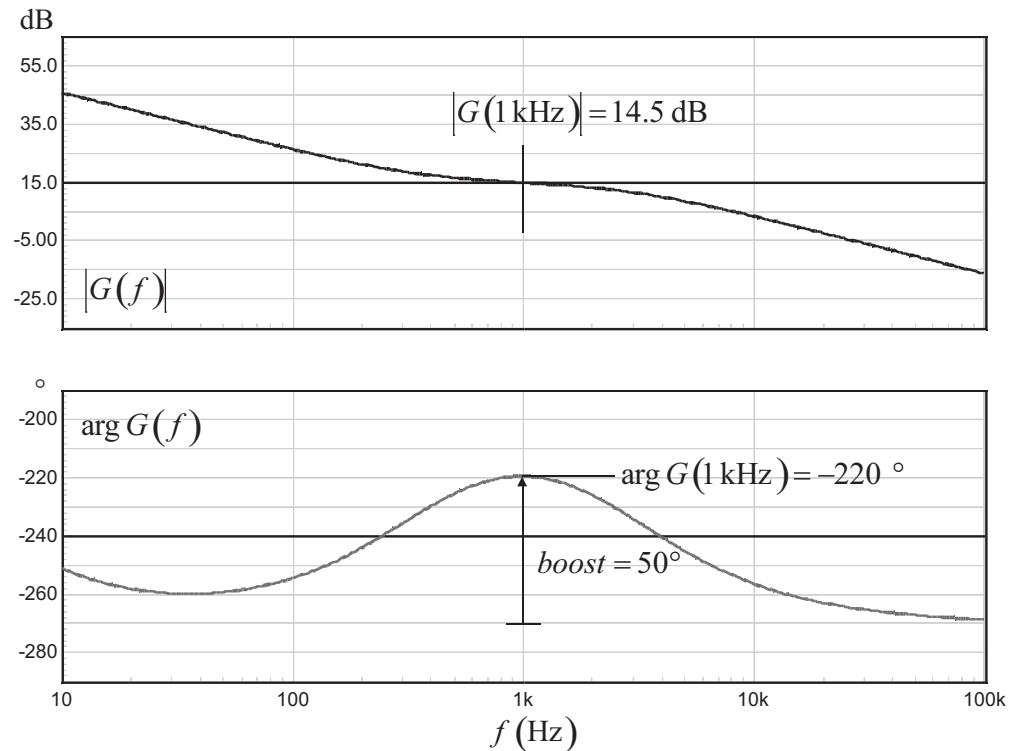


Figure 7.20 The ac results show a slight gain discrepancy, mainly imputable to the LED series resistor and gain deviation brought by the bias resistor.

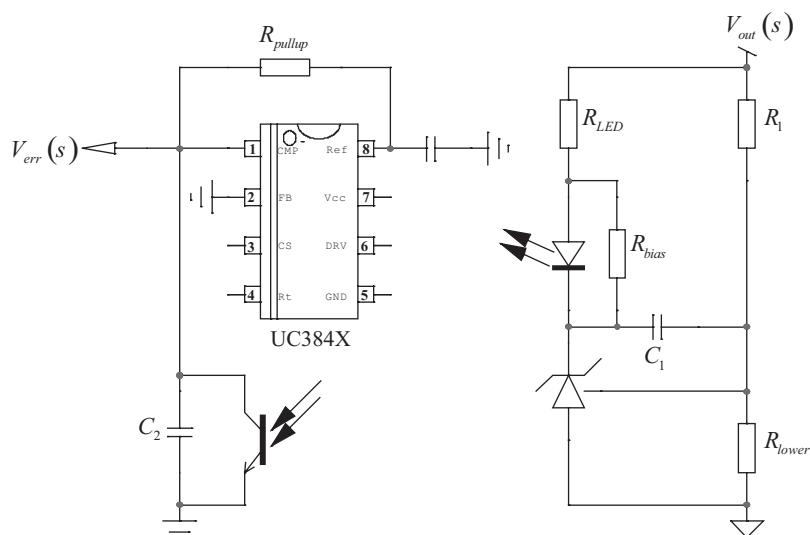


Figure 7.21 By disabling the internal 1-mA source via an extra pull-up resistor connected to the reference voltage, the TL431 can be used as a compensator with a UC384X.

7.11 The Type 2: Common-Collector Configuration and UC384X

The common-collector configuration reverses the control law polarity as indicated by (7.60): if V_{out} deviates from its target by going up, the error voltage increases. In most applications, the error voltage must go down in case of such a deviation. An inversion is thus needed to restore the proper polarity. The internal UC384X op amp can serve this purpose as shown in Figure 7.22. The op amp is wired as a unity gain inverter due to equal resistances values for R_i and R_f . The high-frequency pole is obtained by using C_2 placed across the pull-down resistor. We recommend physically placing this element as close as possible to the PWM controller to minimize noise pickup.

7.12 The Type 2: Disabling the Fast Lane

There are situations where you need flexibility in the selection of the crossover frequency. In other words, you need to select either a gain or an attenuation without being bounded by an upper R_{LED} limit. The way to avoid the limit is to disable the fast lane. As already explained, disabling the fast lane means cutting the parallel path that bypasses the op amp and drives the LED current directly from V_{out} . This is what is illustrated in Figure 7.12 and updated in Figure 7.23.

The transfer function derivation starts by calculating the current circulating in the LED, $I_{LED}(s)$. This current depends on R_{LED} and the TL431 cathode voltage. This is the voltage on the output of the internal op amp, as described by Figure 7.1, arranged in a type 2a configuration:

$$V_{TL431}(s) = -V_{out}(s) \frac{R_2 + \frac{1}{sC_1}}{R_1} = -V_{out}(s) \frac{\frac{sR_2C_1 + 1}{sC_1}}{R_1} = -V_{out}(s) \frac{sR_2C_1 + 1}{sR_1C_1} \quad (7.77)$$

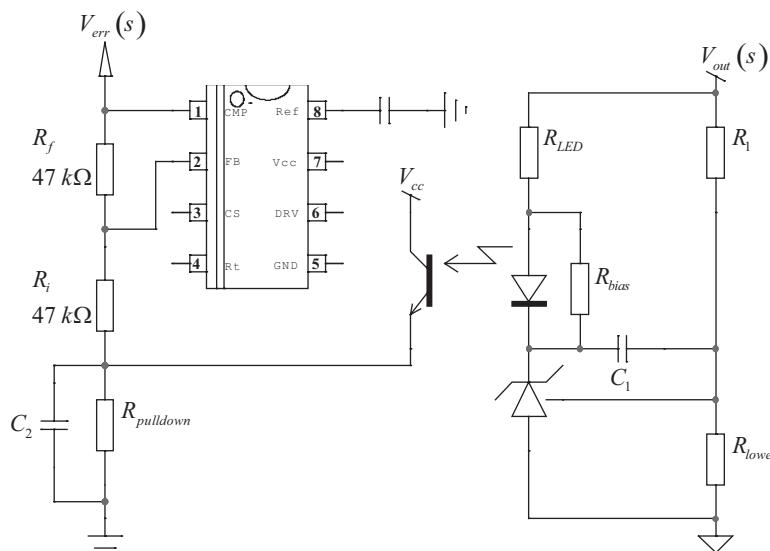


Figure 7.22 A TL431 type 2 wired in a common-collector configuration, driving a UC384X controller whose op amp is wired as an inverter.

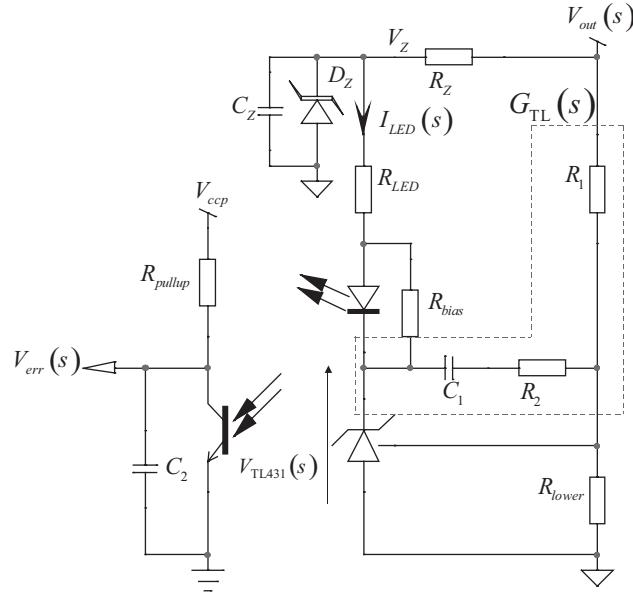


Figure 7.23 The fast lane can be disabled by using a simple Zener-based network or any other type of regulator if needed.

The link to the LED ac current comes easily:

$$I_{LED}(s) = -\frac{V_{TL431}(s)}{R_{LED}} = V_{out}(s) \frac{1}{R_{LED}} \frac{sR_2C_1 + 1}{sR_1C_1} \quad (7.78)$$

This current is conveyed on the optocoupler collector via its CTR. As the feedback voltage is linked to the circulation of the collector current in the network made of R_{pullup} and C_2 in parallel, we have

$$V_{err}(s) = -I_{LED}(s) \text{CTR} \frac{\frac{R_{pullup}}{sC_2}}{\frac{1}{R_{pullup}} + \frac{1}{sC_2}} = -I_{LED}(s) \text{CTR} R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \quad (7.79)$$

The complete transfer function of our type 2 compensator in which the fast lane has been disabled is obtained by combining (7.78) and (7.79):

$$G(s) = -\text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{1 + sR_2C_1}{sR_1C_1(1 + sR_{pullup}C_2)} \quad (7.80)$$

If we factor sR_2C_1 , we can put the transfer function under the following normalized form:

$$G(s) = -\text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \frac{1 + 1/sR_2C_1}{1 + sR_{pullup}C_2} = -G_0 \frac{1 + \omega_z/s}{1 + s/\omega_p} \quad (7.81)$$

where

$$G_0 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} = G_1 G_2 \quad (7.82)$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (7.83)$$

$$G_2 = \frac{R_2}{R_1} \quad (7.84)$$

$$\omega_z = \frac{1}{R_2 C_1} \quad (7.85)$$

$$\omega_p = \frac{1}{R_{pullup} C_2} \quad (7.86)$$

The difference with (7.62) is that the mid-band gain is no longer set by R_{LED} alone, but also by R_2 and R_1 . As R_{LED} is fixed by bias conditions limits—see (7.30)—and R_1 depends on the output voltage setpoint, we have the freedom to adjust R_2 to match our gain requirements. The design thus consists of evaluating the gain block G_1 and checking where to place G_2 so that the product of both gives the mid-band gain we want. This is what the following design example will show.

7.12.1 A Design Example

We want to stabilize a 12-V converter whose transfer function $H(s)$ shows a gain excess of 22 dB at a crossover frequency of 20 Hz. Given the 50° phase boost we need, a type 2 configuration is a must for this design. The component characteristics are the following ones:

$V_{TL431,\min} = 2.5$ V; the TL431 minimum operating voltage.

$I_{bias} = 1$ mA; the additional TL431 bias current.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{ccp} = 5$ V; the pull-up V_{cc} level on the primary side.

$R_{pullup} = 4.7 \text{ k}\Omega$; the optocoupler pull-up resistor.

$\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.

$V_{out} = 12$ V; the converter output voltage.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 10$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

$V_Z = 8.2$ V; the Zener diode breakdown voltage.

$I_{Zbias} = 2$ mA; the Zener diode bias current.

First, we need to calculate the upper limit for the LED resistor. This is made by using (7.34):

$$R_{LED,\max} \leq \frac{8.2 - 1 - 2.5}{5 - 0.3 + 1m \times 0.8 \times 4.7k} 4.7k \times 0.8 \leq 2.09 \text{ k}\Omega \quad (7.87)$$

Adopting a 20 percent safety margin, we select the normalized value of 1.5 kΩ. When associated with the CTR and the pull-up resistor, this network offers a gain G_1 equal to

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} = 0.8 \frac{4.7k}{1.5k} = 2.5 \text{ or } \approx 8 \text{ dB} \quad (7.88)$$

The specification asks for an attenuation of -22 dB. Since we already have a 8 -dB gain with G_1 , G_2 must be calculated to provide an attenuation of -30 dB:

$$G_2 = 10^{\frac{-30}{20}} = 31.6m \quad (7.89)$$

G_2 , as defined by (7.84), involves R_1 and R_2 . As R_1 is fixed, we can immediately obtain the value of R_2 :

$$R_2 = G_2 R_1 = 31.6m \times 38k = 1.2 \text{ k}\Omega \quad (7.90)$$

Where do we place the pole and the zero to obtain the 50° phase boost at 20 Hz? Applying the formulas already derived, we have

$$f_p = \left[\tan(\text{boost}) + \sqrt{\tan^2(\text{boost}) + 1} \right] f_c = 2.74 \times 20 = 54.8 \text{ Hz} \quad (7.91)$$

As the phase peaks at the geometric mean between the pole and the zero, this latter is placed at

$$f_z = \frac{f_c^2}{f_p} = \frac{400}{54.8} = 7.3 \text{ Hz} \quad (7.92)$$

Using (7.85) and (7.86), we can calculate the missing capacitor values:

$$C_1 = \frac{1}{2\pi f_z R_2} = \frac{1}{6.28 \times 7.3 \times 1.2k} = 18.2 \mu\text{F} \quad (7.93)$$

We know that the pole capacitor C_2 is actually made of an extra capacitor C_{col} that we will place in parallel with the collector-emitter parasitic capacitor from the optocoupler:

$$C_2 = \frac{1}{2\pi R_{pullup} f_p} = \frac{1}{6.28 \times 4.7k \times 54.8} = 618.3 \text{ nF} \quad (7.94)$$

Given the characterized optocoupler pole at 10 kHz, the parasitic capacitor is found to be

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 10k \times 4.7k} = 3.4 \text{ nF} \quad (7.95)$$

As the total capacitance is 2.9 nF, the added capacitor C_{col} is simply the difference between (7.74) and (7.75):

$$C_{col} = C_2 - C_{opto} = 618.3n - 3.4n = 615 \text{ nF} \quad (7.96)$$

It is however likely that a $0.68\text{-}\mu\text{F}$ capacitor will be used; therefore, the optocoupler contribution can be neglected.

Let us now have a look at the Zener network. Given the 12-V output, an 8.2-V Zener diode seems an appropriate pick. The choice of the Zener value is dictated by

several arguments: the voltage needs to be sufficiently low compared to the output voltage in order to ensure a good ac isolation between the two dc lines. On the other hand, the Zener voltage must be high enough to offer sufficient bias headroom to the TL431 network. Experience shows that choosing V_Z as being two thirds of the output voltage represents a good tradeoff. By looking at the Zener diode specifications, a 2-mA bias current seems like the correct number to make the device operate far enough from its knee. With these parameters now known, we can calculate the value of the dropping resistor R_Z with the help of (7.37):

$$\begin{aligned} R_Z &= \frac{(V_{out} - V_Z)R_{pullup}\text{CTR}_{\min}}{(V_{ccp} - V_{CE,sat}) + (I_{Zbias} + I_{bias})R_{pullup}\text{CTR}_{\min}} \\ &= \frac{(12 - 8.2) \times 4.7k \times 0.8}{(5 - 0.3) + (2m + 1m) \times 4.7k \times 0.8} = 894 \Omega \end{aligned} \quad (7.97)$$

To improve the decoupling action at low frequencies, a $10-\mu\text{F}$ capacitor is added in parallel with the Zener diode. We have everything now, and we can proceed with the application schematic shown in Figure 7.24. The dc values appearing on the sketch confirm the system is well biased. Let us have a look at the ac response, which is delivered in Figure 7.25.

As we can observe on the graph, the -22-dB target is missed by 3 dB. Despite the small error brought by the LED dynamic resistor R_d , which is neglected in the calculation (around 0.5 dB), the lack of perfect ac decoupling between the regulated voltage V_Z and the output level is the main offender. The mismatch can be compensated by increasing the target by 3-4 dB (e.g., asking for a 26-dB gain rather than the original 22 dB). Another option consists of using an active regulator based on a bipolar, as exemplified in Figure 7.26. Using this technique, the ac analysis shows an error mismatch reduced by 1 dB. This is what Figure 7.27 confirms, comparing both ac responses between Zener-based and a bipolar-based regulators.

As a conclusion, we can see that ac decoupling the fast lane affects the transfer function. Therefore, you must carefully design the ac decoupling circuitry if you plan to suppress the fast lane.

7.13 The Type 3: An Origin Pole plus a Double Pole/Zero Pair

Because of the fast lane presence, the TL431 does not lend itself very well to a type 3 architecture. As we will see in a few lines, the LED series resistor plays two roles, setting new limits on the design procedure. However, in some voltage-mode converters, there is a need for a phase boost higher than 90° where the type 3 with a TL431 still represents a possible candidate. Its architecture appears in Figure 7.28.

The derivation starts by the ac LED current definition, involving the impedance delimited as Z_{LED} in Figure 7.28. The ac current deviated through the bias resistor R_{bias} is purposely neglected:

parameters	parameters
$Vout=12$	$Rmax=((Vz-Vf-Vref)/(Vccp-VCEsat)+(Ibias*(Rpullup*CTR)))*Rpullup*CTR$
	$RLED=Rmax*0.8$
	$Za=(Vout-Vz)*Rpullup*CTR$
	$Zb=(Vccp-VCEsat)+(Ibias*Rpullup*CTR)$
$Ibias=20$	$Rz=Za/Zb$
$Gfc=22$	$fp=(\tan(\text{boost}*\pi/180)+\sqrt{(\tan(\text{boost}*\pi/180))^2+1})*fc$
$\text{boost}=50$	$fz=fc^2/fp$
$Vf=1$	
$Ibias=1m$	
$Vref=2.5$	
$VCEsat=300m$	
$Vccp=5$	
$Vz=8.2$	
$Ibias=1m$	
$Rpullup=4.7k$	
$Fopto=10k$	
$Copto=1/(2*pi*Rpullup*Fopto)$	
$CTR=0.8$	
$G1=Rpullup*CTR/RLED$	
$G2=10^{(-Gfc/20)}$	
$G=G2/G1$	
$pi=3.14159$	
$C1=1/(2*pi*fz*R2)$	
$C2=1/(2*pi*fp*Rpullup)$	
$Ccol=C2-Copto$	
$R2=G*R1$	

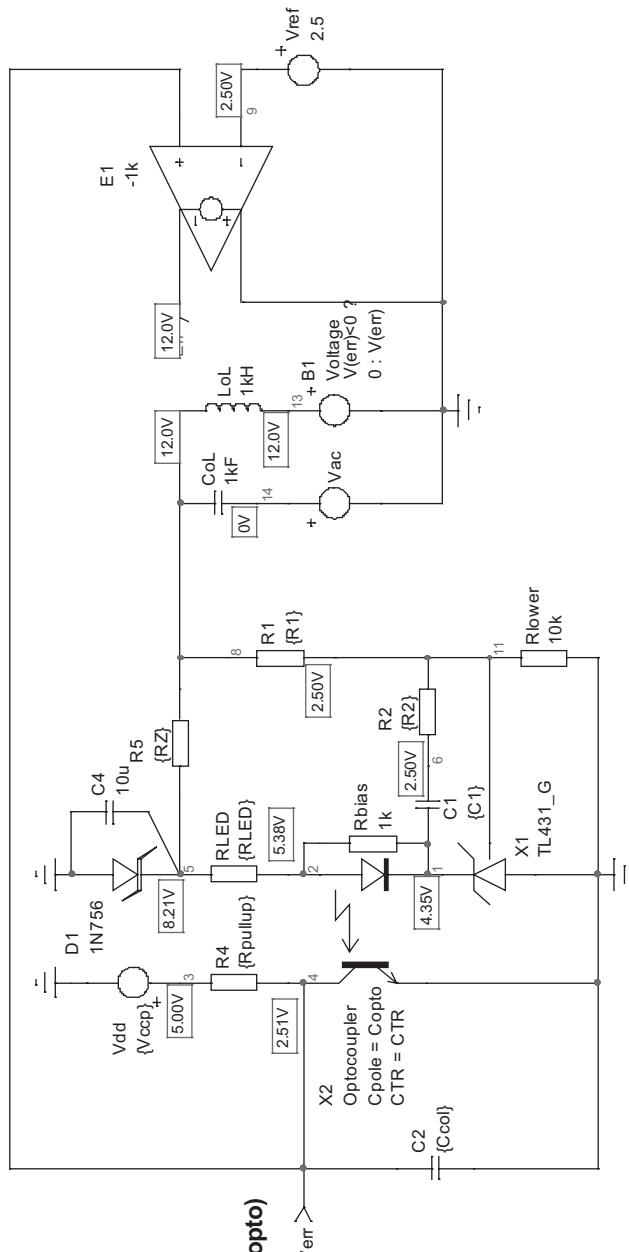


Figure 7.24 The application schematic of the TL431-based type 2 compensator where the fast lane has been disabled.

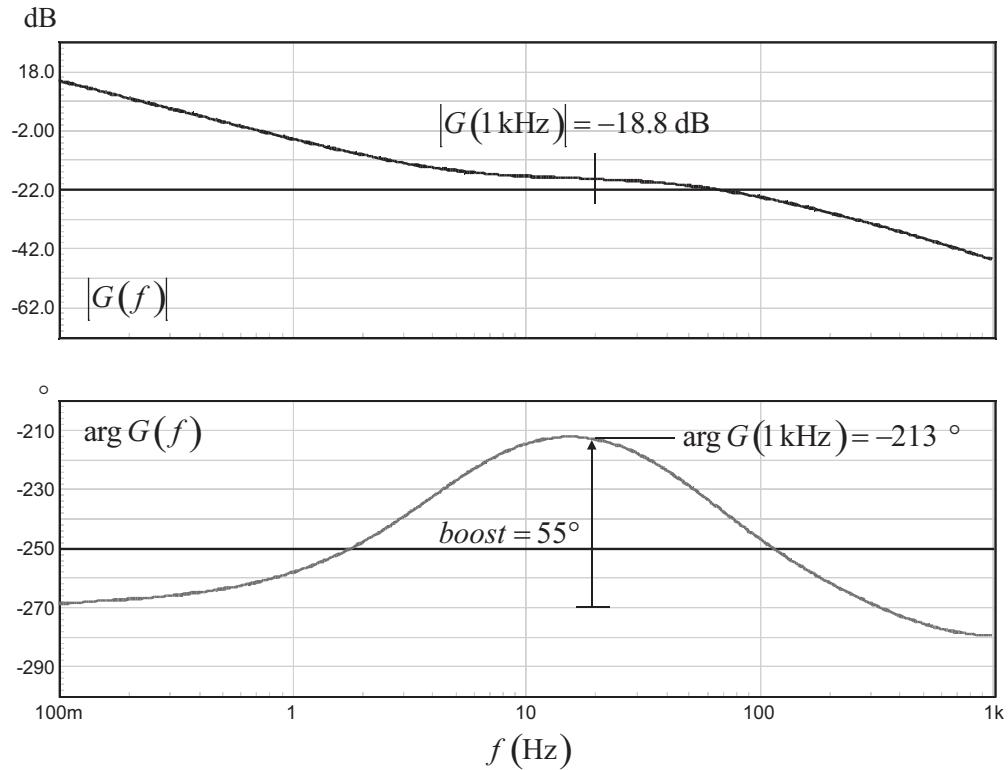


Figure 7.25 The dc response of the Zener-based schematic shows a target mismatch of 3 dB.

$$I_{LED}(s) = \frac{V_{out}(s) - V_{TL431}(s)}{Z_{LED}} = (V_{out}(s) - V_{TL431}(s)) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)} \quad (7.98)$$

The output voltage on the TL431 cathode, $V_{TL431}(s)$, is that of a type 1 compensator:

$$V_{TL431}(s) = -\frac{1}{sC_1R_1}V_{out}(s) \quad (7.99)$$

Substituting (7.99) into (7.98), we obtain

$$I_{LED}(s) = \left(V_{out}(s) + V_{out}(s) \frac{1}{sR_1C_1} \right) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)} \quad (7.100)$$

$$= V_{out}(s) \left(\frac{1 + sR_1C_1}{sR_1C_1} \right) \frac{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)}$$

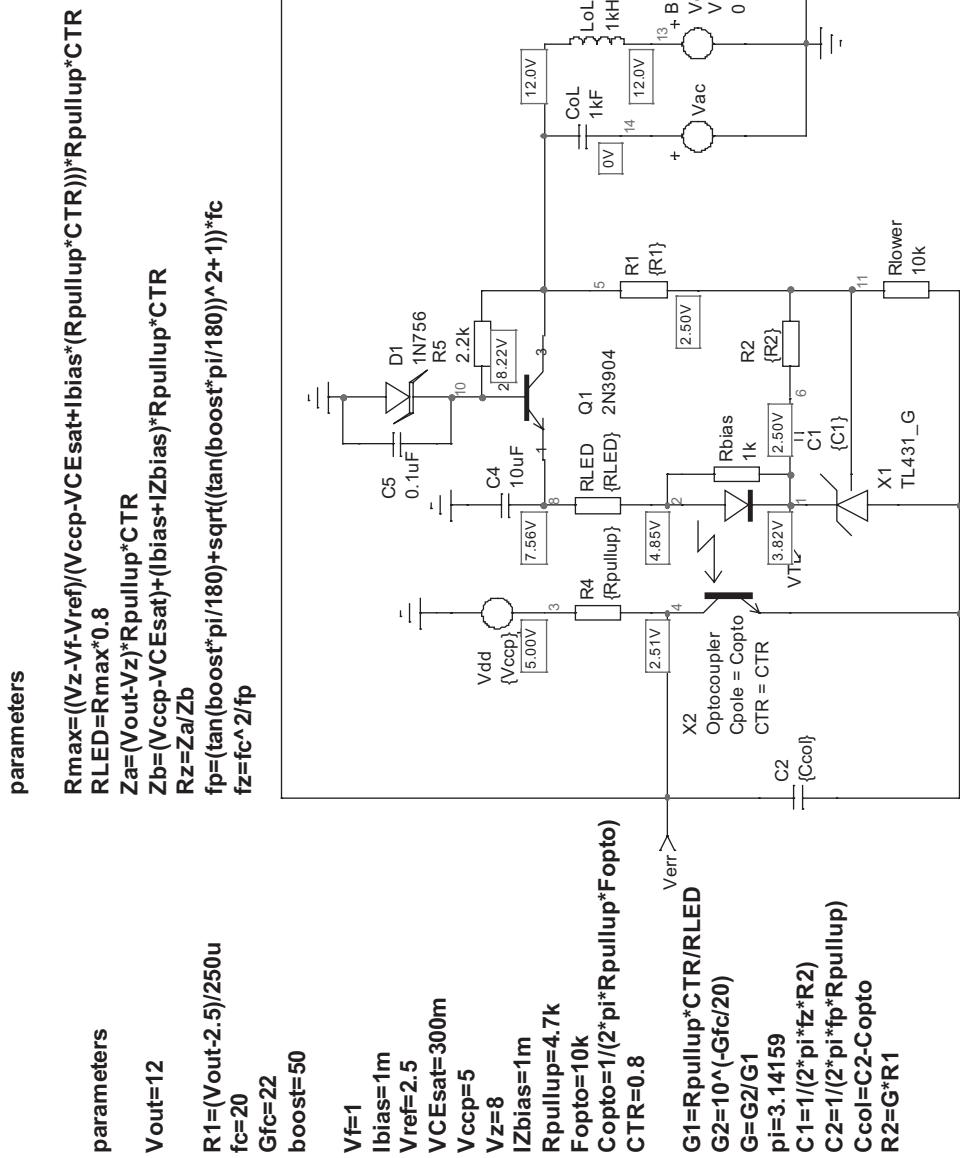


Figure 7.26 A bipolar transistor helps to better reject the ac modulation superimposed on the monitored output voltage.

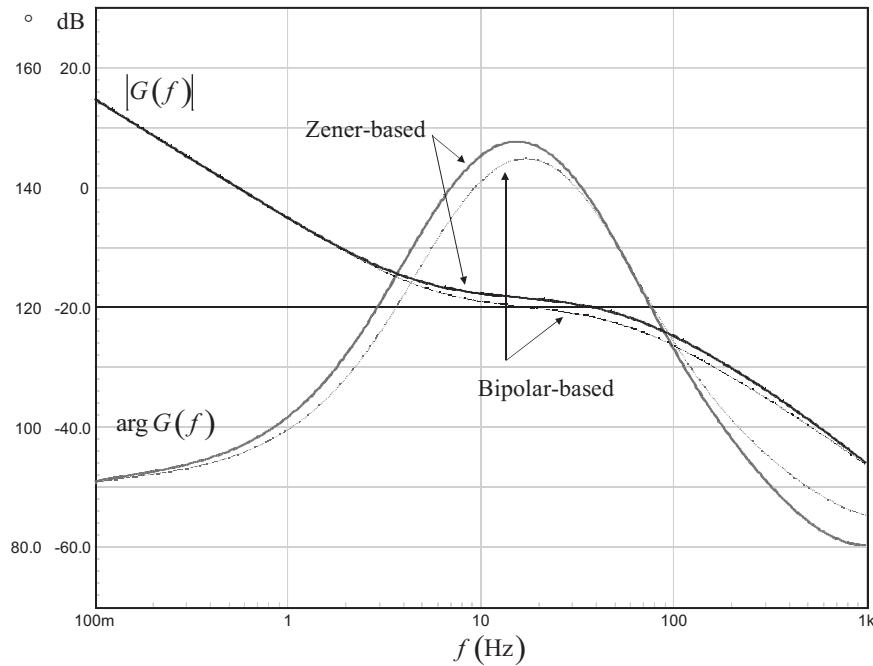


Figure 7.27 Ensuring a better ac decoupling between the TL431 bias and the observed variable clearly improves the overall shape.

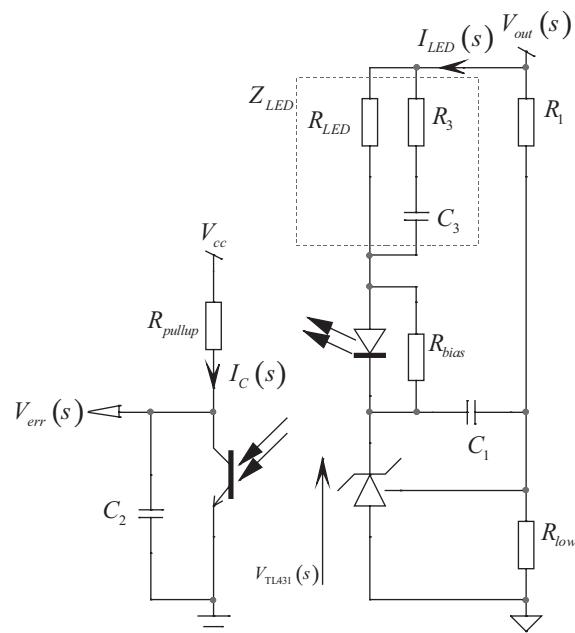


Figure 7.28 The TL431 can be wired in a type 3 configuration; however, the fast lane presence hampers its field of applications.

Rearranging the previous, we have

$$I_{LED}(s) = V_{out}(s) \left(\frac{1 + sR_1C_1}{sR_1C_1} \right) \frac{s(R_{LED} + R_3)C_3 + 1}{R_{LED}(sC_3R_3 + 1)} \quad (7.101)$$

Now realizing that the error voltage $V_{err}(s)$ is linked to the LED current by the optocoupler CTR, we have

$$V_{err}(s) = -I_{LED}(s)R_{pullup} \frac{1}{1 + sR_{pullup}C_2} \text{CTR} \quad (7.102)$$

Substituting (7.101) into (7.102) and rearranging, we obtain the transfer function we are looking for:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{\frac{1 + 1/sR_1C_1}{1 + sR_{pullup}C_2} \frac{sC_3(R_{LED} + R_3) + 1}{1 + sC_3R_3}}{1 + sC_3R_3} = -G_0 \frac{1 + \omega_{z1}/s}{1 + s/\omega_{p1}} \frac{1 + s/\omega_{z2}}{1 + s/\omega_{p2}} \quad (7.103)$$

In this equation, we can identify poles, zeros, and a static gain:

$$G_0 = \frac{R_{pullup}}{R_{LED}} \text{CTR} \quad (7.104)$$

$$\omega_{z1} = \frac{1}{R_1C_1} \quad (7.105)$$

$$\omega_{z2} = \frac{1}{(R_{LED} + R_3)C_3} \quad (7.106)$$

$$\omega_{p1} = \frac{1}{R_{pullup}C_2} \quad (7.107)$$

$$\omega_{p2} = \frac{1}{R_3C_3} \quad (7.108)$$

The magnitude of (7.103) is given by

$$|G(f_c)| = G_0 \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} = \frac{R_{pullup}}{R_{LED}} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (7.109)$$

Then, combining (7.109), (7.105), (7.106), and (7.108) and solving for R_{LED} , R_3 , C_1 , C_2 , and C_3 , we can extract the definitions we need to design the compensator:

$$R_{LED} = \frac{R_{pullup}}{G} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (7.110)$$

$$C_3 = \frac{f_{p2} - f_{z2}}{2\pi f_{p2} f_{z2}} \frac{G}{R_{pullup} \text{CTR}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}} \quad (7.111)$$

$$R_3 = \frac{f_{z2}}{f_{p2} - f_{z2}} \frac{R_{pullup}}{G} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (7.112)$$

$$C_1 = \frac{1}{2\pi f_{z1} R_1} \quad (7.113)$$

$$C_2 = \frac{1}{2\pi R_{pullup} f_{p2}} \quad (7.114)$$

Unfortunately, as with any TL431-based designs, the limit for the LED series resistor values is set by the biasing conditions around the component. We have already derived the maximum value this resistor can take via (7.30). If we combine this definition with the gain expressed in (7.109), we obtain the minimum gain the compensator can be designed for:

$$|G_{\min}| = \frac{V_{cc} - V_{CE,sat} + I_{bias}R_{pullup}\text{CTR}_{\min}}{V_{out} - V_f - V_{TL431,\min}} \frac{\sqrt{1 + \left(\frac{f_{z1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p2}}\right)^2}} \quad (7.115)$$

This G_{\min} term illustrates the crossover gain below which the compensator cannot be designed. For instance, should you find a G_{\min} of 5 dB with (7.115), you could simply not select a crossover frequency where a 3-dB gain is needed. It would not satisfy the biasing conditions for the TL431. However, 6 dB would. Changing the optocoupler CTR or R_{pullup} will not help to modify the result. Actually, (7.115) is made of two terms: the first one (involving V_{TL431} , V_{out} , and so on) corresponds to the minimum biasing conditions needed to operate the TL431-based compensator. The second term involves the poles and zeros position—in other words, the needed phase boost. You can therefore see G_{\min} as another limit for the maximum phase boost you can ask for a selected gain. We have derived an equation linking G_{\min} and the phase boost you want. The result appears next:

$$G_{\min}(\text{boost}) = 20 \log_{10} \left(\frac{V_{cc} - V_{CE,sat} + I_{bias}R_{pullup}\text{CTR}_{\min}}{V_{out} - V_f - V_{TL431,\min}} \sqrt{\cot^2 \left(\frac{\text{boost}}{4} - 45 \right)} \right) \quad (7.116)$$

If we consider the following standard values for the first term of the expression, we can plot (7.116), sweeping the phase boost between 0 and 180° :

$V_{TL431} = 2.5$ V; the TL431 minimum operating voltage.

$V_{out} = 12$ V; the regulated output voltage.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$I_{bias} = 1$ mA; the TL431 extra biasing current.

$R_{pullup} = 20$ k Ω ; the pull-up resistor loading the optocoupler collector.

$CTR_{min} = 0.3$; the CTR associated with the 20-k Ω pull-up resistor.

The result appears in Figure 7.29 and shows a gain starting from a minimum value close to 0 dB (a null phase boost when both poles and zeros are coincident) and going up as the required phase boost increases. Therefore, when using this type of compensator, it will be important to choose a crossover frequency where the needed gain and phase boost do not conflict with (7.115). Should you need a phase boost of 150° , given the adopted component values, the graph instructs us that any crossover point requiring more than 18 dB of gain are possible candidates.

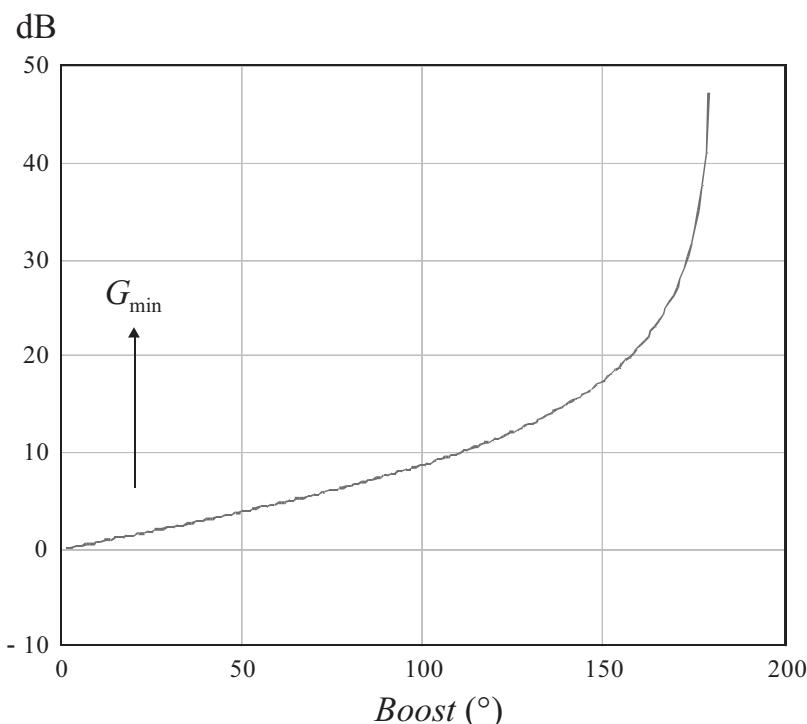


Figure 7.29 The burden of the LED series resistor seriously hampers the gain choices as the required phase boost increases.

7.13.1 A Design Example

In this example, we want to cross over at a 1-kHz frequency with a 15-dB amplification. The needed phase boost is 120°. The parameter list appears next; this is a 12-V converter:

- $V_{TL431,\min} = 2.5$ V; the TL431 minimum operating voltage.
- $I_{bias} = 1$ mA; the TL431 biasing current.
- $V_Z = 8.2$ V; the Zener diode breakdown voltage.
- $I_{Zbias} = 2$ mA; the Zener diode bias current.
- $V_f = 1$ V; the LED forward voltage.
- $V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.
- $V_{cc} = 5$ V; the pull-up V_{cc} level.
- $V_{out} = 12$ V; the converter output voltage.
- $R_{pullup} = 20$ kΩ; the optocoupler pull-up resistor.
- $CTR_{\min} = 0.3$; the minimum optocoupler current transfer ratio.
- $R_1 = 38$ kΩ; the upper resistor in the resistor bridge observing the output variable.
- $f_{opto} = 6$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

Given the needed 120° phase boost at 1 kHz, we first assume to place coincident poles and zeros at a place to be determined. Capitalizing on what has already been derived, we will place a pole pair at the following position:

$$f_{p1,2} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{1k}{268m} \approx 3.7 \text{ kHz} \quad (7.117)$$

The double zero will be located at

$$f_{z1,2} = \frac{f_c^2}{f_p} = \frac{1k^2}{3.7k} \approx 270 \text{ Hz} \quad (7.118)$$

The maximum allowable series LED resistor is first evaluated to check the upper limit:

$$R_{LED,\max} \leq \frac{12 - 1 - 2.5}{5 - 0.3 + 1m \times 0.3 \times 20k} 20k \times 0.3 \leq 4.8 \text{ k}\Omega \quad (7.119)$$

The type 3 passive elements are calculated using (7.110) through (7.114):

$$R_{LED} = \frac{20k}{10^{20}} \times 0.3 \times \frac{\sqrt{1 + \left(\frac{270}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{270}\right)^2}}{\sqrt{1 + \left(\frac{1k}{3.7k}\right)^2} \sqrt{1 + \left(\frac{1k}{3.7k}\right)^2}} \approx 4 \text{ k}\Omega \quad (7.120)$$

Checking this value against that given by (7.119), we are below the limit, leaving us a little margin.

$$C_3 = \frac{3.7k - 270}{6.28 \times 3.7k \times 270} \times \frac{10^{\frac{15}{20}}}{20k \times 0.3} \times \frac{\sqrt{1 + \left(\frac{1k}{3.7k}\right)^2} \sqrt{1 + \left(\frac{1k}{3.7k}\right)^2}}{\sqrt{1 + \left(\frac{270}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{270}\right)^2}} = 138 \text{ nF} \quad (7.121)$$

$$R_3 = \frac{270}{3.7k - 270} \times \frac{20k}{10^{\frac{15}{20}}} \times 0.3 \times \frac{\sqrt{1 + \left(\frac{270}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{270}\right)^2}}{\sqrt{1 + \left(\frac{1k}{3.7k}\right)^2} \sqrt{1 + \left(\frac{1k}{3.7k}\right)^2}} = 308 \Omega \quad (7.122)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_1} = \frac{1}{6.28 \times 270 \times 38k} = 15.5 \text{ nF} \quad (7.123)$$

$$C_2 = \frac{1}{2\pi R_{pullup} f_{p2}} = \frac{1}{6.28 \times 20k \times 3.7k} = 2.15 \text{ nF} \quad (7.124)$$

We know that the total capacitor connected across the optocoupler that forms C_2 is actually made of the optocoupler parasitic pole C_{opto} and the added capacitor C_{col} . The optocoupler pole is located at 6 kHz. Given a pull-up resistor of 20 kΩ, we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} = 1.3 \text{ nF} \quad (7.125)$$

When subtracted from (7.124), you obtain the value for C_{col} , the final capacitor installed across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 2.15n - 1.3n \approx 850 \text{ pF} \quad (7.126)$$

We have everything on hand, we can now check the resulting ac response via our test fixture. It appears in Figure 7.30.

The simulation results are available in Figure 7.31 and show a slight gain discrepancy, explained, as usual, by the LED diode dynamic resistor added to the ac current deviated by the 1-kΩ bias resistor.

7.14 The Type 3: An Origin Pole plus a Double Pole/Zero Pair—No Fast Lane

In the previous example, we have seen that the LED resistor was slightly below its maximum value, leaving a weak design margin. If we had needed a lower gain or a

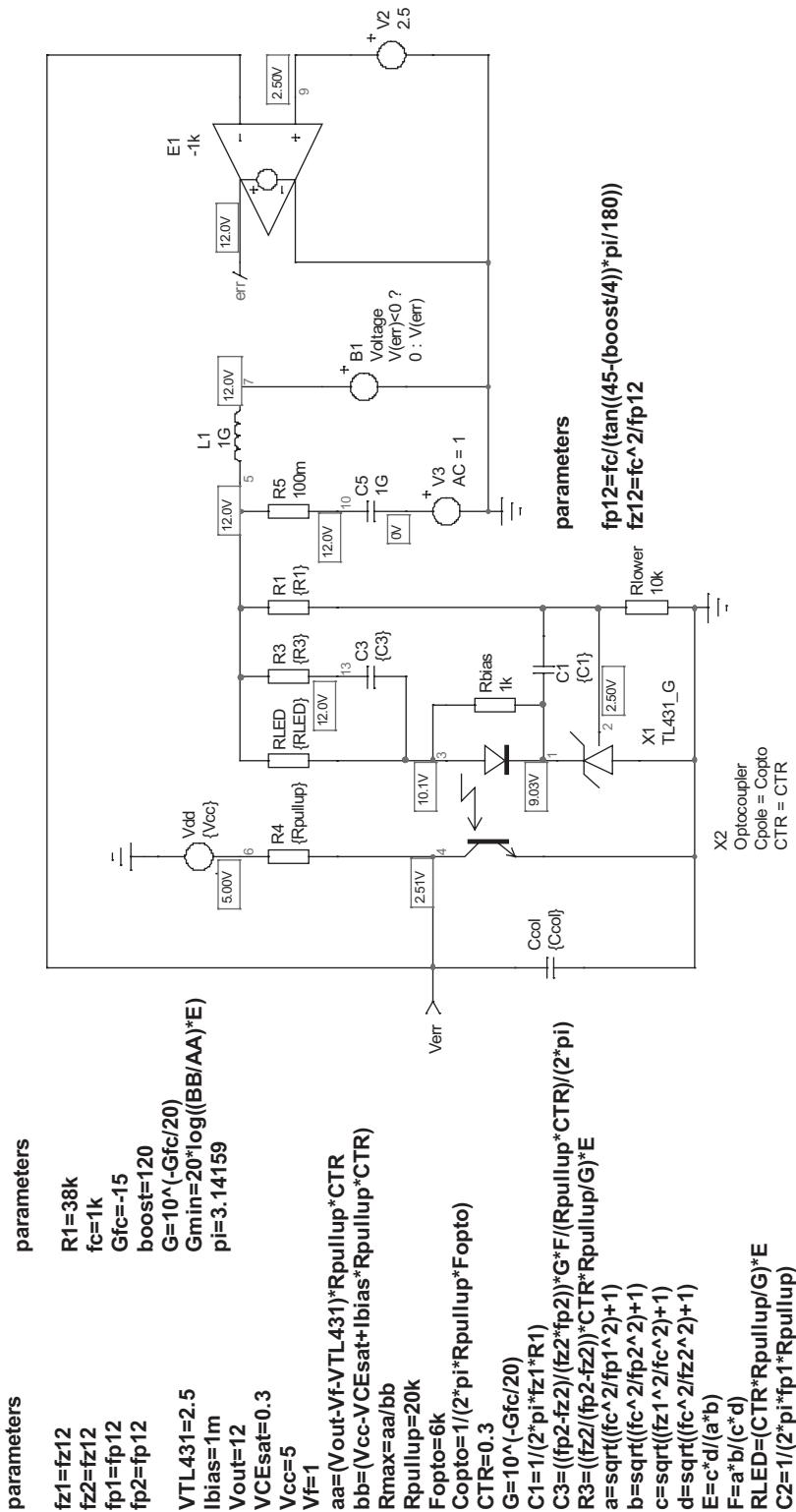


Figure 7.30 The type 3 made with a TL431 can work, but the phase boost and the allowable gain are intimately linked, hampering the flexibility of use.

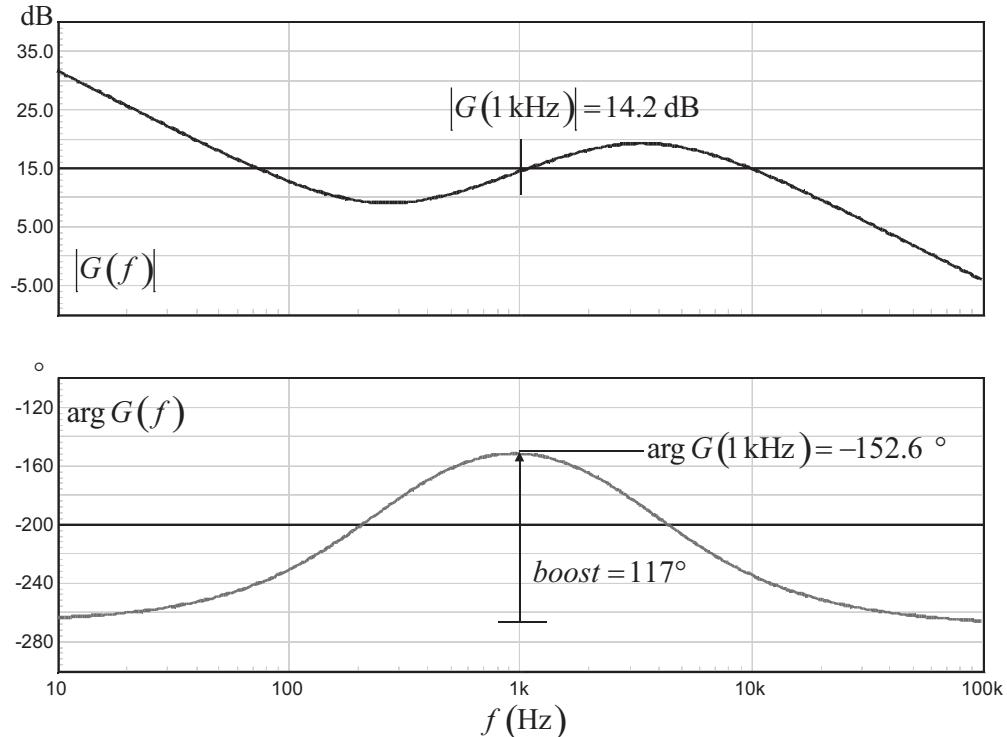


Figure 7.31 The ac response shows results that agree very well with the initial target.

larger phase boost at crossover, we would have hit the limit imposed by the biasing conditions around the TL431. Such problems can be easily overcome by disabling the fast lane. The type 3 with a disabled fast lane appears in Figure 7.32.

The schematic reveals a cascaded configuration where a kind of type 3a circuit appears in the $G_{TL}(s)$ transfer function (2 zeros, 1 origin pole and 1 pole), immediately followed by the optocoupler path, exhibiting a transfer function $O(s)$ affected by a gain and a pole. This latter is now well known and can be expressed as follows:

$$O(s) = \frac{V_{err}(s)}{V_{TL431}(s)} = \frac{R_{pullup}CTR}{R_{LED}} \frac{1}{1 + sR_{pullup}C_2} \quad (7.127)$$

The ac voltage across the TL431 is the ac output voltage multiplied by the ratio of impedances Z_f and Z_i , respectively, involving C_1R_2 and $R_1R_3C_3$:

$$Z_f = R_2 + \frac{1}{sC_1} = \frac{sR_2C_1 + 1}{sC_1} \quad (7.128)$$

$$Z_i = \left(\frac{1}{sC_3} + R_3 \right) \parallel R_1 = \frac{R_1(1 + sR_3C_3)}{sC_3(R_1 + R_3) + 1} \quad (7.129)$$

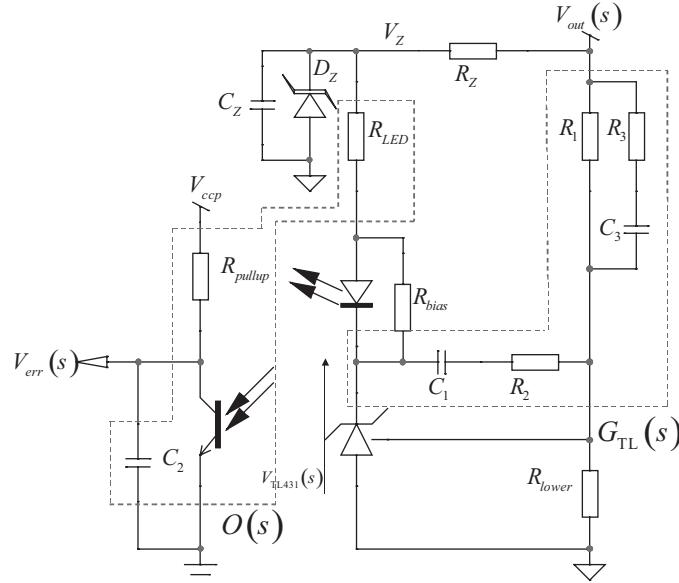


Figure 7.32 The fast lane must be disabled to obtain the best from the type 3 built with a TL431.

$$\begin{aligned}
 G_{\text{TL}}(s) &= -\frac{Z_f}{Z_i} = -\frac{\frac{sR_2C_1 + 1}{sC_1}}{\frac{R_1(1 + sR_3C_3)}{sC_3(R_1 + R_3) + 1}} \\
 &= -\frac{sR_2C_1 + 1}{sR_1C_1} \frac{sC_3(R_1 + R_3) + 1}{(1 + sR_3C_3)} = -\frac{R_2}{R_1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)(1 + sC_3(R_1 + R_3))}{1 + sR_3C_3}
 \end{aligned} \tag{7.130}$$

Once (7.130) and (7.127) are multiplied together and the voltage to current gain from (7.78) is included, we obtain the complete transfer function we are looking for:

$$G(s) = -\frac{R_2R_{\text{pullup}}\text{CTR}}{R_{\text{LED}}R_1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)(1 + sC_3(R_1 + R_3))}{(1 + sR_{\text{pullup}}C_2)(1 + sR_3C_3)} \tag{7.131}$$

This expression can be put under the normalized form:

$$G(s) = -G_0 \frac{\left(1 + \frac{\omega_{z_1}}{s}\right)\left(1 + \frac{s}{\omega_{z_2}}\right)}{\left(1 + \frac{s}{\omega_{p_1}}\right)\left(1 + \frac{s}{\omega_{p_2}}\right)} \tag{7.132}$$

where

$$G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} \frac{R_2}{R_1} = G_1 G_2 \tag{7.133}$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad (7.134)$$

$$G_2 = \frac{R_2}{R_1} \quad (7.135)$$

$$\omega_{z_1} = \frac{1}{R_2 C_1} \quad (7.136)$$

$$\omega_{z_2} = \frac{1}{C_3(R_1 + R_3)} \quad (7.137)$$

$$\omega_{p_1} = \frac{1}{R_3 C_3} \quad (7.138)$$

$$\omega_{p_2} = \frac{1}{R_{pullup} C_2} \quad (7.139)$$

The magnitude of (7.132) is given by

$$|G(f_c)| = \text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{R_2}{R_1} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (7.140)$$

Then, combining and solving for R_{LED} , R_3 , C_2 , C_1 , and C_3 , we can extract the definitions we are looking for:

$$R_2 = \frac{GR_1R_{LED}}{R_{pullup}\text{CTR}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}} \quad (7.141)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} \quad (7.142)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad (7.143)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pullup}} \quad (7.144)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_1 f_{p_2} f_{z_2}} \quad (7.145)$$

With the fast lane removed, the LED resistor no longer plays a role in the pole/zero positions. Its value now solely depends on acceptable bias conditions to give the TL431 the necessary voltage swing, despite unavoidable dispersions on the optocoupler CTR. The formula derived in (7.30) is valid:

$$R_{LED,max} \leq \frac{V_Z - V_f - V_{TL431,min}}{V_{cc} - V_{CE,sat} + I_{bias}CTR_{min}R_{pullup}} R_{pullup}CTR_{min} \quad (7.146)$$

In this expression, the V_Z term represents the selected Zener level obtained from the output. We already derived its value and it appears next:

$$R_Z = \frac{(V_{out} - V_Z)R_{pullup}CTR_{min}}{(V_{cc} - V_{CE,sat}) + (I_{Zbias} + I_{bias})R_{pullup}CTR_{min}} \quad (7.147)$$

All component values are now attached to a design formula, so it is time for the design example!

7.14.1 A Design Example

In this example, we have to cross over at a 1-kHz frequency where a -10-dB attenuation is needed. At the crossover point, the phase must be boosted by 130°. The parameter list appears next and does not change.

$V_{TL431,min} = 2.5$ V; the TL431 minimum operating voltage.

$I_{bias} = 1$ mA; the TL431 biasing current.

$V_Z = 8.2$ V; the Zener diode breakdown voltage.

$I_{Zbias} = 2$ mA; the Zener diode biasing current.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$V_{out} = 12$ V; the converter output voltage.

$R_{pullup} = 20$ kΩ; the optocoupler pull-up resistor.

$CTR_{min} = 0.3$; the minimum optocoupler current transfer ratio.

$R_1 = 38$ kΩ; the upper resistor in the resistor bridge observing the output variable.

$f_{opto} = 6$ kHz; the optocoupler pole that has been characterized with R_{pullup} .

Given the needed 130° phase boost at 1 kHz, we first assume we must place coincident poles and zeros at a location to be determined. Capitalizing on what has already been derived, we will place a pole pair at the following position:

$$f_{p1,2} = \frac{f_c}{\tan\left(45 - \frac{\text{boost}}{4}\right)} = \frac{1k}{221m} \approx 4.5 \text{ kHz} \quad (7.148)$$

The double zero will be located at

$$f_{z_{1,2}} = \frac{f_c^2}{f_p} = \frac{1k^2}{4.5k} \approx 221 \text{ Hz} \quad (7.149)$$

First, let us select the LED series resistor using (7.146):

$$R_{LED,\max} \leq \frac{8.2 - 1 - 2.5}{5 - 0.3 + 1m \times 0.3 \times 20k} 20k \times 0.3 \leq 2.6 \text{ k}\Omega \quad (7.150)$$

Including a 20 percent safety margin, we will choose a 1.8-kΩ resistor. Having this on hand, we can calculate the gain brought by the optocoupler path alone:

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} = 0.3 \times \frac{20k}{2.1k} = 2.85 \text{ or } 9.1 \text{ dB} \quad (7.151)$$

Given the needed 10-dB attenuation, the attenuation we expect from the TL431 chain is simply

$$G_2 = G - G_1 = -10 - 9.1 = -19.1 \text{ dB or } 0.111 \quad (7.152)$$

The rest of the component values are derived using (7.141) through (7.145):

$$R_2 = \frac{0.11 \times 38k \times 1.8k}{20k \times 0.3} \frac{\sqrt{1 + \left(\frac{1k}{4.5k}\right)^2} \sqrt{1 + \left(\frac{1k}{4.5k}\right)^2}}{\sqrt{1 + \left(\frac{221}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{221}\right)^2}} = 936 \Omega \quad (7.153)$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} = \frac{38k \times 221}{4.5k - 221} \approx 2 \text{ k}\Omega \quad (7.154)$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_2} = \frac{1}{6.28 \times 221 \times 1.8k} \approx 777 \text{ nF} \quad (7.155)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pullup}} = \frac{1}{6.28 \times 4.5k \times 20k} \approx 1.8 \text{ nF} \quad (7.156)$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_1 f_{p_2} f_{z_2}} = \frac{4.5k - 221}{6.28 \times 38k \times 4.5k \times 221} \approx 18 \text{ nF} \quad (7.157)$$

We know that the total capacitor connected across the optocoupler that forms C_2 is actually made of the optocoupler parasitic pole C_{opto} and the added capacitor C_{col} . The optocoupler pole is located at 6 kHz. Given a pull-up resistor of 20 kΩ, we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} \approx 1.3 \text{ nF} \quad (7.158)$$

Subtracted from C_2 value, we obtain the capacitor we need to install across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 1.8n - 1.3n = 500 \text{ pF} \quad (7.159)$$

The Zener diode biasing resistor is found by using (7.147):

$$\begin{aligned} R_Z &= \frac{(V_{out} - V_Z)R_{pullup}\text{CTR}_{\min}}{(V_{cc} - V_{CE,sat}) + (I_{Zbias} + I_{bias})R_{pullup}\text{CTR}_{\min}} \\ &= \frac{(12 - 8.2) \times 20k \times 0.3}{5 - 0.3 + (2m + 1m) \times 20k \times 0.3} = 1 \text{ k}\Omega \end{aligned} \quad (7.160)$$

We now have everything on hand and can carry on with the simulation test fixture. It appears in Figure 7.33.

The operating points on the picture shows that the system is well stabilized. We can then start the ac simulation and its results appear in Figure 7.34. The transition point is well respected at 1 kHz, and we have around 10 dB of attenuation at that point. It would have been impossible to reach such an attenuation without disabling the fast lane. The boost is also very close to the target of 130°.

This last description ends our section on the TL431, where we have covered the majority of cases an engineer can face in his design work. Despite a rather low open-loop gain, compared to an op amp, the TL431 lends itself very well to the implementation of compensator once its bias limits are well understood and accounted for in the equations. This is what we have strived to do in the previous lines, showing how the part behaves in the classical type 1, 2, and 3 configurations.

7.15 Testing the Ac Responses on a Bench

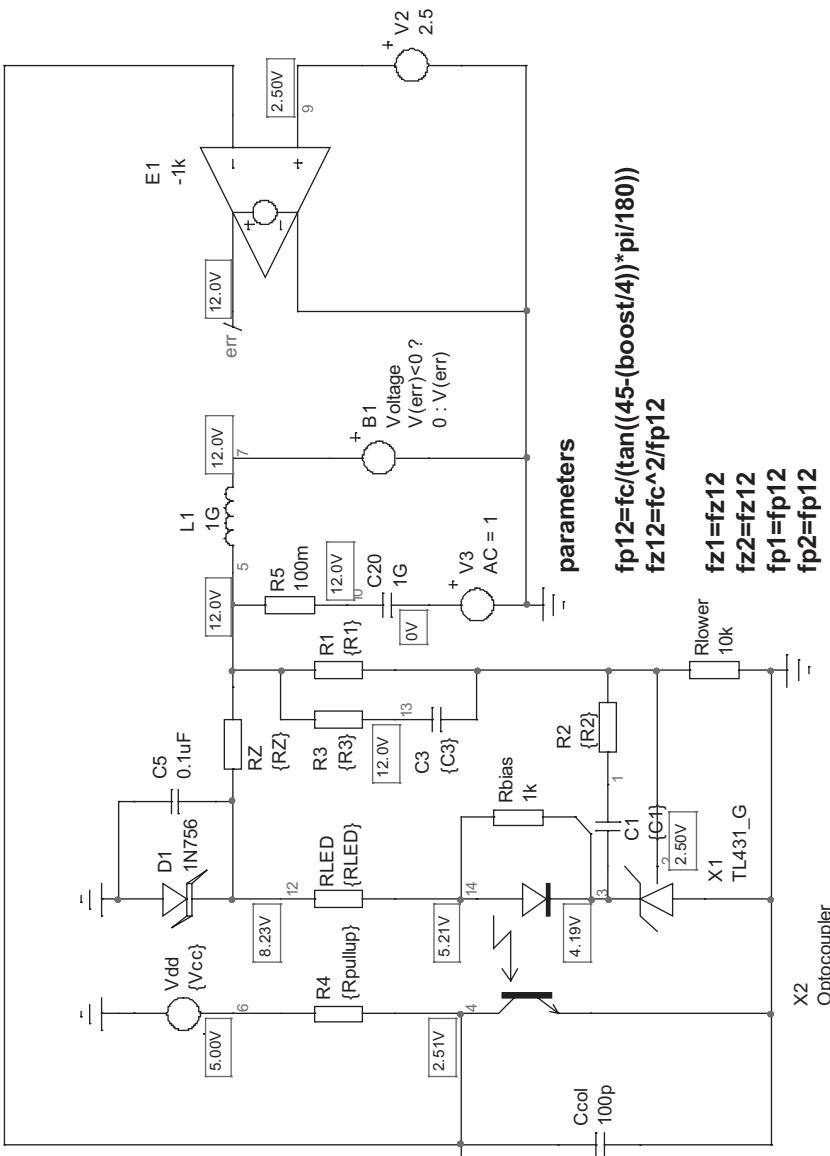
All the ac results that we have presented so far are coming from simulations using a SPICE engine. We know by experience, that reality differs from simulation. To avoid unpleasant surprises, it is a necessity to check on the bench if the assumptions or the hypothesis adopted in a simulation context are validated by practical experiments. To do so, we must find a means to properly bias a TL431-based compensator and ac modulate its input to observe its output. The main difficulty with a high-gain compensator, however, is to maintain the right bias point and prevent the output from running in its upper or lower stops. In our case, we want a collector voltage around 2.5 V, the middle of its dynamic excursion when biased from a 5-V dc source. Assume a TL431 network designed to stabilize a 12-V converter. Even if you carefully adjust a dc power supply biasing the resistive divider network and delivering exactly 12.00 V, there will always be slow temperature drifts and noise that will inexorably push the circuit in its upper or lower stops. Therefore, rather than manually tweaking a dc source, why not automate the biasing process such as we did in our SPICE fixtures? This is exactly what we did in Figure 7.35. A

parameters

$$\begin{aligned}
R_{max} &= ((V_z - V_f - V_{ref}) / (V_{cc} - V_{CEsat} + I_{bias}^*(R_{pullup} * CTR))) * R_{pullup} * CTR \\
R_{LED} &= R_{max} * 0.8 \\
Z_a &= (V_{out} - V_z) * R_{pullup} * CTR \\
Z_b &= (V_{cc} - V_{CEsat}) + (I_{bias} + I_Z) * R_{pullup} * CTR \\
R_z &= Z_a / Z_b
\end{aligned}$$

V_{out}=12

$$\begin{aligned}
R_1 &= (V_{out}-2.5)/250u \\
f_c &= 1k \\
G_{fc} &= 10 \\
boost &= 130 \\
G &= 10^{(-G_{fc}/20)} \\
pi &= 3.14159
\end{aligned}$$



Cpole = Cpto
CIR = CIR

Figure 7.33 When disabling the fast lane, the TL431 lends itself well to the type 3 implementation.

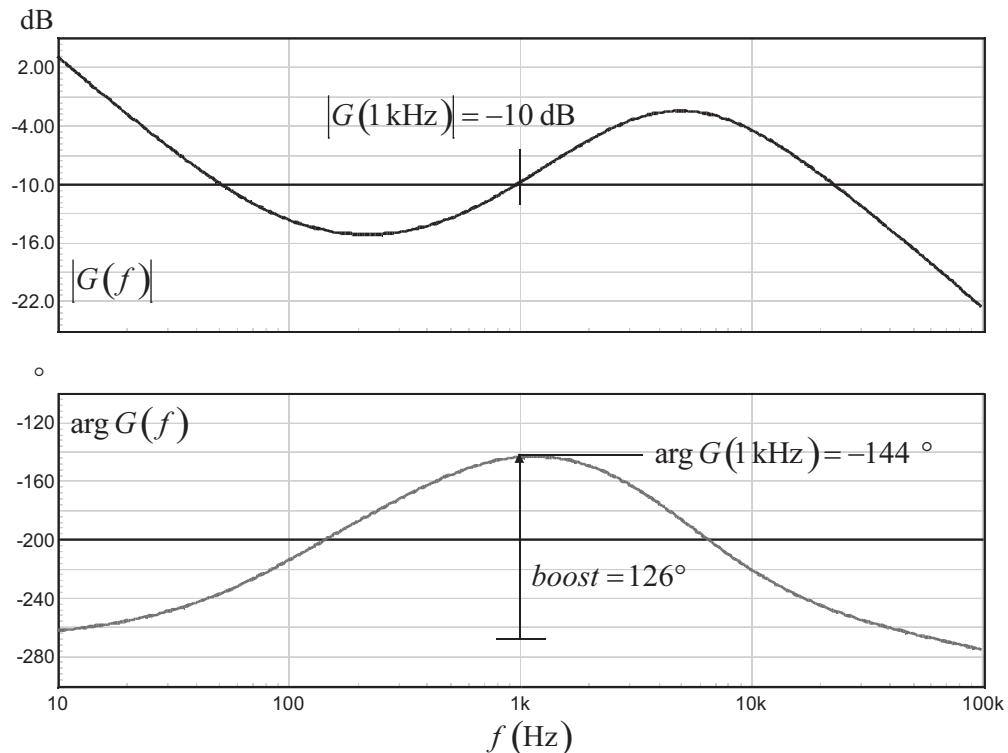


Figure 7.34 The ac results confirm the choices we made. The crossover point at 1 kHz exhibits the right attenuation, and the phase boost is within the specifications.

simple LM358 op amp monitors the optocoupler collector. It adjusts its output so that the collector voltage equals the 2.5-V setpoint present on the op amp inverting input. That way, if a drift occurs or a component is changed, the op amp will automatically adjust its output to keep the collector at the right 2.5-V level. A 1000- μ F

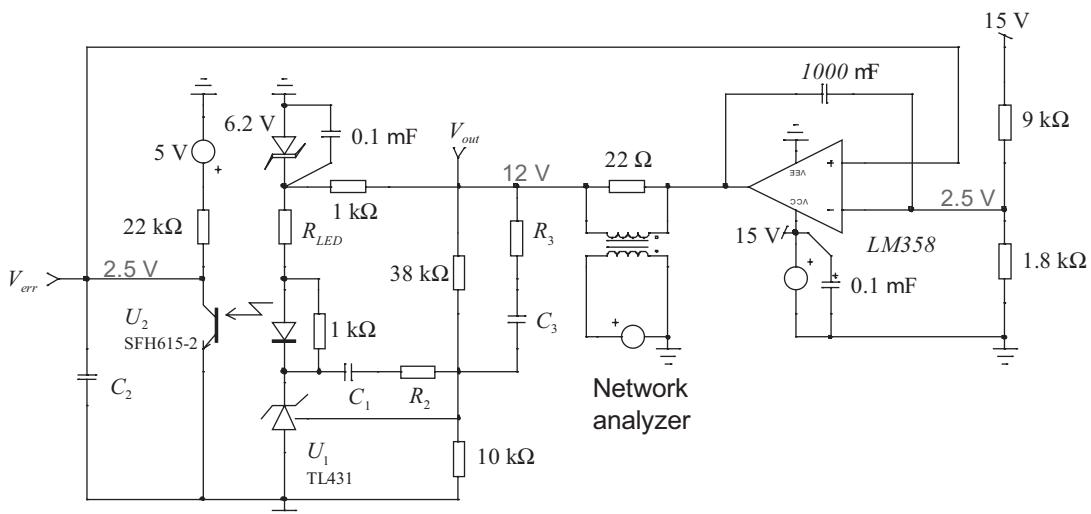


Figure 7.35 Rather than manually fixing the bias point, an op amp does the job automatically by maintaining the right dc voltage on the V_{out} node. R_3 and C_3 are only present for the type 3 study.

capacitor rolls off the loop gain and ensures the stability of the fixture. A network analyzer monitors V_{out} and V_{err} to produce the Bode plot we are looking for.

The first ac results are those of a type 2, and they appear in Figure 7.36. The compensator is designed to cross over at 1 kHz with a 0-dB gain, together with a 50° phase boost. Needless to say, this 0-dB transition would have been impossible to obtain without using the TL431 recommended configuration with the removed fast lane. The shape is in good agreement with the ac results we obtained by simulation.

The test has been carried on a type 3 compensator (see Figure 7.37), where the fast lane has also been disabled. Again, the results are very good, and the boost is up to nearly 120° in this example.

7.16 Isolated Zener-Based Compensator

Using the term compensator for a Zener diode-based design is not really adequate. The Zener diode is not an error amplifier and, besides ensuring a loose regulation, there is not much we can do with it. However, in cheap designs or when a raw dc voltage is good enough, it can be a possible choice. Figure 7.38 portrays the secondary side of a power supply featuring a Zener diode used as a regulator.

The transfer function of this simple arrangement is quite straightforward, capitalizing on what we have derived before:

$$\frac{V_{err}(s)}{V_{out}(s)} = -\text{CTR} \frac{R_{pullup}}{R_{LED}} \frac{1}{1 + sR_{pullup}C_2} = -G_0 \frac{1}{1 + s/\omega_p} \quad (7.161)$$

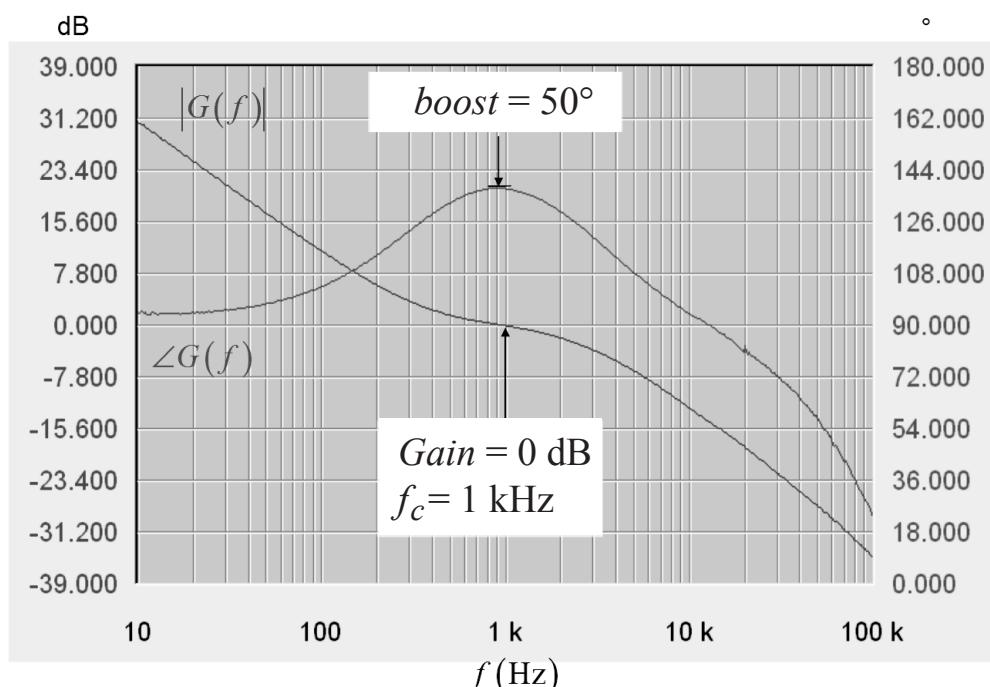
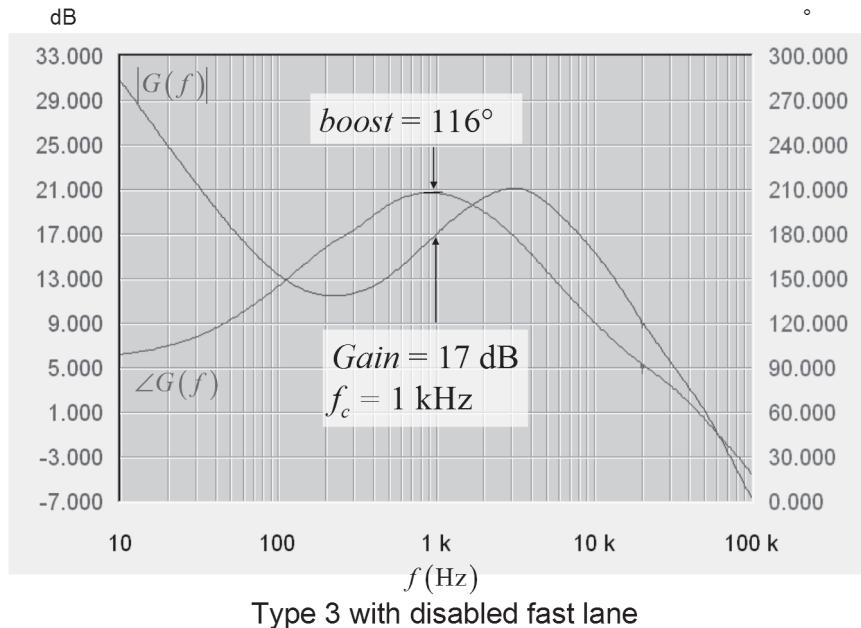


Figure 7.36 The Bode plot extracted with Figure 7.35 fixture confirms the type 2 nature of the tested configuration.



Type 3 with disabled fast lane

Figure 7.37 The ac sweep using the test fixture confirms the behavior of a type 3 compensator.

We have a bit of gain brought by G_0 :

$$G_0 = \text{CTR} \frac{R_{\text{pullup}}}{R_{\text{LED}}} \quad (7.162)$$

and a high-frequency pole:

$$\omega_p = \frac{1}{R_{\text{pullup}} C_2} \quad (7.163)$$

Of course, we could wire a capacitive network across the LED resistor, but with a lack of origin pole imposing a -1 slope, it would produce a bump in the gain curve

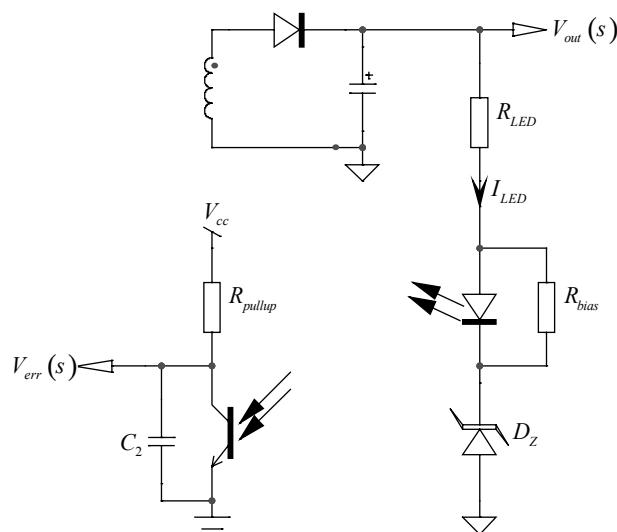


Figure 7.38 The Zener diode requires a sufficient bias current to properly operate.

and not a flat area as with the type 2 kind of curve. This Zener diode-based compensation circuitry does not provide any phase boost. You will thus have to select a crossover frequency on the plant Bode plot where the phase lag is compatible with that brought by the Zener-based network featuring the low-frequency optocoupler pole. The main weaknesses of this approach are the following ones:

1. There is no dc gain as with an op amp or a TL431. The static error can be rather high, and the output impedance of the converter is not very good.
2. The output voltage selection depends on the Zener diode, but also on the LED resistor voltage drop. This drop depends on the error voltage level (the current in the pull-up resistor) and influences the output voltage.
3. You cannot really shape the transfer function; you can only place a high-frequency pole with C_2 and the pull-up resistor.

Despite the remarks, the Zener-based network is popular in low-cost power supplies or when the output voltage precision is not the main design parameter. Actually, as indicated in the second bullet, the output voltage is made of several stacked contributors:

$$V_{out} = V_Z + R_{LED}I_{LED} + V_f \quad (7.164)$$

If V_Z and V_f are constant values, the main offender in the equation is the voltage drop across the LED resistor. This drop is a function of the current circulating in the LED and, thus, in direct relationship to the feedback level. The maximum current value in the LED occurs when the feedback is close to zero—actually the optocoupler saturation voltage. This level is defined by

$$I_{LED,max} = \frac{V_{cc} - V_{CE,sat}}{R_{pullup}CTR_{min}} + I_{bias} \quad (7.165)$$

On the contrary, at maximum power, the feedback voltage is close to V_{cc} , and that is where the LED current is minimum. The variable $V_{CE,max}$ corresponds to the maximum value the feedback voltage can take when the maximum power is asked to the converter:

$$I_{LED,min} = \frac{V_{cc} - V_{CE,max}}{R_{pullup}CTR_{max}} + I_{bias} \quad (7.166)$$

As we can see with these equations, the output voltage will slightly move in relationship to the feedback level. The important design parameter is to select an LED resistor so that its voltage drop remains reasonable compared to the Zener voltage. Otherwise, its contribution will affect V_{out} , and the final precision will seriously suffer. Once the voltage contribution of the LED series resistor is known, we can select the Zener voltage according to (7.164).

7.16.1 A Design Example

The transfer function of the converter we want to stabilize is given in Figure 7.39. On this graph, we can see that the maximum phase lag stays below 90°. Crossing over at 1 kHz requires a 20-dB gain. This is where we will focus our attention.

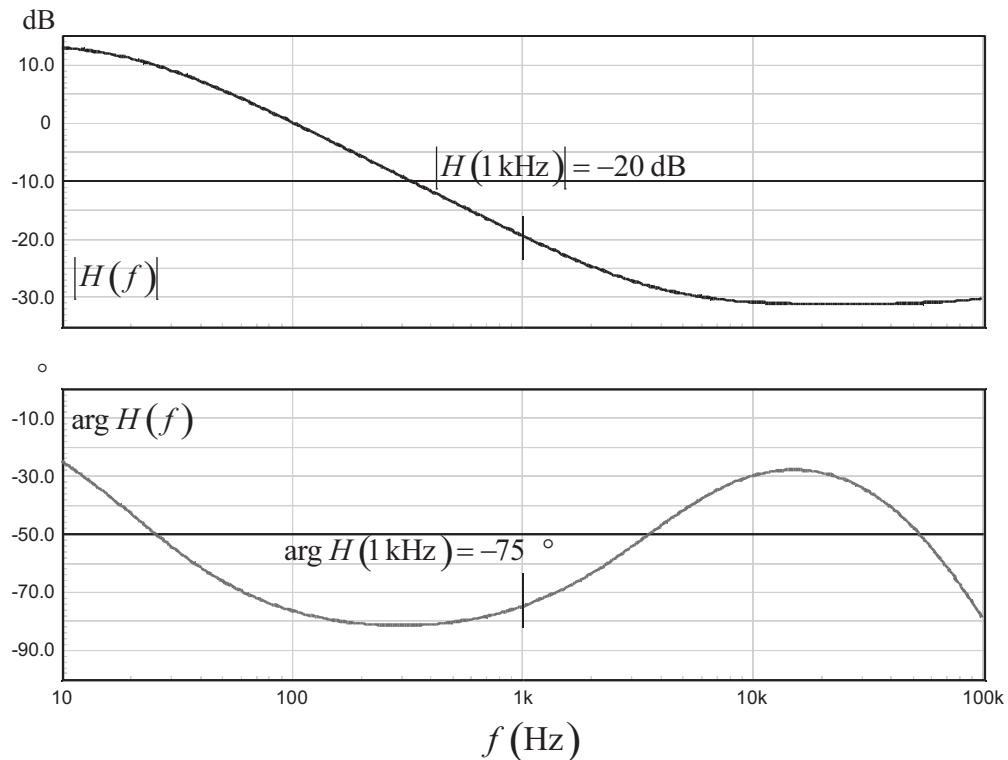


Figure 7.39 The transfer function of the converter $H(s)$ shows a gain deficiency of -20 dB at 1 kHz.

Using (7.162), we can calculate the LED resistor we will install given the following parameters:

$I_{Z_{bias}} = 1$ mA; the Zener diode biasing current.

$V_f = 1$ V; the LED forward voltage.

$V_{CE,sat} = 0.3$ V; the optocoupler saturation voltage.

$V_{CE,max} = 3$ V; the optocoupler voltage at maximum power.

$V_{cc} = 5$ V; the pull-up V_{cc} level.

$V_{out} = 12$ V; the converter output voltage.

$R_{pullup} = 20$ k Ω ; the optocoupler pull-up resistor.

$CTR_{min} = 0.3$; the minimum optocoupler current transfer ratio.

$CTR_{max} = 1.2$; the maximum optocoupler current transfer ratio.

$$R_{LED} = CTR \frac{R_{pullup}}{G_{fc}} = 0.3 \frac{20k}{\frac{20}{10^{20}}} = 600 \Omega \quad (7.167)$$

As explained, the voltage across this LED resistor will affect the output voltage given the current circulating in the optocoupler collector. The variations are calculated using (7.165) and (7.166):

$$\begin{aligned}
V_{R_{LED,\max}} &= R_{LED} I_{LED,\max} = R_{LED} \left(\frac{V_{cc} - V_{CE,sat}}{R_{pullup} \text{CTR}_{\min}} + I_{bias} \right) \\
&= 600 \times \left(\frac{5 - 0.3}{20k \times 0.3} + 1m \right) = 1.07 \text{ V}
\end{aligned} \tag{7.168}$$

$$\begin{aligned}
V_{R_{LED,\min}} &= R_{LED} I_{LED,\min} = R_{LED} \left(\frac{V_{cc} - V_{CE,\max}}{R_{pullup} \text{CTR}_{\max}} + I_{bias} \right) \\
&= 600 \times \left(\frac{5 - 3}{20k \times 1.2} + 1m \right) = 650 \text{ mV}
\end{aligned} \tag{7.169}$$

On average, the voltage variation across R_{LED} is around 860 mV. Considering a rather constant 1 V drop across the optocoupler LED, we can calculate the Zener voltage to get a 12 V output:

$$V_Z = V_{out} - V_f - V_{R_{LED,avg}} = 12 - 1 - 0.86 \approx 10 \text{ V} \tag{7.170}$$

A 10-V Zener diode thus seems to be the right choice. In case the Zener voltage is not available, you still have the ability to slightly tweak the LED series resistance to match the wanted output voltage given the closest Zener voltage you have found. The test fixture appears in Figure 7.40 and confirms the right operating bias points. We are close to our 12-V target.

For noise reasons, we have placed a pole at 5 kHz so that a small capacitor can be placed across the optocoupler, close to the controller pins:

$$C_2 = \frac{1}{2\pi f_p R_{pullup}} = \frac{1}{6.28 \times 5k \times 20k} = 1.6 \text{ nF} \tag{7.171}$$

We know that the total capacitor connected across the optocoupler that forms C_2 is actually made of the optocoupler parasitic pole C_{opto} and the added capacitor C_{col} . The optocoupler pole is located at 6 kHz. Given a pull-up resistance of 20 k Ω , we can calculate its parasitic contribution:

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} = \frac{1}{6.28 \times 6k \times 20k} \approx 1.3 \text{ nF} \tag{7.172}$$

Subtracted from the C_2 value, we obtain the capacitor we need to install across the optocoupler:

$$C_{col} = C_2 - C_{opto} = 1.6n - 1.3n = 300 \text{ pF} \tag{7.173}$$

The ac response can be now tested by observing the V_{err} node. The answer appears in Figure 7.41. The slight 2-dB discrepancy in the gain can be explained by the LED dynamic resistor cumulated with that of the Zener diode itself. It can obviously be compensated, if necessary, by increasing the gain target in (7.167). If we combine both the Figure 7.39 and Figure 7.41 transfer functions, we can unveil the complete open-loop gain $T(s)$ in Figure 7.42. The open-loop dc gain is obviously

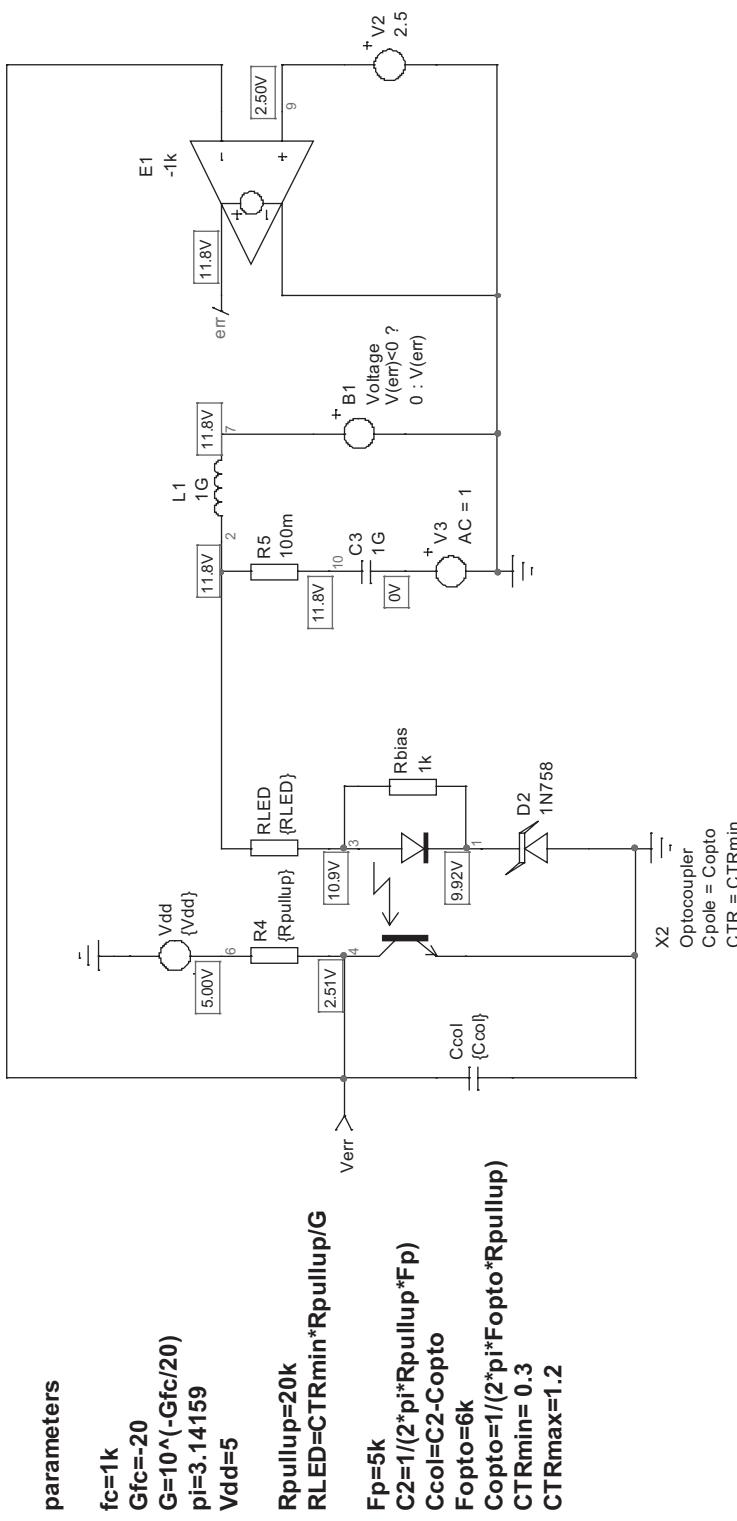


Figure 7.40 The Zener-based test fixture delivers the output voltage close to the target of 12 V.

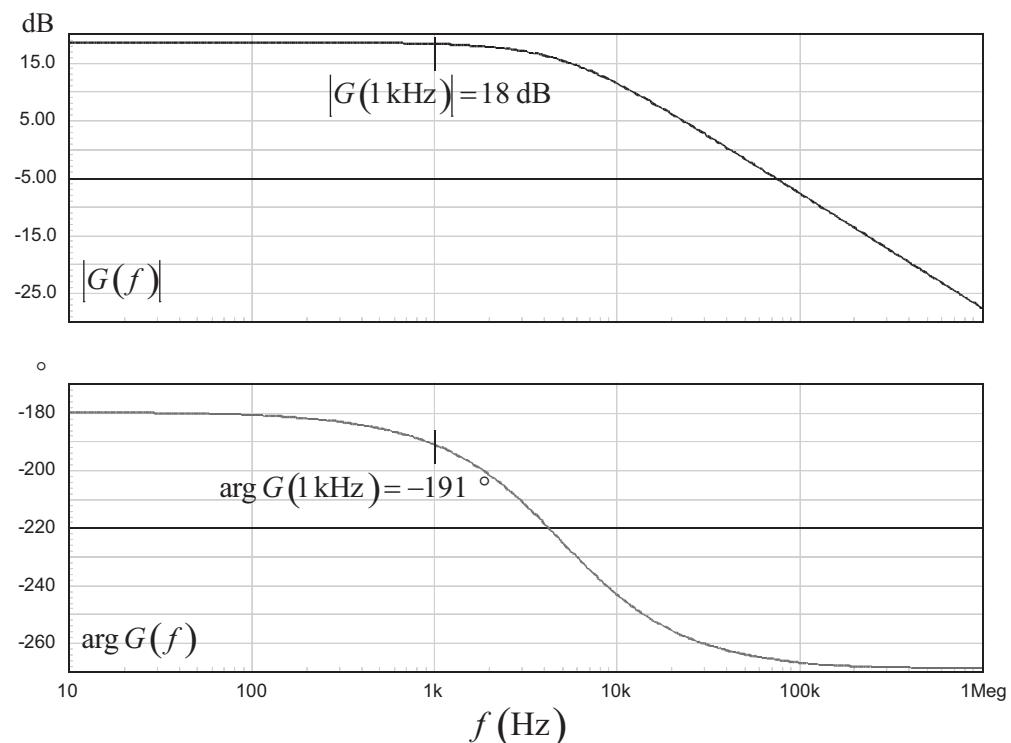


Figure 7.41 The ac response of the Zener-based network. No surprise, there is no origin pole . . .

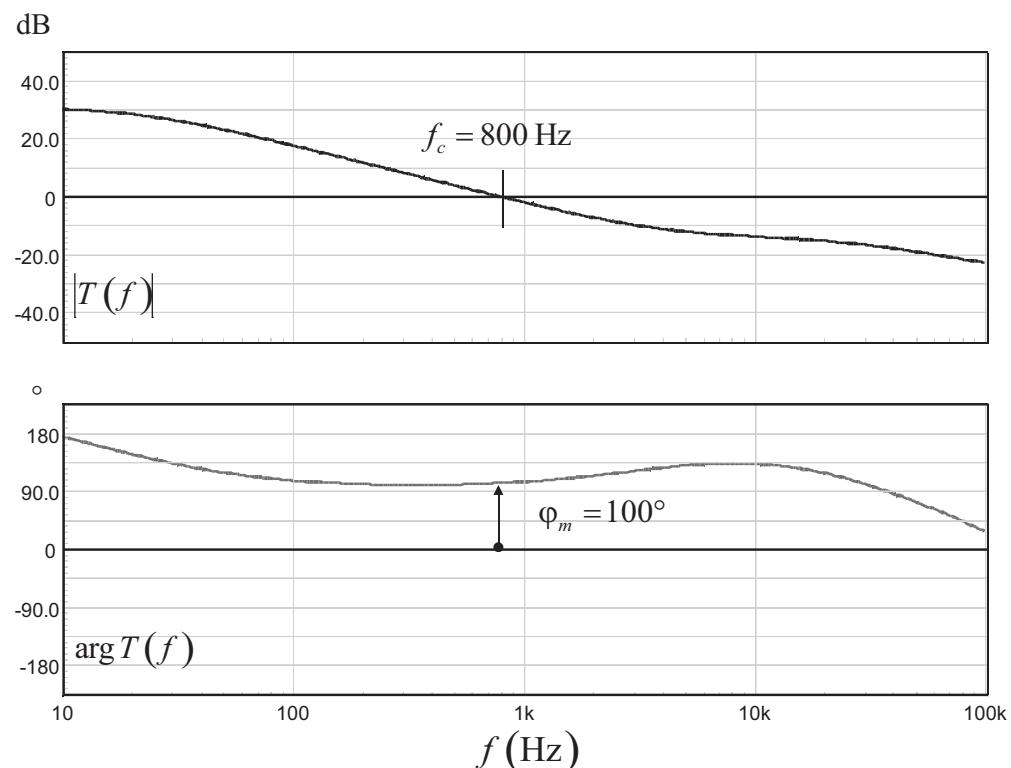


Figure 7.42 The loop gain shows a weak gain, but the phase margin is comfortable.

weak given the lack of origin pole. Owing to the missing 2 dB, we do not crossover at 1 kHz but at 800 Hz. The phase margin is comfortable with a 100° value.

Needless to say, the Zener diode dynamic impedance cannot be simulated with great accuracy, as inducing gain changes when going to the lab. However, experience shows that this first analytical debugging is helpful to figure out an LED series resistor value to wire on the prototype rather than pulling one out of thin air.

7.17 Nonisolated Zener-Based Compensator

In the case of nonisolated converter designs, the isolation barrier brought by the optocoupler is not necessary. Therefore, the implementation of the Zener-based circuitry slightly changes as indicated by Figure 7.43.

Rather than driving a single transistor, we used a current mirror made of two bipolar transistors. If the devices are well matched, the collector current circulating in the pull-up resistor is the same as the one circulating in the LED resistor. We are close to an optocoupler operation with a CTR of 1. The difference might lie in the h_{11} input parameter of transistor Q_1 base-emitter junction that appears in series with the Zener diode. If we neglect it and consider well-paired transistors, the gain is simply

$$\frac{V_{err}(s)}{V_{out}(s)} = -\frac{R_{pullup}}{R_{LED}} \quad (7.174)$$

The output voltage is then obtained by stacking up the various voltage drops:

$$V_{out} = V_Z + R_{LED}I_{LED} + V_{BE} \quad (7.175)$$

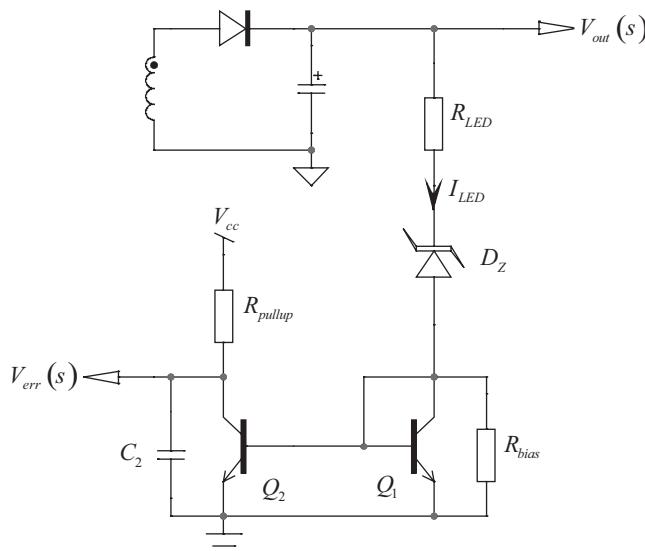


Figure 7.43 With the lack of an optocoupler, a current mirror is used to drive the feedback pin to ground.

The LED current is made of the feedback current plus the dc current imposed by the bias resistor, R_{bias} , placed across the base-emitter junction of Q_1 . A V_{BE} of ≈ 650 mV can be considered for the design procedure at room temperature. The variation of this level is around -2 mV/ $^{\circ}\text{C}$.

$$I_{LED} = \frac{V_{cc} - V_{CE}}{R_{pullup}} + \frac{V_{BE}}{R_{bias}} \quad (7.176)$$

To limit the dc drifts, make sure the transistors are well paired and share the same junction temperature. To that respect, we recommend the usage of dual transistors such as the BC846BDW1T1G from ON Semiconductor. As these devices are manufactured from the same wafer and share a common leadframe, the thermal

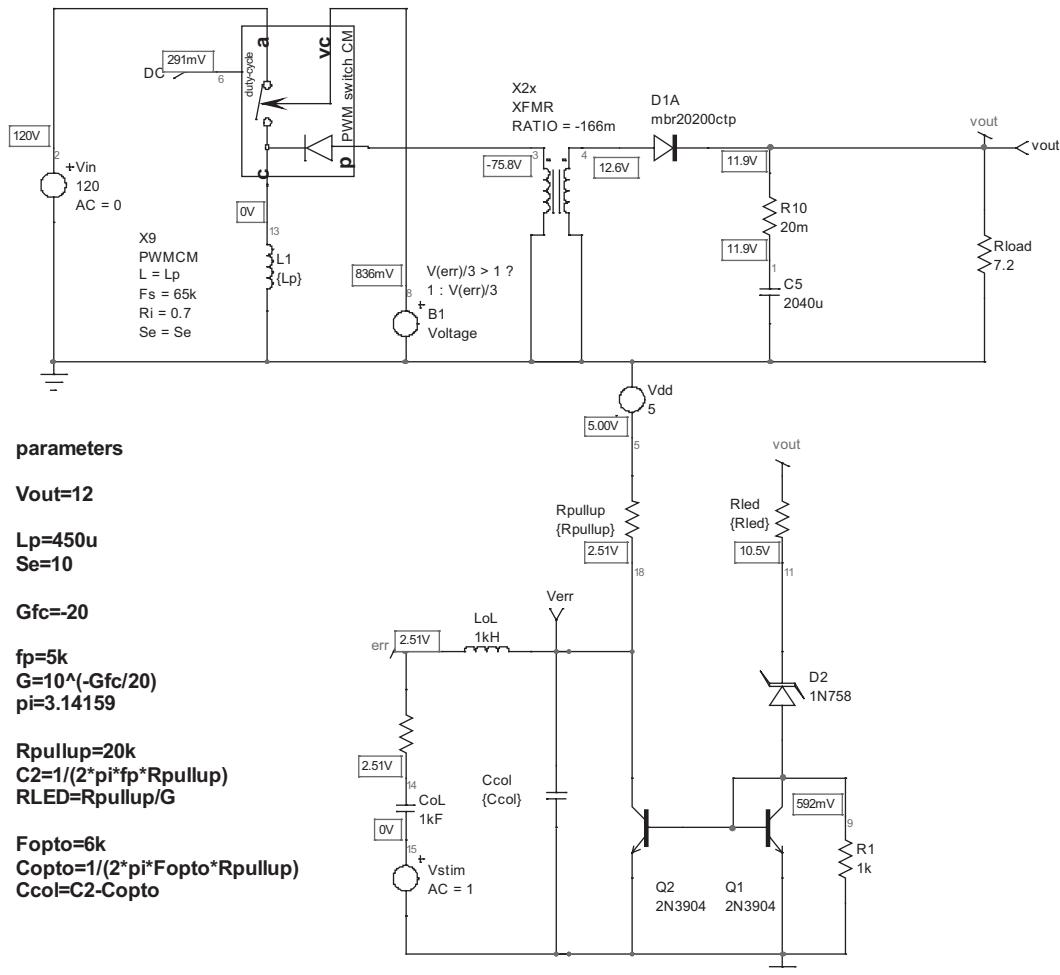


Figure 7.44 Design example with a nonisolated compensator featuring a Zener diode and a current mirror.

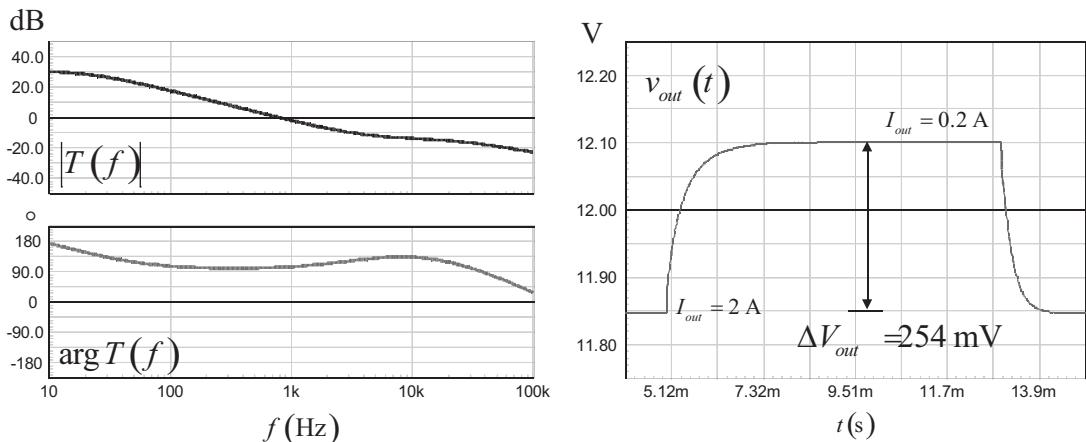


Figure 7.45 The ac and transient responses are not that ridiculous for such a simple compensator! The current is stepped from 2 A to 200 mA in 10 μ s.

performance will be improved as their junction temperature (and thus their V_{BE} forward drops) will drift together. The dc output voltage precision depends on the V_{BE} contribution to the whole chain. Implementing this nonisolated technique where the V_{BE} contributes to a maximum of 10 percent of the dc output is a reasonable tradeoff. For instance, a 650-mV V_{BE} with a 12 V output is acceptable (5.4 percent). On the contrary, adopting this configuration for a 3.3 V output makes no sense at all. The design procedure is the same as the one described for the isolated version.

An application example appears in Figure 7.44 and shows good operating bias points. Despite its simplicity, the circuit works well and, as testified by Figure 7.45, the transient response is acceptable. Please note the square response to an output step, typical of a purely resistive output impedance brought by the lack of origin pole in the compensator transfer function.

7.18 Nonisolated Zener-Based Compensator: A Lower Cost Version

Before closing this section on Zener-based compensators, it is interesting to note the existence of an even cheaper compensator, based on a single bipolar transistor. Disclosed to me by Mr. Louvel, it appears in Figure 7.46 and combines a bipolar transistor with a Zener diode. Used in high-volume low-cost consumer applications, it offers a rather well temperature-compensated error amplifier. The Zener diode voltage is augmented by the series diode D1 forward drop, and it biases the emitter to $V_Z + V_f$. If we assume the V_{BE} of Q_1 to be around the same value of D_1 voltage drop V_f , then the voltage across R_{lower} is roughly that of D_Z . When the voltage on Q_1 base changes, it either forward biases Q_1 (it V_{out} decreases) and V_{err} increases, or it blocks it when V_{out} increases and V_{err} goes down. Based on this observation, the calculation of the elements is rather straightforward. R_Z must provide the

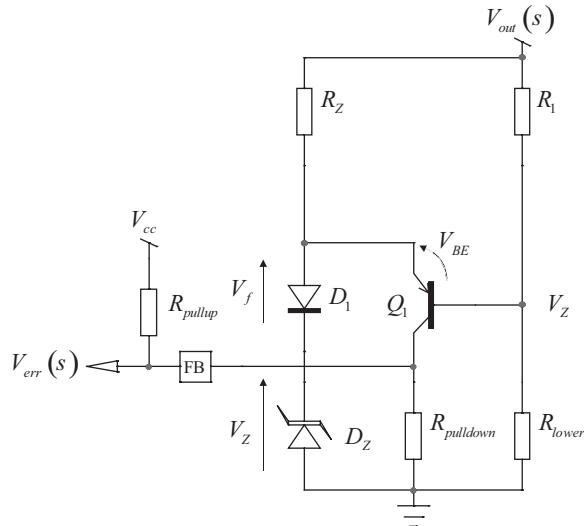


Figure 7.46 Based on a single bipolar transistor, this compensator allows cheap weighted compensation if necessary.

biasing current for the Zener diode but also the current to develop the error voltage across $R_{pulldown}$:

$$R_Z \leq \frac{V_{out} - V_f - V_z}{I_{Zbias} + \frac{V_{err,max}}{R_{pulldown}}} \quad (7.177)$$

The divider network is calculated assuming V_Z appears across R_{lower} :

$$R_{lower} = \frac{V_Z}{I_{bridge}} \quad (7.178)$$

$$R_1 = \frac{V_{out} - V_Z}{I_{bridge}} \quad (7.179)$$

We recommend a bias current for the bridge to be at least $500 \mu\text{A}$ given the bipolar transistor base current. Regarding the Zener diode, a voltage of 6.2 V looks like a good choice, as it is the most stable value over temperature. A bias current for this device around $1\text{--}2 \text{ mA}$ can be accepted.

Please note that this circuitry can only be coupled to a feedback input featuring a pull-up resistor, as in Figure 7.46. At startup, as V_{out} does not yet exist, there can be no voltage across $R_{pulldown}$. If no internal source biases the feedback pin to ask for power, the converter won't start. A controller like a NCP1200 can be a good candidate for this cheap compensator.

7.19 Conclusion

The TL431 is one of the most popular components used in the consumer field. Cheap and easy to bias, you must understand how it works before you can get the best of it. You must read the first section of this article to realize that the designer who thought of this self-contained op amp and reference voltage was a genius! The presence of the fast lane can be used as an advantage, making a type 2 compensator look quite simple at the end. Linked to an optocoupler, you realize that closing a loop with that device has never been that simple.

References

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Appendix 7A: Summary Pictures

Figures 7.47 through 7.51 summarize the component definitions associated with the structures described in the chapter.

Isolated type 1

1 origin pole

$$R_{LED,max} = \frac{(V_{out} - V_f - V_{TL431,min}) R_{pullup} CTR_{min}}{V_{cc} - V_{CE,sat} + I_{bias} CTR_{min} R_{pullup}}$$

$$C_1 = \frac{R_{pullup} CTR}{R_{LED} R_l 2\pi f_{po}}$$

$$C_2 = \frac{R_l C_1}{R_{pullup}}$$

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pulldown}}$$

$$C_{col} = C_2 - C_{opto}$$

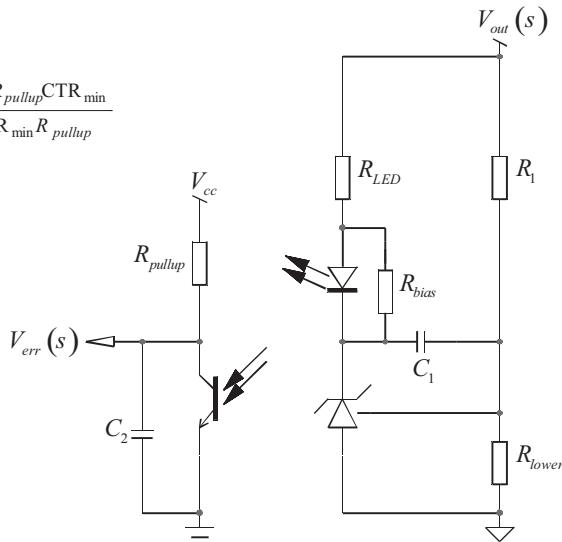


Figure 7.47 The isolated type 1.

Isolated type 2 – fast lane

1 origin pole

1 pole f_p 1 zero f_z

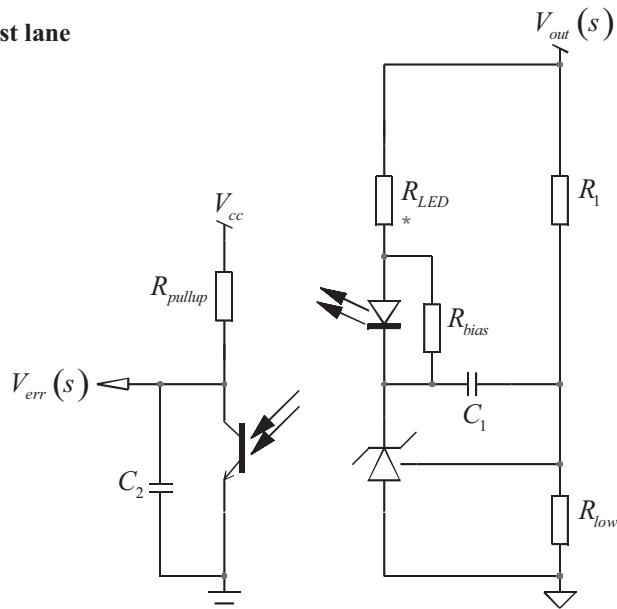
$$R_{LED} = \frac{R_{pullup} \text{CTR}}{G}$$

$$C_1 = \frac{1}{2\pi f_z R_1}$$

$$C_2 = \frac{1}{2\pi R_{pullup} f_p}$$

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pulldown}}$$

$$C_{col} = C_2 - C_{opto}$$



* Check max value

Figure 7.48 The isolated type 2 with fast lane.**Isolated type 2 – no fast lane**

1 origin pole

1 pole f_p 1 zero f_z

$$R_{LED,max} = \frac{(V_Z - V_f - V_{TL431,min}) R_{pullup} \text{CTR}_{min}}{V_{ccp} - V_{CE,sat} + I_{bias} \text{CTR}_{min} R_{pullup}}$$

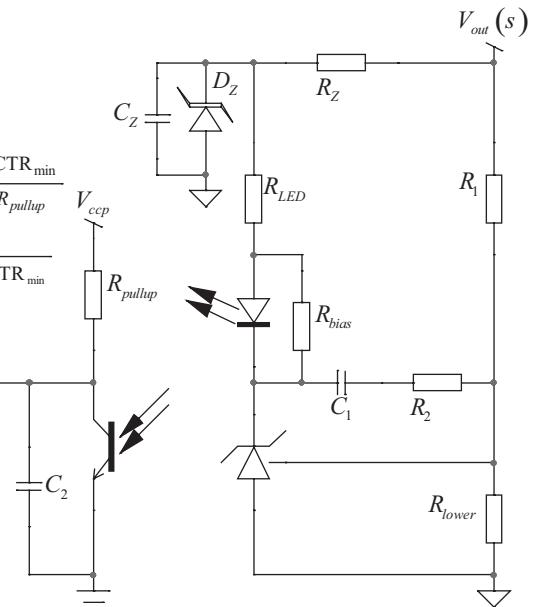
$$R_Z = \frac{(V_{out} - V_Z) R_{pullup} \text{CTR}_{min}}{(V_{cc} - V_{CE,sat}) + (I_{Zbias} + I_{bias}) R_{pullup} \text{CTR}_{min}}$$

$$G_1 = \text{CTR} \frac{R_{pullup}}{R_{LED}} \quad G_2 = 10^{\frac{G-G_1}{20}}$$

$$R_2 = G_2 R_1$$

$$C_1 = \frac{1}{2\pi f_z R_2} \quad C_2 = \frac{1}{2\pi R_{pullup} f_p}$$

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} \quad C_{col} = C_2 - C_{opto}$$

**Figure 7.49** The isolated type 2 without fast lane.

Isolated type 3 – fast lane

1 origin pole

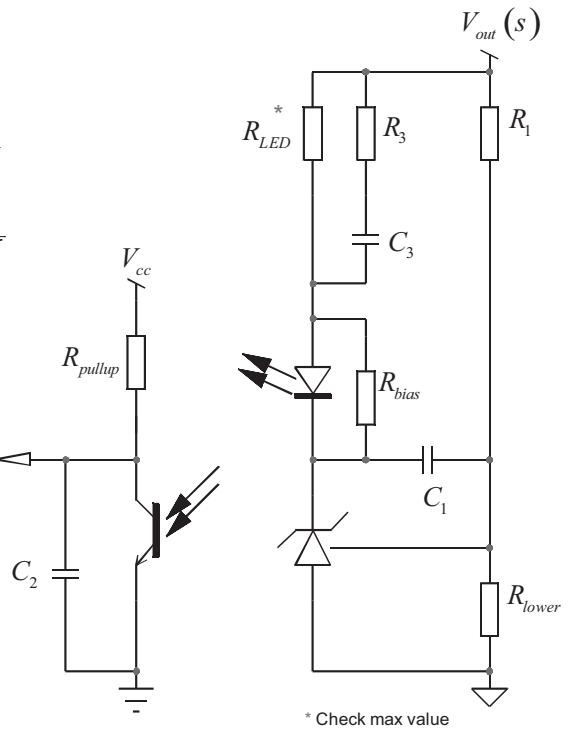
2 poles f_{p1}, f_{p2} 2 zeros f_{z1}, f_{z2}

$$R_{LED} = \frac{R_{pullup}}{G} \text{CTR} \frac{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}$$

$$C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_{LED} f_{p_2} f_{z_2}} \quad R_3 = \frac{f_{z_2} R_{LED}}{f_{p_2} - f_{z_2}}$$

$$C_1 = \frac{1}{2\pi f_{z_1} R_1} \quad C_2 = \frac{1}{2\pi R_{pullup} f_{p_2}}$$

$$C_{opto} = \frac{1}{2\pi f_{opto} R_{pullup}} \quad C_{col} = C_2 - C_{opto}$$

**Figure 7.50** The isolated type 3 with fast lane.**Isolated type 3 – no fast lane**

1 origin pole

2 poles f_{p1}, f_{p2} 2 zeros f_{z1}, f_{z2}

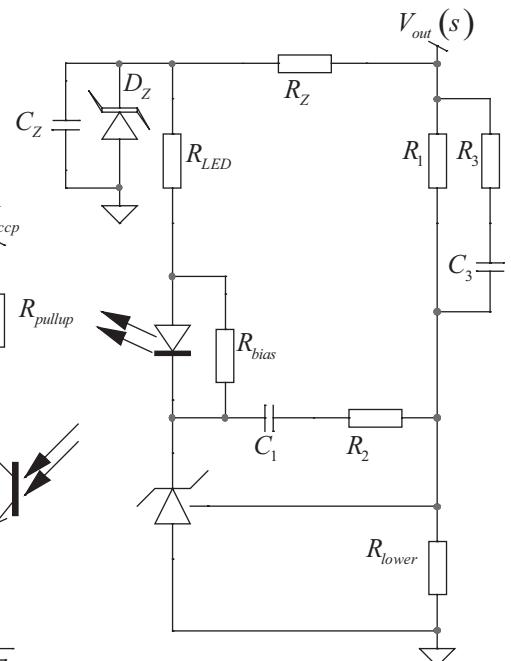
$$R_{LED,max} \leq \frac{(V_Z - V_f - V_{TL431,min}) R_{pullup} \text{CTR}_{min}}{V_{cc} - V_{CE,sat} + I_{bias} \text{CTR}_{min} R_{pullup}}$$

$$R_2 = \frac{GR_1 R_{LED}}{R_{pullup} \text{CTR}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}}{\sqrt{1 + \left(\frac{f_{z_1}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_2}}\right)^2}}$$

$$R_3 = \frac{R_1 f_{z_2}}{f_{p_2} - f_{z_2}} \quad C_1 = \frac{1}{2\pi f_{z_1} R_2} \quad V_{err}(s)$$

$$C_2 = \frac{1}{2\pi f_{p_2} R_{pullup}} \quad C_3 = \frac{f_{p_2} - f_{z_2}}{2\pi R_1 f_{p_2} f_{z_2}}$$

$$R_Z \leq \frac{(V_{out} - V_Z) R_{pullup} \text{CTR}_{min}}{(V_{cc} - V_{CE,sat}) + (I_{Zhias} + I_{bias}) R_{pullup} \text{CTR}_{min}}$$

**Figure 7.51** The isolated type 3 without fast lane.

Appendix 7B: Second Stage LC Filter

In all TL431-based compensation designs we have presented so far, there was no mention of a second-stage *LC* filter. As shown in Figure 7.52, this network is often included in flyback converters to filter out unwanted noise present on the output. As you can imagine, if the filter cutoff frequency is wrongly positioned, it can affect the loop response and degrade the stability margins.

In this chapter, we have shown how to isolate the TL431-based compensator and design it separately from the power stage: whether you use it in a flyback converter, a buck converter, or a boost converter, the equations set remains the same. Unfortunately, it is not possible to isolate a TL431-based compensator equipped with the post *LC* filter from the power stage it is attached to. The reason is that the insertion of the *LC* filter between the load and the power stage modifies the impedances you considered when extracting the converter small-signal model.

A simplified large-signal representation of a DCM fixed-frequency flyback converter appears in Figure 7.53. To calculate the open-loop transfer function, you first need to linearize the current source expression I_{out} . Then, the small-signal output voltage across C_1 is obtained by multiplying \hat{i}_{out} with the equivalent impedance seen by the current source. As the *LC* filter is inserted, you can see how the circuit complicates since the inductor introduces a second-order network in the output path. However, if the series inductor impedance below the crossover frequency is much smaller than Z_1 and Z_2 impedances, then we can consider that the flyback power stage transfer function does not significantly change. This is the case when the added inductance is below $15 \mu\text{H}$ [1]. Choosing a low-value inductance makes sense from an efficiency point of view, as low-inductance magnetic components feature weak ESR values and remain small-size devices. Typical values used in flyback converters are up to a few micro-henries maximum.

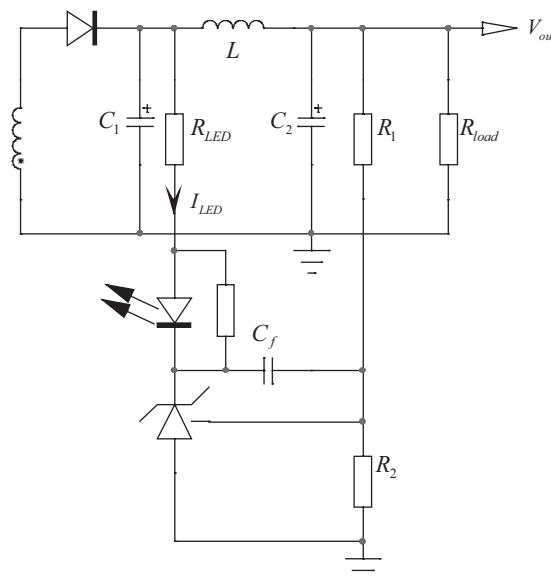


Figure 7.52 An *LC* filter is often inserted at the flyback converter output to filter out unwanted spikes.

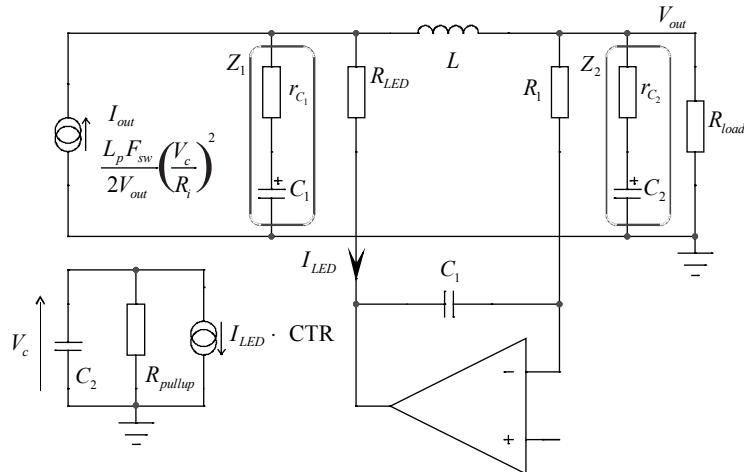


Figure 7.53 The inserted LC network modifies the impedance seen by the considered power stage. Here, we have a simplified large-signal DCM current-mode flyback converter.

A Simplified Approach

We can try, however, to gain insight by considering only the TL431-based transfer function, neglecting the converter loading changes brought by inserting the inductor L . The new equivalent schematic appears in Figure 7.54.

$H(s)$ lumps the LC filter effects loaded by the resistor R_{load} , damped by output capacitor ESR presence. We neglected the inductor dc losses for simplicity. The filter obeys the following equation:

$$H(s) = \frac{1}{1 + \left(\frac{s}{Q\omega_0} \right) + \left(\frac{s}{\omega_0} \right)^2} \quad (7.180)$$

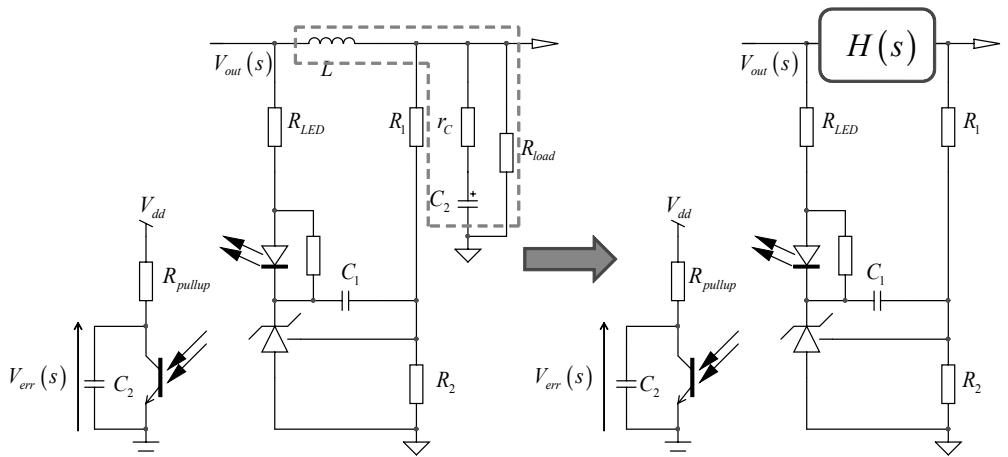


Figure 7.54 If we neglect the loading condition change on the power stage, we can extract the TL431 compensator featuring a post LC filter.

The denominator is that of the buck converter output impedance we have already derived in Chapter 4. Owing to its low entropy form, we can put r_L to zero and immediately get the definitions we need:

$$\omega_0 = \frac{1}{\sqrt{LC_2}} \sqrt{\frac{R_{load}}{r_C + R_{load}}} \quad (7.181)$$

$$Q = \frac{LC_2\omega_0(r_C + R_{load})}{L + C_2(r_c R_{load})} \quad (7.182)$$

If you follow the guidelines detailed in this chapter, you should be able to express the transfer function between V_{err} and V_{out} as follows:

$$\begin{aligned} \frac{V_{err}(s)}{V_{out}(s)} &= -\frac{CTR \cdot R_{pullup}}{R_{LED}} \frac{\left(\frac{H(s)}{sR_l G} + 1 \right)}{1 + sR_{pullup}C_2} \\ &= -\frac{CTR \cdot R_{pullup}}{R_{LED}} \frac{1 + \left(\frac{s}{Q\omega_0} \right) + \left(\frac{s}{\omega_0} \right)^2 + \frac{1}{sR_l G}}{(1 + sR_{pullup}C_2) \left(1 + \left(\frac{s}{Q\omega_0} \right) + \left(\frac{s}{\omega_0} \right)^2 \right)} \end{aligned} \quad (7.183)$$

The transfer function is that of the traditional type 2 architecture to which a double pole and a double zero have been added. To check the effects of these extra terms, we have set up an automated simulation template of a type 2 compensator featuring the output filter. It is given in Figure 7.55. In this template, the inductor value is fixed at $2.2 \mu H$, and C_2 is adjusted to modify the cutoff frequency. The ESR value is calculated so that the product r_C by C_2 is roughly equal to $70 \mu s$, a rule of thumb that can help approximate the ESR value for a standard electrolytic capacitor.

In this compensator, the mid-band gain is set to 20 dB, and the phase boost peaks at 1 kHz. The integrator zero is located at 226 Hz, while the second pole is placed at 5.6 kHz. We have moved the resonant frequency from 10 kHz down to 100 Hz. The results are collected in Figure 7.56 ac plot. The LC network introduces a glitch in the magnitude at the resonant frequency. This glitch is acceptable as long as the resonant frequency occurs in a frequency region where the integrator path through the op amp and C_1 (Figure 7.54) has no gain, as pointed out in [2]: intuitively, the LC filter contribution has more difficulty altering the ac LED current if the integrator attenuation weakens the resonance effects. However, as the resonance approaches the region where the zero is located, the transfer function becomes distorted and the phase goes out of control (500 Hz and 100 Hz).

Simulation at Work

Figure 7.57 shows a 19-V/4-A current-mode flyback converter equipped with the LC filter. The crossover frequency is set to 5 kHz with 70° phase margin. The zero is posi-

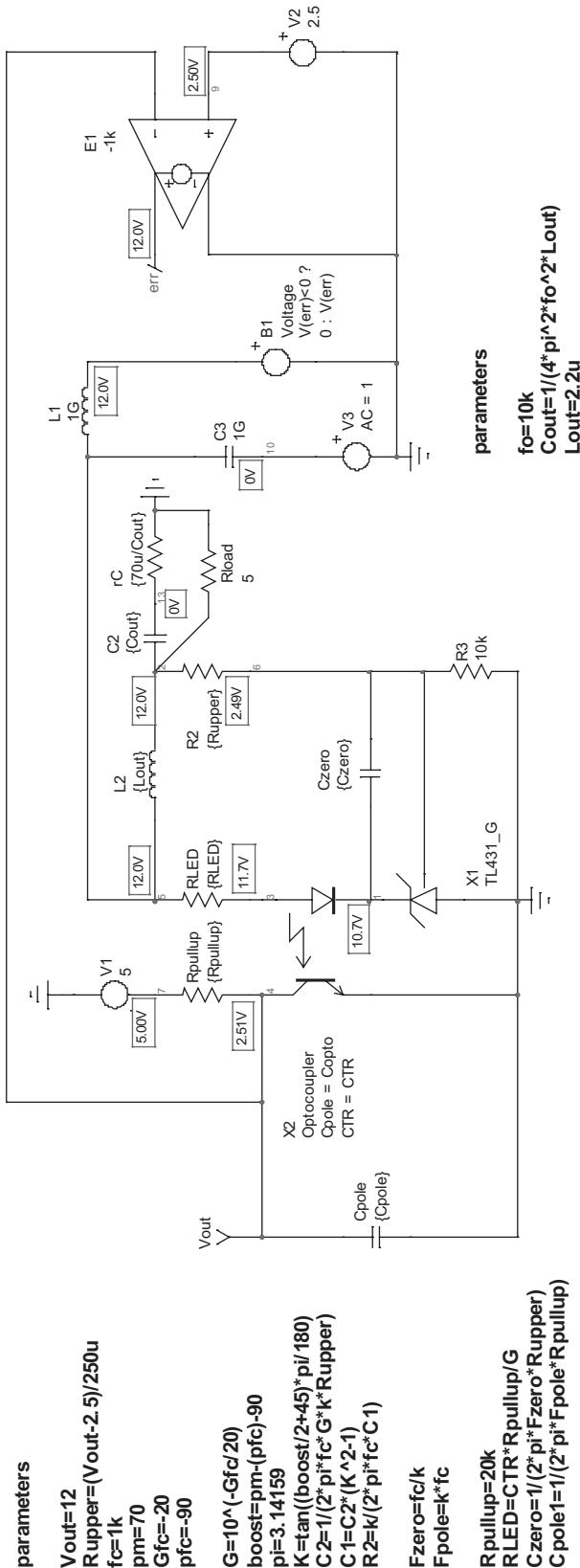


Figure 7.55 An automated type 2 compensator helps us to immediately see the effect of the LC network on the transfer function.

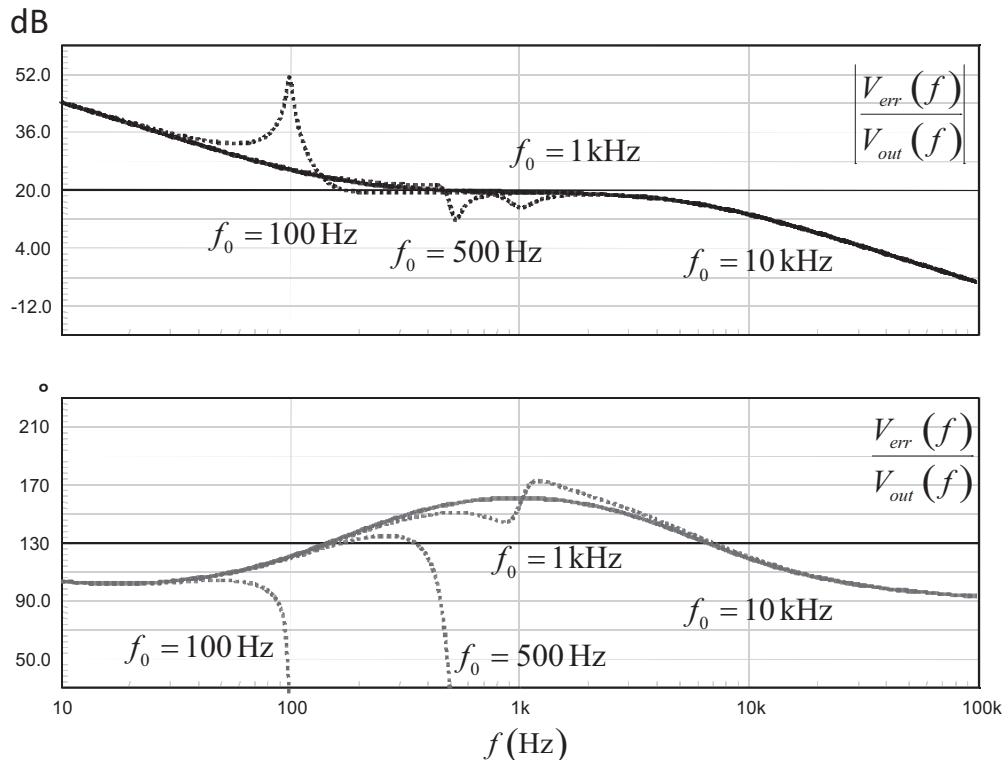


Figure 7.56 This ac plot shows the impact of the post *LC* filter resonant frequency on the TL431-based transfer function.

tioned at 800 Hz. With a fixed inductor value, the second capacitor C_2 is again automatically calculated to create a resonance at the selected frequency point. The ac results are given in Figure 7.58. The loop gain with a $2.2\text{-}\mu\text{H}/115\text{-}\mu\text{F}$ network ($f_0 = 10 \text{ kHz}$) has no impact on the overall shape. When the resonant frequency is tuned to 5 kHz ($L = 4.7 \mu\text{H}$ and $C_2 = 215 \mu\text{F}$), there is still no change of the loop response. Now, when the inductor is increased to $15 \mu\text{H}$ and C_2 to 1.7 mF , the cutoff frequency approaches the zero position and both gain and phase become out of control: the converter is unstable.

As a design recommendation, keep the *LC* network resonance frequency far away from the low-frequency zero location. Around a decade represents a good fit. As observed in the example where the zero seats at 800 Hz, the 10-kHz cutoff frequency does not change the overall response and will offer a good attenuation of the 65-kHz switching frequency ripple. Regarding the inductor value, keep in mind that its addition brings an extra annoying voltage undershoot in presence of sharp output current discontinuities. Values from 1 to $4.7 \mu\text{H}$ are usually observed in ac-dc adapters up to 100 W of output power.

As a final remark, when you install a *LC* filter, make sure the TL431 fast lane connection occurs before the network. You can see in Figure 7.55 that the upper terminal of R_{LED} connects before the inductor and not after. If you connect the resistor directly to the output, the LED current will have direct exposure to the phase and amplitude signals affected by the *LC* network and stability may suffer.

Loop measurements with the *LC* network require that you run multiple measurements in both lanes and vector-combine the data to reconstruct the overall loop

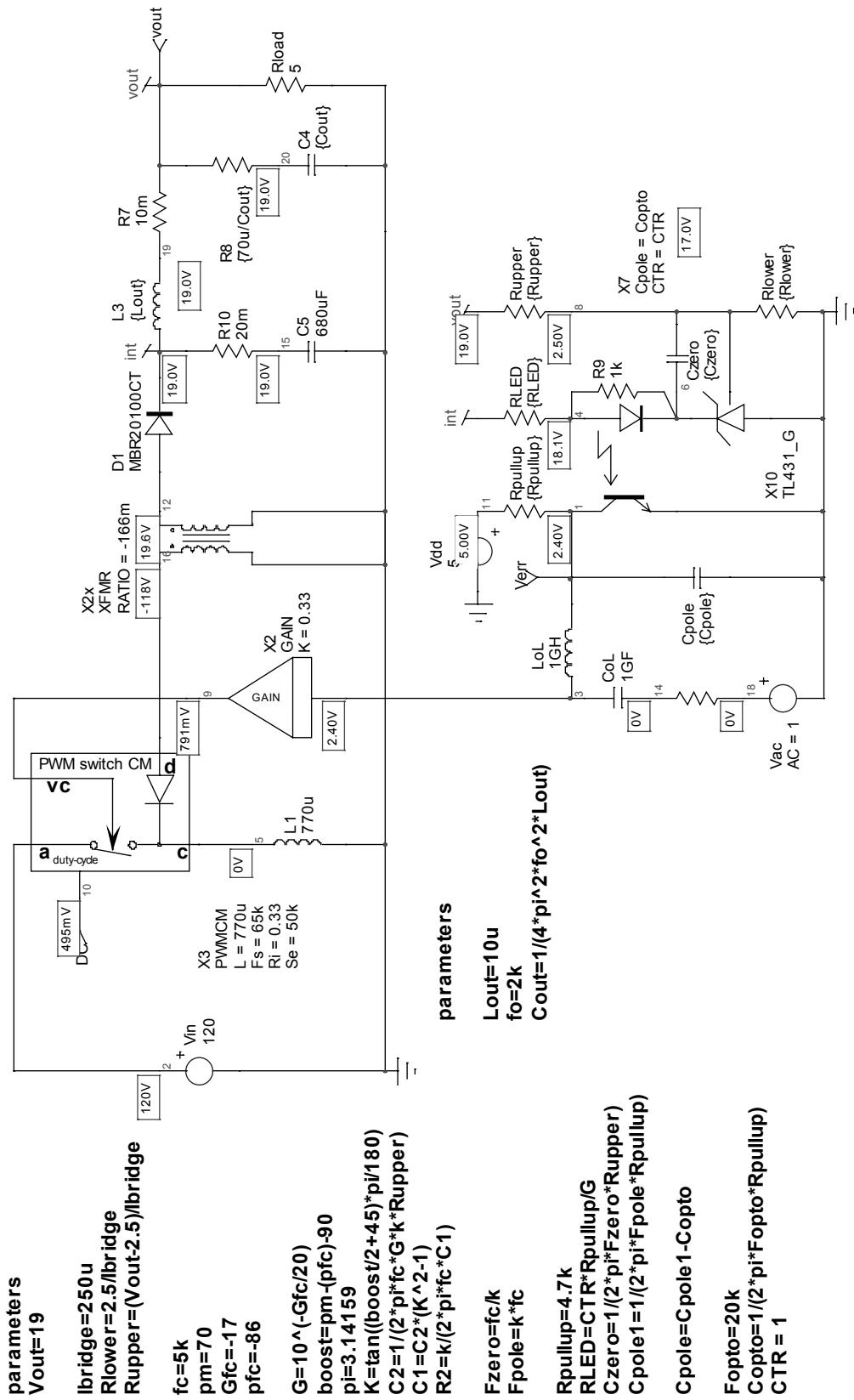


Figure 7.57 A SPICE simulation helps to understand the LC network impact at crossover.

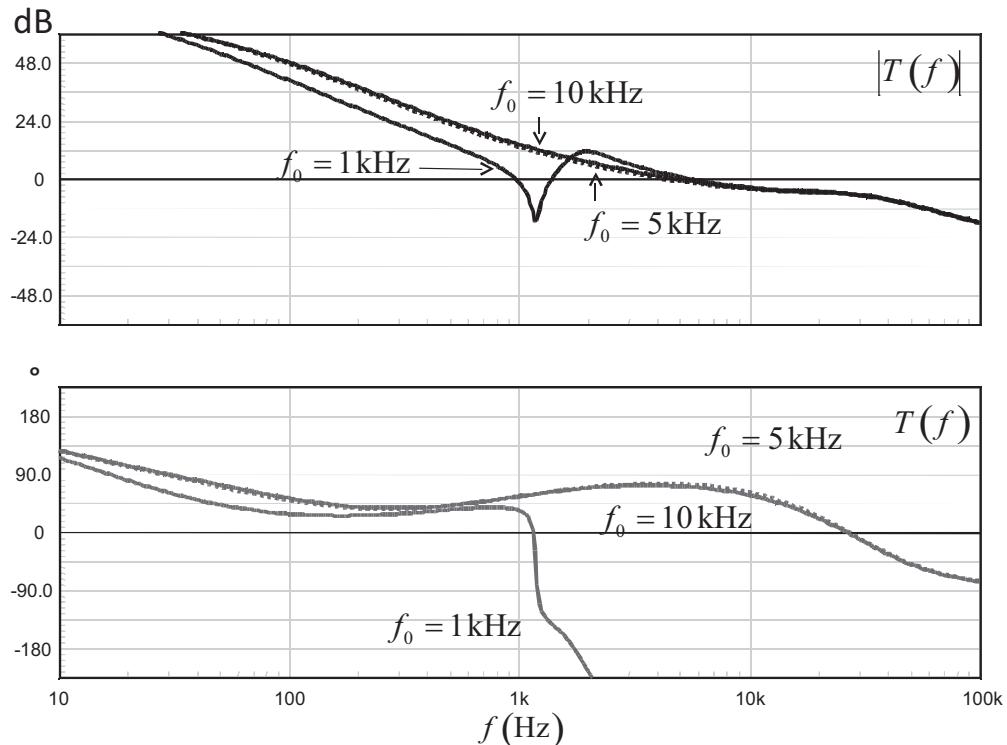


Figure 7.58 Ac results show no alteration at crossover when the *LC* network cutoff frequency stays away from the 1-kHz crossover point.

gain [3]. Another option is to open the loop at the optocoupler collector level as it naturally combines both signals. Please see Chapter 9 for more details.

References

- [1] Irving, B., Y. Panov, and M. Jovanovic, “Small-Signal Model of Variable Frequency Flyback Converter,” APEC 2003 Proceedings, Vol. 2, pp. 977–982.
- [2] Ridley, R., “Designing with the TL431,” Designer Series XV, www.switchingpowermagazine.com.
- [3] Conseil, S., N. Cyr, and C. Basso, “Stability Analysis in Multiple Loop Systems,” AND8327D, www.onsemi.com.

Shunt Regulator–Based Compensators

In the previous chapters, we have studied compensators that deliver an error voltage, $V_{err}(s)$, which controls either the duty ratio D (voltage mode control) or the peak current setpoint (peak-current mode control). Popularized by Power Integrations over the past 15 years, the TOPSwitch® is a high-voltage switcher implementing the *shunt regulator*. Rather than controlling the duty ratio by changing a voltage level on a pin, the company combined the V_{cc} and the feedback pins together so that a single input could not only supply the control section but also drive the duty ratio excursion by monitoring the injected current: a three-pin integrated switcher was born. Even if the loop is controlled by a TL431 or a Zener diode, we dedicated a chapter to describe the compensator implementation given the peculiarity of the circuit. Figure 8.1 shows the representation of the shunt regulator as it can be found in a TOPSwitch device [1].

The circuit works like an active Zener diode featuring a dynamic resistor R_d of $15\ \Omega$. When there is almost no injected current in the feedback pin (FB), the delivered duty ratio is maximum (67 percent). On the contrary, when more than 6 mA are injected, the duty ratio drops to its minimum value or 1.8 percent. Varying the injected current depending on the input/output conditions is the adopted means to adjust the duty ratio. To improve the noise immunity and also to shape the compensator response, a 7-kHz pole was included in the modulator path. We will need to account for his presence during the ac analysis. The curve depicting the modulator transfer function, D versus I_{FB} , appears in Figure 8.2.

Due to the information displayed on the curve, the small-signal gain of the whole modulator can be deduced. It is simply

$$S_{PWM} = \frac{\Delta D}{\Delta I_{FB}} = \frac{1.8 - 67}{6 - 2} \approx -16\%/\text{mA} \quad (8.1)$$

However, in the models we use, the duty ratio value is usually expressed in volts: a 1-V dc signal represents a 100 percent duty ratio. As current is primarily expressed in amperes rather than milliamperes, (8.1) needs to be reformulated to cope with our simulation models:

$$S_{PWM} = \frac{0.017 - 0.67}{6m - 2m} = -163\text{ V/A} \quad (8.2)$$

Expressed in decibels, this slope becomes a gain of

$$G_{PWM} = 20 \log_{10} (163) \approx 44\text{ dB} \quad (8.3)$$

This specific arrangement requires a little bit more of analysis compared to a traditional voltage-mode feedback. However, experience shows that it does not prevent

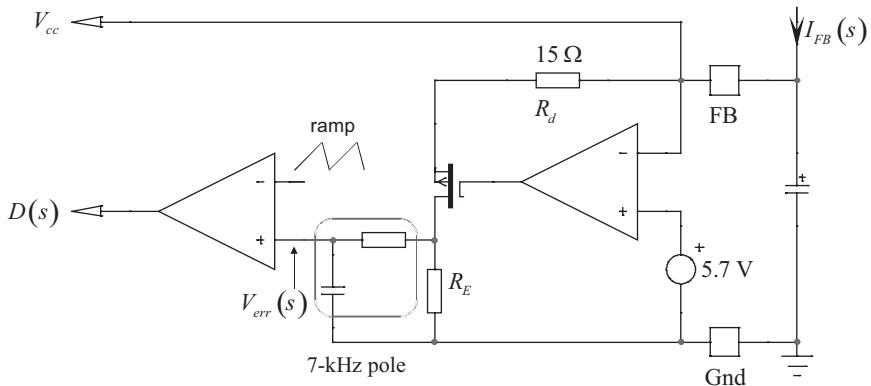


Figure 8.1 The internal structure of a TOPSwitch duty-cycle modulator. Unlike peak-current mode controllers whose setpoint is defined by a control voltage, the shunt regulator deals with a control current.

the implementations of the type 2 and 3 compensators as we described them in the previous chapters. The type 1 will not be described here, as a voltage-mode converter is usually compensated with a type 2 or even a type 3 when continuous conduction mode (CCM) is entered during an overload condition, for instance. If for a given reason a type 1 is needed, just use the type 2 formulas and set the phase boost to 0, and you have it!

8.1 The Type 2: An Origin Pole plus a Pole/Zero Pair

The duty ratio modulator input connects to the TL431-based compensator as suggested by Figure 8.3. The V_{cc} comes from an auxiliary winding, on the primary side of the converter. As the operating voltage of the switcher is around 5.7 V, this V_{cc} has to be above this value. 12 V is usually the adopted level.

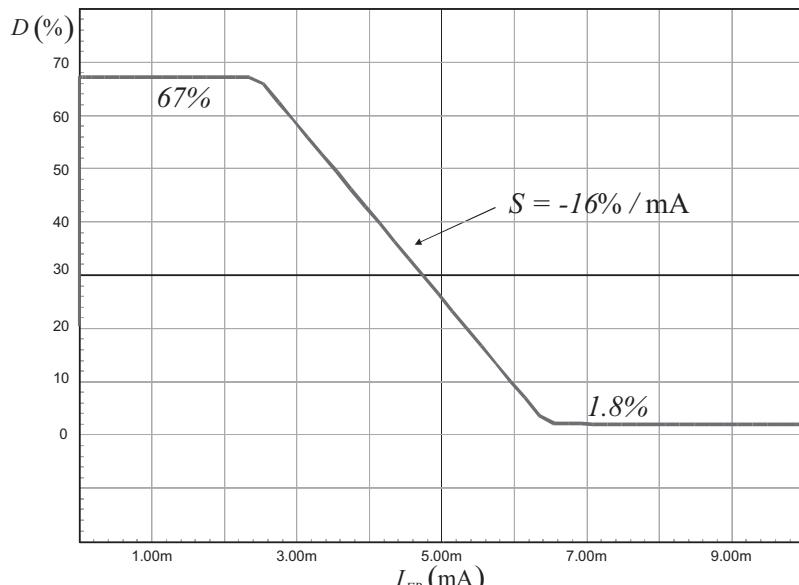


Figure 8.2 This curve shows the duty ratio variations in relationship to the injected current.

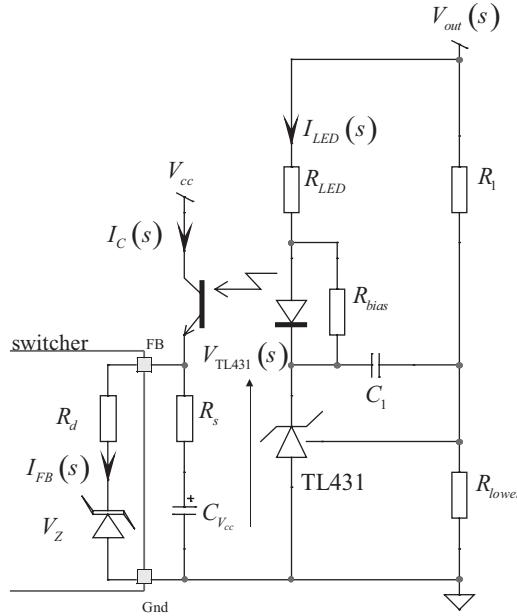


Figure 8.3 The TL431 regulates the output variable by injecting current into the feedback input of the power switcher. This current is derived from an auxiliary voltage.

When the output voltage deviates from its target, let's assume it increases, the current goes up in the optocoupler LED, and more current gets injected into the switcher feedback pin. According to Figure 8.2, the duty ratio diminishes. To ensure the self-supply of the switcher, a V_{cc} capacitor is connected from the feedback pin to the ground. It provides the necessary energy reservoir to help during the startup sequence and rectifies the high-frequency pulses when the converter operates. A 47- μF capacitor is a common choice for this part. Being wired between the feedback pin and ground, it also has an ac role as it introduces a pole. Since a zero might also be helpful for phase boost needs, it is of design practices to add a small resistor R_s in series with the capacitor. However, given the dc drop it introduces at startup, it is not recommended to go beyond 15 Ω unless an extra capacitor is added [2]. You are familiar with the rest of the arrangement around the TL431. Following these remarks, we can start with the ac analysis. Let's start with the ac current circulating in the LED, neglecting the bias current contribution:

$$I_{LED}(s) = \frac{V_{out}(s) - V_{TL431}(s)}{R_{LED}} = \frac{V_{out}(s) + V_{out}(s) \left(\frac{1}{sR_1C_1} \right)}{R_{LED}} = \frac{V_{out}(s)(1 + sR_1C_1)}{R_{LED} sR_1C_1} \quad (8.4)$$

The LED current gives birth to the optocoupler collector current via the CTR of the device:

$$I_C(s) = \text{CTR} I_{LED}(s) \quad (8.5)$$

This current then splits between the feedback pin and the capacitor network made of $C_{V_{cc}}$ and R_s :

$$I_{FB}(s) = I_C(s) \frac{R_s + \frac{1}{sC_{V_{cc}}}}{R_d + R_s + \frac{1}{sC_{V_{cc}}}} = I_C(s) \frac{\frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}}}{\frac{sC_{V_{cc}}(R_s + R_d) + 1}{sC_{V_{cc}}}} = I_C(s) \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \quad (8.6)$$

Now replacing $I_C(s)$ by its expression in (8.5) and (8.4), we have

$$\frac{I_{FB}(s)}{V_{out}(s)} = \frac{\text{CTR}}{R_{LED}} \frac{(1 + sR_1C_1)}{sR_1C_1} \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \quad (8.7)$$

Factoring $1 + sR_1C_1$, we obtain

$$\frac{I_{FB}(s)}{V_{out}(s)} = \frac{\text{CTR}}{R_{LED}} \frac{1 + 1/sR_1C_1}{1 + sC_{V_{cc}}(R_s + R_d)} (1 + sR_s C_{V_{cc}}) \quad (8.8)$$

The current $I_{FB}(s)$ is injected into the duty ratio modulator whose transfer function includes a gain as described by (8.3), followed by a 7-kHz pole:

$$\frac{D(s)}{I_{FB}(s)} = -G_{PWM} \frac{1}{1 + s/\omega_{p2}} \quad (8.9)$$

The pole helps for the noise immunity but also offers the high-frequency pole f_{p2} we need for a type-2 configuration. Unfortunately, it is fixed and we will have to deal with it. If we now combine both expressions given by (8.8) and (8.9), we obtain the complete chain from the compensator input to the duty ratio generator:

$$\frac{D(s)}{V_{out}(s)} = -G_0 \frac{1 + \omega_{z2}/s}{1 + s/\omega_{p1}} \frac{1 + s/\omega_{z1}}{1 + s/\omega_{p2}} \quad (8.10)$$

This is what Figure 8.4 depicts.

In equation (8.10), we have:

$$G_0 = \frac{\text{CTR}}{R_{LED}} G_{PWM} \quad (8.11)$$

$$\omega_{z1} = \frac{1}{R_s C_{V_{cc}}} \quad (8.12)$$

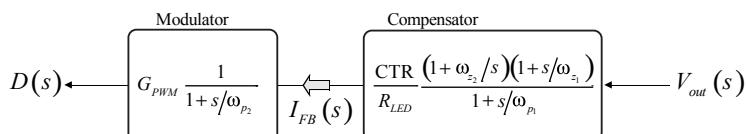


Figure 8.4 The chain from the observed variable to the duty ratio generator cascades two stages: the modulator and the compensator.

$$\omega_{z_2} = \frac{1}{R_1 C_1} \quad (8.13)$$

$$\omega_{p_1} = \frac{1}{(R_d + R_s) C_{V_{cc}}} \quad (8.14)$$

$$\omega_{p_2} = 44 \text{ krad/s} \quad (8.15)$$

This is two-pole and two-zero combination plus an origin pole. As we need a simple pole/zero pair and an origin pole, one pole and one zero will have to be canceled. We will see how in the design example. The resistor setting the mid-band gain is the LED series resistor. We need to extract its value for the magnitude definition of (8.8):

$$|G(f_c)| = \frac{\text{CTR}}{R_{LED}} G_{PWM} \frac{\sqrt{1 + (f_{z_2}/f_c)^2}}{\sqrt{1 + (f_c/f_{p_1})^2}} \frac{\sqrt{1 + (f_c/f_{z_1})^2}}{\sqrt{1 + (f_c/f_{p_2})^2}} \quad (8.16)$$

From which we can extract the value of the LED resistor:

$$R_{LED} = \frac{\text{CTR}}{G} G_{PWM} \frac{\sqrt{1 + \left(\frac{f_{z_2}}{f_c}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{z_1}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \quad (8.17)$$

Let's now have a look at the biasing limits. The maximum duty ratio is obtained when around 7 mA are injected in the feedback pin. As this current circulates in the optocoupler and the LED, its series resistor cannot be too high; otherwise, the compensator will fail to properly regulate in light load conditions where maximum current is needed. The maximum current the LED resistor will face occurs when I_C equals 7 mA:

$$I_{R_{LED},\max} = \frac{I_{C,\max}}{\text{CTR}_{\min}} + I_{bias} \quad (8.18)$$

The current circulating in the LED resistor is made of the reflected collector current plus the bias current I_{bias} . As the voltage on the TL431 cannot be lower than 2.5 V, we have

$$I_{R_{LED},\max} = \frac{V_{out} - V_f - V_{TL431,\min}}{R_{LED}} \quad (8.19)$$

As (8.18) and (8.19) are equal, we can solve the maximum LED resistor value satisfying the proper operating conditions:

$$R_{LED,\max} \leq \frac{\text{CTR}_{\min} (V_{out} - V_f - V_{TL431,\min})}{I_{C,\max} + I_{bias} \text{CTR}_{\min}} \quad (8.20)$$

Now that we have everything on hand, it is time for a design example...

8.1.1 A Design Example

The design example we will choose is a flyback converter operated in DCM. It appears in Figure 8.5 and shows how we combined the voltage-mode model and the shunt regulator sub circuit. The description of these two blocks is thoroughly documented in [3]. The ac sweep requires a little bit of care to choose the opening point. Remember that the loop regulates the output voltage by injecting a current in the feedback pin. In most of our SPICE analysis, we deal with voltage transfer loops. In our example, if we only have access to the feedback pin, we are stuck and need to observe the feedback current, probably through an extra resistor. This is not a big deal, but it requires extra manipulations to get the result. To circumvent this difficulty, we will open the loop after the modulator since it delivers a voltage between 18 mV and 680 mV for a duty ratio comprised between 1.8 percent and 67 percent. This is what the figure shows. This will help to observe the power stage trans-

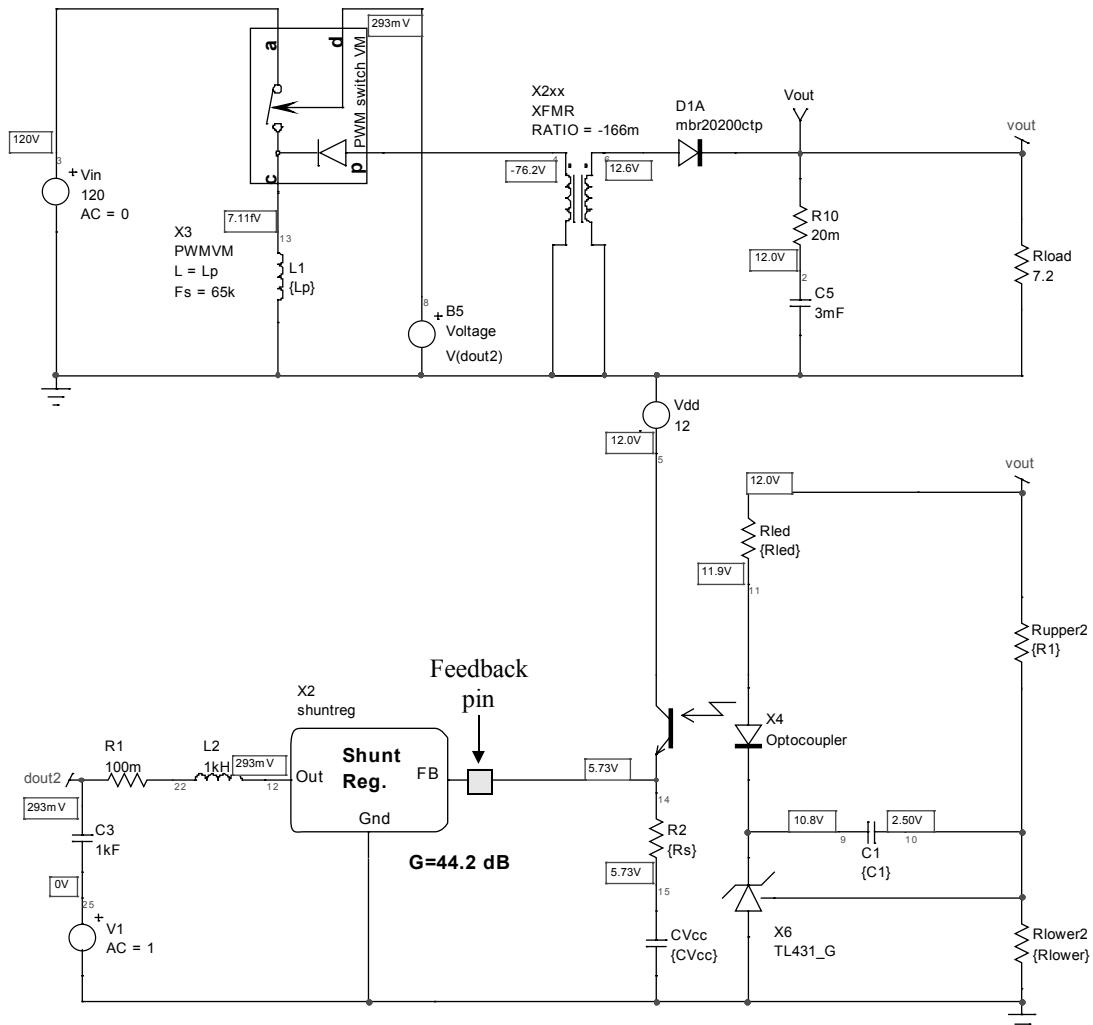


Figure 8.5 The flyback simulation of the TOPSwitch requires a particular loop opening, after the modulator.

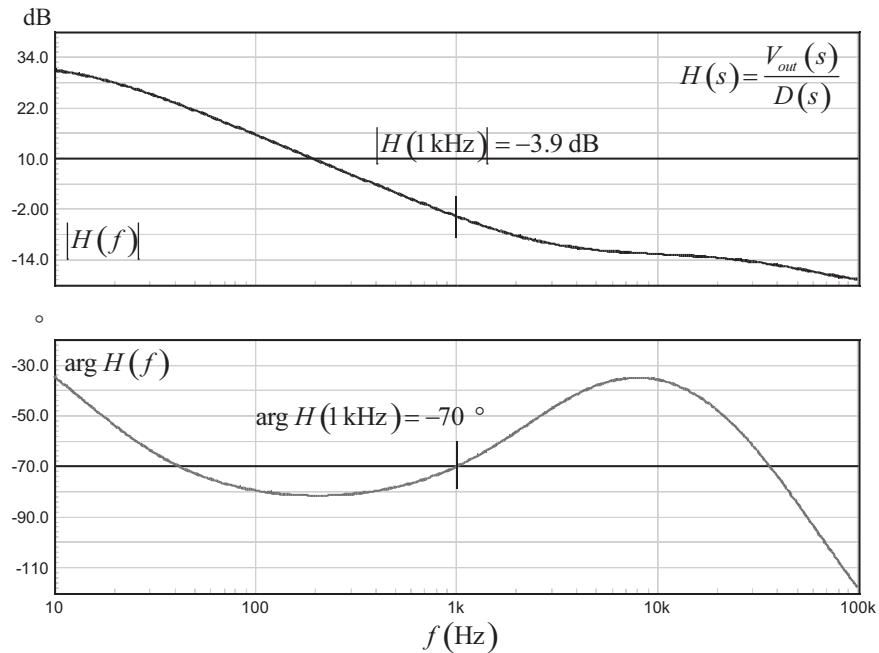


Figure 8.6 The power stage transfer function of the flyback operated in DCM. Please note that this is the output $V_{out}(s)$ to the duty ratio $D(s)$ input that is plotted.

fer function, excluding the modulator of course. The whole chain from V_{out} to D being available through (8.10), we have everything to carry on. One remark though. In real life, you will not be able to open the loop after the modulator since all is internal circuitry. Following guidelines in [4], it is likely that the injection occurs on the feedback pin directly, through a series resistor. In that case, the power stage transfer function will already be affected by the PWM modulator gain of 44 dB. Therefore, when calculating the LED series resistor value with the help of (8.17), the G_{PWM} term will have to disappear from the formula. The rest stays as it is.

The transfer function appears in Figure 8.6. If we select a 1-kHz crossover frequency with 60° phase margin, the gain deficiency at this point is -3.9 dB and the phase lag is -70° .

Let us debut the calculation by assessing the maximum LED resistor value, using (8.20) and assuming the following parameters:

$V_{out} = 12$ V; the output voltage.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1$ mA; the TL431 biasing current when the optocoupler LED is paralleled with a resistor.

$V_{TL431,min} = 2.5$ V; the minimum operating voltage of the TL431.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 38$ k Ω ; the upper resistor in the resistor bridge observing the output variable.

$C_{Vcc} = 47 \mu\text{F}$; the selected V_{cc} capacitor according to the switcher data sheet.

$$R_{LED,\max} \leq \frac{\text{CTR}_{\min} (V_{out} - V_f - V_{TL431,\min})}{I_{C,\max} + I_{bias} \text{CTR}_{\min}} \leq \frac{0.8 \times (12 - 1 - 2.5)}{7m + 1m \times 0.8} \leq 1.09 \text{ k}\Omega \quad (8.21)$$

The 3.9-dB of gain translate to

$$G = 10^{\frac{-Gf_c}{20}} = 10^{\frac{3.9}{20}} \approx 1.6 \quad (8.22)$$

Given the 70° phase lag at the selected crossover frequency and a desired phase margin of 60°, we need to boost the phase by 40°. Considering the 1-kHz frequency selection and the presence of a 7-kHz pole, we need to place a first zero at

$$f_{z_1} = \frac{f_c}{\tan\left(\text{boost} + \tan^{-1}\left(\frac{f_c}{f_{p_2}}\right)\right)} = \frac{1k}{\tan\left(40 + \tan^{-1}\left(\frac{1k}{7k}\right)\right)} = 896 \text{ Hz} \quad (8.23)$$

This first zero will serve to calculate the resistor R_s in series with the 47- μF V_{cc} capacitor:

$$R_s = \frac{1}{2\pi f_{z_1} C_{V_{cc}}} = \frac{1}{6.28 \times 896 \times 47\mu\text{F}} \approx 3.8 \Omega \quad (8.24)$$

It is below the maximum of 15 Ω indicated by the switcher manufacturer, so we are safe. This resistor now combines with the shunt regulator input impedance to form a pole together with the V_{cc} capacitor as explained by (8.14):

$$f_{p_1} = \frac{1}{2\pi(R_d + R_s)C_{V_{cc}}} = \frac{1}{6.28 \times (15 + 3.8) \times 47\mu\text{F}} = 180 \text{ Hz} \quad (8.25)$$

Equation (8.10) actually reveals a type 3 expression exhibiting a double pair of poles/zeros and an origin pole. For our type 2 compensation, one pair of pole/zero must be neutralized. This is the couple $f_{z_2} f_{p_1}$. We know that the first pole f_{p_1} is positioned at 180 Hz; let's us calculate the value of C_1 to position the second zero f_{z_2} right at this point:

$$C_1 = \frac{1}{2\pi f_{z_2} R_1} = \frac{1}{6.28 \times 180 \times 38k} = 23.3 \text{ nF} \quad (8.26)$$

Given the neutralization of a pole/zero pair, we are now left with a type 2 system having a pole at 7 kHz, a zero at 896 Hz, and an origin pole. To finish our design, we just need to calculate the value of R_{LED} as expressed by (8.17):

$$\begin{aligned} R_{LED} &= \frac{\text{CTR}}{G} G_{PWM} \frac{\sqrt{1 + \left(\frac{f_{z_2}}{f_c}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{z_1}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2} \sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} = \frac{0.8}{1.6} \times 10^{\frac{44}{20}} \\ &\times \frac{\sqrt{1 + \left(\frac{180}{1k}\right)^2} \sqrt{1 + \left(\frac{1k}{896}\right)^2}}{\sqrt{1 + \left(\frac{1k}{180}\right)^2} \sqrt{1 + \left(\frac{1k}{7k}\right)^2}} \approx 21 \Omega \end{aligned} \quad (8.27)$$

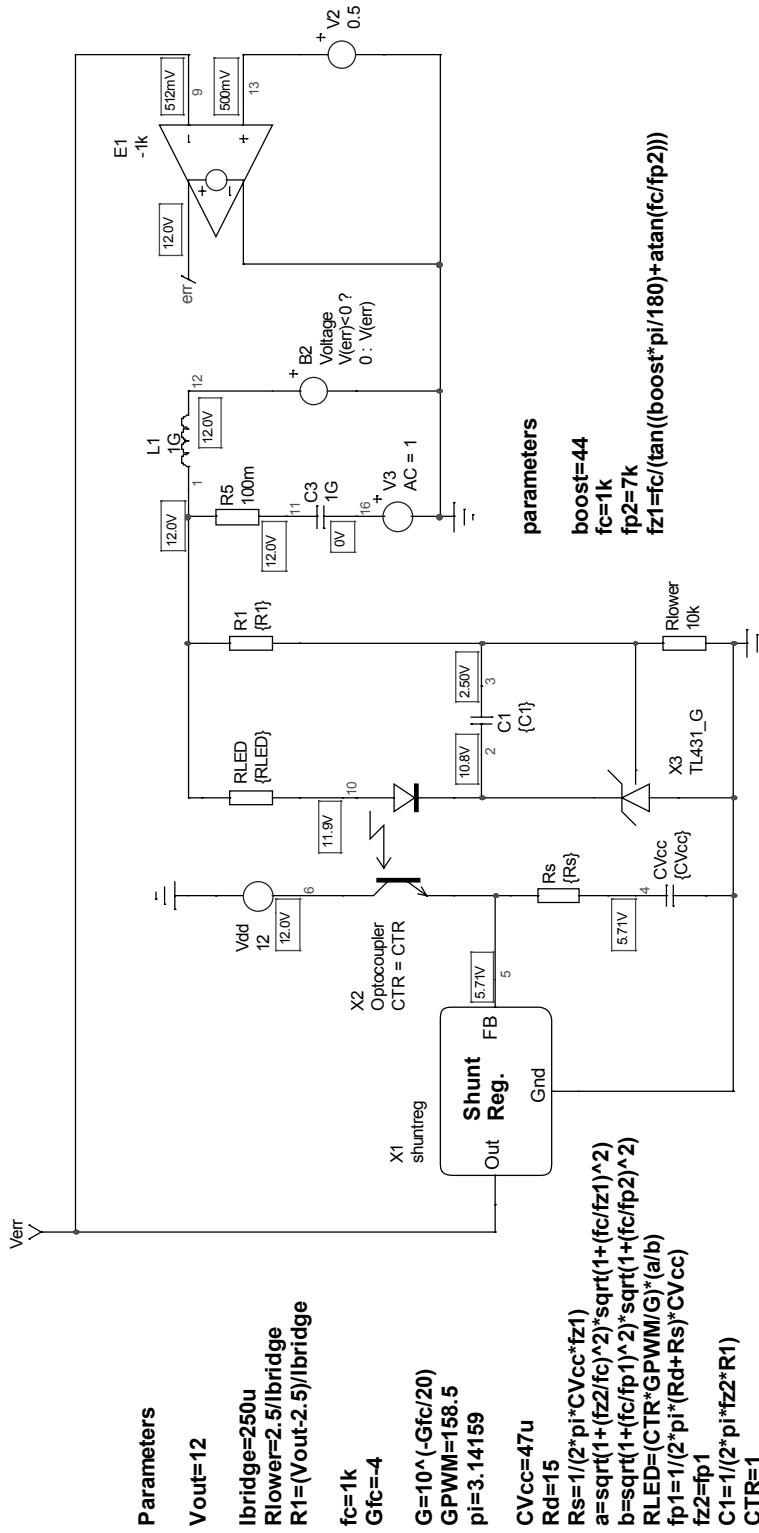


Figure 8.7 The compensator using the shunt regulator works well but requires care in selecting the surrounding elements.

Having all these elements calculated, we can now feed our test fixture and check the ac response of this compensator alone. This is what Figure 8.7 portrays. The bias points are good. The current in the LED resistor is around 3.5 mA, which according to Figure 8.2 must correspond to around 50 percent duty ratio. This is the value obtained on the output of the shunt regulator subcircuit: 512 mV corresponds to a 51.2 percent duty ratio.

The ac response of this compensator appears in Figure 8.8. The overall shape is ok, despite a small mismatch on the gain target. This is the effect of the LED dynamic resistor not accounted for in the calculations. As the series LED resistor is rather small, the contribution of the dynamic resistor is more significant. The phase boost is exhibiting the right value, but the peak is not occurring at the 1-kHz target. This is because of 7-kHz internal pole that we undergo cannot be adjusted at the right value. To benefit from the maximum phase boost, we should change the crossover frequency and put it to

$$f_{c,new} = \sqrt{f_{z1} f_{p2}} = \sqrt{896 \times 7k} = 2.5 \text{ kHz} \quad (8.28)$$

According to Figure 8.6, the gain target should then be changed to ≈ 9 dB in order to crossover at 2.5 kHz.

The compensated version of Figure 8.5 has been ac swept and also tested on transient response. The compound results are given in Figure 8.9 and show a good phase margin of nearly 60° . The output has been stepped from 0.8 A to

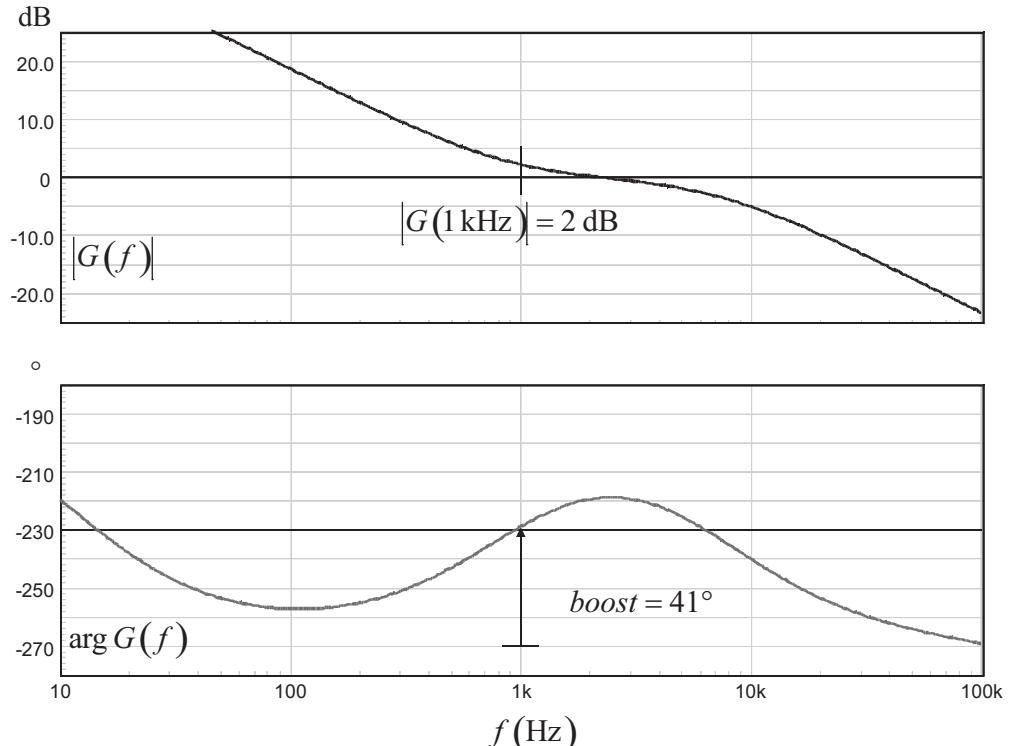


Figure 8.8 The ac response shows a slight discrepancy between the gain target and what is obtained. Again, the culprit is the LED dynamic resistor.

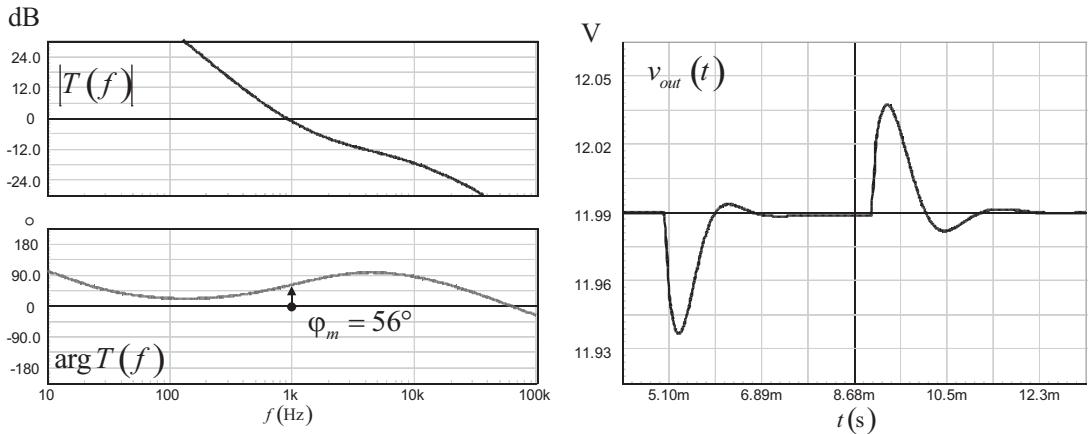


Figure 8.9 The open-loop gain shows a good phase margin, leading to an excellent transient response.

2 A with a slew-rate of 1 A/ μ s, and the deviation is very small: we have a stable power supply.

What limits affect this design? The first one relates to the LED series resistor value. In this design example, we have a 21- Ω resistor, so we have plenty of margin compared to the upper limit of 1 k Ω given by (8.21). The other limitation comes from the resistor inserted in series with the V_{cc} capacitor. This resistor introduces a zero, which is helpful to boost the phase in relationship to the 7-kHz internal pole. However, a resistor in series with the V_{cc} capacitor will affect the storage capabilities of the network during the startup sequence and the auto-recovery mode. This is because the voltage drop that appears across this series element can, in case it is too high, prematurely trip the undervoltage lockout circuitry. The data sheet advises a value less than 15 Ω in some TOPSwitch references. You can go beyond this value, but an extra capacitor has to be added (see [2] for more details). If we stick with a 15 Ω value and the recommended 47- μ F capacitor, the zero you will add cannot be lower than

$$f_{z1,\max} = \frac{1}{2\pi R_{s,\max} C_{V_{cc}}} = \frac{1}{6.28 \times 15 \times 47\mu} \approx 226 \text{ Hz} \quad (8.29)$$

We know that the maximum phase boost peaks at the geometric mean between the considered zero and pole. For a 226-Hz zero and a 7-kHz pole, the peak will occur at

$$f_c = \sqrt{f_{z1} f_{p2}} = \sqrt{226 \times 7k} = 1.25 \text{ kHz} \quad (8.30)$$

At this frequency, the maximum phase boost you can obtain will be

$$\text{Boost}_{\max} = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right) = \tan^{-1}\left(\frac{1.25k}{226}\right) - \tan^{-1}\left(\frac{1.25k}{7k}\right) \approx 70^\circ \quad (8.31)$$

8.2 The Type 3: An Origin Pole plus a Double Pole/Zero Pair

The type 3 compensator offers a larger phase boost than its type 2 counterpart. Unfortunately, because of the fixed internal 7-kHz pole present in the duty ratio modulator and the limit set for the resistor R_s , we cannot expect the full flexibility as with a traditional op amp approach. That being said, let us have a look at a type 3 implementation as it appears in Figure 8.10. The principle remains the same: how do we add another pole/zero pair given the fast lane presence? As we did for the TL431 with a voltage-mode feedback control, a RC network will be added in parallel with the LED series resistor. The network will add the zero/pole pair we are looking for in a type 3 architecture. As we already derived the transfer function of the type 2—see (8.8)—going to the type 3 simply requires us to replace R_{LED} with the equivalent impedance brought by the new network Z_{LED} highlighted in Figure 8.10:

$$Z_{LED} = \frac{R_{LED} \left(R_3 + \frac{1}{sC_3} \right)}{R_{LED} + \left(R_3 + \frac{1}{sC_3} \right)} = R_{LED} \frac{sR_3C_3 + 1}{sC_3(R_{LED} + R_3) + 1} \quad (8.32)$$

Now substituting this expression in (8.8), we have

$$\frac{I_{FB}(s)}{V_{out}(s)} = \frac{\text{CTR}}{R_{LED}} \frac{1 + 1/sR_1C_1}{1 + sC_{V_{cc}}(R_s + R_d)} (1 + sR_s C_{V_{cc}}) \frac{sC_3(R_{LED} + R_3) + 1}{sR_3C_3 + 1} \quad (8.33)$$

The current $I_{FB}(s)$ is injected into the duty ratio modulator whose transfer function includes a gain as described by (8.3), followed by a 7-kHz pole:

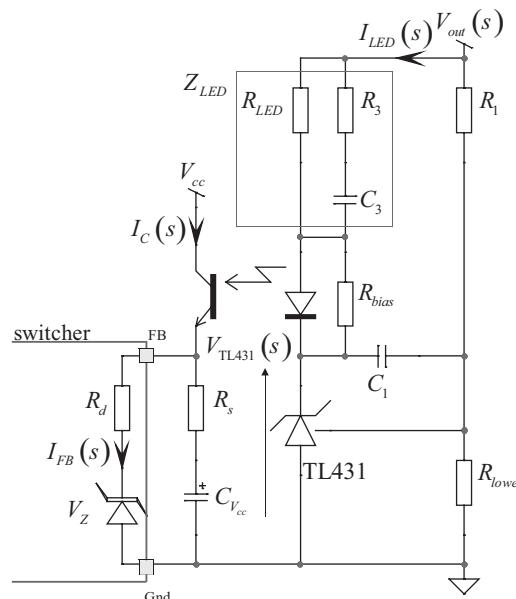


Figure 8.10 A type 3 implementation with a shunt regulator suffers from the limits imposed on R_s and the internal 7-kHz pole.

$$\frac{D(s)}{I_{FB}(s)} = -G_{PWM} \frac{1}{1 + s/\omega_{p_2}} \quad (8.34)$$

If we now combine expressions given by (8.33) and (8.34), we obtain the complete chain from the compensator input to the duty ratio output:

$$\frac{D(s)}{V_{out}(s)} = -G_0 \frac{(1 + \omega_{z_2}/s)(1 + s/\omega_{z_1})(1 + s/\omega_{z_3})}{(1 + s/\omega_{p_1})(1 + s/\omega_{p_2})(1 + s/\omega_{p_3})} \quad (8.35)$$

In (8.35), we have

$$G_0 = \frac{CTR}{R_{LED}} G_{PWM} \quad (8.36)$$

$$\omega_{z_1} = \frac{1}{R_s C_{V_{cc}}} \quad (8.37)$$

$$\omega_{z_2} = \frac{1}{R_1 C_1} \quad (8.38)$$

$$\omega_{z_3} = \frac{1}{sC_3(R_{LED} + R_3)} \quad (8.39)$$

$$\omega_{p_1} = \frac{1}{(R_d + R_s)C_{V_{cc}}} \quad (8.40)$$

$$\omega_{p_2} = 44 \text{ krad/s} \quad (8.41)$$

$$\omega_{p_3} = \frac{1}{sR_3C_3} \quad (8.42)$$

The resistor setting the mid-band gain is the LED series resistor. We first start by extracting the magnitude of the compensator gain, $G(s)$, as derived in (8.35):

$$|G(f_c)| = \frac{CTR}{R_{LED}} G_{PWM} \frac{\sqrt{1 + (f_{z_2}/f_c)^2}}{\sqrt{1 + (f_c/f_{p_1})^2}} \frac{\sqrt{1 + (f_c/f_{z_1})^2}}{\sqrt{1 + (f_c/f_{p_2})^2}} \frac{\sqrt{1 + (f_c/f_{z_3})^2}}{\sqrt{1 + (f_c/f_{p_3})^2}} \quad (8.43)$$

From which we can extract the value of the LED resistor:

$$R_{LED} = \frac{CTR}{G} G_{PWM} \frac{\sqrt{1 + \left(\frac{f_{z_2}}{f_c}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_1}}\right)^2}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{z_1}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_2}}\right)^2}} \frac{\sqrt{1 + \left(\frac{f_c}{f_{z_3}}\right)^2}}{\sqrt{1 + \left(\frac{f_c}{f_{p_3}}\right)^2}} \quad (8.44)$$

The definitions to obtain C_3 and R_3 are rather simple to derive. Extract R_3 from (8.42):

$$R_3 = \frac{1}{2\pi f_{p_3} C_3} \quad (8.45)$$

Substitute (8.45) in (8.39), and solve for C_3 :

$$C_3 = \frac{f_{p_3} - f_{z_3}}{2\pi R_{LED} f_{p_3} f_{z_3}} \quad (8.46)$$

The design methodology will remain similar to that of the type 2. As we have a system featuring three poles and three zeros now, a pole/zero pair has to be neutralized. These are f_{z_2} and f_{p_1} . Then the rest of the components follow easily, as we will see in the upcoming design example.

8.2.1 A Design Example

In this design example, let us assume the following component values:

$V_{out} = 12$ V; the output voltage.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1$ mA; the TL431 biasing current when the optocoupler LED is paralleled with a resistor

$V_{TL431,min} = 2.5$ V; the minimum operating voltage of the TL431.

$CTR_{min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 38$ k Ω ; the upper resistor in the resistor bridge observing the output variable.

$C_{Vcc} = 47 \mu F$; the selected V_{cc} capacitor according to the switcher data sheet.

From the transfer function of the voltage-mode forward converter we want to stabilize, we need a gain of 10 dB at a 2-kHz frequency, while the needed phase boost is 120° at crossover. Is this feasible, given the limitations brought by the shunt regulator? We do not have too many choices. The easiest way is to position a second pole at 7 kHz and see where to position the double zero given the targeted phase boost. From our first chapters, we know that for a given phase boost and a known double pole position (7 kHz in our case), the double zero must be placed at the following place:

$$f_{z_{1,2}} = \frac{f_c}{\tan\left(\frac{\text{boost}}{2} + \tan^{-1}\frac{f_c}{f_{p_{1,2}}}\right)} \quad (8.47)$$

This formula is valid only as long as the denominator, $\tan(x)$, is different from 0. This would occur if x is either 0 or is equal to 90°. From (8.47), we can quickly solve the value of f_c for which x equals 90°:

$$f_c = \tan\left(90 - \frac{\text{boost}}{2}\right) f_{p_{1,2}} \quad (8.48)$$

Given the 7-kHz double pole we have chosen and the 120° we are looking for, it gives us a maximum crossover frequency of

$$f_c = \tan\left(90 - \frac{120}{2}\right) \times 7k \approx 4 \text{ kHz} \quad (8.49)$$

Given the 2-kHz crossover value we want, we have some margin there. To reach the 120° phase boost at 2 kHz and assuming two coincident poles at 7 kHz, we will have to place the double zero at the following frequency:

$$f_{z_{1,2}} = \frac{f_c}{\tan\left(\frac{\text{boost}}{2} + \tan^{-1}\frac{f_c}{f_{p_{1,2}}}\right)} = \frac{2k}{\tan\left(\frac{120}{2} + \tan^{-1}\left(\frac{2k}{7k}\right)\right)} \approx 500 \text{ Hz} \quad (8.50)$$

This value leads us to define the series resistor value, R_s :

$$R_s = \frac{1}{2\pi f_{z_1} C_{V_{cc}}} = \frac{1}{6.28 \times 500 \times 47\mu} = 6.8 \Omega \quad (8.51)$$

Together with the shunt regulator equivalent dynamic resistor, it creates a pole located at

$$f_{p_1} = \frac{1}{2\pi(R_s + R_d)C_{V_{cc}}} = \frac{1}{6.28 \times (6.8 + 15) \times 47\mu} = 155 \text{ Hz} \quad (8.52)$$

This pole has to be canceled by the second zero we are going to place with C_1 :

$$C_1 = \frac{1}{2\pi f_{z_2} R_1} = \frac{1}{6.28 \times 155 \times 38k} = 27 \text{ nF} \quad (8.53)$$

The upcoming design steps require the knowledge of the LED series resistor. Applying (8.44) and using (8.3) for the duty ratio modulator gain, we have

$$R_{LED} = \frac{0.8}{10^{\frac{10}{20}}} \times 163 \times \frac{\sqrt{1 + \left(\frac{155}{2k}\right)^2} \sqrt{1 + \left(\frac{2k}{500}\right)^2} \sqrt{1 + \left(\frac{2k}{500}\right)^2}}{\sqrt{1 + \left(\frac{2k}{155}\right)^2} \sqrt{1 + \left(\frac{2k}{7k}\right)^2} \sqrt{1 + \left(\frac{2k}{7k}\right)^2}} = 50 \Omega \quad (8.54)$$

As the values adopted in this example are the same as in the previous exercise for the type 2, the result of (8.21) still holds. We are safe; there is plenty of margin. The third pole has been chosen to be coincident with the internal one, f_{p_2} , at 7 kHz, and the third zero will also be coincident with the first one at 500 Hz. Using (8.46), we can evaluate the value of C_3 :

$$C_3 = \frac{f_{p_3} - f_{z_3}}{2\pi R_{LED} f_{p_3} f_{z_3}} = \frac{7k - 500}{6.28 \times 50 \times 7k \times 500} = 5.9 \mu\text{F} \quad (8.55)$$

Having C_3 , we can get the series resistor R_3 :

$$R_3 = \frac{1}{2\pi f_{p_3} C_3} = \frac{1}{6.28 \times 7k \times 5.9\mu} = 3.9 \Omega \quad (8.56)$$

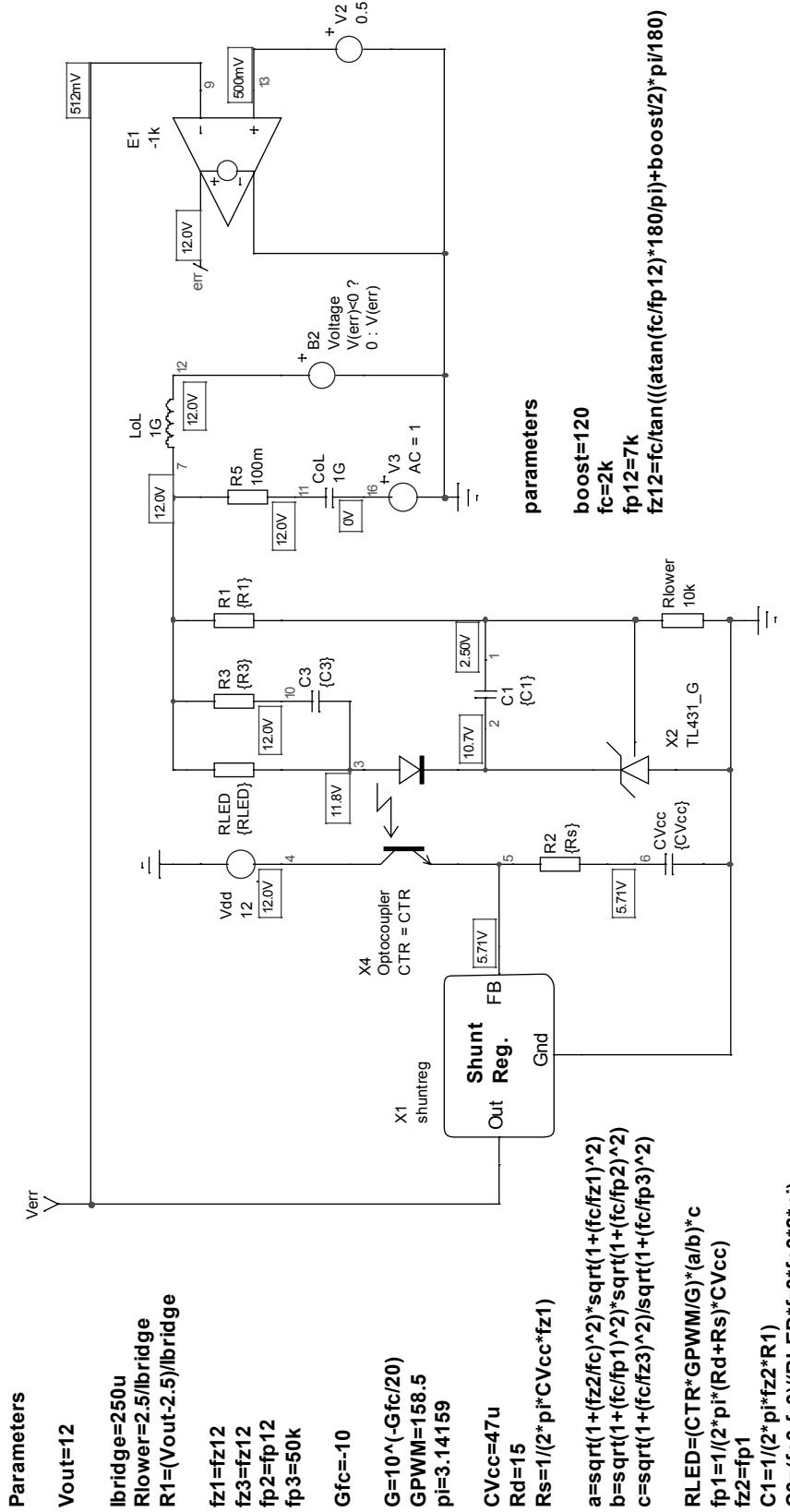


Figure 8.11 The shunt regulator can also be used in a type 3 compensator as it is shown here.

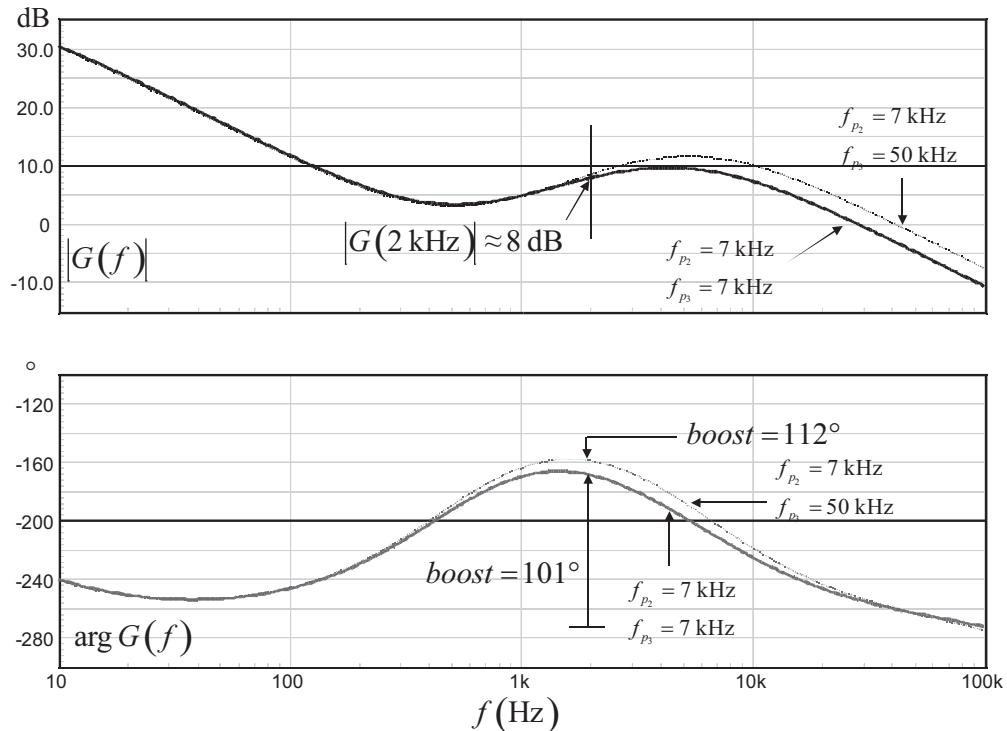


Figure 8.12 The ac response is a real type 3, despite a small mismatch on both the boost in phase and the crossover point.

We are all set now. The ac response of our compensator can now be explored thanks to the automated test fixture presented in Figure 8.11.

Once again, the automated calculations on the left panel help to change the compensator on the fly if needed. The ac response appears in Figure 8.12. There is a small mismatch on the crossover frequency, but this due to the LED dynamic resistance contribution, especially with LED series resistor of less than 100Ω . It also influences the phase boost as we can see on the plot. Since the equations are derived for the general case, we have the leisure to split the double pole and leave one to 7 kHz (we cannot move it; it is internal anyway) and push the second one to half the 100-kHz switching frequency, 50 kHz. As shown in the graph, it helps us to gain a little of phase boost, bringing the total to 112° .

8.3 The Type 3: An Origin Pole plus a Double Pole/Zero Pair—No Fast Lane

We know that the TL431 features a fast lane through the LED series resistor. This path offers to V_{out} a direct access to the duty ratio modulator, without passing through the TL431 op amp section. As we have detailed it in several other sections, the fast lane hampers the flexibility of the type 3 compensator by limiting the gain and the phase boost that can be generated. Figure 8.13 shows how the fast lane can be disabled via the implementation of a simple Zener-based regulator.

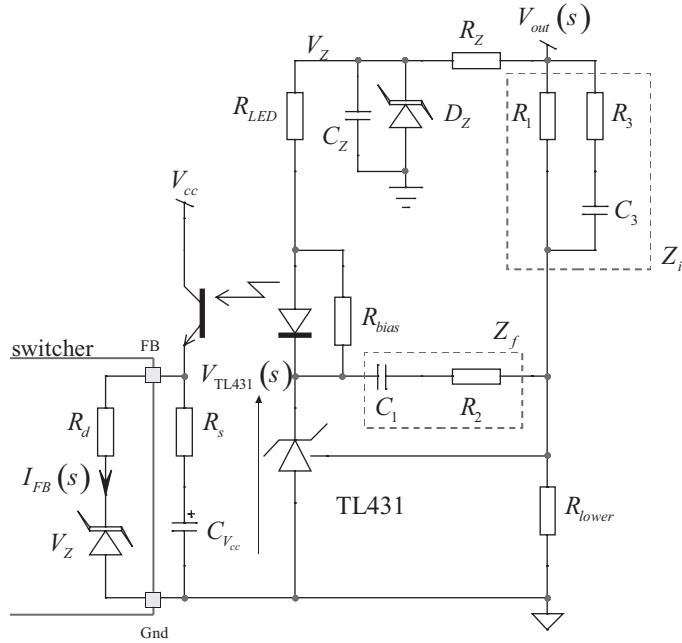


Figure 8.13 By using a simple Zener-based network, it is possible to get rid of the fast lane.

The principle behind the fast-lane deactivation is to remove the direct ac link between the LED ac current and the output voltage to be monitored. As shown in previous sections, and in particular in the TL431 chapter, a compensator based on a TL431 where the fast lane has been removed turns into a simple open-collector compensated op amp. The shunt regulator case does not change this rule. The output of the op amp under concern is the variable $V_{TL431}(s)$ in Figure 8.13. Its output voltage is the following:

$$V_{TL431}(s) = -V_{out}(s) \frac{Z_f}{Z_i} \quad (8.57)$$

Developing and rearranging this expression leads to

$$\begin{aligned} V_{TL431}(s) &= -V_{out}(s) \frac{\frac{sR_2C_1 + 1}{sC_1}}{\frac{R_1(1 + sR_3C_3)}{sC_3(R_1 + R_3) + 1}} = -V_{out}(s) \frac{sR_2C_1 + 1}{sR_1C_1} \frac{sC_3(R_1 + R_3) + 1}{(1 + sR_3C_3)} \\ &= -V_{out}(s) \frac{R_2}{R_1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)(1 + sC_3(R_1 + R_3))}{1 + sR_3C_3} \end{aligned} \quad (8.58)$$

The ac LED current no longer depends on both $V_{out}(s)$ and the op amp voltage but solely on that latter. Therefore,

$$I_{LED}(s) = -\frac{V_{TL431}(s)}{R_{LED}} = \frac{V_{out}(s)}{R_{LED}} \frac{R_2}{R_1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)(1 + sC_3(R_1 + R_3))}{1 + sR_3C_3} \quad (8.59)$$

The expression of the current injected into the shunt regulator has been derived with (8.6):

$$I_{FB}(s) = I_C(s) \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \quad (8.60)$$

As I_C and I_{LED} are linked by the optocoupler CTR, we have

$$\frac{I_{FB}(s)}{V_{out}(s)} = \frac{\text{CTR}}{R_{LED}} \frac{R_2}{R_1} \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)(1 + sC_3(R_1 + R_3))}{1 + sR_3C_3} \quad (8.61)$$

Thanks to (8.9), we know the link between the injected feedback current and the obtained duty ratio. By linking this expression to (8.61), we obtain the complete transfer function of our compensator:

$$\frac{D(s)}{V_{out}(s)} = -G_{PWM} \frac{\text{CTR}}{R_{LED}} \frac{R_2}{R_1} \frac{\left(1 + \frac{1}{sR_2C_1}\right)}{sC_{V_{cc}}(R_s + R_d) + 1} \frac{sR_s C_{V_{cc}} + 1}{1 + s/\omega_{p_2}} \frac{(1 + sC_3(R_1 + R_3))}{1 + sR_3C_3} \quad (8.62)$$

We can put this expression under a more familiar form such as

$$\frac{D(s)}{V_{out}(s)} = -G_0 \frac{(1 + \omega_{z_2}/s)(1 + s/\omega_{z_1})(1 + s/\omega_{z_3})}{(1 + s/\omega_{p_1})(1 + s/\omega_{p_2})(1 + s/\omega_{p_3})} \quad (8.63)$$

In this equation, we have

$$G_0 = G_{PWM} \frac{\text{CTR}}{R_{LED}} \frac{R_2}{R_1} \quad (8.64)$$

$$\omega_{z_1} = \frac{1}{R_s C_{V_{cc}}} \quad (8.65)$$

$$\omega_{z_2} = \frac{1}{R_2 C_1} \quad (8.66)$$

$$\omega_{z_3} = \frac{1}{sC_3(R_1 + R_3)} \quad (8.67)$$

$$\omega_{p_1} = \frac{1}{(R_d + R_s)C_{V_{cc}}} \quad (8.68)$$

$$\omega_{p_2} = 44 \text{ krad/s} \quad (8.69)$$

$$\omega_{p_3} = \frac{1}{sR_3C_3} \quad (8.70)$$

The LED resistor can now be calculated based on the minimum biasing conditions only, and (8.20) is still valid. However, resistor R_2 , which sets the mid-band gain, still needs to be derived according to the magnitude of (8.63):

$$|G(f_c)| = G_{PWM} \frac{\text{CTR}}{R_{LED}} \frac{R_2}{R_1} \frac{\sqrt{1 + (f_{z2}/f_c)^2}}{\sqrt{1 + (f_c/f_{p1})^2}} \frac{\sqrt{1 + (f_c/f_{z1})^2}}{\sqrt{1 + (f_c/f_{p2})^2}} \frac{\sqrt{1 + (f_c/f_{z3})^2}}{\sqrt{1 + (f_c/f_{p3})^2}} \quad (8.71)$$

Solving for R_2 , we have

$$R_2 = \frac{GR_{LED}R_1}{G_{PWM}\text{CTR}} \frac{\sqrt{1 + (f_c/f_{p1})^2}}{\sqrt{1 + (f_{z2}/f_c)^2}} \frac{\sqrt{1 + (f_c/f_{p2})^2}}{\sqrt{1 + (f_c/f_{z1})^2}} \frac{\sqrt{1 + (f_c/f_{p3})^2}}{\sqrt{1 + (f_c/f_{z3})^2}} \quad (8.72)$$

The Zener resistor R_Z must authorize the operating current for the feedback loop to which the bias current for both the Zener diode itself and the TL431 must be added. The current circulating in the LED alone depends on the current sourced by the optocoupler. According to Figure 8.2, this current $I_{C,\max}$ amounts to 7 mA. It peaks to a maximum in the LED when the CTR is minimum. Using these data, we can now derive the Zener dropping resistor value:

$$R_Z = \frac{V_{out} - V_Z}{\frac{I_{C,\max}}{\text{CTR}_{\min}} + I_{Zbias} + I_{bias}} = \frac{(V_{out} - V_Z)\text{CTR}_{\min}}{I_{C,\max} + (I_{Zbias} + I_{bias})\text{CTR}_{\min}} \quad (8.73)$$

In the previous equation, we have the following variables:

V_{out} , the output voltage

I_{bias} , the TL431 biasing current when the optocoupler LED is paralleled with a resistor (usually 1 kΩ for a 1-mA bias)

I_{Zbias} , the Zener diode biasing current

CTR_{\min} , the minimum optocoupler current transfer ratio

$I_{C,\max}$, the maximum current injected into the switcher feedback pin (7 mA, depending on the switcher reference)

Everything needed has been derived, so let us continue with a design example.

8.3.1 A Design Example

Suppose we have the following component values:

$V_{out} = 12$ V; the output voltage.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1$ mA; the TL431 biasing current when the optocoupler LED is paralleled with a resistor.

$V_{TL431,\min} = 2.5$ V; the minimum operating voltage of the TL431.

$I_{Zbias} = 3 \text{ mA}$; the Zener diode bias current.

$V_Z = 8.2 \text{ V}$; the Zener diode breakdown voltage.

$\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.

$R_1 = 38 \text{ k}\Omega$; the upper resistor in the resistor bridge observing the output variable.

$C_{Vcc} = 47 \mu\text{F}$; the selected V_{cc} capacitor according to the switcher data sheet.

From the transfer function of the voltage-mode converter we want to stabilize, we need a gain of 10 dB at a 1-kHz frequency, while the needed phase boost is 130° . Given the internal 7-kHz pole brought by the duty ratio modulator and considering coincident poles, the second pole will also be placed at 7 kHz. Let us calculate the position of the double zeros, considering these coincident poles.

$$f_{z_{1,2}} = \frac{f_c}{\tan\left(\frac{\text{boost}}{2} + \tan^{-1}\frac{f_c}{f_{p_{1,2}}}\right)} = \frac{1k}{\tan\left(\frac{130}{2} + \tan^{-1}\left(\frac{1k}{7k}\right)\right)} = 303 \text{ Hz} \quad (8.74)$$

This value leads us to define the series resistor value, R_s :

$$R_s = \frac{1}{2\pi f_{z_1} C_{Vcc}} = \frac{1}{6.28 \times 303 \times 47\mu} = 11 \Omega \quad (8.75)$$

Together with the shunt regulator equivalent dynamic resistor, it creates a pole located at

$$f_{p_1} = \frac{1}{2\pi(R_s + R_d)C_{Vcc}} = \frac{1}{6.28 \times (11 + 15) \times 47\mu} = 130 \text{ Hz} \quad (8.76)$$

At this point, we need to calculate the LED series resistor we will choose. Applying (8.20) and replacing the parameter V_{out} by the Zener voltage, we find a maximum value of

$$R_{LED,\max} \leq \frac{\text{CTR}_{\min}(V_Z - V_f - V_{TL431,min})}{I_{C,\max} + I_{bias}\text{CTR}_{\min}} \leq \frac{0.8 \times (8.2 - 1 - 2.5)}{7m + 1m \times 0.8} \leq 482 \Omega \quad (8.77)$$

Assuming a 20 percent derating, we will pick a resistor of 385Ω . Knowing this value, we can now use (8.72) and obtain a value for R_2 :

$$R_2 = \frac{\frac{10}{163 \times 0.8} \times 385 \times 38k}{\sqrt{1 + (1k/130)^2}} \cdot \frac{\sqrt{1 + (1k/7k)^2}}{\sqrt{1 + (1k/303)^2}} \cdot \frac{\sqrt{1 + (1k/7k)^2}}{\sqrt{1 + (1k/303)^2}} = 234 \text{ k}\Omega \quad (8.78)$$

Having this resistor on hand, we can evaluate the value of C_1 to position the zero canceling the pole f_{p1} :

$$C_1 = \frac{1}{2\pi f_{z_2} R_1} = \frac{1}{6.28 \times 130 \times 234k} = 5.2 \text{ nF} \quad (8.79)$$

The other elements, C_3 and R_3 are found using (8.55) and (8.56), respectively, where R_{LED} in the first equation is simply replaced by R_1 :

$$C_3 = \frac{f_{p3} - f_{z3}}{2\pi R_1 f_{p3} f_{z3}} = \frac{7k - 303}{6.28 \times 38k \times 7k \times 303} \approx 13 \text{ nF} \quad (8.80)$$

Having C_3 , we can get the series resistor R_3 :

$$R_3 = \frac{1}{2\pi f_{p3} C_3} = \frac{1}{6.28 \times 7k \times 13n} = 1.7 \text{ k}\Omega \quad (8.81)$$

The compensator being ready now, let us check the Zener diode biasing resistor R_Z :

$$R_Z = \frac{(V_{out} - V_Z)\text{CTR}_{\min}}{I_{C,\max} + (I_{Zbias} + I_{bias})\text{CTR}_{\min}} = \frac{(12 - 8.2) \times 0.8}{7m + (3m + 1m) \times 0.8} = 298 \Omega \quad (8.82)$$

We now have everything, and we can use our test fixture as portrayed in Figure 8.14 to test our ac results. The bias points are correct and the Zener voltage features the right value. We can display the response delivered by this compensator in Figure 8.15. A good crossover point can be observed, exactly at 10 dB, as expected. The phase boost is almost 130°, what we wanted from the original specifications.

8.4 Isolated Zener-Based Compensator

Presented in the TL431 chapter, a Zener diode can be implemented to regulate the output voltage of a switcher-based converter. However, this option is valid only for a raw dc output, as the cumulated precision of the stacked elements can barely be better than 10 percent. The application schematic featuring a Zener-based compensator appears in Figure 8.16.

Starting from the feedback current expression already derived in (8.6), we have

$$I_{FB}(s) = I_C(s) \frac{R_s + \frac{1}{sC_{V_{cc}}}}{R_d + R_s + \frac{1}{sC_{V_{cc}}}} = I_C(s) \frac{\frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}}}{\frac{sC_{V_{cc}}(R_s + R_d) + 1}{sC_{V_{cc}}}} = I_C(s) \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \quad (8.83)$$

The collector current is linked to the LED ac current by the CTR. In this application, the dynamic resistor of the Zener diode R_{dZ} can no longer be neglected, as it can be as high as several tens of ohms, depending on the diode type and the biasing conditions. As a result, both the LED resistor R_{LED} and the Zener diode dynamic resistor R_{dZ} appear in series. Accounting for this fact, the LED ac current is

$$I_{LED}(s) = \frac{V_{out}(s)}{R_{LED} + R_{dZ}} = \frac{I_C(s)}{\text{CTR}} \quad (8.84)$$

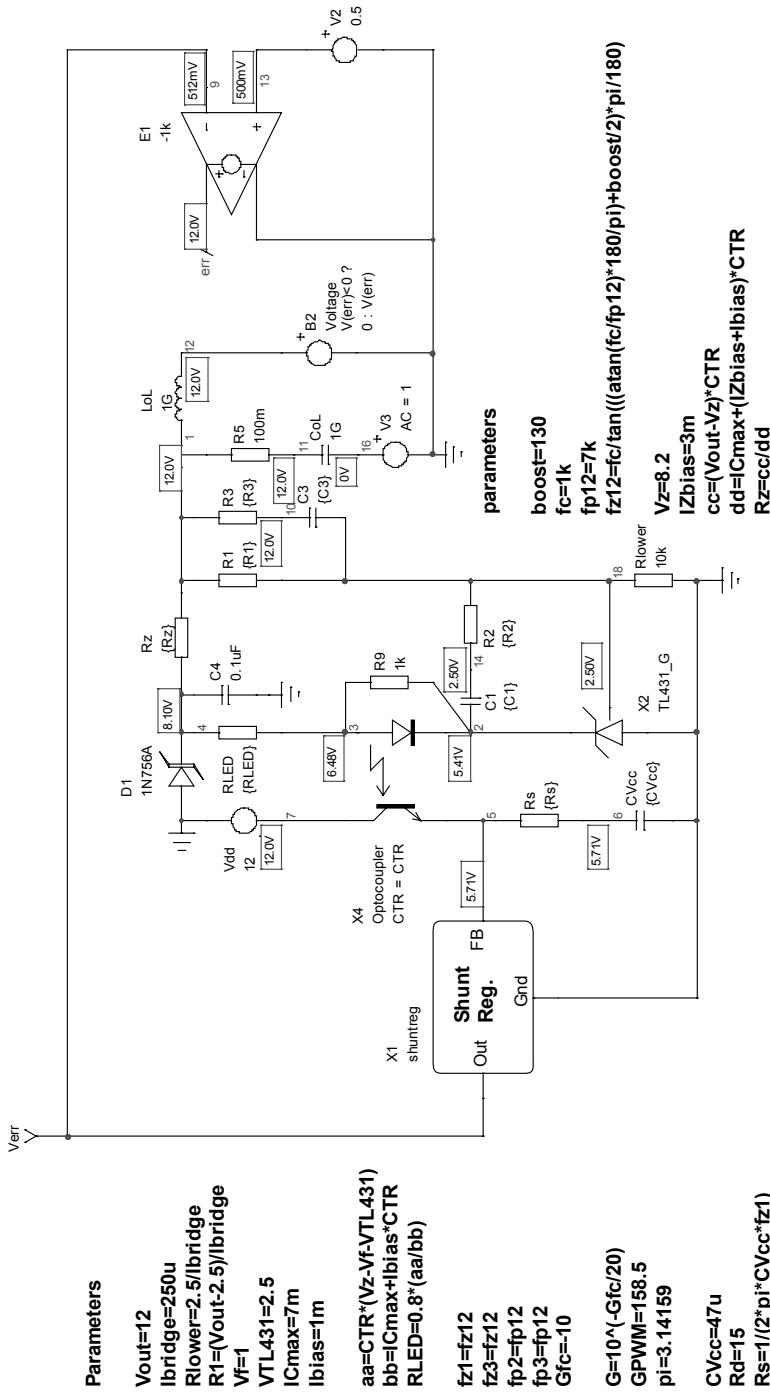


Figure 8.14 The test fixture automates the various component values and lets the user change his or her mind on the fly to test other poles/zeros combinations.

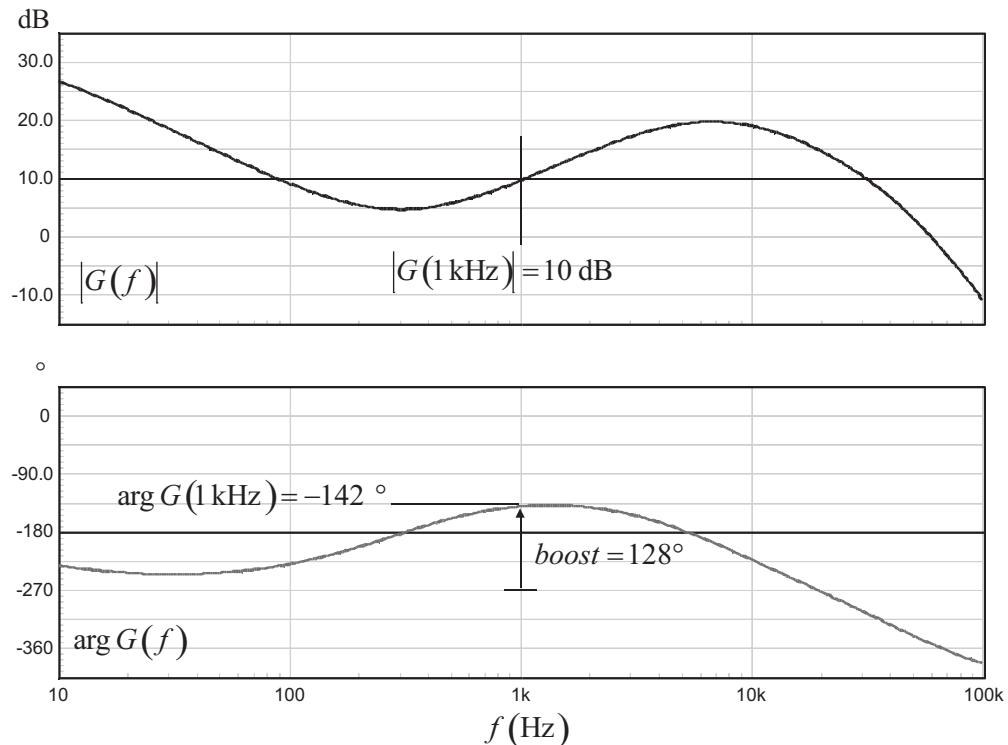


Figure 8.15 The ac response shows a good crossover point and a phase boost within specifications.

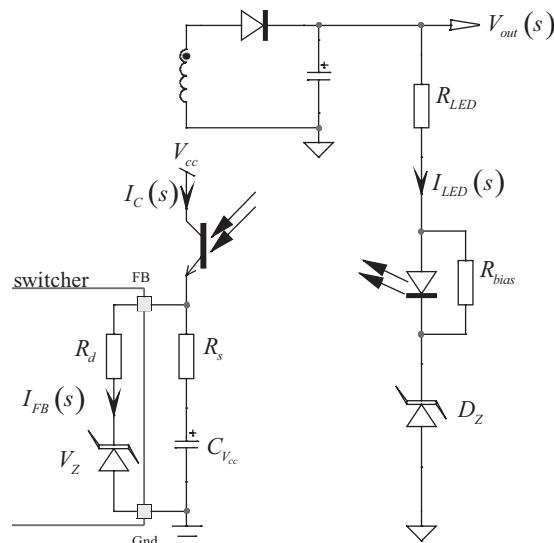


Figure 8.16 A Zener diode can be used in the secondary side to replace the TL431. This solution is only applicable when you expect a roughly regulated dc output level.

Extracting the collector current definition from (8.84) and substituting it in (8.83), we obtain a transfer function:

$$\frac{I_{FB}(s)}{V_{out}(s)} = \frac{\text{CTR}}{R_{LED} + R_{dZ}} \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \quad (8.85)$$

Combined with the internal modulator function given by (8.9), we have

$$\frac{D(s)}{V_{out}(s)} = -G_{PWM} \frac{\text{CTR}}{R_{LED} + R_{dZ}} \frac{sR_s C_{V_{cc}} + 1}{sC_{V_{cc}}(R_s + R_d) + 1} \frac{1}{1 + s/\omega_{p2}} = -G_0 \frac{1 + s/\omega_{z1}}{1 + s/\omega_{p1}} \frac{1}{1 + s/\omega_{p2}} \quad (8.86)$$

In this expression, we can identify

$$G_0 = \frac{\text{CTR}}{R_{LED} + R_{dZ}} G_{PWM} \quad (8.87)$$

$$\omega_{z1} = \frac{1}{R_s C_{V_{cc}}} \quad (8.88)$$

$$\omega_{p1} = \frac{1}{(R_d + R_s) C_{V_{cc}}} \quad (8.89)$$

$$\omega_{p2} = 44 \text{ krad/s} \quad (8.90)$$

We have double pole-single zero type of compensator. The pole and the zero defined by (8.88) and (8.89) are linked together since they share one common element, R_s :

$$\frac{f_{p1}}{f_{z1}} = \frac{1}{(R_s + R_d) C_{V_{cc}}} R_s C_{V_{cc}} = \frac{R_s}{R_d + R_s} \quad (8.91)$$

Unfortunately, they won't be of great help since they will cancel each other. It is, however, interesting to see how they influence the final phase lag. By definition, two poles and one zero bring the following argument:

$$\angle G(f_c) = \tan^{-1} \frac{f_c}{f_{z1}} - \tan^{-1} \frac{f_c}{f_{p1}} - \tan^{-1} \frac{f_c}{f_{p2}} \quad (8.92)$$

The first pole and the first zero are linked as shown by (8.91), and it is interesting to sweep the position of f_{z1} and see how it affects the total phase lag. First, we must update f_{p1} capitalizing on (8.88) and (8.89). From (8.88), R_s is extracted and substituted into (8.89). After some changes, we obtain

$$f_{p1} = \frac{f_{z1}}{2\pi C_{V_{cc}} R_d f_{z1} + 1} \quad (8.93)$$

When substituted into (8.92), we have an equation depending on f_{z1} only:

$$\angle G(f_c) = \tan^{-1} \frac{f_c}{f_{z1}} - \tan^{-1} \frac{f_c (2\pi C_{V_{cc}} R_d f_{z1} + 1)}{f_{z1}} - \tan^{-1} \frac{f_c}{f_{p2}} \quad (8.94)$$

It is now interesting to plot this formula for a given crossover frequency—let's say, 1 kHz—and see what recommendation we could extract on the zero placement. This is what Figure 8.17 portrays. As expected, the lower the zero, the less severe the phase lag

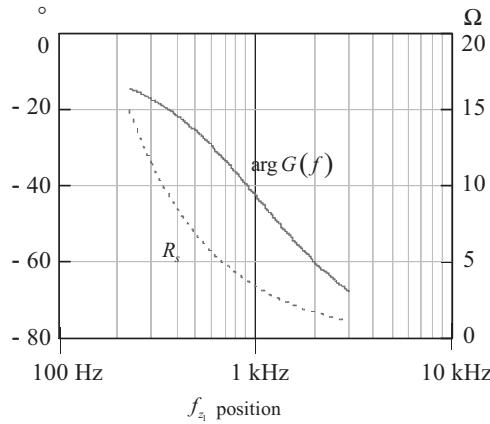


Figure 8.17 As the first zero slides in the low side of the spectrum, the total phase lag gets smaller.

is at 1 kHz. Given the recommendation on the series resistor R_s , whose value depends on the V_{cc} capacitor and the selected zero position, a value around 400 Hz looks like a good choice. The total phase lag at this point (-20°) cumulated with the phase reversal brought by the modulator chain will reach -200° . As indicated by Figure 8.6, at 1 kHz, the phase lag of the power stage is -70° , which when added to the -200° of the compensator should leave around 90° of phase margin at crossover ($360^\circ - 270^\circ$).

The output voltage of a converter stabilized by a Zener-based compensator will exhibit an output level equal to

$$V_{out} = V_Z + R_{LED}I_{LED} + V_f \quad (8.95)$$

The LED current will vary between two extremes, depending on the optocoupler CTR and the injected current in the feedback pin. At low output power, the injected current is maximum to reduce the duty ratio. At higher power conditions, the injected current is decreased to let the duty ratio increase:

$$I_{LED,max} = \frac{I_{FB,max}}{CTR_{min}} + I_{bias} = \frac{2.5m}{CTR_{min}} + I_{bias} \quad (8.96)$$

$$I_{LED,min} = \frac{I_{FB,min}}{CTR_{max}} + I_{bias} = \frac{7m}{CTR_{max}} + I_{bias} \quad (8.97)$$

If we consider the Zener voltage and the LED forward drop constant, the output voltage is likely to change depending on the loading conditions. Fortunately, as the LED series resistance is rather low by definition, the change will stay reasonable.

8.4.1 A Design Example

Suppose we have the following component values:

$V_{out} = 12$ V; the output voltage.

$V_f = 1$ V; the LED forward voltage.

$I_{bias} = 1 \text{ mA}$; the Zener biasing current when the optocoupler LED is paralleled with a resistor.

$\text{CTR}_{\min} = 0.8$; the minimum optocoupler current transfer ratio.

$\text{CTR}_{\max} = 1.2$; the maximum optocoupler current transfer ratio.

$C_{V_{cc}} = 47 \mu\text{F}$; the selected V_{cc} capacitor according to the switcher data sheet.

The power stage transfer function is that of Figure 8.6. For a 1-kHz crossover point, we need to push the gain up by around 4 dB. Before that, we need to calculate the series resistor value R_s to position a zero at 400 Hz, as agreed before:

$$R_s = \frac{1}{2\pi f_{z_1} C_{V_{cc}}} = \frac{1}{6.28 \times 400 \times 47\mu} \approx 8.5 \Omega \quad (8.98)$$

Associated with the shunt regulator input impedance of 15Ω , it leads to positioning the first pole at the following frequency:

$$f_{p_1} = \frac{1}{2\pi(R_s + R_d)C_{V_{cc}}} = \frac{1}{6.28 \times (15 + 8.5) \times 47\mu} = 144 \text{ Hz} \quad (8.99)$$

Having these values on hand, we can now derive the LED series resistor value from the magnitude of (8.86):

$$|G(f_c)| = \frac{\text{CTR}}{R_{LED} + R_{dZ}} G_{PWM} \frac{\sqrt{1 + (f_c/f_{z_1})^2}}{\sqrt{1 + (f_c/f_{p_1})^2}} \frac{1}{\sqrt{1 + (f_c/f_{p_2})^2}} \quad (8.100)$$

From this equation, we can extract the value of the LED resistor. The Zener dynamic resistor can be quickly characterized on the bench or its value can be extracted from the data-sheet parameters at a given bias current. The Zener diode we have selected exhibits a dynamic resistor of 10Ω for a bias current of 10 mA.

$$\begin{aligned} R_{LED} &= \frac{\text{CTR} G_{PWM}}{G} \frac{\sqrt{1 + (f_c/f_{z_1})^2}}{\sqrt{1 + (f_c/f_{p_1})^2}} \frac{1}{\sqrt{1 + (f_c/f_{p_2})^2}} - R_{dZ} = \frac{0.8 \times 163}{10^{20}} \\ &\times \frac{\sqrt{1 + (1k/400)^2}}{\sqrt{1 + (1k/144)^2}} \frac{1}{\sqrt{1 + (1k/7k)^2}} - 10 \approx 21 \Omega \end{aligned} \quad (8.101)$$

With a $21-\Omega$ resistor, we can calculate the corresponding voltage drops depending on the operating feedback conditions:

$$V_{R_{LED,\max}} = R_{LED} I_{LED,\max} = R_{LED} \left(\frac{2.5m}{\text{CTR}_{\min}} + I_{bias} \right) = 21 \times \left(\frac{2.5m}{0.8} + 1m \right) \approx 87 \text{ mV} \quad (8.102)$$

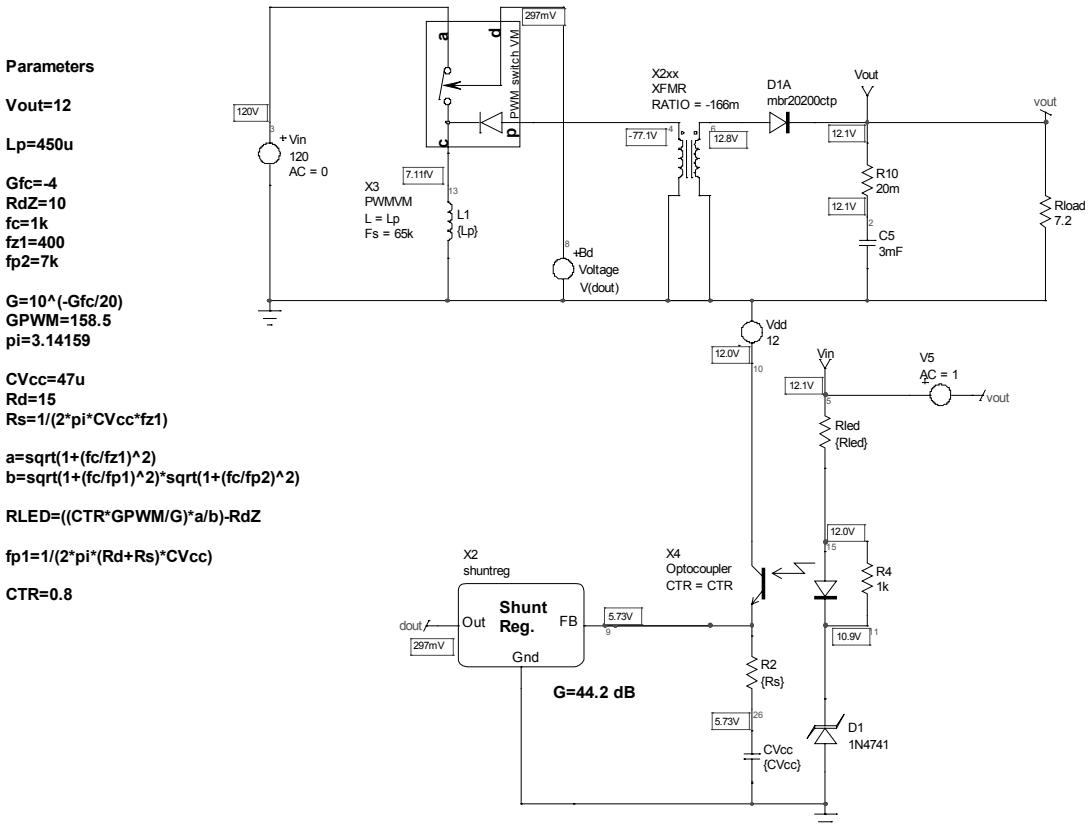


Figure 8.18 The flyback ac simulation fixture has been updated to implement a Zener-based compensator.

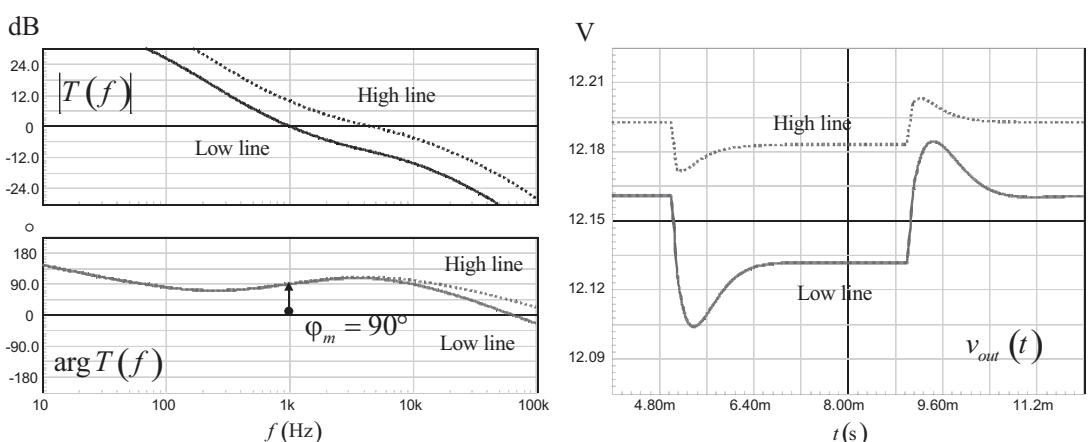


Figure 8.19 The open-loop gain shows a crossover frequency of 1 kHz with a comfortable phase margin of 90° , as expected.

$$V_{R_{LED},\min} = R_{LED}I_{LED,\min} = R_{LED}\left(\frac{7m}{CTR_{\max}} + I_{bias}\right) = 21 \times \left(\frac{7m}{1.2} + 1m\right) = 144 \text{ mV} \quad (8.103)$$

The average value between these two extremes is around 116 mV. Considering a 12-V output and a 1-V voltage drop for the LED, the Zener voltage has to be selected to the following value:

$$V_Z = V_{out} - V_f - V_{R_{LED}} = 12 - 1 - 116m \approx 11 \text{ V} \quad (8.104)$$

With these value selected, we can now use the converter simulation test fixture proposed in Figure 8.5 and update it with the Zener-based compensator. This is what Figure 8.18 shows.

The bias points are good, the output voltage reaches 12 V, and the duty ratio establishes to around 30 percent (297 mV on the *D* input of the average model X_3). By inserting the ac source with the LED series resistor, we can sweep the whole chain. Keeping the ac source in place, it is also possible to run a transient test and assess the response. Both ac and transient results appear in Figure 8.19 and confirm the 1-kHz crossover point, together with a 90° phase margin. The transient response improves as the input voltage changes since the crossover frequency at high line increases to nearly 4 kHz. Please note the slight output voltage dc change at both line extremes. This phenomenon finds its root in the duty ratio setpoint change. As the injected current changes, it induces a different voltage drops across R_{LED} which, summed with the Zener voltage and LED voltage drop, bring a change in the output level.

8.5 Conclusion

This last design example ends our study on shunt regulator-based compensators. Despite the presence of an internal 7-kHz pole, reasonable crossover targets can be achieved as long as one understands the design methodology. In particular, some iterations are necessary to check whether the selected crossover frequency is compatible with the available phase boost.

References

- [1] TOPSwitch data sheet, www.powerint.com.
- [2] TOPSwitch Tips Techniques and Troubleshooting Guide, Power Integrations AN-14.
- [3] Basson, C., *Switch Mode Power Supplies: SPICE Simulations and Practical Designs*, New York: McGraw-Hill, 2008.
- [4] Ridley, R., “Loop Gain Measurement with Current Injection,” *Switching Power*, 2005, <http://www.ridleyengineering.com>.

Appendix 8A: Summary Pictures

Figures 8.20 through 8.22 summarize the component definitions associated with the structures described in the chapter.

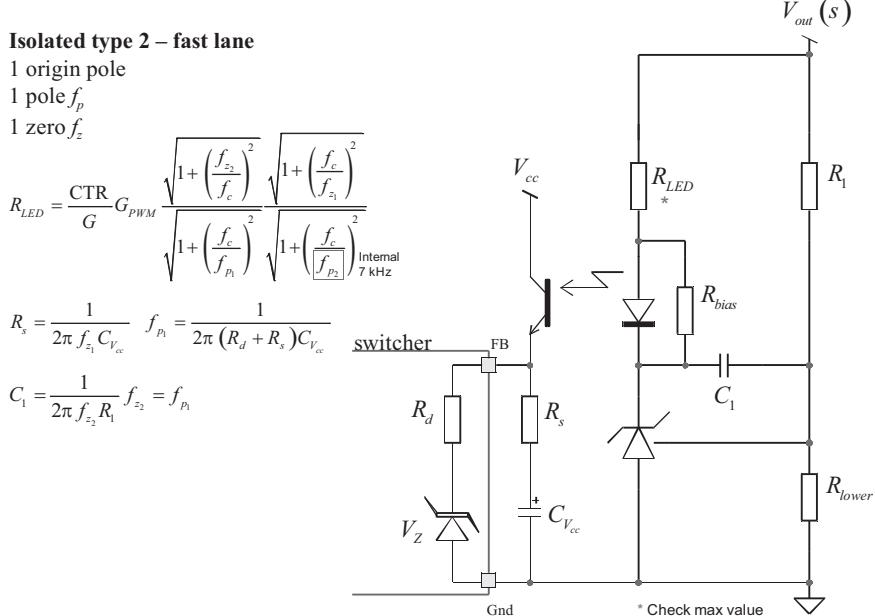


Figure 8.20 The isolated type 2 with fast lane.

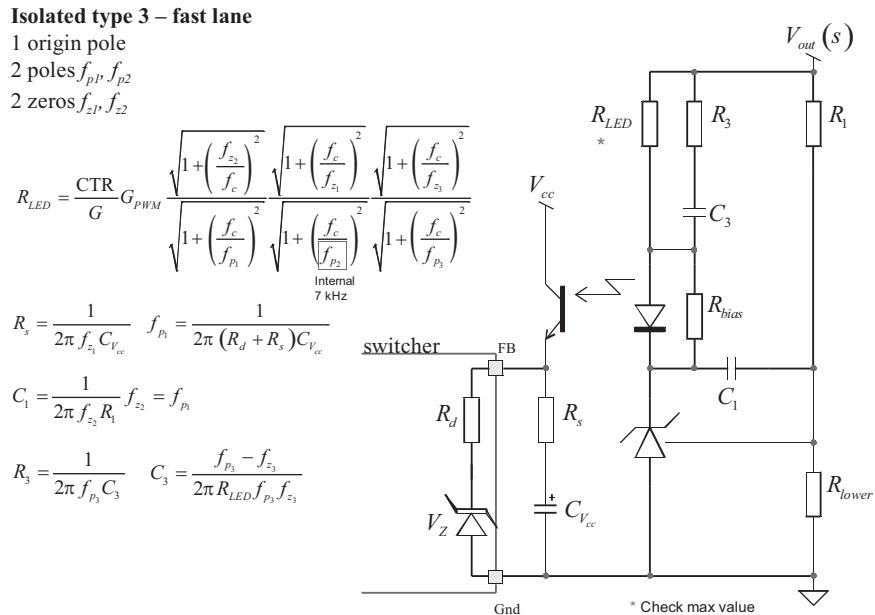


Figure 8.21 The isolated type 3 with fast lane.

Isolated type 3 – no fast lane

1 origin pole

2 poles f_{p1}, f_{p2} 2 zeros f_{z1}, f_{z2}

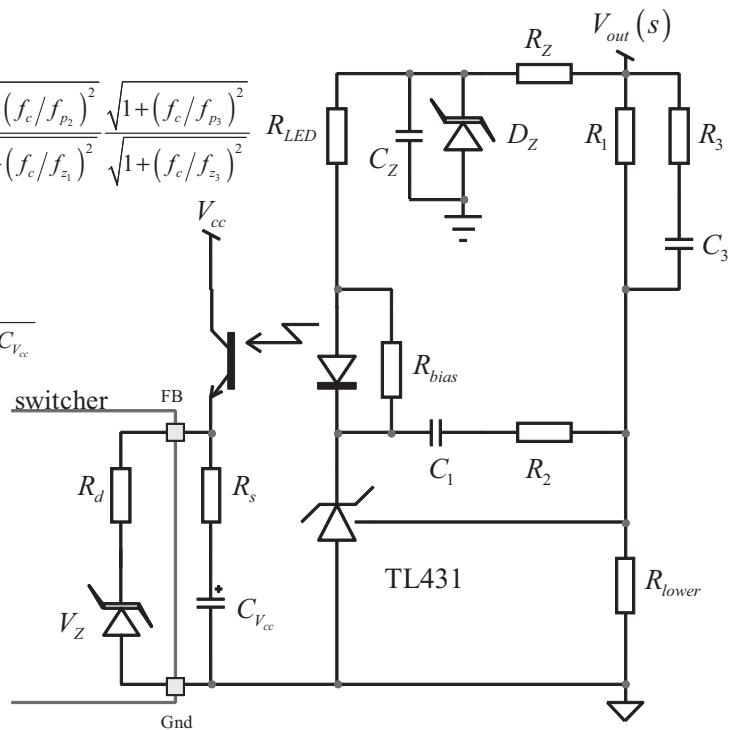
$$R_2 = \frac{GR_{LED}R_1}{G_{PWM} \text{CTR}} \frac{\sqrt{1+(f_c/f_{p1})^2}}{\sqrt{1+(f_{z2}/f_c)^2}} \frac{\sqrt{1+(f_c/f_{p2})^2}}{\sqrt{1+(f_c/f_{z1})^2}} \frac{\sqrt{1+(f_c/f_{p3})^2}}{\sqrt{1+(f_c/f_{z3})^2}}$$

$$R_Z = \frac{(V_{out} - V_Z) \text{CTR}_{\min}}{I_{C,\max} + (I_{Zbias} + I_{bias}) \text{CTR}_{\min}}$$

$$R_s = \frac{1}{2\pi f_{z_1} C_{V_{cc}}} \quad f_{p_1} = \frac{1}{2\pi(R_d + R_s)C_{V_{cc}}}$$

$$C_1 = \frac{1}{2\pi f_{z_2} R_1} \quad C_3 = \frac{f_{p_3} - f_{z_3}}{2\pi R_1 f_{p_3} f_{z_3}}$$

$$R_{LED,\max} \leq \frac{\text{CTR}_{\min} (V_Z - V_f - V_{TL431})}{I_{C,\max} + I_{bias} \text{CTR}_{\min}}$$

**Figure 8.22** The isolated type 3 without fast lane.

Measurements and Design Examples

Now that we understand why we need a compensator and how to design it, it is important to verify whether the prototype measurements on the bench comply with or at least approach our theoretical analysis. If not, then you need to understand where the discrepancy comes from so that you can update the analysis models with the new data. Let us start with the basics: how to open the loop on a prototype and measure the loop gain characteristics.

9.1 Measuring the Control System Transfer Function

In our quest to stabilize a control system, we have focused our energy on the open-loop gain transfer function analysis. However, once the control system operates, it is obviously in closed-loop conditions. To check if our theoretical approach was correct, we thus need a means to practically recreate the analysis conditions in which we purposely considered an open-loop path from the control input u to the output variable y . There are plenty of places in the control system where the return path can be broken. Two of them appear in Figure 9.1.

These are, however, block-based representations. We need a model closer to reality to understand what is at stake here. This updated model shows up in Figure 9.2. We see an op amp-based compensator whose error voltage V_{err} drives the control input of our power stage V_c . It can be a linear or switched converter—it does not change the picture. The loop can be opened either at the op amp output or in the resistive divider path. In both cases, there is a physical interruption of the return path and the control system no longer works as it should.

The loop can be broken for several reasons. For instance, you are at the beginning stage of your project and you need to extract the plant transfer function: there is no small-signal or analytical model for the converter under study. In this case, you want the plant Bode plot $H(s)$ to define the compensator structure given crossover and phase margin design goals. You can exclude the error amplifier and exclusively concentrate on the power stage frequency sweep first. This is the first method that we will explore.

The second option and the most popular one maintains the dc point by keeping the loop closed via a low-value resistor but offers the possibility to open the path in ac via the usage of a transformer. This is the best and most practical option you will use. Not only you will get the plant transfer function $H(s)$ but also the compensator $G(s)$ or the whole open-loop gain $T(s)$. Without this solution, exploring the loop gain, and thus combining H and G , it becomes extremely difficult, if not impossible, to maintain the control system in a linear and safe zone. It must be linear to avoid distortion when you ac modulate the circuit (possibly clipping the observed signal

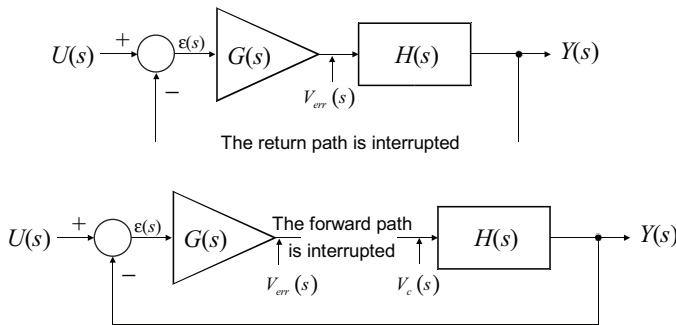


Figure 9.1 The analysis breaks the return path to observe the open-loop transfer function. Two possible examples where to break the loop.

because you are too close to the maximum or minimum output swing) and safe to avoid pushing the converter in one of its upper stops: a zero-volt output is probably okay but the output pushed to its maximum level is certainly dangerous. To avoid both scenarios, it is safer to apply the second method.

9.1.1 Opening the Loop with Bias Point Loss

When you physically open the loop, you obviously disturb the control system. How can it maintain its operating bias point to the targeted value if the return or direct path is broken? For instance, suppose you analyze a 12-V/1-A converter supplied from a 48-V input. If you open the loop, you will have to bias the power stage

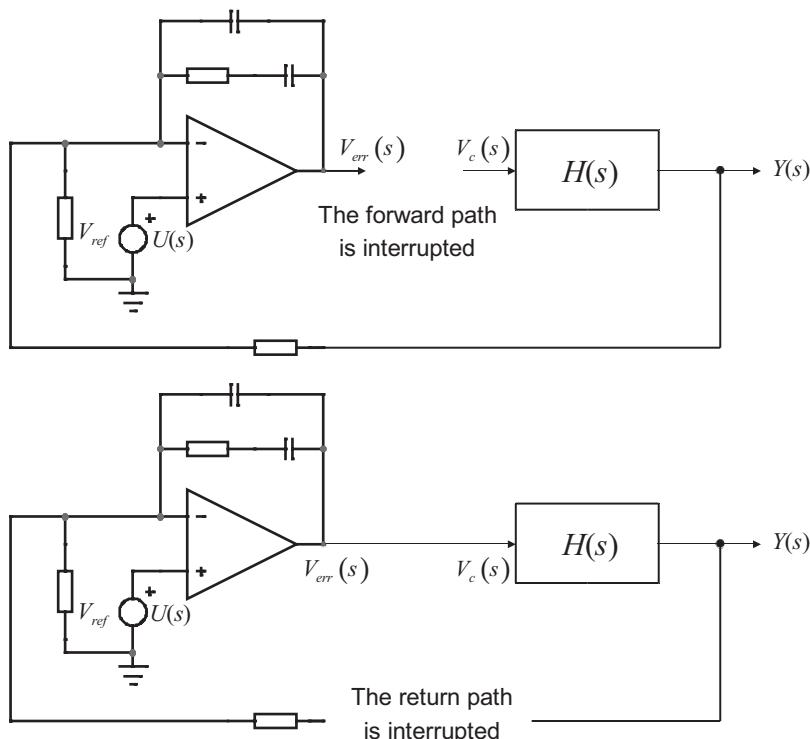


Figure 9.2 The op amp used in the compensator usually exhibits a large amount of gain.

control input so that it delivers the right output at the rated current. Then, once the dc bias is obtained, you will need to inject the ac modulation while observing its output. Ac injection can be done via an ac-coupling capacitor, for instance. This is the first method, described in Figure 9.3. The bias point is imposed by a resistive divider, which will give a finer control to bias the control input and provides impedance for the ac-coupling capacitor to modulate. In this example, we need 400 mV. Should you try to directly deliver this bias level via a dc source, it is very likely that the coarse output voltage adjustment makes the bias point setting a difficult exercise even more so since a switching power supply is a noisy place. It is best to drive the control input via a resistive divider. First, the $1\text{-k}\Omega$ pull-down resistor wired close to the control input will ensure a low driving impedance, minimizing susceptibility to noise. Second, rather than tweaking the bias output voltage to 400 mV, with a $47\text{-k}\Omega$ series resistor, you will adjust the dc source until you reach 12 V on the converter output, giving you a finer adjustment range than without the divider. The noise from the dc bias source will also be divided by the division ratio.

Once the converter output voltage has reached 12 V and delivers its 1 A current, you can hook an ac source through an ac-coupling capacitor and start the modulation. The ac source is part of a network analyzer. Such equipment is available from various manufacturers such as Ridley Engineering, Venable Instruments, or Omicron Lab. These devices also feature two inputs labeled A and B. Input A goes to the control input you sweep, while B observes the output signal. In Figure 9.3, as we want the plant transfer function, $H(s)$, A is connected to the converter control voltage and B collects the output signal data. The network analyzer will automatically plot

$$|H(f)| = 20 \log_{10} \left(\frac{|V_B(f)|}{|V_A(f)|} \right) \quad (9.1)$$

The modulating signal amplitude must be high enough so that the equipment can extract the useful signal from the noisy environment it is swamped in. However, it is important to keep the converter in a small-signal range. To verify this fact, hook

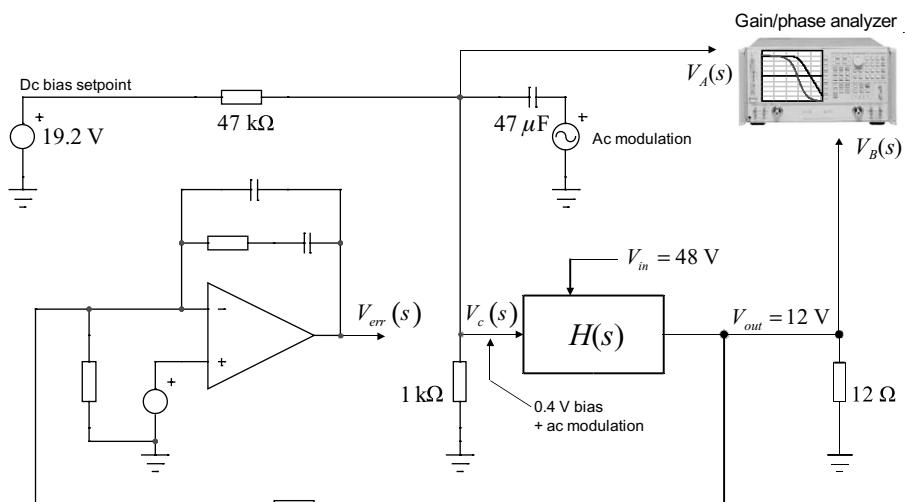


Figure 9.3 If you physically open the loop, you will have to externally force the converter at its operating bias point.

an oscilloscope probe to the output and tweak the modulating amplitude so that signal distortion is minimum (no clipping). No need to have the largest output signal; 1 to 5 percent of the output voltage is the kind of ac modulation amplitude you want. Let's see a practical example.

In Figure 9.4, we have shown an isolated flyback converter operated with a high-voltage controller, the NCP1200. The loop is physically open at the feedback pin level (the optocoupler is disconnected) and we apply an external dc bias via a recommended divider network, R_7 and R_8 . The ac modulation is coupled through capacitor C_4 . Pin 2 signal, actually the converter control voltage $V_c(s)$, connects to input A of the network analyzer. The output signal is collected on the secondary side of the converter and goes to input B of the measurement instrument. As with any high-voltage converter, a few precautions must be taken before you apply power:

- This converter is powered from the ac grid and deals with lethal high-voltage levels. To prevent electric shocks and conflicts with the equipment grounds (oscilloscope, analyzer), you have to power the converter from an *isolated* source. Either ac or dc is fine, but it has to be isolated from the ac grid. For these experiments, we usually power our converters from a dc source. We have used the Xantrex XHR600-1.7 for years, and it is very well suited for these kind of measurements. You can safely clamp its output voltage excursion below 400 V, and the maximum output current can be programmed. In case of short circuit in the board, you naturally limit the damages.

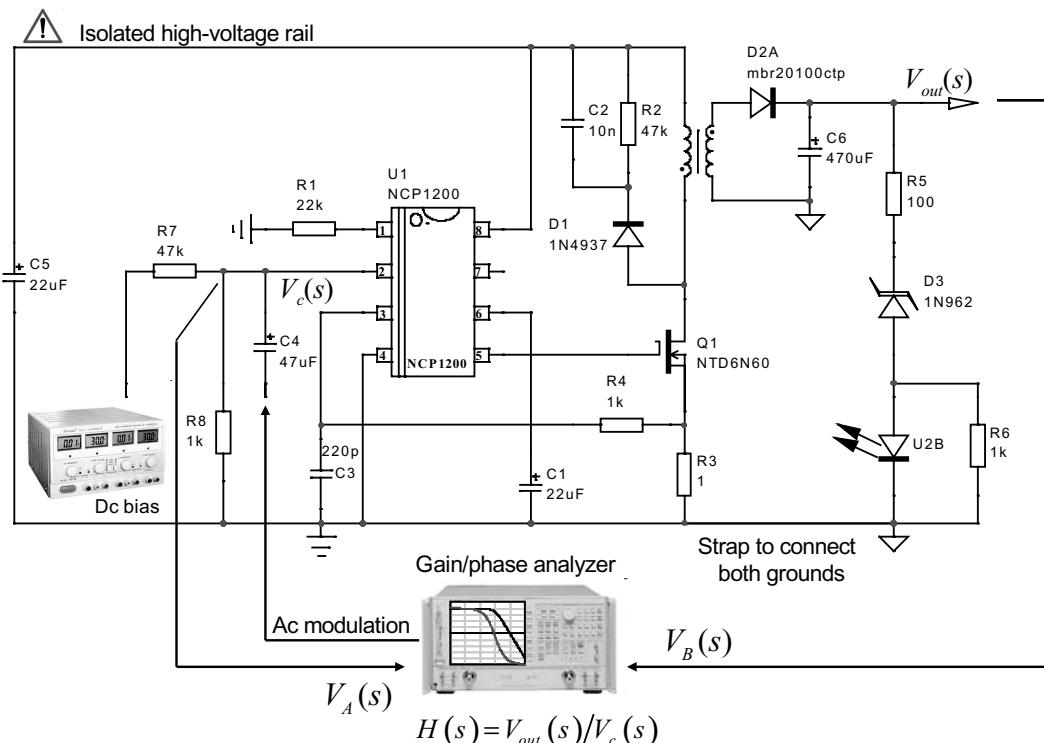


Figure 9.4 In this flyback example, the converter uses a popular current-mode controller, the NCP1200. The loop is open at the feedback pin level (pin 2).

- You are dealing with a converter whose secondary side is isolated from the primary side through an optocoupler. To allow the power stage transfer function measurement, you must tie the secondary and primary grounds together. This is the low-side strap shown in Figure 9.4. You now better understand why an isolation from the grid is an absolute necessity.
- Because the ac-coupling capacitor C_4 is discharged, you should not connect the network analyzer source while the power supply is operating, as you will disturb the dc bias brought by R_7 and R_8 and potentially generate an output transient. To avoid such issue, make sure the analyzer and its ac source are connected and running when you power up the converter.
- It is recommended to use a true resistive load on the output whenever you can. If you do not have access to the required high-power resistor, turn the electronic load into resistance mode and not constant-current mode. We found the constant-current operation could lead to erroneous measurement results.

Now that everything is running, you should be able to obtain a graph such as that of Figure 9.5. The converter was loaded to operate in a continuous conduction mode (CCM). The sweep started at 1 Hz to obtain the dc gain and ended at 100 kHz while the analyzer filter was set to 1 Hz. We started with an ac modulation amplitude of 100 mV and increased it to 250 mV to reduce the spurious noise on the graph. Make sure that changing the ac modulation amplitude reduces the noise

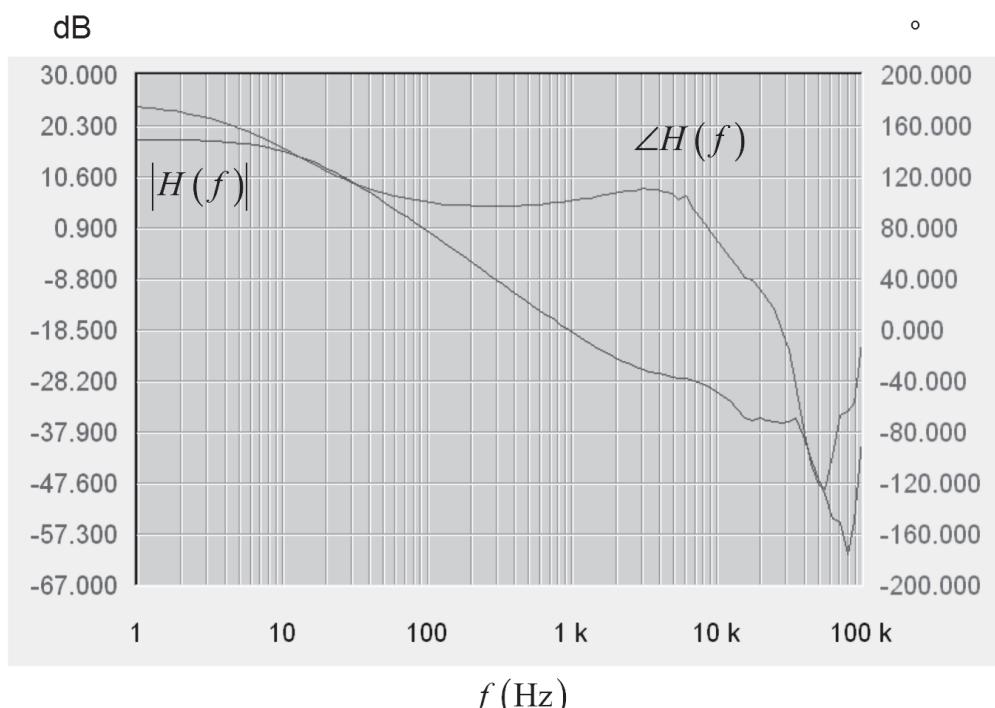


Figure 9.5 The typical ac response of a CCM flyback current-mode power stage.

but does not significantly change the overall response. Otherwise, it is indicative of a nonlinear operation at some point. As noted, if you visualize the output signal entering the analyzer and avoid clipping at all time, it is indicative of a linear operation, and you should be safe.

Measurement techniques require care and experience, especially in a noisy environment such as in a switching power supply. These techniques have been the objects of numerous publications, showing tips and tricks on how to get nice and reliable transfer function graphs. Please consult [1–6] at the end of this chapter for more information on the subject. All of these documents are available from the web.

The simple technique we presented lends itself well for low-gain power stages. Should you try to observe the error amplifier output (whether it is implemented with an op amp or a TL431), the technique becomes almost impossible to apply: any minor change in the dc control bias (noise, temperature drift, and so on), will push the error amplifier dc output in one of its stops (V_{cc} or ground) making an analysis impossible.

Loop interruption is also acceptable in converters where physically breaking the return path remains a safe operation, especially during the startup sequence. It is the case for most flyback-based converters of low to moderate output power levels. For more complex converters, especially high-power types, we do not recommend the physical opening of the loop.

9.1.2 Power Stage Transfer Function without Bias Point Loss

As explained, some converters do not accept the physical opening of their control loop. Sometimes, the converter is designed so a certain power-on sequence is fulfilled. In this case, a manual crank cannot easily be implemented. The case can also arise where the control input is not well accessible, and an opening represents a measurement risk. Fortunately, there is a simple technique that can be applied to a running converter without opening its loop. A typical secondary-side control system appears in Figure 9.6. It uses a TL431, but an op amp-based circuitry would keep the same approach.

The loop is normally closed, and you will disturb it by ac modulating the feedback pin in which impedance is given by the internal pull-up resistor R_4 . In this case, it is $20\text{ k}\Omega$. If you superimpose a modulation on this pin through capacitor C_3 , you will disturb the circuit around its operating point maintained by the TL431. Observing V_{out} and V_c will give you the plant Bode plot.

It is also possible to modulate the junction point of R_1 and R_2 with the network analyzer ac signal and plot the plant transfer function. A coupling capacitor will inject the signal at this point. This capacitor being initially discharged, you have to be careful, as brutally connecting the ac source will disturb the operating point and possibly engender an output overshoot. A 10-nF to 100-nF value should, however, be quickly charged and limit overvoltage risks. This technique keeps the operating point intact and lets you change the working conditions to measure the plant at different points. It does not let you explore the complete open-loop gain $T(s)$. However, if the cutoff frequency imposed by C_2 is too low, the high-frequency modulating signal cannot cross the transmission chain and the excitation at the control pin is drowned into noise. It then becomes difficult or impossible to extract

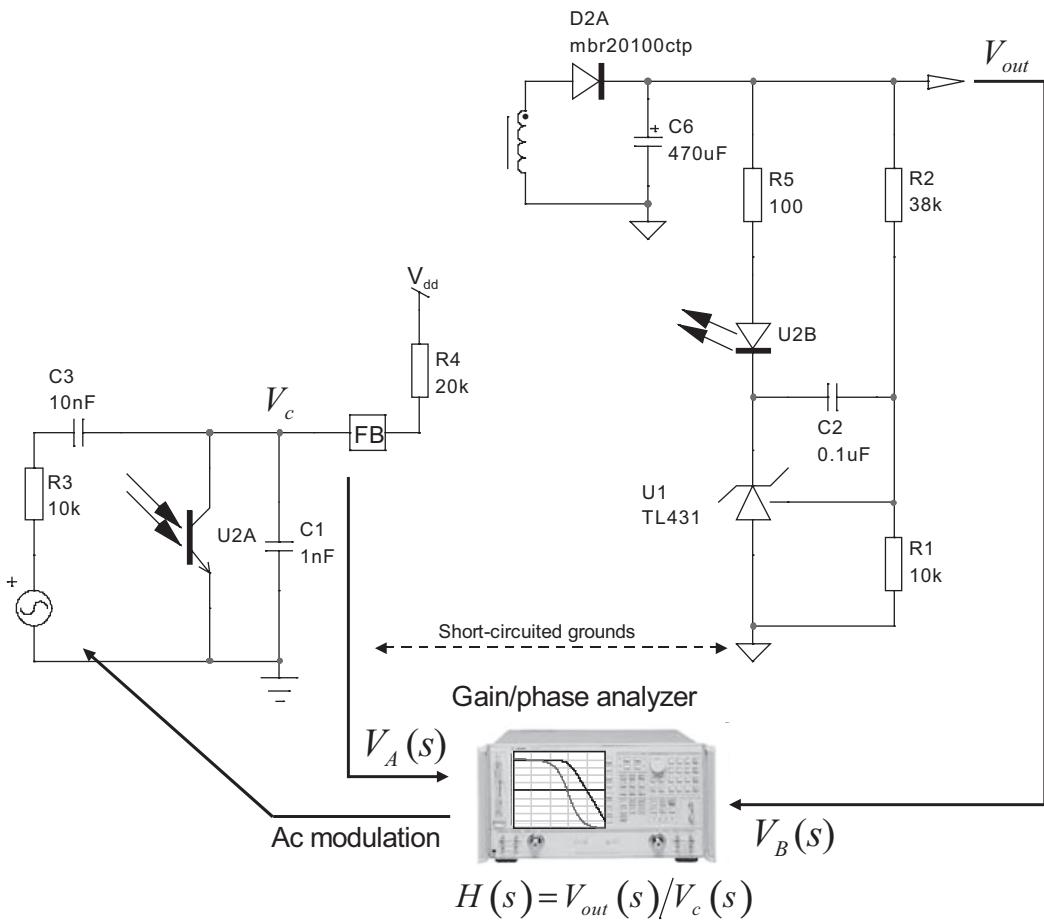


Figure 9.6 The loop is closed but can be perturbed by injecting a signal on the control pin FB.

the high-frequency gain, and you must either directly modulate the feedback pin or jump to the next paragraph.

9.1.3 Opening the Loop in ac Only

Keeping the operating point is important in an analysis, especially if you want to explore different working configurations: load changes, low or high input line, and so on. In any of these situations, the controlled variable (e.g., the output voltage) needs to be kept constant. If you apply the first method, where the loop is physically broken, any change in the input voltage or the loading conditions will require a duty ratio adjustment. You will do it manually via the external dc bias. When you want to cover numerous situations, it can quickly become a rather tedious exercise. By keeping the loop closed in dc, any change in the operating conditions will lead to a new operating point without any external tweak.

We have seen that we could keep the loop closed in dc as suggested in Figure 9.6 and unveil the plant transfer function. However, we could not graph the loop gain

$T(s)$. To maintain the dc point while probing whichever voltage transfer function we like, we need to apply an injection transformer-based method such as that described by Dr. Middlebrook in his founding paper. Please see [7] for details and download. The method preserves the dc point and does not require the physical interruption of the return path. Rather, it locally injects a series perturbation in the path across a resistor as documented in Figure 9.7.

The series resistor maintains the loop in a closed state. Its value typically ranges from 10 to 100 Ω and does not affect regulation. We have chosen 22 Ω in the example. Given the floating configuration of this resistor in both examples, we can only couple a ground-referenced ac source via a transformer. This is what the figure shows. This transformer applies the ac modulation signal across the resistor and is equivalent to the series insertion of a source in the loop. When brought back to a block-based drawing, we can easily picture this fact as illustrated in Figure 9.8. As the reference voltage (the control system setpoint) does not change during the ac sweep, its small-signal value is zero. The schematic simplifies to the lower part of Figure 9.8, which actually depicts a regulator. From this sketch, we can derive a few equations.

$$V_B(s) = -V_A(s)G(s)H(s) \quad (9.2)$$

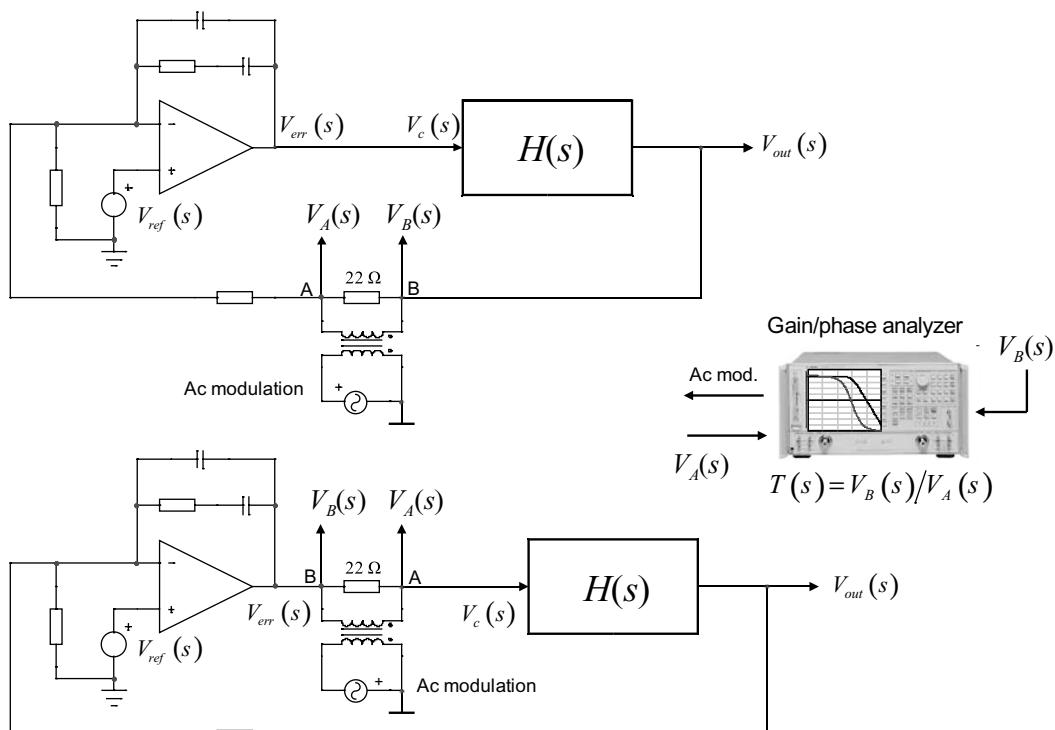


Figure 9.7 The perturbation is injected in series with the return or the direct path. The dc point is kept intact as no physical interruption occurs.

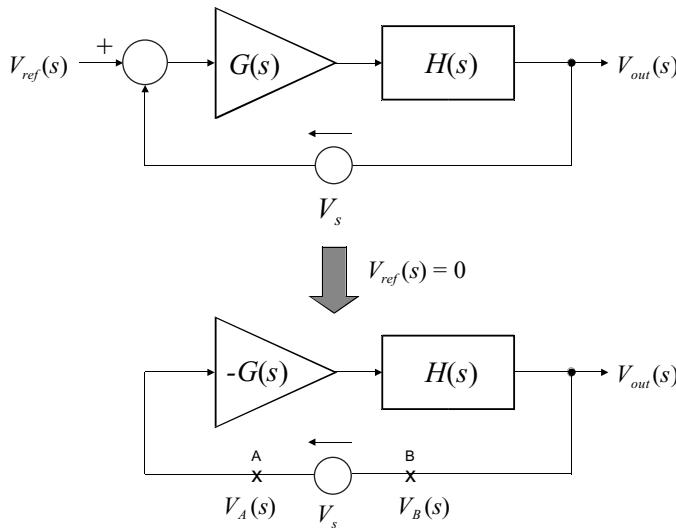


Figure 9.8 The inserted source appears like a perturbation in series with the returned information.

If we plot $V_B(s)/V_A(s)$, we have

$$\frac{V_B(s)}{V_A(s)} = -G(s)H(s) = T(s) \quad (9.3)$$

The minus sign illustrates what we already underlined in previous chapters. In the Figure 9.8 analysis, we naturally include the op amp phase reversal of 180° to which the loop gain argument (phase lag) is added. Therefore, the phase margin is no longer measured as the distance of the open-loop gain argument to the -180° limit but rather to -360° or 0° :

$$\varphi_m = \arg T(f_c) - 0^\circ \quad (9.4)$$

In this configuration, we can consider the sinusoidal voltages as rotating vectors shown in Figure 9.9. The magnitude of the vector (also called its modulus) is the sine wave amplitude, while its argument is the counterclockwise angle formed by the vector with the horizontal axis. You will find more information on this so-called phasor notation in Wikipedia, for instance. In our case, the difference between the

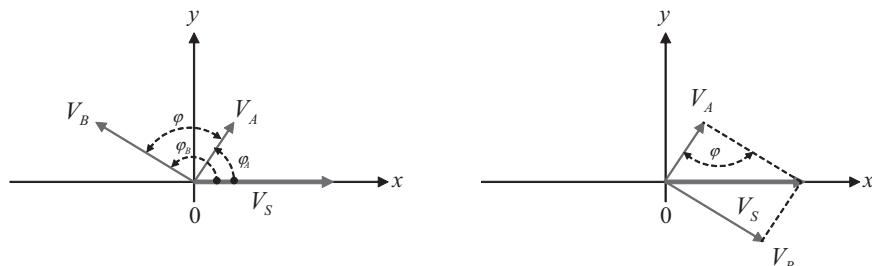


Figure 9.9 The vector sum of A and B signals is constant and equal to the modulating source amplitude V_S .

injected signal in A and the returned signal in B is constant and always equates the source amplitude. We can therefore write

$$\vec{V}_s = \vec{V}_A - \vec{V}_B \quad (9.5)$$

The phase difference between these two signals is nothing other than the difference of the vectors arguments:

$$\angle \vec{B} - \angle \vec{A} = \varphi_B - \varphi_A = \varphi \quad (9.6)$$

On the left side of Figure 9.9, we have drawn the reference vector \vec{V}_S —the ac modulation—and the signals generated at points A and B. They are, respectively, affected by arguments φ_A and φ_B , the angle formed by the vector with the x -axis. From this picture, graphically drawing (9.5) is equivalent to summing:

$$\vec{V}_S = \vec{V}_A + (-\vec{V}_B) \quad (9.7)$$

This is what we did on the right side to show that the result equals the amplitude of vector V_S .

The vector sum of V_A and V_B always satisfies the right side of Figure 9.9. This is the key of operation. Therefore, if V_B changes in amplitude, as the loop gain magnitude and argument also vary, V_A automatically adjusts to keep the constant value imposed by V_S . To illustrate this operating principle, we have run a buck converter simulation template such as that of Figure 9.10. A ground-referenced VCO sinusoidal source sweeps the frequency between 10 Hz and 40 kHz. This source is transformed into a floating stimulus via the B-element B1 that scales down the 1-V source to 20 mV. The ac sweep results appear in Figure 9.11.

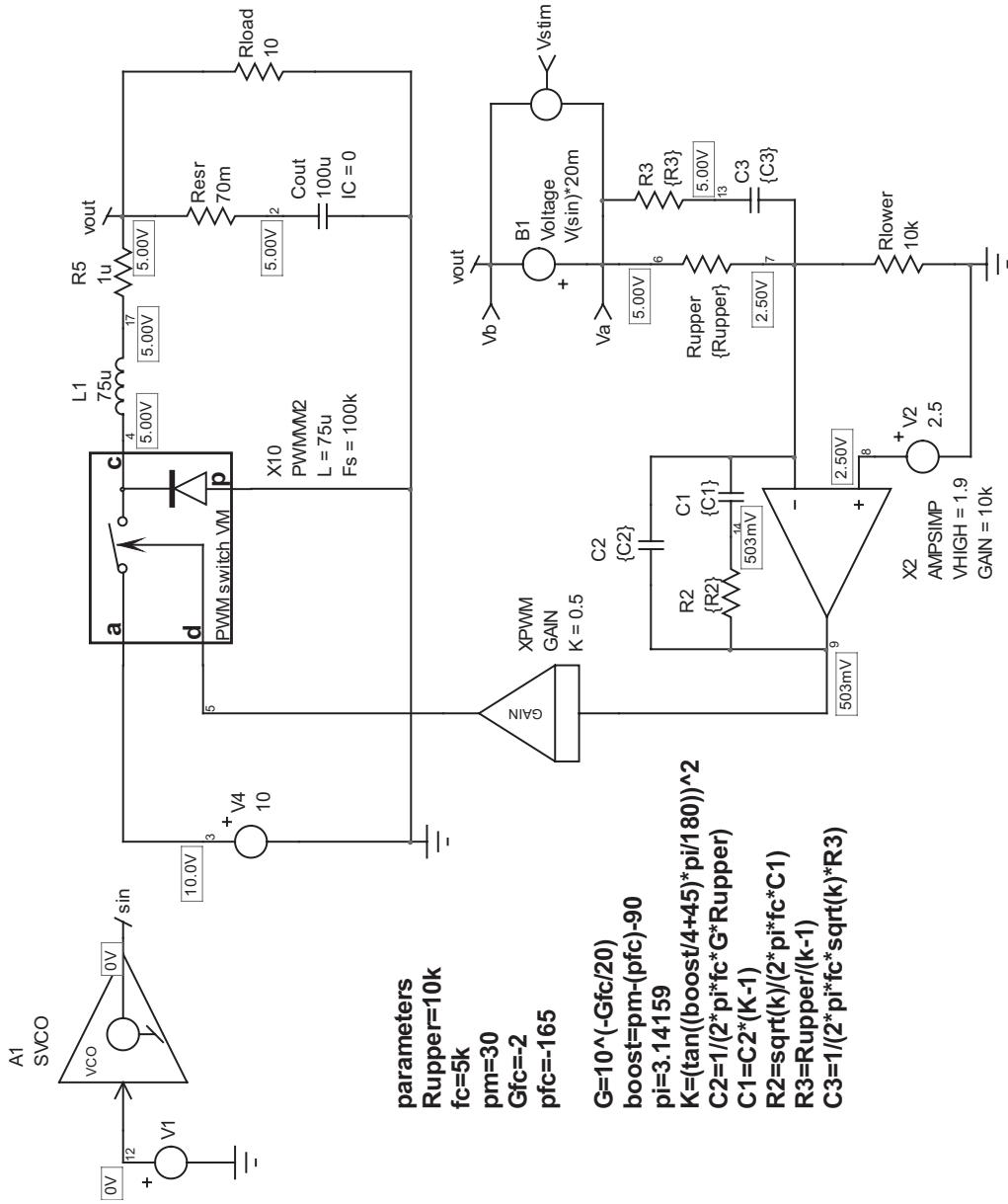
At low frequency, the dc gain is extremely high. Therefore, a small amplitude at point A is sufficient to generate a generous output signal at point B. When the crossover frequency approaches, both amplitudes tend to equalize. Exactly at crossover, they are equal, and the phase difference between both signals is our phase margin φ_m . As the frequency increases beyond crossover, the loop gain diminishes, asking for more signal at point A. Zooms of Figure 9.11 appear in Figure 9.12 and confirm the explanations. In the middle of the figure, the frequency is 4.97 kHz and the phase angle between the signals is:

$$\varphi_m = \frac{17}{201} 360 = 30.4^\circ \quad (9.8)$$

These numbers are in agreement with the calculated parameters in Figure 9.10 left-side template: 5 kHz crossover with a 30° phase margin.

9.1.4 Voltage Variations at the Injection Points

If you observe Figure 9.11, you can see a kind of peaking on signals A and B, at the left side of the graph. This peaking is direct a consequence of (9.5) that must always be satisfied. As such, the amplitude at points A and B permanently adjusts to satisfy this requirement (see [8] for an animated graph). However, as shown in Figure 9.12, the amplitude of one of the signals can shrink to an extremely low value. A few mV



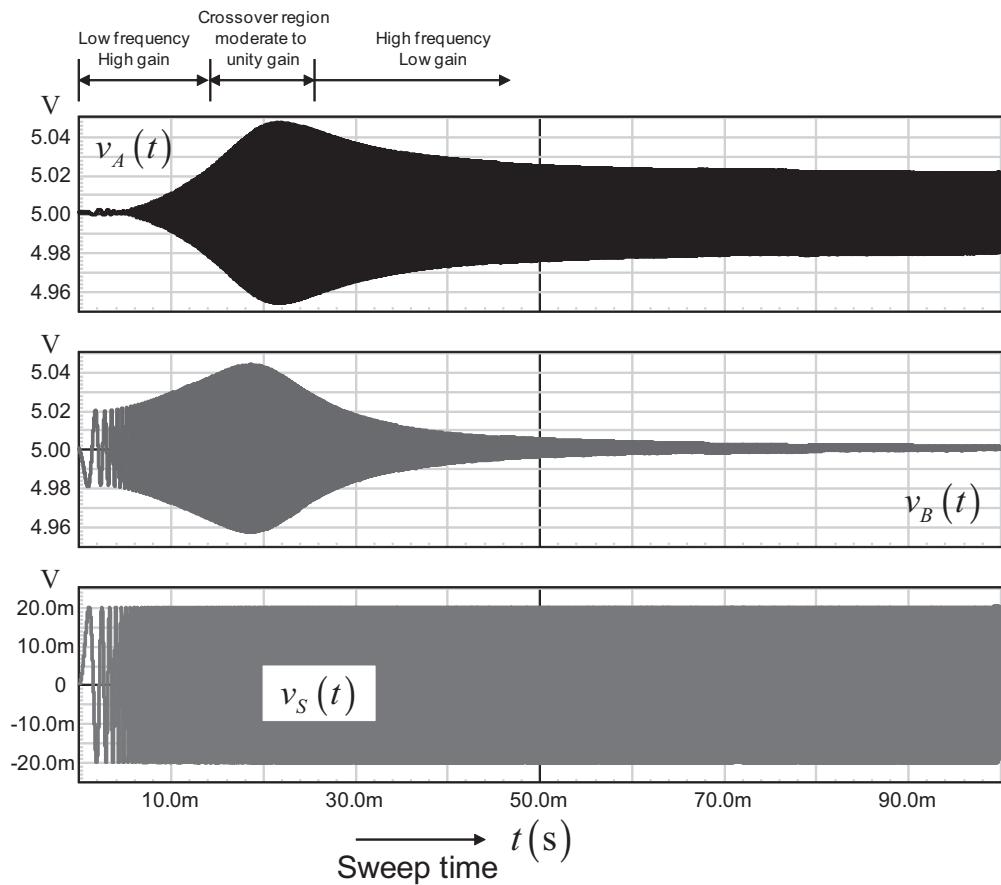


Figure 9.11 This graph shows how the control system permanently adjusts the A and B signals to maintain a constant ac source amplitude.

for signal A appear in the upper portion of the graph (low frequency, well below crossover) and around 1 mV for the low side of the plot (beyond the crossover frequency). How can we explain these changes?

There are two ways to look at the phenomenon. The first one deals with a simple block representation, actually rewriting equations around Figure 9.8. The basis is the simple Laplace equation linking points A and B amplitudes to the modulating signal:

$$V_S(s) = V_A(s) - V_B(s) \quad (9.9)$$

From this expression, we can easily extract the definitions of V_A and V_B :

$$V_B(s) = V_A(s) - V_S(s) \quad (9.10)$$

and

$$V_A(s) = V_S(s) + V_B(s) \quad (9.11)$$

To graphically represent these expressions, we have rearranged Figure 9.8 the way we propose in Figure 9.13.

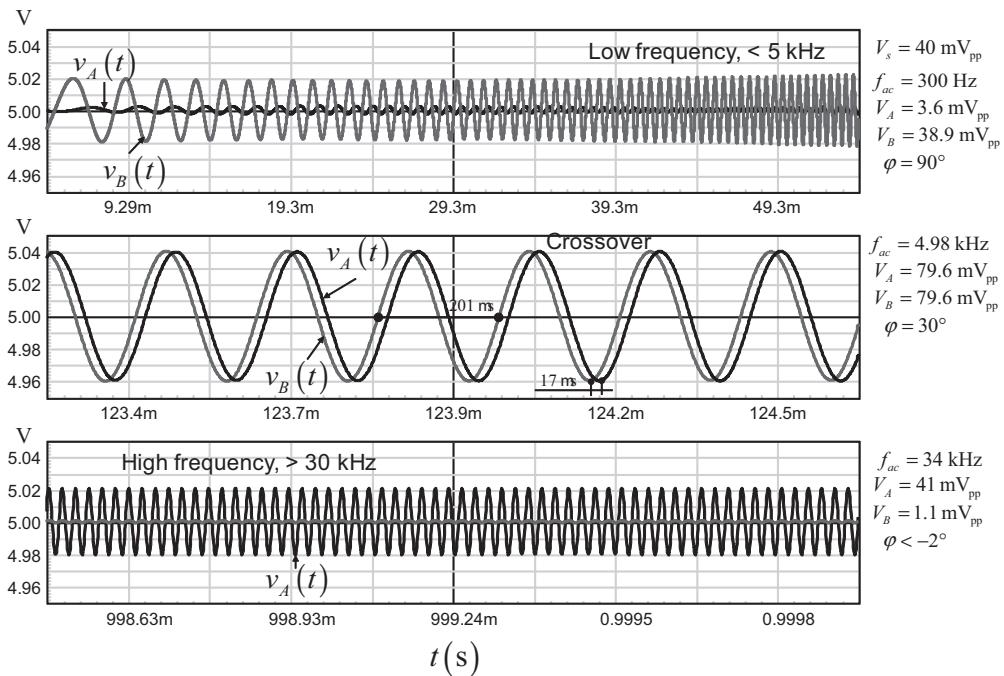


Figure 9.12 The signals amplitude are exactly equal at crossover and allow the phase margin measurement.

From this new picture, considering the inverting sign in the loop gain expression, we can write

$$V_B(s) = V_A(s)T(s) = T(s)[V_S(s) + V_B(s)] \quad (9.12)$$

$$V_B(s)[1 + T(s)] = T(s)V_S(s) \quad (9.13)$$

Finally, we have for V_B :

$$V_B(s) = V_S(s) \frac{T(s)}{1 - T(s)} \quad (9.14)$$

For V_A , the exercise remains similar:

$$V_A(s) = V_S(s) + V_B(s) = V_S(s) + V_A(s)T(s) \quad (9.15)$$

$$V_A(s)[1 - T(s)] = V_S(s) \quad (9.16)$$

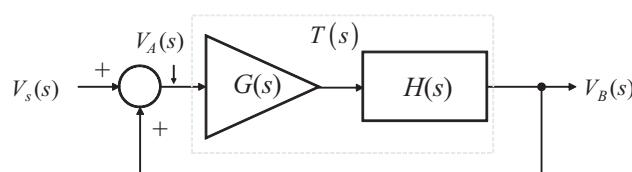


Figure 9.13 This simple representation lets us express V_A and V_B levels easily.

which leads to the following expression for V_A :

$$V_A(s) = V_S(s) \frac{1}{1 - T(s)} \quad (9.17)$$

At very low frequency, the open-loop gain is important, several tens if not hundreds of decibels for an op amp-based circuit. In that case, (9.14) tells us that the output voltage V_B is almost that of the source level and phase reversed. On the contrary, the voltage at point A is extremely small as indicated by (9.17). Actually, the term multiplying V_S should ring a bell: the sensitivity function S tackled in Chapter 3. This function tells you how efficiently a system can reject a perturbation. Indeed, the insertion of the ac modulation is a perturbation that bothers the control system, which tries to reject it as much as it can. It succeeds at low frequency where the gain is strong. This is why the amplitude at point A is naturally small, almost drowned in the noise floor in high-gain systems. We will see that it is almost mandatory to increase the ac modulating source amplitude to make sure the analyzer can extract the signal. When T gets smaller as you slide the frequency axis, you will have to decrease this amplitude to avoid nonlinear operation since the rejection capability becomes weaker. Working with an analyzer that authorizes such source amplitude modulation is an obvious advantage.

The second explanation goes back to vector representation. Figure 9.14 graphs how the vectors sum up at three different frequencies: close to dc, at crossover, and beyond.

At dc, we know that the signal at point B in relation? to the modulating source is out of phase. It is represented as a horizontal vector pointing to the left if vector V_S is horizontal and points to the right. The signal at point A, in our compensation case, is delayed by 90° . Remember our ac plots with a type 3 compensator: we have the 180° of the inverting op amp (or -180° if you wish) and the -90° of the origin pole. The total argument at dc is therefore 90° or -270° . The vector sum of these two signals must equate the magnitude of the modulating signal V_S . At low frequencies, the loop gain is extremely high. Therefore, a small modulating signal at point A is sufficient to get a signal at point B. As both signals are affected by a 90° shift while vector B is horizontal, the only way to construct the vector sum is to have B of almost equal amplitude of the modulating signal while vector A magnitude is extremely small. The drawing in Figure 9.14(a) shows these signals where we purposely changed a little bit the argument of signal B; otherwise, vector A would

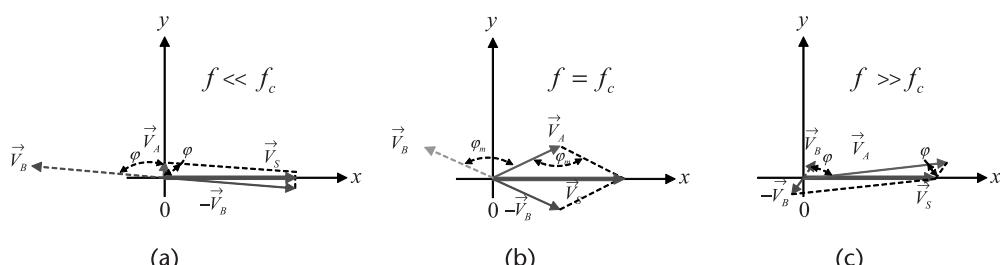


Figure 9.14 The amplitude of A and B adjusts depending on the phase difference between the signals. Their vector sum is constant and equal to the ac source magnitude V_S .

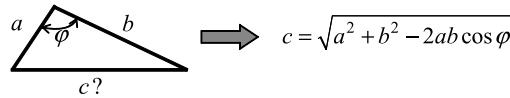


Figure 9.15 The Al-Kashi theorem works for all triangles, included right angled.

be invisible in the drawing. You have an idea of the signals amplitude on the right side of Figure 9.12.

At crossover, as expected, both signals amplitudes are similar since the magnitude of T at this frequency is 1. The phase between the two signals is the converter phase margin φ_m . The graphical representation appears in Figure 9.14(b). In this drawing, the phase margin is greater than 90° , and the amplitude of signals A and B is smaller than that of V_s . However, if you look back at comments in the middle of Figure 9.12, you see that the signals amplitudes exceed that of the source V_s by a ratio of two. How can it be?

To understand the phenomenon, we need to involve a theorem proposed by Persian scientist Al-Kashi (14th century). It is the generalization of the Pythagorean theorem and applies to any type of triangle.

Figure 9.15 represents a simple triangle where none of its angles is 90° . As indicated in the figure, the length c can be computed knowing the cosine of the angle φ . When this angle reaches 90° , the formula reduced to that of Pythagoras. This formula can be applied to our signal vectors, as drawn in Figure 9.16.

By applying Al-Kashi theorem, we immediately have:

$$|\vec{V}_S| = \sqrt{|\vec{V}_A|^2 + |\vec{V}_B|^2 - 2 \cdot |\vec{V}_A| \cdot |\vec{V}_B| \cos \varphi} \quad (9.18)$$

V_A and V_B magnitudes are linked by the open-loop gain T :

$$|\vec{V}_B| = |\vec{V}_A| \cdot |T(s)| \quad (9.19)$$

And the angle φ is nothing more than the loop gain argument at the considered frequency. Combining the previous equations, we can extract the individual values of V_A and V_B as:

$$|V_A(s)| = \frac{|V_S(s)|}{\sqrt{1 + |T(s)|^2 - 2|T(s)| \cos(\arg T(s))}} \quad (9.20)$$

$$|V_B(s)| = \frac{|V_S(s)|}{\sqrt{1 + \frac{1}{|T(s)|^2} - \frac{2}{|T(s)|} \cos(\arg T(s))}} \quad (9.21)$$

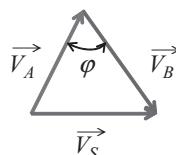


Figure 9.16 The signal amplitudes can be computed knowing the phase angle between the signals.

If we now consider the crossover frequency, it is a special case where both signal amplitudes are equal and the loop gain is 1. From (9.20), we can write:

$$|V_A(s)| = \frac{|V_S(s)|}{\sqrt{2 - 2\cos(\varphi_m)}} = \frac{|V_S(s)|}{\sqrt{2}\sqrt{1 - \cos(\varphi_m)}} \quad (9.22)$$

From our school courses, we can remember that:

$$\sin \frac{\varphi}{2} = \sqrt{\frac{1 - \cos \varphi}{2}} \quad (9.23)$$

From which we extract:

$$\sqrt{1 - \cos \varphi} = \sqrt{2} \sin \frac{\varphi}{2} \quad (9.24)$$

If we substitute this definition in (9.22), we have:

$$|V_A(s)| = |V_B(s)| = \frac{|V_S(s)|}{2 \sin \frac{\varphi_m}{2}} \quad (9.25)$$

Using this definition, we can now plot the amplitudes' evolution in relation to the phase margin at crossover. The graph appears in Figure 9.17. As we can see, a phase margin of 30°—as the one used in the Figure 9.10 template—gives a signal amplitude of 79 mV, very close to what we measured in Figure 9.12.

If we go back to our vector representations and combine again signal A and B of equal amplitudes but affected by three different phase margins, we obtain the drawing shown in Figure 9.18. In Figure 9.18(a), the margin is large, greater than 90°. The phase margin decreases in the middle and the vectors magnitudes have

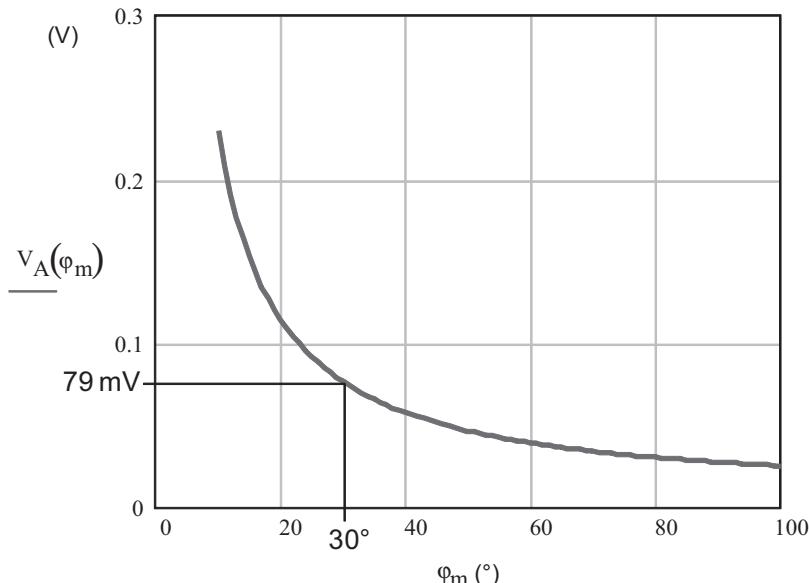


Figure 9.17 As the phase margin decreases at crossover, the signals' amplitudes tend to grow. At zero phase margin, their amplitude is theoretically infinite, indicative of an unstable system.

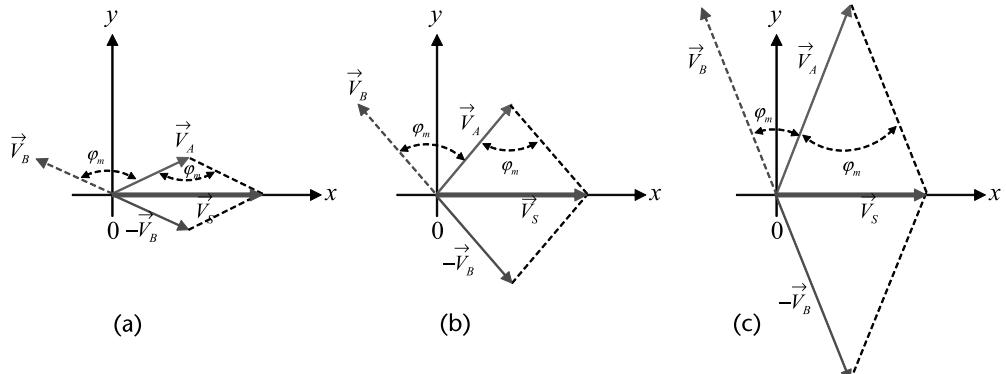


Figure 9.18 This simple drawing clearly illustrates how both V_A and V_B amplitudes run away as the phase margin reduces.

already grown. In Figure 9.18(c), the phase margin is even smaller and the vectors magnitudes exceed that of V_S .

With these two approaches, you now understand why the signals at points A and B change in amplitude across the frequency swept by the analyzer.

As explained, as our switching power supply is a noisy environment, a signal of low amplitude at point A can easily be drowned in the noise, leading to a poor signal-to-noise ratio. It is thus very common to increase the modulating signal in the low frequency portion of the analysis to improve the noise figure. This is particularly true for very high dc gain systems, where sometimes a modulating signal of several volts is necessary: remember, the higher the gain, the more difficult it is to shake the closed-loop system! Then, as crossover is approached, the amplitude must be seriously reduced. If it is not, overmodulation distortion can occur and the ac plot accuracy is affected. Most of the available network analyzers allow the user to adjust its ac modulation amplitude by segments. A typical amplitude pattern is given in Figure 9.19.

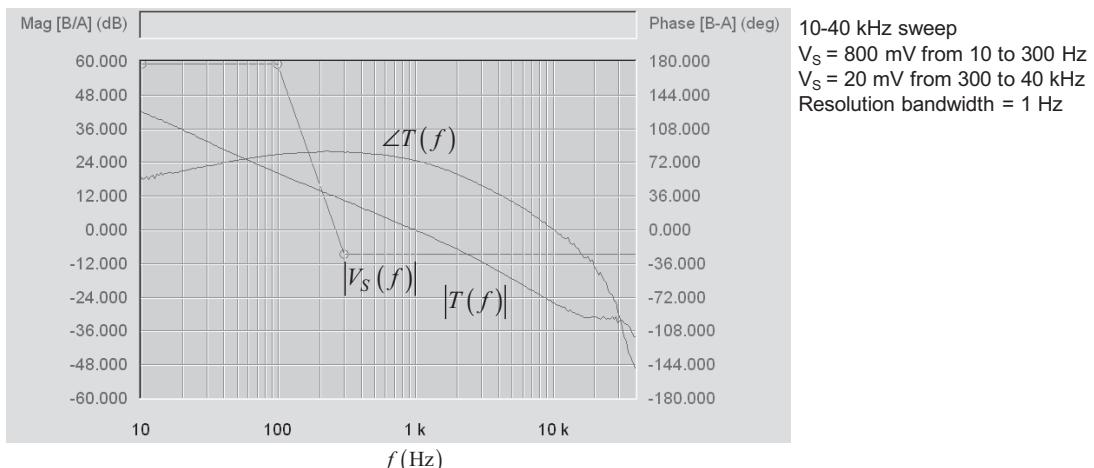


Figure 9.19 To ensure a good signal-to-noise ratio, the network analyzer lets you adjust the modulating signal ac amplitude along the frequency axis. Here is a screenshot obtained with an AP300 analyzer from Ridley Engineering.

It is not detailed here, but prior to any measurements you need to calibrate the probes across the frequency range of interest. It is an essential step to ensure correct results.

9.1.5 Impedances at the Injection Points

You can measure the loop gain by either physically interrupting the loop or by virtue of inserting a stimulus in series with the return path. In both cases, you need to consider the impedances at stakes when interrupting the path. They are the output impedance of the converter where you observe the controlled variable and the input impedance at the considered error amplifier. Let's look at Figure 9.20, where we interrupted the path at the error amplifier output. If we write the control to error transfer function, we will obtain the following expression:

$$T(s) = \frac{V_{err}(s)}{V_c(s)} = -G(s)H(s) \frac{Z_{out}(s)}{Z_{out}(s) + Z_{in}(s)} \quad (9.26)$$

This is the true loop gain affected by the impedances linking the output to the error amplifier input.

We learned in Figure 9.7 that the ac source could also be placed in series somewhere in the return path. To do that, we interrupt the wire between points A and B to insert the modulating source. Before the insertion, A and B were sharing a similar potential as they were connected together. With the source insertion, this relationship is no longer true: point B now drives point A with the ac source in series. What matters now is the impedance relationship between point A and B. Figure 9.21 updates Figure 9.20 by inserting the stimulus at points A and B.

To see the effects of these impedances, let's derive a few equations:

$$V_c(s) = -V_A(s)G(s) \quad (9.27)$$

$$V_B(s) = V_c(s)H(s) - Z_{out}(s)I_1(s) \quad (9.28)$$

The input current is simply:

$$I_1(s) = \frac{V_A(s)}{Z_{in}(s)} \quad (9.29)$$

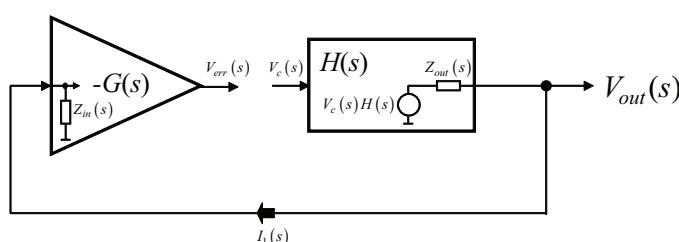


Figure 9.20 The loop is physically opened, but the resistive divider brought by the output/input impedances can alter the measurement.

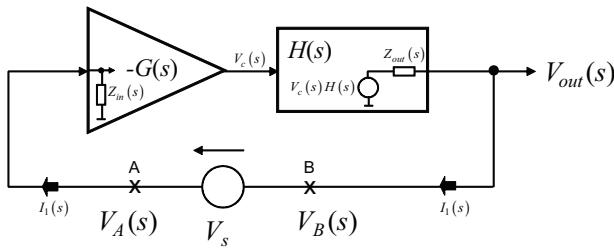


Figure 9.21 Point B must be a low-impedance point, whereas point A input current must be negligible.

Substituting (9.29) in (9.28), we have:

$$V_B(s) = -V_A(s)H(s)G(s) - \frac{Z_{out}(s)}{Z_{in}(s)}V_A(s) \quad (9.30)$$

Rearranging, we obtain the loop gain definition:

$$\frac{V_B(s)}{V_A(s)} = T(s) = -\left[H(s)G(s) + \frac{Z_{out}(s)}{Z_{in}(s)} \right] \quad (9.31)$$

This expression is different than the one derived in (9.26) and shows the effect of circuit impedances. To make the loop gain $T(s)$ independent from these impedances, you need to satisfy the following conditions:

$$Z_{out}(s) \ll Z_{in}(s) \quad (9.32)$$

$$\frac{Z_{out}(s)}{Z_{in}(s)} \ll T(s) \quad (9.33)$$

In other words, you must interrupt the loop at a position where point B output impedance is low and point A input impedance is much higher. Failure to do that will lead to a measurement distortion. References [7, 9] offer alternative methods to cope with a situation in which (9.32) and (9.33) cannot be respected. It naturally requires more manipulations to obtain the correct answer.

9.1.6 Buffering the Data

Most of modern ac-dc pulse width modulation (PWM) controllers no longer include the intelligence on the primary side. By intelligence, I mean the reference voltage and the error amplifier. These two elements are either combined in a TL431 placed on the secondary side or separately associated through an op amp and a discrete reference voltage. The typical architecture you will find is the one shown in Figure 9.22. It is that of a current-mode power supply.

The primary peak current is set by the voltage present on the feedback pin (labeled FB), further divided by R_1 and R_2 before reaching the peak current comparator. The FB pin level is adjusted by the current flowing in the optocoupler collector. This current depends on the TL431 action placed in the secondary side. Depending on the loading conditions, it automatically adjusts the LED current to program the

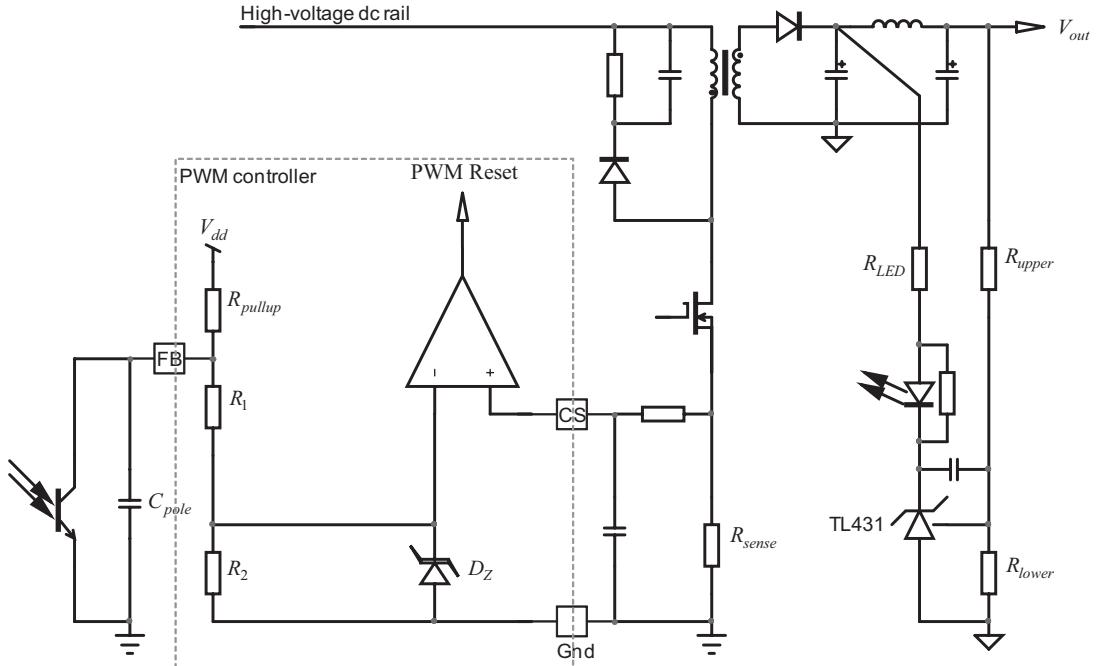


Figure 9.22 In modern power supplies, the intelligence is kept in the secondary side while the primary side features a simple feedback pin setting the inductor peak current or the duty ratio.

adequate peak current on the primary side. As explained in the TL431 chapter, we have two lanes, one fast and one slow. The fast one deals with R_{LED} , while the slow one deals with R_{upper} . One place to open the loop would be in series with R_{upper} , for instance, as it is usually a high-value resistance and the converter output is, by definition, a low-impedance point. Unfortunately, given the dual-lane architecture of the TL431 circuitry, ac modulating the system through R_{upper} would characterize only one path, the slow one. To form the complete chain, you would also need to characterize the other one (the slow lane) by inserting the ac source in series with R_{LED} . However, to apply the superposition theorem, you will need to disconnect one of the two paths and keep it dc biased while modulating the other one. Then, you will need to vector-combine both signals and reconstruct the complete loop gain. Nothing undoable, but it is a rather tedious and long process. Reference [10] shows you how to do that in detail.

If you want to simplify the measurement, the best way is exclude the output filter inductor. If you have selected it so that its cutoff frequency is high, the impact on the measurement is weak. Figure 9.23 illustrates how to connect the source. If you probe V_A and V_B as indicated, you will display the loop gain. Should you need the compensator transfer function including the optocoupler, move the V_B probe and place it at the feedback pin on the optocoupler collector. If you want the plant transfer function, keep V_B as in Figure 9.23 and move V_A to the feedback pin. Watch out: if you do that, you will have to connect both primary and secondary grounds as already suggested in Figure 9.4 and Figure 9.6. Make sure the high-voltage dc bias is fully isolated from the mains and apply safety rules in presence of these high voltages.

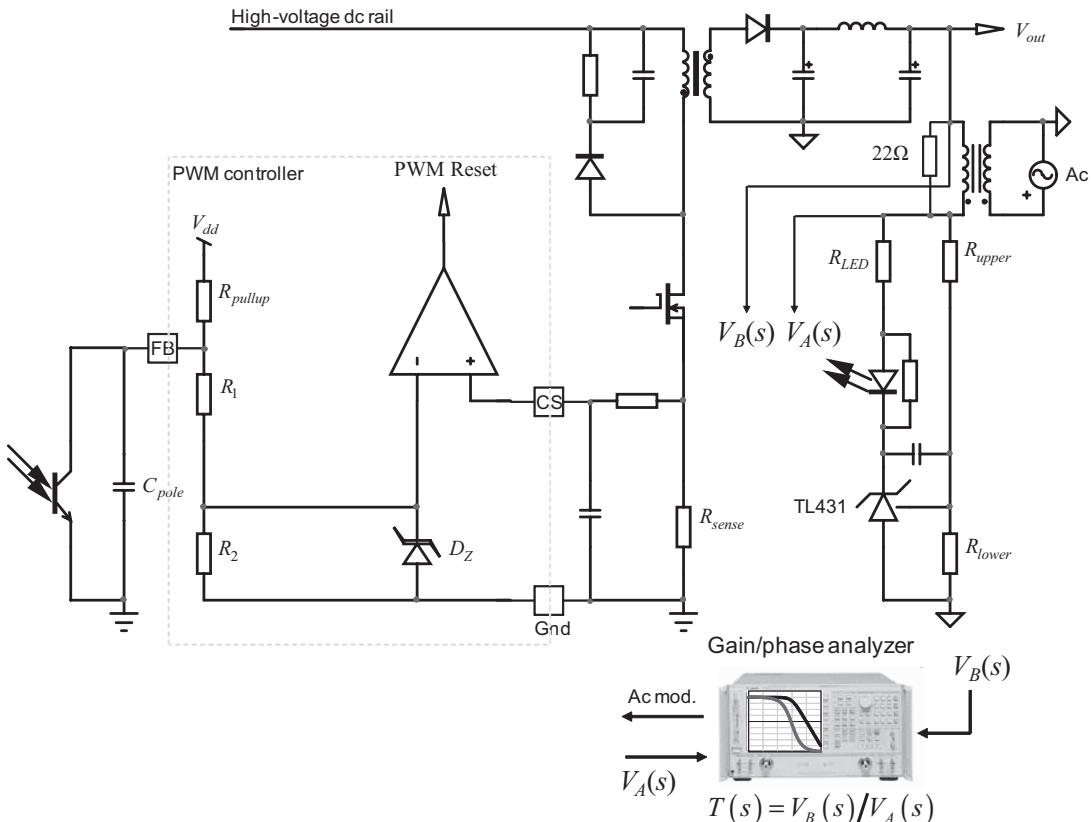


Figure 9.23 Connecting both lanes together helps to run a quick loop gain measurement.

Some designers may not like the fact that the fast lane connection before the output LC filter is ignored by this configuration. To obtain the complete loop gain without touching the secondary-side arrangement, one option is to open at the optocoupler collector. That way, we will capture the complete signal driven by the TL431 combining both lanes. Unfortunately, the optocoupler collector is of rather high output impedance, and if we disconnect it from the controller we lose all the internal bias conditions. The idea is to recreate these conditions externally and buffer the resulting signal before inserting the ac modulation. This is what Figure 9.24 presents. The optocoupler collector is loaded by the equivalent ac resistor R_{eq} present at the controller feedback pin. In our example, it is $R_{pullup} \parallel (R_1 + R_2)$. The internal bias, V_{dd} , is usually 5 V and externally applied on this resistor to reproduce the original bias conditions.

The capacitor placed on the feedback pin creates a pole and has to be moved on the optocoupler collector side to realize the same pole. The NPN transistor buffers the whole and sources the collector signal under a low output impedance. We used a 1-k Ω resistor, but it can be lowered if necessary. Lowered sometimes to make sure the feedback pin can drop to a low voltage if asked by the loop. If R_{eq} is around 15–20 k Ω , a 1-k Ω pull-down works well. For high-bandwidth systems, forward converters (e.g., the pull-up resistor inside the controller) can be down to 4.7 k Ω or less. In that case, to offer the same regulation dynamics, the emitter resistor can be as low as 100 Ω if necessary. In a multi-output system, the insertion of this bipolar

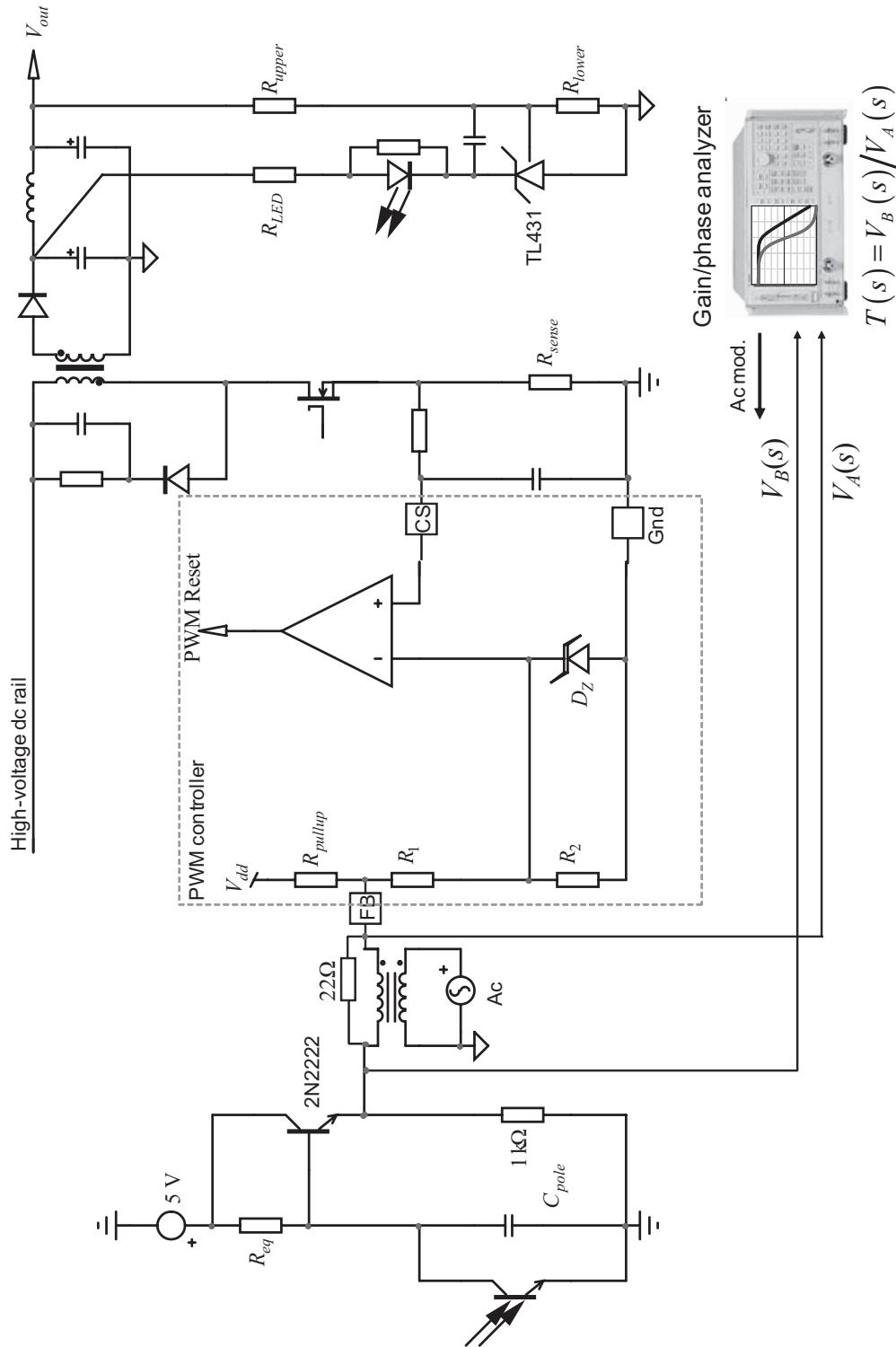


Figure 9.24 A simple bipolar buffers the optocoupler collector and drives the controller with a low output impedance.

transistor can bother the whole operation at startup. You will need some skill to slowly raise the voltages in order to ensure a proper regulation without tripping the protection controller. We have seen this issue in multi-output ATX power supplies, for instance.

Loop gain measurements require experience and patience. Fortunately, a lot of publications and manuals are available on the web to guide you in your experiments. Now that we know how to measure a loop, let's have a look at a few design examples. However, before closing this section, I want to express my gratitude to Dr. Jose Capilla from ON Semiconductor with whom I have had endless discussions on vectors and source amplitudes and whose internal seminar on the subject has been of great help [11].

9.2 Design Example 1: A Forward dc-dc Converter

This first design example covers a transformer-isolated dc-dc converter. Based on a single-switch forward topology, the converter delivers 5 V at a 20 A output current from a telecom network. Assume our converter specifications require a crossover frequency of 10 kHz, together with a 60° phase margin. This last requirement implies an opto-isolating device whose pole is naturally well beyond this crossover value. If we select a slow optocoupler, depending on the adopted feedback scheme, we may encounter difficulties to compensate the phase degradation as its pole kicks in. Adding another zero in the control loop looks like a possible option. However, if this zero provides phase help at first glance, its presence will hamper the recovery time, especially if it is located in the lower portion of the frequency spectrum. Using the inherent optocoupler pole as a companion rather than an enemy is the strategy we recommend.

9.2.1 Moving Parameters

Available optocoupler characterization curves is an element you might want to consider prior to the device selection. Collecting data points because of a weak data sheet content is something you want to avoid. To that respect, the PC817 specification sheet from Sharp offers a great deal of detail. Browsing it indicates that the A version represents a good pick: the CTR varies from 80 percent to 140 percent at a 25°C junction temperature, and as Figure 9.25 confirms a 2-mA LED forward current brings it to 100 percent. Temperature variations shown in Figure 9.26 point out a total span of 60 percent, from a junction temperature ranging from -30 °C up to 100 °C.

As the parameters in the data sheet are guaranteed at 25°C only, the minimum CTR mixing lots-to-lots dispersions and temperature spreads must be updated to:

$$\text{CTR}_{\min} = 80\% \times 60\% = 48\% \quad (9.34)$$

Therefore, we will have to shield our converter design against potential optocoupler CTR changes from 48 percent to around 140 percent, a corresponding 1:3.3 ratio. It is important to mention that these variations are just typical data and

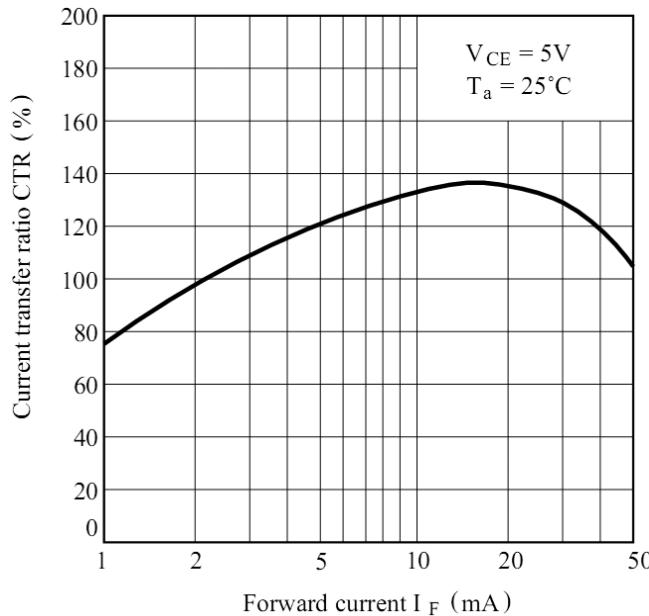


Figure 9.25 The CTR reaches a typical value of 100 percent for a 2-mA LED current.

often not guaranteed in the data sheet. Further discussions are thus necessary with the optocoupler manufacturer to obtain the real dispersion you should expect over the converter lifetime.

Bandwidth-wise, the data sheet offers a frequency characterization in relationship to the collector pull-up resistor. It appears in Figure 9.27 that a 1-k Ω pull-up resistor brings the pole to roughly 25 kHz. This is an excellent value for a 10-kHz

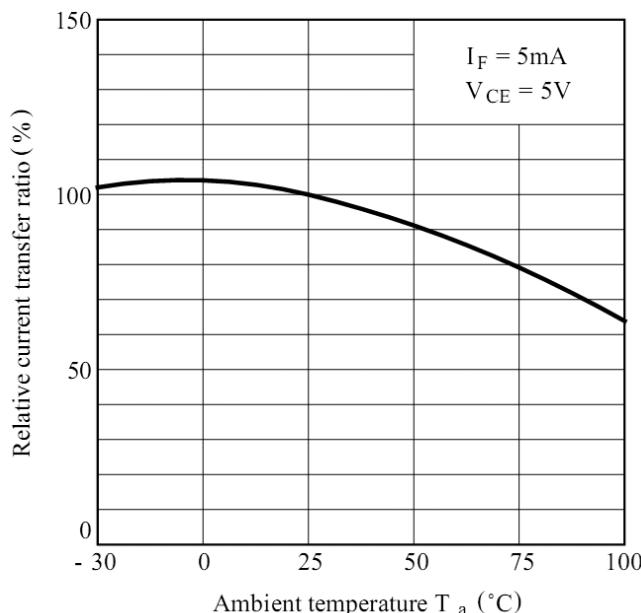


Figure 9.26 CTR versus temperature variations are also available and indicate a 60 percent reduction in the upper range.

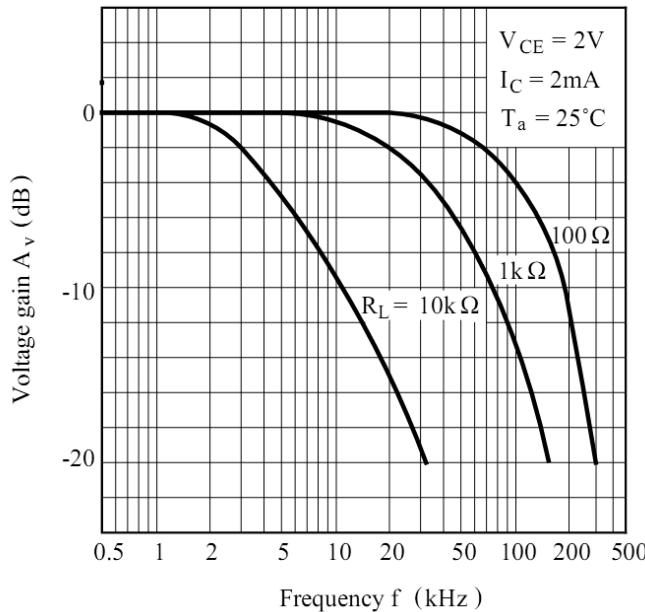


Figure 9.27 The frequency characterization of the PC817 reveals a 25-kHz pole when a pull-up resistor of 1 kΩ is adopted.

bandwidth project. Unfortunately, the document does not indicate the PC817 suffix this curve is attached to. For a serious study, once several optocoupler samples are received, it is the designer's task to set up a characterization fixture such as that described in Chapter 5's Appendix C to extract the pole positions in various operating conditions. In our case, as the selected controller featured a 3.3-kΩ pull-up resistor, we have recharacterized the chain and found a pole around 15 kHz.

Based on this information, we are able to determine the equivalent optocoupler parasitic capacitor value C_{opto} when its collector is loaded with a 3.3-kΩ resistor:

$$C_{opto} = \frac{1}{2\pi R_{pullup} f_{pole}} \approx 3.2 \text{ nF} \quad (9.35)$$

When lacking available bench data (e.g., you did not receive the optocoupler samples at the time of the study), information from Figure 9.27 can be used for a first-pass analysis that you will further refine by extensively testing and characterizing the prototype during laboratory experiments.

9.2.2 The Electrical Schematic

Our converter must deliver 5 V at 20 A from a telecom input power, implying a voltage variation from 36 V to 72 V dc. A forward converter belongs to the buck-derived topology. When operated in voltage-mode, this structure shows a resonating peak brought by the combination of the inductor and the output capacitor. When this resonant frequency is low, the compensation scheme must include a double zero located around the resonant peak. In terms of transient response, a zero involved in the compensation loop, $G(s)$, becomes a pole when you study the closed-loop

transfer function. As we want a fast response with a good recovery time, we must avoid low frequency zeroes. For this reason, the current-mode topology looks like the best choice to go for as it turns the converter into a first-order system at frequencies below half of the switching frequency. Furthermore, the mode transition that occurs in light load conditions does not imply a particular care when designing the control loop. On the contrary, compensating a voltage-mode converter toggling between both modes is a difficult exercise, as the Bode plot dramatically changes when transitioning from the CCM to the discontinuous conduction mode (DCM). For budget reasons, a single-switch topology featuring a demagnetization winding was selected, but the example remains pertinent in case another choice would be adopted (two-switch forward, RCD clamp, and so on).

The NCP1252 from ON Semiconductor is a possible candidate for the PWM control section, as it packs a lot of good features. With its soft-start and frequency jittering capabilities, it can be considered a replacement of choice for future or existing UC384X-based designs. Furthermore, due to its integrated skip-cycle type of control, the circuit accepts no-load conditions without going into overvoltage as with other devices. The application schematic appears in Figure 9.28. Despite the involved power, there is not much around the controller. A simple pull-down resistor of 22 kΩ sets the switching frequency to 200 kHz, while the brown-out network made of R_2 and R_8 ensures the operating input voltage is always greater than 33 V.

The output inductor has been selected for a 10 percent ripple current when the controller switches at 200 kHz. The two output diodes accept up to 40 A, dropping 0.58 V when crossed by a 20-A current ($T_j = 100^\circ\text{C}$). The control loop uses an operational amplifier driving the optocoupler LED cathode while its anode connects to the output voltage rail. This configuration is very close to that of a TL431 featuring two lanes: a slow lane implying the capacitor C_1 and a fast lane brought by R_3 . The transfer function of this type 2 compensator has already been derived in Chapter 5 and equals:

$$\frac{V_{FB}(s)}{V_{out}(s)} = G(s) = - \left[\frac{sR_1C_1 + 1}{sR_1C_1(1 + sR_{pullup}C_1)} \right] \frac{R_{pullup}\text{CTR}}{R_3} = -G_0 \frac{1 + s/\omega_z}{s/\omega_{po}(1 + s/\omega_p)} \quad (9.36)$$

where

$$G_0 = \frac{R_{pullup}\text{CTR}}{R_3} \quad (9.37)$$

$$\omega_{po} = \frac{1}{R_1C_1} \quad (9.38)$$

$$\omega_z = \frac{1}{R_1C_1} \quad (9.39)$$

$$\omega_p = \frac{1}{R_{pullup}(C_{opto} + C_8)} \quad (9.40)$$

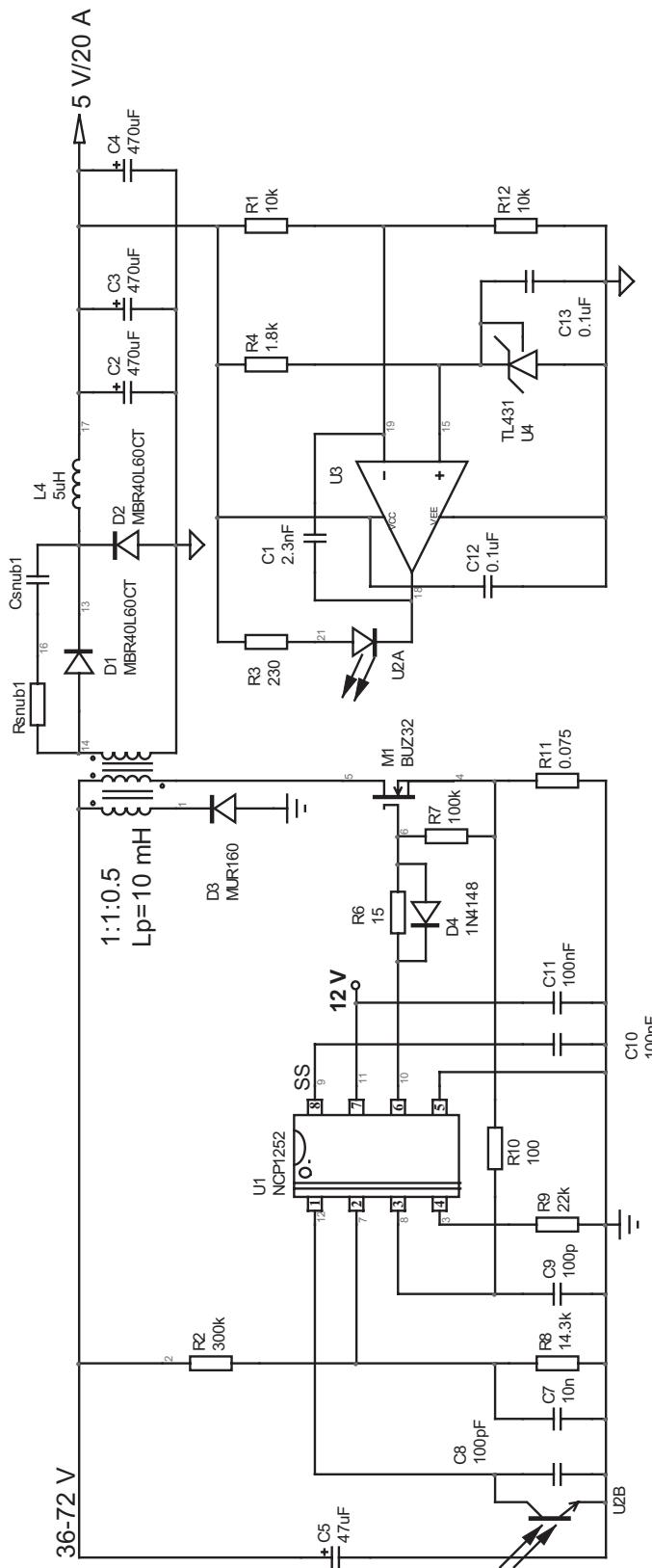


Figure 9.28 The application circuit of the single-switch forward converter using a NCP1252.

In this type of configuration, the dc conditions bounds R_3 values through the minimum output voltage the operational amplifier is capable of. We can show that the maximum value authorized for R_3 obeys the following formula:

$$R_{LED,\max} \leq \frac{V_{out} - V_f - V_{op\ amp,min}}{V_{dd} - V_{CE,sat}} R_{pullup} \text{CTR}_{\min} \quad (9.41)$$

where:

$V_{opamp,min}$, the minimum output voltage the selected operational amplifier can go down to

V_{out} , the output voltage (5 V in our example)

V_f , the optocoupler LED forward drop (≈ 1 V)

CTR_{\min} , the minimum optocoupler current transfer ratio: roughly 50 percent for a PC817A as rounded from (9.34)

$V_{CE,sat}$, the optocoupler saturation voltage (≈ 300 mV at a 1-mA collector current) which imposes the minimum feedback voltage

V_{dd} , the internal bias of the pull-up resistor, usually 5 V

R_{pullup} , the internal pull-up resistor of 3.3 k Ω

If we consider a low-state voltage excursion for the op amp of 150 mV, the LED series resistor cannot exceed the following value:

$$R_{3,\max} \leq \frac{5 - 1 - 0.15}{5 - 0.3} \times 3.3k \times 0.5 \leq 1.35 \text{ k}\Omega \quad (9.42)$$

This condition, unfortunately, sets a minimum gain for the compensator featuring the op amp and the LED connected to the output voltage. According to (9.37), this minimum gain amounts to

$$G_0 = \frac{R_{pullup} \text{CTR}_{\max}}{R_3} = \frac{3.3k \times 1.4}{2.7k} = 1.7 \text{ or } 4.6 \text{ dB} \quad (9.43)$$

Some power stages require an attenuation at crossover. For instance, if your gain analysis of the power stage $H(s)$ reveals a +7-dB gain at 1 kHz, you will have to shape the compensator to make its magnitude equal -7 dB at 1 kHz. If you want to use the configuration described in Figure 9.28, you will be stuck given the result found in (9.43): 4.6 dB minimum gain. The limit is similar to that of the TL431 when its fast lane is used. To design such a compensator, you would have to (a) decouple the LED connection from V_{out} via a Zener or a regulator, or (b) drive the LED anode directly with R_3 connected to ground. This last option would certainly remove the output voltage influence on the compensator, but it would force you to wire the optocoupler in a common collector configuration to account for the phase reversal. Some controllers accept this; some do not.

9.2.3 Extracting the Power Stage Transfer Response

The output power stage ac transfer response can be obtained in different ways: bench measurement, analytical description, and SPICE simulation. Bench measurements require a rather complex setup plus an operational prototype. You must

therefore wait for the various elements to be assembled before data can be exploited for the compensation purposes. On the other hand, the analytical derivation requires a simple sheet of paper and helps you to gain insight in the power stage transfer function. It shows you where the poles and zeros are and what external parameters can influence them. To that respect, going once through this kind of exercise is mandatory for someone serious about loop control. The main drawback is that you need two sets of equations depending on the operating mode (CCM or DCM). For this reason, the SPICE simulation of converters represents an excellent tradeoff. When the parasitic elements such as capacitor equivalent series resistors (ESR) are well extracted from the manufacturer data sheets (or, even better, you measure them through an impedance plot), experience proves that the predicted response matches very well with final measurements carried over the prototype. Furthermore, thanks to auto-toggling average models such as those described in [12], you will have the ability to explore both operating modes and check how your compensation strategies affect the transient response.

The first step is to extract the transfer function of the power stage, $H(s)$, at the lowest input voltage and maximum output current. The template in Figure 9.29 will give you this response. The optocoupler is a simplified model described in [12] but good enough to see the pole effect and its CTR impact on the gain. The B_1 source mimics the controller internals (i.e., the relationship between the feedback voltage and the peak current setpoint): a series diode drops 0.6 V and a divide-by-three bridge further affects the signals. This is what the equation describes, as well as clamping the maximum excursion to 1 V. It is very similar to what is found in a UC384x controller.

From the power stage transfer curve, we will obtain the information at the targeted crossover frequency (10 kHz, in our example) such as the magnitude and the phase lag. These data will feed our compensator calculation flowchart. Figure 9.30 portrays $H(s)$ Bode plot obtained in a few milliseconds of simulation time.

The accuracy of such a plot depends mainly on the parasitic elements. If you have properly extracted the capacitors ESR values, then there is a good chance that the ac simulation will accurately match the data collected in the laboratory. If needed, you can even refine the simple capacitor model by a more accurate one as described in the Kemet site (see [13]). The company offers various modeling software for different capacitor technologies such as Multi Layer Ceramic Capacitors. These comprehensive models reflects the ESR variations versus frequency and fit well simulations of high-quality dc-dc converters for space or military applications, for instance. In this domain, immunity to component variations is of extreme importance.

9.2.4 Compensating the Converter

From this picture, we can see that a 10-kHz crossover frequency requires a lift of 17.2 dB. As the phase lag is 51° at this frequency, we will need to tailor the compensator transfer function $G(s)$ to provide some phase boost to meet the needed phase margin target at crossover. To provide a good dc gain, we will use a compensator type featuring an origin pole in the transfer function. Its presence implies a permanent phase delay of 90° to which the op amp phase reversal adds another

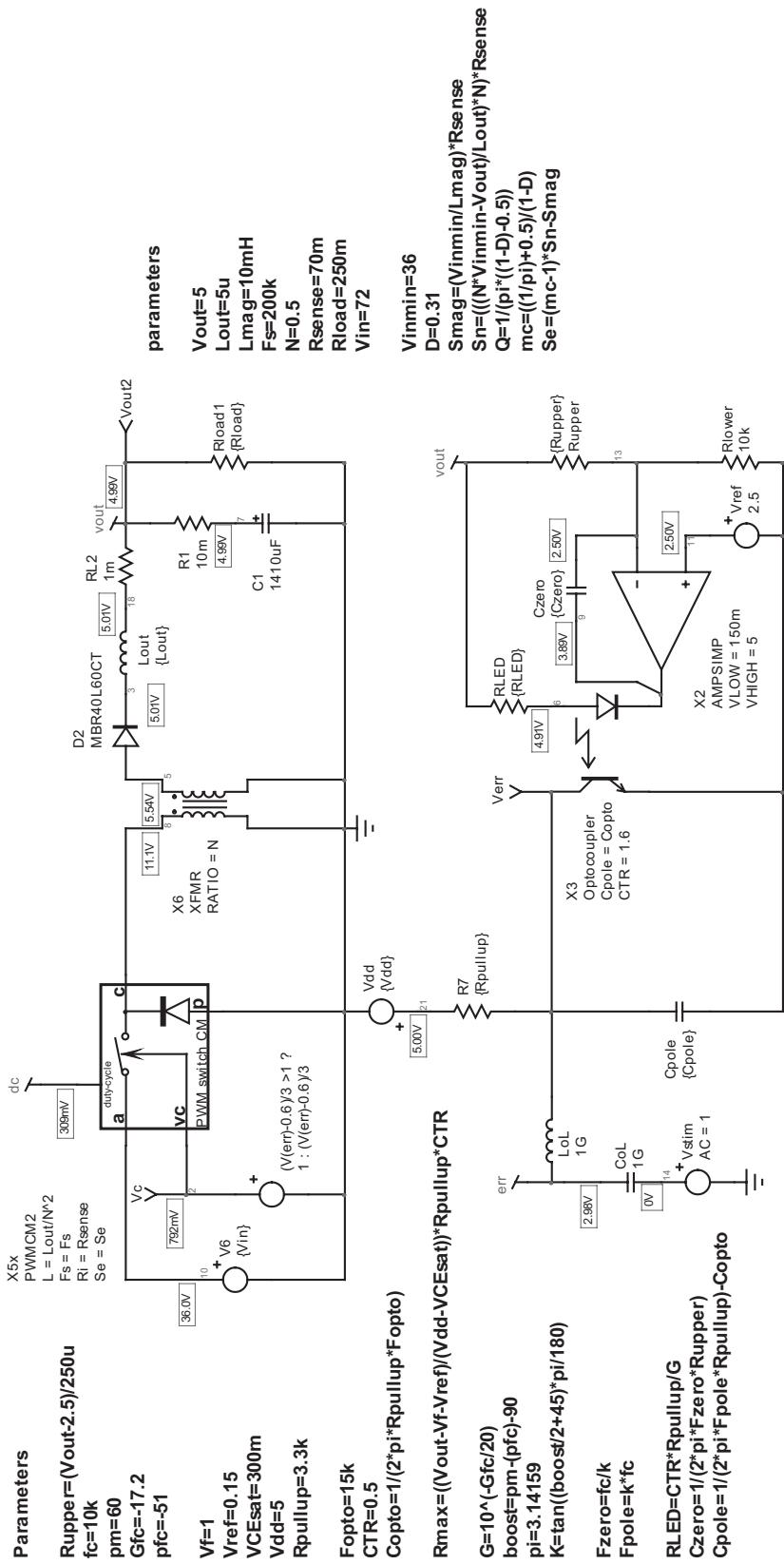


Figure 9.29 An average model operated in current-mode and associated with an op amp can quickly deliver the power stage transfer function.

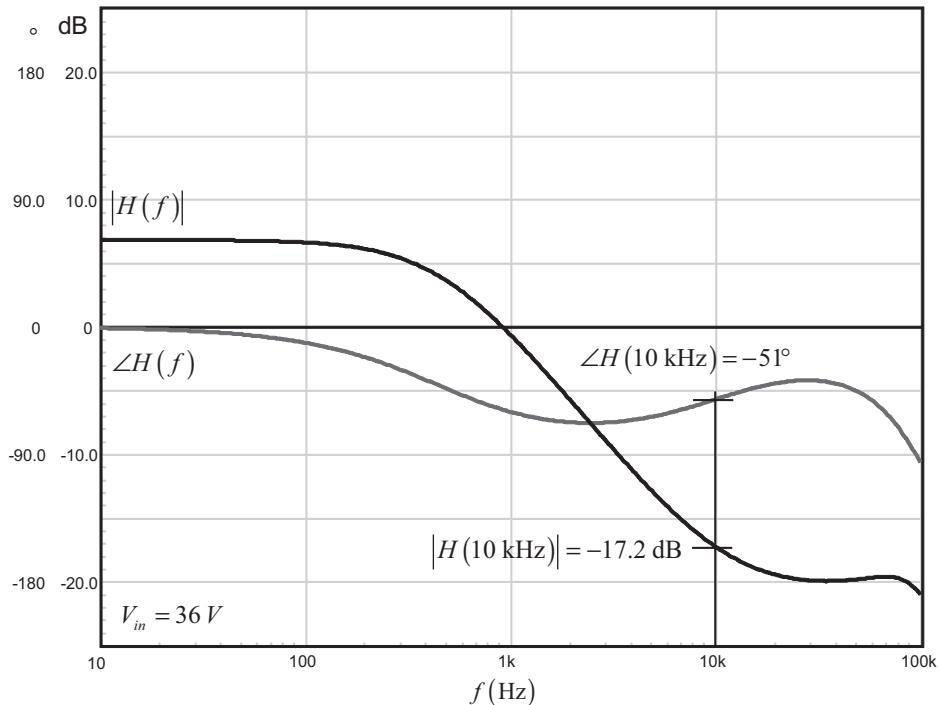


Figure 9.30 The transfer function $H(s)$ of the power stage at low input voltage and full load.

180°, making a total of -270° . If we want to obtain a 60° phase margin at 10 kHz, then the cumulated phase lag of $\arg H(s) + \arg G(s)$ will need to be below $-360 + 60 = -300^\circ$. As the total argument of the power stage plus the origin pole of the compensator reaches $-270 - 51 = -321^\circ$, we need to provide a phase boost of 21° at 10 kHz. Otherwise stated:

$$\text{BOOST} = \varphi_m - \arg H(f_c) - 90^\circ = 60 + 51 - 90 = 21^\circ \quad (9.44)$$

Such a low phase boost can easily be obtained with a type 2 configuration. In the previous chapters, we have seen several methods to help you build the necessary phase boost. Using the k factor described in Chapters 4 and 5, we will place a zero at 6.8 kHz and a pole at 14.5 kHz. We can show that the phase boost brought by this configuration at 10 kHz is exactly:

$$\tan^{-1}\left(\frac{f_c}{f_z}\right) - \tan^{-1}\left(\frac{f_c}{f_p}\right) = 55.8 - 34.6 \approx 21^\circ \quad (9.45)$$

Following equations (9.37), (9.39), and (9.40), we found a zero capacitor C_{zero} of 2.3 nF (C_1 in Figure 9.28) and a pole capacitor of 3.3 nF. According to (9.35), with an optocoupler parasitic capacitance of 3.2 nF, you just need to add a small 100 pF for C_{pole} (C_8 in Figure 9.28) to reach the total value of 3.3 nF. Wire this capacitor as close as possible to the controller pins to locally improve the noise immunity. The gain is set by the LED series resistor (R_3 in Figure 9.28) to cope with the 17.2-dB requirement. Its value is 227Ω and respects the limit set by (9.42).

Calculation on the power stage shows the necessity of external ramp compensation to damp the subharmonic poles. Once the natural ramp brought by the magnetizing current has been accounted for, a level of 16.6 kV/s can be adjusted in the NCP1252 via the current sense series resistor R_{10} . Figure 9.31 shows the loop gain when compensating elements have been placed over the operational amplifier. The upper and lower graph on the picture show the open-loop gain at low and high input line, respectively.

SPICE simulations of averaged models are extremely fast due to the lack of a switching component. This simulation speed helps to immediately assess the impact of the various parasitic elements on the converter stability. In Figure 9.31, the CTR has been changed from 50 to 160 percent to include some margin. It induces a crossover frequency variation from 9.3 kHz up to 23.7 kHz. If the end result keeps a good phase margin at both input voltage extremes, a 23-kHz crossover frequency represents a very aggressive target. The wider the bandwidth, the easier it becomes to collect parasitic noises and unwanted spurious signals. For this particular study, it would be wiser to reduce the crossover frequency around 7 kHz at low line/low CTR and manage a maximal excursion up to 15 kHz, a more reasonable value for a converter.

Once the compensation strategy is confirmed to deliver the right crossover frequency together with the needed phase margin, a transient step response can be performed. Again, thanks to the average modeling technique, the simulation time is flashing and the results appear in Figure 9.32 after a few milliseconds of computing time.

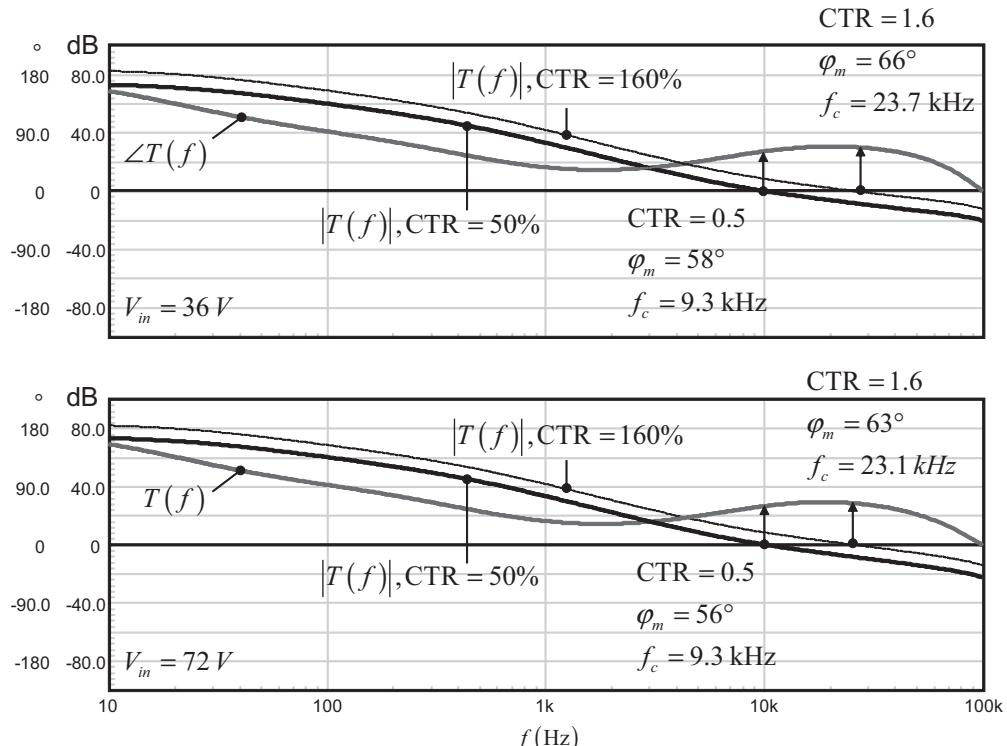


Figure 9.31 Thanks to simulation speed of average models, changing the parameters on the fly is an easy way to test the stability robustness. Here, the CTR is varied between 50 and 160 percent.

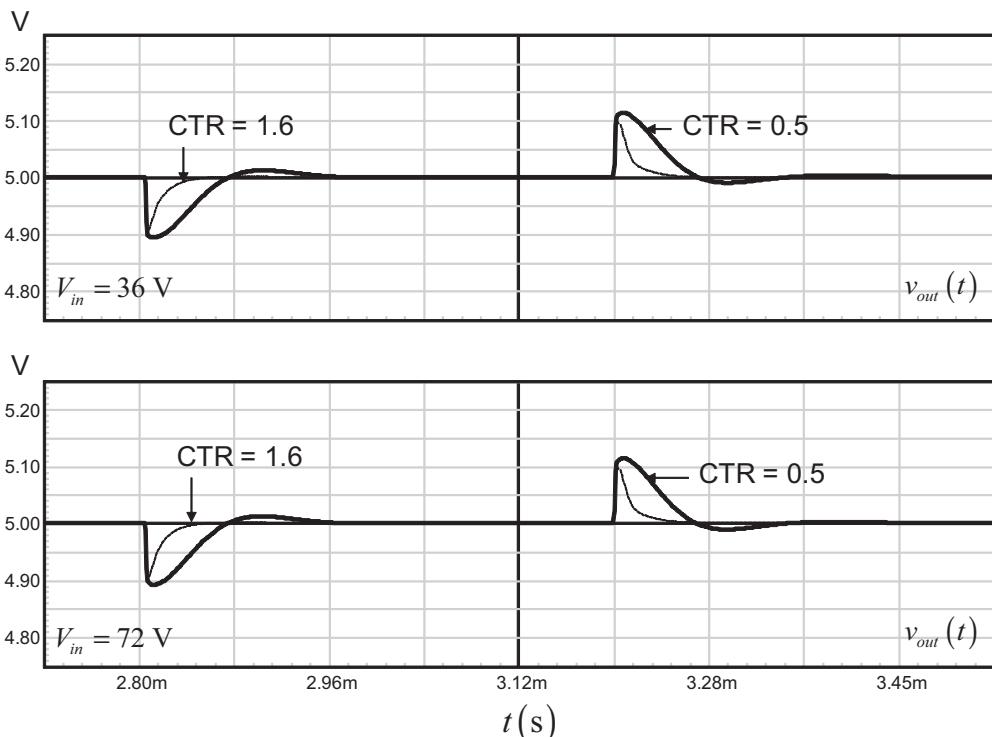


Figure 9.32 Transient response to a step from 10 A to 20 A with a slope of 1 A/ μ s.

As you can observe, the undershoot stays within a 150-mV variation. This variation slightly reduces as the bandwidth increases when the CTR peaks. This is because a direct relationship exists between the undershoot and the converter output impedance, as already explained in Chapter 3. The response is fast with almost zero overshoot in both input voltage conditions, and it satisfies our design requirements for this project. To refine the study, it is now possible to assign tolerances to the rest of the sensitive elements such as the output capacitors and their associated ESR and run a series of ac sweeps in a Monte Carlo style. Thanks to the fast simulation time, you will learn whether dangerous situations could exist when certain dispersions are combined together. Making sure the phase margin never gets too low in all situations will ensure a seamless mass-production period.

9.3 Design Example 2: A Linear Regulator

Power conversion implies not only switching converters but also linear regulators. In this case, the power element no longer operates in a switching mode but remains linear. This operating mode implies a decrease of efficiency but in lack of current and voltage discontinuities, the noise generated by such a converter remains extremely low compared to that of a switching converter.

Numerous application schematics exist for linear regulators. The first family was built around NPN series-pass bipolar transistors used as a dropping or a so-called

ballast element. Still in service these days, this type of regulator requires several volts of input/output differential potential to operate in good conditions. The 78xx series (LM7805, MC7812, and so on) are good examples of these regulators. The typical schematic of such a device appears in Figure 9.33. Yes, I can hear linear regulator designers laughing from here: this is an oversimplified design for the sake of the example! You can see the ballast transistor, actually a darlington, whose base is driven by an op amp. Depending on the current sourced by the op amp, the transistor conducts more or less to feed the load at a constant output voltage. To maintain the transistor conduction, the base voltage needs to stay above the output voltage by two V_{BE} , around 1.3 V typically. Therefore, if you want to deliver 5 V, the minimum input voltage must be above 7 V if you include the various losses incurred to the driving stage (op amp output voltage saturation drop, for instance). This drawback is typical of non-low drop out (LDO) regulators whose conduction losses are rather high. On the contrary, LDO types use a P-channel or a PNP transistor and can accept input/output differential voltages down to a saturation voltage, a few hundred mV. In this mode, the gate or the base is easily brought to ground, and building a V_{GS} is no longer seen as a bias limit. The minimum drop in that case is given by the transistor $R_{DS(ON)}$ if a MOSFET is used. Such a simplified LDO appears in Figure 9.34 and shows how to wire the P-channel transistor so that its body diode does not bother us.

9.3.1 Extracting the Power Stage Transfer Function

The power stage transfer function of both circuits will be extracted using a simple SPICE template where the couple *LoL/CoL* helps to close the loop in dc but opens it in ac. As a reminder, the simulator shorts all inductors and opens all capacitors to compute the dc bias point before starting any type of simulation (ac or dc). This

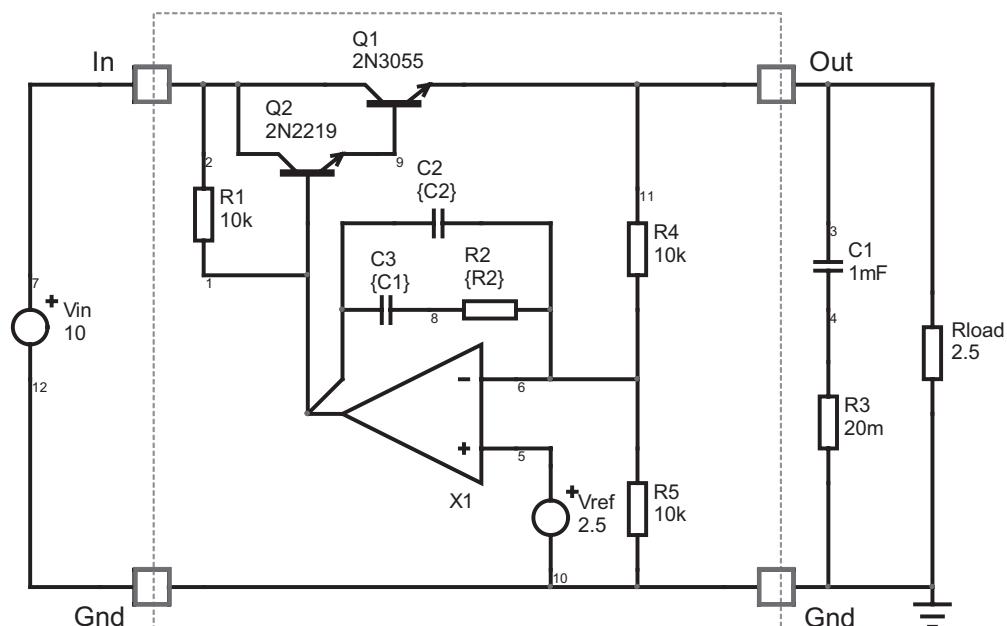


Figure 9.33 A simplified 5-V/2-A linear regulator using a series-pass transistor.

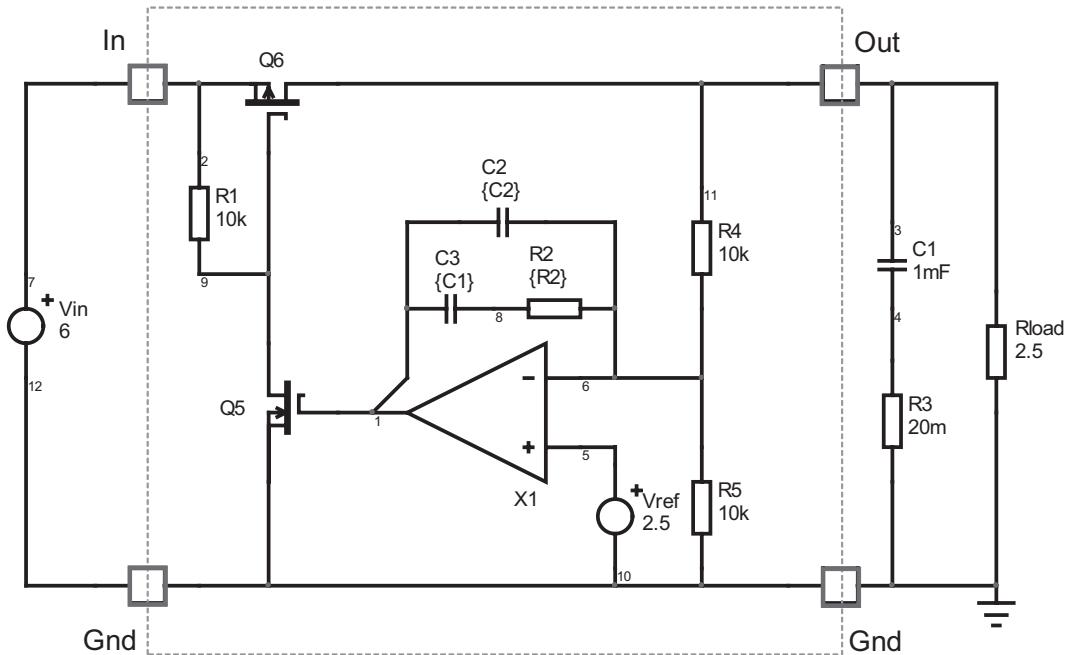


Figure 9.34 A simplified low-dropout regulator built around a P-channel MOSFET transistor.

bias point serves to further linearize the circuit as SPICE handles only linear equations. As a result, before the ac sweep starts, when SPICE computes the bias point, the loop is closed with *LoL* (*CoL* is an open circuit) and the bias point is automatically adjusted via the loop to meet the output target (5 V in our example). When the ac simulation starts, the *LoL/CoL* network forms an extremely low cutoff frequency filter: all ac modulation passes through *CoL* while the return path cannot cross *LoL*, whose high-value is equivalent to an open circuit. The loop is well closed in dc but open in ac. The power stage transfer function is probed in V_{out} while the loop gain, once compensated, is obtained by probing V_{err} . The traditional regulator simulation template is shown in Figure 9.35 while that of the LDO appears in Figure 9.36.

The bias points we have reflected on the schematic confirm the computed results are what we expect. The simulation results are given in Figures 9.37 and 9.38.

9.3.2 Crossover Frequency Selection and Compensation

In Chapter 3, we derived the relationship between the output response undershoot and the crossover frequency. When analyzing the step load output response, we found that the transient output deviation was made of the capacitive value, together with its parasitic elements. If reducing the di/dt will almost eliminate the ESL peak, the response deviation will still include the capacitor and its series ESR addition. Whatever the crossover frequency value, there is no possibility to avoid the ESR times the output current drop. However, rather than pushing the crossover frequency too far, we derived a simple formula at the end of Chapter 3. The formula

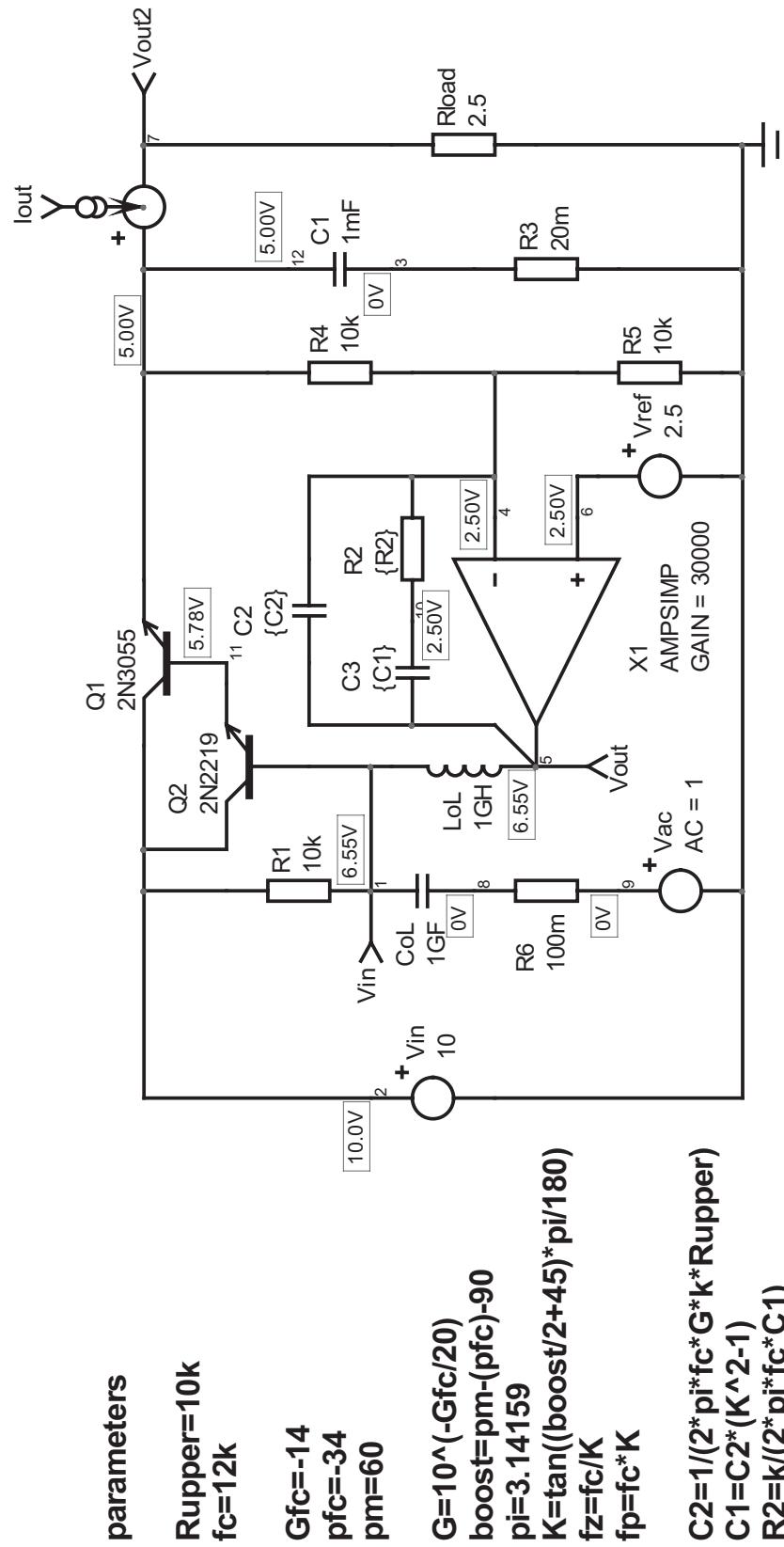


Figure 9.35 The loop is open behind the op amp, just before driving the darlington. We assume that the series-pass element driving circuit is embedded in the op amp.

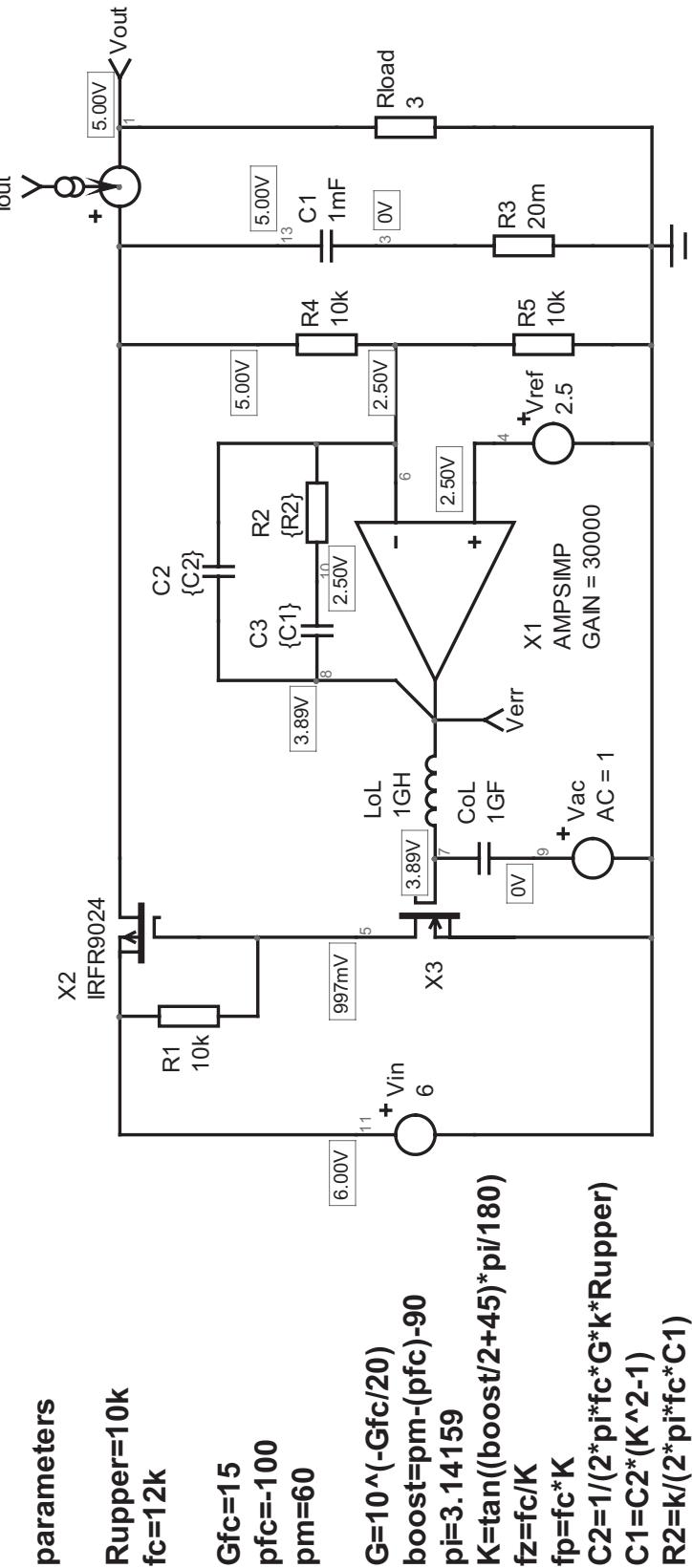


Figure 9.36 The simulation template for the P-channel-based LDO is very similar to that of the bipolar-based regulator.