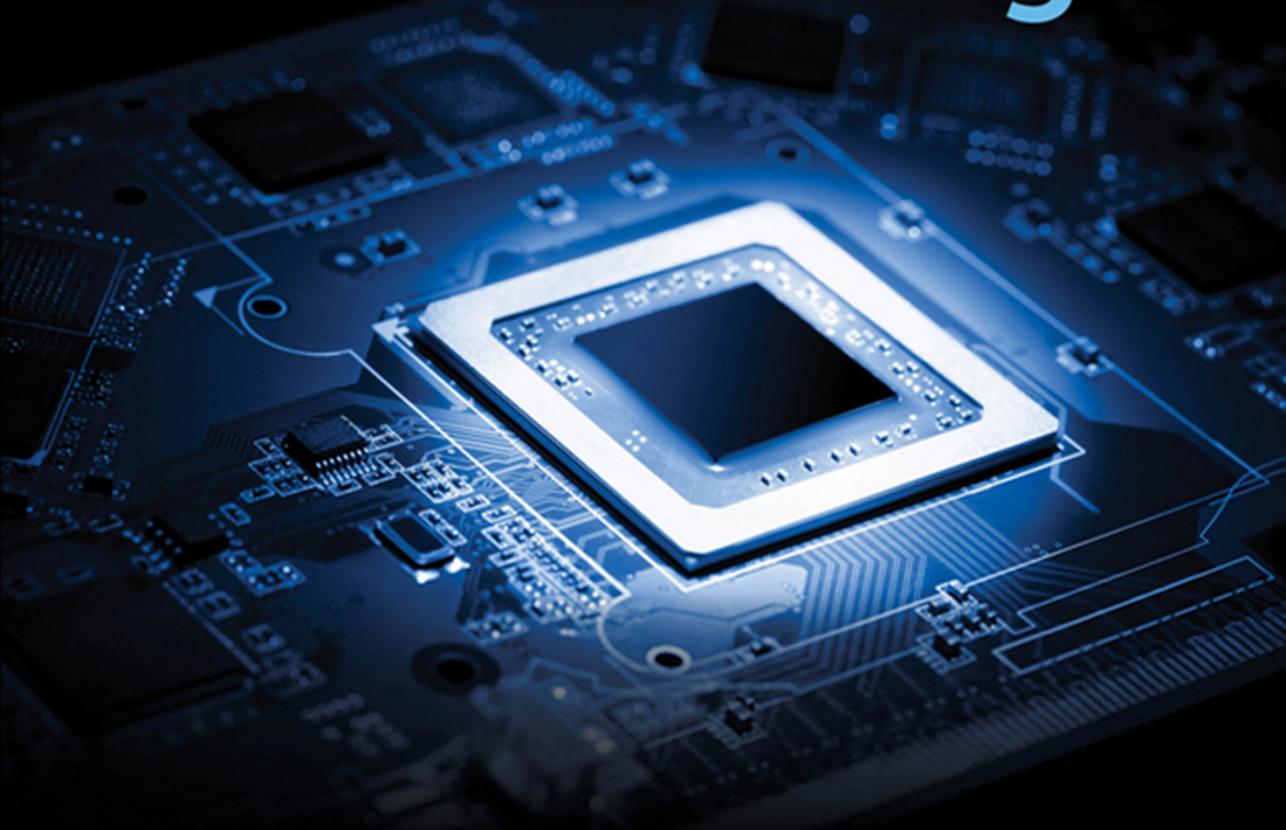


# Power Management Techniques for **Integrated Circuit Design**



Ke-Horng Chen

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# **POWER MANAGEMENT TECHNIQUES FOR INTEGRATED CIRCUIT DESIGN**



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**Ke-Horng Chen**

*National Chiao Tung University, Taiwan*



**WILEY**

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*To my respected parents, Li-Yun Wu and He-Nan Chen, and my wife, Hsin-Hua Pai*



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# About the Author

**Ke-Horng Chen** received his B.S., M.S., and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a part-time IC Designer at Philips, Taipei, Taiwan. From 1998 to 2000, he was an Application Engineer at Avanti Ltd., Taiwan. From 2000 to 2003, he was a Project Manager at ACARD Ltd., where he was engaged in designing power management ICs. He is currently Director of the Institute of Electrical Control Engineering and a Professor with the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he has organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 200 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, and display algorithm and driver designs of liquid crystal display (LCD) TVs.

Dr. Chen has served as an Associate Editor of *IEEE Transactions on Power Electronics* and *IEEE Transactions on Circuits and Systems – Part II: Express Briefs*. He is also an Associate Editor of *IEEE Transactions on Circuits and Systems – Part I*. He joined the Editorial Board of *Analog Integrated Circuits and Signal Processing* in 2013. He is on the IEEE Circuits and Systems (CAS) VLSI Systems and Applications Technical Committee, and the IEEE CAS Power and Energy Circuits and Systems Technical Committee. He belongs to the Society for Information Display (SID) and International Display Manufacturing Conference (IDMC) Technical Program Sub-committees. He is Tutorial Co-Chair of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) 2012 and Track Chair of Integrated Power Electronics, IEEE International Conference on Power Electronics and Drive Systems (PEDS) 2013. He is Technical Program Co-Chair of IEEE International Future Energy Electronics Conference (IFEEC) 2013. He has served as CAS Taipei Section Chair since 2015. He is also Technical Program Committee Member, European Solid-State Circuits Conference (ESSCIRC) 2014–present.

# Preface

Over the past three decades, power management technology has become more important as portable and wearable electronics have become part of our daily lives. It is important to realize the detailed design of power management circuits, including low dropout (LDO) regulators, switching power converters (SWRs), switched-capacitor designs among others, if battery usage lifetime and power-conversion efficiency need to be extended. Although some circuits can be found in analog or power electronics books, the reader cannot get an overall understanding of power management designs. Thus, I have written this book to collect useful material related to power management designs in recent years.

Power management IC designs use low-voltage (LV) and high-voltage (HV) devices. The specialty of this book is including LV and HV power management designs. Moreover, the objective of the book is to let the reader understand the process trend and demand of today's applications from the first. The mathematical analysis in the book is simplified, because in my opinion the reader needs to have the ability to understand the function of power management circuits. After that, the reader can analyze the whole power system and derive the complicated mathematical results. Thus, I have used many easy-to-understand figures in the book to let the reader realize why and how power management should be implemented. Although the reader can understand this via derived equations in some similar books, they can have the fun of thinking about and implementing their own designs if they study the circuits in this book by inspection rather than by equations. Moreover, digital and analog design techniques are introduced because a combination of digital and analog skills can give maximum performance of power management in system-on-chip (SoC) applications.

I have taught most of the material in this book both at the National Chiao Tung University, Hsinchu, Taiwan and in Taiwan industry. The order, the format, and the content are all carefully polished when I deliver the material to readers. It is a pity that much material is not included in this book. However, I encourage the reader to apply the concepts to similar power management designs. I have included some design guidelines in this book to let the reader realize the objective of each design.

Chapter 1 provides the reader with knowledge of LV and HV device characteristics and structure in different advanced technologies for learning the material in this book.

Chapter 2 describes the general design of an LDO regulator used in many power management circuits. Compensation skills are introduced to let the reader realize how to ensure power stability in case of any disturbance from input, output, and loading. A digital LDO regulator is also included for LV applications.

Chapter 3 includes the design guidelines of voltage-mode and current-mode switching power regulators. Compensation skills are also introduced to quantify the behavior of basic pulse-width-modulation (PWM) SWRs by inspection.

Chapter 4 introduces the ripple-based control technique for some applications that demand the features of fast transient response, low power consumption, and compact size solution. In particular, fast transient response is the trend for SWR designs to improve the performance of dynamic voltage/frequency scaling techniques and/or reference tracking techniques.

Chapter 5 shows some ripple-based control techniques to improve the performance of basic designs. Even if parasitic effects become large, the techniques presented here can still have excellent performance. Readers can train themselves by using the circuits in this book, proved for silicon, to implement useful power management circuits.

Chapter 6 shows state-of-the-art single-inductor multiple-output (SIMO) converters used in SoC to minimize the power module size. The power stage design and controller design are included in this chapter. We use the design concepts introduced in Chapters 2–5. The reader can obtain advanced training in power management designs here.

Chapter 7 shows the switching-based battery charger to complete the full function of power management in SoC designs. The basic stability proved by some behavior simulators can let the reader know how to model and increase the whole battery charger system.

Chapter 8 includes some energy-harvesting techniques to let the reader realize the possibility of obtaining energy from the environment. How to convert and how to improve efficiency are shown in this chapter.

# Acknowledgments

This book has benefited from the recent research results of my Master and Ph.D. students. Many experts in both this research field and industry contributed much useful material to this book. Among them are Shen-Yu Peng (National Chiao Tung University, Hsinchu, Taiwan), Meng-Wei Chien (RealTek Corporation, Hsinchu, Taiwan), and Ying-Wei Chou (MediaTek Inc., Hsinchu, Taiwan). I say “thank you” to them.

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My wife, Hsin-Hua, has made some contributions to this book. She encouraged me to complete the whole book using a range of useful circuits proved for silicon. She collected much useful material, including simulation and experimental results.

The book’s production was made possible with the cooperation of staff at John Wiley. I thank James Murphy, Preethi Belkese, Maggie Zhang, Gunalan Lakshmipathy, Revathy Kaliyamoorthy, and Clarissa Lim. Without their help, there would be no book.



# 1

## Introduction

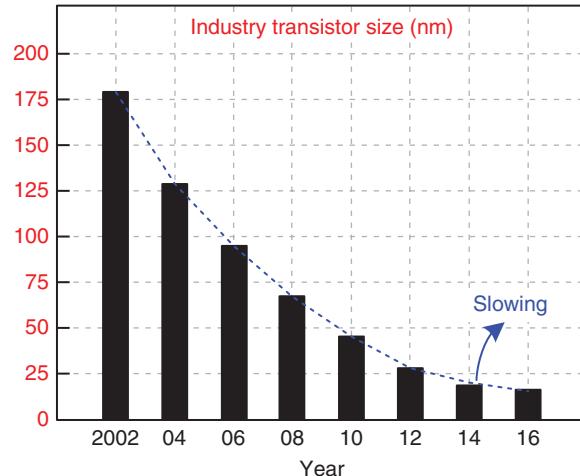
### 1.1 Moore's Law

Over the past few decades, the number of transistors per square inch on integrated circuits (ICs) has doubled every 18 months, which is the forecast of Moore's law and is a continuing condition. However, a physical limitation appears when the transistor size shrinks to 28 nm. Several technology performance boosters, for example dual stress liner (DSL) technology, strained silicon techniques, and the stress memorization technique (SMT), are required to retain the performance of transistors. The industry has failed to keep to the trend predicted by Moore's law. Figure 1.1 depicts how the rate of transistor size scaling has slowed down and is likely to break Moore's law by the end of 2015.

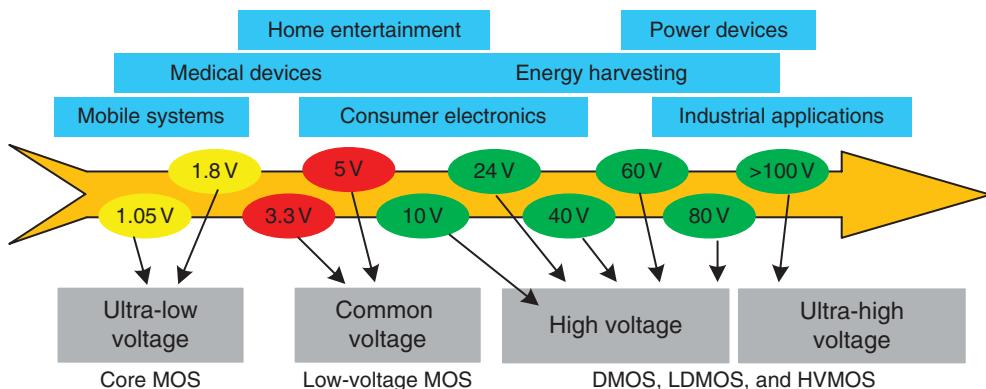
### 1.2 Technology Process Impact: Power Management IC from 0.5 micro-meter to 28 nano-meter

#### 1.2.1 MOSFET Structure

The voltage stress issue of metal–oxide–semiconductor field-effect transistors (MOSFETs) in drivers and power MOSFETs needs careful consideration. The evolution of MOSFETs and their applications are based on different input supply voltage (Figure 1.2). In advanced processes (i.e., 40, 28, and 22 nm), core MOSFETs with characteristics of small silicon size and high speed are used in low-voltage applications. Moreover, conventional low-voltage MOSFETs are applied for low supply voltage conditions in normal processes, such as 22 nm, 0.18  $\mu\text{m}$ , 0.25  $\mu\text{m}$ , and 0.5  $\mu\text{m}$ . Nevertheless, the drain-to-source voltage,  $V_{DS}$  of low-voltage MOSFETs cannot tolerate a high voltage and punches, and will break the MOSFET when the input supply voltage increases. Therefore, double-diffused metal–oxide–semiconductors (DMOSs), vertical



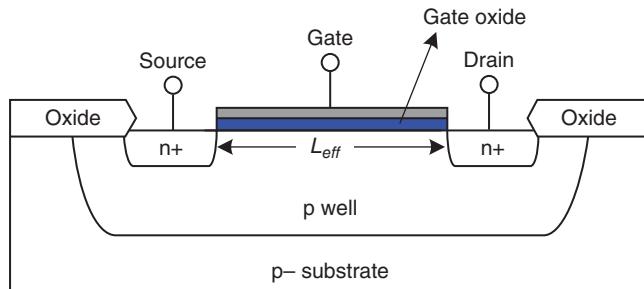
**Figure 1.1** Transistor size scaling rate has slowed down



**Figure 1.2** Evolution of MOSFETs and applications with different input supply voltages

double-diffused metal–oxide–semiconductors (VDMOSs), and laterally diffused metal–oxide–semiconductors (LDMOSs) are applied to bear a high  $V_{DS}$ . However, the gate-to-source voltage,  $V_{GS}$  of such MOSFETs cannot endure a high voltage, which will also damage the MOSFET. A high-voltage metal–oxide–semiconductor (HVMOS) solves the problem here, because its structure can tolerate a high voltage of both  $V_{DS}$  and  $V_{GS}$ .

The structures and characteristics of low-voltage MOSFETs, core MOSFETs, DMOSs, VDMOSs, LDMOSs, and HVMOSs are introduced in the following subsections, followed by a comparison of these MOSFETs.



**Figure 1.3** Structure of typical n-channel low-voltage MOSFET

### 1.2.1.1 Low-Voltage MOSFET

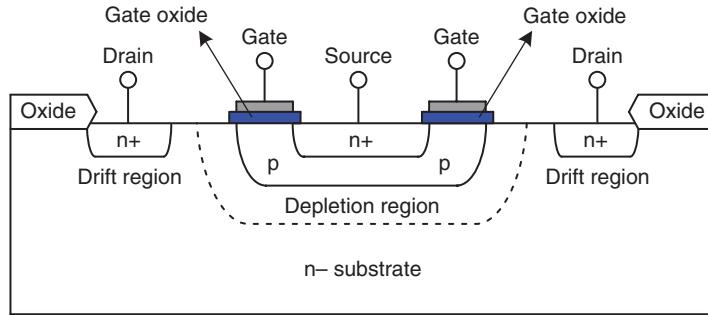
The structure of a typical n-channel low-voltage MOSFET is shown in Figure 1.3. Compared with LDMOSs and HVMOSs, the simple structure of a low-voltage MOSFET has the advantages of small silicon area and longest effective channel length ( $L_{eff}$ ), which is defined as the contact area between the p well and the gate in the n-channel low-voltage MOSFET. Moreover, a thin-gate oxide is designed to achieve the high-speed on-and-off switching of the MOSFET. However, this thin-gate oxide cannot bear the high voltage stress of the  $V_{GS}$ . Moreover, the  $V_{DS}$  only operates in low-voltage stress conditions, because the drift region of drain is too small to tolerate a high voltage of  $V_{DS}$ .

### 1.2.1.2 Core MOSFET

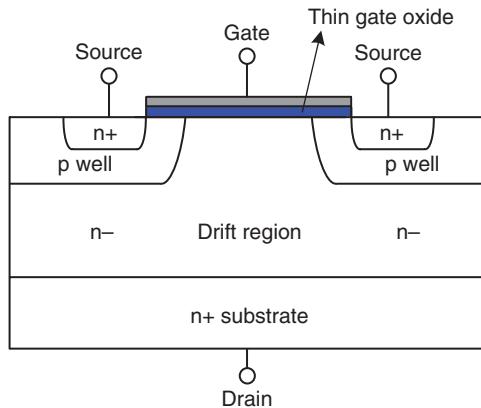
The integrated technique of system-on-chip (Soc) has improved. A core MOSFET with small silicon size reduces the silicon area and increases the operating speed of the Soc [1, 2]. Moreover, the supply voltage evaluates to 1.8 V, 1.05 V, or lower voltages to reduce the system's power dissipation. Therefore, the voltage stress of a core MOSFET cannot bear a conventional supply voltage, such as 3.3 or 5 V, because the oxide layer of the core MOSFET is thinner than that of a low-voltage MOSFET. Conventional supply voltages damage the thinner oxide layer.

### 1.2.1.3 Double-Diffused MOSFET

Figure 1.4 shows a DMOS structure [3, 4]. The effective channel length is produced by p-type diffusion and gate oxide. Moreover, the n-type substrate is very lightly doped in this structure. Light doping provides enough space for expansion of the depleted region between the p-type diffusion and the n+ drain contact regions. Therefore, the breakdown voltage between drain and source is enlarged. This structure can endure a high voltage of  $V_{DS}$  but not a high voltage of  $V_{GS}$ , because of its thin gate oxide.



**Figure 1.4** Structure of DMOS



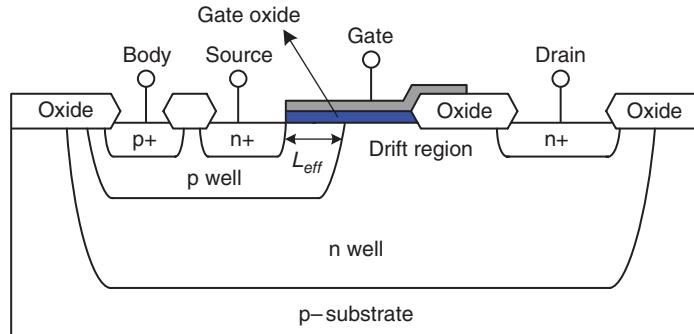
**Figure 1.5** Structure of VDMOS

#### 1.2.1.4 Vertical Double-Diffused MOSFET

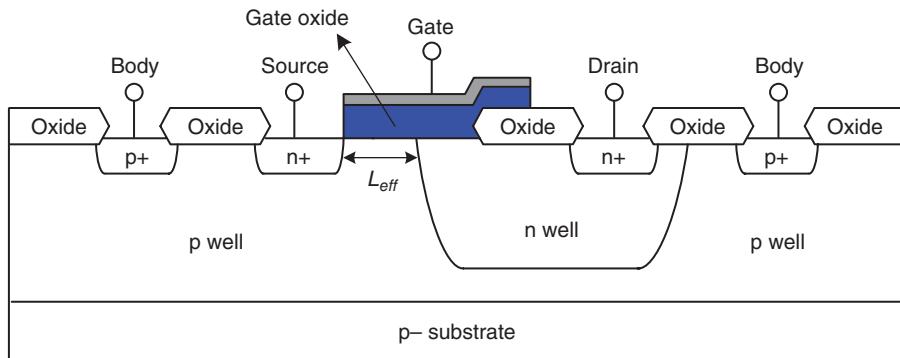
The VDMOS structure combines the concepts of vertical power structures and lateral double diffusion (Figure 1.5) [5]. The drain voltage is vertically supported by the n- layer. Moreover, current flows laterally from the source through the channel, which is parallel to the silicon surface, and then turns at a right angle to flow vertically down through the n- drain layer to the n+ substrate and the drain contact. An effective channel is formed, if a sufficiently positive gate voltage is applied, and the extra drift region of the n- layer can tolerate a high voltage of  $V_{DS}$ . However, the thin gate oxide cannot bear a high voltage of  $V_{GS}$ .

#### 1.2.1.5 Laterally Diffused MOSFET

LDMOS is also applied to solve the problem of high voltage  $V_{DS}$ . The structure of a typical n-channel LDMOS is similar to that of a low-voltage MOSFET, as shown in Figure 1.6 [6, 7]. The difference is that the LDMOS extends the drain drift region by adding an n-well



**Figure 1.6** Structure of typical n-channel LDMOS



**Figure 1.7** Structure of n-channel asymmetric HVMOS

layer to achieve the high-voltage stress tolerance of  $V_{DS}$ . Although this structure solves the high-voltage problem of  $V_{DS}$ , it has several disadvantages. The effective channel length defined by the p well underneath the gate is needed because of the drift extension for the wide drift region. Therefore, the structure causes a significant gate-to-drain overlap region and extends the silicon area, which is proportional to the cost. Moreover, the LDMOS is non-symmetric in the drain and source regions because the extended drift region and the overlap region are only designed on the drain side. However, the thickness of the LDMOS gate oxide is similar to that of a low-voltage MOSFET and cannot tolerate the high voltage of  $V_{GS}$ .

### 1.2.1.6 Asymmetric High-Voltage MOSFET

Asymmetric HVMOSs are applied for high-voltage processes to solve the high-voltage issue with both  $V_{GS}$  and  $V_{DS}$ . The structure of an n-channel asymmetric HVMOS is illustrated in Figure 1.7 [8, 9]. Similarly, an extra n well is used to stretch the drift region of the drain to bear the high voltage of  $V_{DS}$ . Therefore, a reduced effective channel length and gate-to-drain

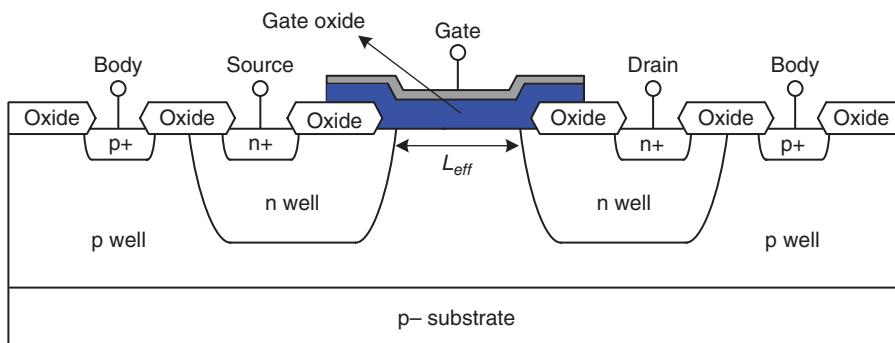
overlay region also occur in the HVMOS structure. Moreover, the thickness of the asymmetric HVMOS gate oxide is increased to extend the high-voltage tolerance of  $V_{GS}$ . However, the thicker gate oxide causes decreased on-and-off switching speed of the asymmetric HVMOS and results in longer system delay times. Furthermore, the silicon area of the asymmetric HVMOS is larger than that of the low-voltage MOSFET, DMOS, and LDMOS because of the extended drift region of the drain and the thicker gate oxide. This asymmetric HVMOS is also non-symmetric in the drain and source regions because only the drain has extended drift region. Consequently, the asymmetric HVMOS has many disadvantages, which decrease system efficiency and increase cost. However, the asymmetric HVMOS is necessary and the aforementioned disadvantages cannot be avoided when the system is in high  $V_{DS}$  and high  $V_{GS}$  conditions. Unfortunately, asymmetric HVMOSs cannot be used in cascade schemes because asymmetric HVMOSs cannot endure the high voltage of  $V_{SB}$ .

### 1.2.1.7 Symmetric High-Voltage MOSFET

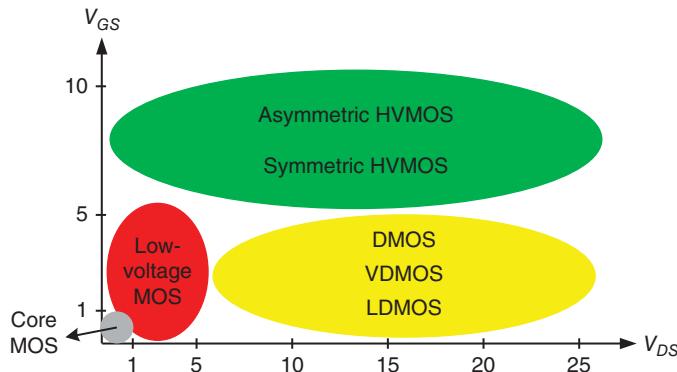
In a symmetric high-voltage MOSFET, the source region does not have an extra n well for the drift region compared with the drain region as shown in Figure 1.7. That is, the source-to-body region cannot tolerate the high-voltage condition. Thus, the symmetric HVMOS structure is preferred to extend the voltage stress tolerance of  $V_{SB}$ , as shown in Figure 1.8 [8, 9], and overcome this problem. The difference with this structure is that the source region of the symmetric HVMOS copies the same method as the drain region to solve the high-voltage issue of  $V_{SB}$ . Both the drain and source regions have an extra n well to endure the high voltage of  $V_{DS}$  and  $V_{SB}$ . Moreover, the gate oxide in the symmetric HVMOS is as thick as that in the asymmetric HVMOS for the high voltage of  $V_{GS}$ . Although the symmetric HVMOS can tolerate all high voltages of  $V_{DS}$ ,  $V_{GS}$ , and  $V_{SB}$ , its structure needs a large silicon area, which increases the cost.

### 1.2.1.8 Comparison

The advantages and disadvantages of low-voltage MOSFETs, core MOSFETs, DMOSs, LDMOSs, and HVMOSs are trade-offs in any design. Figure 1.9 shows different types of



**Figure 1.8** Structure of n-channel symmetric HVMOS



**Figure 1.9** Different types of MOSFETs with different values of  $V_{GS}$  and  $V_{DS}$

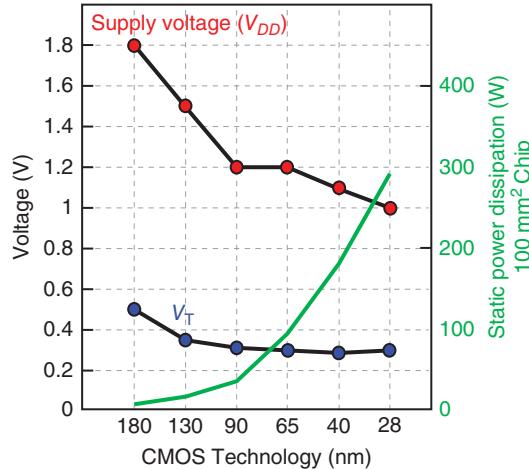
**Table 1.1** Comparison of different MOSFETs

|                     | Silicon area | High-voltage $V_{DS}$ | High-voltage $V_{GS}$ | High-voltage $V_{SB}$ |
|---------------------|--------------|-----------------------|-----------------------|-----------------------|
| Low-voltage MOSFET  | Small        | Damage                | Damage                | Damage                |
| Double DMOSFET      | Medium       | Safe                  | Damage                | Damage                |
| Vertical DMOSFET    | Medium       | Safe                  | Damage                | Damage                |
| Lateral DMOSFET     | Medium       | Safe                  | Damage                | Damage                |
| Asymmetric HVMOSFET | Large        | Safe                  | Safe                  | Damage                |
| Symmetric HVMOSFET  | Large        | Safe                  | Safe                  | Safe                  |

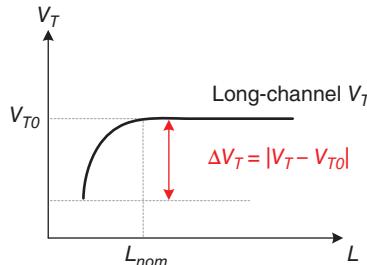
MOSFETs with different values of  $V_{GS}$  and  $V_{DS}$ . Choosing a suitable device under different supply voltage conditions from the different MOSFETs listed in Table 1.1 can achieve high efficiency and/or minimize the cost of the silicon area.

### 1.2.2 Scaling Effects

Given that complementary metal–oxide–semiconductor (CMOS) technology processes are downscaling, more transistors can be fabricated to reduce the cost of ICs. Electrical oxide thickness (EOT), parasitic capacitance, and nominal supply voltage also decrease with each new technology. Therefore, transistor operating speeds are increased and active power consumption is lowered. However, the threshold voltage ( $V_{th}$ ) cannot be scaled down simultaneously with the scaling down of the MOSFET gate length because the leakage current would be extremely large. Static power is increasing enormously, and cannot be neglected because the CMOS technology is continuously scaling down as shown in Figure 1.10. Furthermore, several scaling effects appear in short-channel devices, such as velocity saturation, hot carrier injection, large device mismatch, threshold voltage variations, and increased leakage current. In addition, the reduction of voltage rails, decreased dynamic range, and increased power density are challenges for designers – especially in analog circuit designs [10].



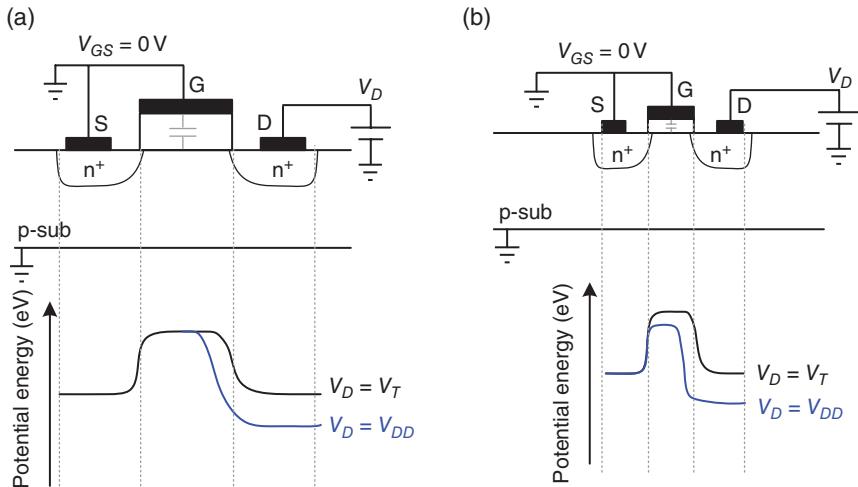
**Figure 1.10** Voltage decreasing and static power increasing vs. CMOS technology scaling down



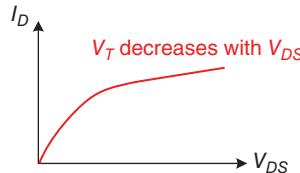
**Figure 1.11**  $V_{th}$  decreases with channel length;  $V_{th}$  roll-off effect

The distance from the source to the drain in short-channel devices is reduced, and thus the depletion regions from the drain and the source are closer. Therefore, as depicted in Figure 1.11,  $V_{th}$  decreases exponentially if the channel is shorter than a certain gate length ( $L_{nom}$ ), and the leakage current becomes unacceptable. This condition is known as the  $V_{th}$  roll-off effect, which circuit designers want to avoid. A first-order model describes that the effect of  $V_{th}$  roll-off is a function of EOT and substrate doping [2]. Therefore, increasing the substrate doping density to narrow the source/drain depletion region and scaling the EOT can minimize  $\Delta V_{th}$  in short-channel devices.

Both the vertical electric field ( $V_{GS}$ ) and the horizontal electric field ( $V_{DS}$ ) can change the channel potential in short-channel devices. Figure 1.12(a) shows that the potential energy of a long-channel device is independent of the drain voltage. The potential barrier of a long-channel device is only controlled by its gate voltage. As Figure 1.12(b) shows, the potential energy of a short-channel device is also affected by its drain voltage. Both gate/source and drain/source voltages can affect the drain current. Given that the x–y electric fields are coupled, the transistor can conduct electrons even if the gate voltage is smaller than  $V_{th}$ . Therefore,  $V_{th}$



**Figure 1.12** (a) Potential energy of long-channel device. (b) Potential energy of short-channel device



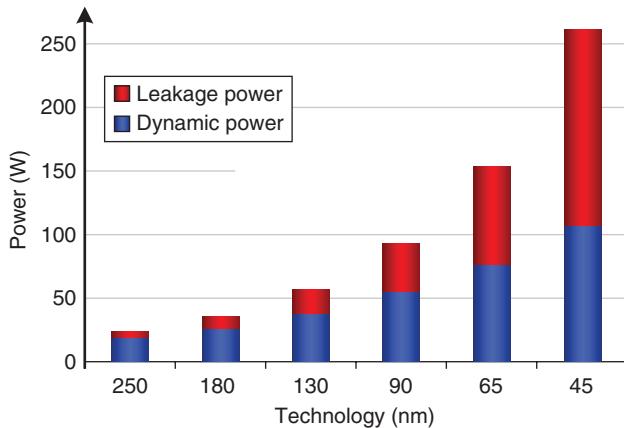
**Figure 1.13** Drain current increases with  $V_{DS}$  in DIBL effect

decreases as the drain bias voltage increases. This phenomenon is known as the drain-induced barrier lowering (DIBL) effect. It is defined by Eq. (1.1) and shown in Figure 1.13:

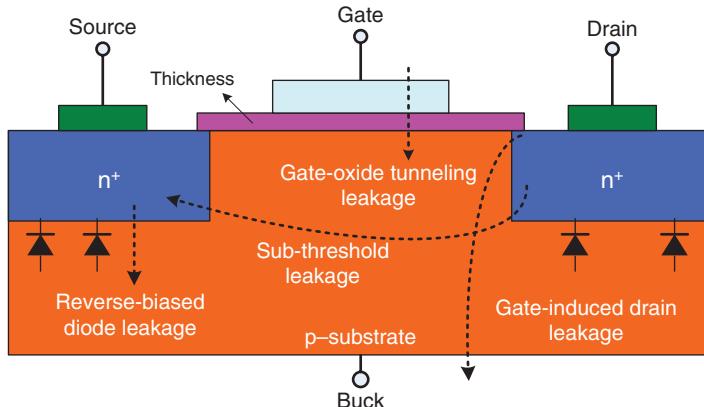
$$DIBL \equiv \frac{|\Delta V_{th}|}{|\Delta V_{DS}|} \quad (1.1)$$

### 1.2.3 Leakage Power Dissipation

Deep sub-micrometer technology integrates high density and diversity of circuit functions on the same chip. This integration has changed the concept of power consumption compared with that in conventional long-channel transistors. The power dissipation trend shows that leakage power accounts for almost one-third of total power consumption among processes below 130 nm, as shown in Figure 1.14. With the continuous scaling down of technology, the supply voltage decreases to meet the requirements of power density and system reliability, but the leakage current increases exponentially.

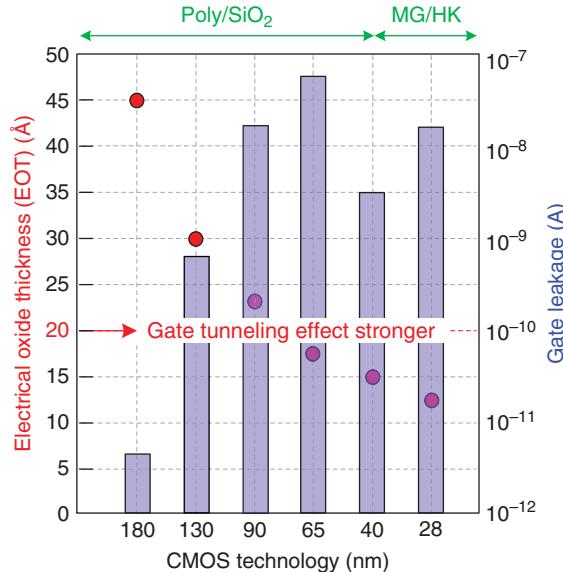


**Figure 1.14** Trend of dynamic and leakage power dissipation [11]



**Figure 1.15** Leakage current path in short-channel devices

A major concern in scaling channel size effects is that the gradual increase of leakage current leads to large static power [12, 13]. Static power needs to be carefully considered, because its value affects operation and performance. Figure 1.15 shows the leakage current in short-channel devices. Given the threshold voltage  $V_{th}$  scaling the non-ideal off-state characteristics of a transistor, sub-threshold current is constantly drawn from the power supply to the ground, even when a transistor operates in the cut-off region. Furthermore, a thinner gate-oxide structure is necessary to control the short-channel effect (SCE) and maintain the transistor driving strength under low supply voltage. The structure also increases the gate leakage current. Thus, the primary leakage currents are sub-threshold and gate-oxide tunneling leakage currents in deep sub-micrometer CMOS circuits. The leakage current includes the gate direct-tunneling leakage current ( $I_G$ ), the gate-induced drain leakage current ( $I_{GIDL}$ ), the reverse-biased junction leakage current ( $I_{REV}$ ), and the sub-threshold or weak-inversion leakage current ( $I_{SUB}$ ).  $I_{GIDL}$  is

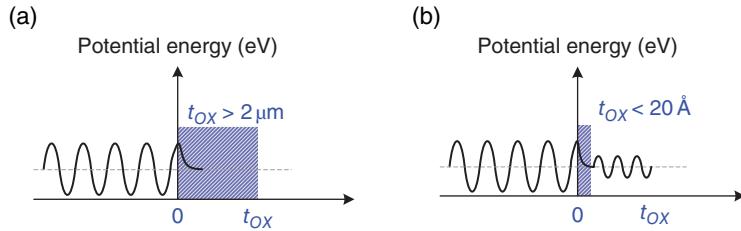


**Figure 1.16** Gate leakage increases with CMOS technology trends from 0.18  $\mu\text{m}$  to 65 nm when the oxide thickness scales down

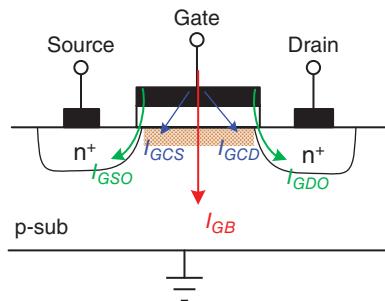
caused by a large horizontal electric field in the overlapping region between drain and gate. It occurs from drain to substrate and increases with higher drain voltage.  $I_{REV}$  occurs because p–n junctions are heavily doped in short-channel devices. It is also known as band-to-band tunneling and increases as the transistor feature size decreases continuously [14].

The leakage current of an off-state transistor ( $I_{OFF}$ ) indicates  $V_{GS} = 0 \text{ V}$  and  $I_G = 0$ . Thus, its value is equal to the summation of  $I_{GIDL} + I_{REV} + I_{SUB}$ . Figure 1.16 shows that the gate leakage increases with CMOS technology trends from 0.18  $\mu\text{m}$  to 65 nm because the oxide thickness continuously scales down. However, the leakage current decreases significantly for a 40 nm CMOS process, because of several performance boosters. However, the current's value increases continuously if the channel length scales down constantly from 40 to 28 nm. High- $k$ /metal gate (HK/MG) technology was introduced in 2006; they use high- $k$  dielectric materials, such as  $\text{TiO}_2$  and  $\text{Ta}_2\text{O}_5$ , and reduce the gate-oxide leakage current. The reason for this is that a high- $k$  dielectric allows a less aggressive reduction in gate dielectric thickness and obtains the required gate overdrive even under low supply voltage operation in deep sub-micron CMOS technologies. The HK/MG is an effective technique to reduce leakage currents and has excellent gate control compared with conventional silicon-dioxide gate insulators. Figure 1.17(b) shows that the quantum tunneling effect of electrons/holes occurs and causes  $I_G$  to become larger than that in Figure 1.17(a) without quantum tunneling effect, when the EOT is smaller than 20 Å. The quantum tunneling effect is a major source of leakage current in deep sub-micron CMOS technologies. The leakage current is still a serious factor, which cannot be ignored in deep sub-micron CMOS technologies, although the introduction of HK/MG technology can reduce  $I_G$ .

As depicted in Figure 1.18, the gate-oxide tunneling leakage current is composed of leakage from the gate to the channel, including gate-to-source leakage current ( $I_{GCS}$ ) and gate-to-drain



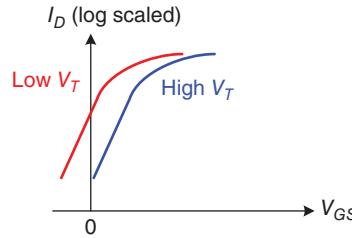
**Figure 1.17** (a) Tunneling effect in long-channel devices. (b) Tunneling effect in short-channel devices



**Figure 1.18** Composition of gate-oxide leakage current

leakage current ( $I_{GCD}$ ), leakage from gate oxide to source ( $I_{GSO}$ ) or drain overlapping regions ( $I_{GDO}$ ), and leakage from gate to substrate or vice versa ( $I_{GB}$ ) [15]. Aggressive scaling down of the gate-oxide thickness increases the electric field oxide across the gate insulator and results in electron tunneling from gate to substrate or vice versa. The resulting current is called the gate-oxide tunneling current, which is the major leakage current in nanometer CMOS technology. Two mechanisms are responsible for this phenomenon. The first is called the Fowler–Nordheim (FN) tunneling mechanism, in which electrons tunnel into the conduction band of the oxide layer. Direct tunneling is more dominant than the FN tunneling mechanism. Here, the electrons tunnel directly to the gate through the forbidden energy gap of the silicon-dioxide layer, which appears when the gap is less than 3–4 nm thick. The resulting current is called the gate direct-tunneling leakage current, and it flows from the gate through the oxide insulation to the substrate or vice versa. Mechanisms for direct tunneling include electron tunneling in the conduction band, electron tunneling in the valence band, and hole tunneling in the valence band. The dominant source of leakage is the direct tunneling of electrons through the gate oxide [16]. This leakage current depends exponentially on the oxide thickness and the supply voltage, as expressed in Eq. (1.2), where:  $E_{ox}$  is the electric field across the oxide;  $W$  and  $L$  are the effective transistor width and length, respectively;  $A = q^3/16\pi^2 h\Phi_{ox}$ ,  $B = 4\pi\Phi_{ox}^{1.2}(2m_{ox})^{0.5}/3hq$ ,  $m_{ox}$  is the effective mass of the tunneling particle,  $\Phi_{ox}$  is the tunneling barrier height,  $h$  is  $\pi/2$  times Planck's constant, and  $q$  is the electron charge. Moreover, the tunneling current exists in both the on-state and the off-state of the MOSFET:

$$I_{gox} = W \cdot L \cdot A \cdot E_{ox}^2 \cdot e^{-B/E_{ox}} \quad (1.2)$$



**Figure 1.19**  $I_D$  vs.  $V_{GS}$  under different  $V_{th}$  shows the trade-off between operation speed and leakage current for circuit designers

The dominant leakage current among three parts of  $I_{OFF}$  is  $I_{SUB}$ , resulting in drain/source current for a MOSFET in weak inversion. Sub-threshold leakage is the drain/source current of a transistor during operation in weak inversion, where transistors continue to turn on despite the gate-source voltage being below the threshold voltage. Sub-threshold conduction occurs, unlike for a strong inversion region, in which the drift current dominates because of the diffusion current of the minority carriers in the channel of a MOSFET device. This condition occurs for several reasons. First is the weak inversion effect. Carriers move by diffusion along the surface, similar to when the gate voltage is below  $V_{th}$ , allowing charge transport across the base of the bipolar transistors. The weak inversion current becomes significant when the gate-to-source voltage is lower than, but close to, the threshold voltage of the device. Second is the DIBL effect, which is the reduction of the threshold voltage of the transistor at higher drain voltages.  $I_{SUB}$  increases exponentially as  $V_{th}$  decreases and/or as  $T$  increases, Eq. (1.3).  $\eta$  is a factor depending on the channel length, and is between 1 and 2;  $q$  is the charge on an electron;  $k$  is Boltzmann's constant;  $T$  is temperature;  $W$  and  $L$  are the width and length of the MOSFET, respectively [2]:

$$I_{DS} (\text{nA}) = 100 \cdot \frac{W}{L} \cdot e^{q(V_{GS} - V_{th})/\eta kT} \quad (1.3)$$

$I_{SUB}$  is strongly sensitive to process, supply voltage, and temperature variation. Circuit designers aim for a low  $V_{th}$  to achieve a fast transient response and a high drain/source current in strong inversion, as depicted in Figure 1.19. In contrast, a high  $V_{th}$  is required for a low leakage current off-state. A trade-off occurs between operation speed and leakage current, which explains why  $V_{th}$  cannot be reduced as the gate length continues to scale down.

Parasitic diodes exist between the source/drain diffusion region and the substrate in one transistor, as depicted in Figure 1.15. These parasitic-diode p–n junctions must be reverse-biased for proper transistor operation. This condition results from minority carrier diffusion and drift near the edge of depletion regions, and also from the generation of electron–hole pairs in the depletion regions of reverse-bias junctions. This results in the leading transistor consuming power in the form of a reverse-bias current  $I_{REV}$ , which is drawn from the power supply. The current magnitude depends on the area of source/drain diffusion and the current density, which in turn is determined by the doping concentration. Highly doped shallow junctions and halo doping, necessary to control SCEs in nanometer devices, have escalated the leakage

**Table 1.2** Transistor leakage in short-channel devices

| Leakage current | Influence  | Existence              | Solutions                   |
|-----------------|------------|------------------------|-----------------------------|
| $I_G$           | Large      | On-state and off-state | HK/MG                       |
| $I_{SUB}$       | Large      | Off-state              | Higher $V_{th}$             |
| $I_{REV}$       | Very small | On-state and off-state | Dopant profile optimization |
| $I_{GIDL}$      | Small      | Off-state              | Dopant profile optimization |

current. Thus, the electron tunneling effect across the p–n junction causes junction leakage. The currents can be expressed as in Eqs. (1.4) and (1.5) [17]:

$$I_{BD} = A \cdot J_s \cdot (e^{q \cdot V_{BD}/kT} - 1) \quad (1.4)$$

$$I_{BS} = A \cdot J_s \cdot (e^{q \cdot V_{BS}/kT} - 1) \quad (1.5)$$

where  $A$  is the area of the junction,  $J_s$  is the reverse saturation current density,  $V_{BD}$  and  $V_{BS}$  are the reverse bias voltage across the junction, and  $kT/q$  is the thermal voltage. Reverse-biased diode leakage further becomes crucial if the source/drain region continues to be heavily doped.

$I_{GIDL}$  is caused by a high field effect in the drain junction of MOS transistors. The silicon surface in an NMOS transistor has almost the same potential as the p-type substrate, and acts like a p region because of the heavier doping than the substrate when the gate is biased to form an accumulation layer in the silicon surface under the gate. A dramatic increase in some effects, such as avalanche multiplication and band-to-band tunneling, can be observed when the gate is at zero or negative voltage, and the drain is at the supply voltage level. Minority carriers underneath the gate are swept to the substrate to form the  $I_{GIDL}$  path, as shown in Eq. (1.6) [18]. A higher supply voltage and a thinner oxide lead to an increased  $I_{GIDL}$ , as shown in Eq. (1.6), where  $A$  is a pre-exponential parameter,  $B$  (typically 23–70 MV/cm) is a physically based exponential parameter, and  $E_s$  is the transverse electric field at the surface depending on operating voltage and gate-oxide thickness:

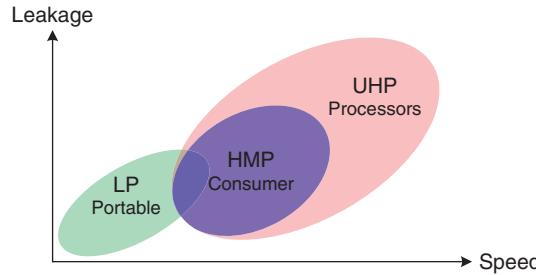
$$I_{GIDL} = A \cdot E_s \cdot e^{-B/E_s} \quad (1.6)$$

The steep doping profile that occurs at the drain edge increases the band-to-band tunneling currents, especially as the drain/bulk voltage increases. Therefore, a thinner oxide and a higher supply voltage increase  $I_{GIDL}$  drastically. Controlling the doping concentration in the drain of the transistor is the best way to control  $I_{GIDL}$ . Table 1.2 summarizes the contribution of leakage currents in short-channel devices. Corresponding solutions are also listed.

### 1.3 Challenge of Power Management IC in Advanced Technological Products

#### 1.3.1 Multi- $V_{th}$ Technology

The power density increases continuously with the scaling down of the gate length. Thus, multiple-threshold voltage (multi- $V_{th}$ ) ICs have been widely used to optimize power and maintain



**Figure 1.20** Trade-off between operation speed and leakage current

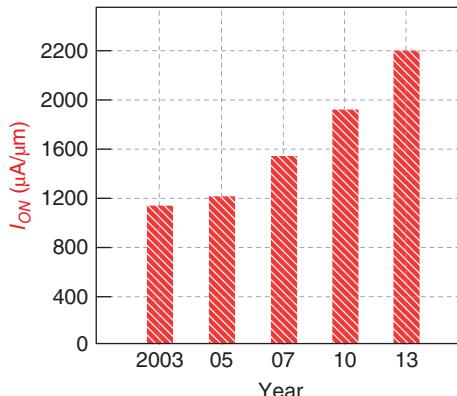
**Table 1.3** Performance optimization strategies

| Requirement                   | Chosen devices    | Design methodology   |
|-------------------------------|-------------------|--|
| Ultra-high performance        | U-LVT/LVT/<br>RVT | 1. Simulated with U-LVT and LVT<br>2. Replaced by RVT on non-critical path |
| High performance medium power | LVT/RVT           | 1. Simulated with LVT<br>2. Replaced by RVT on non-critical path           |
| Low power                     | HVT/RVT           | 1. Simulated with HVT<br>2. Replaced by RVT on large-timing path           |

operation speed in various industries. Long-channel devices in previous CMOS technologies utilized a  $V_{th}$  implant to dominate the threshold voltage. Today, multi-threshold devices in deep sub-micron CMOS technologies are fabricated with different channel length and halo implantation optimization. The area cost and layout blueprint are similar to those for high-threshold voltage (HVT) and low-threshold voltage (LVT) devices. This convenience enables circuit designers to implement multi- $V_{th}$  ICs. As illustrated in Figure 1.20, a trade-off exists between operating speed and leakage current among different products. For example, in ultra-high-performance applications, processors in mobile phones are dominated by ultra-low-threshold voltage (U-LVT) devices with selective LVT devices or regular-threshold voltage (RVT) devices on non-critical paths. Table 1.3 summarizes the choice of several devices with corresponding requirements and design methodologies.

### 1.3.2 Performance Boosters

In Figure 1.21, the transistor on-state current density ( $I_{ON}$ ) continues to increase because strained-silicon technologies are introduced around a 90 nm node. Continuing  $I_{ON}$  improvement is related to a growing range of performance boosters, as listed in Table 1.4. Some techniques, such as the contact-etch-stop-liner (CESL) technique, SMT, and embedded silicon-germanium (eSiGe) technologies for improving the PMOS transistor, are used to enhance 90 and 65 nm processes. The CESL technique provides tension and compression to NMOS and PMOS transistors, respectively, to significantly improve mobility [19]. For CMOS



**Figure 1.21** Trends of  $I_{ON}$  in NMOS

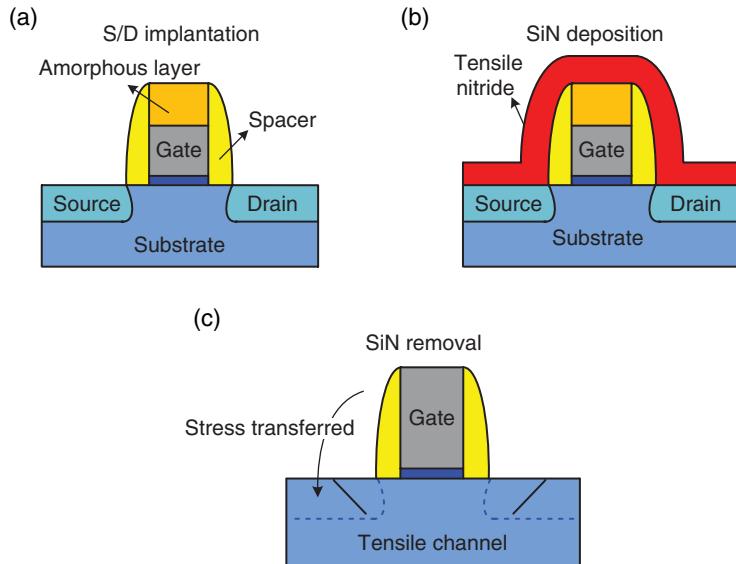
**Table 1.4** Performance boosters vs. technology node

| Performance boosters | 90 nm | 65 nm | 40 nm | 28 nm |
|----------------------|-------|-------|-------|-------|
| CESL                 | ✓     | ✓     | ✗     | ✗     |
| SMT                  | ✗     | ✗     | ✓     | ✓     |
| eSiGe for PMOS       | ✓     | ✓     | ✓     | ✓     |
| SiC for NMOS         | ✗     | ✗     | ✓     | ✓     |
| DSL                  | ✗     | ✗     | ✓     | ✓     |
| HK/MG technology     | ✗     | ✗     | ✓     | ✓     |

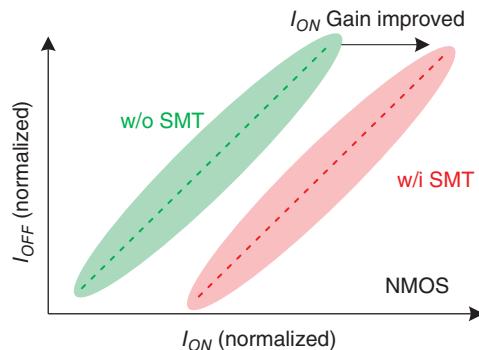
technologies below 65 nm, SMT is introduced and widely used to boost the performance of NMOS transistors. SMT can result in longitudinal tensile stress, which is good for NMOS mobility [20]. A brief description of SMT formation is provided in Figure 1.22(a)–(c) [21]. Tensile nitride is formed after the S/D implantation as SiN deposition. SMT formation can be achieved after the removal of SiN. Moreover, Figure 1.23 shows trends of NMOS  $I_{ON}$  with SMT. However, SMT cannot be used in metal gates, which is an important trend in relation to the technology below the 40 nm node.

In further advanced technologies, such as 40 and 28 nm, SiC for improving the NMOS transistor, the DSL technique, and the HK/MG technique are employed to improve device performance. Moreover, Figure 1.24(a), (b) shows the dimension in 2D and the cross-section of the device, respectively. PMOS and NMOS have each aimed for a uniaxial stress direction to improve the performance, as shown in Table 1.5.

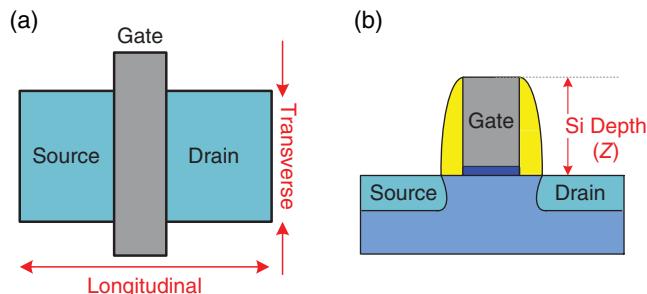
Moreover, an embedded source/drain stressor for the PMOS transistor in a 90 nm process is introduced and known as eSiGe S/D technology, as shown in Figure 1.25(a). This technology provides longitudinal compressive stress for PMOS mobility but has no influence on NMOS. However, it has drawbacks, such as a larger junction leakage [23]. Thus, a  $\text{Si}_3\text{N}_4$  cap layer is utilized in the 40 nm process to enhance NMOS mobility. The  $\text{Si}_3\text{N}_4$  cap layer can provide longitudinal tensile stress. Figure 1.25(b) shows the NMOS transistor with its corresponding stressor. The DSL technology in Figure 1.26 is used to boost the performance of a different type



**Figure 1.22** Brief description of SMT formation: (a) S/D implantation; (b) SiN deposition; (c) SiN removal



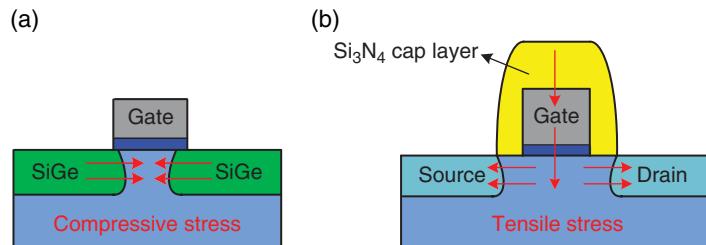
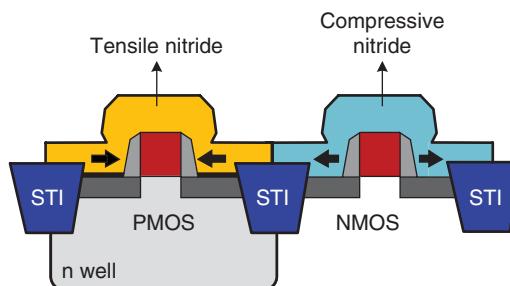
**Figure 1.23** Trends of NMOS  $I_{ON}$  with SMT



**Figure 1.24** Direction of stress to transistor: (a) longitudinal and transverse; (b) Z-direction [22]

**Table 1.5** Desired stress in CMOS process [22]

| Direction    | NMOS        | PMOS        |
|--------------|-------------|-------------|
| Longitudinal | Tensile     | Compressive |
| Transverse   | Tensile     | Tensile     |
| Si-depth (Z) | Compressive | Tensile     |

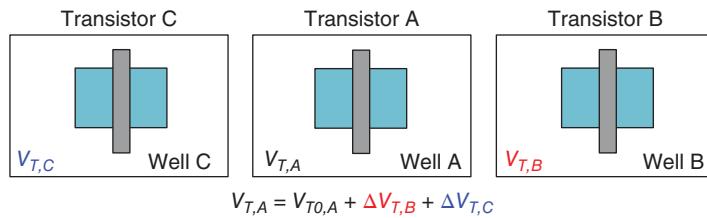
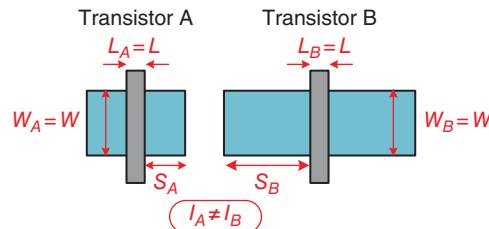
**Figure 1.25** MOSFET with each corresponding stressor: (a) compressive stress for PMOS transistor; (b) tensile stress for NMOS transistor**Figure 1.26** DSL technology for both NMOS and PMOS transistors

of MOSFET, because this DSL technology applies a SiN film to create tensile stress on the NMOS transistor and compressive stress on the PMOS transistor.

Gate leakage has become a major problem when the EOT is scaled below 20Å. Moreover, dopant penetration and dielectric degradation occur [24]. For a continuously scaled down EOT, the integration of HK/MG technology in a 40/28 nm node significantly improves the performance in terms of gate leakage reduction. HK/MG technology utilizes a high- $k$  dielectric to increase the gate-oxide capacitance ( $C_{OX}$ ), although it has already been increased by scaling down the EOT. A higher on-state driving current with increased  $C_{OX}$  ensures improved performance. Thus, HK/MG technology is widely used in ultra-high-performance products. There are two main integration methods for HK/MG technology: gate-first metal-inserted-poly-Si gate (MIPS) and gate-last replaced metal gate (RMG). The main difference between these two methods is that the metal electrode is deposited either before or after the high-temperature activation anneals during fabrication. Both methods are under continuing development. A comparison of the two methods is presented in Table 1.6 [25–30].

**Table 1.6** Comparison table for two HK/MG approaches [25–30]

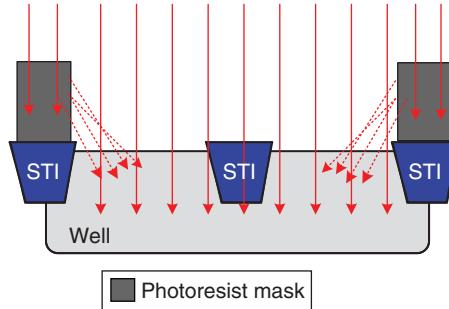
|                      | MIPS  | RMG           |
|----------------------|-------|---------------|
| High- $k$ dielectric | First | First or last |
| Metal gate           | First | Last          |
| Thermal budget       | High  | Low           |
| EOT                  | Thick | Thin          |
| Mobility             | Low   | High          |
| Process complexity   | Low   | High          |
| Cost                 | Low   | High          |

**Figure 1.27** Explanation of layout-dependent proximity effect**Figure 1.28** Explanation of LOD effect

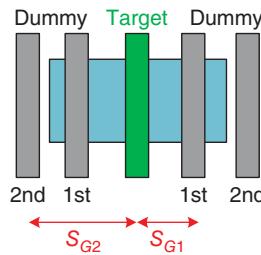
### 1.3.3 Layout-Dependent Proximity Effects

Given the nanometer CMOS technology, a growing number of transistors have been fabricated on the same well. Transistors are very close to each other and induce several layout-dependent proximity effects. These effects are unintentional and contrary to the intentional stress effect introduced in Section 1.2.2, because transistors interact with each other. Figure 1.27 shows a simple example in which the threshold voltage can be changed by neighboring transistors. Proximity effects can degrade the on-state current and shift the threshold voltage.

The length of diffusion (LOD) effect is caused by mechanical compressive stress induced by shallow trench isolation (STI), which is used to isolate devices and produce compressive stress as the wafer cools down [31]. The LOD effect with different diffusion length can cause a current difference even if transistors have the same length and width, as shown in Figure 1.28. However, the well proximity effect (WPE), as shown in Figure 1.29, is induced because



**Figure 1.29** Explanation of WPE effect



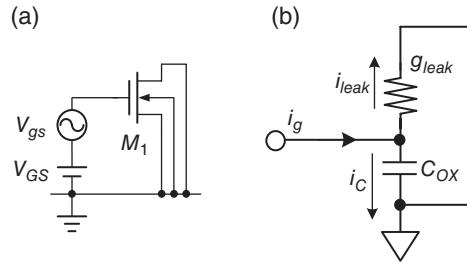
**Figure 1.30** Explanation of PSE effect

high-energy dopant ions scatter into the well edge from the edge of the photoresist mask [32]. Therefore, transistors exhibit a difference in threshold voltage  $V_{th}$  because different distances from a well edge.  $V_{th,A}$  is affected by the variations of  $V_{th,B}$  and  $V_{th,C}$ . A polyspace effect (PSE) is caused by the first or second neighboring polylines, as shown in Figure 1.30. Transistors with minimum poly-to-poly spacing have a large variation in  $V_{th}$  and on-state current. Designers today have to focus on minimizing layout-dependent proximity effects during layout and post-simulation to ensure chip quality in nanometer technologies.

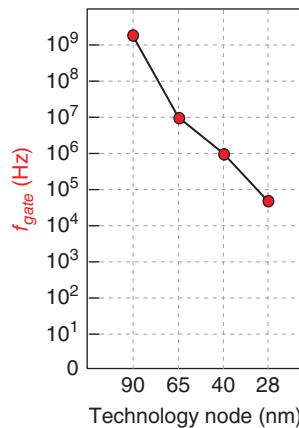
### 1.3.4 Impacts on Circuit Design

Nanometer devices cause impacts on physical limitations and IC design, especially analog IC design. As mentioned in Section 1.2.1, the major problem is gate tunneling leakage as transistors are continuously scaling down. The gate-leakage tunneling current can introduce a low-frequency pole ( $f_{gate}$ ) and degrade system stability, transient response time, and voltage variation.

The degradation of the loop filter of a phase-lock-loop (PLL) can enlarge the frequency variation [33]. A test circuit diagram of gate tunneling current is shown in Figure 1.31(a), and its small signal model is shown in Figure 1.31(b), where the gate-leakage tunneling current ( $i_C$ ) is through  $C_{ox}$  and depends on the input signal frequency. The total gate leakage is composed of  $i_{leak}$  and  $i_C$ , where  $i_{leak}$  is the gate leakage that is not caused by the tunneling effect. Therefore, two current components have the same magnitude at one certain frequency ( $f_{gate}$ ).  $f_{gate}$  can be



**Figure 1.31** Test diagrams of  $f_{gate}$  because of gate leakage current: (a) circuit diagram; (b) small signal equivalent model



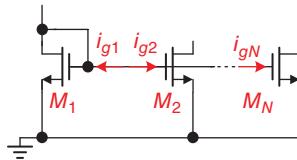
**Figure 1.32** Trends of  $f_{gate}$  vs. technology node

estimated as expressed in Eq. (1.7) [34]. Figure 1.32 explains that  $f_{gate}$  is lowered because of the enlarged gate-tunneling leakage current and has to be considered because the technology node scales down continuously. Moreover, Figure 1.33 shows that the gate-tunneling leakage also enlarges the mismatch among current mirrored transistors:

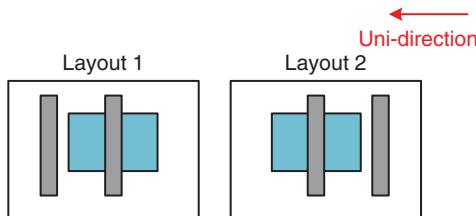
$$f_{gate} = \frac{1}{2\pi C_{IN}(g_{Leakage})} \quad (1.7)$$

Another major change is that the characteristics of transistor symmetry break down in deep sub-micron technologies. For example, all poly gates of core devices in a 28 nm process must be in the vertical direction, and a single transistor can be influenced by other transistors several micrometers away. A simple description of a broken-down symmetry is shown in Figure 1.34.

Analog designers widely utilize certain digital circuits or circuit techniques to minimize device mismatch and solve the mismatch problems that accompany process scaling. For example, digital circuits, such as trimming logic and auto-calibration circuits, are widely inserted into critical analog systems or feedback loops. The requirements of a digital



**Figure 1.33** Current mirror mismatch because of gate current leakage



**Figure 1.34** Symmetry breaking down in deep sub-micron technology

temperature sensor are increased, because temperature variation is a significant factor in scaling effects. Moreover, a circuit technique, such as stack devices, is proposed to minimize the leakage current. Therefore, the trends of scaling devices continue to challenge circuit designers in complex ways.

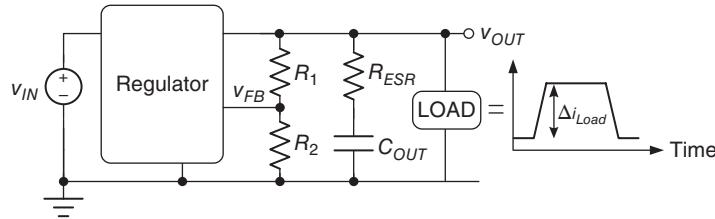
## 1.4 Basic Definition Principles in Power Management Module

Some commonly used design specifications are defined to evaluate the performance of power management modules. These design specifications include both transient and steady-state performance.

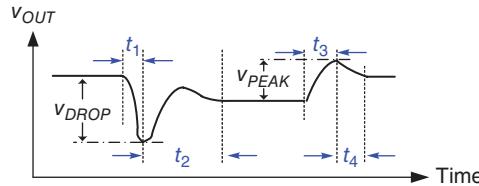
### 1.4.1 Load Regulation

Load regulation, as defined in Eq. (1.8), is one of the steady-state performances that influence output voltage accuracy. Different load conditions indicate the voltage regulation ability of the power management module. A smaller value of the load regulation ensures higher precision of the output voltage. Load regulation is related to the open-loop gain of the converter. Therefore, higher open-loop gain is required to ensure better regulation, but the system stability worsens. Compensation techniques need a relationship between input variation and output voltage regulation. A small value of the line regulation indicates better immunity in case of input voltage variation. Consequently, good line regulation performance leads to robust operation against the input supply variation:

$$\text{Line regulation} = \frac{\Delta v_{OUT}}{\Delta v_{IN}} (V/V) \quad (1.8)$$



**Figure 1.35** Illustration of time domain analysis for load transient response



**Figure 1.36** Output voltage waveform of load transient response in regulator

#### 1.4.2 Transient Voltage Variations

Distinct operating modes in Soc applications cause different transient responses. The power management module needs to handle a versatile load transient response and ensure high performance of the Soc. A good transient response implies a small voltage transient variation and a fast settling time at the output voltage when a sudden load change occurs. System bandwidth determines the performance of the transient response. That is, a wide system bandwidth indicates a short response time contributed by a fast control loop in the power management module. Frequency domain and time domain analyses are performed to further achieve transient response.

In the frequency domain analysis of a power management module, the position of the poles and zeros leads to distinct responses when the transient load occurs. A large system bandwidth and a fast response time would be obtained if the system dominant pole is set at a higher frequency region; however, stability is difficult to guarantee. A slow transient response time is derived once the dominant pole is set at low frequencies; nevertheless, stable operation can be ensured easily. To correctly refer to the frequency domain analysis, an illustration of time domain analysis for the load transient response is shown in Figure 1.35. The output node usually contains a feedback voltage divider (\$R\_1\$ and \$R\_2\$), an output capacitor (\$C\_{OUT}\$), and its equivalent series resistance (\$R\_{ESR}\$). The output voltage waveform of the load transient response is shown in Figure 1.36. When the load transient response occurs in case of a light-to-heavy load change, the transient period \$t\_1\$ and the drop voltage \$v\_{DROP}\$ are determined by the system bandwidth and the output capacitor \$C\_{OUT}\$ with its equivalent series resistance \$R\_{ESR}\$. The output capacitor functions as a current source to sustain the request for the output load current. The voltage drop \$v\_{DROP}\$ in the load transient response can be formulated as:

$$v_{DROP} = v_{ESR} + v_{cap} = \Delta i_{OUT} R_{ESR} + \frac{\Delta i_{OUT} \cdot t_1}{C_{OUT}} \quad (1.9)$$

The transient period  $t_2$  is determined by the time during which the high-side power switch can charge the output capacitor back to its regulated voltage. The phase margin of the control loop and any pole/zero doublets affect the transient settling time. The total period, containing  $t_1$  and  $t_2$ , is known as the transient recovery time. The voltage variation  $v_{PEAK}$  occurs when the output load suddenly changes from heavy to light load. The determination of the transient periods,  $t_3$  and  $t_4$ , is similar to that of the transient periods,  $t_1$  and  $t_2$ , respectively. The voltage  $v_{PEAK}$  in the load transient response can also be formulated as:

$$v_{PEAK} = v_{ESR} + v_{cap} = \Delta i_{OUT} R_{ESR} + \frac{\Delta i_{OUT} \cdot t_3}{C_{OUT}} \quad (1.10)$$

### 1.4.3 Conduction Loss and Switching Loss

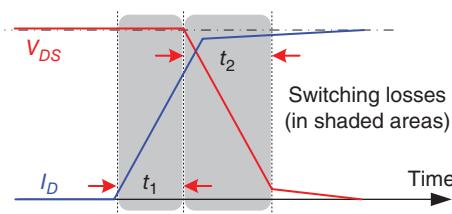
Given the large driving current flowing through the power stage of the power management module, the conduction loss obviously affects the power conversion efficiency. The conduction loss of the high-side power switch in the buck converter can be expressed as in Eq. (1.11). The on-resistance of the high-side power switch  $R_{onp}$  is inversely proportional to the power transistor size:

$$P_{conH} = (i_{LOAD})^2 \cdot R_{onp} \cdot \frac{v_{OUT}}{v_{IN}} \quad (1.11)$$

The conduction loss of the low-side power switch in the buck converter can be shown as in Eq. (1.12), with the low-side power switch on-resistance  $R_{onn}$ :

$$P_{conL} = (i_{LOAD})^2 \cdot R_{onn} \cdot \frac{v_{IN} - v_{OUT}}{v_{IN}} \quad (1.12)$$

A trade-off is observed between the conduction loss and the active silicon area. The utilization of large power switches directly reduces the conduction loss at the power stage, but the cost also increases because of the large silicon area. The switching loss results from the switching interval of the power switches. As depicted in Figure 1.37, the switching loss is proportional to the input voltage  $v_{IN}$  and the load current  $i_{OUT}$  in the buck converter. When the power switches turn on, the driving current increases, whereas the voltage across the drain and source of the power switch decreases. That is, the intersection of the conducting current and the voltage drop



**Figure 1.37** Illustration of switching loss of power switch

across the power switch causes power loss during the switching period. The switching loss during the period  $t_1$  in the switching operation of the power switch can be obtained as:

$$P_{swt1} = \frac{1}{2}(v_{IN} \cdot i_{LOAD}) \cdot t_1 \quad (1.13)$$

When the conducting current rises to its target value, the current is sustained, whereas the drop in voltage across the power switch decreases. Similarly, the switching loss derived during the period  $t_2$  in the switching operation is shown as:

$$P_{swt2} = \frac{1}{2}(v_{IN} \cdot i_{LOAD}) \cdot t_2 \quad (1.14)$$

The switching loss in one switching operation of one power switch is the summation of  $P_{swt1}$  and  $P_{swt2}$ . The total switching loss of one power switch with a constant switching frequency  $f_{sw}$  in the power management module can be expressed as:

$$P_{sw} = P_{swt1} + P_{swt2} = (v_{IN} \cdot i_{LOAD}) \cdot (t_1 + t_2) \cdot f_{sw} \quad (1.15)$$

#### 1.4.4 Power Conversion Efficiency

Power conversion efficiency is the most important design issue, especially in the battery-operated power management module. Power conversion efficiency is defined as the ratio of the provided output power to the total power received from the input supply. It can be formulated as:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{con} + P_{sw} + P_Q + P_{others}} \quad (1.16)$$

The total power received from the input supply needs to provide the following items: the output power ( $P_{OUT}$ ), the conduction loss at the power stage ( $P_{con}$ ), the switching loss at the power stage ( $P_{sw}$ ), the quiescent current power of the control circuits ( $P_Q$ ), and the power loss caused by parasitic elements in realistic silicon fabrication ( $P_{others}$ ). Therefore, minimizing the power losses can lead to high power conversion efficiency to enhance the competitiveness of a power management module.

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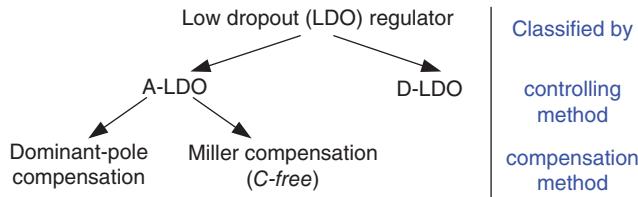
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# 2

## Design of Low Dropout (LDO) Regulators

Low dropout (LDO) regulators are widely used in portable electronic devices because they occupy small chip and printed circuit board (PCB) areas. The performance advantages of these regulators include low quiescent current and wide bandwidth (BW), which result in fast transit response. Unlike switching regulators (SWRs), LDO regulators convert voltage through a linear operation, and thus a well-regulated output voltage can be derived without the occurrence of output voltage ripples. However, LDO regulators suffer from an inherent disadvantage, namely poor power conversion efficiency (PCE) if the ratio of the output voltage to the input voltage is small, because a large voltage stress over the pass transistor causes significant power loss. When considering the small silicon area, compact PCB, and reduced discrete component costs, an LDO regulator is one candidate that can provide a conversion function for regulated and scaled-down voltages. LDO regulators are frequently utilized as post-regulators in series with SWRs to suppress voltage ripples from the switching operation of SWRs caused by their large open-loop gain. In general, the combination of an SWR in series with an LDO regulator can be viewed as a simple and efficient power management module if the ratio of the output voltage to the input voltage, as well as the open-loop gain, can remain large in the LDO regulator. An LDO regulator is regarded as a voltage buffer for decreasing voltage ripples at the cost of slightly reduced PCE.

LDO regulators have structures that are defined according to their controlling methods and compensated skills. As illustrated in Figure 2.1, LDO regulators may either be analog-low dropout (A-LDO) regulators or digital-low dropout (D-LDO) regulators. The controller of the former is designed with analog circuits, whereas that of the latter is designed with digital circuits. A-LDO regulators have two major categories, namely dominant pole compensation, which involves a large compensation capacitor  $C_{ou}$  located at the output node, and a capacitor-free ( $C$ -free) structure, which involves a dominant pole generated by Miller compensation capacitance.



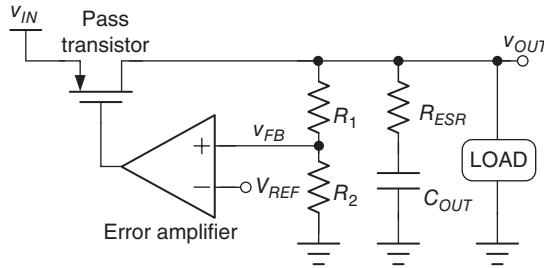
**Figure 2.1** Classification of LDO regulators

Applications determine the suitable type of LDO to use. Various multimedia and portable devices demand Soc integration. Soc typically requires a compact-size, fast-transient, low-noise supply voltage. A *C-free* structure can be made compact at the expense of a large quiescent current and transient voltage variation. An A-LDO regulator with dominant pole compensation improves the transient voltage variation and reduces the quiescent current at the cost of a large output capacitor. When considering a D-LDO regulator as the post-regulator, an improvement in transient response and regulator size leads to the feasibility of integration; however, a trade-off occurs between regulation performance and quiescent current.

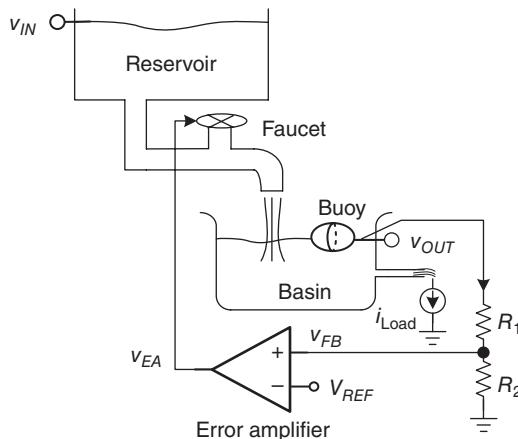
In this chapter, the basic LDO regulator is first introduced. Then, concerns over compensation for loop stability are presented to develop dominant pole compensation and *C-free* structures. Design flow and tips are also illustrated to understand the specifications and performance in A-LDO regulators. The characteristics of A-LDO and D-LDO regulators are then discussed and compared. LDO regulators with specific features are introduced to satisfy the requirements of various applications. Furthermore, low-power techniques, including novel dynamic-voltage scaling (DVS) and analog dynamic-voltage scaling (ADVS), are introduced for compatible utilization in Soc applications.

## 2.1 Basic LDO Architecture

In general, the voltage drop across power transistors in LDOs results in unavoidable heat in the power transistors. LDOs are appropriate for low-power applications because of heat dissipation. A simple LDO consists of an error amplifier (EA) and power transistors to eliminate ripples and regulate output voltage. LDO regulators have the smallest layout and footprint area, and a low quiescent current to provide small volume and high current efficiency. Figure 2.2 illustrates the architecture of a basic LDO regulator. The dropout voltage across the pass transistors is defined as the voltage difference between the input supply voltage and the output voltage. A small dropout voltage can lead to satisfactory PCE. However, decreasing the dropout voltage of an LDO may decrease the gain of the last stage, and thus deteriorate the regulation performance. A trade-off occurs between PCE and regulation performance. Designers generally use large power transistors to reduce the dropout voltage effectively and take advantage of its low on-resistance. However, large power transistors increase the silicon area, and thus the chip cost also increases. Moreover, the transient response is slowed down by the limited slew rate designed in the EA when driving at the gate of the power transistor. Given the differences between the reference voltage  $V_{REF}$  and the feedback voltage  $V_{FB}$ , the output voltage of the EA



**Figure 2.2** Structure of a basic LDO regulator



**Figure 2.3** Operation of LDOs explained using an emulated reservoir and basin system controlled by a buoy with closed-loop system

controls the gate voltage of the pass transistors, and thus modulates the current flowing through the pass transistors.

Given the negative feedback control, LDO regulators can regulate the output voltage irrespective of load current and input voltage variations if the loop gain is sufficiently large. Any switching disturbance from a pre-regulator, such as SWRs, can be effectively reduced by an effective loop gain. However, an increased loop gain may cause stability deterioration because high-frequency poles will be higher than the crossover frequency. Hence, another trade-off occurs between the regulation performance and system stability.

As illustrated in Figure 2.3, the operation of LDOs can be explained by an emulated reservoir and basin system, which is controlled by a buoy with a closed-loop system. The input voltage  $V_{IN}$  is emulated by the reservoir. The power transistor functions as a faucet, and the charge stored in an output capacitor can be regarded as the water stored in a basin. The pipe aperture of the faucet implies driving capability. The height of the water in the basin represents the level of the output voltage. The load current can be viewed as water flowing out at the bottom of a basin. To control the water level at a constant height, similar to a regulated voltage level labeled

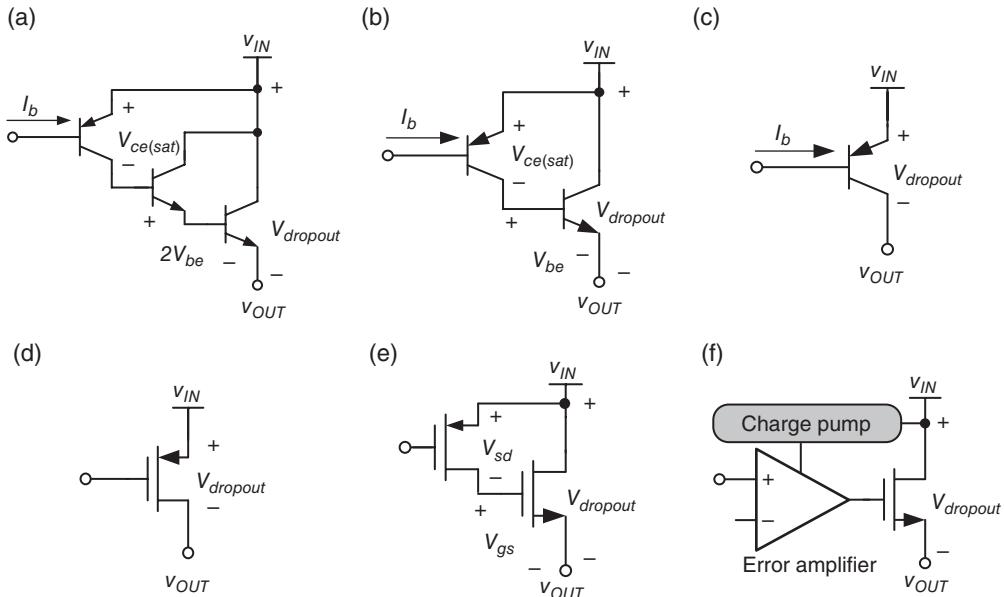
$V_{OUT}$  in LDOs, a closed-loop system should be formed using the buoy to detect the water level. The detected water level is scaled down and compared with the predefined reference voltage  $V_{REF}$  to obtain an error control signal  $V_{EA}$ . That is,  $V_{EA}$  can be used to determine how tight or loose the faucet is. Water flowing out of the faucet can correspond to the value of  $V_{EA}$ . Under a dynamic equilibrium condition, the water flowing into and out of a basin remains in dynamic balance, which is maintained by the negative feedback system. In the emulated reservoir and basin system, only the water level that is similar to the output voltage level in LDOs is monitored. Thus, the system is called a voltage-mode control system.

How fast the faucet can be turned tightly or loosely determines how fast the water level can reach the desired level in case of a sudden change in output load current. In the emulated reservoir and basin system, the water level is controlled by the negative feedback closed-loop system, wherein the water level is sensed by the buoy. A large pipe aperture of the faucet can deliver high current to the basin, but the faucet experiences driving difficulty of the EA output. Thus, turning the faucet to an adequate position requires good driving capability of the EA. Furthermore, the water level is easily maintained at a constant level by a basin with a large volume, because a sudden considerable change in loading current cannot instantly disturb the water level of a large basin even if the faucet has not been turned to an adequate position. Moreover, if the output load current changes from high to low, then the water level will remain high for a short period because of the absence of an extra path for surplus water to flow out of the basin. To reach the desired water level, an extra path where water can rapidly flow out of the basin is required, which leads to wastage of valuable water. Evidently, this approach is not energy efficient and not environmentally friendly. If cost and energy efficiency are considered, a bulky basin is not the appropriate design to keep the water level constant.

In summary, two concerns are worth mentioning. First, the driving capability of the EA depends on the faucet size, and affects the rapid delivery of the current from the reservoir to the basin. Second, the basin size determines the volume of water stored in it and influences the maintenance of the water level in case of any sudden change in output load current. These two issues can be mapped into similar LDO designs, and thus two possible large capacitances should be considered carefully in LDO design. The first large capacitance is located at the output node and the second is located at the output of the EA, which can be mapped into two capacitances at  $V_{OUT}$  and  $V_{EA}$  in Figure 2.3, respectively. The values of these capacitances determine the types of suitable LDO topology. Therefore, application requirements have to be considered first. One of the possible topologies has to be selected to satisfy all specifications. In the following sections, compensation and advanced techniques are introduced to enhance LDO performance.

### 2.1.1 Types of Pass Device

The faucet is the power transistor. Thus, the type of power transistor suitable for LDO designs should be identified. All possible pass transistor designs are shown in Figure 2.4. Considering the type of bipolar transistor (BJT) as pass transistor, NPN Darlington, NPN, and PNP shown in Figure 2.4(a)–(c), respectively, can be used to obtain the advantage of high driving capability because of the high current gain of BJTs. However, BJTs have two obvious disadvantages. First, the dropout voltage required by the voltage headroom, which consists of base/emitter and collector/emitter voltages, to keep the BJT working in the active region



**Figure 2.4** Pass devices include (a) NPN Darlington, (b) NPN, (c) PNP, (d) N-MOSFET, (e) P-MOSFET, and (f) N-MOSFET with one charge pump circuit

is large. In Figure 2.4(a)–(c), the dropout voltage is  $V_{ce(sat)} + 2V_{be}$ ,  $V_{ce(sat)} + V_{be}$ , and  $V_{ec(sat)}$ , respectively. Thus, in low-quiescent and low-power Soc applications, Darlington NPN and NPN configurations are unsuitable because of their large dropout voltage. By contrast, the PNP configuration is the most appropriate configuration because its minimum dropout voltage is only  $V_{ec(sat)}$ , which is typically 0.4 V. The second critical disadvantage is the large leakage current at the base terminal. The base current is basically proportional to the value of  $I_C/\beta_n$  or  $I_C/\beta_p$ , where  $I_C$  is the collector current and  $\beta_n, \beta_p$  are the current gains of the NPN and PNP transistors, respectively. In general,  $\beta_n$  and  $\beta_p$  are within the ranges of 50–100 and 5–10, respectively. The leakage current caused by the non-zero base current is strongly affected by current gain. If a LDO voltage is required, then the most appropriate BJT is the PNP transistor; however, this transistor suffers from a large leakage current because of its low  $\beta_p$  compared with the NPN transistor, which has a large  $\beta_n$ .

A MOSFET is selected to replace the BJT as the power transistor to eliminate these two critical and obvious disadvantages, as shown in Figure 2.4(d)–(f). In general, no DC flows into or out of the gate terminal of the MOSFET. Thus, the leakage current problem can be solved completely and low quiescence is guaranteed. However, the driving capability of a MOSFET is considerably smaller than that of a BJT, and thus a large aspect ratio of the MOSFET is required to generate a similar driving current to that provided by a BJT. An obvious disadvantage is the large silicon area occupied by the MOSFET.

In Figure 2.4(d) the p-channel MOSFET (P-MOSFET) with large aspect ratio has a lower dropout voltage than its counterpart PNP transistor, which has a minimum dropout voltage limited to approximately 0.2 V. That is, if the LDO regulator requires LDO voltage and low quiescent current, then the P-MOSFET is the best choice among the various configurations.

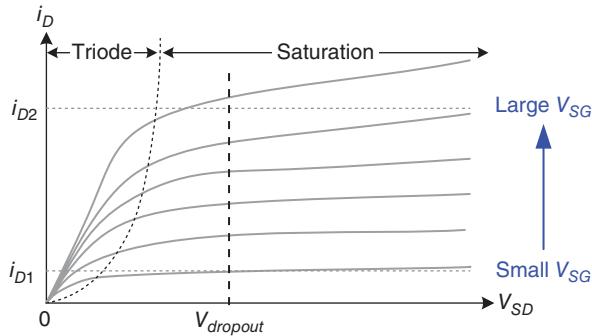
**Table 2.1** Comparison of different pass devices

|               | NPN Darlington          | NPN                    | PNP           | NMOS                   | PMOS          |
|---------------|-------------------------|------------------------|---------------|------------------------|---------------|
| $I_{Load}$    | High                    | High                   | High          | Medium                 | Medium        |
| $I_q$         | Medium                  | Medium                 | Large         | Low                    | Low           |
| $V_{dropout}$ | $V_{ce(sat)} + 2V_{be}$ | $V_{ce(sat)} + V_{be}$ | $V_{ec(sat)}$ | $V_{gs} + V_{ds(sat)}$ | $V_{sd(sat)}$ |
| Speed         | Fast                    | Fast                   | Slow          | Medium                 | Medium        |
| Compensation  | Easy                    | Easy                   | Complex       | Easy                   | Complex       |

However, the P-MOSFET also has several disadvantages. For example, it requires a larger silicon area to compensate for the lower mobility  $\mu_p$  than in the n-channel MOSFET (N-MOSFET). Moreover, the P-MOSFET works as a common source (CS) stage in an LDO regulator. The gate-to-drain capacitance  $C_{gd}$  is amplified by the Miller effect and increases the difficulty of loop compensation. By contrast, the N-MOSFET shown in Figure 2.4(e) works as a source follower (SF) stage that functions as a buffer stage in an LDO regulator. Thus, the compensation complexity of an LDO regulator with N-MOSFET is considerably lower than that of an LDO regulator with P-MOSFET. Considering the dropout voltage of an N-MOSFET, a large voltage headroom equal to  $V_{sd} + V_{gs}$  is the critical disadvantage, which is similar to that in the BJT. To address this problem in commercial products, a charge pump circuit can be used to decrease the dropout voltage, as shown in Figure 2.4(f). The boosted supply voltage for the EA can minimize the dropout voltage, but an LDO regulator suffers from switching noise caused by the charge pump circuit. A trade-off appears to occurs between noise suppression and dropout voltage. An off-chip low-pass filter is inserted between the control signal and the gate of the N-MOSFET, because an on-chip low-pass filter is difficult to apply. Consequently, the disadvantages are extra off-chip components and a large PCB area.

The products listed in Table 2.1 use P-MOSFETs as power transistors because of their low quiescence and LDO voltage at the cost of complex compensation skills. In the following section, compensation skills are introduced by assuming that a P-MOSFET is used as the power transistor. Before ending this subsection, the  $I-V$  curve of the power P-MOSFET is observed, as shown in Figure 2.5. The P-MOSFET works similarly to the faucet shown in Figure 2.3. Controlling the value of the source-to-gate voltage  $V_{SG}$ , which is similar to the tightness or looseness of the faucet, can determine the current flowing through the power P-MOSFET. At light loads (e.g.,  $i_{D1}$  in Figure 2.5), a small  $V_{SG}$  indicates less current flowing out of the input supply voltage  $V_{IN}$ . By contrast, increasing  $V_{SG}$  at heavy loads (e.g.,  $i_{D2}$ ) can loosen the faucet to force a high current to flow through the power P-MOSFET. In case of a load change from light to heavy (e.g., from  $i_{D1}$  to  $i_{D2}$ ), a large  $V_{dropout}$  can guarantee that the power P-MOSFET will work in the saturation region for high gains in CS configuration, where  $V_{dropout}$  is the source-to-drain voltage of the P-MOSFET.

A high gain in the system loop leads to a well-regulated output voltage. However, as mentioned previously, a large  $V_{dropout}$  implies poor PCE of an LDO regulator. Ensuring that the power P-MOSFET at the saturation region has a constant  $V_{dropout}$  and a large  $V_{dropout}$  is required at heavy loads, but redundant and power inefficient at light loads because of the small  $V_{SG}$ . If  $V_{dropout}$  can be adjusted according to the output load current conditions, then the PCE can be kept high over a wide load range, which is referred to as the ADVS technique. ADVS and digital-dynamic voltage scaling (DDVS) are introduced later.



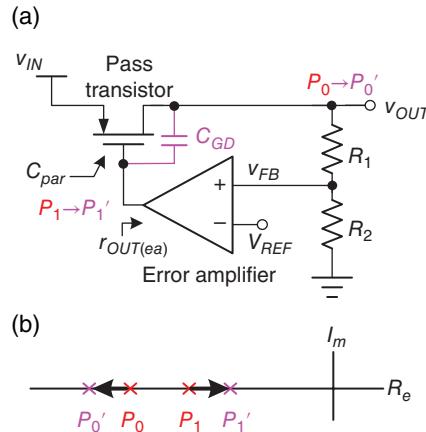
**Figure 2.5**  $I$ - $V$  curve of the power P-MOSFET

## 2.2 Compensation Skills

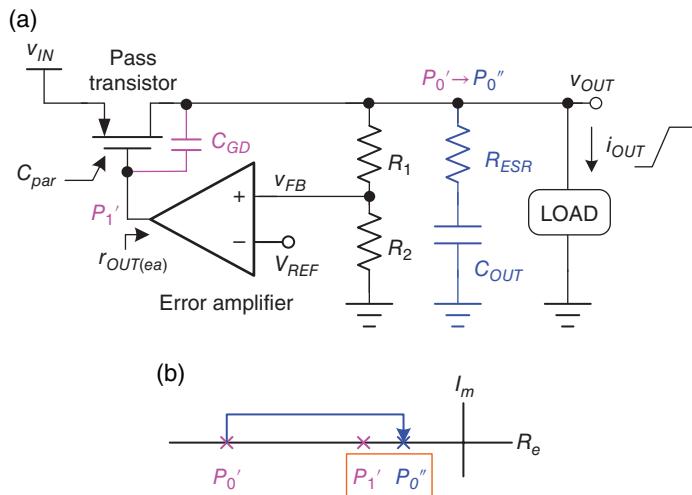
As illustrated in Figure 2.2, the regulation of an LDO regulator is structured with a negative feedback loop, and thus the output voltage can be regulated at a desired voltage level. Therefore, the frequency response should be designed carefully not only for stability, but also for transient response. In general, compensation skills should ensure that an LDO regulator has various capabilities, including low quiescent current at light loads, high current efficiency, low voltage operation, and high driving capability. Different compensation skills present various challenges that correspond to different specifications of systems and applications. In this section the characteristics of poles and zeros provide the concept of compensation skills for LDO regulators. Pole distribution is introduced first.

### 2.2.1 Pole Distribution

First, in the design of the LDO regulator shown in Figure 2.6(a), the existence of poles can be clearly identified at  $P_0$  and  $P_1$ , located at the LDO output and the first stage output, respectively. Without considering the Miller effect on the gate-to-drain capacitance and by adding output capacitors at the output node,  $P_1$  is below  $P_0$ , as shown in Figure 2.6(b), because a large parasitic capacitance  $C_{par}$  and a large output resistance  $r_{OUT(ea)}$  are observed at the gate of the power MOSFET and at the output of the EA, respectively.  $r_{OUT(ea)}$  is large because of the low quiescent current requirement. Given that the power P-MOSFET should be large to provide high driving capability, the gate-to-drain capacitance  $C_{GD}$  is sufficiently large to be a Miller capacitance with the gain contributed by the power P-MOSFET. Thus,  $P_1$  and  $P_0$  are split by the Miller capacitance  $C_{GD}$ ; that is,  $P_0$  moves toward high frequencies as a new high-frequency pole  $P'_0$  while  $P_1$  moves toward the origin as a new low-frequency pole  $P'_1$ . The root locus of the pole-splitting effect that results from a large  $C_{GD}$  is illustrated in Figure 2.6(b). Consequently, system stability can be ensured if two poles can be widely split by  $C_{GD}$ . That is, a low-frequency pole  $P'_1$  at the gate of the power MOSFET can be regarded as the system-dominant pole without being affected by other low-frequency poles because the first non-dominant pole  $P'_0$  is now located at high frequencies.



**Figure 2.6** Basic LDO regulator. (a) Schematic. (b) Root locus showing the pole-splitting effect with Miller capacitance  $C_{GD}$

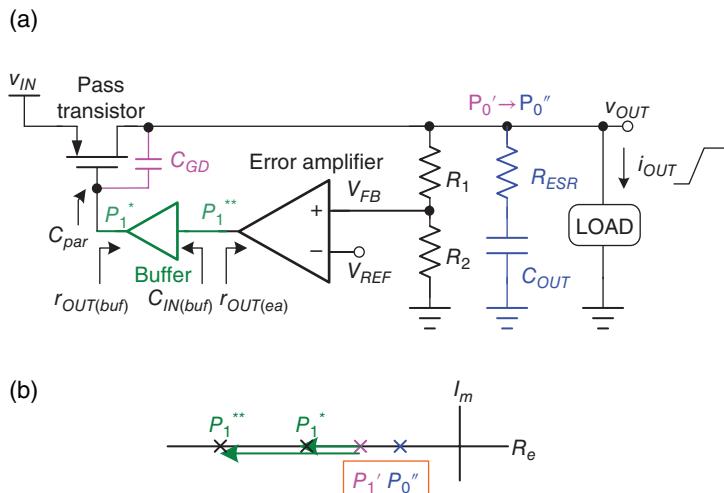


**Figure 2.7** Basic LDO regulator with a large output capacitor to deal with significant sudden loading current change. (a) Schematic. (b) Root locus

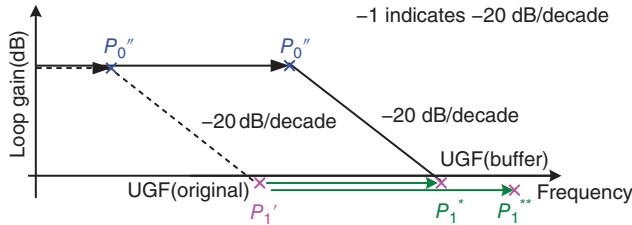
When checking the requirements of LDO regulators, experiencing the sudden load changes required for system operation is necessary. As previously mentioned, a sudden load change cannot immediately change the water level of a big basin in the emulated reservoir and basin system. Thus, connecting a large output capacitor at the output to sustain a well-regulated output voltage is easy, as shown in Figure 2.7(a). A large output capacitor solves the sudden load change problem, but the stability decreases because the large output capacitor forces the output pole toward the origin with the role of dominant pole. Meanwhile, the pole at the gate

of the power P-MOSFET is not the dominant pole anymore. The position of the output pole changes from  $P_0'$  to  $P_0''$ , where  $P_0''$  is considerably lower than  $P_1'$  because of the large output capacitor.  $P_0''$  becomes the new dominant pole of the system when a large output capacitor is used. However, we should remember the subsequent problem that two low-frequency poles, namely  $P_0''$  and  $P_1'$  (the output pole and the pole at the gate of the power P-MOSFET, respectively) exist in the LDO regulator. Consequently, the phase margin (PM) is deteriorated by two low-frequency poles, as shown in Figure 2.7(b). Given that the output pole is now the dominant pole, the previous non-dominant pole is located at the gate of the power MOSFET and should move toward high frequencies to increase the system stability. Obviously, we should determine how to push  $P_1'$  toward high frequencies or add a compensation zero to cancel its effect. If this problem is reviewed carefully, we can determine that the output resistance of EA is large because of the low quiescent current. The resistor/capacitor (RC) time, which is constant at the gate of the power P-MOSFET, is too large. Thus, the EA cannot directly drive large parasitic capacitance at the gate of the power P-MOSFET if a low quiescent current is still required.

A useful technique to alleviate large RC time constants occurring at the gate of the power P-MOSFET is to add a buffer stage between the output of the EA and the gate of the power MOSFET, as illustrated in Figure 2.8(a). Consequently, the driving capability and the PM can be simultaneously enhanced by the inserted buffer stage. The buffer stage splits a low-frequency pole  $P_1'$  into two high-frequency poles, namely  $P_1^*$  and  $P_1^{**}$ , as shown in Figure 2.8(b).  $P_1^*$  and  $P_1^{**}$  have small RC time constants, that is  $C_{par} * r_{OUT(buf)}$  and  $C_{IN(buf)} * r_{OUT(ea)}$ , respectively, where  $C_{IN(buf)}$  and  $r_{OUT(buf)}$  are the input capacitance and output resistance of the buffer stage, respectively.  $C_{IN(buf)}$  and  $r_{OUT(buf)}$  are small because of the characteristics of the voltage buffer. The large RC time constant stops increasing when the buffer stage is used.  $P_1^*$  is below  $P_1^{**}$  because of the large parasitic capacitance  $C_{par}$  at the gate of the power P-MOSFET.  $P_1^*$  becomes the first non-dominant pole after the buffer stage is inserted.



**Figure 2.8** Basic LDO regulator with a buffer stage. (a) Schematic. (b) Root locus



**Figure 2.9** Relationship between the dominant pole and non-dominant poles in the frequency domain before and after the buffer stage is inserted

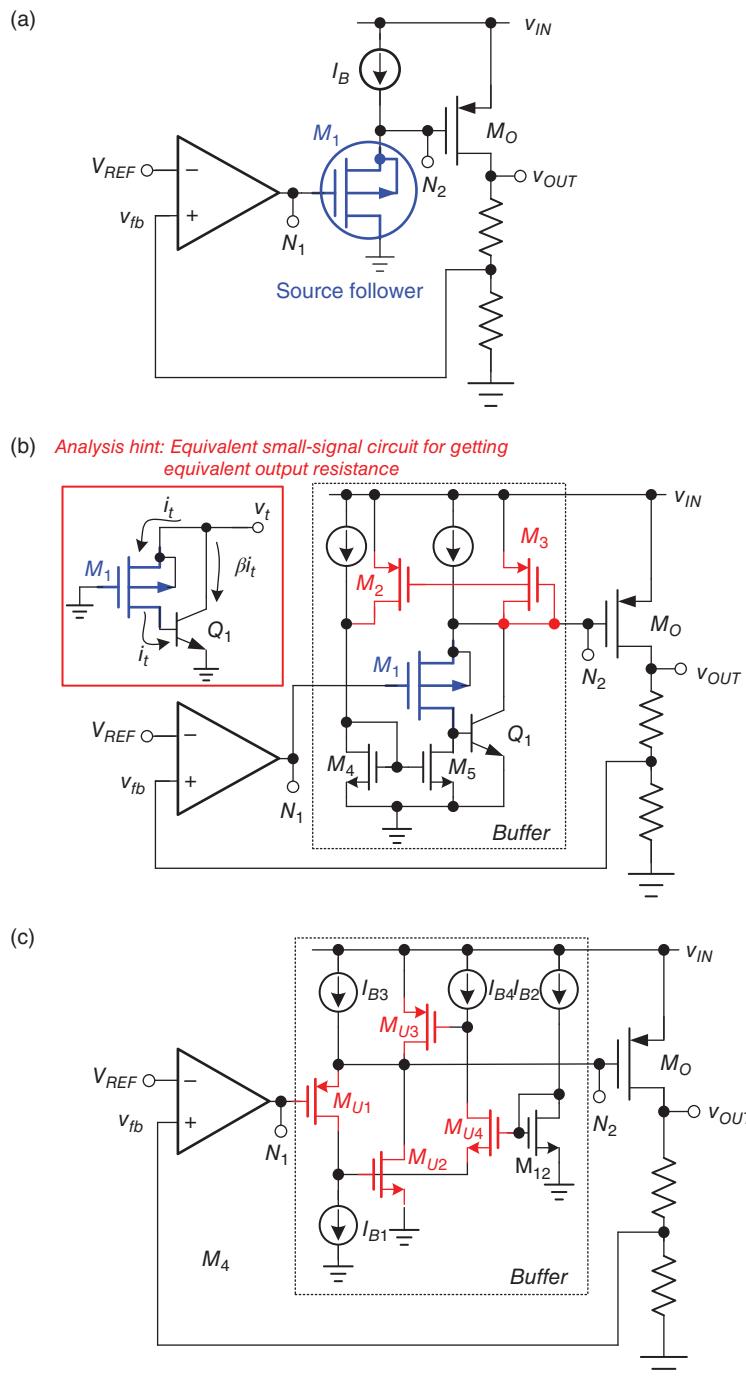
After the buffer stage is inserted, the low-frequency pole  $P_1^*$  gains a small RC time constant. If  $P_1^*$  is set at the unity gain and no low-frequency pole exists below  $P_1^*$ , excluding the output pole  $P_0''$ , a line with slope  $-20 \text{ dB/decade}$  can be drawn to determine the highest position of  $P_0''$ , as illustrated in Figure 2.9. Similarly, before the buffer stage is inserted, the original position of  $P_0''$  can be determined by drawing a line with slope  $-20 \text{ dB/decade}$  from the location of  $P_1'$ , which is also found at unity gain. Figure 2.9 shows the possible working range of  $P_0''$ . In conclusion, if  $P_0''$  is located at the highest position, then the RC time constant of  $P_0''$  can be reduced because  $P_1^*$  is above  $P_1'$ . The advantages of a smaller RC time constant of  $P_0''$  are twofold. First, the LDO regulator can tolerate a high loading current, which indicates a small equivalent output resistance. Second, the LDO regulator can remain stable if a small output capacitor is used at medium loads instead of the conventional design without using the buffer stage.

Basically, the buffer can be a simple SF, as depicted in Figure 2.10(a), with an equivalent output resistance of  $1/g_{m1}$ . However,  $1/g_{m1}$  is not sufficiently small to push the pole toward high frequencies. Thus, the design target is to reduce the equivalent output resistance. The analysis can involve a test voltage  $v_t$  applied at source  $M_1$  when the equivalent output resistance is measured, as depicted at the top left of Figure 2.10(b). The small signal current  $i_t$  ( $\approx g_{m1}v_t$ ) is redirected to the base terminal of an additional BJT  $Q_1$  to generate an amplified current  $\beta i_t$ . The advantage of this technique is that the small signal  $i_t$  is enlarged by the current gain  $\beta$  of the BJT. Given the local negative feedback, the equivalent output resistance of the buffer can be attenuated by a factor of  $(\beta + 1)$ , which can be expressed as:

$$r_{OUT(buf)} \approx \frac{1}{g_{m1}} \cdot \frac{1}{(\beta + 1)} \quad (2.1)$$

In general, only lateral PNP or NPN BJT is provided in the standard CMOS process. Thus, the designer can use a bipolar-CMOS-DMOS (BCD) process to facilitate design at the expense of cost and silicon area. To solve this issue, the function of the BJT device can be substituted by combining MOSFETs from  $M_{U1}$  to  $M_{U4}$ , as shown in Figure 2.10(c). A new equivalent output resistance is expressed in Eq. (2.2), which indicates that the output resistance is reduced by the  $(g_{m2}r_{o1} + g_{m3}g_{m4}r_{o1}r_{o4})$  contributed by the local negative feedback control of MOSFETs from  $M_{U1}$  to  $M_{U4}$  without any additional process:

$$r_{OUT(buf)} \approx \frac{1}{g_{m1}} \cdot \frac{1}{(g_{m2}r_{o1} + g_{m3}g_{m4}r_{o1}r_{o4})} \quad (2.2)$$

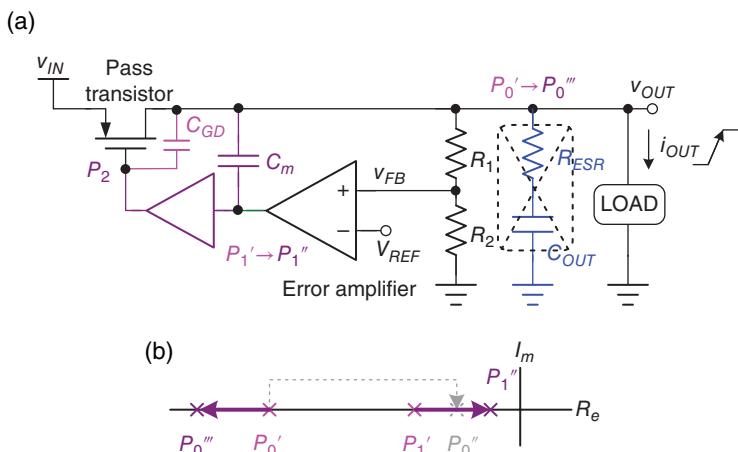


**Figure 2.10** Structure of the LDO regulator with a buffer stage, which can be implemented with (a) an SF configuration, (b) an SF with a local negative feedback implemented by BJT, and (c) an SF with a reduced output resistance implemented by CMOS devices

As previously mentioned, the size of the output capacitor can be reduced if a buffer stage is used. The output capacitor cannot be implemented on the same silicon because  $P_1^*$  in Figure 2.9 should be pushed higher than  $P_1'$ , because the acceptable size of an on-chip capacitor is within the range of several pico-farads compared with an external output capacitor that measures several micro-farads. That is, the advantage of the buffer stage is that it allows the external output capacitor to be smaller than that of the conventional LDO design without a buffer stage. Consequently, the external output capacitor remains too large to become an on-chip capacitor even if a buffer stage is used.

To obtain a compact-sized solution for the LDO regulator, the output capacitor shown in Figure 2.7 is used because the large charge stored in a large output capacitor can deal with instant load changes. If this large output capacitor is removed, then the power transistor should be rapidly turned on or off because the small charge stored in the parasitic output capacitance cannot satisfy the load change requirements of the system. If the system bandwidth is sufficiently large, the LDO regulator has the capability to handle a sudden load change even when the large output capacitor is removed. The Miller compensation skill, which is completely contrary to the dominant-pole compensation skill, can be applied to LDO regulators without adding any large external output capacitor. The Miller compensation skill can have a large bandwidth if a gain-stage amplifier is inserted between the EA and the power transistor. Thus, a high bandwidth is achieved but Miller capacitors are necessary. The inherent gate-to-drain capacitance  $C_{GD}$  can be regarded as a Miller capacitor. Only one Miller capacitor  $C_m$  is necessary, as shown in Figure 2.11(a). The characteristics and features of the two aforementioned compensation skills should be examined to identify which skill is more suitable for Soc applications.

Figure 2.11(a) shows that a Miller capacitor  $C_m$  is added and a large output capacitor  $C_{OUT}$  is removed. Consequently, Figure 2.11(b) shows that the pole at  $V_{OUT}$  moves toward high frequencies from  $P_0'$  to  $P_0'''$ , while the pole at the output of the EA moves toward low frequencies from  $P_1'$  to  $P_1''$ .  $P_1''$  replaces  $P_0'$  in the dominant-pole compensation skill as the new dominant pole because of the Miller effect. The advantage of this process is that the Miller capacitor  $C_m$  is considerably smaller than the original  $C_{OUT}$ , because the Miller effect amplifies the equivalent capacitance. Moreover, another Miller capacitance  $C_{GD}$  can split  $P_2$  and  $P_0'''$  into high



**Figure 2.11** Basic LDO regulator with Miller compensation. (a) Schematic. (b) Root locus

frequencies. However, without a large  $C_{OUT}$ , any load transient response will cause a larger output transient voltage variation than the dominant-pole compensation skill if two compensation skills are assumed to have the same unity gain frequency (UGF), because the small basin cannot accommodate large water system requirements if the bandwidth does not increase.

When the load changes from heavy to light, the equivalent output impedance decreases, and then  $P_0'''$ , which is the pole at  $V_{OUT}$ , moves toward a lower frequency. To maintain the performance of the transient response, extending the UGF is a challenge, particularly under ultra-light load conditions.

### 2.2.2 Zero Distribution and Right-Half-Plane (RHP) Zero

LDO regulators experience a load change from Soc applications. Thus, the bandwidth of LDO regulators should be sufficiently high to have a good transient load response. To extend the bandwidth further, a left-half-plane (LHP) zero is required to cancel the effect of the first non-dominant pole. We provide several common techniques to generate LHP zero, without being affected by right-half-plane (RHP) zero. The first well-known technique, as shown in Figure 2.12(a), is to use an equivalent series resistance at the output capacitor to form an LHP zero according to the equivalent output impedance:

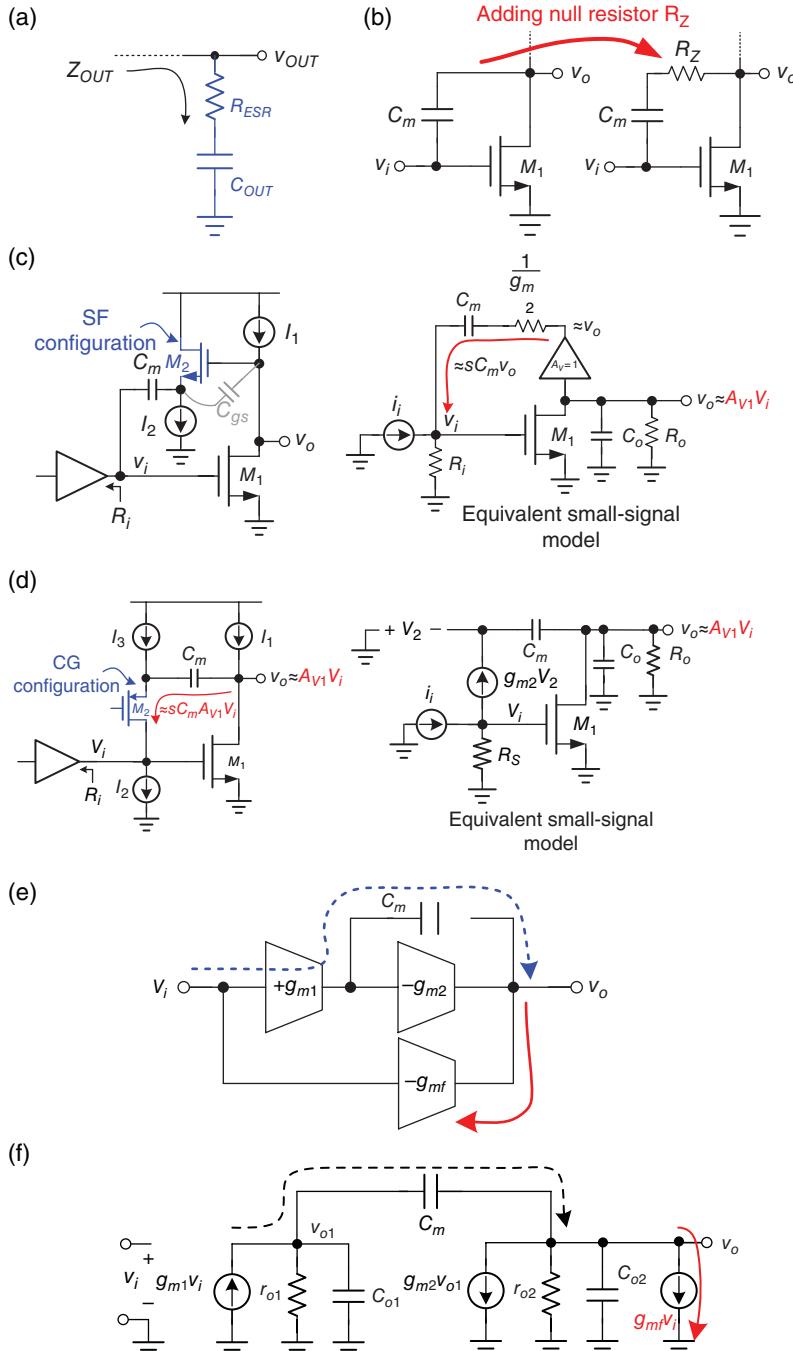
$$Z_{OUT} = R_{ESR} + \frac{1}{sC_{OUT}} = \frac{1 + sR_{ESR}C_{OUT}}{sC_{OUT}} \quad (2.3)$$

The ESR value is temperature dependent, and thus determining an exact value in the design is difficult. Moreover, in case of a loading current change, any current flowing through the ESR will cause a large IR-drop voltage. The transient voltage variation becomes large, which is not desired in power management design. Thus, low ESR output capacitors are favored in converter designs.

In general, in a CS configuration, the Miller capacitor  $C_m$  will contribute an RHP zero, which is not desired in regulator designs. RHP zero is caused by a feedforward path through  $C_m$  from  $v_i$  to  $v_o$ . RHP zero significantly deteriorates the system stability, because it contributes +20 dB and  $-90^\circ$  per decade. Thus, removing the RHP zero effect is necessary. As shown in Figure 2.12(b), the second technique is to convert RHP zero into LHP zero through the null resistance  $R_Z$  in series with  $C_m$ . If  $1/g_{m1}$  is considerably smaller than  $R_Z$ , then the expression of LHP zero ( $\omega_Z$ ) is shown as:

$$\omega_Z \approx \frac{1}{C_m(g_{m1}^{-1} - R_Z)} \quad (2.4)$$

where  $g_{m1}$  is the transconductance of MOSFET  $M_1$ . Furthermore, given that the implementation of  $R_Z$  occupies a large silicon area, conventional MOSFET resistance working in the triode region can be used. However, its equivalent resistance value suffers from perturbations resulting from output voltage variation. Figure 2.12(c) shows an effective technique to remove RHP zero by adding a SF in series with a Miller capacitor  $C_m$  on the feedback path from  $v_o$  to  $v_i$ , which indicates that the voltage difference across  $C_m$  remains at  $v_i - v_o$ . However, the input capacitance observed at  $v_i$  is the series equivalent capacitance generated by  $C_m$  and  $C_{gs2}$ . Consequently, the equivalent capacitance becomes smaller than that of the original design. That



**Figure 2.12** LHP zero generation methods. (a) ESR on the output capacitor. (b) Miller capacitor with a null resistor  $R_Z$ . (c) SF configuration used to remove RHP zero. (d) CG configuration used to remove RHP zero. (e) Feedforward path forms parallel architecture to obtain one LHP zero. (f) Small signal model of (e) showing the effect of the feedforward path

is, RHP zero moves toward infinity, and thus an LHP zero is generated. After calculation, the transfer function is derived as:

$$\frac{v_o}{i_i} = \frac{-g_{m1}R_oR_i(1 + C_m/g_{m2}s)}{R_oC_oC_m(1/g_{m2} + R_i)s^2 + [(1/g_{m2} + g_{m1}R_oR_i)C_C + R_oC_o]s + 1} \quad (2.5)$$

The generated LHP zero is expressed in Eq. (2.6), which is determined by controlling the transconductance value of  $M_2$ :

$$\omega_Z = -\frac{g_{m2}}{C_m} \quad (2.6)$$

The RHP zero disappears in the circuit, but a disadvantage must be pointed out in this case. The maximum allowable output voltage must be higher than  $V_{OD(\text{current source } I_2)} + V_{GS2}$ , which indicates that the output voltage cannot be too low. Thus, another technique can be used to improve the solution to this problem. The circuit configuration is shown in Figure 2.12(d), where transistor  $M_2$  works as a common gate (CG) configuration. The output voltage signal is converted into a current signal  $sC_m v_o$ , which is injected into the  $v_i$  node and summed with the input current  $i_i$ . The transfer function from  $i_i$  to  $v_o$  is expressed in Eq. (2.7) with one generated LHP zero, as shown in Eq. (2.8):

$$\frac{V_o}{i_i} = \frac{-g_{m1}R_iR_o \left(1 + \frac{C_m}{g_{m2}}s\right)}{R_o/g_{m2}C_oC_ms^2 + \left[(1 + g_{m1}R_i)R_oC_m + \frac{C_m}{g_{m2}} + R_oC_o\right]s + 1} \quad (2.7)$$

$$\omega_Z = -\frac{g_{m2}}{C_m} \quad (2.8)$$

Moreover, the feedforward path can generate an LHP zero via an active signal path, because it can alleviate the effect of RHP zero through  $C_m$ . Figure 2.12(e) shows a two-stage amplifier with the Miller compensation capacitor  $C_m$ . The feedforward amplifier with transconductance  $g_{mf}$  can provide a feedforward signal path that is used to move RHP zero toward infinity, thus transforming it into LHP. That is, if  $g_{mf}$  is equal to  $g_{m1}$ , then no net current signal out of the output exists, and thus the output voltage is zero when  $\omega$  approaches infinity, as shown in Figure 2.12(f). After the transfer function is derived, setting  $g_{mf} = g_{m1}$  can move zero to LHP and equal to  $-g_{m2}/C_{o1}$ , which is above the UGF, where  $C_{o1}$  is the output capacitance of the first stage. RHP zero is effectively removed from the system, even if LHP zero is not well defined in this case.

An explanation of LHP and RHP zeros helps in the following LDO designs. Before providing the detailed designs, the specifications and design considerations of the LDO regulator are carefully addressed in the following section.

## 2.3 Design Consideration for LDO Regulators

Several specifications should be mentioned in LDO designs. Such specifications can be classified into two categories, namely steady-state and dynamic characteristics. Steady-state specifications include dropout voltage  $V_{dropout}$ , line regulation, load regulation, temperature

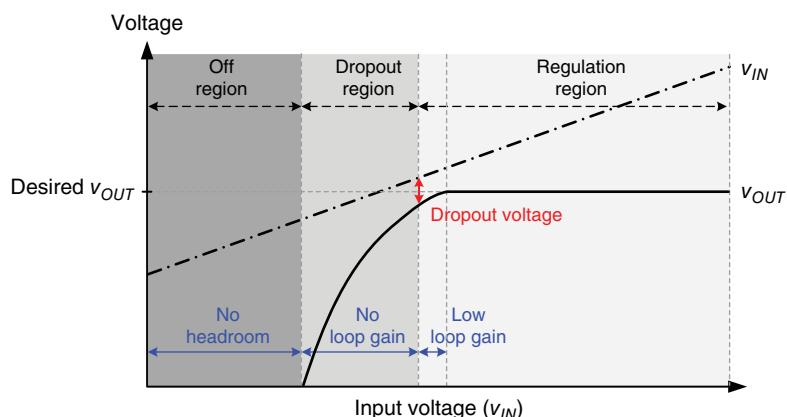
coefficient (TC), and maximum/minimum load current, among others. Meanwhile, dynamic specifications include line/load transient voltage variations, transient recovery time, pole/zero doublets, PM, and adaptive quiescent operating current, among others. The following subsections explain each specification in the LDO designs.

### 2.3.1 Dropout Voltage

As shown in Figure 2.13, when a certain desired  $V_{OUT}$  is assumed under certain loading conditions, different  $V_{IN}$  refer to various operating regions, including the off region, dropout region, and regulation region. Different operating regions lead to varying  $V_{OUT}$  performances. In the regulation region,  $V_{OUT}$  can be regulated within the allowable dropout voltage  $V_{dropout}$ . This voltage can be estimated by the voltage difference between the input voltage and the output voltage when  $V_{OUT}$  deviates from its nominal regulated voltage of approximately 2%. That is, the voltage across the power transistor that is defined as  $V_{dropout}$ . When  $V_{dropout}$  increases with decreasing  $V_{IN}$ , the power transistor eventually loses its gain and  $V_{OUT}$  gradually deviates from its desired value. As soon as the power transistor turns to function as a switch instead of an analogy gain stage, the system loop gain drastically decreases and consequently, the LDO regulator loses its capability to regulate  $V_{OUT}$ . The  $V_{OUT}$  value is determined according to  $V_{IN}$ ,  $I_{Load}$ , and  $R_{on}$ , where  $R_{on}$  is the equivalent resistance of the power transistor. Under this situation, the operation enters the dropout region. The voltage across the power transistor can basically be expressed as:

$$V_{dropout} = I_o R_{on} \quad (2.9)$$

As  $V_{IN}$  decreases further,  $R_{on}$  increases continuously because the input voltage that drives the power transistor is too low. Under this situation,  $V_{OUT}$  is decreased to the ground and the operation enters the off region.



**Figure 2.13** Characteristic curve of input voltage and output voltage that defines the dropout voltage  $V_{dropout}$

Operation in the regulation region is necessary for LDO regulators to provide regulated performance and driving capability. When a small  $V_{dropout}$  and a large  $I_{Load}$  are desired, LDO regulators should be out of the regulation region. The feedback controller can adjust the  $R_{on}$  that corresponds to  $V_{dropout}$  to regulate  $V_{OUT}$  when operation occurs in the regulation region. The minimum  $V_{dropout}$  is the worst-case scenario in the regulation region, when LDO regulators consider the largest  $I_{Load}$  and the minimum  $R_{on}$ . To ensure that LDO regulators are operating within the regulation region, increasing the size of the power transistors can reduce  $R_{on}$  and then ease the limitation of  $V_{dropout}$ . However, this process increases the complexity of the compensation network.

LDO regulators are typically utilized for two purposes. The first purpose is to function as the voltage converter to provide step-down supply voltage. In this case, the requirements are simple architecture, small silicon area, and low cost with minimal requirement for passive components such as inductors and capacitors. However, a large  $V_{dropout}$  is inevitable because LDO regulators are used for step-down voltage conversion. The PCE of LDO regulators is sacrificed because of the considerable power loss across power transistors compared with SWRs.

The second purpose of LDO regulators is to work as post-regulators to provide a noise-suppression function for low-noise voltage in sensitive analog circuits.  $V_{dropout}$  is expected to be minimal to prevent power loss. In modern LDO regulator designs, the trade-off between efficiency and the silicon area occupied by power transistors is considered; thus,  $V_{dropout}$  is designed within the range of 200 mV.

### 2.3.2 Efficiency

PCE is defined as the ratio of the output power  $P_{OUT}$  to the input power  $P_{IN}$ , as expressed in Eq. (2.10). The output power  $P_{OUT}$  is equal to the product of the output voltage and the output loading current. The input power is equal to the product of the input voltage and the input current  $I_{IN}$ :

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}I_{Load}}{V_{IN}I_{IN}} \quad (2.10)$$

In Eq. (2.11),  $I_{IN}$  includes the loading current  $I_{Load}$  and the quiescent current  $I_q$  that consists of all the biasing currents in the EA, the bandgap reference, feedback resistance network, and so on:

$$I_{IN} = I_{Load} + I_q \quad (2.11)$$

Overall, the PCE in Eq. (2.10) can be modified to Eq. (2.12), which is a product of voltage conversion efficiency and current efficiency as respectively defined in Eqs. (2.13) and (2.14):

$$\eta = \frac{I_{Load}V_{OUT}}{(I_{Load} + I_q)V_{IN}} = \eta_V \cdot \eta_I \quad (2.12)$$

where

$$\eta_V = \frac{V_{OUT}}{V_{IN}} \times 100\% \quad (2.13)$$

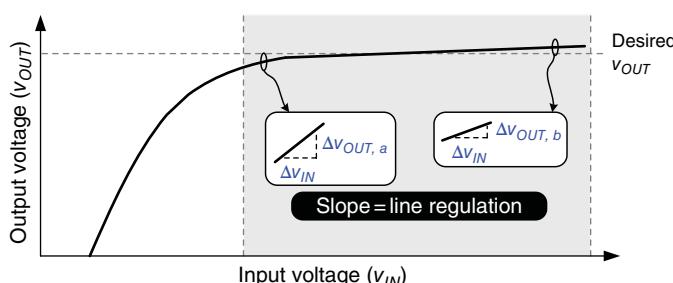
and

$$\eta_I = \frac{I_{Load}}{I_{Load} + I_q} \times 100\% \quad (2.14)$$

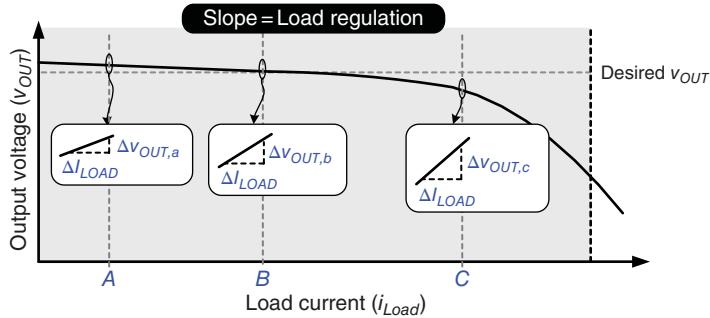
Under heavy loads, the PCE in Eq. (2.12) is approximately equal to the ratio of  $V_{OUT}$  to  $V_{IN}$ , because  $I_{Load}$  is considerably larger than  $I_q$ . This finding indicates that the dropout voltage  $V_{dropout}$  limits the efficiency performance. Meanwhile, the current efficiency  $\eta_I$  cannot be ignored in expressing the overall PCE under light loads. The standby and light-load modes occupy most of the time in portable devices. That is, a high  $\eta_I$  becomes an important factor in determining battery usage time. Thus, to obtain high current efficiency, the quiescent current  $I_q$  should be adaptive to the variation in loading current  $I_{Load}$  to obtain a high  $\eta_I$  over a wide load range. Under light loads, a low quiescent current requirement is typically set to maintain a high  $\eta_I$ . Having a low  $I_q$  if the system loading current is low in standby mode has become a challenge. Under heavy loads, however, a high  $\eta_I$  can still be maintained if  $I_q$  is increased to correspond to the loading current. Even if  $I_q$  can be adjusted adaptively by the loading current, maintaining the performance of the LDO regulator remains a challenge because of the limited bandwidth and slew rate of the operational amplifier (OPA). The required performance of LDO designs is first reviewed. Then, possible techniques to satisfy the specifications are discussed later in this book.

### 2.3.3 Line/Load Regulation

Line and load regulations are two important steady-state performances of LDO regulators because they indicate the percentage of output voltage variation in case a perturbation occurs from the input voltage and the output loading current, respectively. Line regulation is defined as the output voltage variation caused by an input line voltage variation, as shown in Figure 2.14. Line regulation can be expressed as Eq. (2.15), where  $L_o$  is the loop gain of the LDO regulator;  $g_m$  and  $r_o$  are the transconductance and the output resistance of the power MOSFET, respectively;  $\beta$  is the feedback factor. To obtain good line regulation, a high loop gain is required but



**Figure 2.14** Definition of line regulation



**Figure 2.15** Definition of load regulation

stability may deteriorate. Thus, a trade-off occurs between regulation performance/accuracy and stability:

$$\text{Line regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{g_m r_o}{L_o} + \frac{1}{\beta} \cdot \left( \frac{\Delta V_{REF}}{\Delta V_{IN}} \right) \quad (2.15)$$

When  $V_{IN}$  decreases, the dropout voltage also decreases. In Figure 2.14, the line regulation is drastically degraded when  $V_{IN}$  is reduced to a certain level. Given the constraint of dropout voltage, the loop gain of the LDO regulator is degraded because of the reduced  $V_{IN}$ . That is,  $\Delta V_{OUT,a} > \Delta V_{OUT,b}$ , assuming that the input variation  $\Delta V_{IN}$  is the same as that in Figure 2.14.

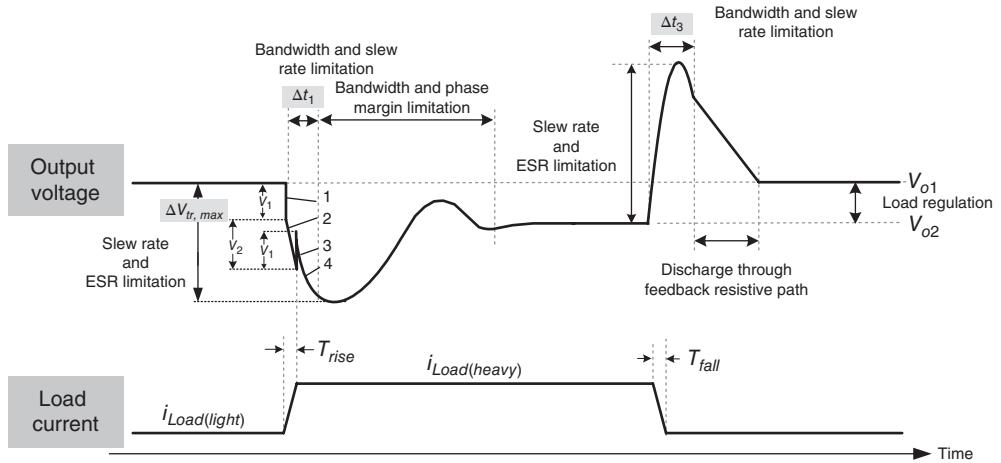
The load regulation is defined by the output voltage variation in case of a change in loading current, as shown in Figure 2.15. To obtain good load regulation, a high loop gain is required, but the stability worsens and the compensation becomes complex. The expression of load regulation is given in Eq. (2.16), where  $L_o$  is the loop gain of the LDO regulator and  $r_o$  is the output resistance of the power MOSFET:

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = - \frac{r_o}{1 + L_o} \quad (2.16)$$

If a P-MOSFET is selected as the power transistor, then the loop gain of the LDO regulator depends strongly on the load conditions. A heavy load condition typically reduces gain, and thus the load regulation is degraded gradually as shown in Figure 2.15. When the load current change ( $\Delta I_{Load}$ ) is the same, the change in output voltage is large under heavy load conditions. That is,  $\Delta V_{OUT,c} > \Delta V_{OUT,b} > \Delta V_{OUT,a}$  (Figure 2.15), because the loading current at point C is significantly higher than that at point A.

### 2.3.4 Transient Output Voltage Variation Caused by Sudden Load Current Change

The transient response can be used to test the dynamic performance of LDO regulators. This response can be categorized into two types. The first type, called load transient response, is caused by load current variation. The second type, called line transient response, is caused by line voltage variation.



**Figure 2.16** Load transient response in case of a load current change

As shown in Figure 2.16, when the LDO regulator experiences a load current step change, the output voltage requires time to be regulated by the negative feedback control. During a light-to-heavy load current change, the transient voltage variation can be divided into four parts. The first segment of the output voltage variation is contributed by the equivalent series inductance (ESL) in the output capacitor, because the voltage variation is equal to  $V_1 = ESL^*di/dt$ , which can also be expressed as  $V_1 = ESL^*(I_{Load(heavy)} - I_{Load(light)})/T_{rise}$ . Similarly, the ESR in the output capacitor also expresses the voltage drop  $V_2$  as segment 2. When the load current is set to  $I_{Load(heavy)}$ , the ESL expresses the upward effect as segment 3. Finally, the output voltage experiences a transient response that is determined by the dynamic behavior of the converter and by the applied control method in segment 4. The ESR can sometimes be regarded as the current sensor to let the output ripple as the pulse width modulation (PWM) ramp in ripple-based control. The utilization of ESR as current sensor will be explained in detail in the following sections.

In case of a load current change, the pass device cannot immediately supply sufficient load current because this device works similarly to a faucet and requires time to be turned on to obtain a large current. Therefore, the output voltage experiences a voltage drop. The drop period  $\Delta t_1$  depends on the closed-loop bandwidth  $BW_{cl}$  and the slew rate at the power MOSFET gate terminal. The response time can be approximated using Eq. (2.17), where  $C_{par}$  is the parasitic capacitance at the power MOSFET gate terminal and  $I_{sr}$  is the biasing current of the EA:

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par} \frac{\Delta V}{I_{sr}} \quad (2.17)$$

Here,  $BW_{cl}$  is the bandwidth at light loads.

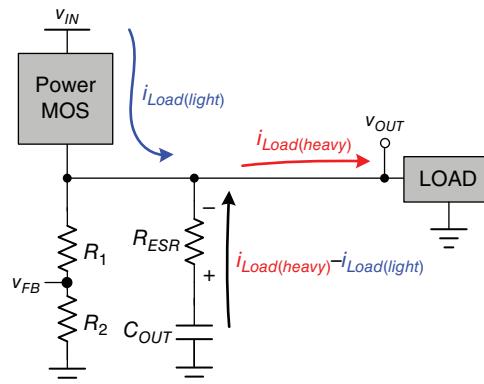
Similarly,  $\Delta t_3$  can be expressed as in Eq. (2.18). However, the values of  $\Delta t_1$  and  $\Delta t_3$  are different, because the bandwidths under light and heavy load conditions vary:

$$\Delta t_3 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par} \frac{\Delta V}{I_{sr}} \quad (2.18)$$

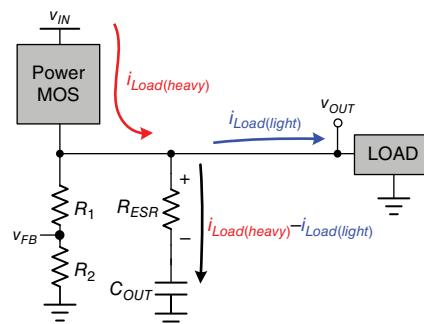
where  $BW_{cl}$  is the bandwidth at heavy loads.

In this case, we can derive the maximum transient voltage variation  $\Delta V_{tr,max}$  during transient response. To simplify the expression, the ESL effect is first ignored. Thus, in case of light-to-heavy and heavy-to-light load changes, as shown in Figures 2.17 and 2.18, respectively, the power MOSFET delivers current that is either too low or too high, respectively, to the output load. Considering the energy difference between the input voltage source and the output loading, the output capacitor works as the buffer to keep the output voltage well regulated before a dynamic equilibrium is established. That is, the output capacitor can deliver energy to the output first before the gate-to-source voltage power MOSFET is adjusted to an adequate voltage (Figure 2.17). By contrast, additional energy is injected into the output capacitor before the power MOSFET is turned off to a suitable operating position (Figure 2.18). That is, the maximum transient output voltage variation  $\Delta V_{tr,max}$  can be derived using Eq. (2.19) to represent the undershoot/overshoot voltage:

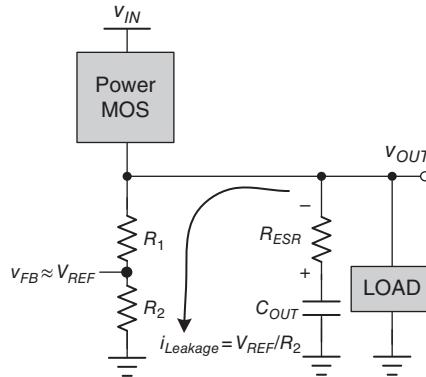
$$\Delta V_{tr,max} = \frac{I_{Load(heavy)} - I_{Load(light)}}{C_{OUT}} \cdot \Delta t_1 \text{ (or } \Delta t_3\text{)} + \Delta V_{ESR} \quad (2.19)$$



**Figure 2.17** Output voltage drops in case of a light-to-heavy load change



**Figure 2.18** Output voltage overshoots in case of a heavy-to-light load change



**Figure 2.19** Output overshoot voltage is dissipated by the feedback divider resistors

The first term in Eq. (2.19) indicates that the output capacitor  $C_{OUT}$  functions as the buffer before the power MOSFET can work properly after the period  $\Delta t_1$  or  $\Delta t_3$ , which is the time during which the power MOSFET starts to react to a light-to-heavy or a heavy-to-light load change, respectively. Simultaneously, current flows into or out of the output capacitor. The IR-drop voltage caused by the ESR can be represented by the second term in Eq. (2.19). Under both light-to-heavy and heavy-to-light load changes, the IR-drop voltage caused by the ESR will result in significant output transient voltage variation. Thus, ESR is undesirable in LDO regulators. In currently available commercial products, capacitors with low ESR are selected. For example, a multi-layer ceramic capacitor (MLCC) is frequently used in LDO regulators to ensure low output voltage ripples.

The overshoot voltage shown on the right of Figure 2.16 can be dissipated by the leakage current at the feedback divider resistors, as shown in Figure 2.19. Thus, the decreasing slope of the output voltage depends on the value of the divider resistors. However, a large overshoot voltage may damage the next Soc stage, which is implemented in an advanced nanometer process with low voltage characteristics. Thus, in conventional LDO regulators, a dummy resistive load can be connected to the output to dissipate additional energy. However, this process is applied at the cost of efficiency.

The other dynamic performance is line transient response. When the input voltage steps down to a smaller value, the power MOSFET will deliver a reduced load current, and thus cause a voltage dip. This response is similar to the load transient response in case of a light-to-heavy load current change. By contrast, when the input voltage steps up to a larger value, the power MOSFET will deliver a higher load current than the required output load, and thus produce an overshoot voltage. This response is similar to the load transient response in case of a heavy-to-light load current change.

Based on the preceding discussion, a conclusion can be drawn on which general methods can be used to improve the dynamic transient response. These methods include applying a wide bandwidth for a closed loop, implementing a fast slew rate at the power MOSFET gate terminal, using a large output capacitor, and reducing the ESR. These methods are similar to those presented in the discussion of the emulated reservoir and basin system. A large output capacitor can sustain the voltage variation in terms of temperature, but limits the bandwidth. With a large output capacitor, the compensation becomes too complex to be able to extend the bandwidth.

By contrast, when a large output capacitor is discarded, a wider bandwidth is required and the complexity increases. Moreover, a fast slew rate is required to compensate for the degraded transient response caused by the absence of a large output capacitor. This condition is the reason why the quiescent current is typically higher when a *C-free* structure is applied compared with when dominated pole compensation is implemented. In conclusion, a trade-off between performance and cost occurs in these methods.

## 2.4 Analog-LDO Regulators

As discussed in Sections 2.2 and 2.3, the design strategy in A-LDO regulators can be classified into two basic categories according to compensation skill. That is, the location of the dominant pole is first determined. In the first category, the dominant pole is located at the output because a large output capacitor is used. In the second category, called a *C-free* or capacitor-less LDO regulator, the dominant pole is generated by the Miller capacitance without using a large output capacitor.

Conventional LDO regulators use a large output capacitor with several microfarads to set the dominant pole at the output node. Considering that a large physical capacitor is used, the compensation method is called the dominant-pole compensation skill. An obvious disadvantage of this method is the use of a large off-chip capacitor, which increases the PCB area.

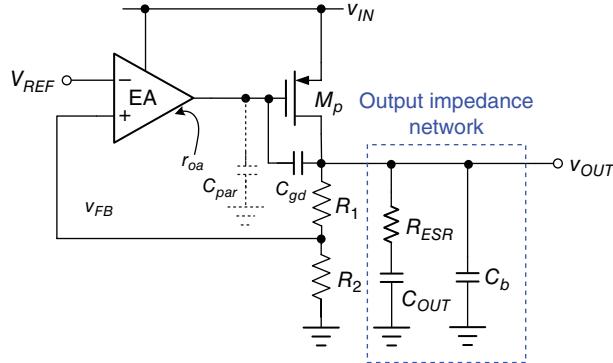
By contrast, the dominant pole can be generated by an amplified capacitance through the Miller effect. Using a large physical off-chip capacitor to form the dominant pole is unnecessary. The *C-free* LDO regulator got its name from the removal of the large off-chip capacitor, which was replaced with a small on-chip Miller capacitor to form the dominant pole and increase the system stability. When considering highly integrated LDO regulators for Soc applications, the *C-free* LDO regulator exhibits the advantages of reducing the effects of bonding wires and decreasing the silicon area occupied by the input/output (I/O) pads to connect off-chip passive components.

According to the following subsections, the specifications of LDO regulators for portable electronics should include three basic requirements: low quiescent current, wide input range operation, and improved regulation performance. Based on these requirements, we examine the advantages and disadvantages of the two categories of LDO regulators to identify the differences between these designs. The LDO regulators with the dominant-pole compensation skill are examined first.

### 2.4.1 Characteristics of Dominant-Pole Compensation

Figure 2.20 shows the LDO regulator with the dominant-pole compensation skill. In general, the dominant-pole compensation skill is utilized when the equivalent output capacitance of the next stage circuit is undetermined. Inserting a large output capacitor  $C_{OUT}$  can ensure that the dominant pole is located at the output node even if the input capacitance of the next stage circuit is unknown. Moreover, it can deal with the large load step occurring at the next stage circuit.

A basic LDO regulator includes an EA, feedback divider resistors  $R_1$  and  $R_2$ , and a power P-MOSFET. In this regulator, a large gate-to-drain capacitance  $C_{gd}$  can be expected across the gate and drain terminals of the P-MOSFET. That is, the total parasitic capacitance  $C_{par}$  at the gate of the P-MOSFET is determined by the Miller capacitance  $C_{gd}^*(1 + A_{v(MP)})$ , where  $A_{v(MP)}$  is the voltage gain of the P-MOSFET in the CS configuration. Moreover, the output resistance



**Figure 2.20** Conventional LDO regulator

$r_{oa}$  of the EA is large because of its low quiescent current in portable electronics. The pole at the gate of the P-MOSFET, which is called the first non-dominant pole  $P_{1st\_non}$ , will be at low frequencies and expressed through the following equation:

$$P_{1st\_non} = \frac{1}{r_{oa} C_{par}} \quad (2.20)$$

The dominant-pole compensation skill connects a suitable output impedance network to the output node. The constitution of the output impedance network includes two capacitors: the large output capacitor  $C_{OUT}$  and the bypass capacitor  $C_b$ , which has a smaller value than  $C_{OUT}$ .  $C_b$  can generate a pole at high frequencies to promote decade loop gain and reduce high-frequency noise. Moreover, the ESR resistance  $R_{ESR}$  of  $C_{OUT}$  should be considered in stability analysis, whereas the ESR resistance of  $C_b$  can be disregarded because  $C_{OUT}$  is larger than  $C_b$ .

In this case, all poles and zeros are examined if the output impedance network is used. The equivalent output impedance  $Z_{OUT}$  can be expressed as in Eq. (2.21), where  $r_{out}$  is the equivalent output resistance:

$$\begin{aligned} Z_{OUT} &= r_{out} \parallel (R_1 + R_2) \parallel \frac{(1 + sR_{ESR}C_{OUT})}{sC_{OUT}} \parallel \frac{1}{sC_b} \\ &= \frac{(r_{op} \parallel (R_1 + R_2)) \cdot (1 + sR_{ESR}C_{OUT})}{s^2(r_{op} \parallel (R_1 + R_2))R_{ESR}C_{OUT}C_b + s[(r_{op} \parallel (R_1 + R_2)) + R_{ESR}]C_{OUT} + s[r_{op} \parallel (R_1 + R_2)]C_b + 1} \end{aligned} \quad (2.21)$$

The denominator in Eq. (2.21) is a second-order polynomial that indicates the two poles contributed by  $C_{OUT}$  and  $C_b$ , as expressed in Eqs. (2.22) and (2.23), respectively:

$$P_0 = \frac{1}{r_{out}C_{OUT}}, \text{ if } (R_1 + R_2) \gg r_{op} \gg R_{ESR} \quad (2.22)$$

$$P_{2ndskip-1pt\_non} = \frac{1}{R_{ESR}C_b} \quad (2.23)$$

Meanwhile, the numerator in Eq. (2.12) is a first-order polynomial. A zero, which is contributed by  $R_{ESR}$ , is located at low frequencies:

$$Z_{ESR} = \frac{1}{R_{ESR}C_{OUT}} \quad (2.24)$$

In this case, the relationship of three poles and one zero is illustrated in Figure 2.21(a). Two low-frequency poles are located below the UGF. Thus, ESR zero can alleviate the effect of the first non-dominant pole  $P_{1st\_non}$  while ensuring that the second non-dominant pole  $P_{2nd\_non}$  is above the UGF to satisfy the stability requirement. That is, the stability requirement sets an ESR stable region in the design of LDO regulators. If ESR zero is found at an extremely low frequency, a high gain will cause  $P_{2nd\_non}$  to be located below the UGF, which reduces the system stability. By contrast, if ESR zero is located at high frequencies, then the effect of  $P_{2nd\_non}$  will not be alleviated before the UGF, and thus the PM is insufficient. As shown in Figure 2.21(b), the curve of load current versus ESR value shows the ESR stable region set by the stability requirement.

Furthermore, different load currents will change the shape of the frequency response, as shown in Figure 2.21(c). According to Eq. (2.25), the dominant pole  $P_0$  will move toward high frequencies if the load current increases.  $P_0$  is regarded as a load-dependent pole:

$$P_0 = \frac{1}{r_{out}C_{OUT}} \propto I_{Load}, \text{ where } r_{out} \propto \frac{1}{I_{Load}} \quad (2.25)$$

Similarly, the loop gain  $L_O$  and the UGF can respectively be derived from Eqs. (2.26) and (2.27):

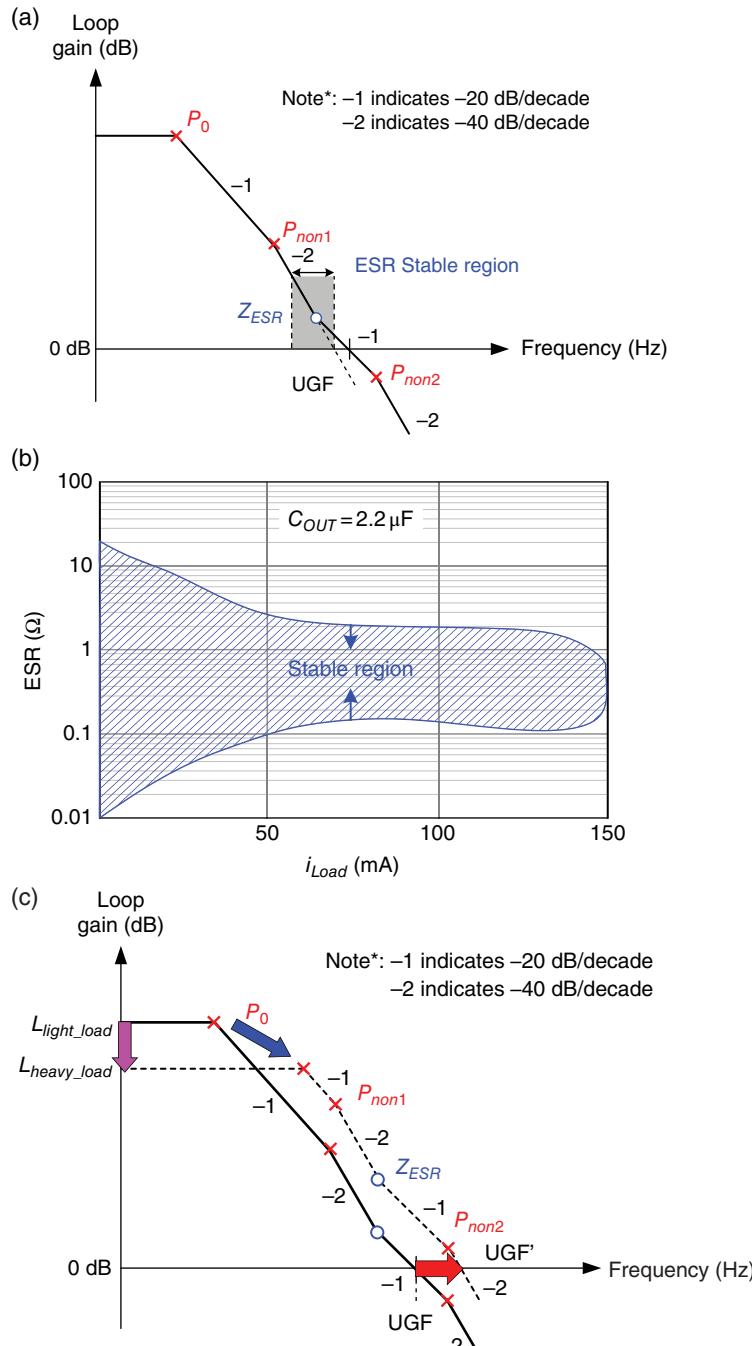
$$L_O = \beta A_{EA} A_{v(Mp)} \propto g_{mp} r_{OUT} \propto \sqrt{I_{Load}} \times \frac{1}{\lambda I_{Load}} = \frac{1}{\sqrt{I_{Load}}} \quad (2.26)$$

where  $\beta = \frac{R_2}{R_1 + R_2}$ ,  $A_{EA}$  is the error amplifier gain, and  $g_{mp} (\propto \sqrt{I_{Load}})$  is the transconductance of the power MOSFET;

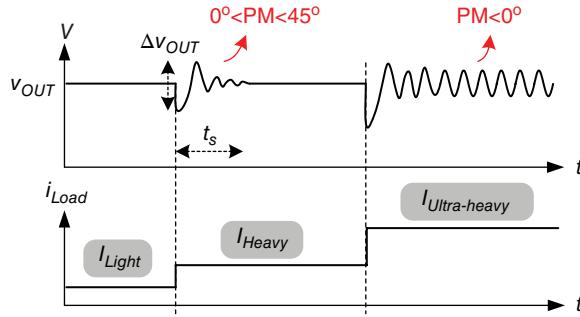
$$\text{UGF} = L_O \cdot P_0 \propto \sqrt{I_{Load}} \quad (2.27)$$

Although the loop gain  $L_O$  decreases when the load current increases, the UGF still moves toward high frequencies because  $P_0$  moves toward such frequencies more drastically than the decrease in  $L_O$ . However, a further decrease in  $L_O$  will degrade the regulation performance without benefiting the system stability.

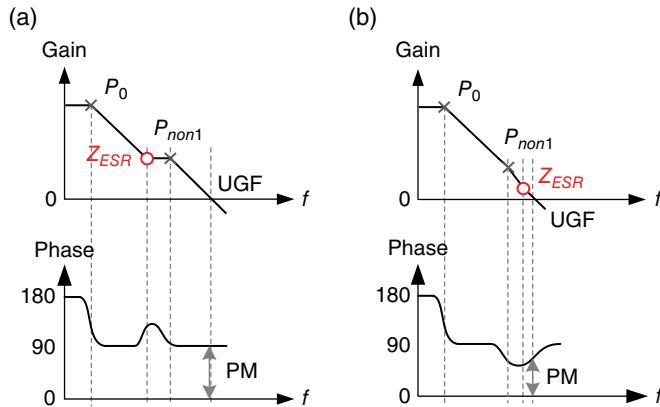
Figure 2.22 shows the output voltage waveforms in the LDO regulator with dominant-pole compensation. The PM degrades as the load increases, because the UGF moves toward high frequencies, and thus high-frequency poles appear below the UGF. When the PM degrades to a value that is smaller than  $45^\circ$ , the transient performance suffers from an obvious damping voltage variation ( $\Delta V_{OUT}$ ) and long settling time ( $t_s$ ). When the PM degrades to a value that is smaller than  $0^\circ$  under an ultra-heavy load, the feedback loop becomes a positive feedback and the output voltage experiences oscillation.



**Figure 2.21** Analysis of the frequency response of the LDO regulator with dominant-pole compensation. (a) ESR stable region. (b) Relationship of load current vs. ESR. (c) Frequency response under different load current conditions



**Figure 2.22** In dominant-pole compensation, the unstable phenomenon of the LDO regulator is caused by load current limitation as the load gradually changes from light to heavy



**Figure 2.23** If the second non-dominant pole can be disregarded, then (a) a large ESR results in a robust and stable system, whereas (b) a small ESR can achieve a small recovery transient time

Moreover, when ESR zero is utilized to compensate for the first non-dominant pole, it can be designed at a frequency lower or higher than  $P_{non1}$ , as shown in Figure 2.23(a), (b), respectively. When  $P_{non2}$  is considerably higher than the UGF and can be disregarded, the case presented in Figure 2.23(a) is more robust because the frequency of  $Z_{ESR}$  is lower than  $P_{non1}$  and can increase the PM to approximately  $90^\circ$ . However, the LDO regulator with  $90^\circ$  PM exhibits a stable transient response but a long recovery time. Moreover, a low-frequency  $Z_{ESR}$  implies a large  $R_{ESR}$  value, which seriously deteriorates the dip voltage of the transient response. By contrast, the case shown in Figure 2.23(b) can achieve an improved transient response with an adequate PM of approximately  $60^\circ$ .

Furthermore, the variation in  $R_{ESR}$  caused by the temperature change leads to a difficulty in achieving system stability. A variable  $R_{ESR}$  causes different  $Z_{ESR}$  frequencies, which in turn result in a varying UGF, even if the load condition does not change. The PM can be deteriorated by  $P_{non2}$  when the UGF draws closer to  $P_{non2}$ .

Consequently, the ESR compensation skill can hardly ensure stability under different load conditions because of the non-constant unit gain frequency. That is, no simple rule can define the ESR compensation. The best means to ensure stability is to use a large ESR in the worst-case scenario. However, an undesirably large  $R_{ESR}$  may cause an unintended voltage dip when the load changes. As such, other techniques to generate an extra zero without using a large ESR for the dominant-pole compensation skill can be utilized. Moreover, inserting a buffer stage can cause the non-dominant pole that is moving toward higher frequencies to alleviate the UGF constraint, as discussed in Section 2.2.

#### 2.4.1.1 Considering the Power MOSFET at the Triode Region

In the preceding discussion, the characteristic of frequency response is based on the power MOSFET that is operating in the saturation region. In general, when the voltage conversion ratio of the LDO regulator is large,  $V_{dropout}$  is also large, which enables the power MOSFET to operate easily in the saturation region with an acceptable silicon area. By contrast, when  $V_{dropout}$  is small or when the load range is large, keeping the power MOSFET operating within the saturation region is difficult. That is, the power MOSFET will operate in the triode region. In Soc applications, for example, the battery voltage and the conversion that supplies voltage to core devices are decreased simultaneously. Consequently,  $V_{dropout}$  is reduced and the power transistor operates in the triode region. The characteristics of frequency response are different from the results derived in Eq. (2.27). The characteristics of the dominant pole and loop gain can be derived from Eqs. (2.28) and (2.29), respectively. In addition, the UGF expressed in Eq. (2.30) is constant and independent of load current conditions:

$$P_{don} = P_0 = \frac{1}{r_{out} C_{OUT}} \propto \sqrt{I_{Load}}, \text{ where } r_{out} \propto \frac{1}{\sqrt{I_{Load}}} \quad (2.28)$$

$$L_o = \beta A_{oa} A_p = \beta g_{ma} r_{oa} g_{mp} r_{out} \propto \frac{1}{\sqrt{I_{Load}}} \quad (2.29)$$

$$\text{with } \begin{cases} \beta, g_{ma}, \text{ and } r_{oa} \text{ constant} \\ g_{mp} = \text{constant, when } V_{DS} \text{ is constant} \\ r_{out} \propto \frac{1}{\sqrt{I_{Load}}} \end{cases}$$

$$\text{UGF} = L_o \cdot P_{don} \propto \frac{1}{\sqrt{I_{Load}}} \cdot \sqrt{I_{Load}} = \text{constant} \quad (2.30)$$

Furthermore, for the power MOSFET that is operating in the triode region, the gain contributed by the power transistor degrades considerably. To maintain good output voltage regulation, enhancing the EA gain is necessary. Therefore, designing a gain-enhanced EA and an adequate pole/zero distribution is an important concern in the following discussion.

### 2.4.2 Characteristics of C-free Structure

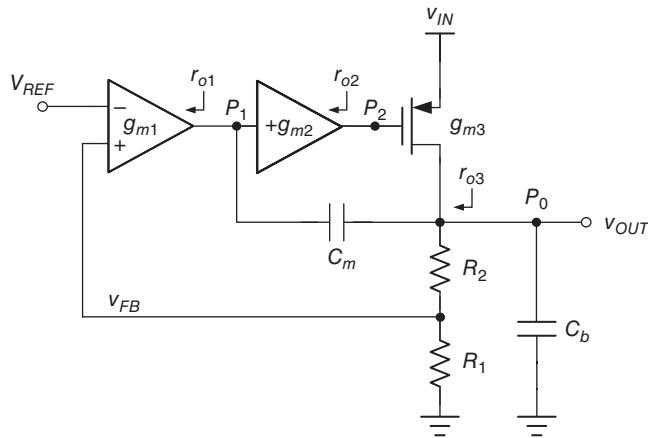
An A-LDO regulator with Miller compensation can be used to supply energy to the Soc if the output capacitance from the next stage is known. No extra output capacitor is required, and thus this regulator is called the *C-free* LDO regulator. The advantage of this regulator is its high integration in the entire Soc, with an embedded power management system, because of the absence of an output capacitor. Given that the output capacitance consists of parasitic capacitance, the transient response of *C-free* LDO regulators will be considerably different from that of dominant-pole compensation, even if only one small bypass capacitor  $C_b$  is used to prevent a large dip voltage from occurring in case of load current change.

As shown in the emulated reservoir and basin system illustrated in Figure 2.3, the basin is too small to experience any sudden load current change. Thus, the only means to solve the sudden change in load current is to turn on the faucet rapidly to provide sufficient water to the output. Consequently, the *C-free* LDO regulator should be designed as a multi-stage architecture to enable it to attain a high DC gain, which can extend the bandwidth. Furthermore, a small Miller capacitor is typically used to guarantee system stability even when the DC gain is increased by a multi-stage architecture.

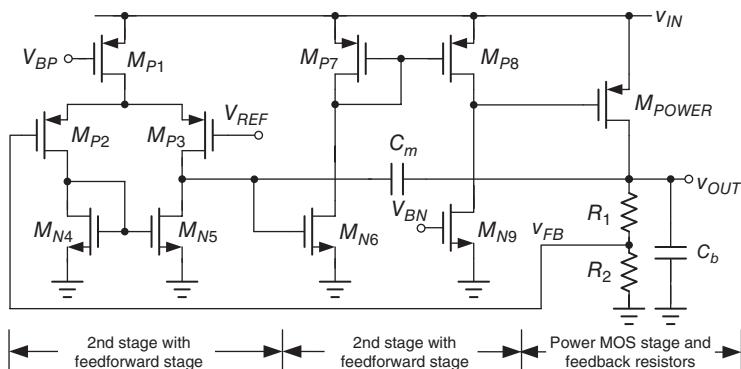
However, removing the output capacitor also results in several disadvantages in the regulated output voltage. Without a large output capacitor, the output voltage easily suffers from any noise disturbance or load transient variation. A noise disturbance at the output node is difficult to suppress because of the absence of a suitable bypass path. Such a path is formed by a large output capacitor in the dominant-pole compensation technique to generate high-frequency noise signals. When a heavy-to-light/light-to-heavy load transient occurs, redundant or insufficient energy will cause the voltage to overshoot or undershoot, respectively. To suppress the transient voltage variation, a large UGF is necessary to control the power transistor immediately and provide adequate power delivery. When a designer aims to obtain a large UGF for fast transient response, all non-dominant poles should be moved to frequencies that are considerably higher than the UGF. A multi-stage EA should be carefully designed to suppress any noise disturbance effectively.

Figure 2.24 shows the simplest LDO regulator designed using a three-stage OPA compensated with single Miller compensation (SMC) with a Miller capacitor  $C_m$  [1, 2]. By considering a large gate-to-drain capacitance  $C_{gd}$ , the LDO regulator has an inherent nested Miller compensation (NMC) structure [3–6]. The first stage consists of the transconductance  $g_{m1}$  of differential pairs to provide high gain. The second stage comprises positive  $g_{m2}$  as a single positive gain-boosting stage. The third stage involves the power P-MOSFET with its output impedance. Given its three stages, this structure has at least three poles. The dominant pole  $P_{non1}$  at the first stage output, which is contributed by a Miller capacitor  $C_m$ , is located at low frequencies. The first non-dominant pole  $P_{non2}$  appears at the gate of the power P-MOSFET because of its large size. The second non-dominant pole  $P_0$ , which is contributed by the output impedance because of its parasitic capacitance, is carried by the power line of the sub-supplied circuit and the equivalent output resistance.

Figure 2.25 shows a transistor-level example of the LDO regulator compensated by a single Miller capacitor  $C_m$ . The first stage, which is implemented by a differential amplifier, consists of transistors  $M_{P1}$ – $M_{P3}$  and  $M_{N4}$ ,  $M_{N5}$ .  $g_{m1}$  is the transconductance of the input differential pairs  $M_{P2}$  and  $M_{P3}$ . Transistors  $M_{N6}$  and  $M_{P7}$ ,  $M_{P8}$  form the second stage to provide a positive gain-boosting effect, where  $g_{m2}$  is the transconductance of  $M_{N6}$ . The power



**Figure 2.24** SMC for the three-stage LDO regulator

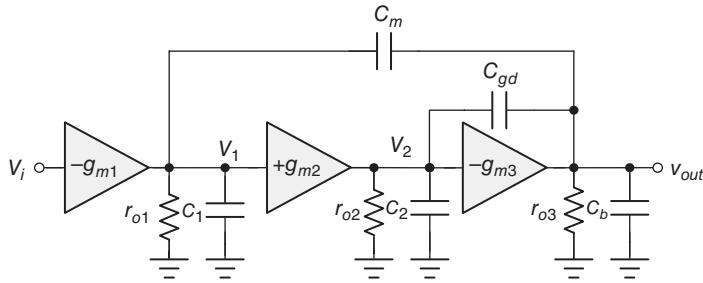


**Figure 2.25** SMC capacitor for the three-stage LDO regulator

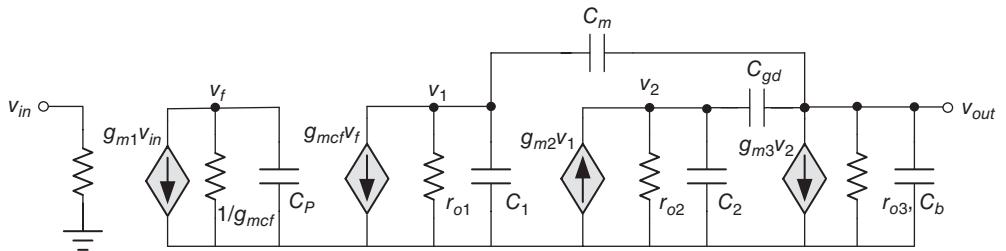
MOSFET and its output impedance form the third stage, where  $g_{m3}$  is the transconductance of  $M_{POWER}$ .

Figure 2.26 shows the simplified open-loop structure when considering all equivalent parasitic capacitances to analyze the frequency response, where  $g_{m1}$ ,  $g_{m2}$ , and  $g_{m3}$  are the transconductances of the first, second, and third stages, respectively.  $r_{o1}$ ,  $r_{o2}$ , and  $r_{o3}$  are the equivalent output resistance of each stage.  $C_1$ ,  $C_2$ , and  $C_b$  are the equivalent output capacitance of each stage. In particular,  $C_{gd}$  is included because of the large capacitance contributed by the power P-MOSFET.

The small signal model shown in Figure 2.26 is illustrated further in Figure 2.27. Based on Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) theorems, the transfer function from input to output can be given as in Eq. (2.31), where  $A_0$  is the open-loop



**Figure 2.26** Analysis of the LDO regulator with SMC skill



**Figure 2.27** Equivalent small signal model for the basic structure of the three-stage  $C$ -free LDO regulator

DC gain and  $P_{dom}$  (the dominant pole of the system) are expressed in Eqs. (2.32) and (2.33), respectively:

$$\frac{v_{out}}{v_i} = A_o \frac{\left(1 + s \frac{C_{gd}}{g_{m3}} - s^2 \frac{C_m C_{gd}}{g_{m2} g_{m3}}\right)}{\left(\frac{s}{P_{dom}} + 1\right) \left[s^2 \frac{C_{gd} C_b}{g_{m2} g_{m3}} + s \frac{C_{gd} (g_{m3} - g_{m2})}{g_{m2} g_{m3}} + 1\right]} \quad (2.31)$$

$$A_0 = g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} \quad (2.32)$$

$$P_{dom} = \frac{1}{r_{o1} [C_m (g_{m2} r_{o2} g_{m3} r_{o3})]} \quad (2.33)$$

Based on the numerator of Eq. (2.31), the second-order polynomial contains two zeros, which are separately located in RHP and LHP. The two zeros can be disregarded because they are located at high frequencies compared with the UGF. As mentioned in Section 2.2.2, if one LHP zero is required, then one null resistance can be in series with the Miller capacitor to convert RHP zero to LHP zero. One interesting result that can be observed is the UGF given in Eq. (2.34), which shows that its value is independent of the output capacitance because all non-dominant poles are pushed above the UGF:

$$\text{UGF} = A_0 \cdot P_{dom} = \frac{g_{m1}}{C_m} \quad (2.34)$$

The root locus of the  $C$ -free LDO regulator is shown in Figure 2.29 when the load current decreases. Under heavy loads, two non-dominant poles are separated at LHP. Two

high-frequency non-dominant poles, namely  $P_{non1}$  and  $P_{non2}$ , can be expressed in Eqs. (2.35) and (2.36), respectively. These poles are contributed by the gate-to-drain capacitance  $C_{gd}$  of the power MOSFET and the output capacitance  $C_3$ , respectively:

$$P_{non1} \approx \frac{g_{m2}}{C_{gd}} \quad (2.35)$$

$$P_{non2} \approx \frac{g_{m3} C_{gd}}{C_2 C_b} \quad (2.36)$$

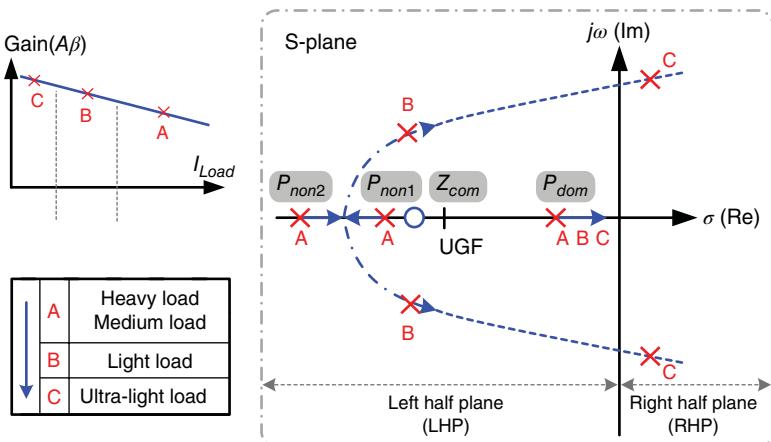
$P_{non2}$  is load dependent because it is located at the output node. That is,  $P_{non2}$  moves toward high and low frequencies at heavy and light loads. In case of decreasing load current, two separated poles will run into each other to become complex poles, as shown at point B in Figure 2.28. In this case, these poles remain located at LHP, and thus the system is stable but the PM decreases continuously. Once the load current decreases further to light or ultra-light load conditions, these two poles may move from LHP to RHP. The system becomes unstable, as shown at point C in Figure 2.28.

The natural frequency  $\omega_0$  and the damping factor  $Q$  are derived from Eqs. (2.37) and (2.38), respectively:

$$\omega_0 = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} \quad (2.37)$$

$$Q = \sqrt{\frac{C_2 C_b}{g_{m2} g_{m3}}} \frac{g_{m2} g_{m3}}{(g_{m3} - g_{m2}) C_{gd}} \quad (2.38)$$

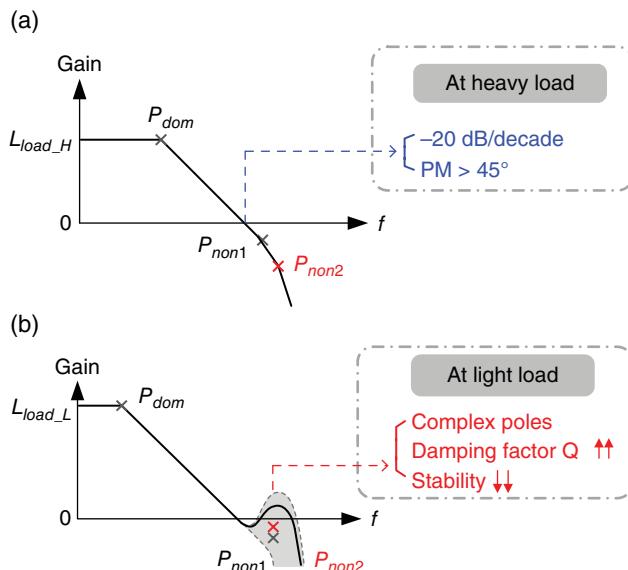
Similarly, we can explain the scenario of complex poles under light loads at different  $Q$  values. Given the decrease in  $g_{m3}$  under light loads, the denominator will gradually decrease and even become negative, which indicates that a high  $Q$  effect becomes serious under light loads.



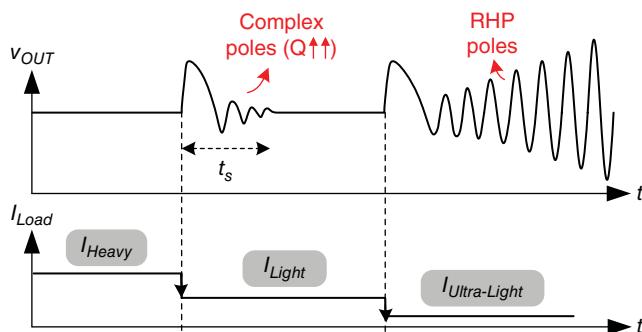
**Figure 2.28** Root locus of the  $C$ -free LDO regulator when the load current decreases

As soon as  $g_{m3}$  becomes smaller than  $g_{m2}$ , the complex poles move from LHP to RHP. Then, the system becomes unstable. Figure 2.29(a), (b) shows the positions of the two non-dominant poles under heavy and light loads, respectively. Given the frequency peaking that occurs in Figure 2.29(b) caused by the high  $Q$  effect, the gain margin and PM are insufficient to guarantee system stability.

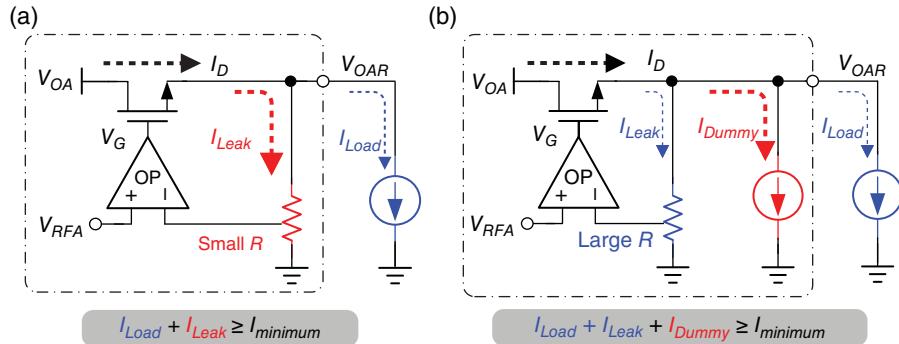
As illustrated in Figure 2.30, the output voltage gradually becomes unstable because of the variation in complex poles and the increase in  $Q$ , which is an expected phenomenon when the load current decreases continuously to ultra-light load conditions. Output voltage ringing and long settling time ( $t_s$ ) during the transient period are caused by insufficient gain margin and PM.



**Figure 2.29** Frequency response of the  $C$ -free LDO regulator at (a) heavy loads and (b) light loads



**Figure 2.30** Load transient response in case of different load current changes in the  $C$ -free LDO regulator



**Figure 2.31** Conventional solution to alleviate minimum load limitation in the *C-free* LDO regulator with (a) an increased quiescent current or (b) a dummy loading current

Moreover, the slewing problem affects the transient response time of the *C-free* LDO regulator. Without the assistance of an output capacitor during the load transient period, the transient response can be improved by a slightly higher quiescent current to achieve a low impedance and a high slew rate (SR). However, the current efficiency is poor under light loads. Moreover, the biasing current of the second stage should be sufficiently large to drive the power MOSFET and satisfy the transient requirements. Consequently, a high quiescent current increases the values of  $g_{m2}$  and  $Q$ . That is, the minimum load current constraint will become larger than the expected value because increasing  $g_{m2}$  will cause the denominator to decrease according to Eq. (2.45). Compared with the corresponding LDO design with dominant-pole compensation, the *C-free* LDO regulator exhibits poor transient performance if the quiescent current is limited to the same value in both compensation techniques.

In designing *C-free* LDO regulators, the minimum load current requirement constraint seriously degrades the PCE under light-load or no-load conditions. An extra minimum loading current at  $V_{OUT}$  of tens or hundreds of microamperes is necessary. That is, to avoid an unstable light-load scenario, the load current should be larger than the minimum load current constraint. The *C-free* LDO regulator exhibits the disadvantage of minimum load current constraint, which may cause the efficiency to degrade under considerably light loads. In battery-powered electronics, such a regulator will shorten the battery usage time. The basic minimum load current can be established by the leakage current generated by the feedback divider resistors. A dummy loading current is sometimes consumed at the output. Consequently, efficiency is restricted because of the increased leakage current ( $I_{Leak}$ ) or dummy load current ( $I_{Dummy}$ ) payment to satisfy the minimum load current requirements, as shown in Figure 2.31(a), (b), respectively. Although an ultra-light load is required when a Soc system enters standby mode, the current wasted through the power MOSFET remains large and results in substantial power loss. Thus, the battery usage time of portable electronics is shortened.

#### 2.4.2.1 Comparison between *C-out* LDO and *C-free* LDO

The preceding discussion presents the characteristics of dominant-pole compensation and the *C-free* structure. Table 2.2 provides a comparison of the LDO regulator design with different compensation methods. Considering Soc applications, the *C-free* LDO regulator is widely

**Table 2.2** Comparison between dominant-pole compensation LDO and *C-free* LDO

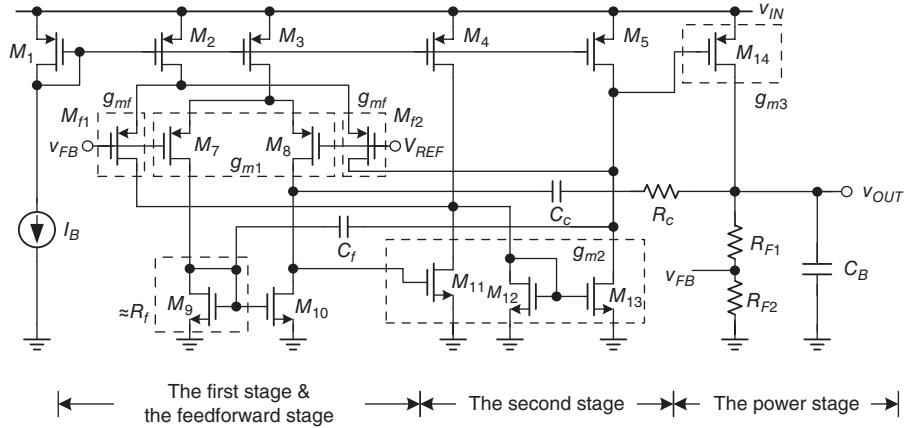
|                              | Dominant-pole compensation LDO   | <i>C-free</i> LDO  |
|------------------------------|--|--|
| Dominant pole                | Output capacitor   | Miller capacitor   |
| UGB to load condition        | 1. Saturation-region power MOSFET<br>→ Dependent<br>2. Linear-region power MOSFET<br>→ Independent | Independent  |
| Load range                   | Limitation of maximum load   | Limitation of minimum load   |
| Quiescent current            | 1. Increase for good SR and transient response   | 1. Increase for good SR<br>2. Increase for moving non-dominant pole to higher frequency<br>3. Increase for stability at ultra-light load |
| Defense of voltage variation | Excellent  | Poor   |
| DVS speed                    | Slow   | Fast   |

utilized compared with the dominant-pole compensation LDO regulator. However, based on the table, the *C-free* LDO controls the degraded performance because of the discarded large output capacitor. To improve performance and achieve competitive specifications, the following subsections introduce the design methodologies for the *C-free* LDO regulator.

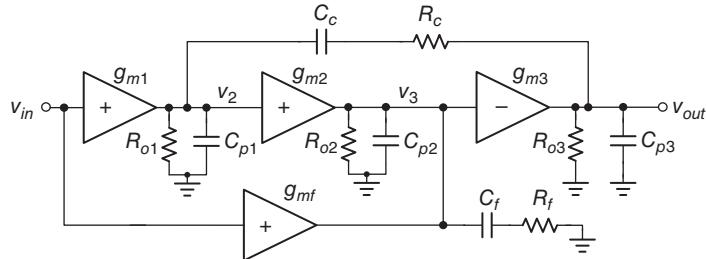
#### 2.4.3 Design of Low-Voltage *C-free* LDO Regulator

For the Soc applications fabricated in an advanced process, the voltage stress that can be sustained by core devices is drastically scaled down. Implementing a high gain in conventional designs via a cascode structure is difficult, because of the decreasing voltage headroom caused by the decreasing input voltage. Given the decreasing voltage headroom, designing a multi-stage *C-free* LDO regulator under a low-input-voltage operation is useful. Under low-voltage operation, a conventional LDO regulator with dominant-pole compensation suffers from low DC gain, and thus the regulation performance deteriorates drastically. In the currently available nanometer CMOS process, the Soc requires the local LDO regulator to provide regulation performance and high power supply rejection (PSR). That is, a multi-stage *C-free* LDO regulator with a capacitor-less structure and a high DC gain is one suitable design for low-input-voltage operation. In this study, we present several design techniques for *C-free* LDO regulators to improve the regulation performance.

Figure 2.32 shows the schematic of a multi-stage *C-free* LDO with a compensation-enhancement multi-stage amplifier (CEMA) [7]. To obtain high gain, the structure must consist of three gain stages. Transistors  $M_7$  and  $M_8$  constitute the first gain stage. The second stage is composed of transistor  $M_{11}$  with a current mirror to obtain a positive gain. Meanwhile, the



**Figure 2.32** Schematic of the multi-stage *C*-free LDO regulator with CEMA



**Figure 2.33** Small signal model of the CEMA structure in an open loop

power MOSFET  $M_{14}$  constitutes the third gain stage. The feedforward stage consists of transistors  $M_{f1}$  and  $M_{f2}$  to generate one compensation zero. The equivalent resistance  $R_f$  is composed of the diode-connected transistor  $M_9$ , and thus has an equivalent resistance of  $1/g_{m9}$ . This structure can be supplied by sub-1 V to overcome the small voltage headroom in the analog design and achieve on-chip compensation by simultaneously utilizing two small compensation capacitors. Given the cascaded structure, the voltage gain of the multi-stage amplifier can be increased even under low-voltage operation. A high gain and a large UGF can still be maintained by the multi-stage amplifier to achieve good regulation and a fast transient response, respectively.

Figure 2.33 shows the equivalent circuit of the multi-stage *C*-free LDO design, where  $C_c$ ,  $C_f$ , and  $R_f$  are the compensation components.  $L_O(s)$  expressed in Eq. (2.39) is the transfer function of the open loop. After simplifying Eq. (2.39), the DC gain and the positions of poles and zeros are shown in Eq. (2.40), which includes three poles ( $\omega_{pL2}$ ,  $\omega_{ph1L2}$ , and  $\omega_{ph2L2}$ ) and two zeros ( $\omega_{zL2}$  and  $\omega_{zhL2}$ ):

$$L_O(s) \approx \frac{K[1 + a_1 s + a_2 s^2]}{(1 + sC_c g_{m2} g_{m3} R_{o1} R_{o2} R_{o3})[1 + b_1 s + b_2 s^2]} \quad (2.39)$$

where

$$\begin{aligned}
 K &= g_{m1}g_{m2}g_{m3}R_{o1}R_{o2}R_{o3} \\
 a_2 &= \frac{g_{m1}g_{m2}R_{o1}R_cR_fC_cC_f}{g_{m1}g_{m2}R_{o1} + g_{mf}}, \quad a_1 = R_cC_c + \frac{g_{mf}R_{o1}C_c}{g_{m1}g_{m2}R_{o1} + g_{mf}} + R_fC_f \\
 b_1 &= \frac{(C_f + C_{p2})(C_c(R_{o1} + R_{o3} + R_c) + C_{p3}R_{o3})}{C_cg_{m2}g_{m3}R_{o1}R_{o3}} + \frac{C_{p3}(R_{o1} + R_c)}{g_{m2}g_{m3}R_{o1}R_{o2}} \\
 b_2 &= \frac{C_{p3}(C_f + C_{p2})(R_{o1} + R_c)}{g_{m2}g_{m3}R_{o1}} \\
 L_O(s) &\approx \frac{K \left(1 + \frac{s}{\omega_{pL2}}\right) \left(1 + \frac{s}{\omega_{zL2}}\right)}{\left(1 + \frac{s}{\omega_{pL2}}\right) \left(1 + \frac{s}{\omega_{ph1L2}}\right) \left(1 + \frac{s}{\omega_{ph2L2}}\right)} \tag{2.40}
 \end{aligned}$$

According to Miller's theorem, pole  $\omega_{pL2}$ , which is provided by Eq. (2.41) using a small on-chip capacitor  $C_c$  within the range of several pico-farads, is regarded as the system dominant pole:

$$\omega_{pL2} = \frac{1}{C_cg_{m2}g_{m3}R_{o1}R_{o2}R_{o3}} \tag{2.41}$$

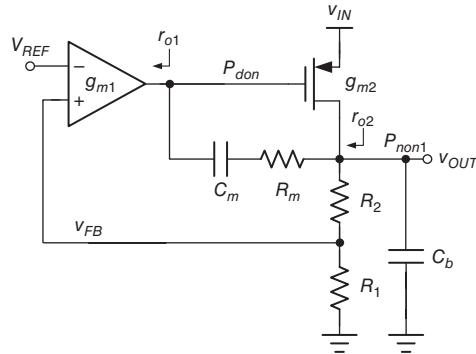
The compensation zero  $\omega_{zL2}$ , as expressed in Eq. (2.42), is generated by the feedforward gain stage in CEMA. Moreover, the on-chip compensation resistor  $R_c$  can further push  $\omega_{zL2}$  toward low frequencies to achieve adequate PM:

$$\omega_{zL2} \approx \frac{g_{m1}g_{m2}}{C_c(g_{mf} + R_cg_{m1}g_{m2})} \tag{2.42}$$

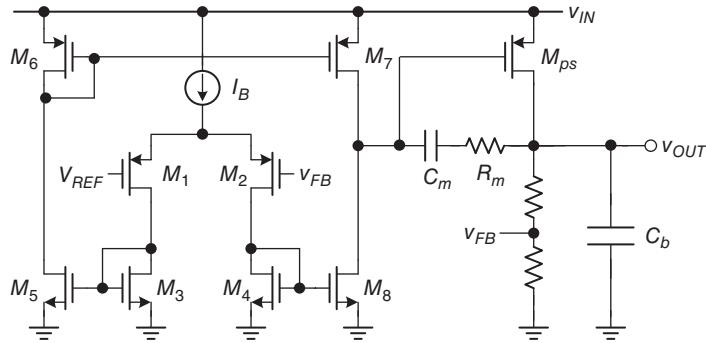
The generated low-frequency pole/zero pair, namely  $\omega_{pL2}$  and  $\omega_{zL2}$ , can guarantee system stability. Considering the other two non-dominant poles contributed by the second-order polynomial of the denominator of Eq. (2.39), the stability will deteriorate when complex poles are formed. To avoid complex poles, the criteria presented through Eq. (2.43) should be held:

$$\begin{aligned}
 b_1^2 &\geq 4b_2 \\
 \Rightarrow \left( \frac{(C_f + C_{p2})(C_c(R_{o1} + R_{o3} + R_c) + C_{p3}R_{o3})}{C_cg_{m2}g_{m3}R_{o1}R_{o3}} + \frac{C_{p3}(R_{o1} + R_c)}{g_{m2}g_{m3}R_{o1}R_{o2}} \right)^2 &\geq 4 \cdot \frac{C_{p3}(C_f + C_{p2})(R_{o1} + R_c)}{g_{m2}g_{m3}R_{o1}} \tag{2.43}
 \end{aligned}$$

In particular, satisfying the aforementioned inequality becomes difficult if the value of  $C_{p2}$  is small when the LDO regulator with a small power MOSFET requires working under low-power operation. Consequently, a compensation capacitor  $C_f$  is utilized to satisfy Eq. (2.43) easily. The pole-splitting technique is achieved for two non-dominant poles by providing the low impedance of  $1/g_{mf}$  through a short path with  $C_f$  at high frequencies. That is, the pole



**Figure 2.34** Two-stage *C*-free LDO regulator



**Figure 2.35** Circuit implementation of the two-stage *C*-free LDO regulator

at the second stage output can be moved toward higher frequencies. To understand the advantage of the multi-stage *C*-free LDO further, Figure 2.34 illustrates a simplified *C*-free LDO with two-stage structure for detailed comparison.

Figure 2.35 provides an example to illustrate the two-stage *C*-free LDO regulator.

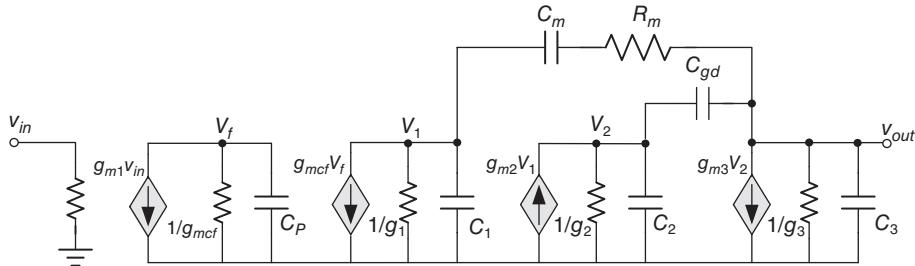
The transfer function can be derived from Eq. (2.44) according to the small signal model shown in Figure 2.36:

$$L_O'(s) \approx A_0 \frac{\left(1 + \frac{s}{Z_1}\right)}{\left(\frac{s}{P_{dom}} + 1\right)\left(\frac{s}{P_{non1}} + 1\right)} \quad (2.44)$$

where

$$A_0 = g_{m1}r_{o1}g_{m2}r_{o2}$$

$$P_{dom} \approx \frac{1}{r_{o1}[(C_m + C_{gd})g_{m2}r_{o2}]}$$



**Figure 2.36** Equivalent small signal model of the two-stage *C*-free LDO regulator

$$P_{non1} = \frac{1}{r_{o2}C_b}, Z_1 = \frac{1}{R_m C_m}$$

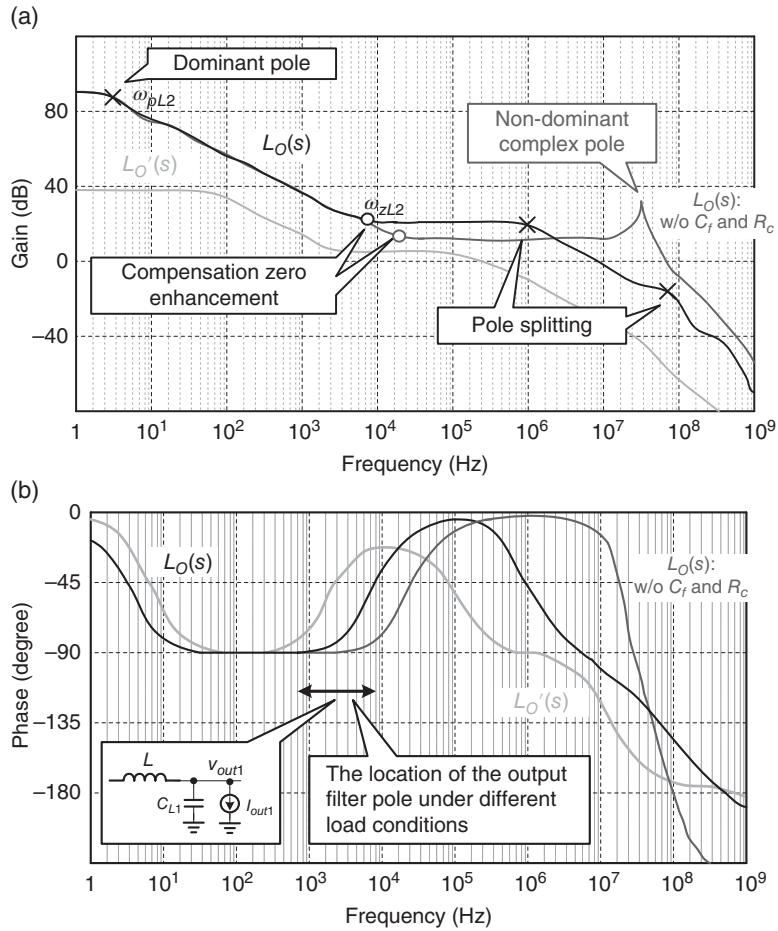
In Eq. (2.44), the dominant pole  $P_{dom}$  is contributed by the Miller capacitor and  $C_{gd}$  at the node of the gate of the power P-MOSFET. Given that the power MOSFET is sufficiently large,  $C_{gd}$  behaves as the Miller capacitance without requiring an extra physical capacitor. By contrast, the only non-dominant pole  $P_{non1}$  is generated at the output node. To extend the UGF further, zero  $Z_1$ , which is provided by  $C_m$  and  $R_m$ , can be used to cancel the effect of  $P_{non1}$ . However, the two-stage *C*-free LDO cannot achieve a high gain. Moreover, the UGF is limited by  $P_{non1}$  under light loads because  $Z_1$  cannot compensate for the PM over a wide load range.

Figure 2.37 presents a comparison of the frequency responses of the LDO regulators with a two-stage structure, a three-stage structure, and a three-stage structure with CEMA. The  $L_O'(s)$  from the two-stage *C*-free LDO has a DC voltage gain that is significantly smaller than 40 dB, which cannot guarantee a regulated output driving voltage in the power management module. Meanwhile, the  $L_O(s)$  from the three-stage structure with CEMA can effectively provide a high DC gain even under a low supply voltage operation of 1 V. That is, the DC voltage gain can be raised higher than 80 dB to achieve good regulation performance. In addition, the compensation zero enhancement and non-dominant pole splitting in CEMA are indicated. The location of the output filter pole of the DC/DC converter is also provided in Figure 2.37. The system PM varies from 55° to 80° under different load conditions.

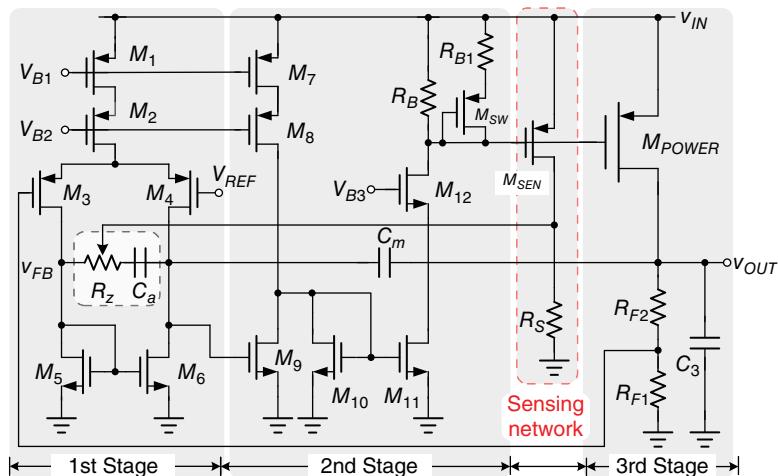
#### 2.4.4 Alleviating Minimum Load Current Constraint through the Current Feedback Compensation (CFC) Technique in the Multi-stage C-free LDO Regulator

In general, the LDO regulator should guarantee high PSR and fast transient response. Hence, these two factors should be simultaneously considered along with minimum load current. In this case, the multi-stage LDO with the current feedback compensation (CFC) technique can be used to alleviate the minimum load constraint for the *C*-free LDO regulator while achieving high PSR and fast transient response.

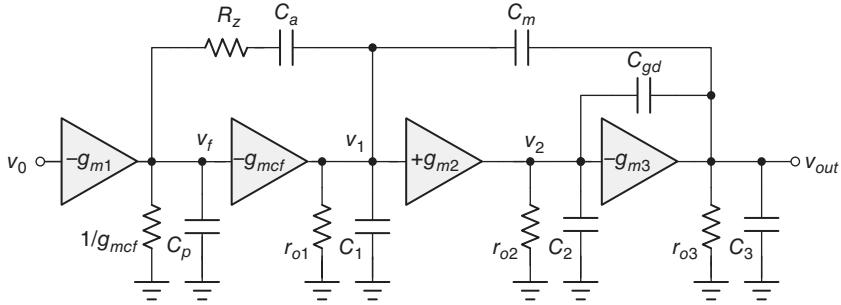
The CFC structure consists of three stages, as shown in Figure 2.38. The first stage, which involves  $M_1$ – $M_6$ , converts differential in-signals to single-end out-signals and achieves high gain. The second stage involves  $M_7$ – $M_{12}$  and  $R_B$ . During this stage, transistors  $M_7$ – $M_{10}$  form



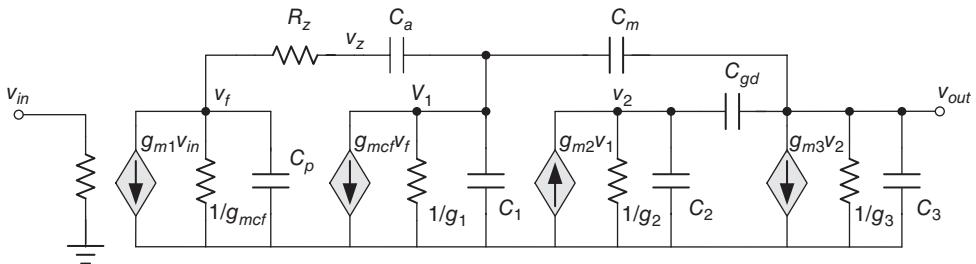
**Figure 2.37** Comparison of three different EAs in frequency response. (a) Gain. (b) Phase



**Figure 2.38** Architecture of the CFC C-free LDO regulator



**Figure 2.39** Equivalent small signal circuit of the CFC *C*-free LDO regulator



**Figure 2.40** Complete small signal model of the CFC *C*-free LDO regulator

a wideband stage and create a ground reference. Meanwhile, transistors  $M_{11}$  and  $M_{12}$  form a CS stage with resistive load  $R_B$  to achieve high PSR performance. The third stage is structured by the power P-MOSFET with CS configuration. The feedback divider resistors  $R_{F1}$  and  $R_{F2}$  form the shunt feedback to regulate the output voltage. The Miller capacitor is connected to both the ground reference node, which is the output of the first stage, and the output node to avoid noise that is directly passing from the supply source to the output. The compensation network  $C_a$  and the resistance  $R_Z$  are used to control the gain and the phase dynamically under different loads. The value of the resistance  $R_Z$  can be adjusted by the current sensing network, which is composed of  $M_{SEN}$  and  $R_S$ .

The analysis structure of the CFC *C*-free LDO regulator is illustrated in Figure 2.39.  $g_{m1}$ ,  $g_{m2}$ , and  $g_{m3}$  are the equivalent transconductances of each stage.  $r_{o1}$ ,  $r_{o2}$ , and  $r_{o3}$  are the equivalent output reactances of each stage.  $C_1$ ,  $C_2$ , and  $C_3$  are the lumped parasitic capacitors of each stage. Given that the value of the gate-to-drain capacitor of the power P-MOSFET is large, the parasitic capacitor should be considered and is represented as  $C_{gd}$ .

Based on the KVL and KCL theorems, the transfer function of Figure 2.40 from the input to the output can be derived from Eq. (2.45), where  $A_o$  is the open-loop DC gain as expressed in Eq. (2.46). The dominant pole of this system is  $P_{dom}$ :

$$\frac{v_{out}}{v_0} = -A_{vo} \frac{(sC_aR_z + 1)(a_2s^2 + a_1s - 1)}{\left(1 + \frac{s}{P_{dom}}\right)\left(1 + \frac{s}{P_{non1}}\right)} \cdot \frac{1}{(b_2s^2 + b_1s + 1)} \quad (2.45)$$

where

$$a_2 = \frac{C_m C_2}{g_{m2} g_{m3}}, \quad a_1 = \frac{g_{m2} C_{gd}}{g_{m2} g_{m3}}, \quad b_2 = \frac{C_2 C_3}{g_{m2} g_{m3}}$$

$$b_1 = \frac{\left(\frac{1}{g_{mcf}} + R_z\right) \left(C_3 / r_{o2} + C_2 / r_{o3} + (g_{m3} - g_{m2}) C_{gd}\right) C_a C_m + (C_m + 2C_a) C_2 C_3}{\left(C_3 / r_{o2} + C_2 / r_{o3} + (g_{m3} - g_{m2}) C_{gd}\right) (C_m + 2C_a) + 2g_{m2} C_{gd} C_a + \left(\frac{1}{g_{mcf}} + R_z\right) g_{m2} g_{m3} C_a C_m}$$

$$A_{vo} = g_{m1} r_{o1} g_{m2} r_{o2} g_{m3} r_{o3} \quad (2.46)$$

The system consists of four poles and three zeros. One LHP zero  $Z_{LHP}$  for dynamic compensation is contributed by the capacitor  $C_a$  and the resistor  $R_Z$ :

$$Z_{LHP} = \frac{1}{C_a R_Z} \quad (2.47)$$

The two zeros provided by the second-order polynomial are each located in RHP and LHP. These zeros can be disregarded because they are considerably higher than the UGF. The dominant pole in Eq. (2.48), which is proportional to the root of  $I_{Load}$ , is decided by  $C_m$  and the output resistance in the first stage:

$$P_{dom} = \frac{g_1 g_2 g_3}{g_{m2} g_{m3} C_m} \propto \frac{1}{\sqrt{I_{Load}} \times \frac{1}{I_{Load}}} = \sqrt{I_{Load}} \quad (2.48)$$

The second and third non-dominant poles,  $P_{non2}$  and  $P_{non3}$ , are respectively generated by the gate-to-drain capacitance  $C_{gd}$  at the gate of the power P-MOSFET and the capacitor  $C_3$  at the output node. Given that  $P_{non3}$  depends strongly on  $I_{Load}$ , the two poles from the second-order polynomial in the denominator of Eq. (2.45) can be expressed in different forms under various load conditions for a clear analysis.  $P_{non3}$  moves toward high frequencies under heavy loads, and thus  $P_{non2}$  and  $P_{non3}$ , which are roughly expressed as in Eq. (2.49), are far from each other. By contrast,  $P_{non2}$  and  $P_{non3}$  are close to each other when  $P_{non3}$  moves toward low frequencies under light loads.

$$P_{non2} = \frac{g_{m2}}{C_{gd}}, \quad P_{non3} = \frac{g_{m3} C_{gd}}{C_2 C_3} \text{ under heavy loads} \quad (2.49)$$

To discuss the effect of complex poles, the natural frequency  $\omega_0$  and a damping factor featured in  $P_{non2}$  and  $P_{non3}$  can be derived as follows:

$$\omega_o = \sqrt{\frac{g_{m2} g_{m3}}{C_2 C_3}} \text{ and}$$

$$Q = \sqrt{\frac{\frac{1}{C_2 C_3} (g_2 C_3 + g_3 C_2 + (g_{m3} - g_{m2}) C_{gd}) (C_m + 2C_a) + 2g_{m2} C_{gd} C_a + \left(\frac{1}{g_{mcf}} + R_Z\right) g_{m2} g_{m3} C_a C_m}{g_{m2} g_{m3} \left(\frac{1}{g_{mcf}} + R_Z\right) (g_2 C_3 + g_3 C_2 + (g_{m3} - g_{m2}) C_{gd}) C_a C_m + (C_m + 2C_a) C_2 C_3}} \quad (2.50)$$

under light loads

To alleviate the influence of a high  $Q$  value, which results from the two non-dominant poles under light loads, an extra pole  $P_{non1}$ , expressed in Eq. (2.51), is inserted into the frequency around the UGF:

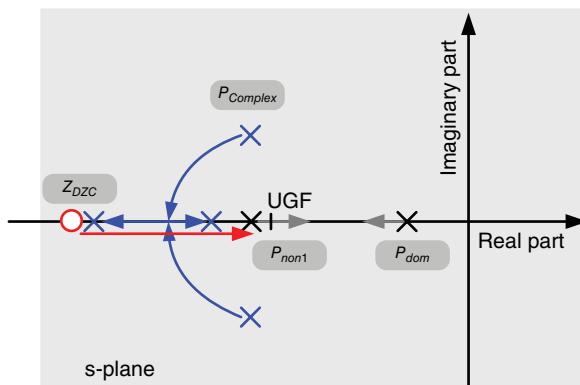
$$P_{non1} = \frac{g_{m2}g_{m3}C_m}{\left(\frac{1}{g_{mcf}} + R_Z\right)g_{m2}g_{m3}C_aC_m + \left(C_2/r_{o3} + g_{m3}C_{gd}\right)(C_m + 2C_a)} \propto \frac{1}{k_1 + k_2\sqrt{I_{Load}}} \quad (2.51)$$

where

$$k_1 = C_a \left( \frac{1}{g_{mcf}} + R_Z \right) \text{ and } k_2 = \frac{C_2(C_m + 2C_a)}{g_{m2}C_m}$$

Figure 2.41 illustrates the root locus of the poles and zeros when the load current increases from light to heavy. The UGF is nearly constant in the aforementioned *C-free* structure. According to Eqs. (2.48) and (2.51),  $P_{dom}$  moves to a high frequency, whereas  $P_{non1}$  moves to a low frequency. The lower frequency of  $P_{non1}$  deteriorates the PM, and thus the compensated zero with a large resistor  $R_Z$  can dynamically move to a lower frequency under heavy loads to guarantee stability. Moreover, the complex poles will separate into two poles as the load current increases. This phenomenon implies that the effects of  $P_{non2}$  and  $P_{non3}$  can be disregarded under heavy loads.

Compared with the  $Q$  value of the basic *C-free* LDO regulator shown in Eq. (2.38), the CFC technique uses the  $C_a$ ,  $R_Z$ , and dynamic output impedance of the second stage to introduce other factors and maintain a low  $Q$  value over a wide range of load conditions, as indicated in Eq. (2.50). Moreover, this technique realizes the minimum load constraint by an existing LHP pole even under ultra-light loads.



**Figure 2.41** Poles and zero locations of the CFC LDO as the load increases

#### 2.4.4.1 Ultra-Light Load Condition with Small $R_Z$

Under light loads,  $P_{non2}$  and  $P_{non3}$  form complex poles with a three-stage LDO design. In this case, Eq. (2.50) can be simplified to Eq. (2.52) and  $Q$  can be reduced by the second and third terms of the denominator, that is  $C_2C_3(C_m+2C_a)/(1/g_{mcf}+R_Z)$  and  $g_2C_aC_mC_3$ , to decrease its value:

$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \frac{g_{m2}g_{m3}C_aC_m}{(g_{m3}-g_{m2})C_aC_mC_{gd} + g_2C_aC_mC_3 + \left(\frac{1}{g_{mcf}} + R_Z\right)} \quad (2.52)$$

The compensated resistor  $R_Z$  should be small to achieve a low  $Q$  value. Based on direct observation,  $R_Z$  increases the equivalent resistance at the output node through the path of  $C_m$  at high frequencies. That is, the equivalent resistance is  $R_Z$  in series with  $1/g_{mcf}$ . The sensing network can adjust  $R_Z$  to have a small value under ultra-light loads.  $Q$  and  $P_{non1}$  can be derived from Eqs. (2.53) and (2.54), respectively, as follows:

$$P_{non1} = \frac{g_{mcf}}{C_a} \quad (2.53)$$

$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \cdot \frac{\frac{1}{g_{mcf}}g_{m2}g_{m3}C_aC_m}{(C_m + 2C_a)C_2C_3} = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \cdot \frac{\frac{1}{g_{mcf}}g_{m2}g_{m3}C_m}{\left(\frac{C_m}{C_a} + 2\right)C_2C_3} \quad (2.54)$$

Although  $R_Z$  is helpful in reducing  $Q$ , the peaking of  $Q$  still affects stability. To improve the constraint of minimum load current further, pole  $P_{non1}$  is set at a frequency that is near the UGF. Figure 2.42 illustrates the contribution of  $P_{non1}$ , which accelerates the decay of the gain after surpassing the frequency of the UGF.

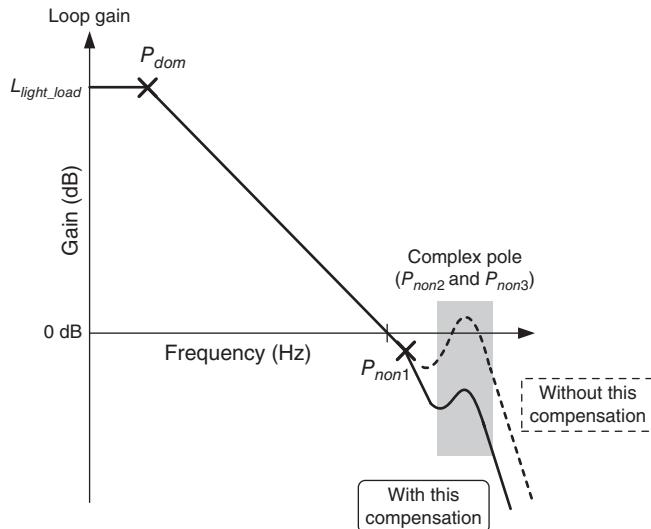
To maintain the PM at approximately  $60^\circ$ ,  $P_{non1}$  must be placed twice higher than the UGF, as shown in Eq. (2.55). This setup results in a low  $Q$  of 5.

$$P_{non1} > 2 \cdot \text{UGF} = 2 \frac{g_{m1}}{C_m} \quad (2.55)$$

To avoid complex poles and an unstable system, the first non-dominant pole must be set to at least half the natural frequency, as shown in Eq. (2.56). Given that the magnitude rolls off with a slope of  $-20$  dB/decade after the UGF and a slope of  $-40$  dB/decade after the first non-dominant pole, a gain margin of at least  $18$  dB exists for complex poles and low  $Q$  approximations.

$$P_{non1} < \frac{1}{2}\omega_o \quad (2.56)$$

The compensated zero is located at a relatively high frequency compared with the UGF, because  $R_Z$  is small. Consequently, the PM of the overall system can be determined by Eq. (2.57), which is near  $60^\circ$ :



**Figure 2.42** CFC capacitor-free LDO under a light load condition

$$\begin{aligned}
 PM &= 180^\circ - \tan^{-1} \left( \frac{\text{UGF}}{P_{don}} \right) - \tan^{-1} \left( \frac{\text{UGF}}{P_{non1}} \right) - \tan^{-1} \left( \frac{\frac{\text{UGF}}{\omega_o}}{Q \left[ 1 - \left( \frac{\text{UGF}}{\omega_o} \right)^2 \right]} \right) \\
 &= 90^\circ - \tan^{-1} \left( \frac{\text{UGF}}{P_{non1}} \right) - \tan^{-1} \left( \frac{\frac{\text{UGF}}{\omega_o}}{Q \left[ 1 - \left( \frac{\text{UGF}}{\omega_o} \right)^2 \right]} \right) = 90^\circ - 26.56^\circ - 2^\circ \approx 60^\circ
 \end{aligned} \tag{2.57}$$

Based on the preceding analysis, compensation capacitors  $C_m$  and  $C_a$  can be derived from Eqs. (2.58) and (2.59), respectively, as follows:

$$C_m = 2 \frac{g_{m1}}{g_{mcf}} C_a = 4 g_{m1} \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \tag{2.58}$$

$$C_a = 2 g_{mcf} \sqrt{\frac{C_2 C_3}{g_{m2} g_{m3}}} \tag{2.59}$$

#### 2.4.4.2 Light-to-Medium Load Condition

As the load increases from light to medium, that is 1–10 mA,  $P_{non1}$  moves toward lower frequencies because  $R_Z$  increases. As the  $R_Z$  value increases,  $P_{non1}$ ,  $\omega_0$ , and  $Q$  can be derived from

Eqs. (2.60) to (2.62), respectively. In this case, a low  $Q$  can also be maintained, and Eq. (2.63) still holds true because of the slight probability of  $R_Z$ :

$$P_{non1} = \frac{1}{\left(\frac{1}{g_{mcf}} + R_Z\right)C_a} \quad (2.60)$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_2C_3}} \quad (2.61)$$

$$Q = \sqrt{\frac{C_2C_3}{g_{m2}g_{m3}}} \cdot \frac{g_{m2}}{C_{gd}} \quad (2.62)$$

$$P_{non1} > 2 \cdot \text{UGF} \quad (2.63)$$

The PM of the overall system can be determined by  $P_{dom}$  and  $P_{non1}$ , as shown in Eq. (2.64):

$$\begin{aligned} \text{PM} &= 180^\circ - \tan^{-1}\left(\frac{\text{UGF}}{P_{dom}}\right) - \tan^{-1}\left(\frac{\text{UGF}}{P_{non1}}\right) \\ &= 90^\circ - \tan^{-1}\left(\frac{\text{UGF}}{P_{non1}}\right) \\ &\approx 60^\circ \end{aligned} \quad (2.64)$$

#### 2.4.4.3 Heavy Load Condition with Large $R_Z$

As the load increases further from 10 to 100 mA,  $P_{non1}$ , as shown in Eq. (2.65), will move to a lower frequency, because both the output reactance  $g_3$  and  $R_Z$  increase. The low-frequency zero  $Z_{DZC}$ , expressed in Eq. (2.66), will alleviate the  $P_{non1}$  effect:

$$P_{non1} = \frac{g_{m2}g_{m3}C_m}{\left(\frac{1}{g_{mcf}} + R_Z\right)g_{m2}g_{m3}C_aC_m + g_3C_2(C_m + 2C_a)} \quad (2.65)$$

$$Z_1 = \frac{1}{R_ZC_a} \quad (2.66)$$

The second-order polynomial in Eq. (2.45) can be simplified to Eq. (2.67) under heavy loads. If the discriminant function of the second-order polynomial in Eq. (2.67) is smaller than zero, then a pair of complex poles exists in the system. However, these complex poles are located at high frequencies and have no effect on the system stability. If the discriminant function of the second-order polynomial in Eq. (2.67) is larger than zero, then two separate poles exist in the system. Finally, if a second non-dominant pole exists, then the locations of the poles are shown in Eq. (2.68), which are found at high frequencies and have negligible effects on the system stability:

$$s^2 \frac{C_2 C_3}{g_{m2} g_{m3}} + s \frac{g_3 C_2 + g_{m3} C_{gd}}{g_{m2} g_{m3}} + 1 \approx s^2 \frac{C_2 C_3}{g_{m2} g_{m3}} + s \frac{g_{m3} C_{gd}}{g_{m2} g_{m3}} + 1 \quad (2.67)$$

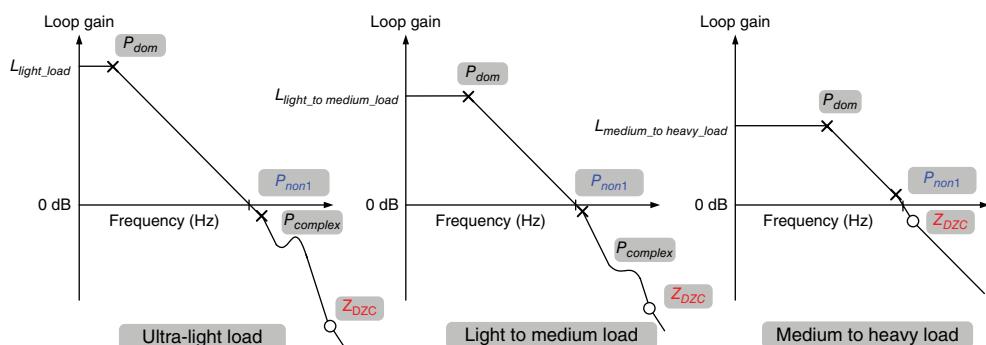
$$\begin{aligned} P_{non2} &= \frac{g_{m2} g_{m3}}{g_3 C_2 + g_{m3} C_{gd}} \quad \text{and} \quad P_{non3} = \frac{g_3 C_2 + g_{m3} C_{gd}}{C_2 C_3} \\ \Rightarrow P_{non2} &= \frac{g_{m2}}{C_{gd}} \quad \text{and} \quad P_{non3} = \frac{g_{m3} C_{gd}}{C_2 C_3} \end{aligned} \quad (2.68)$$

The overall system contains two low poles and one low zero. The system stability can be determined as follows:

$$\begin{aligned} \text{PM} &= 180^\circ - \tan^{-1} \left( \frac{\text{UGF}}{P_{don}} \right) - \tan^{-1} \left( \frac{\text{UGF}}{P_{1st-non}} \right) + \tan^{-1} \left( \frac{\text{UGF}}{Z_{LHP}} \right) \\ &= 90^\circ - \tan^{-1} \left( \frac{\text{UGF}}{P_{1st-non}} \right) + \tan^{-1} \left( \frac{\text{UGF}}{Z_{LHP}} \right) \\ &\approx 60^\circ \end{aligned} \quad (2.69)$$

#### 2.4.4.4 Summary of CFC Capacitor-Free LDO Regulators

The frequency responses of CFC capacitor-free LDO regulators under different load conditions are summarized in Figure 2.43. Under ultra-light load conditions smaller than 1 mA, the dominant pole contributes a 90° phase shift. The first non-dominant pole contributes a near 30° phase shift, and the complex poles contribute minimal phase shift. The overall system stability can be maintained at 60°. Under light to medium load conditions, that is approximately 1–10 mA, the dominant pole contributes the same phase shift. The first non-dominant pole moves to lower frequencies and contributes a 30° phase shift. The complex poles move to higher frequencies and do not contribute any phase shift. Thus, the system stability is maintained at 60°. Finally, under medium to heavy load conditions, approximately 10–100 mA, the dominant pole contributes the same phase shift. The first non-dominant pole moves further



**Figure 2.43** Variations of poles and zero locations in the CFC C-free LDO regulator over a wide load range

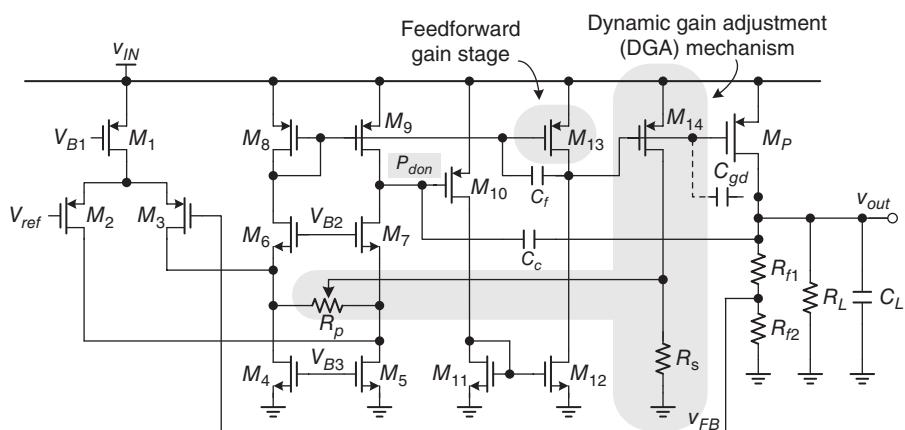
toward even lower frequencies, and the dynamic zero also moves toward lower frequencies to alleviate the pole effect. Therefore, the PM of the CFC *C-free* LDO regulator can be maintained at 60° within the entire load range.

#### 2.4.5 Multi-stage LDO Regulator with Feedforward Path and Dynamic Gain Adjustment (DGA)

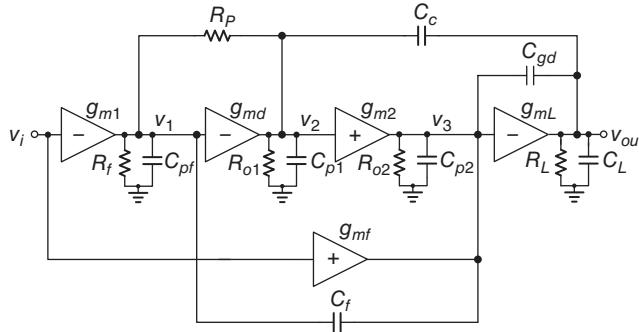
With the development of advanced nanometer processes in recent years, the supply voltage has been continuously scaled down. Consequently, LDO regulators are required to operate under sub-1 V. To understand the design in detail, an example implemented in a 65 nm CMOS technology is presented here. The design specifications are described as follows. The input voltage  $V_{IN}$  can range from 0.9 to 1.2 V; the latter is the voltage stress of the 65 nm core device. The dropout voltage is approximately 200 mV, with a maximum load current of 100 mA. To achieve stable operation, a minimum load of 50  $\mu$ A is required.

Figure 2.44 shows a schematic of the four-stage LDO with feedforward path and dynamic gain adjustment (DGA). Moreover, the feedforward gain stage contributed by  $M_{13}$  is included to accelerate the transient response at the gate of the power P-MOSFET  $M_P$ . As mentioned earlier, the feedforward path contributes LHP zero in the frequency domain to improve stability. The DGA mechanism, which consists of  $M_{14}$  and  $R_S$ , is used to sense the load current and adjust the resistance value of  $R_p$  to guarantee stability even at ultra-light loads.

Figure 2.45 shows the structure of the sub-1 V multi-stage LDO design. Considering its cascade structure, the voltage gain of the multi-stage amplifier can be increased under low-voltage operation. A high-voltage gain is basically composed of three gain stages:  $g_{m1}$ , which includes  $g_{md}$ ,  $g_{m2}$ , and  $g_{mL}$ . Moreover, a feedforward gain stage  $g_{mf}$  accelerates the slew rate at the gate of the pass element and generates LHP zero to improve LDO stability. In addition, the compensation capacitor  $C_c$  is amplified by Miller's theorem to determine the dominant pole in the system.  $C_f$  is inserted to split high-frequency complex poles under light loads and prevent



**Figure 2.44** Schematic of the sub-1 V four-stage LDO with feedforward gain stage and DGA mechanism



**Figure 2.45** Structure of the sub-1 V multi-stage LDO regulator

non-dominant complex poles from moving toward RHP to ensure stability. Furthermore, resistance  $R_p$  is proportionally adjusted to  $I_{Load}$  by the DGA mechanism. Hence,  $R_p$  can be used to adjust the DC voltage gain and the UGF to avoid phase deterioration under ultra-light loads. The transfer function is given in Eq. (2.70) according to Figure 2.45. The exact analysis of the multi-stage LDO can be illustrated through three different output load conditions, as discussed in the following subsections.

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L \frac{R_f(g_{md}R_p - 1)}{(R_p + g_{md}R_{o1}R_f)}} \left[ 1 + s \left( R_f C_f + \frac{g_{mf}R_{o1}C_c}{g_{m1}g_{m2}R_{o1} + g_{mf}} \right) \right] \\ \frac{(1 + sC_c g_{m2}g_{mL}R_{o1}R_{o2}R_L) \left[ 1 + s \frac{(R_p + R_f)(g_{md}(C_{gd} + C_f) - g_{m2}(C_c + C_L)) + g_{mf}(C_f + C_2 + C_c)}{g_{m2}g_{mL}} + s^2 \frac{C_L(C_{gd} + C_f + C_2)}{g_{m2}g_{mL}} \right]}{(2.70)}$$

#### 2.4.5.1 Medium to Heavy Load Currents ( $g_{mL}$ Significantly Larger than $g_{m1}$ and $g_{m2}$ )

As the load current increases from 10 to 100 mA, the transfer function in Eq. (2.70) is approximated as:

$$\frac{v_{out}}{v_{in}} \approx \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_L \left( 1 + s \frac{g_{mf}C_c}{g_{m1}g_{m2}} \right)}{\left( 1 + s \frac{(C_{gd} + C_f + C_2)(R_p + R_f)}{g_{m2}} \right) \left[ 1 + s \frac{g_{m2}}{g_{m2}g_{mL}} + s^2 \frac{C_L(C_{gd} + C_f + C_2)}{g_{m2}g_{mL}} \right]} \quad (2.71)$$

The dominant pole  $\omega_{don}$ , a feedforward LHP zero  $\omega_{zf}$ , and a system UGF are given respectively as:

$$\omega_{don} = \frac{1}{C_c g_{m2}g_{mL}R_{o1}R_{o2}R_L} \quad (2.72)$$

$$\omega_{zf} = \frac{g_{m1}g_{m2}}{C_c g_{mf1}} \quad (2.73)$$

$$\text{UGF} = \frac{g_{m1}}{C_c} \quad (2.74)$$

The first non-dominant pole at the gate of the power MOSFET is close to the feedforward zero  $\omega_{zf}$ . Moreover, the second non-dominant pole at the output node is located at high frequencies because of the large  $g_{mL}$ . Consequently, a one-pole system is achieved with a theoretical PM of 90°. Thus, the stable operation of the multi-stage LDO is derived under medium to heavy load conditions because of the split high-frequency LHP non-dominant poles.

#### 2.4.5.2 Light to Medium Output Load Currents ( $g_{mL}$ Slightly Larger than $g_{m1}$ and $g_{m2}$ )

As the load current increases from a light to a medium load range, that is approximately 1–10 mA, the non-dominant pole at the output node moves toward the origin, which results in the occurrence of complex poles, with the first non-dominant pole at the gate of the power MOSFET. Based on the transfer function of Eq. (2.70), the relationship among non-dominant complex poles can be exhibited as follows:

$$\text{UGF} = \frac{g_{m1}}{C_c} \quad (2.75)$$

Under this condition, complex poles are located at high frequencies, but will have an influence on the phase shift. The complex pole frequency  $\omega_o$  and  $Q$  are respectively indicated by:

$$\omega_o = \sqrt{\frac{g_{m2}g_{mL}}{C_L(C_{gd} + C_f + C_2)}} \quad (2.76)$$

$$Q = \sqrt{\frac{C_L(C_{gd} + C_f + C_2)}{g_{m2}g_{mL}}} \times \left[ \frac{g_{m2}g_{mL}}{(R_p + R_f)(g_{mL}(C_{gd} + C_f) - g_{m2}(C_c + C_L) + g_{mf}(C_f + C_2 + C_c))} \right] \quad (2.77)$$

Increasing  $g_{mL}$  and  $C_f$  can push complex poles toward higher frequencies, and thus decrease the  $Q$  value to improve the system stability. Thus, implementing  $C_f$  can minimize the unintended phase shift caused by complex poles under light to medium load conditions.

#### 2.4.5.3 Ultra-Light Load Current ( $g_{mL}$ Smaller than $g_{m1}$ and $g_{m2}$ )

Under ultra-light loads (i.e., below 1 mA) a small  $g_{mL}$  will lead to an unstable LDO system. As mentioned in the discussion on light to medium load conditions, non-dominant complex poles with a high  $Q$  factor reduce the PM. Consequently, a higher  $Q$  factor is derived with decreasing

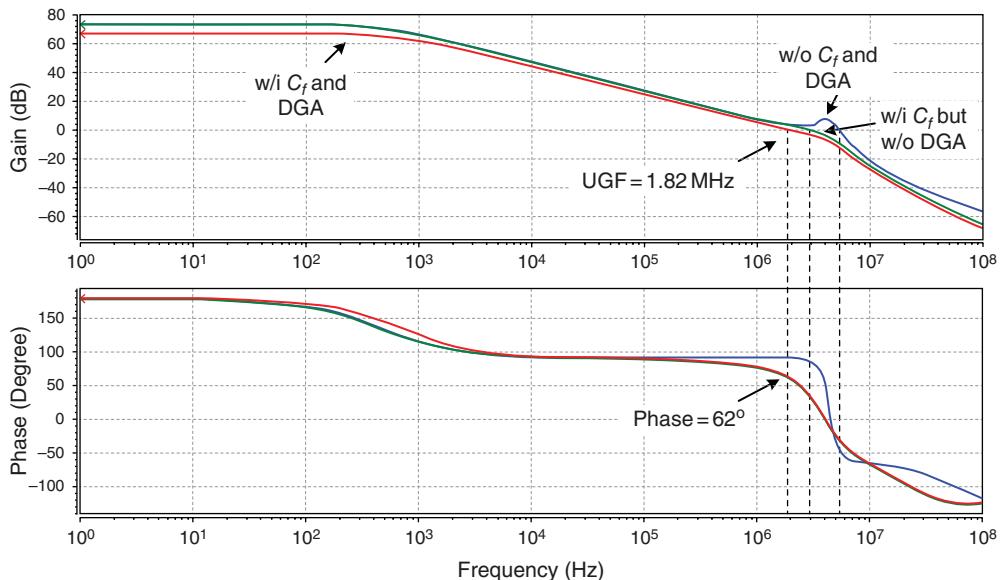
$g_{mL}$ . Non-dominant complex poles will move toward the RHP to deteriorate system stability. The boundary condition between stable and unstable operations can be expressed as:

$$\begin{aligned} g_{mL}(C_{gd} + C_f) - g_{m2}(C_c + C_L) + g_{mf}(C_f + C_2 + C_c) &> 0 \\ \Rightarrow g_{mL} &> \frac{g_{m2}(C_c + C_L) - g_{mf}(C_f + C_2 + C_c)}{(C_{gd} + C_f)} \end{aligned} \quad (2.78)$$

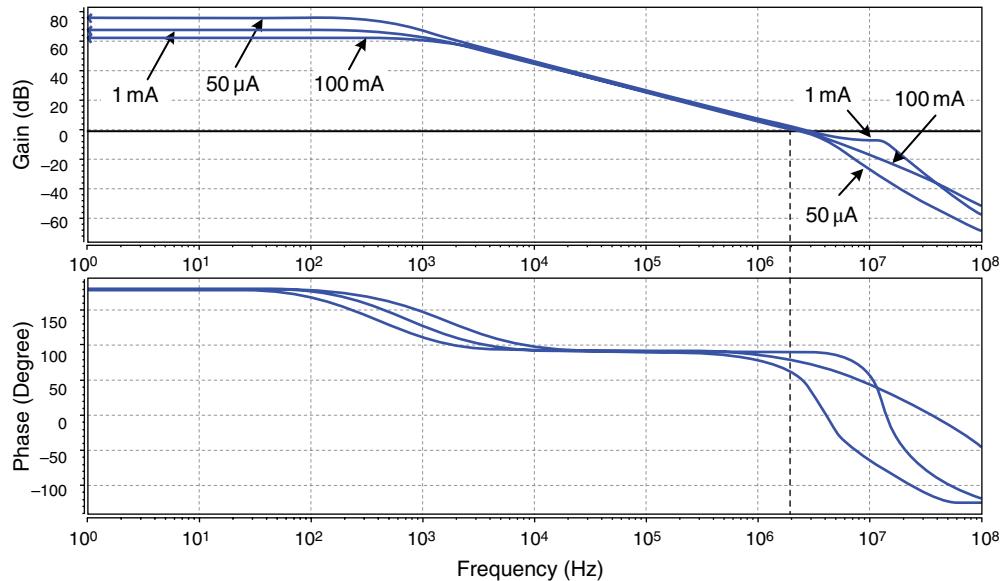
RHP poles can be eliminated when the  $s$  term of the second-order function in Eq. (2.70) is positive. Thus, a minimum value of  $g_{mL}$  must be contained to ensure stability. A minimum load current of the multi-stage LDO can be obtained to maintain a minimum  $g_{mL}$  value.

Nevertheless, non-dominant complex poles under ultra-light loads still affect the phase shift around the UGF. A load-dependent resistance  $R_p$ , proportional to the output loading current, is used to adjust the DC voltage gain in the DGA mechanism. Given the high voltage gain at ultra-light loads, decreasing the DC voltage gain and the UGF does not obviously influence the transient response. The DGA mechanism can minimize the effect caused by non-dominant complex poles, and thus ensure LDO stability.

Figure 2.46 shows the frequency response under an ultra-light load condition of  $50 \mu\text{A}$  with and without a flying capacitor  $C_f$  and the DGA mechanism. In the case without both  $C_f$  and the DGA mechanism, non-dominant complex poles appear near the UGF and result in a poor PM. With the implementation of  $C_f$ , the  $Q$  factor decreases but an inadequate PM remains. The DGA mechanism can slightly decrease the DC voltage gain and the UGF of the LDO to enhance the system PM. Thus, operation under an ultra-light load can be realized.



**Figure 2.46** Comparison of frequency responses under a  $50 \mu\text{A}$  load condition at different implementations



**Figure 2.47** Frequency responses under different output load conditions

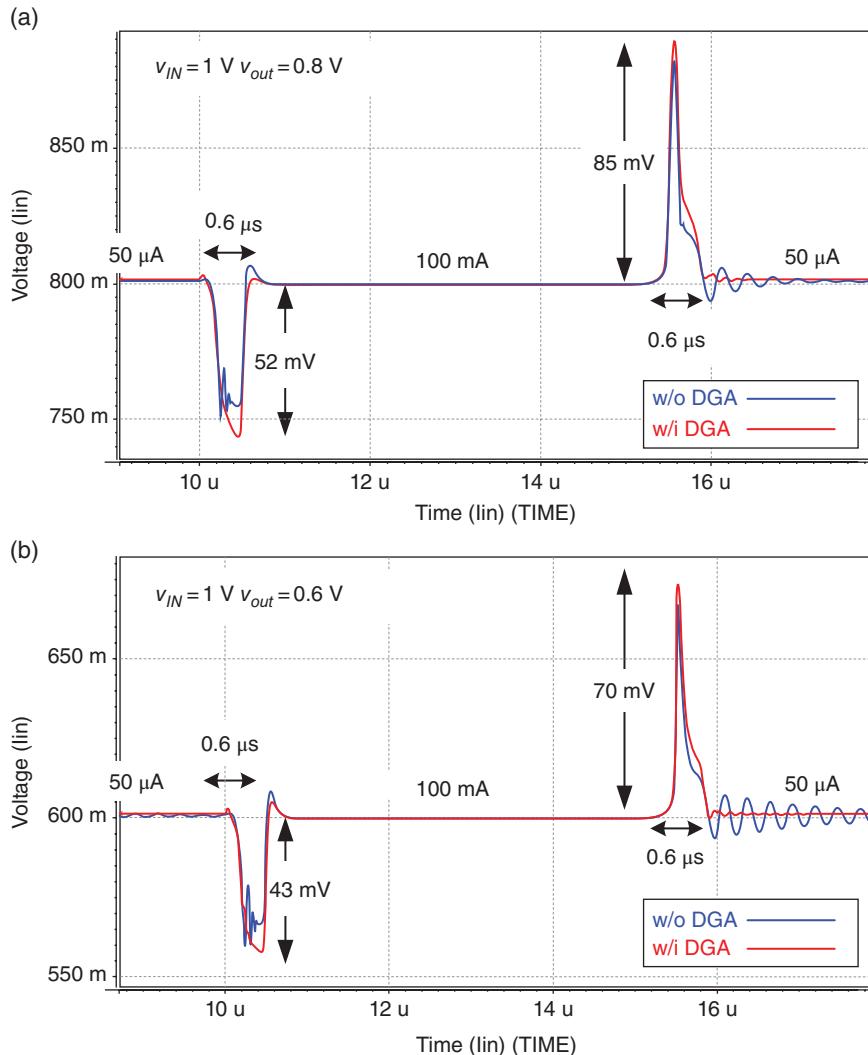
Figure 2.47 shows the frequency responses under different load conditions, ranging from  $50\text{ }\mu\text{A}$  to  $1\text{ mA}$ , and then to  $100\text{ mA}$ . With the DGA mechanism, which can dynamically adjust the DC voltage gain through load detection, the correct operating function is achieved under all load conditions.

Figure 2.48 shows the load transient response under an input voltage of  $1\text{ V}$ . In Figure 2.48(a), the output voltage is regulated to  $0.8\text{ V}$  with undershoot and overshoot voltages of approximately  $52$  and  $85\text{ mV}$ , respectively, when the load changes from  $50\text{ }\mu\text{A}$  to  $100\text{ mA}$ , and vice versa, within a load step of  $1\text{ }\mu\text{s}$ . The transient recovery time is approximately  $0.6\text{ }\mu\text{s}$ . By contrast, the transient response under an output voltage of  $0.6\text{ V}$  is presented in Figure 2.48(b). The undershoot and overshoot voltages are  $43$  and  $70\text{ mV}$ , respectively, with a load step ranging from  $50\text{ }\mu\text{A}$  to  $100\text{ mA}$ , and vice versa. The transient recovery time is approximately  $0.6\text{ }\mu\text{s}$ .

## 2.5 Design Guidelines for LDO Regulators

In this section of the book we provide typical guidelines for designing LDO regulators. The crucial design parameters that should be considered carefully before implementing a circuit are as follows:

- reading the specifications carefully
- load considerations
- output capacitor considerations
- on-chip capacitor considerations
- MOSFET-cap considerations
- system compensation considerations



**Figure 2.48** Load transient responses under  $50 \mu\text{A}$  to  $100 \text{ mA}$ , and vice versa. (a)  $V_{IN}=1 \text{ V}$ ,  $V_{OUT}=0.8 \text{ V}$ . (b)  $V_{IN}=1 \text{ V}$ ,  $V_{OUT}=0.6 \text{ V}$

- voltage range
- power MOSFET size estimation.

Before starting, the specifications should be read carefully. Compensation methods and techniques have both advantages and limitations, that is, the actual design exhibits trade-off with performance. Consequently, some important conditions provided in the specifications can help designers determine an adequate structure.

For example, load considerations include the desired driving capability and the load range. The driving capability suggests that designers should provide a wide bandwidth, a large SR, or

a large output capacitance to sustain  $V_{OUT}$  regulation during instances of changing loads. To satisfy the load range requirement, a designer should be careful with the maximum/minimum load limitation when using dominant-pole compensation or a *C-free* structure. In some applications, such as power for PA, the required large capacitance with nano- to micro-farads at the node of the supply voltage is unavoidable. Such a large capacitance can provide low frequency. For the desired gain, PM, and UGF, a pole can obstruct frequency response compensation regardless of whether dominant-pole compensation or a *C-free* structure is applied. By contrast, on-chip capacitances are utilized for the desired poles or zeros to provide adequate frequency response. In this case, the capacitance value should be determined carefully when considering the cost of the silicon area. On-chip capacitance can be realized using different types of device, such as poly–insulator–poly (PIP), metal–insulator–metal (MIM), or MOSFET-capacitance. In particular, the cross voltage can directly vary the capacitance when MOSFET-capacitance is used. Thus, the designer should ensure that cross voltages are sufficiently large under all conditions with varying loads, input voltages, and output voltages. In general, the specifications of load consideration and output capacitance loading provide sufficient information for the designer to plan the compensation strategy. Meanwhile, the operating ranges of the input or output voltage are related to the frequency response and stability because different cross voltages can vary the gain, small signal resistance, and operating region. Once a power transistor operates in the linear and saturation regions at different input/output voltages, the gain and small signal resistance of the transistor significantly change and seriously influence the frequency response. In this case, compensation should be adjusted adequately for different situations. Finally, the size of the power transistor is estimated. The desired dropout voltage and driving capability can basically determine the minimum size of a power transistor. Hence, the designed size should be larger than the minimum size. By contrast, the maximum size of a power transistor should be limited not only because of concerns about using unnecessary silicon area, but also because an extremely large power transistor can degrade the DC operation of the EA under light loads. For example, to drive a large p-type power transistor under a light load, the driving voltage level should be extremely high. This voltage may be the upper voltage headroom of the last EA stage, and thus the gain is decreased drastically. Consequently, a power transistor with adequate size should be designed.

### 2.5.1 Simulation Tips and Analyses

After circuit implementation, performance can be checked through the following simulations. AC analysis is used to analyze the frequency response, including gain, PM, and UGF. Moreover, checking the slew rate in case of a large signal operation is also important. DC analysis is employed to check the operating region of each MOSFET, and DC specifications such as line and load regulations. Transient analysis is utilized to check dynamic performance during the transient period and power-on sequence. Planning the power-on sequence with an adequate soft start is important to ensure safe operation, without any damage caused by overcurrent, overvoltage, and so on, before quiescent operation is established.

Finally, full-chip simulation should be carefully executed. In this step, designers should consider possible parasitic components existing on the silicon and the PCB. Such components include the capacitance of the back-end circuit; on-resistance through the power delivery path; and R, L, and C in bond wires, among others. Moreover, designers should consider process,

voltage, and temperature (PVT) variations. However, considering numerous factors draws from the simulation time. As previously stated, appropriate design and simulation considerations can effectively guarantee the yield rate after fabrication:

- AC analysis
- DC analysis
- transient analysis
- power-on sequence and soft-start design
- full-chip simulation
- consideration of PVT variations.

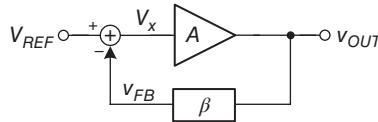
Designers should know how to utilize simulation tools to analyze circuit performance, as discussed in the preceding paragraphs. These tools can also be used to verify the original functions and yield rate after fabrication. Therefore, the authors strongly encourage designers to anticipate all possible situations that chips may encounter in practice. Designers should first learn to establish simulation environments. Understanding design issues and practical system operating environments is helpful for this purpose. However, checking all possible considerations is impossible because such a process not only increases the design complexity but also requires considerable simulation time. Therefore, the trade-off between robust simulation and efficient design procedure should be balanced carefully.

### 2.5.2 Technique for Breaking the Loop in AC Analysis Simulation

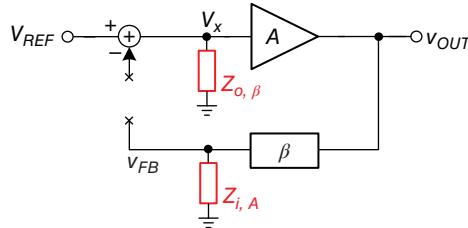
An open-loop structure without a feedback path is applied to reduce complexity or alleviate the BW constraint, while the regulated voltage is varied significantly because of the loading effect. To guarantee the quality of the regulated voltage, a closed-loop structure is used as the basis to design power regulators. The stability of the closed-loop structure should be designed carefully; such stability is generally confirmed by the gain margin and PM. However, a closed-loop structure experiences difficulties in AC simulation because the processes of injecting the stimulus and obtaining the output signal should be determined. The characteristics of a closed-loop system can be obtained from an open-loop analysis whose bode plot reflects its corresponding gain margin and PM. That is, the analysis is simplified by conducting an open-loop analysis, which is achieved by breaking the loop. Thus, determining how to break the loop adequately is important to maintain simulation accuracy without being affected by the loading effect. Two methods are recommended for this purpose, and these are introduced as follows.

Figure 2.49 illustrates a typical circuit block that represents a power converter with a feedback loop. Block  $A$  provides the open-loop gain, whereas block  $\beta$  provides the path to feed the output voltage  $V_{OUT}$ , which enables the reference voltage  $V_{REF}$  to regulate the output voltage.

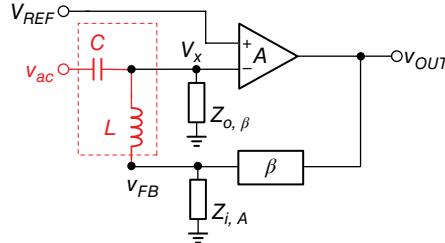
When breaking the loop, the input and output impedances should be considered at the broken node to build an accurate model. In Figure 2.50, the output impedance  $Z_{o,\beta}$  of block  $\beta$  is added to the front end of the breaking node while the input impedance  $Z_{i,A}$  of block  $A$  is added to the back end of the breaking node. In Figure 2.51, the test AC signal source  $v_{ac}$ , a test inductor  $L$ , and a test capacitor  $C$  are used to extract the transfer function during simulations. The test inductor  $L$  conducts DC information to maintain the DC operating voltage in a steady state. Meanwhile,  $L$  blocks AC information, and thus the circuit forms as an open loop in view of the small signal aspect. By contrast, the test capacitor  $C$  conducts only the test AC signal



**Figure 2.49** Model of a typical converter circuit



**Figure 2.50** Basic principle for breaking a feedback loop

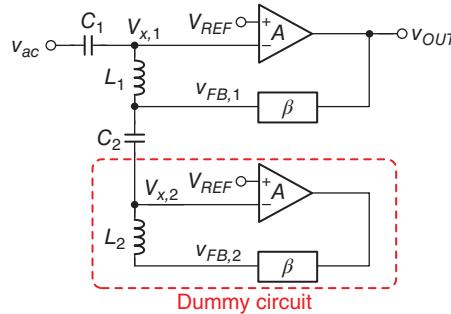


**Figure 2.51** General method for breaking a feedback loop

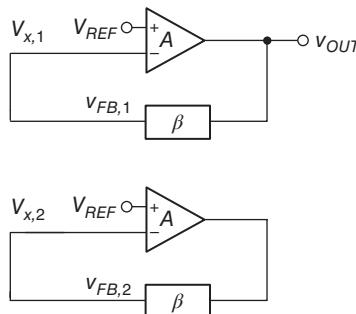
$v_{ac}$ , but blocks any DC information. Consequently, the DC voltage of  $V_x$  will not be influenced by the AC signal source. Given that  $L$  and  $C$  are expected to be ideal components with infinite values, their values should be high, on the order of several megas. For example,  $L$  can be 100 MH and  $C$  can be 100 MF. The transfer function can be obtained by observing the value of  $v_{FB}/v_{ac}$ .

However, deriving accurate input/output impedance values is not easy or convenient. As such, one possible method to break a loop is to select a high impedance node as the breaking node to reduce the complexity of the analysis. For example, a MOSFET gate is typically chosen as the breaking node because of its high impedance. Consequently, the input impedance  $Z_{i,A}$  can be disregarded. Moreover, the output impedance  $Z_{o,\beta}$  can also be ignored. The AC and DC components at  $V_x$  can be determined directly by  $v_{ac}$  and  $v_{FB}$  through  $C$  and  $L$ , respectively, to derive the transfer function. This procedure does not provide an exact solution to the transfer function, because the assumption is high impedance at the gate of the power MOSFET. Furthermore, designers may experience a situation in which the high impedance node is difficult to find in the loop. When the breaking node is not a high impedance node, the corresponding impedance  $Z_{i,A}$  should be considered; however, this action increases the complexity of analysis.

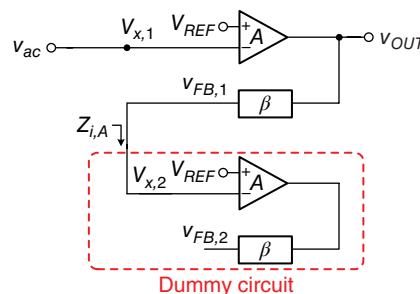
Figure 2.52 presents another approach to establish an accurate model related to the original circuit. Test capacitors,  $C_1$  and  $C_2$ , and test inductors,  $L_1$  and  $L_2$ , provide adequate AC and DC paths for the same purpose mentioned earlier. The values of these test passive components are set on the order of several megas. When considering the DC domain, the DC operating voltage



**Figure 2.52** Accurate model for breaking a feedback loop



**Figure 2.53** DC operating points correctly established



**Figure 2.54** In the AC domain, the circuit topology reflects an exact solution to the transfer function without being affected by the selection of the breaking node

of each circuit block can be established as shown in Figure 2.53, because of the short paths provided by the inductors  $L_1$  and  $L_2$ , and the open paths provided by  $C_1$  and  $C_2$ . By contrast, when considering the AC domain, Figure 2.54 shows that the capacitors  $C_1$  and  $C_2$  are shorter and the inductors  $L_1$  and  $L_2$  are opened, and thus the circuit block exhibits one open loop and the dummy circuit is utilized to provide  $Z_{i,A}$ . Consequently, the AC and DC characteristics are confirmed, and thus this approach can reflect an accurate model without being affected by the selection of the breaking node. Similarly, the transfer function can be obtained from the value of  $v_{FB,1}/v_{ac}$ .

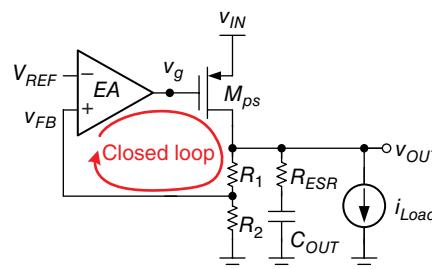
### 2.5.3 Example of the Simulation Results of the LDO Regulator with Dominant-Pole Compensation

In this subsection, we provide basic simulation methods to verify the performance and function of the LDO regulator whose specifications are listed in Table 2.3. These will guide the reader to perform the simulations step by step. The verified performances include stability, dropout voltage, line regulation, load regulation, overshoot/undershoot voltage, and settling time during transient response.

In AC analysis, Figure 2.55 illustrates the closed loop in the LDO regulator with dominant-pole compensation. The first step is to identify the possible location of the breaking node in the entire LDO regulator. In general, the input impedance of the EA is assumed to be infinitely large because the first stage is implemented by a CS amplifier. Thus, Figure 2.56(a) shows that the breaking node is selected on the path from  $V_{FB}$  to the non-inverting terminal of the EA. Figure 2.56(b) shows that  $L_{ideal}$  and  $C_{ideal}$  are added to provide the paths for conducting DC and AC signals, respectively, to determine the quiescent operating points and the transfer function, respectively. The conducting path for DC signals can maintain the function of DC operation with adequate values of  $V_{IN}$ ,  $V_{OUT}$ ,  $V_{REF}$ , and  $I_{Load}$ . Based on DC operation, the conducting path for AC signals can determine the frequency response. Readers may believe that this process is an alternative method to connect DC voltage sources directly to the breaking node as quiescent operating points. However, a high loop gain in the LDO regulator will result in a severe error if a slight error caused by the deviation of quiescent operating points occurs.

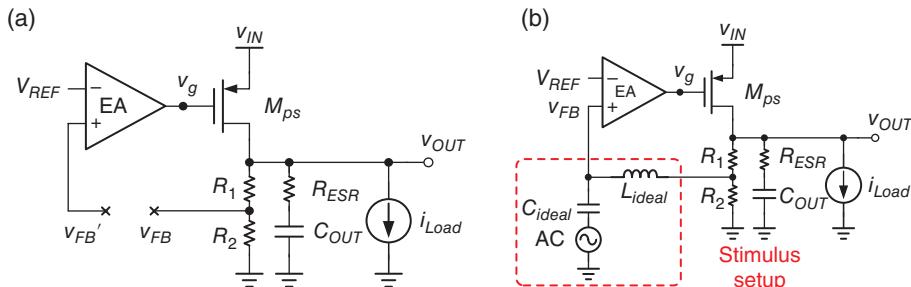
**Table 2.3** Specifications of the LDO regulator

| Parameter                               | Value                                | Unit          |
|---|--------------------------------------|---------------|
| Compensation                            | Dominant-pole compensation           |               |
| Technology                              | 0.25 $\mu\text{m}$ CMOS (5 V device) |               |
| Input voltage ( $V_{IN}$ )              | 3.0–4.5                              | V             |
| Output voltage ( $V_{OUT}$ )            | 2.7                                  | V             |
| Reference voltage ( $V_{REF}$ )         | 1.2                                  | V             |
| Load current ( $I_{Load}$ )             | 1–100                                | mA            |
| Output capacitor ( $C_{OUT}$ )          | 4.7                                  | $\mu\text{F}$ |
| ESR of output capacitance ( $R_{ESR}$ ) | 5                                    | $\Omega$      |

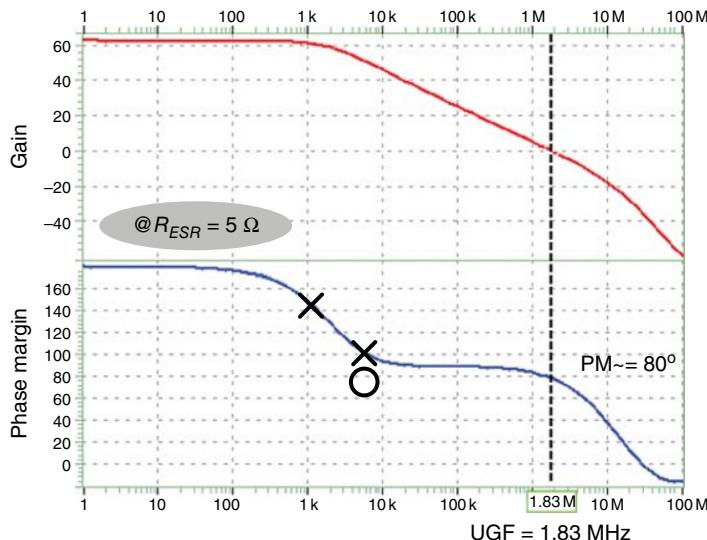


**Figure 2.55** Illustration of the LDO regulator for AC analysis

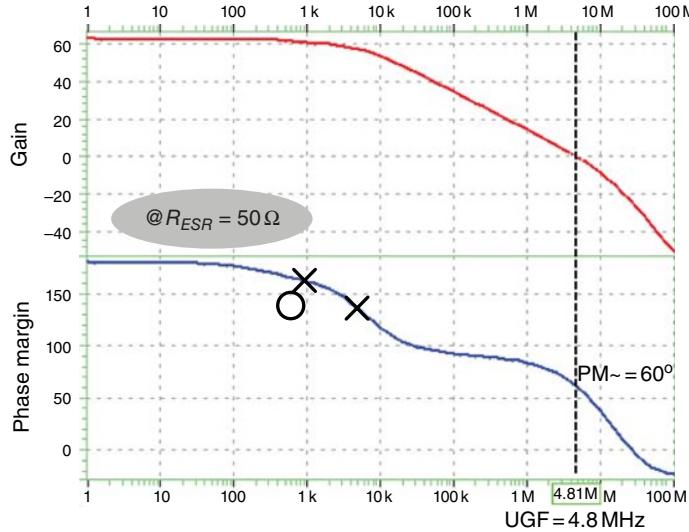
Given the simple single-stage design, the poles and zeros of the EA, which are located at high frequencies, can be disregarded. Therefore, two poles,  $P_1$  and  $P_2$ , which are located at  $V_{OUT}$  and  $v_g$ , respectively, are considered for stability analysis. Moreover, ESR zero  $Z_1$ , which is contributed by  $R_{ESR}$  and  $C_{OUT}$  at  $V_{OUT}$ , can have a phase boost of  $90^\circ$ . If dominant-pole compensation is used, Figure 2.57 shows the frequency response when  $V_{IN}$ ,  $V_{OUT}$ , and  $I_{Load}$  are 3 V, 2.8 V, and 100 mA, respectively.  $P_1$  is located at approximately 1 kHz and zero  $Z_1$  is designed at approximately 4 kHz to cancel the effect of  $P_2$ . Compared with those in Figure 2.57, the frequency responses in Figures 2.58 and 2.59 show the different locations of zero  $Z_1$  and provide different performances. In Figure 2.58, the UGF and PM increase and decrease, respectively, because a large  $R_{ESR}$  ( $50 \Omega$ ) causes  $Z_1$  to be located at lower frequencies compared with  $P_2$ . In Figure 2.59, the UGF and PM decrease and increase, respectively, because a smaller  $R_{ESR}$



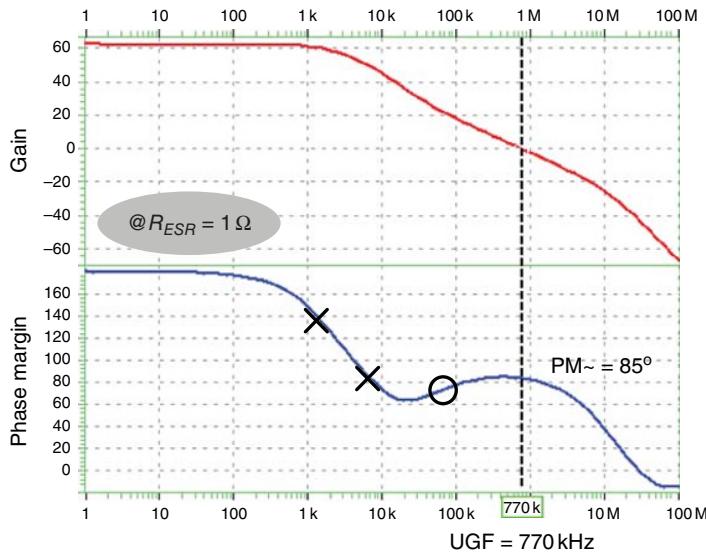
**Figure 2.56** (a) Conceptual approach to break the loop at the high impedance node. (b) Setup of the stimulus



**Figure 2.57** Frequency response with  $R_{ESR} = 5 \Omega$  and  $I_{Load} = 100 \text{ mA}$



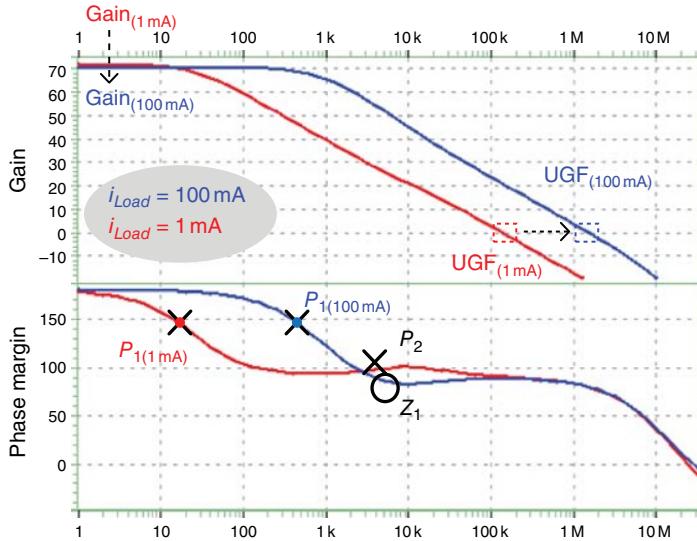
**Figure 2.58** Frequency response with  $R_{ESR} = 50 \Omega$  and  $I_{Load} = 100 \text{ mA}$



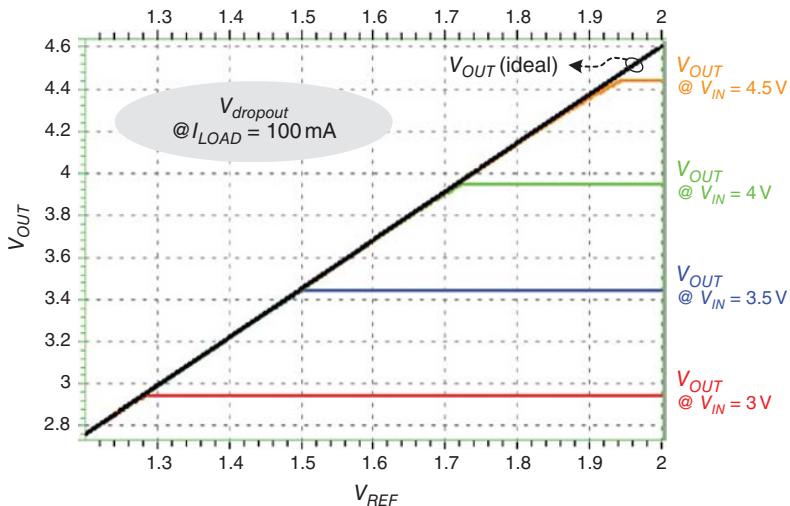
**Figure 2.59** Frequency response with  $R_{ESR} = 1 \Omega$  and  $I_{Load} = 100 \text{ mA}$

( $1 \Omega$ ) causes zero  $Z_1$  to be located at higher frequencies compared with  $P_2$ . Consequently,  $R_{ESR} = 1 \Omega$  can provide adequate frequency compensation.

In Figure 2.60 the frequency response is verified under different loading conditions, including 1 and 100 mA. A decreasing loading condition leads to higher gain ( $\text{Gain}_{(1 \text{ mA})} > \text{Gain}_{(100 \text{ mA})}$ ), lower frequency of  $P_1$  ( $P_{1(1 \text{ mA})} > P_{1(100 \text{ mA})}$ ), and smaller UGF ( $\text{UGF}_{(1 \text{ mA})} < \text{UGF}_{(100 \text{ mA})}$ ). Moreover, when checking the simulation conditions, a complete verification should include



**Figure 2.60** Comparison of frequency responses under  $I_{Load} = 1 \text{ mA}$  and  $I_{Load} = 100 \text{ mA}$



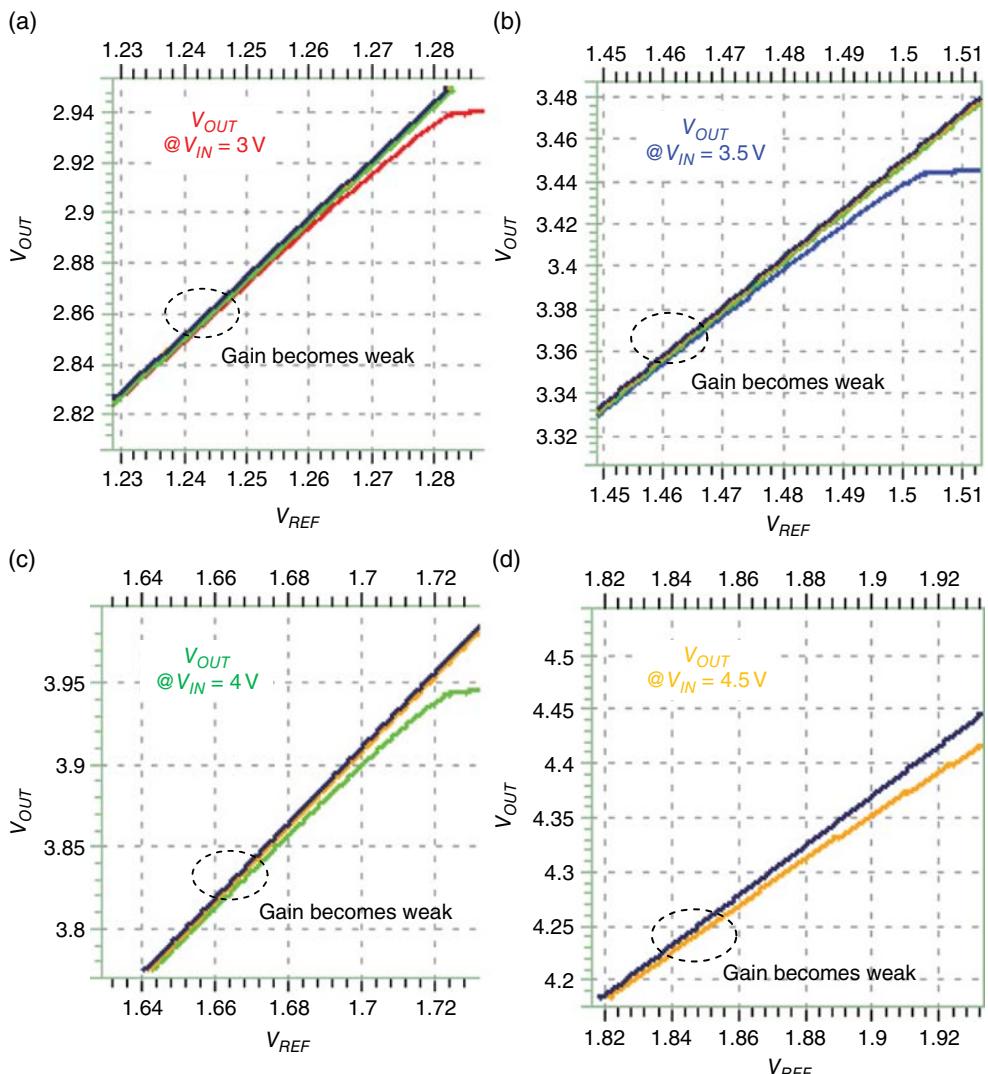
**Figure 2.61** Dropout voltage with different  $V_{IN}$  values ranging from 3 to 4.5 V

all combinations of different  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{Load}$ , temperature, and so on, to ensure system stability even under the worst operating conditions (Figure 2.60).

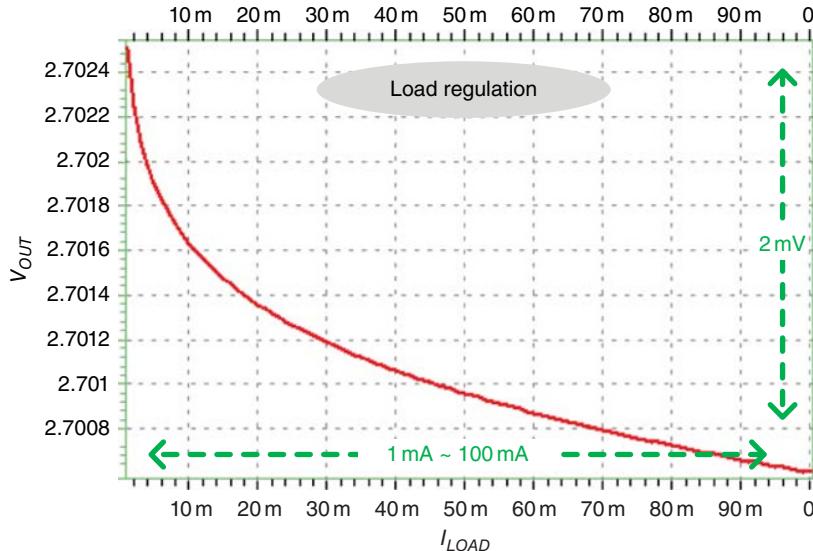
DC analysis can verify the dropout voltage, load regulation, and line regulation. First, the dropout voltage  $V_{dropout}$  is observed if  $V_{IN}$  and  $V_{OUT}$  increase continuously, as shown in Figure 2.61. If  $I_{Load}$  is set to its maximum value of 100 mA,  $V_{OUT}$  is observed in case of increasing  $V_{IN}$  and  $V_{REF}$ . The ideal output value  $V_{OUT(ideal)}$  can track the increasing trend of  $V_{REF}$

because of the negative feedback control. When  $V_{IN}$  is set to 3 V, increasing  $V_{REF}$  causes  $V_{OUT}$  to also increase. As shown in Figure 2.62(a), where  $V_{IN}$  is set to 3 V, the loop gain becomes weak, and thus the dropout voltage can be determined as approximately 140 mV when the curve of  $V_{OUT}$  deviates from  $V_{OUT(ideal)}$ . Similarly, Figure 2.62(b)–(d) shows  $V_{dropout}$  when  $V_{IN}$  is 3.5, 4, and 4.5 V, respectively.

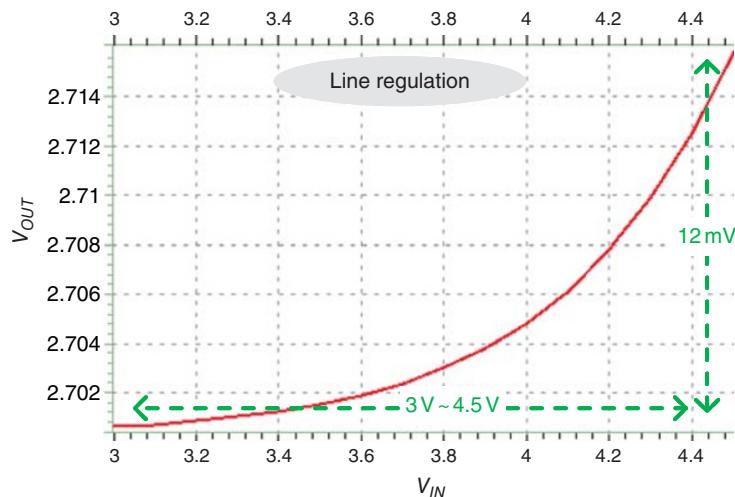
Figures 2.63 and 2.64 show the load regulation and the line regulation, respectively. In Figure 2.63, the load regulation is verified when  $V_{IN}$  is 3 V,  $V_{OUT}$  is 2.7 V, and  $I_{Load}$  ranges from 1 to 100 mA. The variation at  $V_{OUT}$  is 2 mV, which indicates that the performance of load regulation is approximately 20.2 mV/A. In Figure 2.64,  $I_{Load}$  is set to its maximum condition of



**Figure 2.62** Dropout voltage with (a)  $V_{IN} = 3\text{ V}$ , (b)  $V_{IN} = 3.5\text{ V}$ , (c)  $V_{IN} = 4\text{ V}$ , and (d)  $V_{IN} = 4.5\text{ V}$



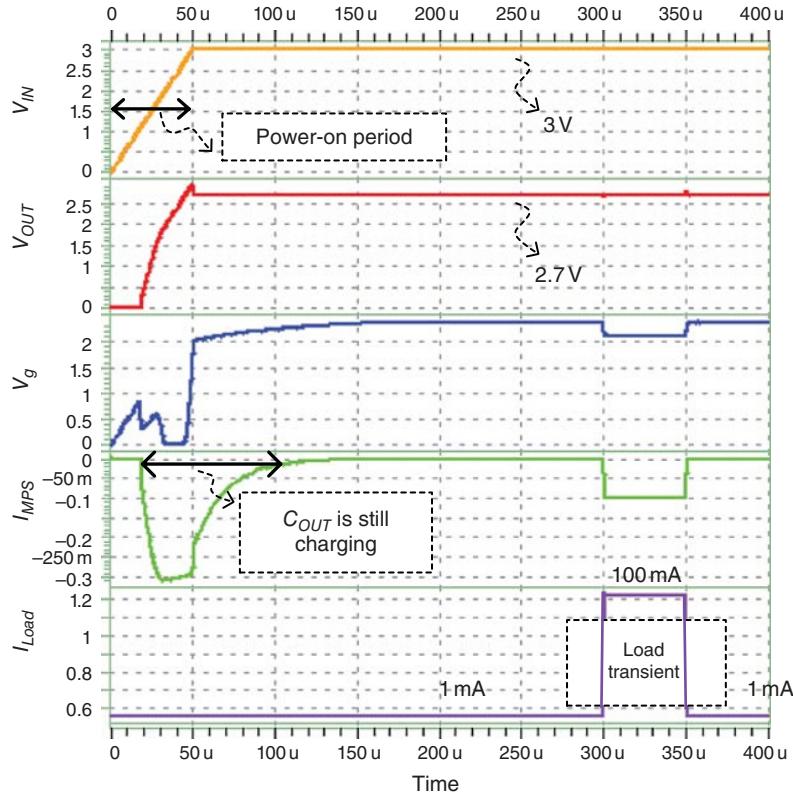
**Figure 2.63** Load regulation when  $I_{Load}$  ranges from 1 to 100 mA



**Figure 2.64** Line regulation when  $V_{IN}$  ranges from 3 to 4.5 V

100 mA, because this condition will lead to the worst loop-gain case. Line regulation is verified when  $V_{IN}$  ranges from 3 to 4.5 V,  $V_{OUT}$  is 2.7 V, and  $I_{Load}$  is 100 mA. The variation at  $V_{OUT}$  is 12 mV, which indicates that the performance of load regulation is approximately 8 mV/V.

Figure 2.65 shows the simulation results of transient response. In the beginning,  $V_{IN}$  is set to increase from 0 to 3 V within 50  $\mu$ s, which emulates the power-on situation in real cases. After the power-on period of 50  $\mu$ s, the system has not yet settled down because  $V_g$  and  $I_{MPS}$  still have varying values, although  $V_{OUT}$  is regulated at 2.7 V.  $V_{OUT}$  consists of the cross voltages of  $C_{OUT}$  and  $R_{ESR}$ . This variable indicates that  $C_{OUT}$  has not yet been charged to the desired voltage of

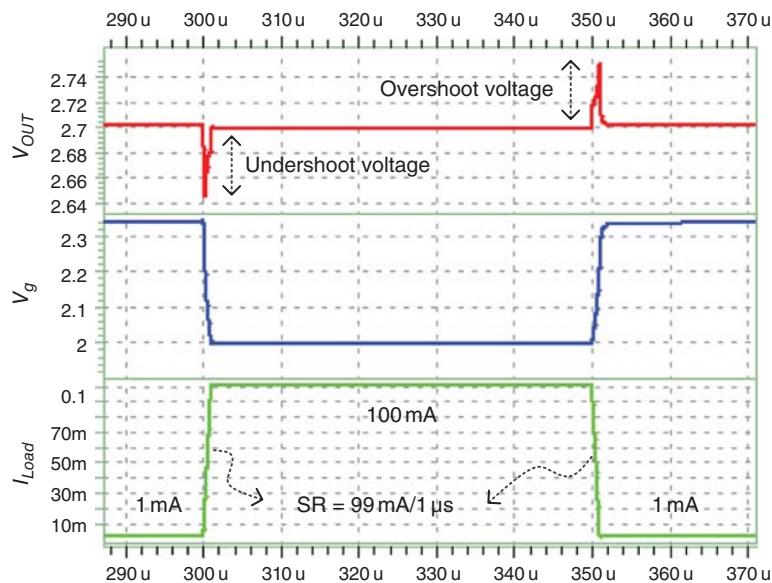


**Figure 2.65** Transient response

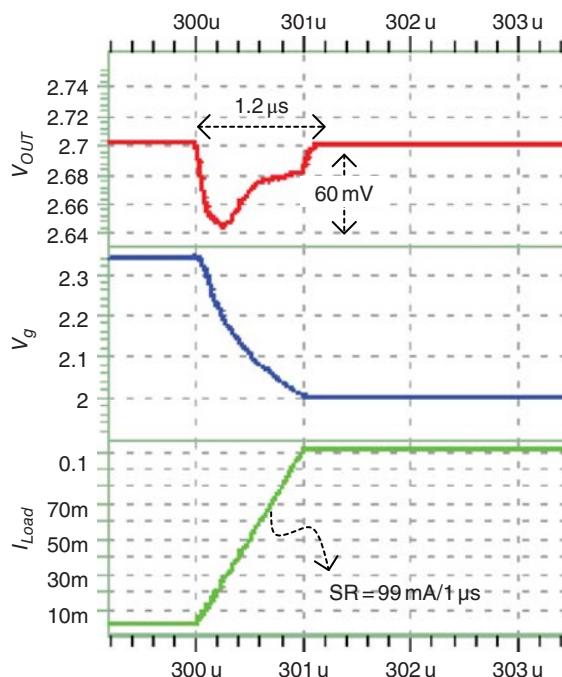
2.7 V. To analyze the load transient response, designers should avoid setting any loading change during this unstable period.

During the transient response period, the loading current changes from 1 to 100 mA and from 100 to 1 mA at 300 and 350  $\mu$ s, respectively. The slew rate of the loading current is 1  $\mu$ s. Figure 2.66 provides detailed zoomed-in images of waveforms that occur during the load transient period. When the loading current changes from 1 to 100 mA, the EA controls  $V_g$  to adjust the corresponding driving capability of the power P-MOSFET. In particular,  $V_g$  experiences a sudden voltage change from 2.34 to 2 V, which incurs a large signal variation and indicates that the large-signal characteristics of the EA should be carefully designed. The slew rate of the EA always affects the transient response, even if the PM is adequate. Figures 2.67 and 2.68 show the voltage undershoot, voltage overshoot, and settling time. Moreover, the performance of load regulation can be verified from  $V_{OUT}$  in a steady state under different loading current conditions, as shown in Figure 2.69.

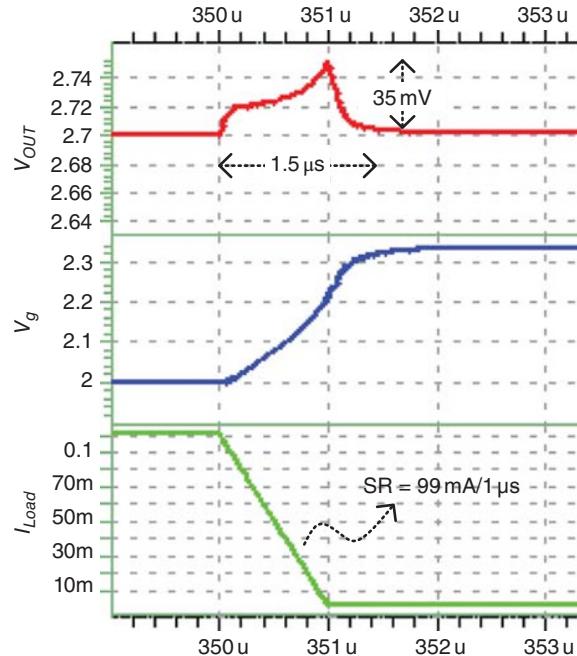
If the load transient performance cannot satisfy the specifications, designers can modify the design or the compensation to recheck the simulation results. Notably, regardless of whether AC analysis or transient response analysis is checked first, the other should always be checked after. The cross reference between AC analysis and transient response analysis should be consistent.



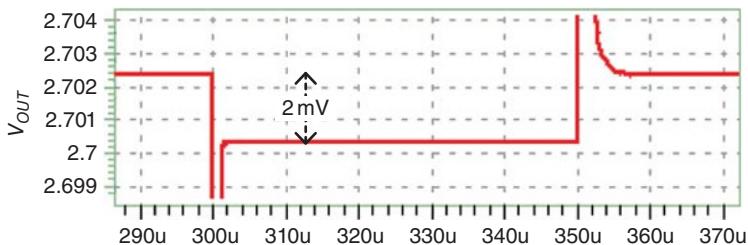
**Figure 2.66** Transient response when  $I_{Load}$  changes from 1 to 100 mA, and vice versa



**Figure 2.67** Load transient from light to heavy loads



**Figure 2.68** Load transient from heavy to light loads



**Figure 2.69** Load regulation when  $I_{Load}$  changes from 1 to 100 mA, and vice versa

## 2.6 Digital-LDO (D-LDO) Design

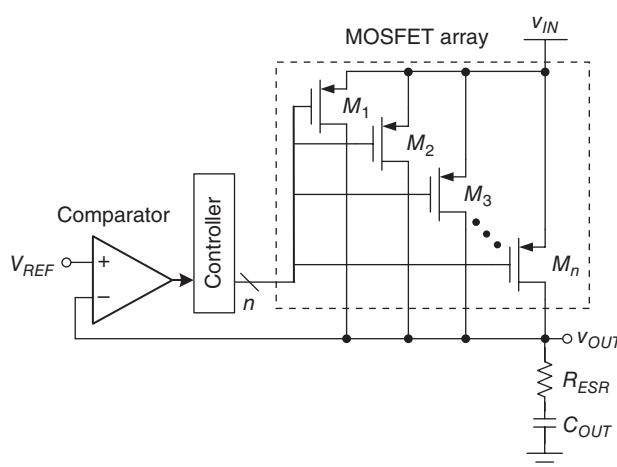
To obtain a high PCE, several approaches have been developed to maintain stability and consume a low quiescent current, even under no-load conditions. However, a low quiescent current induces difficulty in performance enhancement for most LDO regulators. Moreover, for adequate PM and transient response, a structure becomes more complex and the design cost increases correspondingly. Thus, D-LDO regulators have been proposed; the controllers of these regulators are implemented by digital circuits, to turn on/off the power MOSFET array fully [8–10]. Considering their digital implementation, D-LDO regulators can feature fast transit response, a simplified compensation network, and they can work under ultra-low supply voltages. We first introduce the concept of D-LDO regulators and then provide an advanced controller to improve the performance further.

### 2.6.1 Basic D-LDO

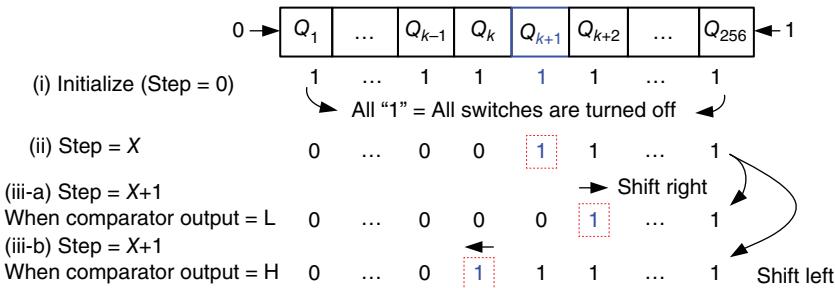
Figure 2.70 illustrates the basic structure of a D-LDO regulator, which consists of a power MOSFET array, a comparator, and a digital controller. In the design of the power MOSFET array, a large power MOSFET is divided into several sub-MOSFET units (SMUs). Each unit is driven by an  $n$ -bit digital control signal from the digital controller. Instead of a complex and noise-sensitive analog amplifier, a comparator is used to monitor the output voltage  $V_{OUT}$  and compare it with the reference voltage  $V_{REF}$ . That is, the logic high or low of the comparator output signal is fed into the digital controller to determine the number of turning-on SMUs. Different numbers of turning-on SMUs can be regarded as several on-resistances that are parallel to an equivalent on-resistance of the power MOSFET. Consequently, different driving capabilities that correspond to various loading current conditions can be adjusted. For example, under heavy loading current conditions, many SMUs are turned on to reduce the equivalent on-resistance and obtain high driving capability.

In general, a simple digital controller can be realized by an up/down counter or a shift register that is controlled by a one-bit compact or output. Moreover, an additional clock signal can be used to synchronize all control signals. The size of the SMUs in the MOSFET array can be designed in binary-code form. As shown in Figure 2.71 [8], the digital controller can be realized by a shift register, wherein the SMUs in the MOSFET array are designed with uniform size.

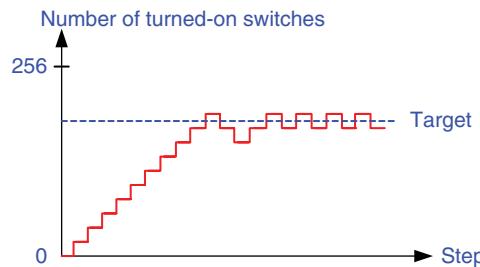
Compared with the power MOSFET that is controlled by an analog amplifier, a digital control method fully turns on/off each SMU in the power MOSFET array. From a digital perspective, fully turning a system on and off indicates high noise immunity. In a steady state, the number of turning-on power MOSFETs indicates the loading current condition. The shift register will have a dynamic equilibrium under a bistable condition that oscillates between two coding words. That is, the number of turning-on SMUs increases and decreases back and forth if equilibrium is established. However, the back-and-forth operation incurs voltage ripples, as shown in Figure 2.72; these ripples are similar to the switching voltage ripples in SWRs. Unlike



**Figure 2.70** Basic structure of a D-LDO regulator



**Figure 2.71** Shift register used to control on/off switching of the power MOSFET array



**Figure 2.72** Up/down counting control method in D-LDO regulators causes undesired voltage ripples

A-LDO regulators, the undesired voltage ripples will degrade the advantages of the ripple-free characteristic of LDO regulators. The resolution of a switching MOSFET array determines how large a voltage ripple is. A high resolution results in a low output ripple. Furthermore, the transient response time is determined by the frequency of a clock signal and the resolution of the switching MOSFET array. A high frequency results in a fast response and a short recovery time. Nevertheless, the operating frequency cannot be increased without limitation because a high-frequency operation will result in insubstantial power consumption, thus worsening the PCE. That is, the bandwidth of D-LDO regulators is determined by the operating frequency and the resolution of the power MOSFET array when the digital control method is used.

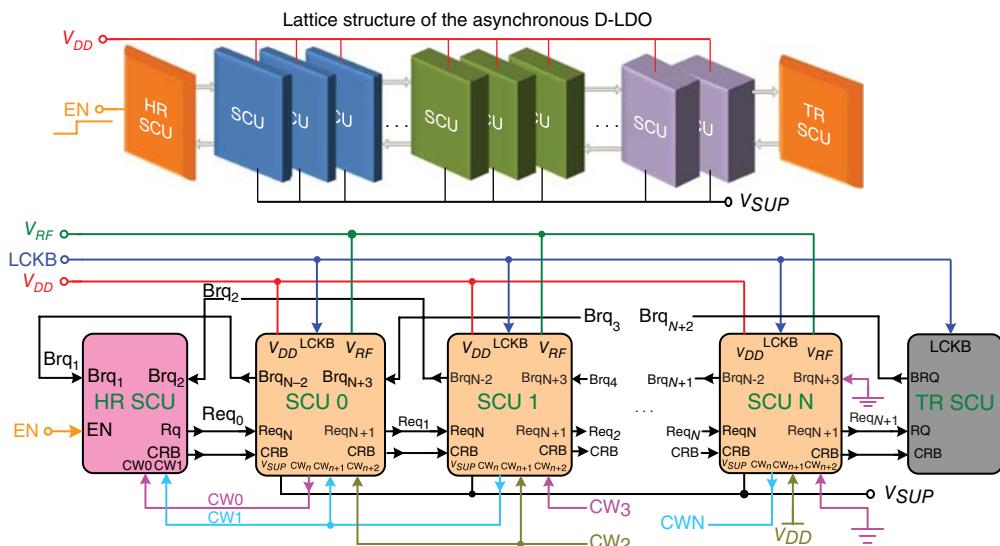
A fast transient response can be achieved more easily in the digital control method than in the analog control method if the operating frequency is simply increased without considering the PCE. Moreover, the digital control method has another advantage, that is, only the pole at the output should be considered because full-swing signals can push poles and zeros to high frequencies. The system can be simplified into a single-pole system, alleviating the constraint of the loading current range, particularly for the minimum light load requirement in the *C-free* LDO regulator.

Given the advantages of fast transient and wide load range operation, D-LDO regulators are more suitable for DVS-based applications. Moreover, a wide operating voltage ranges from the device threshold voltage  $V_{th}$  to nearly the highest supply voltage (even if only the minimum biasing current is used to ensure voltage regulation). When considering an advanced nanometer

process, D-LDO regulators are also among the candidates for point-of-load (POL) power converters. The following subsections introduce several advanced control methods for D-LDO regulators. For example, the lattice asynchronous self-timed control (LASC) technique is introduced to effectively reduce the power consumption required for synchronous clock control and output voltage caused by a bi-stable operation. Expanding the concept of the DVS technique from the task layer to the instruction layer, the instruction cycle-based dynamic voltage scaling (iDVS) technique is introduced to achieve the advantage of effective power saving. Considerable power can be saved at both the architectural and the circuit levels if the iDVS technique is used.

## 2.6.2 D-LDO with Lattice Asynchronous Self-Timed Control

A basic D-LDO regulator synchronously adjusts the driving capability with a predefined reference clock. Although a fast transient response and low-voltage operation can be obtained with D-LDO regulators compared with A-LDO regulators, the power consumption remains constrained by the synchronous clock. To improve the performance, a LASC control for *C-free* D-LDO regulators, as illustrated in Figure 2.73, has been developed without any clock signal because of its asynchronous control. The operation of the LASC is similar to that of a clock-free bidirectional shift register that determines the activity of each SMU. Without a synchronous clock, asynchronous control realizes the hand-shaking operation between adjacent SCUs. Therefore, the trade-off between the PCE and the transient response speed can be compromised. That is, in case of a load change, the equivalent clock



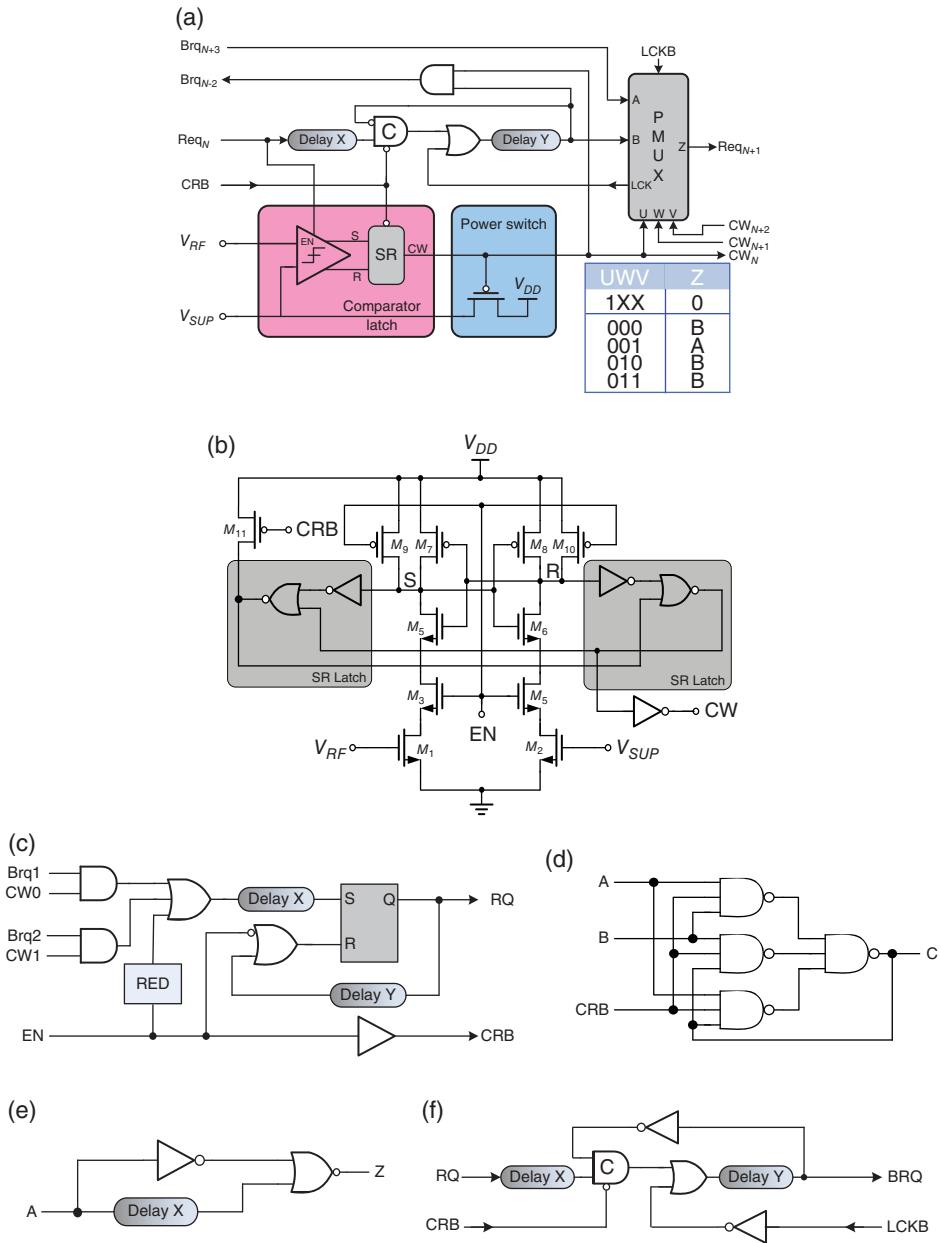
**Figure 2.73** Implementation of an asynchronous D-LDO regulator with the LASC technique [11]

frequency is effectively increased to achieve a fast transient response. By contrast, the equivalent clock frequency is automatically decreased for energy/power saving in standby mode. This condition indicates that the D-LDO regulator with the asynchronous control technique can simultaneously exhibit the advantages of high PCE and fast transient response.

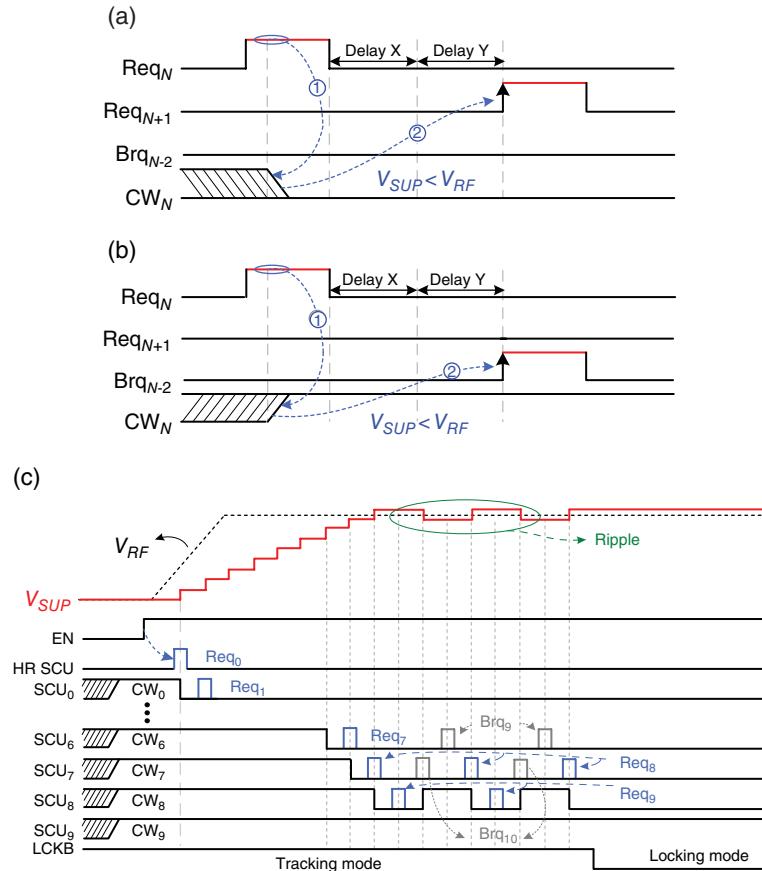
A driven source is an event, and thus the problems of clock skew and synchronous surging current never occur. Figure 2.74 shows that the LASC D-LDO regulator consists of an SCU, an SR-latch comparator, a heading reflector (HR), and a terminal reflector (TR). As shown in Figure 2.74(a), the SCU contains a Muller C-gate, an SR-latch comparator, a power switch, a path multiplexer, and control logics to modulate power switches to ensure the regulated output voltage  $V_{SUP}$ . In Figure 2.74(b), the SR-latch comparator is triggered by an active high enable signal EN, which is controlled by the forward request pulse of the previous stage. The dynamic comparator compares  $V_{SUP}$  with  $V_{RF}$  to generate signals  $CW_0-CW_N$  to turn on/off the corresponding power switch.

The path multiplexer determines the forward request signal  $Req_{n+1}$ , either from the prior stage or the later stage backward request signal  $Brq_{n+3}$  according to the results  $CW_n$ ,  $CW_{n+1}$ , and  $CW_{n+2}$ . The table in Figure 2.74(a) shows the overall operating principle of the SCU-based Muller C-gate self-timed control. As shown in Figure 2.74(c), HR ensures that all SCUs in the LASC D-LDO regulator will return to their initial states. HR also guarantees that power switches are turned off by setting the signal current-ripple based (CRB) to low when the EN signal is forced to be low. The Muller C-gate shown in Figure 2.74(d) is a basic component of asynchronous circuits. The behavior of an  $n$ -input Muller C-gate changes the output state to 3high if all inputs are high and to low if all inputs are low. Otherwise, the  $n$ -input Muller C-gate maintains the same output as that in the previous state. As shown in Figure 2.74(e), the rising edge detector (RED) circuit generates a single pulse to trigger the HR circuit to pump the first request pulse, and thus activate the LASC D-LDO regulator when EN changes from low to high. To address the boundary condition, the TR circuit, as depicted in Figure 2.74(f), helps the forward request signal reflected from the termination when  $V_{SUP}$  cannot acquire a sufficient power supply during the final SCU stage. Furthermore, HR prevents the backward request signal from disappearing when  $V_{SUP}$  derives an overcharge load during the first SCU stage.

Figure 2.75(a), (b) shows the timing diagram of a single SCU stage operation under different conditions that correspond to the circuit in Figure 2.74(a). When  $V_{SUP}$  is smaller than the reference voltage  $V_{RF}$  in an SCU stage that is triggered by the signal  $Req_n$  from the prior stage, the level-active SR-latch comparator outputs low-signal  $CW_n$  to turn on the power switch. Thus, the voltage for  $V_{SUP}$  can be increased to track  $V_{RF}$ . The forward request signal  $Req_{n+1}$  is generated by the self-time control mechanism after a deterministic delay, that is “delay X + delay Y,” when the next SCU stage performs a shift-right operation, which activates additional power switches to regulate  $V_{SUP}$ . If  $V_{SUP}$  is greater than  $V_{RF}$ , then the control signal  $CW_n$  will be pulled high to turn off the power switch at this stage. The backward request signal  $Brq_{n-2}$  will be triggered by the self-time mechanism after a deterministic delay, that is “delay X + delay Y,” when the prior SCU stage performs a shift-left operation to reduce the driving capability of  $V_{SUP}$ . Figure 2.75(c) shows the operation timing diagram of the LASC D-LDO regulator. First, EN is pulled low and then, the LCKB signal is forced to high during the power-on reset state. All SCU stages are initialized to turn off all power switches. Once the power-on sequence of the



**Figure 2.74** Implementations of (a) SCU, (b) SR-latch comparator, (c) HR, (d) Muller C-gate, (e) rising edge detector, and (f) TR



**Figure 2.75** Timing diagrams. (a) Single SCU operation when  $V_{SUP}$  is smaller than  $V_{RF}$ . (b) Single SCU operation when  $V_{SUP}$  is larger than  $V_{RF}$ . (c) LASC operation when EN is activated

processor is complete and the EN signal is forced to high, the HR SCU pumps the first request signal  $Req_0$  into the LASC controller, and thus the asynchronous D-LDO regulator output voltage  $V_{SUP}$  can start tracking the reference voltage  $V_{RF}$  according to the required power. During the up-tracking period, the LASC functions as the shift-right operation to increase the number of turning-on power switches by shifting the control signals from  $CW_0$  to  $CW_N$ . When  $V_{SUP}$  reaches its target value of  $V_{RF}$ , backward request signals are generated to stop the delivery of supplementary power to  $V_{SUP}$ . When the LASC operation converges to the adjacent SCU stages, or when the present supply voltage is adequate for correct operation, the signal LCKB is cleared to change the operating state from the tracking mode and return to the locking mode. The operation of the LASC D-LDO regulator ends with the indication of the signal LCKB. Thus, output voltage ripples are eliminated in the LASC D-LDO regulator because all SCUs are in a steady state. Therefore, all devices are also in a steady state and the current consumption closely approaches the  $0.18\ \mu\text{m}$  process core device leakage current, which is approximately

80 nA because of the fully digital D-LDO regulator. The LASC D-LDO regulator achieves a fast response and an ultra-low static current consumption simultaneously.

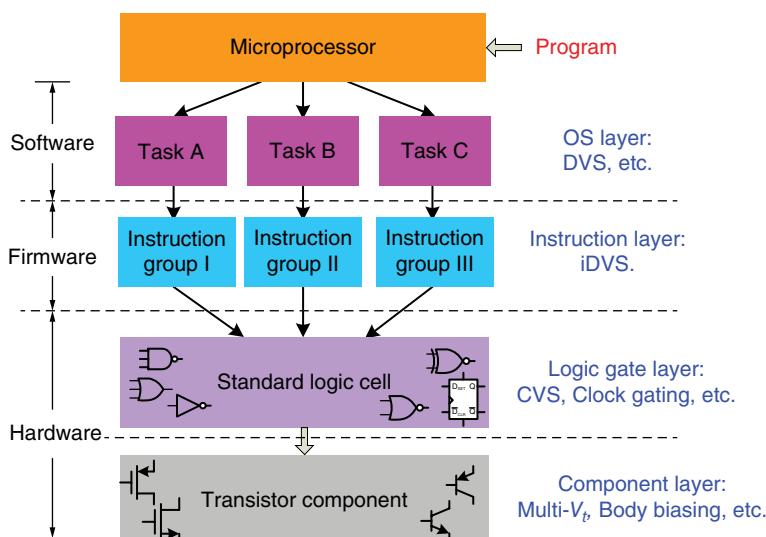
### 2.6.3 Dynamic Voltage Scaling (DVS)

#### 2.6.3.1 Introduction to Basic DVS

Portable electronics are essential products in our daily lives, covering a wide range of applications, including devices and gadgets used for entertainment, communication, and biomedicine. These electronic products contain processors, such as digital signal processors (DSPs), advanced reduced instruction set computing machines (ARMs), and microcontroller units (MCUs), as core components. Therefore, designing low-power processors to save as much power as possible, and extend the battery life of portable devices, is critical.

Figure 2.76 shows the hierarchical processor architecture. The figure also demonstrates that programs are executed from the high-level operating system (OS) layer to the lowest transistor component layer. The program stored in the memory is accessed by the OS to dispatch and schedule different priority tasks. The basic unit of a task is the individual instruction.

After the processor decodes the instructions, the logic gate circuits are activated to perform specific computations. The corresponding layer then accepts the logical control signals to enable or disable millions of transistors. Hence, various techniques have been presented to reduce the power consumption of processors according to the hierarchical processor architecture. In Figure 2.76, state-of-the-art multiple-threshold voltage and body-bias adjustment techniques are employed to reduce the power consumption down to the lowest level of the architecture, that is, the transistor component layer [12]. For simplicity, the clustered-voltage-scaling (CVS) technique at the logic gate layer is adopted to reduce power, because



**Figure 2.76** Low-power management strategy for processors

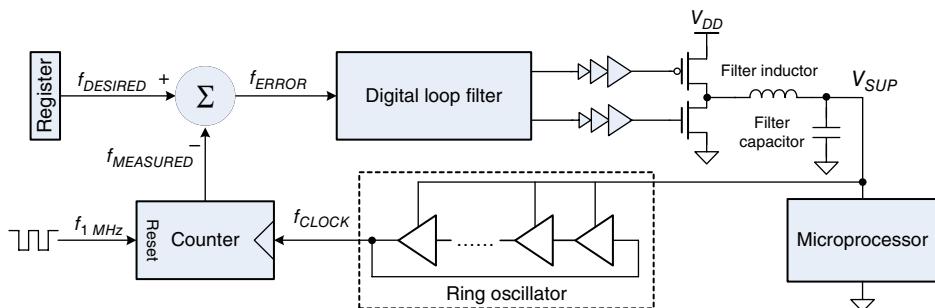
of the distinct CVS of the characteristics of each function block [13]. These techniques exhibit limited power-reduction capabilities and require specific processes supported by the foundries, or careful layout placement of a logical cell with multi-power grids. By contrast, the DVS technique in the OS layer is an effective means to reduce the power consumption, because dynamic power consumption depends on a quadratic function of the supply voltage  $V$  and the clock frequency  $f$ , as shown in Eq. (2.79), where  $C$  is the equivalent dynamic operating capacitance:

$$P \propto CV^2 \quad (2.79)$$

The DVS technique is appropriate for low-power DSP designs fabricated using the standard CMOS process [14–16]. The conventional DVS task-based control circuit presented in [17] and illustrated in Figure 2.77 uses a closed loop to ensure that the clock frequency ( $f_{DESIRED}$ ) satisfies the desired processor operating clock frequency, which is assigned by the OS and stored in the frequency register for a specific task execution. If peak performance is unnecessary, then the operating clock frequency can be decreased to save considerable power. To evaluate the operating clock frequency, the ring oscillator is provided with a real-time supply voltage  $V_{SUP}$  that is generated by an inductor-based SWR to determine the digital numerical clock frequency ( $f_{CLOCK}$ ). Moreover, the supply-determined  $f_{CLOCK}$  is compared with  $f_{DESIRED}$  to identify the digital frequency error signal ( $f_{ERROR}$ ) and produce the control signal by using a digital filter. Finally, the drivers located after the digital loop filter turn the power MOSFETs on/off to modify the output voltage  $V_{SUP}$ . Given the closed loop,  $V_{SUP}$  can be adjusted to be sufficiently high to guarantee that  $f_{CLOCK}$  is close to  $f_{DESIRED}$ .

Therefore, the dynamic frequency scaling (DFS) technique is implemented by the rapid processor clock frequency according to the minimal and dynamic scaling supply voltage. If high efficiency is considered, then the suitable power supply regulator is an inductor-based converter with a low transient response. Consequently, the DVS tracking speed is restricted from a few microseconds to a few milliseconds. The delay caused by voltage tracking decreases efficiency and processor performance. Various fast voltage tracking methods for high-performance DVS response have been reported to satisfy the DVS requirement [18, 19].

The conventional task-based DVS technique allows all tasks in a scheduler to complete just-in-time operations. The OS depends on run-time workload to adjust the supply voltage dynamically, which leads to a substantial power saving [20, 21]. However, the supply voltage  $V_{DD}$  of

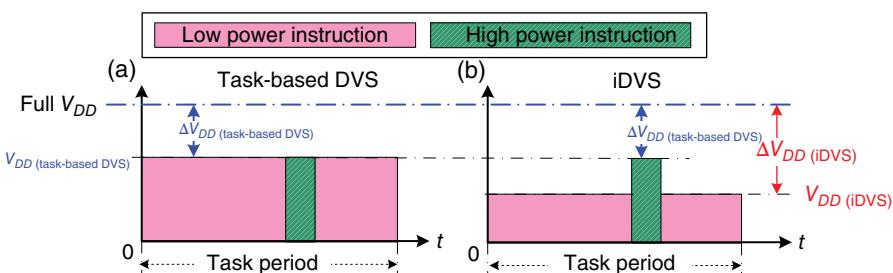


**Figure 2.77** Conventional task-based DVS control circuit

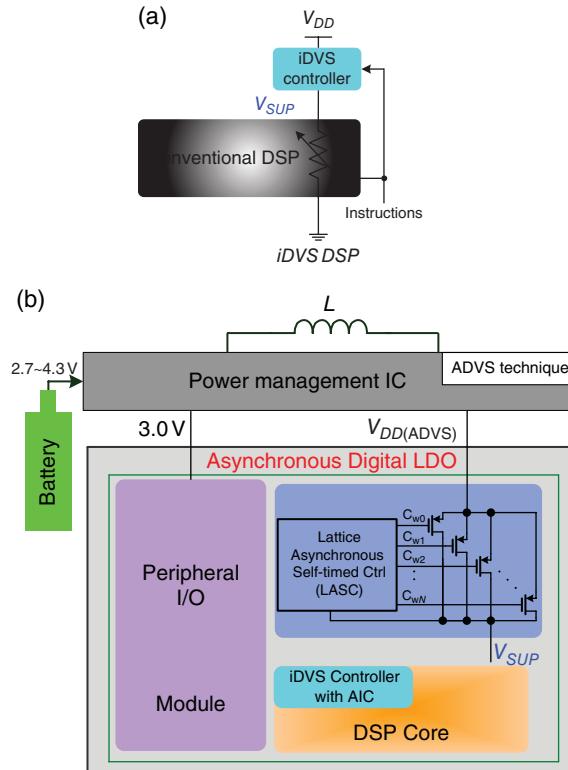
the conventional task-based DVS is limited by the highest power instruction in a task operation, as illustrated in Figure 2.78(a). That is,  $V_{DD}$  is kept high without being scaled down to save power. Thus, the conventional task-based DVS with a conservative scheduler will fail to scale down  $V_{DD}$  because the processor has no slack time. Alternatively, the conventional task-based DVS technique can change the processor operating clock frequency to facilitate a voltage scaling operation; however, this process deteriorates its performance.

A rapidly changing processor clock frequency induces several problems when controlling peripheral modules. These problems include control of signal timing errors and a missing communication data latch in peripheral devices such as synchronous dynamic random access memory (SDRAM), inter-integrated circuit ( $I^2C$ ), analog-to-digital converter (ADC), digital-to-analog converter (DAC), universal asynchronous receiver/transmitter (UART), and flash memory peripheral interface. The reason for such a problem is the dependence of peripheral devices in SoC on a constant clock and predictable control signals. An alternative iDVS technique [22] employs the DVS technique on the instruction layer to overcome the aforementioned drawbacks. One task consists of numerous instructions, as shown in Figure 2.78(b). If the DVS technique is applied on the instruction layer, then more slack time slots can be derived in the iDVS technique. This technique can reduce the power consumption more than the conventional task-based DVS technique.

To further understand this, the processor is regarded as a dynamic loading and emulated by an adjustable resistor that is controlled by instructions, as shown in Figure 2.79(a). The iDVS technique, which is based on different instructions, does not change or stall the processor operating clock frequency. Thus, the processor performs with a minimum power supply to save power. Through the task-based DVS technique, power consumption can be reduced if the operating tasks have low power consumption. Low-power DSP designs can have a powerful energy-saving capability if the DVS technique is applied on the instruction layer. Figure 2.79(b) shows an example of DSP with the iDVS technique to save power dissipation, wherein the LASC D-LDO regulator is used as the voltage buffer to improve the transient response. The SWR cannot satisfy the slew rate requirement of the DSP core. Thus, the LASC D-LDO regulator can exhibit fast reference tracking to satisfy the voltage slew rate requirement. Consequently, the DSP performance and efficiency can be maintained simultaneously. Moreover, at the DSP core side, the iDVS controller requires the adaptive instruction-cycle control (AIC) circuit to guarantee fast voltage tracking speed and high operating frequency. Moreover, an additional design flow for the iDVS technique, with the help of an automatic computer-aided design (CAD) tool, is also required to maximize power-saving performance.



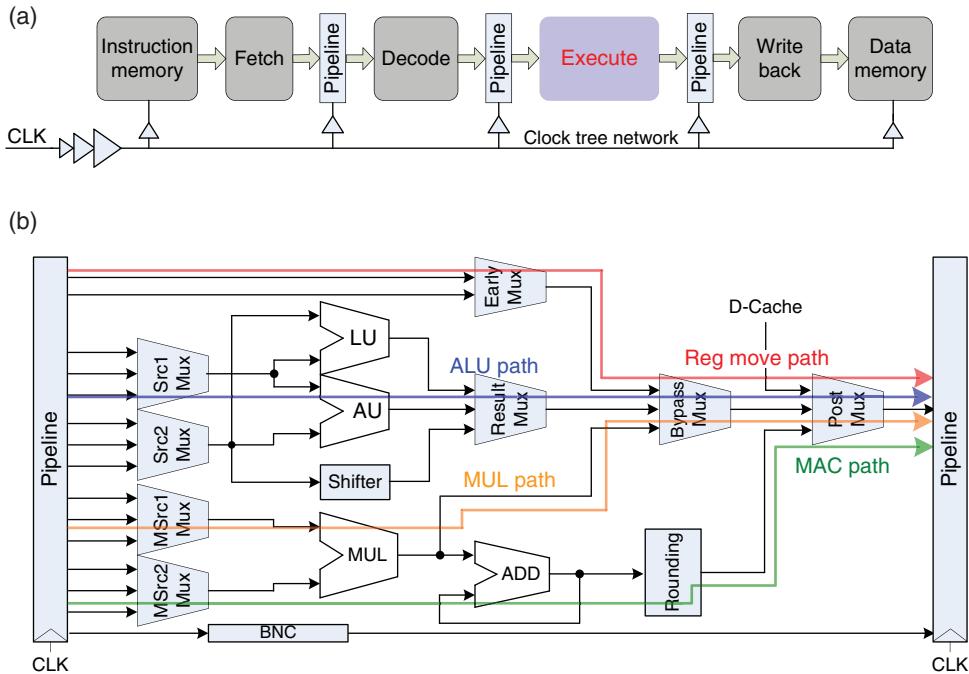
**Figure 2.78** (a) Conventional task-based DVS limited by high power instruction. (b) iDVS effectively reduces power consumption



**Figure 2.79** (a) Concept of iDVS operation. (b) DSP core with implementation of the iDVS technique

### 2.6.3.2 Instruction-Cycle-Based Dynamic Voltage Scaling (iDVS)

Processors are designed to provide versatile application programs. When listening to a Moving Picture Experts Group audio layer III (MP3) while simultaneously browsing a picture from a flash memory device, the OS dispatches file-system access and the MP3/Joint Photographic Experts Group (JPEG) decoding algorithm. Similarly, when taking a phone call, the OS of an embedded system launches the key-scan service and the speech compressing/decompressing code-excited linear prediction (CELP) algorithm once mobile phone buttons are pressed. Although these task programs have different characteristics, their fundamental unit is the instruction unit. The basic steps of program execution in a processor are instruction fetching, decoding, execution, and storing, as illustrated in Figure 2.80(a). The most complicated part is the execution unit, shown in Figure 2.80(b), which can provide all types of hardware circuit to support different complex instructions. Each instruction has a corresponding critical data path to complete execution. Critical paths occupy only a small fraction of the total number of paths within a chip. However, the clock speed of a synchronous processor is determined by the worst delay of the critical paths. These critical paths usually map high-power-consuming and long-data-path instructions that are subject to single-instruction multiple-data (SIMD) instructions, such as divide (DIV), normalize (NORM), and multiply-and-accumulate (MAC). Long slack time occurs in non-critical path instructions.



**Figure 2.80** (a) Basic steps of program execution. (b) Critical paths during instruction execution

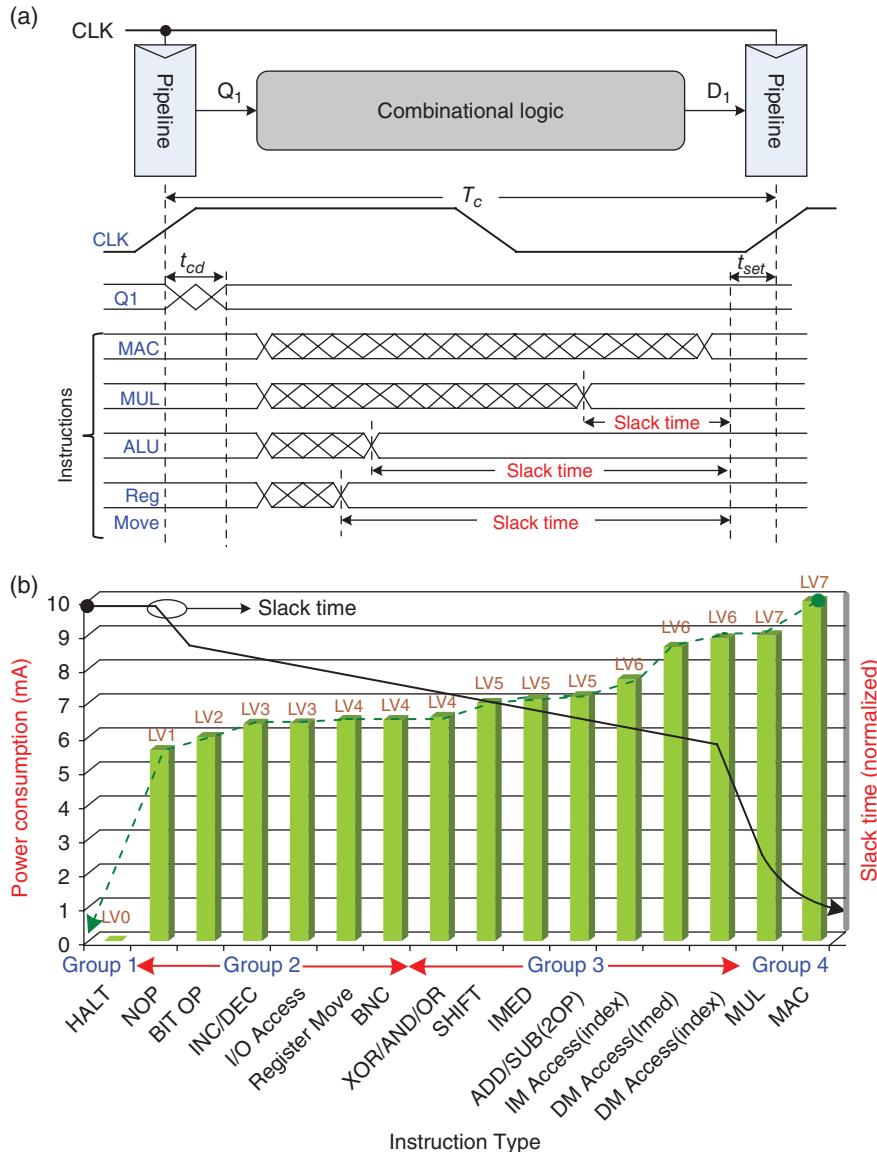
Different instructions present varying slack time, as shown in Figure 2.81(a). The measured slack time and its corresponding power consumption with different instructions are shown in Figure 2.81(b), with the supply voltage fixed at 1.8 V. In summary, a long slack time corresponds to a low power consumption because of the small supply voltage provided by the iDVS technique. Reducing the supply voltage in CMOS circuits affects the propagation delay  $T_d$  expressed in Eq. (2.80), which is inversely proportional to  $V_{DD}$  and the maximum operating frequency  $f_{max}$ :

$$T_d \propto \frac{V_{DD}}{(V_{DD} - V_t)^n} \propto \frac{1}{f_{max}} \quad (2.80)$$

where  $V_t$  is the threshold voltage determined by foundry process parameters.

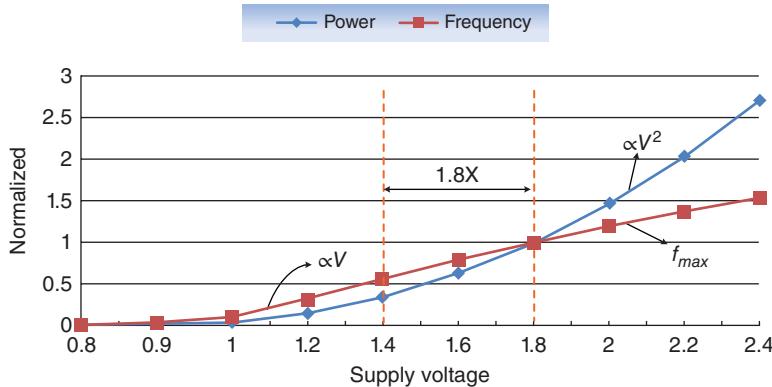
For simplicity, instructions can be classified into different power groups, namely Groups 1–4, for the iDVS technique to provide the corresponding  $V_{DD}$ .

The test chip of a 23-stage ring oscillator in a 0.18  $\mu\text{m}$  CMOS process uses 1.8 V core devices. Figure 2.82 shows the maximum operating frequency  $f_{max}$  and the total power consumption with respect to the supply voltage variation. According to the data measured at the supply voltage of 1.8 V, the unit of the y-axis is the normalized operating frequency and the normalized power consumption. The linear relationship between circuit operating frequency and supply voltage  $V_{DD}$  ranges from 1.2 to 1.8 V. If  $V_{DD}$  is scaled down from 1.8 to 1.4 V, then  $f_{max}$  is still larger than half of the maximum operating frequency at 1.8 V. Thus, the scaling range of  $V_{DD}$  for



**Figure 2.81** (a) Slack time in different instructions. (b) Measured slack time and power consumption in different instructions

normal operation in iDVS is from 1.2 to 1.8 V, excluding HALT and no operation (NOP) instructions. The minimum  $V_{DD}$  should be larger than 1 V; otherwise, the level-shift signal will experience serious delay when traveling from the level-shift circuit to peripheral I/O modules. Power reduction can be achieved if the iDVS technique reduces the  $V_{DD}$  of the instruction execution on the non-critical path while maintaining a high supply voltage on the critical paths to satisfy complex instruction timing requests. The iDVS dynamically adjusts  $V_{DD}$  based on the



**Figure 2.82** Normalized operating frequency and normalized power consumption vs. supply voltage in a 23-stage ring oscillator fabricated via the 0.18  $\mu\text{m}$  CMOS process

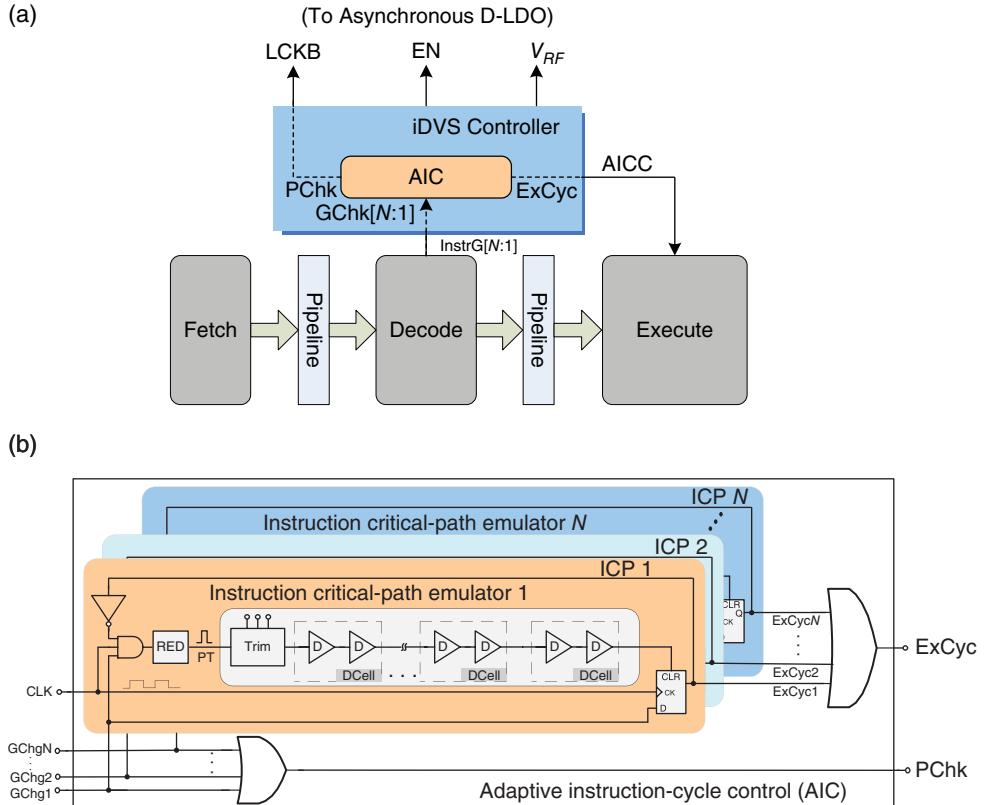
instruction-cycle domain to guarantee sufficient power for the appropriate execution of instructions.

In conventional DVS systems, a voltage transition will stall the entire processor operation unless the required power for instructions is available, which results in serious degradation of the million instructions per second (MIPS) performance. By contrast, the iDVS technique uses an embedded all-digital LASCD-LDO regulator with low quiescent current to achieve high-speed voltage tracking capability and provide in-demand power for instruction execution. Moreover, the LASCD-LDO regulator receives assistance from the AIC circuit to avoid the aforementioned drawbacks. The AIC scheme can adaptively adjust the instruction execution cycle time to guarantee that each instruction is correctly executed during voltage tracking for high-performance iDVS operation. That is, the iDVS-based design processor does not change the processor clock frequency or stall the entire processor clock during DVS operation. Consequently, the clock frequency is kept constant, which is suitable for controlling peripheral I/O devices in the Soc.

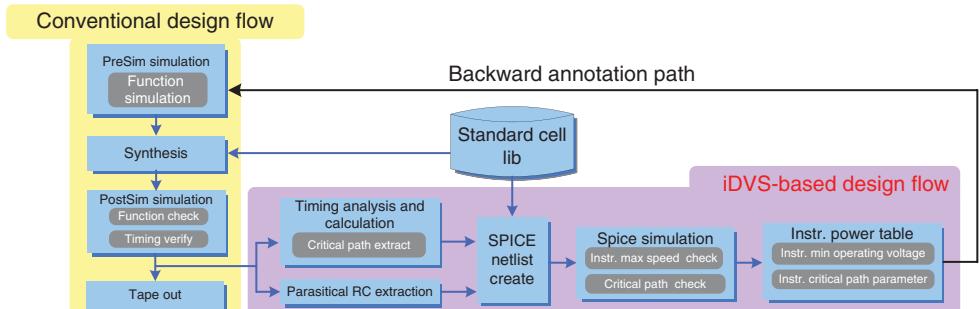
### 2.6.3.3 Adaptive Instruction-Cycle Control

An instruction unit occupies one clock cycle in the reduced instruction set computing (RISC) design. A real-time adaptive instruction cycle should be performed in the AIC circuit to adapt to the scaling supply voltage level of the LASCD-LDO regulator.

Figure 2.83(a), (b) shows the topologies of the iDVS controller and the AIC circuit, respectively. The instruction critical path (ICP) shown in Figure 2.83(b) emulates the relative instruction group critical path delay, which is synthesized by the standard cell delay component after timing verification through the iDVS CAD design flow shown in Figure 2.84. Given that a processor has thousands of data paths and millions of logic gates, identifying the corresponding critical data path for each instruction and the relative operating voltage for the iDVS technique is an important issue. Manually analyzing the correlation between critical data paths and instructions is impractical. Circuit extraction tools obtain register-transfer-level (RTL) components and parasitic RC from the ICP to derive the parameters required by the ICP emulator. The extracted circuit netlist is used for simulation program with integrated circuit emphasis



**Figure 2.83** (a) Topology of the iDVS controller with the AIC circuit. (b) AIC circuit



**Figure 2.84** Standard cell library design flow with the iDVS-based design flow

(SPICE) simulations to obtain the minimum operating voltage for each instruction under PVT variations.

The design flow contains three steps, outlined as follows. First, hardware specifications are coded into the hardware description language (HDL) according to the traditional design flow to synthesize the cell-based circuit for post-simulation, which can check the function and verify

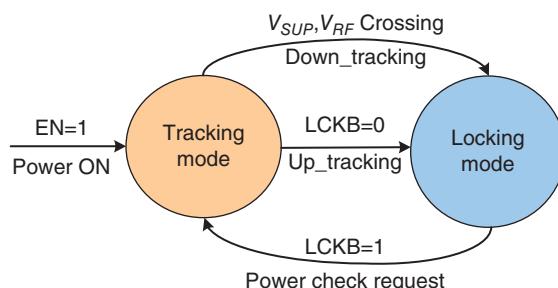
timing. The critical path of each instruction at the post-stimulation stage can be extracted by the timing analysis tool. A SPICE simulator is used to establish the critical path table for correlating the minimum operating voltage to each corresponding instruction. The timing parameter of each ICP is also extracted to create the ICP in the AIC circuit. The final step is the backward annotation of each instruction power catalog and timing constraint to the iDVS controller in the HDL design. Considering the assistance of RC extraction and the timing analysis tools, the iDVS technique can fit any standard cell library provided by foundries.

Instructions with the same characteristics of data path or power consumption are grouped into one ICP emulator. Each ICP contains a RED, standard-cell delay components, a delay trimming module, and control logics. The delay trimming module is an option for minimizing mass-production deviation after a minor adjustment. Figure 2.85 shows the operating states of the iDVS controller with the timing diagrams, as presented in Figure 2.86. The DSP instruction cycle is synchronized with the edge-triggered clock signal CLK. In each cycle, different instructions as presented in Figure 2.81 are decoded to generate the instruction group signal InstrG[N:1]. When the DSP consecutively executes the instruction stream, the iDVS controller monitors the required power for each instruction according to the instruction power table generated by the CAD design flow.

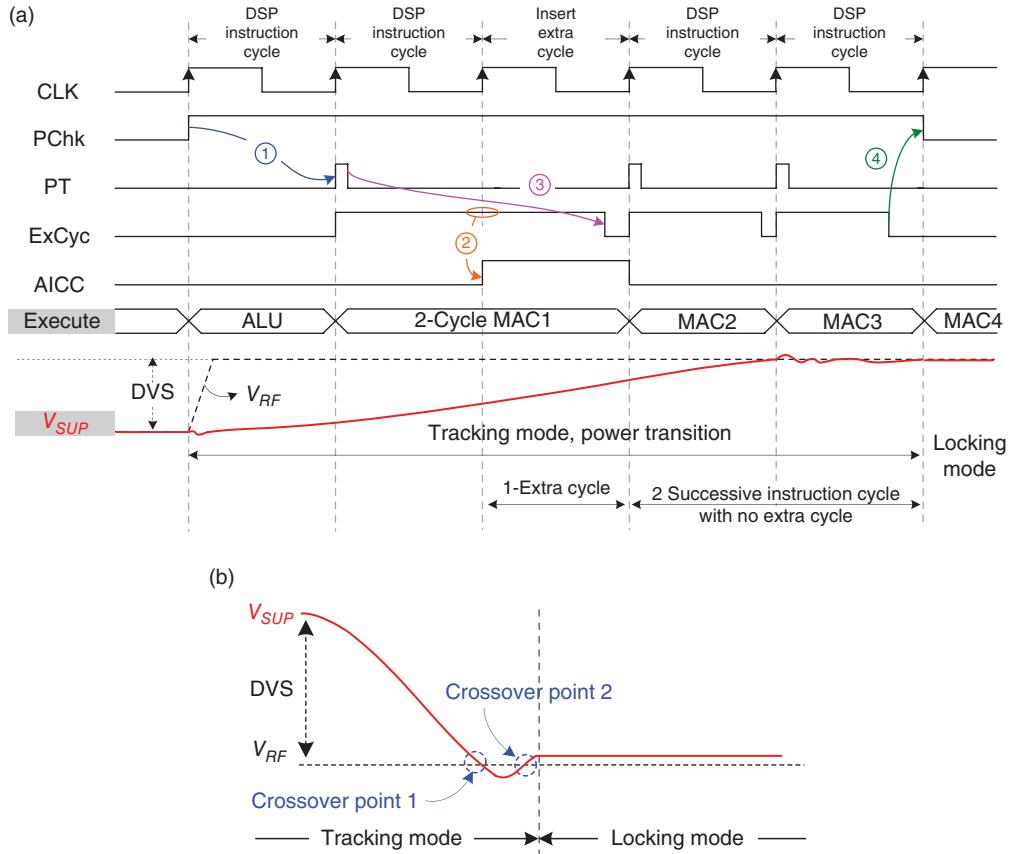
Once iDVS detects that the required execution power of the next instruction is different from that of the current execution instruction group, the instruction group changes the signals GChg [N:1] to the AIC circuit.

In the next stage, the iDVS controller enters the tracking mode from its operating state to activate the LASC D-LDO regulator by setting the signal LCKB to high. As shown in Figure 2.86(a), given the characteristics of the DSP pipeline structure, the voltage transition command is issued before an instruction is executed prior to the one-clock cycle. Once RED detects the instruction group change signals, which are synchronized with CLK, RED will induce one pulse signal PT to the ICP emulator. The next operation of the AIC circuit is similar to the race condition, to test whether the instruction can finish execution within one instruction cycle at the present supply voltage  $V_{SUP}$ . If PT passes through the ICP emulator and simultaneously exceeds the rising edge of the CLK, then the AIC circuit will pull the signal ExCyc to low, which is synchronized by the iDVS controller to generate the signal AICC. Thus, the signal AICC is set to low to inform the DSP execution unit that an extra cycle is not required during the instruction cycle.

By contrast, the passing of PT through the ICP emulator, and the lag of the rising edge of the CLK, indicates that  $V_{SUP}$  provides insufficient power. DSP should insert an extra cycle to



**Figure 2.85** Operating states of the iDVS controller



**Figure 2.86** Timing diagram of iDVS operation. (a) Up-tracking condition. (b) Down-tracking condition

complete current instruction execution by setting AICC to high. According to Eq. (2.80) and Figure 2.82, no instruction is required to exceed two cycles for execution in the section of 1.4–1.8 V. Given the instruction for pre-decoding the pipeline structure and the fast transition response of the LASC D-LDO regulator, the iDVS-based DSP only requires one extra cycle during up-tracking voltage transition. If the iDVS controller detects a low level of AICC within two successive instruction cycles, then the supply voltage is well regulated and sufficient for instruction execution. The iDVS controller then withdraws the power check request signal PChk and returns to locking mode by setting LCKB to low.

During down-tracking voltage transition, the supply voltage  $V_{SUP}$  is sufficiently high to avoid blocking DSP execution. The control sequence of down-tracking voltage transition is shown as follows. First, the D-LDO regulator pulls the  $V_{SUP}$  to low. The iDVS controller then sends the group change signals GChg[N:1] to the AIC circuit and continuously monitors the comparison result of  $V_{SUP}$  with the reference voltage  $V_{RF}$ . Finally, the iDVS controller returns to locking mode by setting the LCKB to low until  $V_{SUP}$  and  $V_{RF}$  have two crossover points after signal AICC is maintained at low levels within two successive instruction cycles, as shown in

Figure 2.86(b). Simultaneously, the iDVS controller withdraws the power check request signal PChk. The supply voltage is adequate for executing instructions in locking mode. Therefore, the AIC mechanism achieves correct instruction execution during iDVS voltage transition without stopping the operation clock.

## 2.7 Switchable Digital/Analog-LDO (D/A-LDO) Regulator with Analog DVS Technique

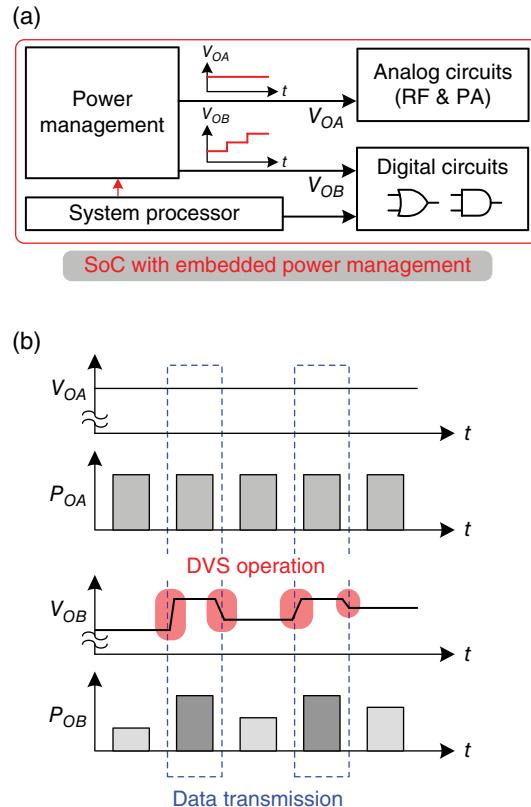
### 2.7.1 ADVS Technique

In Soc applications, the sub-circuits can mainly be sorted into digital and analog sub-circuits. According to the analog/digital characteristics, different demands are made in supply voltage source qualities, such as driving capability, input/output voltage variation, transient response, noise immunity, and so on.

That is, power management is an essential design issue in Soc, which requires distributive voltage and current levels for distinct sub-circuits. Figure 2.87(a) shows the Soc with an analog sub-circuit and a digital sub-circuit, provided separately by supply voltages  $V_{OA}$  and  $V_{OB}$  from power management. Moreover, power reduction capability is another necessary feature in power management. DVS is the most efficient technique for power reduction. The DVS function is generally implemented in digital blocks, and thus the digital circuit power consumption can also be optimized by different operating instructions or tasks in Soc. To realize DVS-based power management, the power converter works with the system processor, which can send voltage indication signals to the power converter to adjust the output voltage. As shown in Figure 2.87(b), if Soc enters into data transmission operation, then the increase in  $V_{OB}$  satisfies the Soc speed requirement. The decrease in  $V_{OB}$  also conserves power when data transmission ends. Comparatively, analog circuits cannot use a similar DVS technique in digital circuits because the supply voltage for analog circuits should be kept constant to maintain some important performance. Moreover, when one SWR is used to provide  $V_{OA}$ , the switching voltage ripple at the  $V_{OA}$  will degrade accuracy, power supply rejection ratio (PSRR), and so on. By contrast, the LDO regulator can be utilized to suppress noise for high-quality supply voltage, sacrificing efficiency with a large dropout voltage when the LDO regulator directly converts  $V_{OA}$  from the input voltage  $V_{IN}$ . To reduce the power consumption on the dropout voltage of the LDO regulator, an LDO regulator is generally cascaded in series with a switching-based power converter. Consequently, complete conversion efficiency is expressed as:

$$\eta_{complete} = \eta_{switching} \cdot \eta_{LDO} \quad (2.81)$$

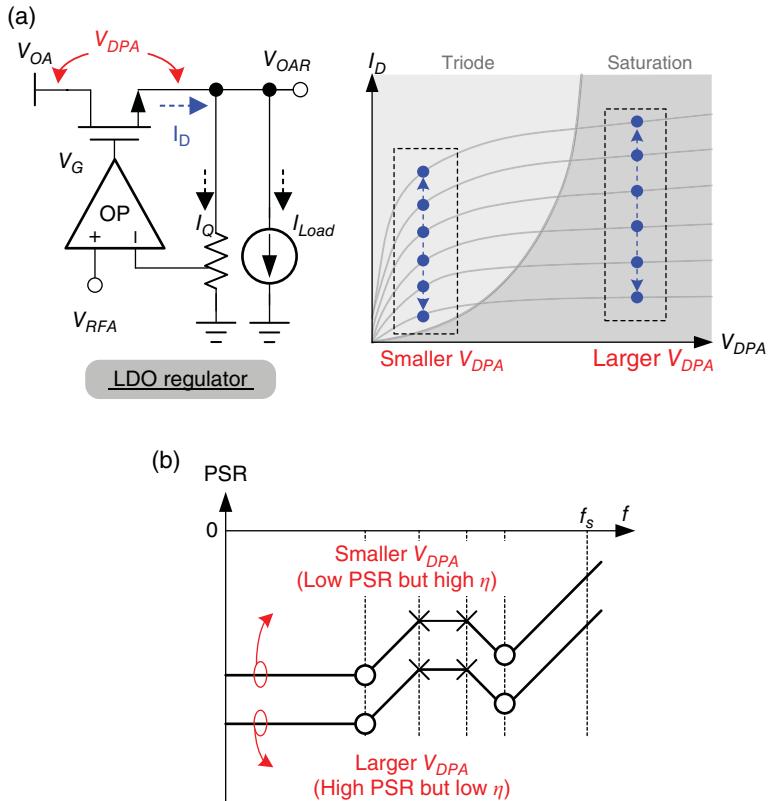
To maintain high efficiency and a high-quality supply voltage for analog sub-circuits, a switching-based power converter is responsible for a wide conversion ratio, whereas the LDO regulator is responsible for switching noise suppression with adequate dropout voltage. To prolong the battery life further using time for portable devices, we need to think whether a solution is available to improve the efficiency further. The dropout voltage of the LDO regulator remains a serious factor to limit complete conversion efficiency, although a switching-based power converter can benefit most complete conversion efficiencies because of the usage of the storage component, inductor, and capacitor. For example, the maximum  $\eta_{complete}$  is



**Figure 2.87** (a) Power management in Soc provides two distinct supply voltages,  $V_{OA}$  and  $V_{OB}$ , for digital and analog circuits, respectively. (b) DVS techniques at  $V_{OB}$  corresponding to the Soc operation compared with the fixed voltage at  $V_{OA}$

approximately 81% when  $\eta_{switching}$  is 90% and  $\eta_{LDO}$  is 90%. Consequently, the dropout voltage of the LDO regulator should be designed more carefully to improve efficiency.

Figure 2.88(a) illustrates the relationship between the dropout voltage  $V_{DPA}$  and the current of the power MOSFET in the analog LDO regulator. The performance of voltage ripple suppression depends on the dropout voltage across the pass transistor, which is regarded as a buffer between the input supply voltage and the output voltage. The power MOSFET in the triode region, which operates with a small dropout voltage, behaves as a 1 V controlled resistance. However, its PSR becomes worse than that in the deep saturation region. By contrast, a large dropout voltage in the deep saturation region improves the PSR but deteriorates the PCE, as shown in Figure 2.88(b). The definition of the ADVS technique for analog circuits is to scale the SWR output voltage dynamically, and simultaneously the dropout voltage  $V_{DPA}$  according to the output loading condition, and maintaining  $V_{OAR}$  constant for analog circuits. That is, the ADVS technique considers the trade-off between efficiency and output voltage ripple without affecting the performance of analog circuits in the Soc [23]. The cooperation between the SWR and the LDO becomes one design issue if the ADVS technique is applied in the Soc.



**Figure 2.88** (a) Dropout voltage  $V_{DPA}$  of the LDO regulator. (b) Relationship between dropout voltage  $V_{DPA}$  and PSR

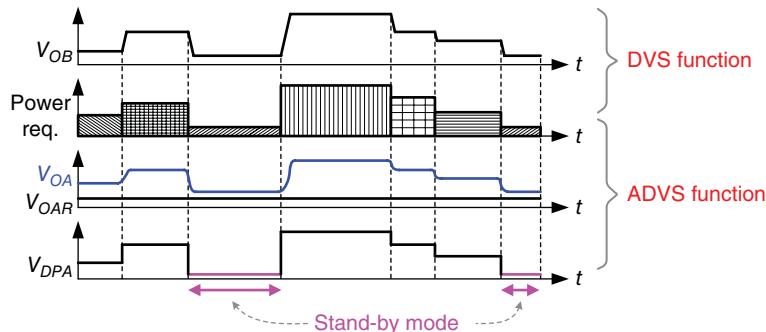
The drain current in the saturation region is shown in Eq. (2.82). The boundary condition between the triode region and the saturation region is defined as the  $V_{DS}$  that is equal to  $V_{OV}$  in Eq. (2.83).  $V_{DS}$  is proportional to the square of the drain current  $I_D$  if the channel length modulation parameter  $\lambda$  is neglected.

$$I_D = \frac{1}{2} k_n' \left( \frac{W}{L} \right) V_{OV}^2 (1 + \lambda V_{DS}) \text{ where } V_{DS} \geq V_{OV} \quad (2.82)$$

$$V_{DS} = V_{OV} \propto \sqrt{I_D} \quad (2.83)$$

As the loading current decreases, only a small dropout voltage is required to ensure proper functioning of the power MOSFET in the saturation region for good PSR. Therefore, a small dropout voltage can eliminate superfluous conduction power loss on the power MOSFET and enhance PCE.

Figure 2.89 compares the operations of both the DVS function in digital circuits and the ADVS function in analog circuits. When the Soc enters into operating mode, the DVS function that is indicated by the system processor is activated to optimize power consumption. The



**Figure 2.89** Operations of the DVS function in digital circuits and the ADVS function in analog circuits

ADVS function also enables dynamic dropout voltage adjustment of the LDO regulator to guarantee high PSR and PCE. This procedure can be realized by adjusting the output voltage level of  $V_{OA}$  corresponding to the loading current condition at  $V_{OAR}$ .

### 2.7.2 Switchable D/A-LDO Regulator

To realize versatile power management performance for Soc, reducing power loss in standby mode is a crucial consideration for prolonging battery life. As discussed earlier, the *C-free* LDO regulator encounters obstacles in stability under ultra-light load. In response to the disadvantages of the *C-free* LDO design, the output should dissipate a minimum load current to ensure stability but sacrifice power efficiency. Consequently, the switchable digital/analog low drop-out (D/A LDO) regulator has been developed.

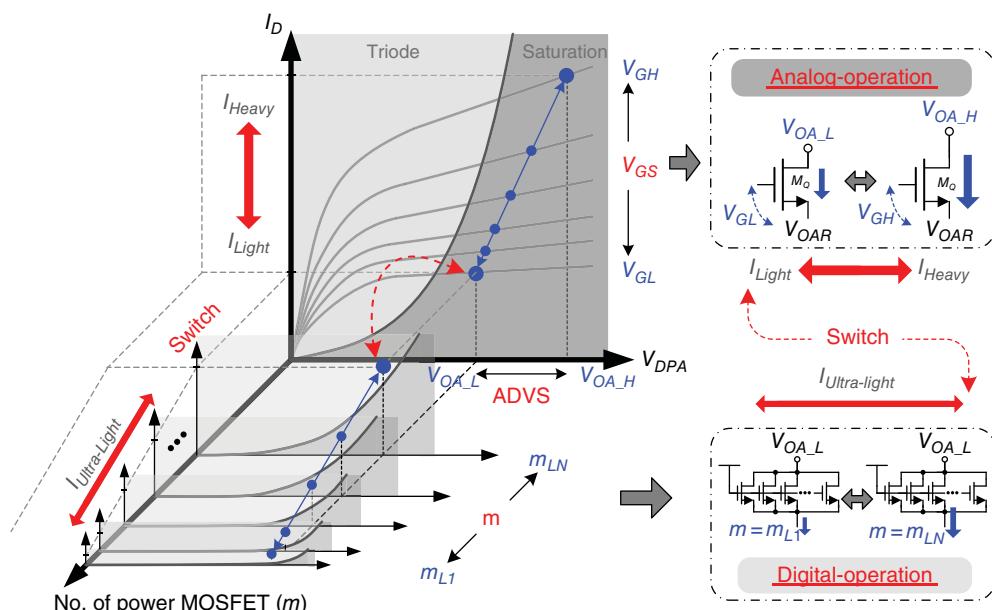
When the switchable D/A LDO regulator works in an analog operation, the power MOSFET is driven by an analog amplifier. Through the ADVS technique, the LDO regulator can exhibit good noise suppression. By contrast, the switchable D/A LDO regulator works in a digital operation if the Soc enters in silent or standby mode. The power MOSFET is driven by a digital controller, such as the D-LDO regulator. Although the capability of ripple suppression decreases, the sub-circuits in most applications can tolerate a large voltage variation in standby mode. Moreover, the dropout voltage is reduced to a relatively small value for an energy-efficient operation.

In prior studies, the current flowing through the resistor divider and the quiescent current are equal to tens or hundreds of microamperes. To reduce the loading current to a value lower than the minimum load current required by the conventional *C-free* LDO regulator, the D/A LDO regulator is switched from analog to digital operation. Thus, under ultra-light loads, the pole in the output moves toward the origin and stability decreases drastically. Without the assistance of the dummy load current, the power MOSFET is modulated by the digital controller rather than by the analog controller (the EA) to decrease the quiescent current significantly. Thus, the digital operation of the D/A LDO regulator breaks through the limitations of the minimum load current for the capacitor-free LDO regulator. The digitally operated LDO regulator confirms stability even under a no-load condition, while consuming only 50 nA quiescent current in the controller and 0.5  $\mu$ A current in the resistor divider. One advantage of this regulator is that

the digital controller features a low quiescent current and further enhances the PCE. In turn, a high current efficiency is achieved over a wide range of load current with a compact solution to Soc power management.

The concept of a switchable D/A LDO regulator is illustrated by the  $I$ - $V$  characteristic curve in Figure 2.90. According to the loading current from the Soc power requirement, analog or digital operation is initiated to ensure voltage regulation and achieve high power efficiency. An analog operation uses the ADVS function to adjust the adaptive dropout voltage to maintain high efficiency.

The right section of Figure 2.90 illustrates the operating behavior of the power MOSFET  $M_Q$  in either analog or digital operation. In particular, the EA controls  $M_Q$  to determine an adequate gate voltage level that corresponds to the load current condition. Moreover, given the regulated output voltage,  $V_{OAR}$ , of the D/A LDO regulator, the loading current adjusts the dropout voltage to determine the adequate output voltage  $V_{OA}$  from the SWR. When the loading condition changes from heavy to light,  $V_{OA}$  changes from  $V_{OA\_H}$  to  $V_{OA\_L}$  and obtains a smaller dropout voltage while simultaneously decreasing the gate voltage level from  $V_{GH}$  to  $V_{GL}$  for an appropriate driving capability. If the loading current decreases under certain values, analog operation switches to digital operation to save power. During digital operation, the transistor  $M_Q$  is divided into several parallel SMUs. Portions of the SMUs are turned on and off by the digital controller according to the load current. The number of turned-on SMUs is denoted  $m$ . When the load current decreases continuously, the value of  $m$  shrinks. Thus, the switchable D/A LDO regulator selects suitable analog and digital operations to satisfy the demand from analog circuits in the Soc.



**Figure 2.90**  $I$ - $V$  characteristic curve of the switchable function in analog and digital operations

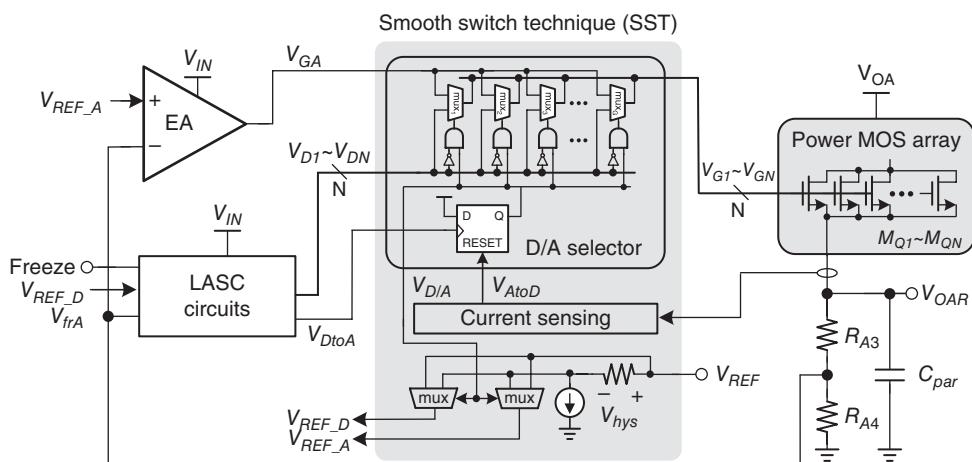
### 2.7.2.1 Switchable D/A LDO Regulator

A schematic of the switchable D/A LDO regulator is provided in Figure 2.91. Digital and analog operations indicate that SMUs are controlled by LASC [24] and the EA [25], respectively. The smooth switch technique (SST) decides whether digital or analog operation is used with respect to the loading current condition. The key point is a continuous and smooth switching procedure between digital and analog operations. The D/A selector is structured by an array of multiplexers and controlled by the load-dependent signals  $V_{AtoD}$  and  $V_{DtoA}$ . Pass transistors  $M_{Q1}$  to  $M_{QN}$  are controlled by the gate control signals  $V_{D1}$  to  $V_{DN}$  of the digital controller or the analog signal  $V_{GA}$  of the analog controller.

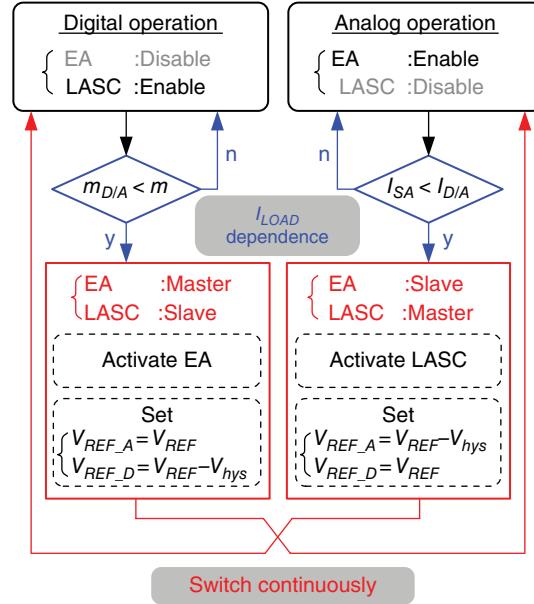
In analog operation, the EA generates the error signal  $V_{GA}$  to guarantee the output voltage  $V_{OAR}$  under different output loading current conditions, where each gate voltage, from  $V_{G1}$  to  $V_{GN}$ , of the pass transistors is connected to the error signal  $V_{GA}$ . By contrast, in digital operation, the LASC circuit generates thermometer control codes for each of the pass transistors when the Soc enters silent mode. The digital control method releases the minimum load limitations at only several microamperes for the system to conserve power effectively. Moreover, the frozen operation in the LASC circuit reduces the quiescent current to an ultra-low value for high efficiency. The switchable D/A LDO regulator achieves ripple suppression and energy-efficient operation in a distinct mode for high efficiency.

### 2.7.2.2 Smooth Switch Technique (SST)

The switchable D/A LDO regulator indicates that only one analog/digital operation can be enabled in case of a loading current change. The SST ensures a continuous and smooth takeover procedure between analog and digital operations to prevent undesirable oscillations that induce considerable output voltage ripples. The hysteresis window  $V_{hys}$  adjusts the reference voltages of the D/A LDO regulator during the switching procedure. The flowchart in Figure 2.92



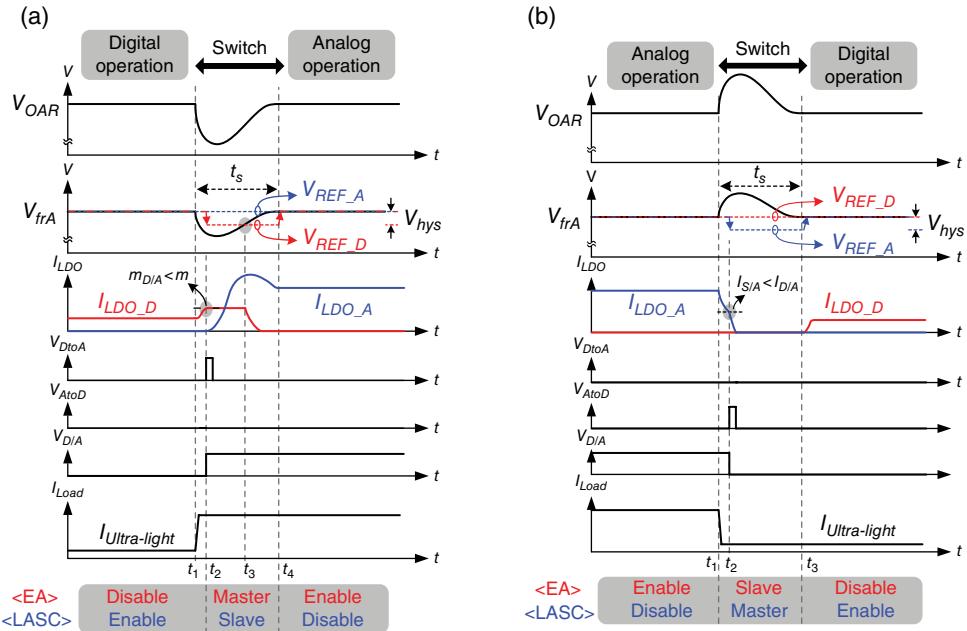
**Figure 2.91** Schematic of the switchable D/A LDO regulator



**Figure 2.92** Flowchart of the switchable technique

describes the operation procedure during switching. The increasing value of  $m$  becomes larger than the predefined  $m_{D/A}$ , which triggers the operating procedure via the pulse signal  $V_{DtoA}$  when the LDO regulator switches from digital to analog operation as the loading current increases. Thus, the EA is activated and the reference voltage of LASC, that is  $V_{REF\_D}$ , also changes from  $V_{REF}$  to the value of  $V_{REF} - V_{hys}$ . The EA and LASC temporarily operate simultaneously. Meanwhile, the EA gradually dominates control of the SMUs when the feedback voltage  $V_{frA}$  is larger than  $V_{REF\_D}$ . The EA and LASC represent the master and the slave, respectively. Finally, the switching procedure is complete when the EA takes over the operation and disables LASC automatically. By contrast, when the LDO regulator switches from analog to digital operation during loading current decreases, the decreasing sensing current  $I_{SA}$  becomes smaller than the predefined  $I_{D/A}$  and triggers the switching procedure by the pulse signal  $V_{AtoD}$  in Figure 2.91. The following switching procedure is complete via the aforementioned opposite procedure.

The operation waveforms of the SST are shown in Figure 2.93. The currents  $I_{LDO\_D}$  and  $I_{LDO\_A}$  flow through the SMUs and are controlled by LASC and the EA, respectively. In cases of increasing loading current, digital operation switches to analog operation, as illustrated in Figure 2.93(a). At  $t = t_1$ ,  $I_{LDO\_D}$  increases corresponding to the increasing number of turned-on SMUs. At  $t = t_2$ , if  $m$  is larger than  $m_{D/A}$  then the EA is enabled and the reference voltage of LASC,  $V_{REF\_D}$ , changes from  $V_{REF}$  to the value of  $V_{REF} - V_{hys}$ . Consequently, the EA and the LASC function have a master-slave relationship. During this period, the EA controls the remaining switched-off SMUs and  $I_{LDO\_A}$  subsequently increases to regulate the output voltage  $V_{OAR}$ . Once the feedback voltage  $V_{frA}$  increases to a value higher than  $V_{REF\_D}$  at  $t = t_3$ ,  $I_{LDO\_D}$  is reduced to zero and LASC is automatically disabled. Finally, the switching



**Figure 2.93** Control mechanism of the switchable technique between digital operation and analog operation. (a) Switching from digital operation to analog operation. (b) Switching from analog operation to digital operation

procedure is complete after  $V_{OAR}$  recovers at  $t = t_4$ . Analog operation takes over and enables only the EA. LASC is shut down to enable single analog loop control work.

Analog operation can be switched back to digital operation if the loading current decreases to a sufficiently low value, as shown in Figure 2.93(b). At  $t = t_1$ , the  $I_{LDO\_A}$  controlled by the EA decreases continuously. At  $t = t_2$ , once the condition of  $I_{SA}$  is smaller than that of  $I_{D/A}$ , LASC is enabled and the reference voltage of the EA,  $V_{REF\_A}$ , changes from  $V_{REF}$  to the value of  $V_{REF} - V_{hys}$ . Thus,  $I_{LDO\_D}$  gradually increases while  $I_{LDO\_A}$  decreases to zero. The switching procedure is complete when  $V_{OAR}$  is recovered at  $t = t_3$ .

According to the load condition, the SMUs are controlled by the analog or digital controller determined by the SST. Approximately 10% of the SMUs are driven by the digital controller under light loads. Meanwhile, 90% of the SMUs are turned off. During the D/A switching procedure under light-to-heavy load changing, the analog controller controls a portion of the power MOS units, while the digital controller controls other portions. The analog controller controls all power MOSFET units at the end of the load change. Finally, none of the SMUs is controlled by the digital controller. Consequently, the energy delivered to the output is continuous to retain a low output voltage variation. By reflecting the variation of the output voltage through the feedback network, the condition  $m_{D/A} < m$  or  $I_{SA} < I_{D/A}$  implies which controller is suitable for use. Thus, the SMUs are adequately controlled even if the loading condition changes faster than the switching time. Upon setting the reference voltage to  $V_{REF} - V_{hys}$ , stability is confirmed if a moderate or long period is used as the hysteresis window.

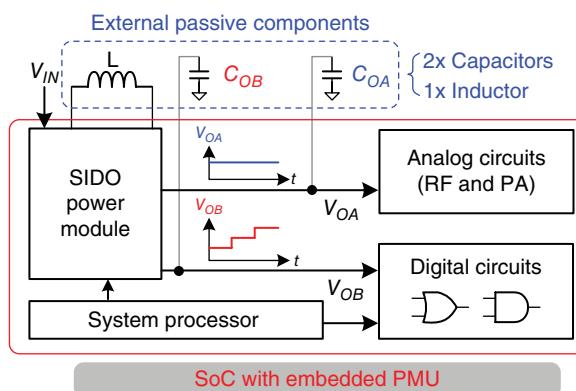
### 2.7.2.3 ADVS PMU with Combined SWR and Switchable D/A LDO Regulator for Soc

Among currently available advanced power management unit (PMU) designs, the single-inductor dual-output (SIDO) converter is used to further reduce PMU size, where the two output voltages are  $V_{OA}$  and  $V_{OB}$  for analog and digital sub-circuits in the Soc, respectively, as shown in Figure 2.94. The advantage of the SIDO converter is its compact size, which can be attributed to the usage of only one off-chip inductor compared with others that use multiple off-chip inductors [7,19,26–28]. Detailed design guidelines are provided in the next chapter.

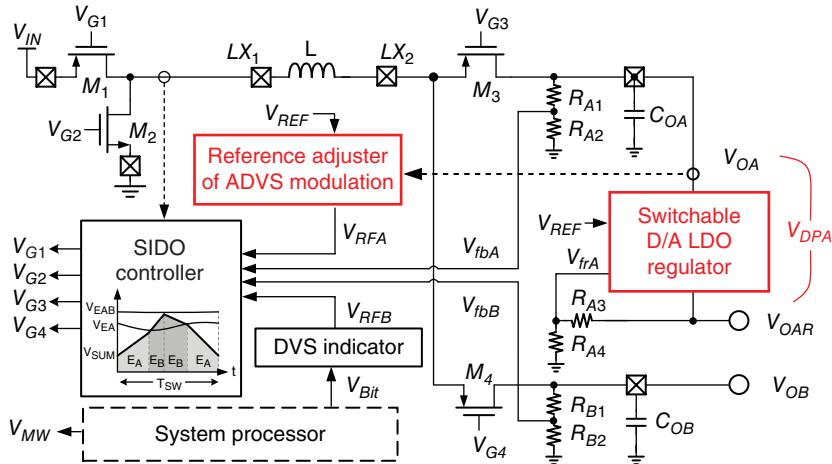
For high efficiency, the ADVS technique can be implemented in the PMU design. That is, the combination of SWR and the switchable D/A LDO regulator can provide ADVS PMU for Soc. With regard to PMU design using the dual DVS techniques in Soc, the SIDO converter shown in Figure 2.95 has two outputs. The first output is for digital sub-circuits and the second, with the switchable D/A LDO regulator, is for analog sub-circuits.

With only one off-chip inductor, the power stage of the SIDO converter is composed of four power switches from  $M_1$  to  $M_4$ . These switches transfer the energy from the input battery to both outputs,  $V_{OA}$  and  $V_{OB}$ .  $V_{OB}$  supplies digital circuits directly to the Soc. In DVS operation, the DVS indicator receives the control signal  $V_{Bit}$  from the system processor to generate the reference voltage  $V_{RFB}$  for  $V_{OB}$ . By contrast, the switchable D/A LDO regulator is cascaded in series with the  $V_{OA}$  of the SIDO converter to guarantee supply quality for analog circuits.

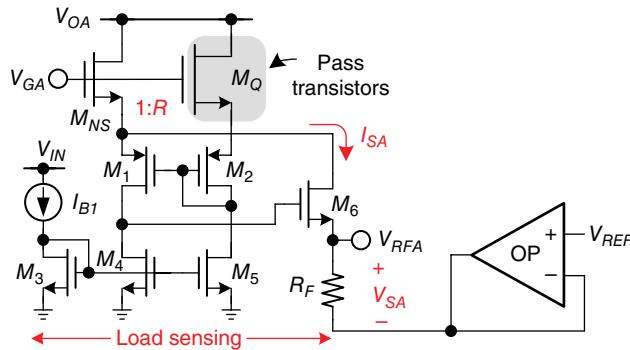
When the D/A LDO regulator is operated using the analog function, the load current condition at  $V_{OA}$  is reflected to the reference adjuster of ADVS modulation to adjust the dropout voltage dynamically, which subsequently leads to voltage ripple suppression or power conservation. If the output load condition at  $V_{OA}$  continuously decreases to an ultra-light condition, then the switchable D/A LDO regulator is switched to digital operation. Thus, the quiescent current decreases because the digital controller and the dropout voltage are minimized to enhance power efficiency further. The load-dependent technique indicates the switching procedure between analog and digital operations in the switchable D/A LDO regulator. Therefore, with the feedback control loop in the SIDO power module, the ADVS and DVS functions are achieved at  $V_{OA}$  and  $V_{OB}$ , respectively. The SIDO controller uses the current-programmed



**Figure 2.94** SIDO converter used in PMU design to deliver the advantage of a compact size solution



**Figure 2.95** Structure of the SIDO power module for dual DVS functions



**Figure 2.96** Reference adjuster in the ADVS technique

control scheme [28] to realize the energy delivery function at the power stage and ensure high power efficiency.

A schematic of the reference adjuster in ADVS is presented in Figure 2.96. The current flowing through the pass transistors must be monitored to adjust the dropout voltage dynamically in the analog LDO regulator. The load-sensing circuit obtains the supply current information. Then, the replica-sensed current  $I_{SA}$  generates the reference voltage  $V_{RFA}$  by resistor  $R_F$  to modulate the output voltage level of  $V_{OA}$  properly and achieve an optimal dropout voltage in the switchable D/A LDO regulator, which operates in the analog operation.  $V_{SA}$  reflects the dropout voltage corresponding to the loading current condition in the analog LDO regulator. That is, an adequate dropout voltage is maintained in the analog LDO regulator with regard to the loading current condition. High efficiency and PSR can be maintained in the analog LDO regulator. By contrast, the D/A switchable LDO regulator is switched to digital operation if the loading current condition is under light loads. The major reason for this procedure is to break through the limitation requested in the C-free LDO regulator. The digital operation of the D/A

LDO regulator reduces the minimum load current requirement to near zero [7]. Meanwhile, the dropout voltage is continuously minimized and the quiescent current can be reduced further to maintain high efficiency even under ultra-light loads. The switchable D/A LDO regulator ensures high efficiency over a wide load range and implements the ADVS technique in the PMU design.

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# 3

## Design of Switching Power Regulators

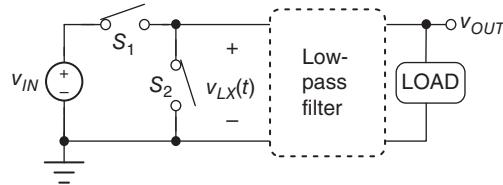
### 3.1 Basic Concept

DC/DC switching regulators (SWRs) are widely used in power management units because of their high efficiency, adjustable output voltage, and high driving capability [1–7]. Figure 3.1 shows the basic components of a DC/DC switching converter. As implied by the name “switching,” switches  $S_1$  and  $S_2$  control the amount of energy delivered from the input DC voltage source  $v_{IN}$  to the output  $v_{OUT}$ . When  $S_1$  and  $S_2$  are on and off, respectively, energy is delivered from  $v_{IN}$  to  $v_{OUT}$ . When  $S_1$  and  $S_2$  are off and on, respectively, no energy is delivered from  $v_{IN}$  to  $v_{OUT}$ . By switching  $S_1$  and  $S_2$  alternatively, the energy delivered to  $v_{OUT}$  can be adequately controlled. Next, a low-pass filter is needed to filter out the high-frequency components produced in the switching operation. The DC component, which is equal to the average value in Fourier analysis, can be similarly derived. Finally, a DC voltage is presented at  $v_{OUT}$  to provide energy to the output load.

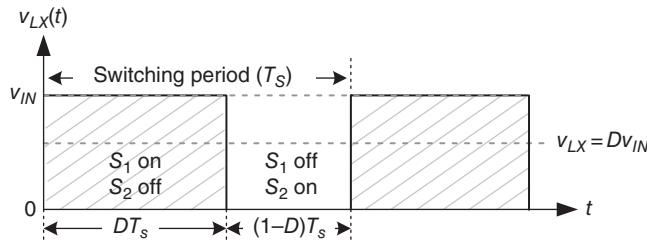
It should be mentioned here that  $S_1$  and  $S_2$  cannot be turned on concurrently, even for a very short time. Simultaneously turning on  $S_1$  and  $S_2$  drains the energy from input to ground and causes a large energy loss.

Allocating the turn-on time of  $S_1$  and  $S_2$  is an issue. When a certain output voltage for a certain load condition is required, the turn-on time ratio of  $S_1$  and  $S_2$  must remain the same to deliver constant energy to the output, no matter how many times  $S_1$  and  $S_2$  turn on alternately. First, a switching period (cycle)  $T_S$  is defined to easily achieve this. The relationship between switching frequency  $f_S$  and switching period  $T_S$  is:

$$f_S = \frac{1}{T_S} \quad (3.1)$$



**Figure 3.1** Basic components of a DC/DC switching converter



**Figure 3.2** Periodic waveforms at the switching node

The time it takes to transfer energy from input to output in a switching cycle is the so-called duty cycle or duty ratio in Eq. (3.2) for DC/DC switching converters. The duty cycle is equal to the ratio of the turn-on time of  $S_1$  to the switching period. Since the switching cycle repeats again and again, a fixed switching frequency operation occurs.

$$D = \frac{\text{Turn-on time of } S_1}{T_S} \quad (3.2)$$

The switching activity can easily be observed from the switching node  $LX$  that connects two switches  $S_1$  and  $S_2$ , as depicted in Figure 3.2. Figure 3.2 also shows the on time of  $S_1$  and  $S_2$  in a switching cycle.

As depicted in Figure 3.2, when  $S_1$  turns on,  $LX$  is connected to the supply voltage  $v_{IN}$  and  $v_{LX}(t) = V_{IN}$ , where  $V_{IN}$  is the DC component of  $v_{IN}(t)$ . When  $S_2$  is turned on,  $LX$  is pulled down to the ground at zero voltage level. The low-pass filter helps filter out high-frequency harmonics to obtain the DC component of the signal  $v_{LX}(t)$ . That is, the average value of  $v_{LX}(t)$  in a periodic duration is equal to the DC component derived from the Fourier transform analysis. The DC value of the switching node signal  $v_{LX}(t)$  is:

$$\overline{v_{LX}}(t) = \frac{1}{T_S} \int_0^{T_S} v_{LX}(t) dt = DV_{IN} \quad (3.3)$$

Given that the output voltage is equal to the average value of  $v_{LX}(t)$ , we can conclude that the output voltage is equal to the input supply voltage multiplied by the duty cycle. Therefore, we can set the output voltage of the SWR with this topology using the duty cycle as indicated in Eq. (3.4). In other words, in a fixed switching frequency operation, modulating the duty cycle

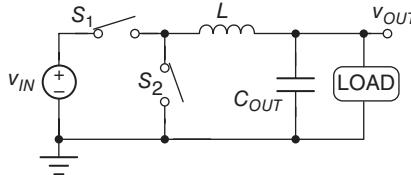
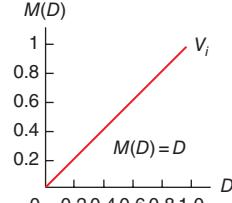
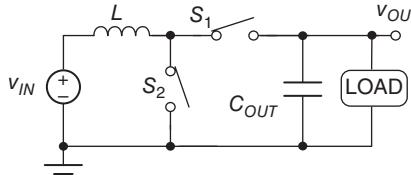
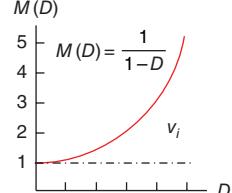
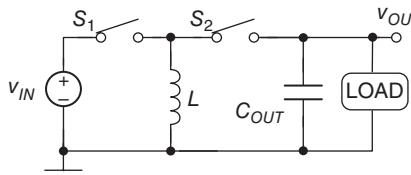
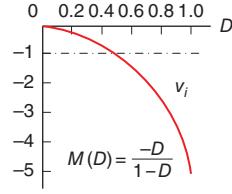
can effectively control the output voltage. This method is one of the most popular SWR control methods, called pulse width modulation (PWM).

$$D = \frac{v_{OUT}}{v_{IN}} \quad (3.4)$$

From Figure 3.2,  $D$  must take a value between 0 and 1 because  $v_{LX}(t)$  is a periodic signal. In this type of SWR, the output voltage is equal to or smaller than the supply voltage. Only the “buck” or “step-down” voltage can be obtained (compared with the supply voltage). Therefore, this topology is a buck converter. In addition, other basic topologies of the SWR include the boost and buck-boost converters. A boost converter can convert the supply voltage to a higher level, while the buck-boost converter can realize either a step-up or step-down voltage level.

Similar to a buck converter, boost and buck-boost converters are composed of switches and a filter. The filter is realized by a second-order LC filter, which contains an off-chip inductor and an off-chip capacitor. The continuity of the inductor current decides the current to *LOAD*, and the capacitor stabilizes the output voltage. A summary of the three basic inductor-based SWR topologies is shown in Table 3.1. These topologies, which contain switches and a filter, are named the power stage because the topologies can provide large amounts of power to *LOAD*. These converters can guarantee both good energy-driving capability and high power-conversion efficiency.

**Table 3.1** Summary of the three basic inductor-based SWR topologies

| Name                                | Topology  | Conversion ratio   |
|-------------------------------------|---|--|
| Buck (step-down)                    |   | $M(D) = D$                |
| Boost (step-up)                     |  | $M(D) = \frac{1}{1-D}$   |
| Boost/boost (step-up and step-down) |  | $M(D) = \frac{-D}{1-D}$  |

**Table 3.2** Comparison of distinct basic power management modules

|                  | Linear regulators | Charge pumps | Switching regulators |
|------------------|-------------------|--------------|----------------------|
| Regulation type  | Buck only         | Buck/boost   | Buck/boost           |
| Noise            | Low               | Medium       | High                 |
| Efficiency       | Low               | Medium       | High                 |
| Power capability | Medium            | Medium       | High                 |
| Footprint area   | Compact           | Moderate     | Large                |
| Cost             | Low               | Medium       | High                 |
| Complexity       | Low               | Medium       | High                 |
| EMI              | Low               | Medium       | High                 |

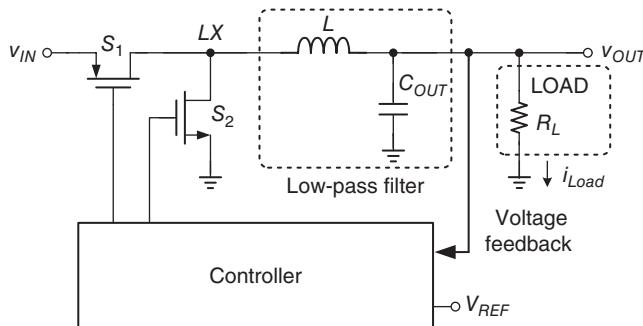
The conversion ratio represents the ability to convert the output voltage from the supply voltage. Given a certain value of the duty cycle, the output voltage can be determined by a conversion ratio, which is represented by  $M(D)$ . When  $M(D)$  is equal to one, the output voltage is equal to the supply voltage. As mentioned before, in a buck converter, the output voltage is equal to the input supply voltage multiplied by the duty cycle. Thus, the conversion ratio of the buck converter can be expressed as  $M(D) = D$ . The boost converter provides a step-up operation, in which the output voltage level is higher than the input voltage. The conversion ratio of the boost converter  $M(D)$  can be expressed as  $M(D) = 1/(1-D)$ . The buck-boost converter carries out either a step-up or a step-down operation with conversion ratio  $M(D) = -D/(1-D)$ . As a result, different power management topologies realize distinct supply functions in different applications.

A comparison of distinct basic power management modules is listed in Table 3.2. A simple low-dropout (LDO) regulator generates a ripple-free output voltage but sacrifices power-conversion efficiency. By contrast, a switching-type power management results in a switching output voltage ripple and therefore degrades the quality of the voltage supply. The output voltage ripple may result in improper operations in noise-sensitive sub-circuits. Electromagnetic interference (EMI) problems caused by switching operations need to be solved to enhance the quality of the power management module. However, its high power-conversion efficiency is the main design consideration in battery-operated electronics.

### 3.2 Overview of the Control Method and Operation Principle

As discussed in Section 3.1, the output voltages of SWRs can be controlled by a duty cycle. We discuss how to obtain the signal of the duty cycle and how SWRs generate well-regulated voltages at different load conditions.

A straightforward method is to keep detecting the output voltage and adjust the duty cycle accordingly. If the output voltage is lower than the target value, increasing the duty cycle can transfer more energy to the output. If the output voltage is higher than the target value, decreasing the duty cycle can decrease the energy transferred to the output. Therefore, the output voltage can be controlled under all load conditions or input voltage variations. Such a control method is illustrated in Figure 3.3.



**Figure 3.3** Closed-loop control method for switching buck converter

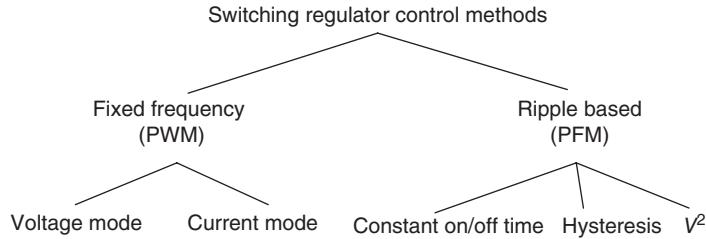
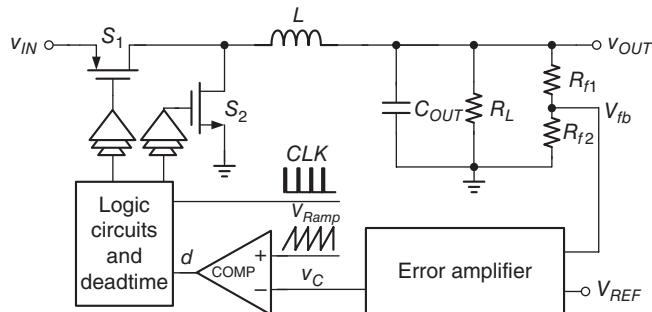
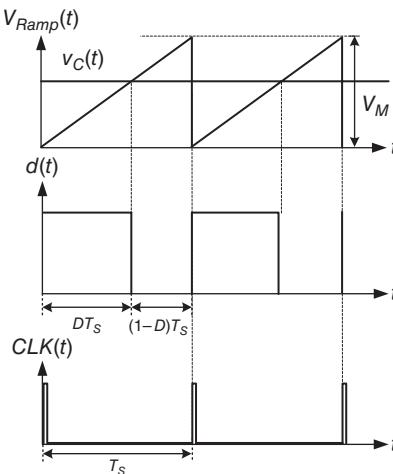
Without the controller, the output voltage is determined by a fixed duty cycle (which is preset according to the input and target output values). The energy is transferred to the output by the power stage without detecting the output voltage. This is an “open-loop control.” Load variation can result in an output voltage apart from the target voltage. By contrast, a “closed-loop control” is constructed by voltage feedback. The output voltage is regulated at the target value by adjusting the duty cycle. The closed-loop control can be viewed as a feedback system, which modifies the output impedance of the buck converter for voltage regulation.

As shown in Figure 3.3, the target output voltage is set by a reference voltage  $V_{REF}$ , which is usually generated by a bandgap circuit. The output voltage is sent to the controller, after which it forms a voltage feedback loop. The controller can adjust the duty cycle according to the amount of output voltage deviation from  $V_{REF}$ .

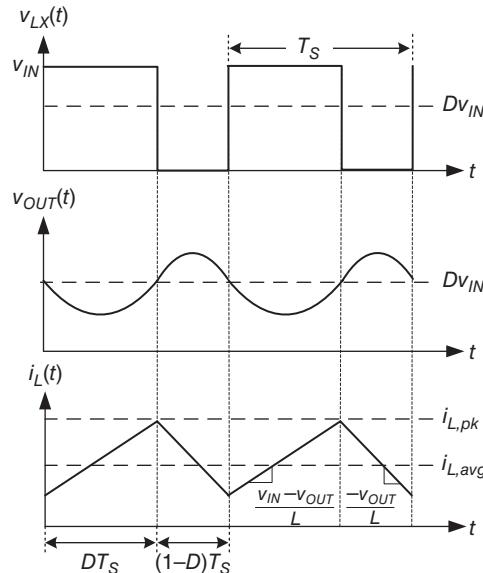
The next step is to design the controller to achieve a closed-loop control. The classification of the SWR control methods is shown in Figure 3.4. The control methods can be classified into two main categories: fixed-frequency control and ripple-based control. The fixed-frequency control is the well-known PWM, which is mentioned in Figure 3.2. A clock signal is required to define the switching frequency. The fixed-frequency control contains a voltage-mode control, which has a basic voltage feedback as illustrated in Figure 3.3 and a current-mode control, which requires additional current-sensing information. By contrast, the ripple-based control does not require a clock signal to indicate the start of each switching cycle. Instead, the switching frequency varies with the requirement of output voltage or inductor current. The ripple-based control contains constant on time, constant off time, hysteresis, and  $V$ -square ( $V^2$ ) control.

Figure 3.5 illustrates the voltage-mode controller in Figure 3.3. First, the difference between the voltage feedback  $V_{fb}$  and the reference voltage  $V_{REF}$  is required to indicate the trend of the duty cycle (i.e., increase or decrease). A single-ended error amplifier (EA), which is usually used, can generate the error signal  $v_C$  by amplifying the difference between  $V_{fb}$  and  $V_{REF}$ . Next, the duty cycle, which controls  $S_1$  and  $S_2$ , must be generated according to  $v_C$ . Through the closed-loop control,  $v_{fb}$  becomes equal to  $V_{REF}$  to achieve voltage regulation. Here,  $R_{f1}$  and  $R_{f2}$  form a voltage divider to obtain the voltage feedback signal proportional to  $v_{OUT}$ . By adjusting the ratio of  $R_{f1}$  and  $R_{f2}$ , the target output voltage can be adjusted according to  $V_{REF}$ .

To achieve fixed-frequency control, the clock signal  $CLK(t)$  defines the switching frequency and indicates the start of each switching cycle. The ramp signal  $v_{RAMP}$ , which is synchronized to  $CLK(t)$ , is required to generate the duty cycle. By comparing  $v_C(t)$  with  $v_{RAMP}(t)$ , the duty cycle

**Figure 3.4** Classification of SWR control methods**Figure 3.5** Architecture of the voltage-mode controlled buck converter**Figure 3.6** Operation waveforms of the voltage-mode buck converter

is generated as shown in Figure 3.6. By comparison,  $v_C(t)$  is converted to the duty cycle, which indicates the DC-value deviation of  $v_{OUT}(t)$  in the time domain. When  $v_{RAMP}(t)$  is smaller than  $v_C(t)$ ,  $d(t)$  is high,  $S_1$  is on, and  $S_2$  is off. When  $v_{RAMP}(t)$  is higher than  $v_C(t)$ ,  $d(t)$  is low,  $S_1$  is off, and  $S_2$  is on. This control method, which contains the output voltage feedback, is the voltage-mode control.

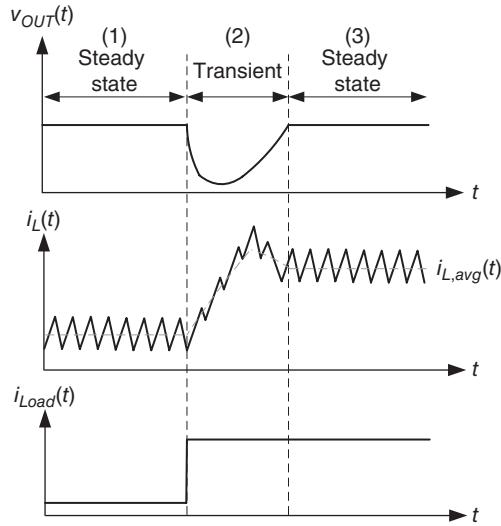


**Figure 3.7** Steady-state waveforms of the buck converter

The power-stage waveforms of the buck converter in a steady state are illustrated in Figure 3.7. In a switching cycle  $T_S$ , the switching node  $LX$  is connected to  $v_{IN}$  and ground in  $DT_S$  and  $(1-D)T_S$ , respectively. Accordingly, the voltage across the inductor  $L$  is  $v_{IN} - v_{OUT}$  and  $-v_{OUT}$ , respectively. Thus, the slope of the inductor current is  $(v_{IN} - v_{OUT})/L$  and  $-v_{OUT}/L$ , respectively. With the constant  $v_{IN}(t)$  and load condition, the system operates in a steady state.  $v_{OUT}(t)$  and  $i_L(t)$  return to the same values at the end of each switching cycle. The voltage second balance principle of  $L$  and the charge balance principle of  $C_{OUT}$  are met. Stable energy is delivered to the output, and  $v_{OUT}(t)$  is well regulated at the value of  $Dv_{IN}$ . The average inductor current  $i_{L,avg}$  is equal to the load current in the steady state.

When the load current increases, the load transient response waveforms are illustrated in Figure 3.8. In region (1) the buck converter operates in a steady state, and  $i_{L,avg}(t)$  is equal to  $i_{LOAD}(t)$ . If the load current suddenly increases in region (2), the buck converter cannot provide sufficient energy to the output, that is,  $i_{L,avg}(t)$  is less than  $i_{LOAD}(t)$ . Therefore, an undershoot voltage occurs at  $v_{OUT}(t)$ . Through the voltage feedback loop, the duty cycle starts to increase until  $v_{OUT}(t)$  recovers to its original regulated value. At this time, the buck converter operates in a steady state in region (3). The inductor current is equal to the new load current level.

When the load condition varies (i.e., load transient), the voltage-mode controlled converter can detect the perturbation at  $v_{OUT}$  through the voltage feedback loop and modulate the duty cycle to regulate  $v_{OUT}$ . When  $v_{IN}$  varies (i.e., line transient), the duty cycle must be adjusted to retain  $v_{OUT}$  at the regulated value. However, the controller can modulate the duty cycle only through the voltage feedback loop. Therefore,  $v_{OUT}$  must deviate from its original regulated

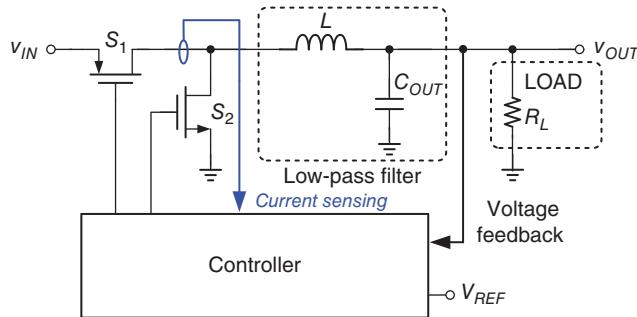


**Figure 3.8** Load transient waveforms of the buck converter

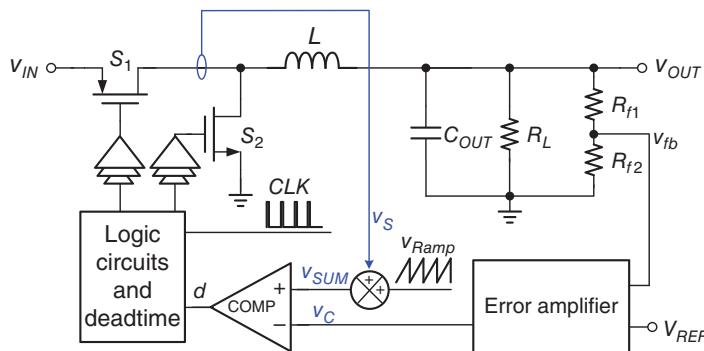
value to help adjust the error signal and duty cycle. This induces large overshoot/undershoot voltages at  $v_{OUT}$ . For instance, when  $v_{IN}$  increases,  $v_{OUT}$  also increases without adjusting the duty cycle. Next, the voltage feedback decreases  $v_C$ , thereby decreasing the duty cycle. Finally,  $v_{OUT}$  recovers to its original regulated value. Is obtaining information on  $v_{IN}$  before affecting  $v_{OUT}$  possible? The answer is obvious if another path exists to reflect the perturbation from the line voltage. That is, a feedforward technique can help improve the line transient response.

It can be noticed that the inductor current not only directly indicates different loading current conditions but also includes  $v_{IN}$  information. By sensing the inductor current, current-sensing information is added to the controller as shown in Figure 3.9. Current-sensing information can provide  $v_{IN}$  information directly before affecting  $v_{OUT}$ . In other words, current sensing provides a feedforward path to improve the performance of the line transient. With current-sensing information, this control method is called current-mode control. By contrast, voltage feedback is still required for voltage regulation because current feedback cannot obtain  $v_{OUT}$  information directly.

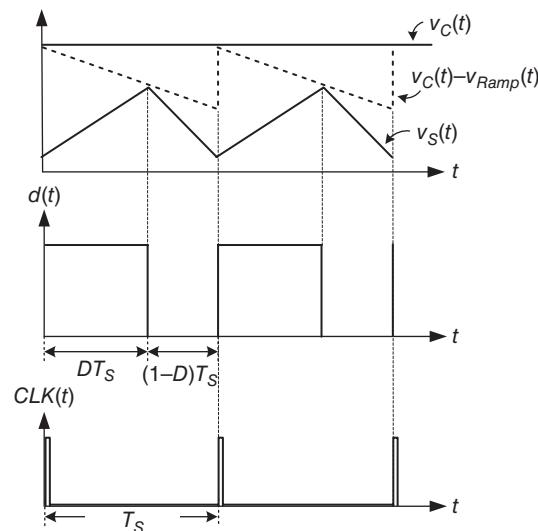
The architecture of the current-mode controlled buck converter is illustrated in Figure 3.10. Excluding the original circuit blocks in voltage-mode control, the sensed inductor current  $v_S$  is added to  $v_{RAMP}$  to generate the summation signal,  $v_{SUM}$ . Operation waveforms are illustrated in Figure 3.11. In contrast to the voltage-mode control, which compares  $v_{RAMP}(t)$  with  $v_C(t)$  to determine  $d(t)$ , the current-mode control compares the sensed inductor current  $v_S(t)$  with  $v_C(t)$  (i.e., ignoring  $v_{RAMP}(t)$  here for simplification). When  $d(t)$  is high,  $S_1$  is turned on to simultaneously increase the inductor current and  $v_S(t)$ . The duty cycle is determined when  $v_S(t)$  is equal to  $v_C(t)$ . That is, when  $v_S(t)$  reaches  $v_C(t)$ ,  $d(t)$  turns to low,  $S_1$  turns off, and  $S_2$  turns on to decrease  $v_S(t)$ . Since the duty cycle is determined by the peak value of  $v_S(t)$ , this control method is also called peak-current-mode control in conventional power electronics.



**Figure 3.9** Adding current-sensing information to the buck converter



**Figure 3.10** Architecture of the peak-current-mode controlled buck converter



**Figure 3.11** Operation waveforms of the peak-current-mode buck converter

**Table 3.3** Comparison of voltage- and current-mode controls

|                             | Voltage-mode control | Current-mode control |
|-----------------------------|----------------------|----------------------|
| Voltage feedback            | Yes                  | Yes                  |
| Current feedback            | No                   | Yes                  |
| Feedforward                 | No                   | Yes                  |
| Typical compensation method | Type III (PID)       | Type II (PI)         |

$v_{RAMP}(t)$  is required for output voltage stabilization because sub-harmonic oscillation occurs when  $D$  is larger than 0.5 in the current-mode control [8]. The condition for preventing sub-harmonic oscillation is expressed as:

$$m_a \geq \frac{v_{OUT}}{2L} \quad (3.5)$$

where  $m_a$  is the slope of  $v_{RAMP}(t)$ .

A comparison of the voltage-mode control and current-mode control is listed in Table 3.3. The corresponding compensation method is also introduced to distinguish between the advantages and disadvantages of the two control methods.

### 3.3 Small Signal Modeling and Compensation Techniques in SWR

As discussed in Section 3.2, the power stage of the buck converter can be controlled using several control methods to achieve regulation performance. These control methods include the voltage feedback and current feedforward, which form outer and inner loops, respectively. System stability is considered through modeling and small signal analysis of the power stage, controller, and whole system.

#### 3.3.1 Small Signal Modeling of Voltage-Mode SWR

As discussed above, the duty cycle is an ideal DC value according to  $v_{IN}$  and  $v_{OUT}$ . In practice, perturbation may occur in the input DC source, output loading, and circuit devices in the controller. Therefore, negative feedback control helps suppress the perturbation to present a stable and well-regulated output voltage by automatically adjusting the duty cycle. In the frequency domain, the duty cycle  $d(s)$  is expressed as in Eq. (3.6), where  $D$  represents the DC component of the duty cycle to define the DC bias point (quiescent operating point), and the AC component  $\hat{d}(s)$  indicates the small signal carried on the DC bias point. From the perspective of the converter,  $D$  indicates the duty cycle in a steady state if  $v_{OUT}$  is well regulated, while  $\hat{d}(s)$  represents a small signal variation, which contains line/load variation and noise components.

$$d(s) = D + \hat{d}(s) \quad (3.6)$$

where  $D \gg d(t)$ .

As mentioned in Section 3.1, the average value of  $v_{LX}(s)$  is equal to  $d(s)$  multiplied by  $v_{IN}$ . From the average perspective, the output voltage of the buck converter can be viewed as a fraction of  $v_{LX}(s)$  using  $L$ ,  $C_{OUT}$ , and  $R_L$ :

$$v_{OUT}(s) = d(s)v_{IN} \frac{\frac{1}{sC_{OUT}} || R_L}{sL + \frac{1}{sC_{OUT}} || R_L} \quad (3.7)$$

where  $v_{OUT}(s) = V_{OUT} + \hat{v}_{OUT}(s)$  and  $d(s) = D + \hat{d}(s)$ .

A small signal model can be obtained by removing the DC components. The small signal model and the transfer function from duty to output are shown in Figure 3.12 and Eq. (3.8), respectively. In other words, for a given operating point (i.e., input voltage  $V_{IN}$ , output voltage  $V_{OUT}$ , load resistor  $R_L$ , and duty cycle  $D = V_{OUT}/V_{IN}$ ), the small signal model of the buck-converter power stage can be expressed as in Figure 3.12. This transfer function, which represents the small signal from duty to output, is defined as the duty-to-output transfer function  $G_{vd}(s)$ :

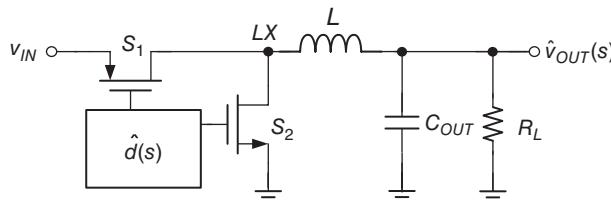
$$G_{vd}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{d}(s)} = V_{IN} \cdot \frac{1}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \quad (3.8)$$

From Eq. (3.8),  $G_{vd}(s)$  of the buck converter contains a second-order polynomial in the denominator, meaning that the filter provides two poles in the buck-converter system. Considering such a characteristic, we can rewrite Eq. (3.8) using the second-order polynomial form:

$$G_{vd}(s) = \frac{1}{1 + \frac{2\zeta s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (3.9)$$

where  $\zeta$  is the damping ratio and  $\omega_0$  is the undamped natural frequency. The damping ratio describes how oscillations decay in a system after a disturbance. The undamped natural frequency is the frequency at which a system tends to oscillate in the absence of a damping force. In DC/DC converter systems and filter engineering, the standard second-order polynomial form is usually used:

$$G_{vd}(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \quad (3.10)$$



**Figure 3.12** Duty-to-output small signal model of the buck converter power stage

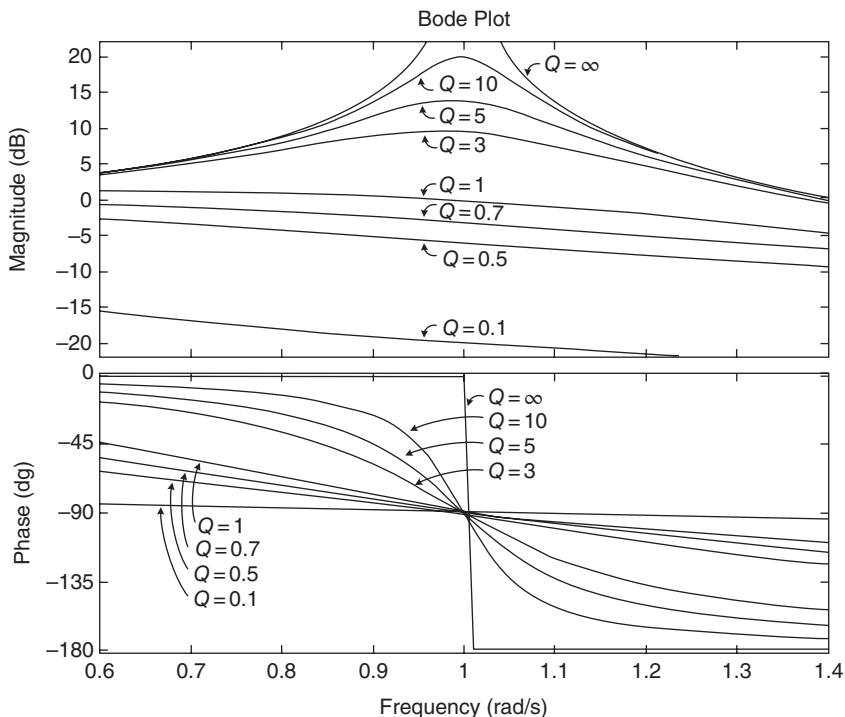
where  $Q$  is the quality factor that represents the dissipation in a system, that is, the maximum stored energy divided by the dissipated energy per cycle. Moreover, the  $Q$  factor indicates the form of two poles. If  $Q < 0.5$ , then two separate real poles exist. If  $Q > 0.5$ , then complex conjugate pairs exist. The relationship of  $\zeta$  and  $Q$  is expressed as:

$$Q = \frac{1}{2\zeta} \quad (3.11)$$

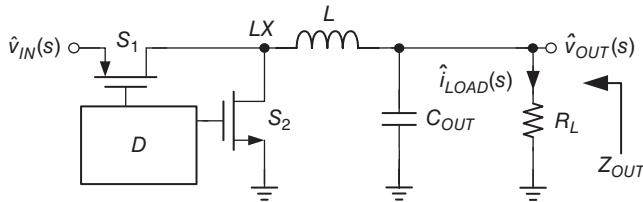
By comparing Eq. (3.8) with Eq. (3.10),  $Q$  and  $\omega_0$  can be expressed as:

$$Q = \frac{R_L}{\sqrt{\frac{L}{C_{OUT}}}} \quad \text{and} \quad \omega_0 = \frac{1}{\sqrt{LC_{OUT}}} \quad (3.12)$$

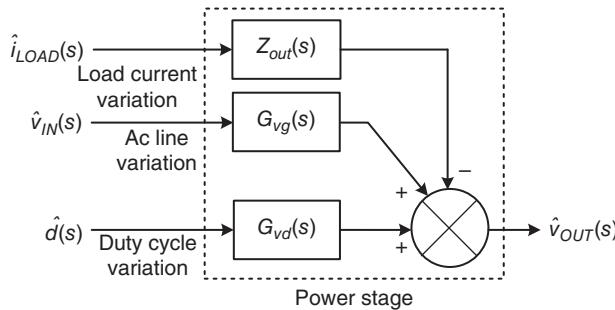
The natural frequency is determined by taking the square root of the product of the inductance and capacitance. The  $Q$  factor is related to  $R_L$ ,  $L$ , and  $C_{OUT}$ . The normalized Bode plot of Eq. (3.10) with different  $Q$  is illustrated in Figure 3.13. The natural frequencies with different  $Q$  are normalized to 1. The phase decreases from  $0^\circ$  to  $180^\circ$  because two poles exist. However, the phase shapes near  $1 \text{ rad/s}$  are different. Under a low  $Q$  condition, the two poles are separate, the phase slowly decreases, and the magnitude does not peak. Under a high  $Q$  condition, complex



**Figure 3.13** Normalized Bode plot of Eq. (3.10) with different  $Q$



**Figure 3.14** Disturbances in the power stage



**Figure 3.15** Complete power-stage model of a DC/DC converter with an open loop

conjugate poles induce peaking in magnitude, and the phase decreases dramatically at 1 rad/s. Different  $Q$  conditions greatly affect the frequency compensation for stabilizing the system.

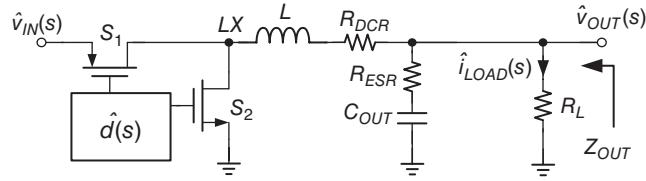
Considering all the small signal sources in the power stage, except for the duty cycle variation, the input line voltage and loading current condition variation also disturb the output voltage. The duty cycle, line, and load variation can be viewed as three small signals to the system. Therefore, the line-to-output and output impedance transfer functions are derived in Eqs. (3.13) and (3.14), respectively, to describe the disturbance as shown in Figure 3.14 (similar to the way that the duty-to-output transfer function is derived).

$$G_{vg}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{v}_{IN}(s)} = D \cdot \frac{1}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \quad (3.13)$$

$$Z_{OUT}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{i}_{LOAD}(s)} = \frac{sL}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \quad (3.14)$$

The complete model of the power stage with an open loop is illustrated in Figure 3.15. Three independent disturbance sources – duty cycle, AC line voltage, and load current variations – are present. The output voltage of the power stage can be expressed by the superposition of these three independent disturbance sources:

$$\hat{v}_{OUT}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_{IN} - Z_{OUT}(s)\hat{i}_{LOAD} \quad (3.15)$$



**Figure 3.16** Disturbances in the power stage with parasitic resistances

where the control-to-output, line-to-output, and output impedance are shown in Eqs. (3.16), (3.17), and (3.18), respectively:

$$G_{vd}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{d}(s)} \Bigg|_{\begin{subarray}{l} \hat{v}_{IN}=0 \\ \hat{i}_{LOAD}=0 \end{subarray}} \quad (3.16)$$

$$G_{vg}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{v}_{IN}(s)} \Bigg|_{\begin{subarray}{l} \hat{d}=0 \\ \hat{i}_{LOAD}=0 \end{subarray}} \quad (3.17)$$

$$Z_{OUT}(s) = \frac{\hat{v}_{OUT}(s)}{\hat{i}_{LOAD}(s)} \Bigg|_{\begin{subarray}{l} \hat{v}_{IN}=0 \\ \hat{d}=0 \end{subarray}} \quad (3.18)$$

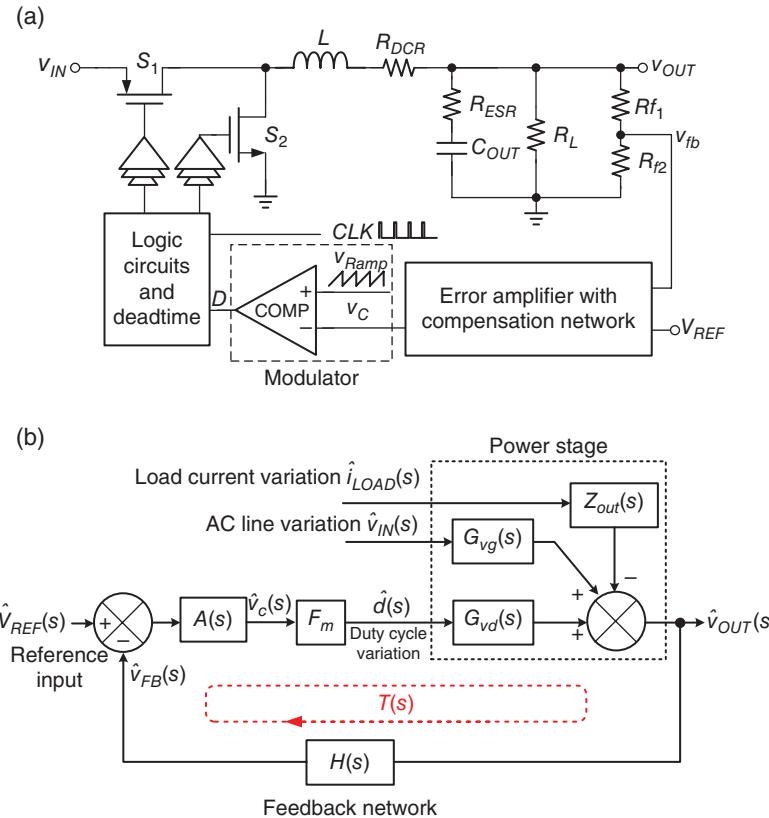
In reality, the inductor and the capacitor have their individual parasitic resistances: direct current resistance  $R_{DCR}$  and equivalent series resistance  $R_{ESR}$ , respectively. As illustrated in Figure 3.16,  $R_{DCR}$  is especially important to the efficiency evaluation and current balance in multi-phase converter applications. In addition,  $R_{ESR}$  introduces a zero and affects the frequency response. Therefore, in such applications,  $R_{DCR}$  and  $R_{ESR}$  are required to be included in  $G_{vd}(s)$ .

The parasitic  $R_{ESR}$  in  $C_{OUT}$  introduces an LHP zero, which must be considered in stability analysis. Through the derivation method of  $G_{vd}(s)$ ,  $\omega_0$  is independent of  $R_{DCR}$  and  $R_{ESR}$ . However,  $R_{DCR}$  and  $R_{ESR}$  affect the value of  $Q$ , which changes the shape of the phase near  $\omega_0$  and influences system stability. For simplicity, we usually ignore the variation in  $Q$  in frequency response analysis. Considering  $R_{ESR}$ ,  $G_{vd}(s)$  is approximately shown as:

$$G_{vd}(s) \approx V_{IN} \frac{\frac{s}{C_{OUT}R_{ESR}}}{1 + \frac{L}{R_L} + s^2LC_{OUT}} \quad (3.19)$$

### 3.3.2 Small Signal Modeling of the Closed-Loop Voltage-Mode SWR

A basic voltage-mode controlled DC/DC buck converter with all circuit blocks is shown in Figure 3.17(a). The corresponding model of the whole system is illustrated in Figure 3.17(b). The feedback network  $H(s)$ , which is composed of two feedback resistors  $R_{f1}$  and  $R_{f2}$ ,



**Figure 3.17** Voltage-mode controlled DC/DC buck converter: (a) schematic of the whole converter; (b) corresponding system model

is derived in Eq. (3.20). Using the feedback network, the output voltage information \$v\_{FB}\$ is fed back as \$H(s)v\_{OUT}\$:

$$H(s) = \frac{R_{f2}}{R_{f1} + R_{f2}} \quad (3.20)$$

The error signal between the feedback voltage \$\hat{v}\_{FB}\$ and the reference voltage \$\hat{v}\_{REF}\$ is amplified by the EA, which contains the compensation network and is represented by \$A(s)\$. The modulator compares the error signal \$\hat{v}\_C\$ with \$v\_{RAMP}\$ to generate the duty cycle, and its modulation gain is represented by \$F\_m\$. According to Figure 3.6, the transfer function from \$\hat{v}\_C\$ to \$\hat{d}\$ can be expressed as:

$$F_m = \frac{\hat{d}(s)}{\hat{v}_C(s)} = \frac{1}{V_M} \quad (3.21)$$

where \$V\_M\$ is the amplitude of the signal \$v\_{RAMP}\$.

A complete voltage-mode buck converter can be modeled as shown in Figure 3.17. Three transfer functions –  $G_{vd}$ ,  $G_{vg}$ , and  $Z_{out}$  – are defined to represent the relationships between the control input, output, and disturbances.  $G_{vd}$  is the open-loop control-to-output transfer function,  $G_{vg}$  is the open-loop line-to-output transfer function, and  $Z_{out}$  is the equivalent output impedance. The negative feedback control is used through the feedback network  $H(s)$ , compensator network  $A(s)$ , and modulator gain  $F_m$  to alleviate the variation caused by the disturbances.

The complete output voltage closed-loop expression, which considers the perturbations from the reference voltage, input source, and loading current variations, is shown in Eq. (3.22). Negative feedback can suppress the perturbation, stabilize the system, and maintain the voltage regulation. The loop gain  $T(s)$ , which is the product of the forward and feedback gains in the voltage feedback loop, is expressed as in Eq. (3.23).

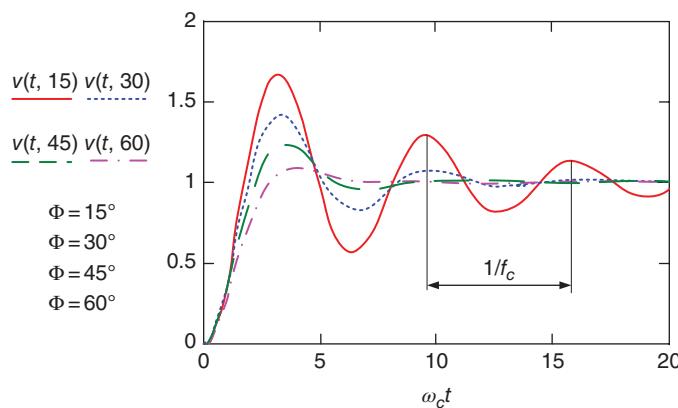
$$\hat{v}_{OUT}(s) = \hat{v}_{REF}(s) \frac{1}{H(s)} \cdot \frac{T(s)}{1+T(s)} + \hat{v}_{IN} \frac{G_{vg}(s)}{1+T(s)} - \hat{i}_{LOAD} \frac{Z_{OUT}(s)}{1+T(s)} \quad (3.22)$$

$$T(s) = G_{vd} \cdot A(s) \cdot F_m \cdot H(s) = G_{vd} \cdot A(s) \cdot F_m \text{ if } H(s) = 1 \quad (3.23)$$

The loop gain  $T(s)$  should be analyzed to design a stable buck converter. Generally, achieving high DC gain at low frequencies, a  $45^\circ$  phase margin, and at least a 10 dB gain margin is demanded. However,  $G_{vd}(s)$  contains two poles that result in a  $180^\circ$  phase delay and instability as derived in Eq. (3.19).  $A(s)$ , which has not yet been determined in the previous discussion, can adjust the DC gain and generate poles and zeros to compensate for the insufficient phase margin. The compensation methods are introduced in Section 3.3.3.

The phase margin determines the amount of ringing when the load changes. The transient responses of different phase margins are shown in Figure 3.18. For a fast transient response, a  $60^\circ$  phase margin is suitable. However, sustaining  $60^\circ$  for all input, output, and load conditions is not easy. Thus, at least  $45^\circ$  is sufficient. Note that the ringing frequency in Figure 3.18 is related to the crossover frequency  $f_c$  of  $T(s)$ .

Aside from the gain and phase margin, a high bandwidth is required to obtain a fast transient response. Most importantly, the design of the highest crossover frequency is limited within 1/5 or 1/10 of the converter switching frequency  $f_s$  to ensure that the switching noise does not increase.



**Figure 3.18** Transient response of different phase margin

### 3.3.2.1 Frequency Compensation Design in Voltage-Mode SWR

In frequency compensation design, the crucial issue is to design the transfer from the output to the control. The path from the output to the control contains the sensor gain  $H(s)$ , compensated EA  $A(s)$ , and modulation gain  $F_m$ . Thus, compensation techniques can be applied on any one of the transfer functions. For a voltage-mode buck converter, the loop transfer function  $T(s)$  can be expressed as in Eq. (3.24) if  $H(s) = 1$ . One zero and two poles perform at the power stage.  $\omega_O$  is the frequency of the double poles, which are composed of the output filter  $L$  and  $C_{OUT}$ . The equivalent series resistance zero  $\omega_{Z(ESR)} = 1/(C_{OUT}R_{ESR})$  is derived from the ESR and output filter capacitor. The Bode plot of the control-to-output transfer function  $G_{vd}(s)$  is illustrated in Figure 3.19.

$$T(s) = G_{vd}(s) \cdot F_m \cdot A(s) \quad (3.24)$$

where

$$G_{vd}(s) = V_{IN} \frac{1 + \frac{s}{\omega_{Z(ESR)}}}{1 + \frac{s}{Q\omega_O} + \frac{s^2}{\omega_O^2}}, \quad \omega_O \approx \frac{1}{\sqrt{LC_{OUT}}}, \quad \omega_{Z(ESR)} = \frac{1}{R_{ESR}C_{OUT}}, \quad Q \approx \frac{R_L}{\sqrt{\frac{L}{C_{OUT}}}}$$

Several design cases of  $A(s)$  are analyzed and discussed as follows. The frequency response and its corresponding transient response are also shown.

First, we use a proportional compensation (P-compensation). That is, the compensation network contains a low DC gain  $K_L$ , as shown in Eq. (3.25). Thus,  $T(s)$  can be expressed as in Eq. (3.26).

$$A(s) = -K_L \quad (3.25)$$

$$T(s) = F_m \cdot V_{IN} \frac{1 + \frac{s}{\omega_{Z(ESR)}}}{1 + \frac{s}{Q\omega_O} + \frac{s^2}{\omega_O^2}} \cdot (-K_L) \quad (3.26)$$

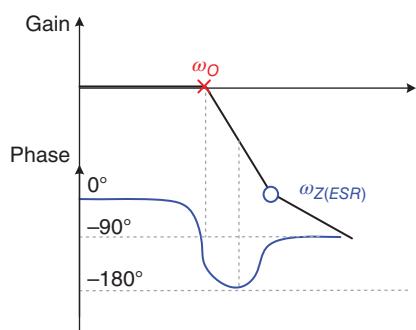


Figure 3.19 Bode plot of the power stage

The corresponding Bode plot is illustrated in Figure 3.20(a). With the low DC gain of  $K_L$  and LC double poles  $\omega_O$ , the phase margin deteriorates by  $180^\circ$  before the unit gain frequency. Although the LHP ESR zero can increase the phase margin by  $90^\circ$ , the phase margin is not improved because the ESR zero is at frequencies that are significantly higher than the unit gain frequency. The  $0^\circ$  phase margin induces an unstable operation in the buck converter. Thus, the output voltage cannot be regulated. The Bode plot from the simulation results is shown in Figure 3.20(b). High-frequency poles that inherently exist in the EA cause the  $K_L$  and phase to drop as the frequency increases. Figure 3.20(c) indicates the corresponding simulation results. The voltage-mode buck converter is not stable and oscillates between 1.32 and 1.42 V.

A simple method that ensures the stable operation of the voltage-mode buck converter without modifying  $A(s)$  is the use of an output capacitor with a high ESR value. Placing the ESR zero below the unit gain frequency can help improve the phase margin. As shown in Figure 3.21(a), if  $\omega_{Z(ESR)}$  is placed at lower frequencies, a larger phase margin can be obtained to increase the stability. As depicted in Figure 3.21(b),  $\omega_{Z(ESR)}$  is placed at three times  $\omega_O$ . The lowest phase still has  $57^\circ$  within unit gain frequency. The corresponding transient response from light to heavy load and vice versa is shown in Figure 3.21(c). The output voltage  $V_{OUT}$  is regulated near the predefined value with stable operation.

However, if any additional zeros do not improve the phase margin, then the DC gain cannot be increased to a higher level because the phase margin decreases below zero. This occurs because of the inherent high-frequency poles in the EAs. A low DC gain indicates poor load regulation and low output voltage accuracy. In addition, if the ESR zero is considered as a compensation zero to cancel the effect of double poles, then  $\omega_{Z(ESR)}$  moves toward the origin to increase the system stability. The design criterion of ESR zero is that the ESR zero must place below  $3\omega_O$  to ensure enough phase margin, since a poor phase margin results in a large ringing in case of load change. As shown in Figure 3.22, the lowest phase degrades from  $56^\circ$  to  $45^\circ$  and  $40^\circ$  if the ESR zero  $\omega_{Z(ESR)}$  changes from  $3\omega_O$  to  $4\omega_O$  and  $5\omega_O$ , respectively. If  $\omega_{Z(ESR)}$  is smaller than  $3\omega_O$ , the phase margin can be increased again to  $90^\circ$ , as shown in Figure 3.21(a).

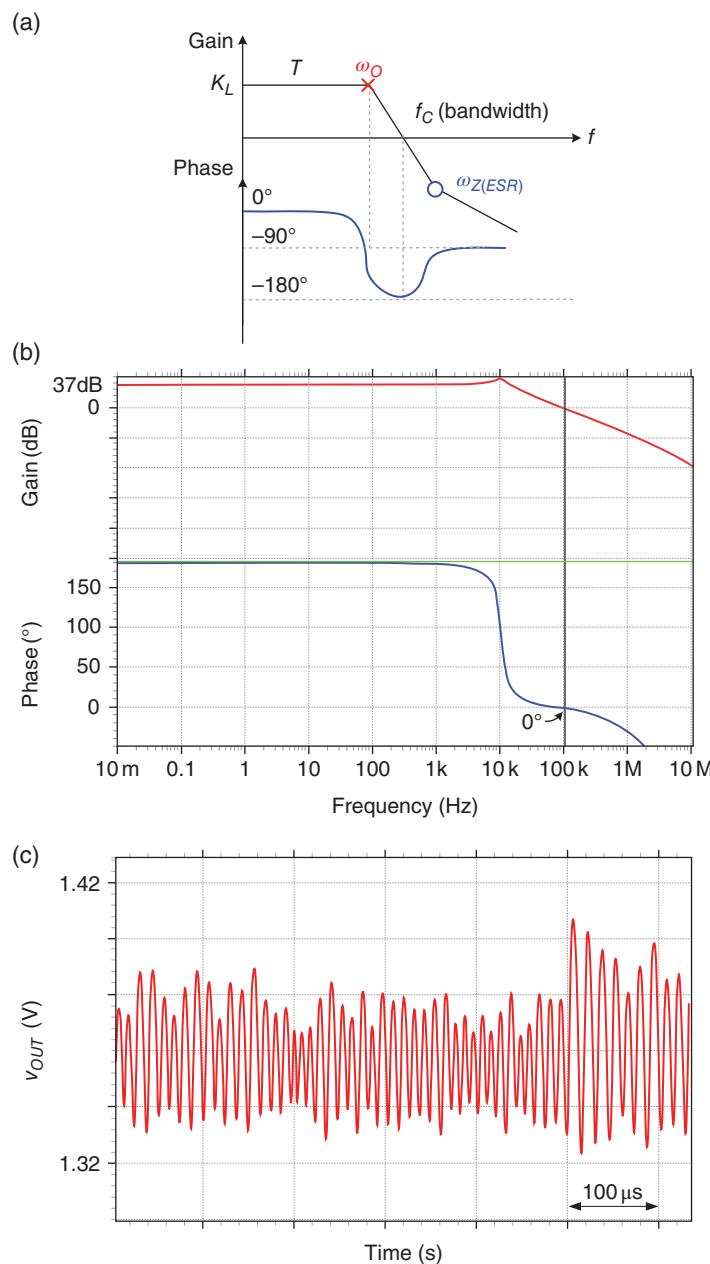
The output voltage can be well regulated by a high ESR. However,  $\omega_{Z(ESR)}$  is composed of the ESR and the output capacitor. The current flowing in or out of the capacitor induces a voltage drop across the ESR. As indicated in Figure 3.21(c), a large voltage ripple (i.e., 15 mV in the simulation) and undershoot/overshoot voltage (i.e., 33 mV in the simulation) occur because of the IR drop voltage formed by the current variations across the ESR. Using the ESR zero can certainly simplify the compensation technique at the cost of regulation performance.

To improve the regulation performance, an integrator is used to increase the DC gain as expressed in Eq. (3.27). Thus, Eq. (3.26) can be modified to Eq. (3.28) with a high DC gain of  $K_H$ .

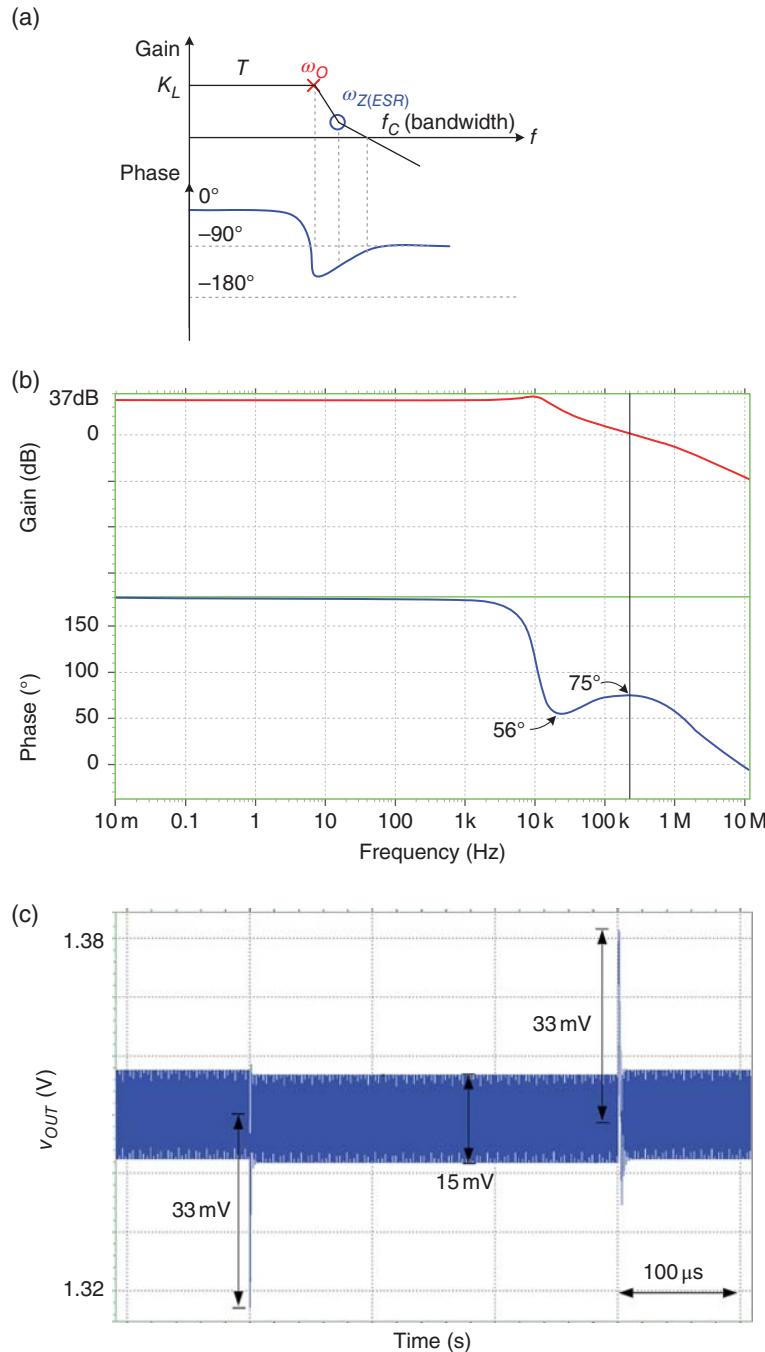
$$A(s) = -\frac{K_H}{s} \quad (3.27)$$

$$T(s) = F_m \cdot V_{IN} \frac{1 + \frac{s}{\omega_{Z(ESR)}}}{1 + \frac{s}{Q\omega_O} + \frac{s^2}{\omega_O^2}} \cdot \left( -\frac{K_H}{s} \right) \quad (3.28)$$

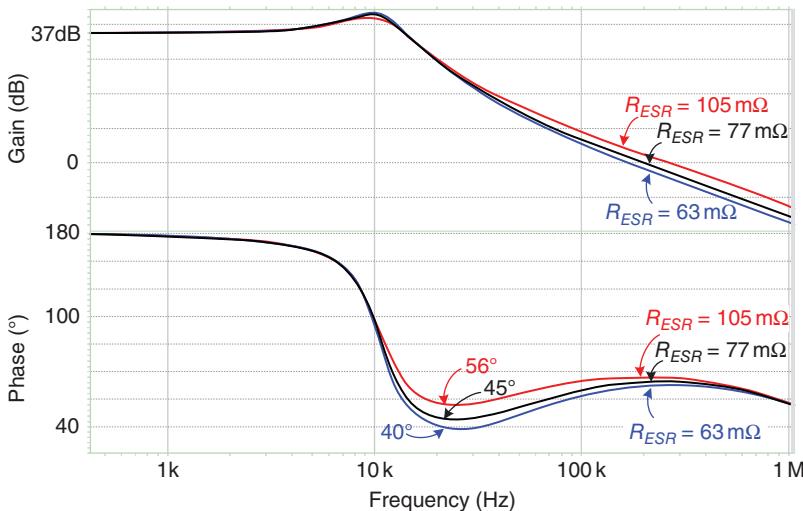
After using an integrator, the loop transfer function contains three poles according to Eq. (3.28). One pole at the origin is formed by the ideal integrator, thereby contributing a



**Figure 3.20** (a) Bode plot, (b) Bode plot by simulation results, and (c) unstable  $V_{OUT}$  in the simulation results when  $A(s) = -K_L$



**Figure 3.21** (a) Bode plot, (b) Bode plot by simulation results, and (c) simulation of  $V_{OUT}$  when  $A(s) = -K_L$  with a large ESR



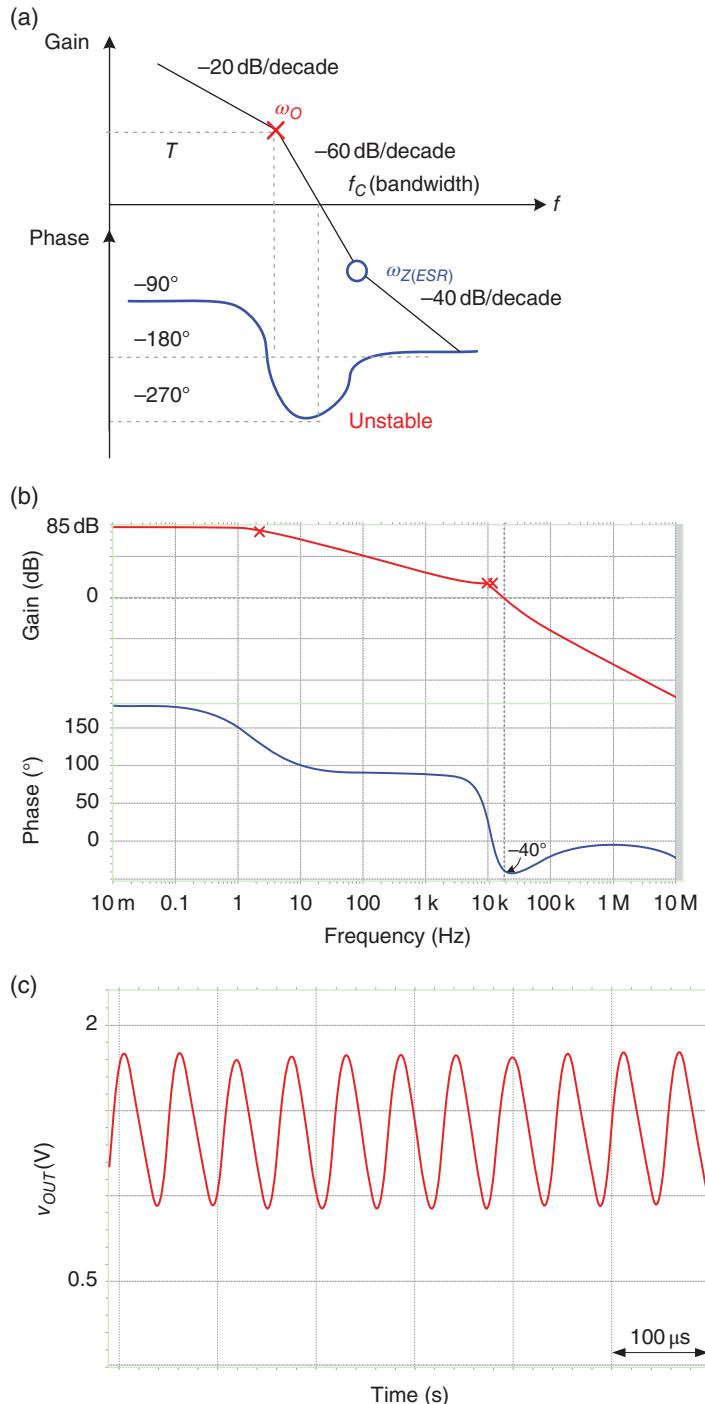
**Figure 3.22** Comparison of the Bode plots when the ESR zeros are placed at  $3\omega_O$  ( $R_{ESR} = 105 \text{ m}\Omega$ ),  $4\omega_O$  ( $R_{ESR} = 77 \text{ m}\Omega$ ), and  $5\omega_O$  ( $R_{ESR} = 63 \text{ m}\Omega$ )

90° delay. After the compensation with an ideal integrator, two possible scenarios may occur as shown in Figure 3.23.

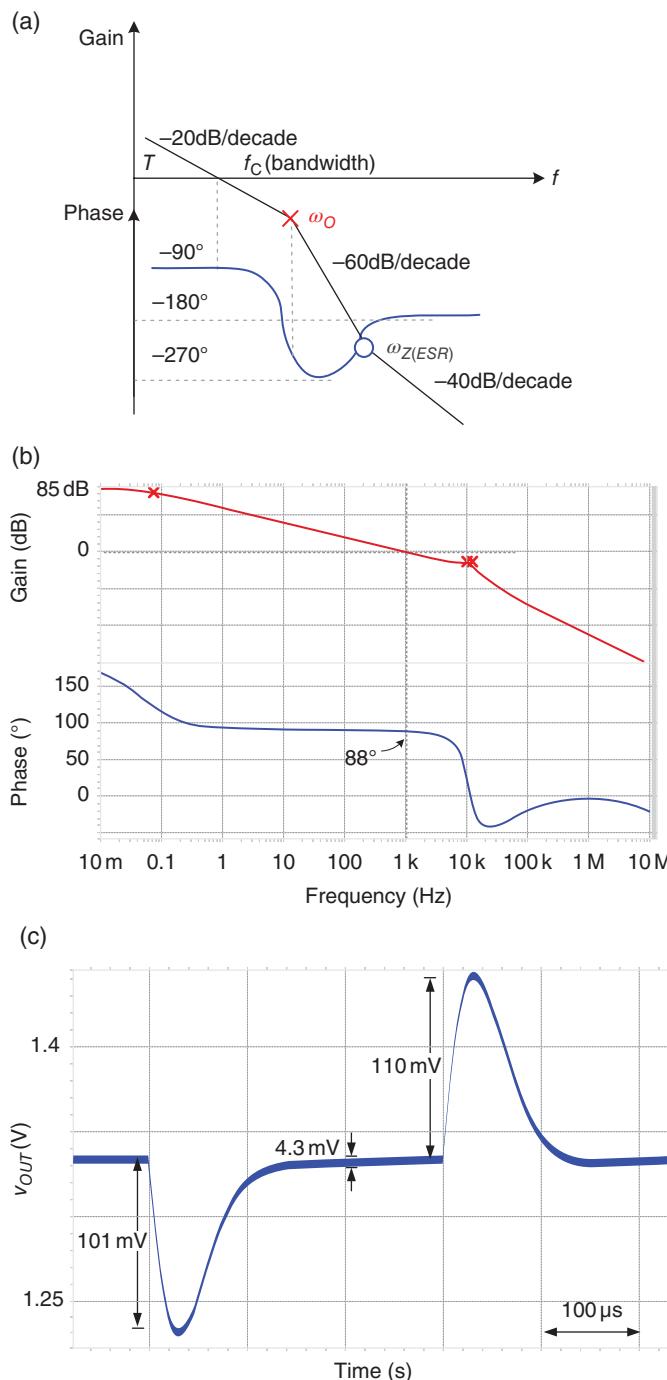
In Figure 3.23(a), if the DC gain is increased to a higher level, the system becomes evidently unstable because the phase margin is significantly lower than zero. In Figure 3.23(b), the simulated phase margin becomes  $-40 \text{ dB/decade}$ . In the simulation results, the dominant pole contributed by the integrator is not at the origin because a non-ideal EA has a limited low-frequency gain. The corresponding transient response in Figure 3.23(c) indicates an unstable output voltage. Lowering the DC gain can basically force the loop-transfer function to incur a lower crossover frequency  $f_C$  before seeing the LC double poles. Hence, if the  $f_C$  is designed to be substantially smaller than the LC double poles, the buck converter can be regarded as a one-pole system with an improved phase margin of 90°. Unfortunately, a lower DC gain degrades the output voltage accuracy, and a lower  $f_C$  slows down the transient response of the converter.

The other possible scenario is shown in Figure 3.24(a) without decreasing the DC gain; a large-compensation capacitor is placed at the output of the EA to further push the dominant pole toward the origin. As depicted in Figure 3.24(b), the phase margin becomes 88° with a relatively low bandwidth. The double poles can be viewed as high-frequency poles compared with the low bandwidth. Thus, the system becomes more stable. However, the dynamic response is sacrificed, as shown in Figure 3.24(c). For any load change, the transient recovery time is very long. This compensation method may be used to simplify the power module design in some applications where a fast transient response is not the major concern.

In summary, the two possible scenarios cannot have high DC gain and large bandwidth for regulation performance and fast transient response concurrently. To conquer these problems, two additional LHP zeros are needed below the crossover frequency  $f_C$  to increase the phase margin if a high DC gain is required at the same time. Type III compensation, which is commonly used in voltage-mode buck converters, is introduced to have two LHP zeros.



**Figure 3.23** (a) Bode plot, (b) Bode plot by simulation results, and (c) simulation of  $V_{OUT}$  with high-DC-gain EA



**Figure 3.24** (a) Bode plot, (b) Bode plot by simulation results, and (c) simulation of  $V_{OUT}$  when a large-compensation capacitor is placed at the output of a high-gain EA

Equation (3.29) depicts Type III compensation containing three LHP poles and two LHP zeros to obtain a high DC gain and a large bandwidth at the same time:

$$A(s) = -\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (3.29)$$

The corresponding frequency response is illustrated in Figure 3.25. With the help of two zeros  $\omega_{z1}$  and  $\omega_{z2}$ , the  $180^\circ$  phase delay caused by LC double poles can be compensated. The other two high-frequency compensation poles  $\omega_{p1}$  and  $\omega_{p2}$  are used to suppress high-frequency noise through the effect of  $-20$  dB/decade contributed by each pole. Since  $\omega_{z1}$  and  $\omega_{z2}$  compensate the phase delay of  $\omega_O$ ,  $T(s)$  can be viewed as a one-pole system within the bandwidth, which is unconditionally stable. In other words, high DC gain and adequate phase margin can be achieved simultaneously by Type III compensation. Usually,  $\omega_{z1}$  is placed below  $\omega_O$  to achieve the phase lead while  $\omega_{z2}$  is placed above  $\omega_O$  to decrease the phase drop. To ensure a suitable phase margin and a large bandwidth, the crossover frequency  $f_c$  is usually designed between  $\omega_{z2}$  and  $\omega_{p1}$ . To further enlarge the bandwidth, placing  $\omega_{p1}$  at the location of ESR zero,  $\omega_{Z(ESR)}$ , can effectively extend the crossover frequency and speed up the transient response. After using Type III compensation, the loop transfer function can be modified as:

$$T(s) = F_m \cdot V_{IN} \frac{1 + \frac{s}{\omega_{Z(ESR)}}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \cdot \left[ -\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \right] \quad (3.30)$$

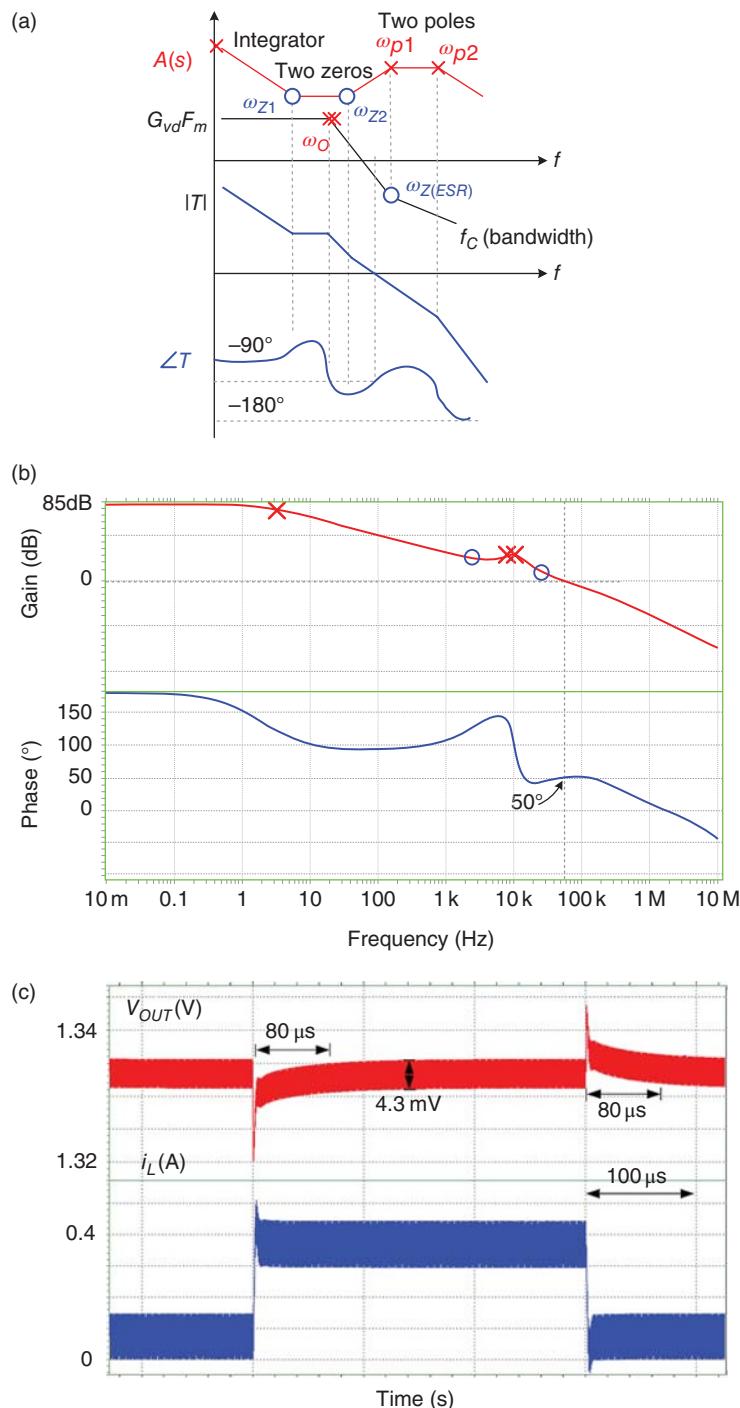
If using Type III compensation, the simulated Bode plot is shown in Figure 3.25(b). A high DC gain of  $85$  dB and  $50^\circ$  of phase margin can ensure good regulation and stable operation. As shown in Figure 3.25(c), compared with a large-compensation capacitor with high-gain EA, the transient response time of Type III compensation is much faster. Both undershoot and overshoot are much smaller. With a small ESR value, the voltage ripple is small. Zoomed-in transient responses with Type III compensation are shown in Figure 3.26.

The EA with Type III compensation is depicted in Figure 3.27, which contains input and feedback impedances  $Z_I$  and  $Z_F$ . With an ideal EA, the transfer function can be expressed by the ratio of  $Z_F$  to  $Z_I$  expressed as:

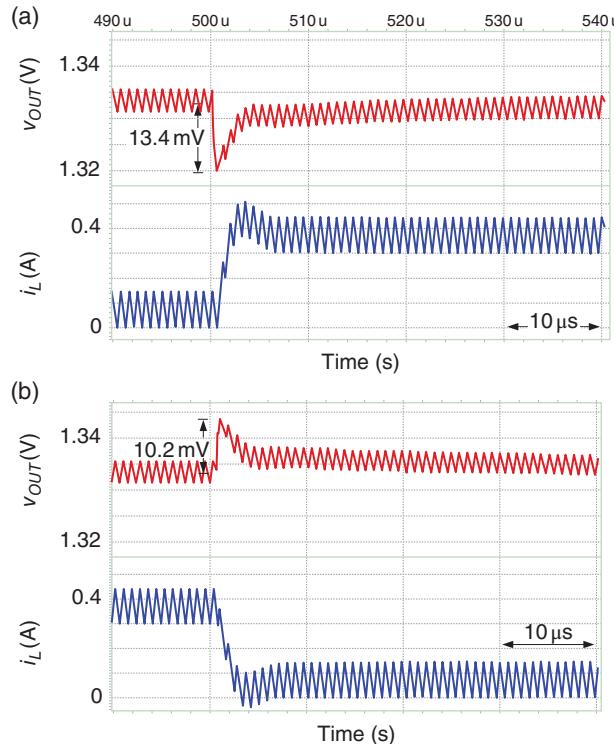
$$A(s) = \frac{\hat{v}_C}{\hat{v}_o} = -\frac{Z_F}{Z_I} \quad (3.31)$$

where

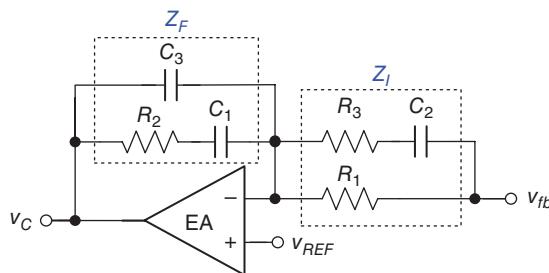
$$Z_F = \frac{1}{sC_3} \left| \left( R_2 + \frac{1}{sC_1} \right) \right| \quad \text{and} \quad Z_I = R_1 \parallel \left( R_3 + \frac{1}{sC_2} \right)$$



**Figure 3.25** (a) Bode plot, (b) Bode plot by simulation results, and (c) simulation of  $V_{OUT}$  if Type III compensation is used



**Figure 3.26** If Type III compensation is used, zoomed-in transient response is shown in case of (a) light-to-heavy load change and (b) heavy-to-light load change



**Figure 3.27** Type III compensation technique

By comparing Eq. (3.31) with Eq. (3.30), the locations of three poles and two zeros are listed as:

$$\begin{aligned} \omega_{z1} &= \frac{1}{R_2 C_1}, \quad \omega_{z2} = \frac{1}{C_2(R_1 + R_3)} \\ \omega_{p0} &= 0, \quad \omega_{p1} = \frac{1}{R_3 C_2}, \text{ and } \omega_{p2} = \frac{1}{R_2 \left( \frac{C_1 C_3}{C_1 + C_3} \right)} \approx \frac{1}{R_2 C_3} \text{ if } C_1 \gg C_3 \end{aligned} \quad (3.32)$$

To generate phase compensation near  $\omega_O$  from  $\omega_{z1}$  and  $\omega_{z2}$ ,  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$  inevitably take larger values. Since  $\omega_{p1}$  and  $\omega_{p2}$  are used to suppress the switching noise without affecting the stability,  $R_3 \ll R_1$  and  $C_3 \ll C_1$  are needed to prevent phase degradation.

The large resistor and capacitor values derived are not easily implemented with silicon. Hence, Type III includes numerous external compensation components. Cost, printed circuit board (PCB) area, and switching noise are known to significantly deteriorate the converter performance.

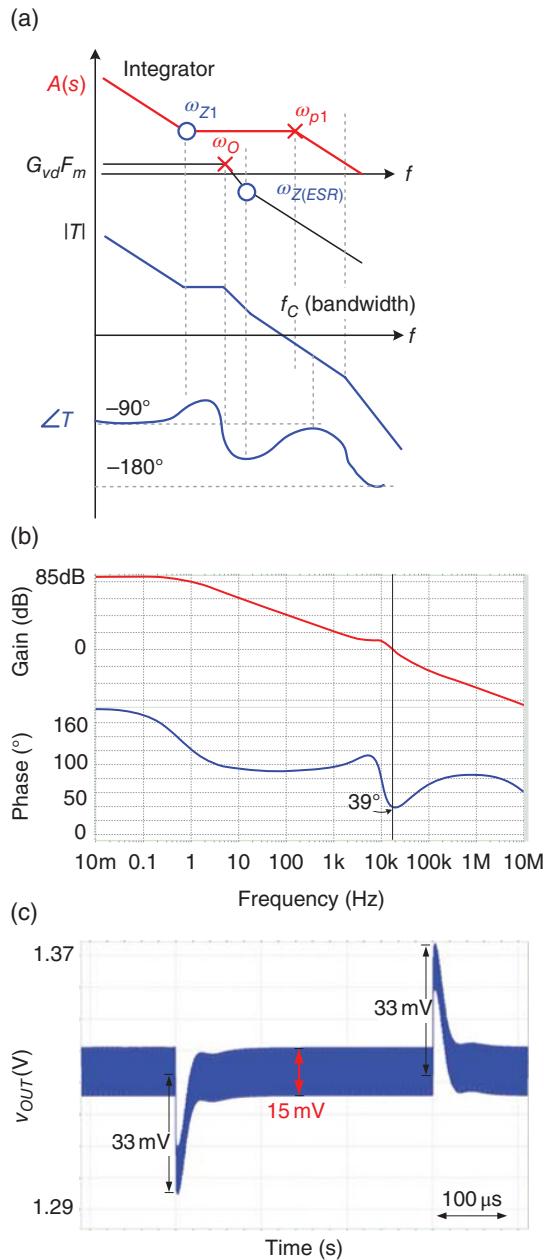
As mentioned earlier, a higher ESR value can provide a  $90^\circ$  phase lead within a crossover frequency. Here, using the ESR zero can simplify the compensation network without limiting the bandwidth. Thus, the compensation network requires only a compensation zero, a dominant pole at the origin, and a noise-suppressing high-frequency pole. In other words, Type II compensation can be used if the ESR zero is employed. The expression of Type II compensation and its corresponding  $T(s)$  are shown in Eqs. (3.33) and (3.34), respectively:

$$A(s) = -\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)} \quad (3.33)$$

$$T(s) = F_m \cdot V_{IN} \frac{1 + \frac{s}{\omega_{Z(ESR)}}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \cdot \left[ -\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)} \right] \quad (3.34)$$

The Bode plot is illustrated in Figure 3.28(a). Once more, the dominant pole is ideally at the origin.  $\omega_{z1}$  is placed below  $\omega_O$  to provide a  $90^\circ$  phase lead, and  $\omega_{ESR}$  also compensates for the phase delay caused by  $\omega_O$ . Here,  $\omega_{z1}$  and  $\omega_{ESR}$  replace the functions  $\omega_{z1}$  and  $\omega_{z2}$  in Type III compensation. An adequate phase margin can be achieved with fewer external components compared with Type III compensation. However, the output ripple is larger than that of Type III compensation because of the higher ESR, as shown in Figure 3.28(c).

Based on the discussion above, the compensation methods that stabilize the operation of buck converters can be classified into four types, as summarized in Table 3.4. A combined low DC gain and ESR zero results in the fastest transient response because of the large bandwidth. Integrator compensation requires a large-compensation capacitor, resulting in a slow transient response. Introducing two zeros by either Type III or Type II compensation with the ESR zero can increase the bandwidth with a high DC gain and shorten the transient response time. Type III compensation requires six external components that occupy a large PCB area. The corresponding detailed conditions in the simulation tool “Hspice” and the simulation results are listed and compared in Table 3.5. With a large ESR, the compensation networks are simplified at the cost of voltage ripple and undershoot/overshoot voltage performance. In terms of low voltage ripple, good transient, and regulation performances, Type III compensation is the most commonly used technique for voltage-mode buck converters. A complete architecture of the voltage-mode buck converter is illustrated in Figure 3.29.



**Figure 3.28** (a) Bode plot, (b) Bode plot by simulation results, and (c) simulation of  $V_{OUT}$  with Type II compensation and a large ESR

**Table 3.4** Comparison of different compensation methods in voltage-mode buck converters

| Method                 | $A(s)$   | Topology | Ripple/transient/regulation |
|------------------------|--|----------|-----------------------------|
| Low DC gain + ESR zero | $-K_L$   |          | Larger/fastest/poor         |
| Integrator             | $-\frac{K_H}{s}$   |          | Smaller/slowest/good        |
| Type III               | $-\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$ |          | Smaller/faster/good         |
| Type II + ESR zero     | $-\frac{K_H}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)}$   |          | Larger/faster/good          |

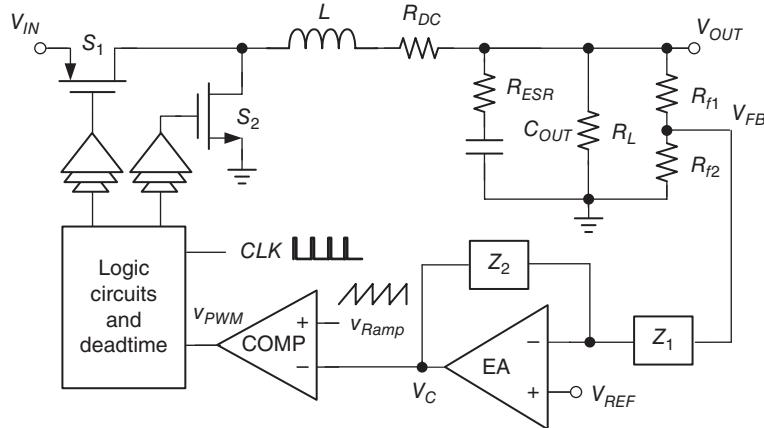
**Table 3.5** Comparison of Hspice simulation results in different compensation methods

| Method                     | Hspice conditions  | Voltage ripple (mV) | Recovery time (μs) | Overshoot/sundershoot (mV) |
|----------------------------|--|---------------------|--------------------|----------------------------|
| Low DC gain + ESR zero     | $K_L = 37 \text{ dB}$ ,<br>$R_{ESR} = 105 \text{ mΩ}$  | 15                  | 7                  | 33/33                      |
| Integrator                 | $K_H = 85 \text{ dB}$ , $C_1 = 2000 \text{ pF}$ ,<br>$R_{ESR} = 30 \text{ mΩ}$   | 4.3                 | 240                | 101/110                    |
| Type III<br>(or PID)       | $K_H = 85 \text{ dB}$ , $C_1 = 22 \text{ pF}$ ,<br>$C_2 = 68 \text{ pF}$ , $C_3 = 0.2 \text{ pF}$ ,<br>$R_1 = 100 \text{ kΩ}$ , $R_2 = 2.2 \text{ MΩ}$ ,<br>$R_3 = 1 \text{ kΩ}$ , $R_{ESR} = 30 \text{ mΩ}$ | 4.3                 | 80                 | 13.4/10.2                  |
| Type II (or PI) + ESR zero | $K_H = 85 \text{ dB}$ , $C_1 = 150 \text{ pF}$ ,<br>$C_2 = 0.2 \text{ pF}$ , $R_1 = 150 \text{ kΩ}$ ,<br>$R_{ESR} = 105 \text{ mΩ}$  | 15                  | 88                 | 33/33                      |

$L = 4.7 \mu\text{H}$ ,  $C_{OUT} = 47 \mu\text{F}$ ,  $f_s = 1 \text{ MHz}$ ,  $R_L = 18/3.6 \Omega$  (light/heavy load).

### 3.3.3 Small Signal Modeling of Current-Mode SWR

The design of the compensation network for the voltage-mode buck converter is complex because of its complex poles at the power stage. The input voltage feedforward technique for improving the line transient response further increases the complexity of the design.



**Figure 3.29** Complete architecture of the voltage-mode buck converter

In addition, another current sensor is required to achieve an over-current protection (OCP) function, which is necessary in the power management unit to increase reliability. Therefore, we consider what kind of control technique can address the problem met by the voltage-mode control technique. The current-mode control is one solution that is popular in present power management circuits. Current sensing inherently exists in current-mode controlled converters, as illustrated in Figure 3.10. With the sensed inductor current, the input voltage information is obtained simultaneously. The control system and compensation network are simpler in current-mode control techniques than in voltage-mode control techniques.

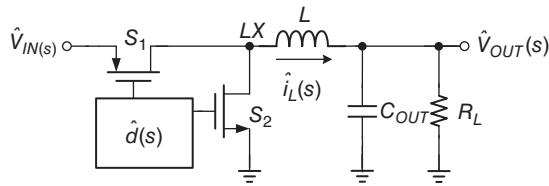
Before discussing frequency compensation in current-mode control buck converters, small signal modeling is again derived. The power-stage model of the buck converter, including  $G_{vd}$  and  $G_{vg}$ , has already been derived in Figure 3.15. However, the transfer functions represent only the duty-to-output and input-to-output characteristics. In the current-mode control, a transfer function and a model related to the inductor current are required. Here, duty-to-current and input-to-current transfer functions must be derived. Figure 3.30 illustrates the derivations of small signal models for duty-to-current and input-to-current transfer functions.

With the average concept,  $i_L$  can be expressed as  $V_{LX}$  divided by the impedance, as seen by  $V_{LX}$  to ground in Eq. (3.35). The DC quiescent operating point and perturbation for each signal are expressed in Eq. (3.36).

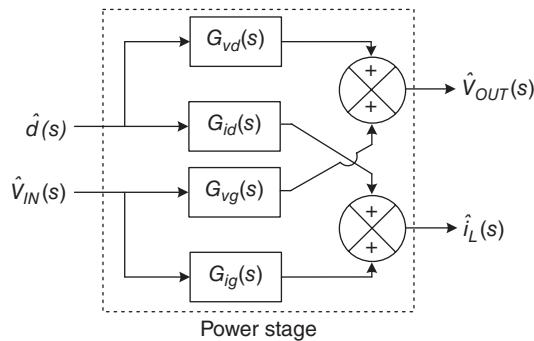
$$i_L(s) = d(s) \cdot v_{IN}(s) \cdot \frac{1}{sL + \frac{1}{sC_{OUT}}||R_L} \quad (3.35)$$

$$i_L(s) = I_L + \hat{i}_L(s), v_{IN}(s) = V_{IN} + \hat{v}_{IN}(s), \text{ and } d(s) = D + \hat{d}(s) \quad (3.36)$$

Following Eqs. (3.35) and (3.36), the duty-to-current and line-to-current transfer functions, defined as  $G_{id}(s)$  and  $G_{ig}(s)$ , respectively, can be obtained in Eqs. (3.37) and (3.38).



**Figure 3.30** Small signal model of the buck converter power stage for the derivation of the duty-to-current and input-to-current transfer functions



**Figure 3.31** Complete power-stage model of a DC/DC converter (open loop)

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{IN}}{DR_L} \cdot \frac{1}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \quad (3.37)$$

$$G_{ig}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{IN}(s)} = \frac{D}{R_L} \frac{1}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \quad (3.38)$$

By combining Figure 3.15 with Eqs. (3.37) and (3.38), the complete power-stage model of a DC/DC converter, including  $i_L$ , is illustrated in Figure 3.31.

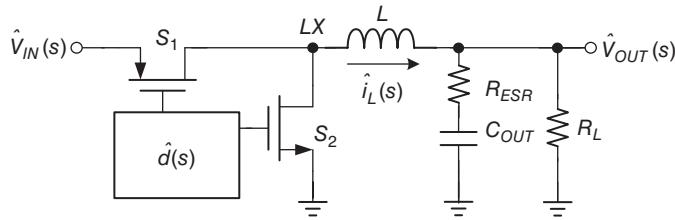
The output voltage of a power stage can be expressed in Eq. (3.39) by the superposition of two independent disturbance sources. Similarly, the inductor current of the power stage can be expressed in Eq. (3.40) by the superposition of two independent disturbance sources.

$$\hat{v}_{OUT}(s) = G_{vd}(s) \cdot \hat{d}(s) + G_{vg}(s) \cdot \hat{v}_{IN} \quad (3.39)$$

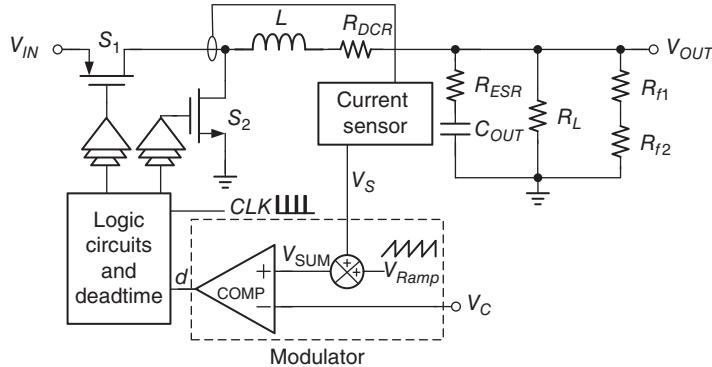
$$\hat{i}_L(s) = G_{id}(s) \cdot \hat{d}(s) + G_{ig}(s) \cdot \hat{v}_{IN} \quad (3.40)$$

where control-to-current and line-to-current are shown in Eqs. (3.41) and (3.42), respectively.

$$G_{id}(s) = \left. \frac{\hat{i}_L(s)}{\hat{d}(s)} \right|_{\hat{v}_{IN}=0} \quad (3.41)$$



**Figure 3.32** Disturbances in the power stage with parasitic resistances



**Figure 3.33** Current-mode controlled DC/DC buck converter with the current-sensing loop closed

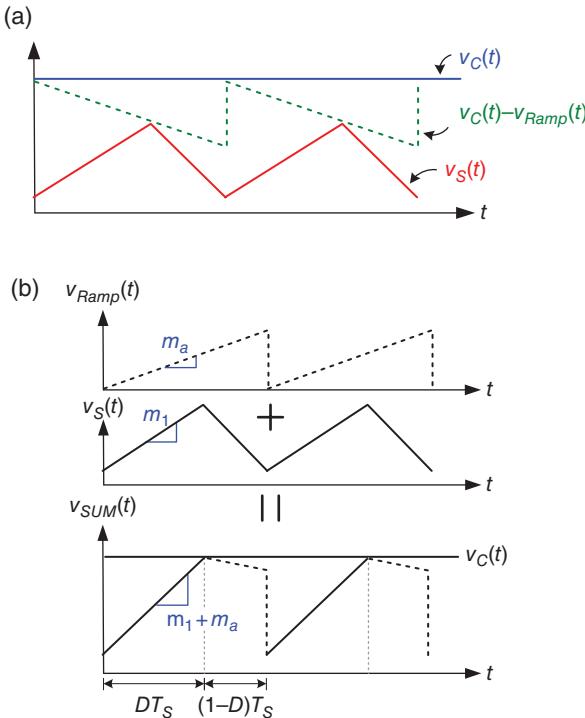
$$G_{ig}(s) = \left. \frac{\hat{i}_L(s)}{\hat{V}_{IN}(s)} \right|_{\hat{d}=0} \quad (3.42)$$

Furthermore, in Figure 3.32, if the ESR value of the output capacitor is considered and the  $R_{DCR}$  of the inductor is neglected, then Eqs. (3.37) and (3.38) are modified to Eqs. (3.43) and (3.44), respectively, with an ESR zero.

$$G_{id}(s) \approx \frac{V_{IN}}{DR_L} \cdot \frac{1 + \frac{s}{C_{OUT}R_{ESR}}}{1 + s\frac{L}{R_L} + s^2LC_{OUT}} \quad (3.43)$$

$$G_{ig}(s) \approx \frac{D}{R_L} \cdot \frac{1 + \frac{s}{C_{OUT}R_{ESR}}}{1 + s\frac{L}{R_L} + s^2LC_{OUT}} \quad (3.44)$$

Figure 3.33 shows a current-mode controlled DC/DC buck converter with the current-sensing loop closed. The inductor current is sensed by the current sensor and added to  $V_{RAMP}$  to generate the summation signal  $V_{SUM}$ . By comparing  $V_{SUM}$  with  $v_C$ , the duty cycle is generated. In contrast to voltage-mode control, the slope of  $V_{RAMP}$  should follow the inequality of



**Figure 3.34** Operation waveforms of the peak current-mode buck converter: (a)  $v_S$  compared with the subtraction result of  $v_C$  and  $V_{RAMP}$  to determine the duty and (b)  $v_{SUM}$ , which is the summation of  $v_S$  and  $V_{RAMP}$ , compared with  $v_C$  to determine the duty

Eq. (3.5) to prevent sub-harmonic oscillation. Here, the control signal  $v_C$  can be temperately viewed as a current reference voltage that controls the peak current of the buck converter.  $v_C$  can sometimes be used to stand for the approximate output loading current.

The operation waveform is usually illustrated as in Figure 3.34(a). The duty cycle is intuitively determined when the peak of the sensed inductor current  $v_S$  reaches the control signal  $v_C$ . To avoid sub-harmonic oscillation,  $V_{RAMP}$  is introduced for slope compensation. Instead, the duty cycle is determined when the peak of  $v_S$  reaches  $v_C - V_{RAMP}$ . To simplify the derivation of the current-mode control model, the three signals  $v_C$ ,  $V_{RAMP}$ , and  $v_S$  are combined and illustrated in a different manner, as shown in Figure 3.34(b). The slope of  $V_{RAMP}$ , which suppresses sub-harmonic oscillation, is  $m_a$ , while the slope of  $v_S$  is  $m_1$ , which is proportional to  $v_{IN} - v_{OUT}$ . By combining  $V_{RAMP}$  and  $v_S$ , the slope  $v_{SUM}$  is equal to  $m_1 + m_a$  before  $v_{SUM}$  reaches  $v_C$ .  $m_1 + m_a$  helps determine the duty cycle in the current-mode control.

Using the same derivation concept as  $F_M$  in voltage-mode control, the modulation gain is the reciprocal of the ramp amplitude  $V_M$ . Here, given that the slope during  $(1 - D)T_S$  does not involve duty cycle determination, the effective amplitude of  $V_M$  can be viewed as  $(m_1 + m_a) T_S$ . The modulation gain is then derived in Eq. (3.45), where  $M$  is used to indicate the ratio of the compensation slope  $m_a$  and the inductor current charging slope  $m_1$ , as shown in

Eq. (3.46). The characteristic of the current-mode control will be completely different, if different  $M$  values are applied in Eq. (3.45), as discussed later.

$$F_m = \frac{\hat{d}(s)}{\hat{v}_C(s)} = \frac{1}{V_M} = \frac{1}{(m_1 + m_a)T_S} = \frac{1}{Mm_1 T_S} \quad (3.45)$$

$$M = 1 + \frac{m_a}{m_1} \quad (3.46)$$

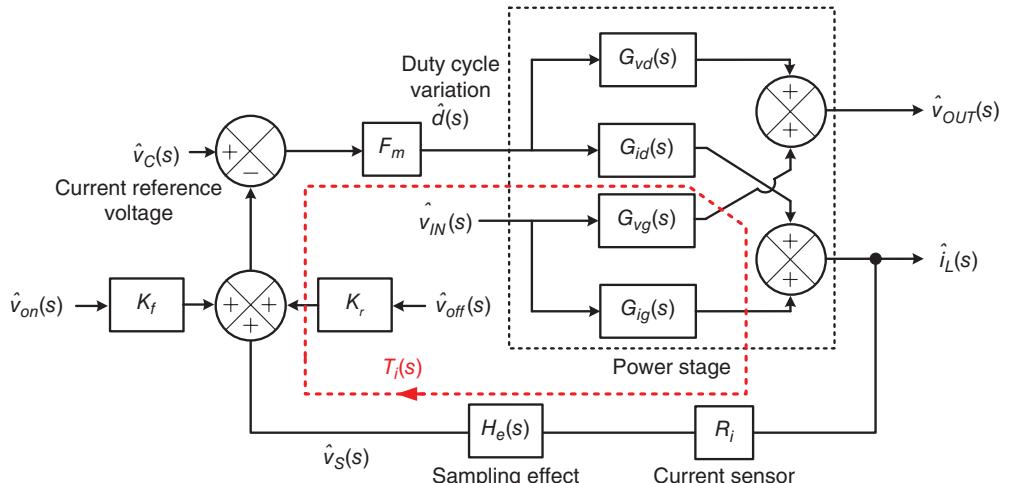
Figure 3.35 shows the current-mode control equivalent model with the current loop closed. The current sensor, which senses the inductor current value  $I_L$  and converts it to the voltage signal  $V_S$ , has a transfer function of resistance  $R_i$ , as shown in Eq. (3.47). If the switching frequency is constant, the current-mode control in PWM can be considered a sample-and-hold system with the sampling instant occurring at  $DT_s$  [9]. Thus, the current sampling effect is modeled and converted into a continuous-time representation as shown in Eq. (3.48), where  $H_e(s)$  contains two RHP zeros. In this analysis,  $H_e(s)$  is accurate from 0 to half of the switching frequency.

$$R_i = \frac{v_S}{i_L} \quad (3.47)$$

$$H_e(s) \approx \frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q_n} + 1 \quad (3.48)$$

where

$$Q_n = -\frac{2}{\pi} \text{ and } \omega_n = \frac{\pi}{T_s}$$



**Figure 3.35** Current-mode control equivalent model with current loop closed

The  $K_f$  and  $K_r$  listed in Eqs. (3.49) and (3.50), respectively, provide the feedforward voltage across the inductor during on-time and off-time periods, respectively [9]. During on-time and off-time periods, the voltage across the inductor is  $v_{IN} - v_{OUT}$  and  $v_{OUT}$ , respectively.

$$K_f = -\frac{DT_s R_i}{L} \cdot \left(1 - \frac{D}{2}\right) \quad (3.49)$$

$$K_r = \frac{(1-D)^2 T_s R_i}{2L} \quad (3.50)$$

The perturbations on the on- and off-time periods are  $\hat{v}_{on}$  and  $\hat{v}_{off}$ , respectively, as shown in Eqs. (3.51) and (3.52), respectively, and affect the duty cycle.

$$\hat{v}_{on} = \hat{v}_{IN} - \hat{v}_{OUT} \quad (3.51)$$

$$\hat{v}_{off} = \hat{v}_{OUT} \quad (3.52)$$

The current-mode control in Figure 3.35 contains a current loop with the transfer function  $T_i(s)$ . By comparing the sensed inductor current with the current reference voltage, the duty cycle can be obtained by the modulator. At the power stage, the inductor current is generated according to the duty cycle. The current loop gain  $T_i(s)$  is derived as:

$$T_i(s) = \frac{LR_i}{R_L(1-D)T_s M} \cdot \frac{1 + \frac{s}{C_{OUT}R_{ESR}}}{1 + s \frac{L}{R_L} + s^2 LC_{OUT}} \cdot H_e(s) \quad (3.53)$$

The control-to-output transfer function is desirable in demonstrating the characteristic of the current-mode control. With the closed current loop  $T_i(s)$ , the current-mode control-to-output transfer function is derived in Eq. (3.54).  $F_p(s)$  and  $F_h(s)$  are shown in Eqs. (3.55) and (3.56), respectively.

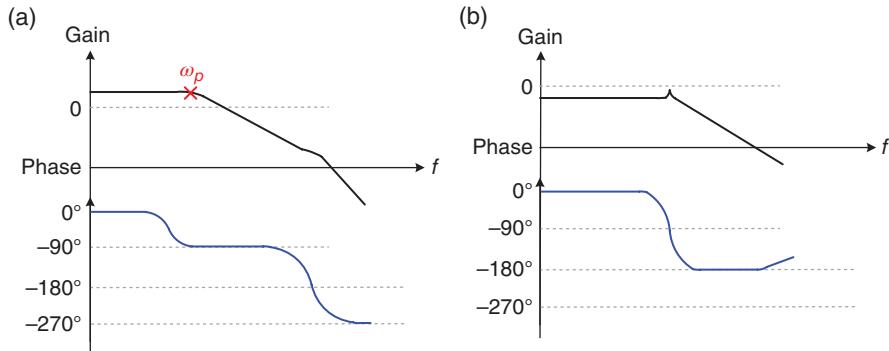
$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx \frac{D \cdot \left[M(1-D) - \left(1 - \frac{D}{2}\right)\right]}{\frac{L}{R_L T_s} + M(1-D) - 0.5} \cdot F_p(s) \cdot F_h(s) \quad (3.54)$$

$$F_p(s) = \frac{1 + s C_{OUT} R_{ESR}}{1 + \frac{s}{\omega_p}} \quad (3.55)$$

where

$$\omega_p = \frac{1}{R_L C_{OUT}} + \frac{T_s}{LC} \cdot [M(1-D) - 0.5]$$

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2}} \quad (3.56)$$



**Figure 3.36** Bode plot of the current-mode control-to-current (a) with an appropriate small value of  $M$  and (b) with a large value of  $M$

where

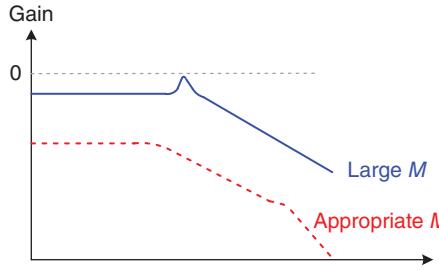
$$Q = \frac{1}{\pi[M(1-D)-0.5]}$$

Figure 3.36 illustrates the Bode plots of the current-mode control-to-current in two different cases. The typical characteristic of current-mode control is shown in Figure 3.36(a) with an appropriate small value of  $M$ . That is,  $m_a$  is equal to  $m_2$ , which follows Eq. (3.5). The DC loop gain is larger than zero to regulate the inductor current value. The control-to-current transfer function contains one dominant pole contributed by  $\omega_p$ . It is worth mentioning that  $\omega_p$  is approximately equal to  $1/R_L C_{OUT}$  with a small value of  $M$ . In other words, the current-mode control buck converter can be viewed as a one-pole system whose dominant pole is located at the output and is contributed by  $R_L$  and  $C_{OUT}$ . With only one pole, the compensation design is much simpler than that in voltage-mode control and is a useful approximation when designing and simulating.

However, a large value of  $M$  indicates a large compensation slope and the possible formation of complex poles, because  $\omega_p$  moves slightly toward higher frequencies and one of the high-frequency poles moves toward low frequencies. Since a large  $M$  represents a ratio of compensation slope much larger than the sensed inductor current, the current information is largely suppressed. Thus, the DC gain drops below zero. The characteristic of typical current-mode control disappears. With a large compensation slope, the current sensed signal is ignored. Therefore, the duty cycle is merely determined by comparing  $v_C$  with  $V_{RAMP}$ , which is similar to the voltage-mode control method and coincides with complex poles existing in the voltage-mode controlled buck converter. With an excessively large  $M$  indicating a large compensation slope, the current-mode control degenerates to the voltage-mode control.

By contrast, the line-to-output transfer function can be used to demonstrate the characteristic of the line transient response. The line-to-output transfer function in the current-mode control is derived as:

$$\frac{\hat{v}_{OUT}}{\hat{v}_{IN}} = \frac{D \cdot \left[ M(1-D) - \left( 1 - \frac{D}{2} \right) \right]}{\frac{L}{R_L T_S} + M(1-D) - 0.5} \cdot F_p(s) \cdot F_h(s) \quad (3.57)$$



**Figure 3.37** Comparison of the line-to-output transfer function in the current-mode control with appropriate small and large values of  $M$

Figure 3.37 illustrates a comparison of the current-mode line-to-output transfer function with an appropriate small value and large value of  $M$ . The line-to-output transfer function can indicate the input noise suppression ability of converters. With an appropriate value of  $M$ , low DC gain can largely suppress input-voltage perturbation. In contrast, with a larger value of  $M$ , high DC gain deteriorates the ability of input-voltage perturbation suppression. Furthermore, it coincides with the advantage of the current-mode control in terms of good line regulation performance because it has inherent feedforward characteristics. On the contrary, poor input-voltage perturbation suppression occurs in the voltage-mode control buck converters because input information does not directly feed into the voltage-mode controller.

### 3.3.3.1 Frequency Compensation Design in Current-Mode SWR

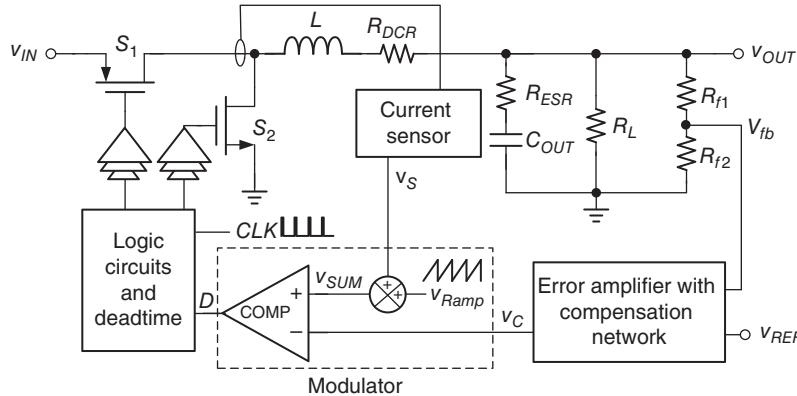
In deriving a small signal model of the current loop, the control signal  $v_C$  can be moderately considered a current reference voltage that controls the peak current of a buck converter. In reality, the current reference needs to be adjusted according to different output loading conditions. To generate a dynamic current reference voltage, the output voltage is fed back for comparison with the reference voltage  $V_{REF}$ , as shown in Figure 3.38. When  $v_{OUT}$  is lower than  $V_{REF}$ , the inductor current  $I_L$  is smaller than the output loading current  $i_{LOAD}$ . A lower  $v_{OUT}$  also causes the output voltage to drop. Therefore, the dynamic increase in the current reference can increase  $i_L$  to meet the requirement of  $i_{LOAD}$ . Through the voltage feedback loop, current reference generation and voltage regulation can be achieved simultaneously.

With voltage feedback, the current-mode model in Figure 3.35 can be modified to that in Figure 3.39. The control-to-output transfer function has previously been derived in Eq. (3.54). Hence, the equivalent model of the complete current-mode model with voltage feedback loop can be simplified as shown in Figure 3.40.

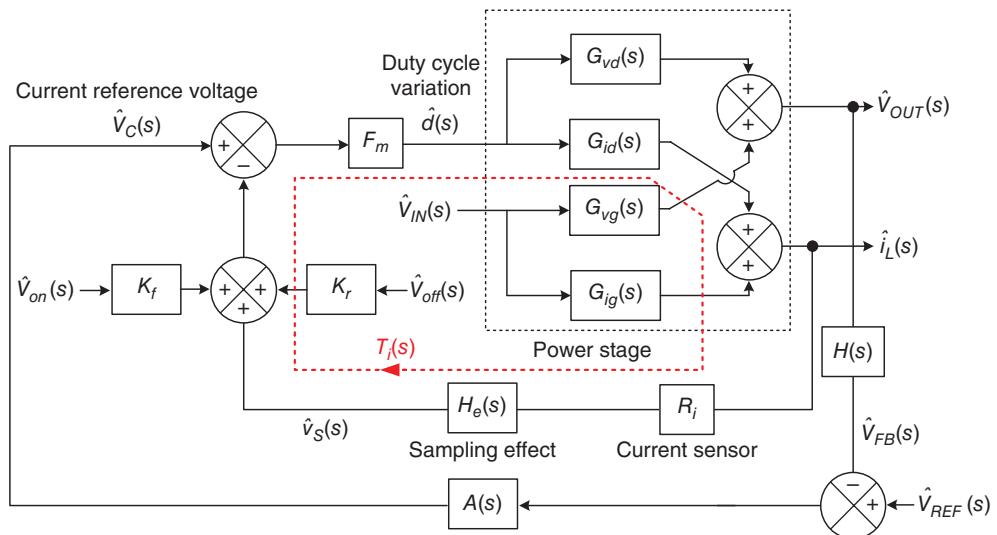
Using the simplified model, the approximate  $T(s)$  in Figure 3.40 can easily be obtained:

$$T(s) \approx \frac{\hat{v}_{OUT}(s)}{\hat{v}_C(s)} \cdot A(s) = K \cdot \frac{1 + sC_{OUT}R_{esr}}{1 + \frac{s}{\omega_p}} \cdot A(s) \quad (3.58)$$

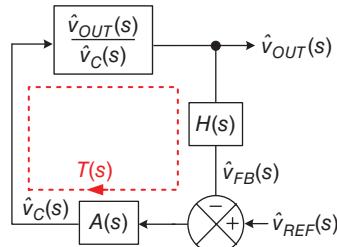
where  $\omega_p \approx \frac{1}{R_L C_{OUT}}$  and  $K$  represents the DC gain derived in Eq. (3.54).



**Figure 3.38** Current-mode controlled DC/DC buck converter with the current-sensing closed loop and outer voltage feedback loop



**Figure 3.39** Complete current-mode model with voltage feedback loop

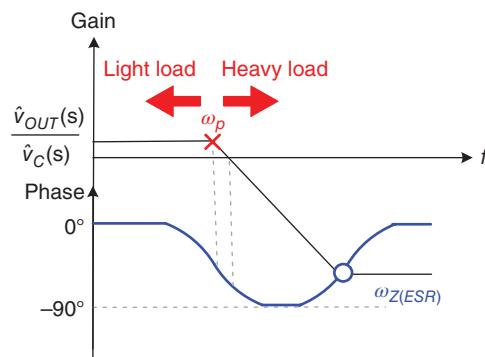


**Figure 3.40** Equivalent model of the complete current-mode model with voltage feedback loop

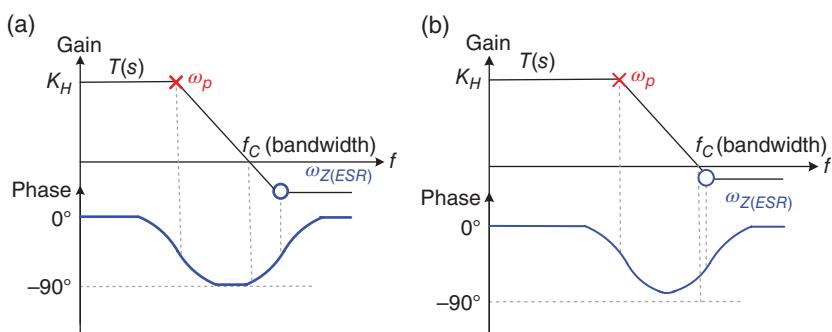
The current-mode control contains one pole and one zero. Similar to the voltage-mode control, the output capacitor and its ESR value form a zero. The pole is supplied by the output capacitor and load resistance. The Bode plot of the simplified current-mode control-to-output model is illustrated in Figure 3.41. The load resistance  $R_L$  varies with different output loading conditions. Thus, the location of  $\omega_p$  varies accordingly. At a light load,  $\omega_p$  moves toward the origin. At a heavy load,  $\omega_p$  moves toward higher frequencies.

The frequency response characteristic of the current mode is less complex than that of the voltage mode. Thus, the compensation network design can be simplified. Furthermore, the EA with compensation network is expressed by  $A(s)$ . An adequate  $A(s)$  must be adapted to different load conditions in the following analysis. By introducing the high-DC gain  $K_H$  for voltage regulation, the Bode plot can be illustrated, as shown in Figure 3.42. The DC gain is approximately equal to  $K_H + K$  ( $\approx K_H$  because  $K_H \gg K$ ). Here,  $T(s)$  is a one-pole system with dominant pole  $\omega_p$ . At both light and heavy loads, the phase margin is larger than  $90^\circ$ .

The simulation results of the current-mode control with high DC gain  $K_H$  are shown in Figure 3.43. As depicted in Figure 3.43(a), the phase margin at light and heavy loads is  $31^\circ$



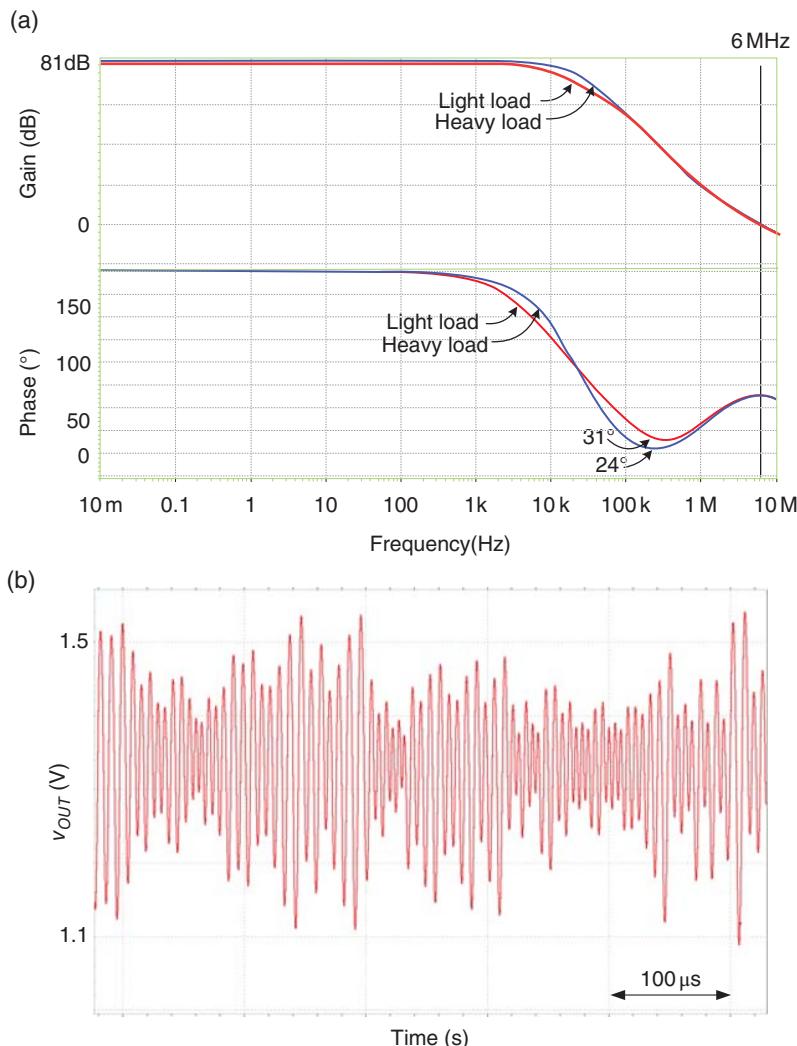
**Figure 3.41** Bode plot of the simplified current-mode control-to-output model



**Figure 3.42** Bode plot of the simplified current-mode model with a high DC gain of  $K_H$  at (a) light and (b) heavy loads

and  $24^\circ$ , respectively, indicating that the converter is stable. Interestingly,  $v_{OUT}$  is unstable in Figure 3.43(b). Instability results because the designed bandwidth is too large. As a rule of thumb, the crossover frequency should be lower than 1/10 or 1/5 of the switching frequency. A crossover frequency of 6 MHz is inappropriate in this case because of the switching frequency of 1 MHz. Moreover, the transfer function in Eq. (3.58) is an approximate model that does not include high-frequency poles and zeros. Additionally, a low-frequency dominant pole must be introduced.

An integrator with a transfer function, shown in Eq. (3.59), is ideally used to insert a dominant pole at the origin. In circuit implementation, a large-compensation capacitor is placed



**Figure 3.43** (a) Bode plot from the simulation results and (b) simulation results of  $V_{OUT}$  with a high DC gain of  $K_H$

at the output of the EA to further direct the dominant pole toward the origin. The corresponding  $T(s)$  is expressed in Eq. (3.60).

$$A(s) = -\frac{K_H}{s} \quad (3.59)$$

$$T(s) \approx K \cdot \frac{1 + sC_{OUT}R_{esr}}{1 + \frac{s}{\omega_p}} \cdot \left( -\frac{K_H}{s} \right) \quad (3.60)$$

Figure 3.44 illustrates the Bode plot of the simplified current-mode model with an integrator. The crossover frequency is lower than  $\omega_p$  and 1/10 of the switching frequency at light or heavy loads because of the pole at the origin.

The simulated Bode plot in Figure 3.45(a) indicates a large sufficient phase margin and a low crossover frequency. In reality, the dominant pole is located at low frequencies if a finite EA gain is obtained. As depicted in Figure 3.45(b), stable operation and good regulation can be obtained. However, a large undershoot/overshoot and a slow transient response occur as a result of the small bandwidth. To achieve stable operation and faster transient response, Type II compensation or PI compensation is commonly adopted in the current-mode control.

Type II compensation contains two poles and one zero. As shown in Figure 3.46,  $\omega_{p1}$  serves as the dominant pole and  $\omega_{z1}$  is introduced to compensate the phase delay caused by the output pole  $\omega_p$ .  $\omega_{p2}$  at higher frequencies is used to suppress high-frequency switching noise. As illustrated in Figure 3.46(a), (b), load variations result in different phase margins – although stable operation is ensured with an appropriate  $\omega_{z1}$  design.

The circuit implementation of Type II compensation is illustrated in Figure 3.47. Assuming that the ideal EA has an infinite gain, Eq. (3.61) can be derived. Two poles and one zero are expressed in Eqs. (3.62)–(3.65), respectively.

$$A(s) = -K \cdot \frac{\left( 1 + \frac{s}{\omega_{z1}} \right)}{\left( 1 + \frac{s}{\omega_{p1}} \right) \left( 1 + \frac{s}{\omega_{p2}} \right)} \quad (3.61)$$

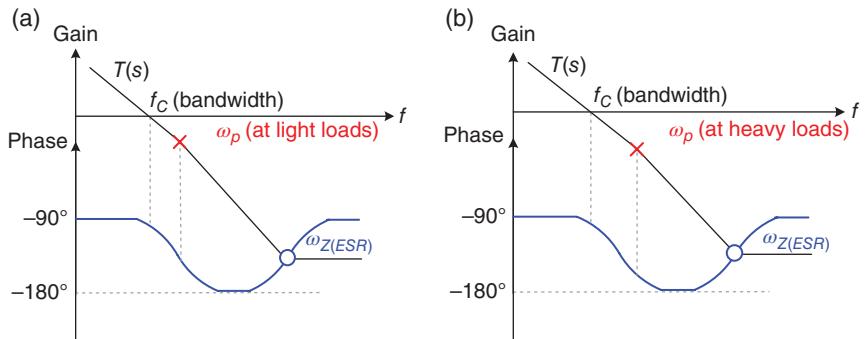
$$K = \frac{1}{R_f C_2} \quad (3.62)$$

$$\omega_{p1} = 0 \quad (3.63)$$

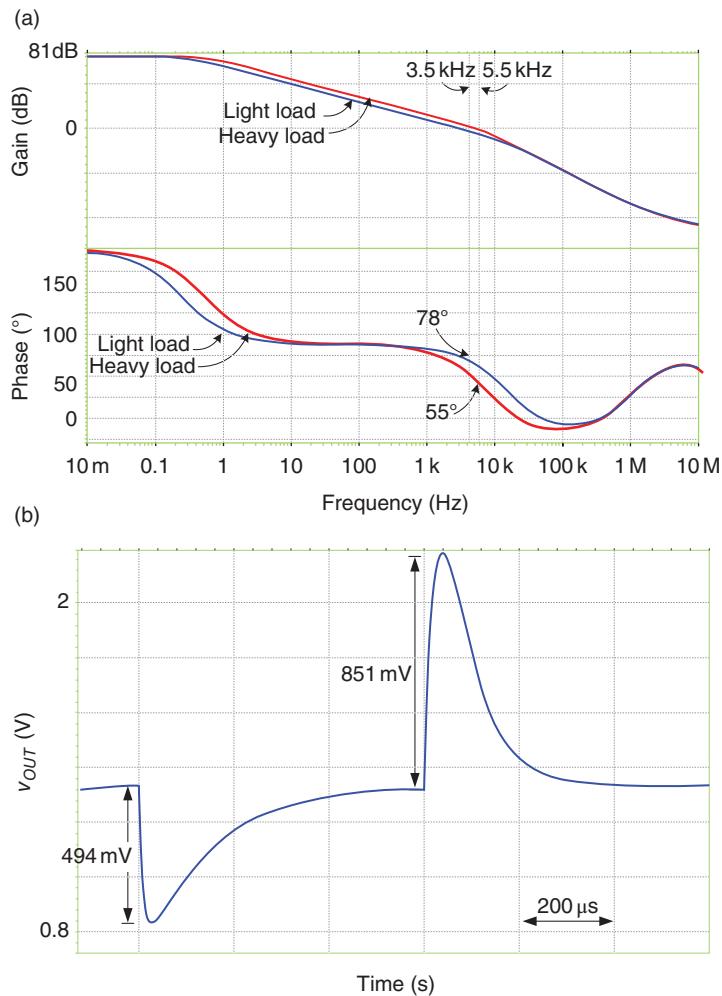
$$\omega_{z2} = \frac{C_2 + C_1}{C_2 C_1 R_1} \approx \frac{1}{C_2 R_1} \text{ if } C_1 \gg C_2 \quad (3.64)$$

$$\omega_{p2} = \frac{1}{C_1 R_1} \quad (3.65)$$

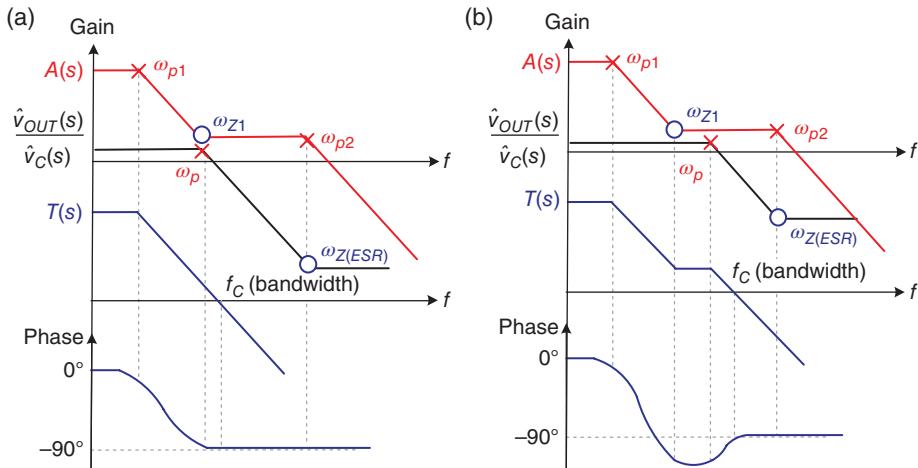
The Bode plot of the simulation results is shown in Figure 3.48. The dominant pole is not located at the origin but at low frequencies, because of the finite gain of the EA. A stable and



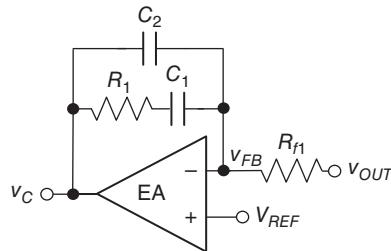
**Figure 3.44** Bode plot of the simplified current-mode model with an integrator at (a) light and (b) heavy loads



**Figure 3.45** (a) Bode plot of simulation results and (b) simulation results of  $V_{OUT}$  when a large-compensation capacitor is placed at the output of a high-gain EA



**Figure 3.46** Bode plot of the simplified current-mode model with Type II compensation at (a) light and (b) heavy loads

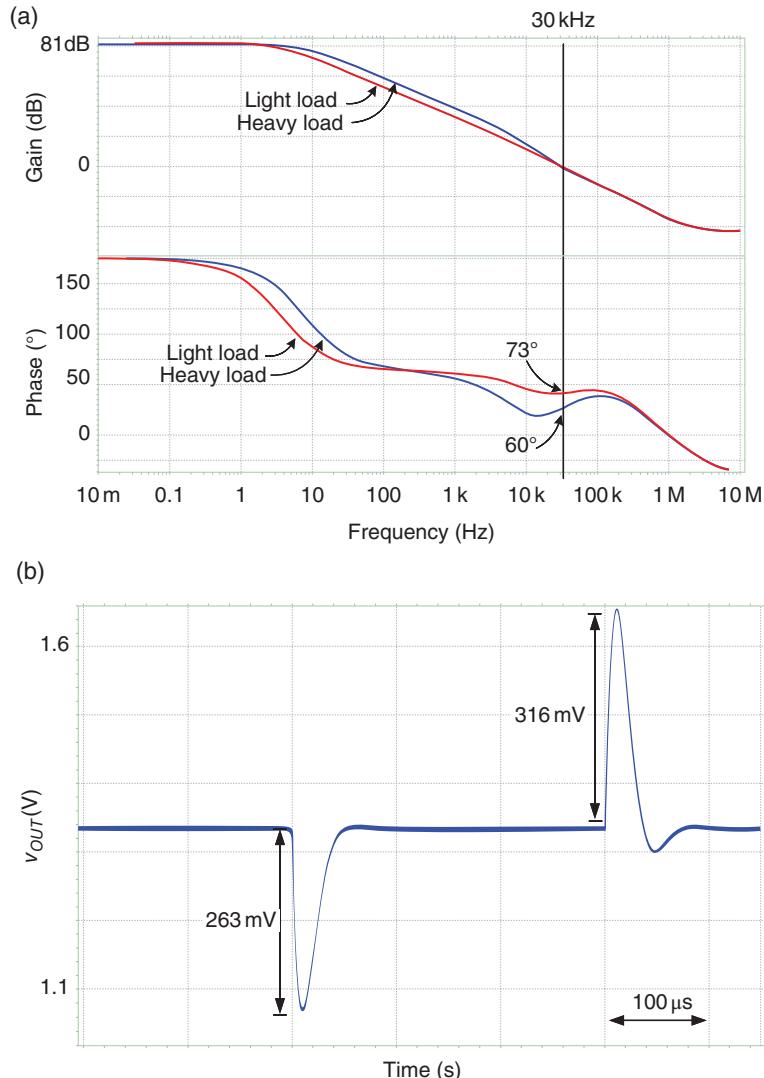


**Figure 3.47** Topology of Type II (PI) compensation

well-regulated output voltage is shown in Figure 3.48(b), even when the phase margins are slightly different at light and heavy loads. Furthermore, the undershoot/overshoot and transient response are significantly improved because the bandwidth is extended by introducing a zero in Type II compensation.

The detailed simulation waveforms of the current-mode control buck converter are illustrated in Figure 3.49. The current sensor determines the inductor current as signal  $v_s$  when the high-side MOSFET is turned on. As shown in Figure 3.49(b), the DC value of  $v_s$  increases with an increase in inductor current.  $v_{SUM}$  represents the total waveform of  $v_s$  and  $V_{RAMP}$ . When  $v_{SUM}$  reaches  $v_C$ , the duty cycle is determined. In Figure 3.49(a), (b),  $v_C$  is higher at heavy loads to increase the inductor current level. This process verifies that  $v_C$  can generate the current-control voltage through the voltage feedback loop.

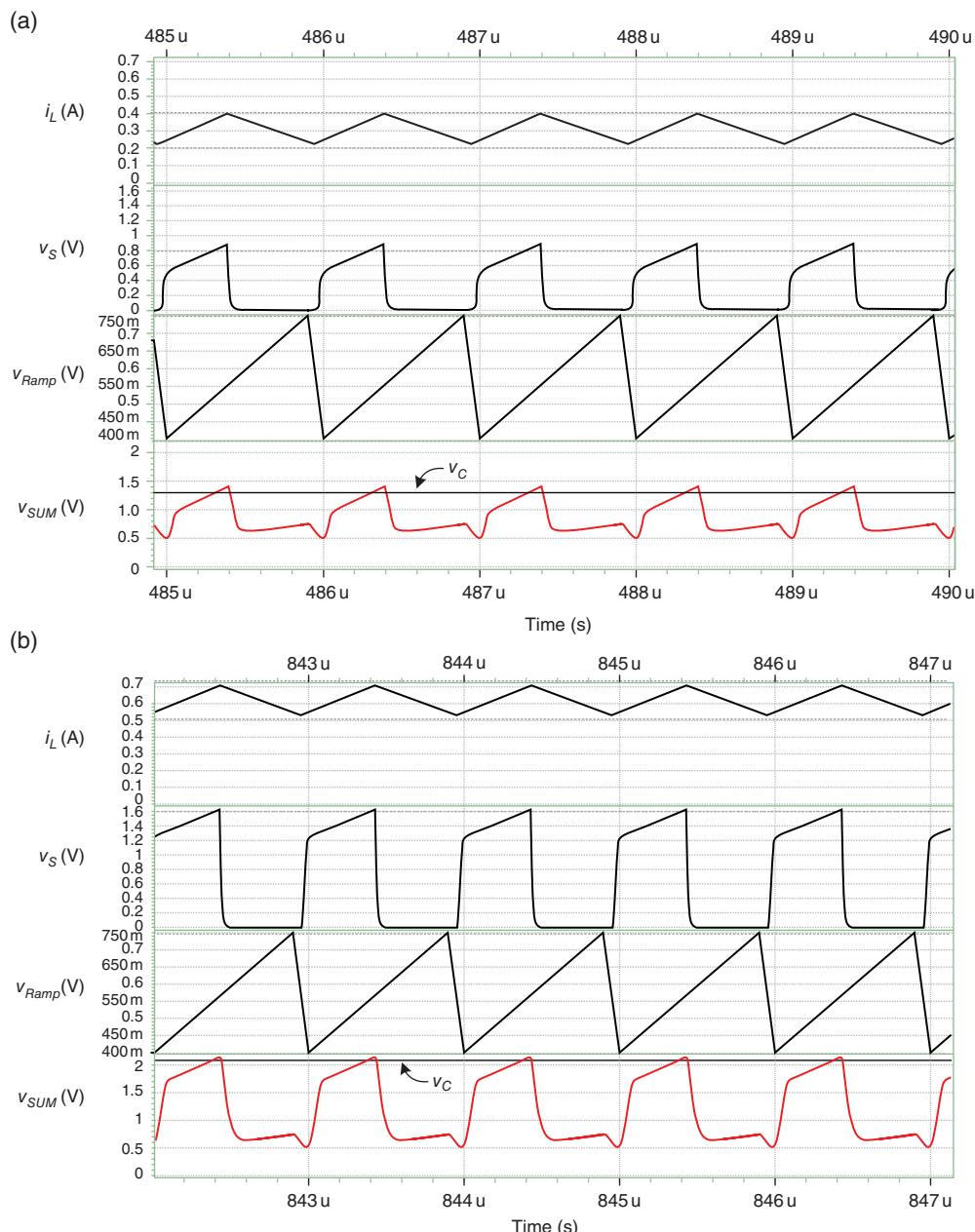
An alternative method of implementing Type II compensation is illustrated in Figure 3.50. Instead of  $v_{FB}$ ,  $C_1$  and  $C_2$  are connected to the ground. The transfer function can be derived using Eq. (3.66). The poles and zero are expressed in Eqs. (3.67)–(3.69), respectively. Similar to the original Type II compensation, the alternative Type II compensation contains two poles



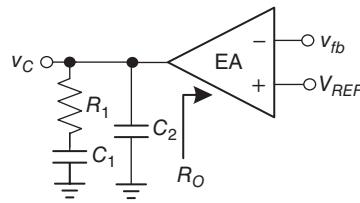
**Figure 3.48** (a) Bode plot of the simulation results and (b) simulation results of  $V_{OUT}$  with Type II compensation

and one zero. The dominant pole is contributed by the output resistance  $R_O$  and the capacitance  $C_1$  of the EA. The corresponding  $T(s)$  is expressed in Eq. (3.70).

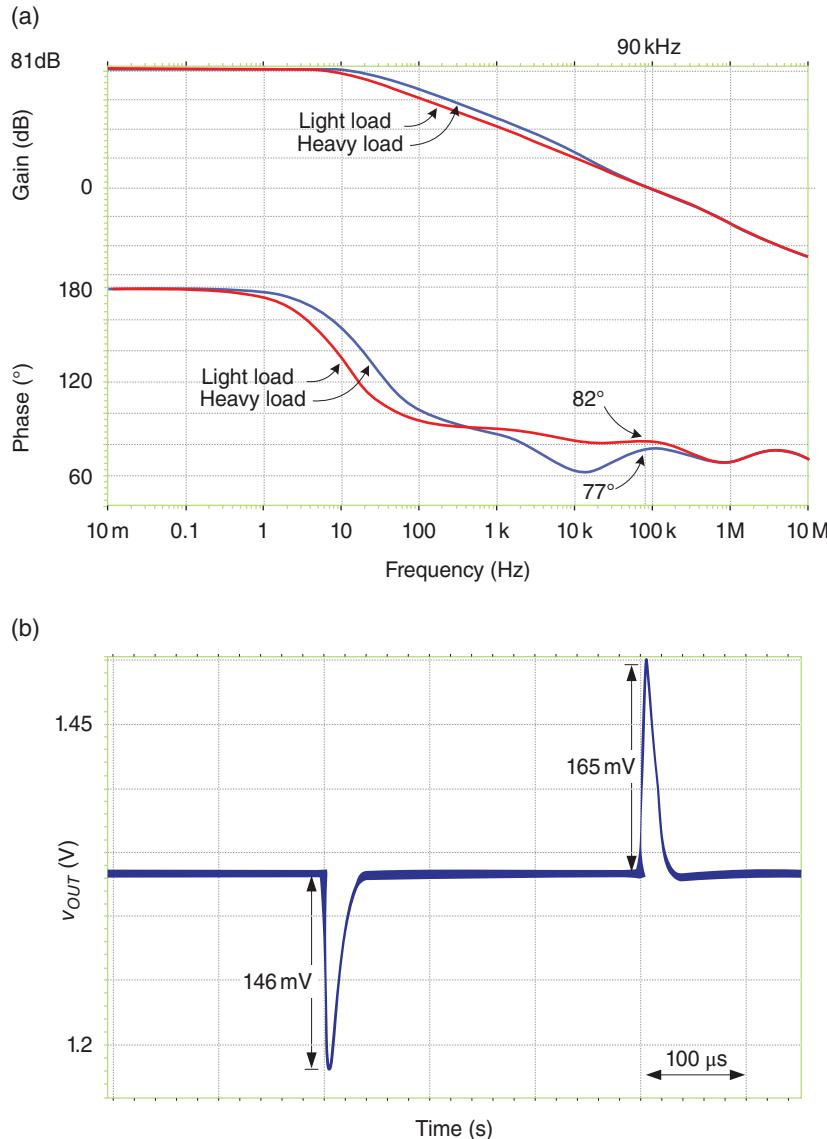
$$A(s) = -K_H \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \quad (3.66)$$



**Figure 3.49** Detailed simulation waveforms of the current mode at (a) light and (b) heavy loads



**Figure 3.50** Alternative topology of Type II compensation



**Figure 3.51** (a) Bode plot of the simulation results and (b) simulation results of  $V_{OUT}$  with the alternative Type II compensation

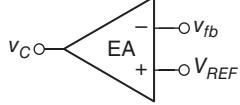
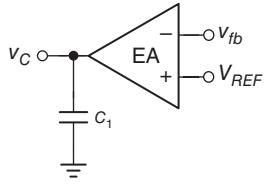
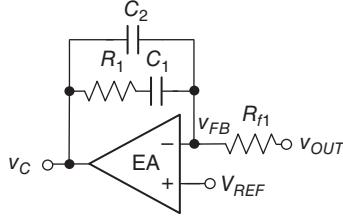
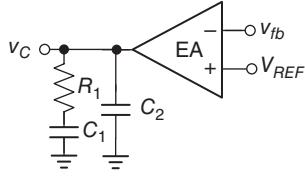
$$\omega_{p1} \approx \frac{1}{C_1 R_O} \quad (3.67)$$

$$\omega_{z1} = \frac{1}{C_1 R_1} \quad (3.68)$$

$$\omega_{p2} \approx \frac{1}{C_2 R_1} \quad (3.69)$$

$$T(s) \approx K \cdot \frac{1 + s C_{OUT} R_{esr}}{1 + \frac{s}{\omega_p}} \cdot \left( -K_H \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \right) \quad (3.70)$$

**Table 3.6** Comparison of different compensation methods in current-mode buck converters

| Method                   | $A(s)$   | Topology  | Ripple/transient/regulation |
|--------------------------|--|---|-----------------------------|
| High DC gain             | $-K_H$   |    | Unstable                    |
| Integrator               | $-\frac{K_H}{s}$   |   | Small/slowest/good          |
| Type II (PI)             | $A(s) = -K \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$ <p>where <math>K = \frac{1}{R_{f1} C_2}</math>, <math>\omega_{p1} = 0</math>,</p> $\omega_{z2} \approx \frac{1}{C_2 R_1}, \omega_{p2} = \frac{1}{C_1 R_C}$ |  | Small/fast/good             |
| Alternative Type II (PI) | $A(s) = -K_H \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$ <p>where <math>\omega_{p1} \approx \frac{1}{C_1 R_O}</math>, <math>\omega_{z2} = \frac{1}{C_1 R_1}</math>,</p> $\omega_{p2} \approx \frac{1}{C_2 R_1}$   |  | Small/fastest/good          |

**Table 3.7** Comparison of Hspice simulation results with different compensation methods

| Method       | Hspice condition  | Ripple (mV) | Recovery time ( $\mu$ s)/ $f_C$ (kHz) | Overshoot/undershoot (mV) |
|--------------|---|-------------|---------------------------------------|---------------------------|
| High DC gain | $K_H = 81$ dB   | NA          | NA                                    | NA                        |
| Integrator   | $K_H = 81$ dB, $C_1 = 2000$ pF  | 6           | 400/3.5                               | 494/851                   |
| Type II (PI) | $K_H = 81$ dB, $C_1 = 50$ pF,<br>$C_2 = 2$ pF, $R_1 = 150$ k $\Omega$ | 6           | 110/30                                | 263/316                   |
| Alternative  | $K_H = 81$ dB, $C_1 = 50$ pF, $C_2 = 2$ pF, $R_1 = 150$ k $\Omega$    | 6           | 54/90                                 | 13.4/10.2                 |
| Type II (PI) |   |             |                                       |                           |

$L = 4.7$   $\mu$ H,  $C_{OUT} = 4.7$   $\mu$ F,  $f_s = 1$  MHz,  $R_L = 4.3/2.15$   $\Omega$  (light/heavy load),  $R_{ESR} = 30$  m $\Omega$ .

The simulation results are shown in Figure 3.51. If  $C_1$ ,  $C_2$ , and  $R_2$  have the same values, the resultant crossover frequency is extended from 30 to 90 kHz. The transient response in Figure 3.51(b) indicates a smaller overshoot/undershoot and a shorter recovery time than the original Type II compensation. Thus, we can conclude that a larger bandwidth and a better transient response can be achieved by the alternative Type II compensation with the same component values as the original Type II compensation.

A comparison of the different compensation methods for current-mode buck converters is summarized in Table 3.6. Without inserting any pole and zero, the current-mode buck converter becomes unstable because the switching noise involves its bandwidth. By adding a large capacitor at the output of the EA, the integrator provides stable operation and slow transient response. To accelerate the transient response, Type II compensation introduces two poles and one zero. An alternative Type II compensation topology is adopted to further extend the bandwidth of the current-mode buck converter. A faster transient response can be achieved (Table 3.7).

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