Experiment 0 : Combinational Circuits – I

Part 2: A simple combinational circuit

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## Overview of the experiment:

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| The circuit has 8 inputs x7; x6; x5; x4; : : : x0 and two outputs y1; y0. The output bit y1 is 1 if and only if the number of input bits that are 1 is greater than the number of input bits that are 0. The output bit y0 is the complement of y1. |

## Approach to the experiment:

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| The approach was to somehow partition the bits and store the information as we go along higher levels of execution.  In this way the information got carried in each stage to the next stage. |

## Design document and VHDL code if relevant:

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| The design broadly included using 5 Full Adders ,2 Half Adders,1 AND gate,2 OR gates and 1 NOT gate.  VHDL code for comb\_ckt-    VHDL code for Dut file- |

## RTL View:

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| RTL view of the combinational circuit |

## DUT Input/Output Format:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| Mention the format (LSB/MSB of input and output) and few test cases from trace-file.   |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | Input |  |  |  |  |  |  |  | Output |  | Mask |  | | MSB |  |  |  |  |  |  | LSB | MSB | LSB | MSB | LSB | | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | O2 | O1 | M2 | M1 | | 1  0 | 0  1 | 0  0 | 1  1 | 1  0 | 1  0 | 1  0 | 0  1 | 1  0 | 0  1 | 1  1 | 1  1 | |

## RTL Simulation:

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| RTL simulation screen shot |

## Gate-level Simulation:

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| Gate-level simulation screen shot |

## Krypton board\*:

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## Observations\*:

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## References:

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| No references |

\* To be submitted after the tutorial on ”Using Krypton.