Task: 8

Title: Developing FPGA Architecture for ADAS in Electric Vehicles

1. Introduction

Safety measures in automobiles, such as shatter-resistant glass, three-point seatbelts, and airbags, have evolved from passive accident mitigation to active safety improvements using modern technology like embedded vision in ADAS systems. Autonomous vehicles, integral to the next generation of mobile-connected devices, utilize systems on a chip (SoCs) to connect sensors to actuators, enabling 360-degree vision and advanced functionality. This research focuses on deploying an FPGA for ADAS in level 5 autonomous vehicles, particularly for complex vision tasks. The report proposes an efficient ADAS solution on FPGA, integrating lane detection, object detection, distance estimation, and traffic light recognition, with optimized performance on Altera Cyclone V FPGA to achieve 55 FPS for one channel.

2. Reference Study

Traditional car automation techniques rely on microprocessors designed for automotive applications, meeting stringent real-time processing, reliability, and safety requirements. The advent of FPGAs in the 1980s brought popularity due to their reprogramming ability and parallel processing capabilities. Lane detection often uses edge detection algorithms, with Canny Edge Detection being superior due to accurate edge localization and automatic thresholding, which is employed in this report. Traffic light recognition in autonomous systems uses a combination of color-based segmentation, pattern matching, and machine learning techniques like the YOLOv5 algorithm to detect traffic lights in complex urban environments.

3. Materials and Method used

The processing unit in an ADAS system is responsible for analysing the information from the sensors and making decisions based on that. The processing unit may be implemented using a microcontroller, a processor, or an FPGA, depending on the application's specific requirements. The FPGA used in this project is the Intel DE10 Nano. The DE10-Nano is a compact, low-power development board featuring an Intel Cyclone V FPGA. The DE10-Nano is equipped with a dual-core Arm Cortex-A9 processor, which can be used to run software applications. The Hough transform [5] is an image-processing technique used in edge detection to improve the accuracy and robustness of lane detection. It is used in a variety of other applications, such as detecting circles, ellipses, and other geometric shapes in images.

4. Results and Discussion

4.1 Lane Detection

Figure 1 is the snapshot of an input fed to the lane detection pipeline. Figure 2 is the final output. The lane detection feature is used to detect the lane where the car is currently present and the ones that may exist on either side of the lane. The green overlay on the input gives a clear understanding of the path ahead of a driver. This feature has increased importance when it is integrated into an autonomous driving system[1] wherein the car is itself expected to take decisions. The lane departure warning system provides a physical alarm to the driver about the

departure from the existing lane. CARLA[2][3] was used to visualize these results in a real-time environment as shown in Fig.3.

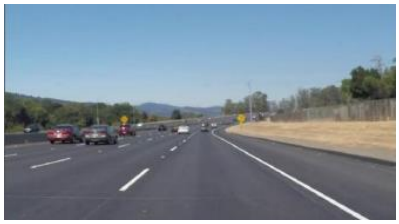

Figure1: Input to line detection pipeline

Figure 2: Lane detected output

Figure 3: Visualization of CARLA

4.2 Object Detection, Object Distance Estimation, Traffic Light Detection

Figure 4 describes the features of object detection, object distance estimation and traffic light detection. The bounding boxes have different colours for different objects – orange for cars, red for people, etc. At the header of these bounding boxes are the identified objects' labels and a number that lies between 0 to 1 called objectness. Objectness indicates the accuracy with which the algorithm has identified the object. Further, a green bounding box enclosing a traffic signal signaling 'green for go' is also seen. In the case of traffic light , the bounding box labels the signal identified.

Figure 4: Object detection, distance estimation, traffic light detection

5. Conclusion

The implementation of ADAS on FPGA comes with advantages like parallel processing capabilities of FPGA[4] , low power consumption and better throughput, along with a great deal of cost reduction. According to the August 2016 Traffic Safety Facts Research Note by the National Highway Traffic Safety Administration (NHTSA)[5] , "The Nation lost 35,092 people in crashes on U.S. roadways during 2015." This 7.2% increase was "the largest percentage increase in nearly 50 years." An analysis revealed that about 94% of those accidents were caused by human error. The application of this project is a stepping stone towards bringing a transformation in the automobile industry towards safer roads and safer pedestrians. The work carried out in this report has brought to light, promising areas of further research [6] in the ADAS system optimization field. Further improvements by deep model compression and software hardware collaborative optimization can be obtained.

References

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