VISHNU INSTITUTE OF TECHNOLOGY

(AUTONOMOUS)

VISHNUPUR, BHIMAVARAM – 534 202

STUDENT NOTEBOOK

COMPUTER ORGANIZATION

II B.Tech. I Semester CSE :: 2023 – 2024

Established by

SRI VISHNU EDUCATIONAL SOCIETY

153, Sita Nilayam, Dwarakapuri Colony, Punjagutta,

HYDERABAD – 500 082. Ph. No. 040 – 23352916

VISHNU INSTITUTE OF TECHNOLOGY

VISION

To empower the students through Academic excellence and Ethics so as to bring about social transformation and prosperity.

MISSION

1. To expand the frontiers of knowledge through quality education.
2. To provide value added Research and development.
3. To embody a spirit of excellence in Teaching, Creativity, Entrepreneurship and Outreach.
4. To provide a platform for synergy of Academy, Industry and Community.
5. To inculcate high standards of Ethical and Professional behaviour.

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

VISION

To build a strong teaching-learning base with a flair for innovation and research that responds to the dynamic needs of the software industry and the society with good ethical practices.

MISSION

1. To provide strong foundation both in theory and applications of Computer Science & Engineering, so as to solve real-world problems.
2. To empower students with state-of-art knowledge and up to date technological skills, making them globally competent.
3. To promote research, innovation and entrepreneurship with focus on industry and social outreach.
4. To foster civic minded leadership with ethics and values among students.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Graduates will have knowledge of mathematics, science, engineering fundamentals, and in-depth studies in Computer Science Engineering, and will be able to apply them for formulating, analyzing and solving real world problems.

PEO2: Graduates will succeed in earning coveted entry level positions in leading Computer Software and Hardware Firms in India and abroad.

PEO3: Graduates will succeed in the pursuit of advanced degrees and research in engineering or other fields and will have skills for continued, independent, lifelong learning and professional development throughout life.

PEO4: Graduates will have good communication skills, entrepreneurial skills, leadership qualities, ethical values and will be able to work in teams with due attention to their social responsibilities.

COURSE STRUCTURE

II YEAR I SEMESTER								
S.No	**Category**	**Subjects**	**L**	**T**	**P**	**C**	**I**	**E**
1	BS / PC	Discrete Mathematical Structures	3	0	0	3	30	70
2	PC	Data Structures	3	0	0	3	30	70
3	PC	Database Management Systems	3	0	0	3	30	70
4	ESC	Object Oriented Programming through Java	3	0	0	3	30	70
5	PC	Computer Organization	3	0	0	3	30	70
6	PC Lab	Data Structures Lab	0	0	3	1.5	15	35
7	PC Lab	Database Management Systems Lab	0	0	3	1.5	15	35
8	PC Lab	Object Oriented Programming through Java Lab	0	0	3	1.5	15	35
9	SO	Skill Oriented Course – I 1) Animations – 2D Animation 2) Web Application Development Using Full Stack – Module – I	0	0	4	2	--	50
10	MC	Environmental Science	2	0	0	0		
	Total Credits					**21.5**	**195**	**505**
	Total Marks						**700**	

Department of Computer Science & Engineering

Syllabus: II B.Tech-I Semester

(R-20 Regulations)

Computer Science & Engineering (CSE)

Course Title: Computer Organization

UNIT -I:

Basic Structure of Computers: Functional unit, Basic Operational concepts, Bus structures, System Software, Performance, The history of computer development.

UNIT -II:

Machine Instruction and Programs: Instruction and Instruction Sequencing: Register Transfer Notation, Assembly Language Notation, Basic Instruction Types, Addressing Modes, Basic Input/output Operations, The role of Stacks and Queues in computer programming equation. Component of Instructions: Logic Instructions, shift and Rotate Instructions, Arithmetic and Logic Instructions, Branch Instructions, Addressing Modes, Input/output Operations

UNIT -III:

INPUT/OUTPUT ORGANIZATION: Accessing I/O Devices, Interrupts: Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, Buses: Synchronous Bus, Asynchronous Bus, Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI) Bus, Universal Serial Bus (USB)

UNIT -IV:

The Memory Systems: Basic memory circuits, Memory System Consideration, ReadOnly Memory: ROM, PROM, EPROM, EEPROM, Flash Memory, Cache Memories: Mapping Functions, INTERLEAVING Secondary Storage: Magnetic Hard Disks, Optical Disks,

UNIT -V:

Processing Unit: Fundamental Concepts: Register Transfers, Performing An Arithmetic Or Logic Operation, Fetching A Word From Memory, Execution of Complete Instruction,

Hardwired Control, Micro programmed Control: Microinstructions, Micro program Sequencing, Wide Branch Addressing Microinstructions with next –Address Field

TEXT BOOKS:

1. Computer Organization, Carl Hamacher, Zvonks Vranesic, Safea Zaky, 5th Edition, McGraw Hill.

2. Computer Architecture and Organization, John P. Hayes, 3rd Edition, McGraw Hill.

REFERENCE BOOKS:

1. Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI

2. Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition PHI/Pearson

3. Fundamentals or Computer Organization and Design, - Sivaraama Dandamudi Springer Int.

4. “Computer Organization and Design: The Hardware/Software Interface” by David A. Patterson and John L. Hennessy.

E-Resources:

https://www.javatpoint.com/computer-organization/

https://www.geeksforgeeks.org/computer-organization/

LESSON PLAN

CLASS: II Year I Sem. **BRANCH: CSE**

SUBJECT: Computer Organization **ACADEMIC YEAR:** 2023-24

PREREQUISITES:

- Basic knowledge of computer is required.

COURSE OBJECTIVES: Students are expected to

- To understand Architecture of modern Computer.
- To understand Notations, Logic Instructions, shift and Rotate Instructions, Arithmetic and Branch Instructions, Input/output Operations.
- To understand different types of Addressing Modes.
- To understand how computer stores positive & negative numbers using 1's & 2's complement.
- To learn how a computer performs arithmetic operations like Addition, Subtraction, Multiplication, Division etc.

COURSE OUTCOMES:

After completion of the course, the student will be able to

• Students can understand the architecture of modern computer.

• Understanding of different instruction types.

• Students can calculate the effective address of an operand by addressing modes

• They can understand how computer stores positive and negative numbers.

• Understanding of how a computer performs arithmetic operation of positive and negative numbers.

S.No.	No.Of Classes	Topic	Page No	Reference
UNIT 1: Basic Structure of Computers				
1	1	Basic Structure of Computers	2	T1
2	1	Functional unit	3	T1
3	1	Basic Operational concepts	7	T1
4	1	Bus structures	9	T1
5	1	System Software	10	T1
6	2	Performance	13	T1
7		The history of computer development	19	T1
Total No.of Classes: 08				
UNIT 2: Machine Instruction and Programs				
8	1	Machine Instruction and Programs, Instruction and Instruction Sequencing	25 - 37	T1
9	1	Register Transfer Notation, Assembly Language Notation	57 - 58	T1
10	1	Basic Instruction Types	38	T1
11	3	Addressing Modes	48	T1
12	1	Basic Input/output Operations	64	T1
13	2	The role of Stacks and Queues in computer programming equation	68	T1
14	1	Component of Instructions: Logic Instructions	81	T1
15	1	Shift and Rotate Instructions, Arithmetic and Logic Instructions	82	T1
16	1	Input/output Operations	121	T1
Total No.of Classes: 12				

UNIT 3: Input/Output Organization				
17	1	Accessing I/O Devices,	204	T1
18	1	Interrupts: Interrupt Hardware	208 - 201	T1
19	2	Enabling and Disabling Interrupts	211	T1
20	2	Handling Multiple Devices	213	T1
21	2	Direct Memory Access,	234	T1
22	2	Buses: Synchronous Bus, Asynchronous Bus	241 - 244	T1
23	2	Interface Circuits, Standard I/O Interface: Peripheral Component Interconnect (PCI), Bus, Universal Serial Bus (USB)	259 - 272	T1
Total No.of Classes: 12				
MID – I Examinations				
UNIT 4: The Memory Systems				
24	1	Basic memory circuits	292	T1
25	1	Memory System Consideration	293	T1
26	2	Read Only Memory: ROM, PROM	309 – 311	T1
27	1	EPROM, EEPROM	311	T1
28	1	Flash Memory	312	T1
29	1	Cache Memories: Mapping Functions	316	T1
30	1	Interleaving	330	T1
31	2	Secondary Storage: Magnetic Hard Disks, Optical Disks	344	T1
Total No.of Classes: 10				

UNIT 5: Processing Unit				
32	1	Fundamental Concepts: Register Transfers	412 - 415	T1
33	1	Performing An Arithmetic or Logic Operation	415	T1
34	1	Fetching A Word from Memory	417	T1
35	1	Execution of Complete Instruction	421	T1
36	1	Hardwired Control	425	T1
37	1	Micro programmed Control: Microinstructions	429 – 432	T1
38	1	Micro program Sequencing	435	T1
39	2	Wide Branch Addressing Microinstructions with next –Address Field	437 - 440	T1
Total No.of Classes: 9				
MID – II Examinations				
Preparation				
End Examinations				

TEXT BOOKS:

1. Computer Organization, Carl Hamacher, Zvonks Vranesic, Safea Zaky, 5th Edition, McGraw Hill.

2. Computer Architecture and Organization, John P. Hayes, 3rd Edition, McGraw Hill.

Signature of the Faculty **Signature of the HOD**

Question Bank

UNIT 1: Basic Structure of Computers

1. List the steps needed to execute the machine instruction Add LOCA, R0 in terms of transfer between processor and the memory along with some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and this address initially in register PC. The first two steps might be expressed as:

- Transfer the content of register PC to register MAR.
- Issue read command to the memory and then wait until it has transferred the requested word int register MDR.

2. What is performance measurement? Explain the overall SPEC rating for the computer in a program suite.

3. Describe the operational concepts between the processor and memory.

4. Mention four types of operations to be performed by instructions in a computer. Explain with basic types of instruction formats to carry out C [A] + [B].

5. Explain different functional units of a computer.

6. How to measure the performance of the computer? Explain.

7. Explain clearly SPEC rating and its significance. Assuming that the reference computer is ultra SPARCIO work station with 300 MHz ultra-SPARC processor. A company has to purchase 1000 new computers hence ordered testing of new computer with SPEC 2000. Following observations were made.

Programs	Runtime on reference computer	Runtime in new computer
1	50 Mins	5 Mins
2	75 Mins	4 Mins
3	60 Mins	6 Mins
4	30 Mins	3 Mins

The company system manager will place the order for purchasing new computers only if the overall SPEC rating is at least 12. After the said test will the system manager place order for purchase of new computers.

8. With a neat diagram, discuss the concepts of a computer.

9. Draw the connection between processor and memory and mention the functions of each component in the connection.

10. Write the difference between RISC and CISC processors.

11. Draw and Explain the connection between memory & processor with respective registers.

12. A program contains 1000 instructions. Out of that 25% instructions requires 4 clock cycles, 40% instructions require 5 clock cycles & remaining require 3 clock cycles for execution. Find the total time required to execute the program running in a 1 GHz.

13. How to measure the performance of the computer? Explain.

UNIT 2: Machine Instruction and Programs

1. Define addressing modes. Give the details of different addressing modes.

2. What is stack organization? Explain implementation of stack with notations and applications.

3. Explain Shift and Rotate instructions with examples.

4. Explain logical instructions and rotate instructions with examples.

5. Discuss briefly instructions and instruction sequencing and Explain

(a) Register transfer notation (b) Assembly language Notation

(c) Relative Addressing Mode (d) Auto Decrement Addressing Mode

6. Explain Basic Instruction types with examples.

7. With the help of diagram explain basic I/O operations.

8. Explain PUSH and POP operations in Stack and Discuss Queue implementation with applications.

9. Using 8086 Microprocessor Arithmetic instructions write an algorithm and program 8-bit Hexadecimal numbers for

(a) ADD (b) ADC (C) SUB

(d) MUL (e) DIV (f) CBW

10. Discuss about Branch Instructions with Examples.

11. What is Subroutine? How to pass parameters to subroutine? Illustrate with an example.

12. Discuss briefly encoding of Machine Instructions.

13. With a neat diagram, describe input and output operations.

14. List the name, assembler syntax & addressing functions for the different addressing modes.

15. With example, explain subroutine stack frame.

UNIT 3: Input/Output Organization

1. In a situation where multiple devices capable of initiating interrupts are connected to the processor, explain the implementation of interrupt priority, using individual INTER and INTA and a common INTR line to all devices.

2. Define memory mapped I/O and I/O mapped I/O with examples.

3. What are the different methods of DMA? Explain.

4. Explain (i) Interrupt Enabling (ii) Interrupt Disabling

5. Explain the following terms (i) Interrupt service routine (ii) Interrupt Latency

6. Define Interrupt? With example illustrate the concept of interrupts.

7. Explain in detail, the situations where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems.

8. Explain following methods of handling interrupts from multiple devices.

9. Discuss how interrupt requests from several I/O devices can be communicated to a processor through a single INTR line.

10. With neat sketches, explain the various methods for handling multiple interrupt requests.

11. With a neat diagram, explain in detail input interface circuit.

12. With a neat diagram, explain in detail output interface circuit & timing interface.

13. With a neat diagram, explain in detail I/O interface circuit.

14. Explain tree structure of USB with split bus operation.

15. Explain the Serial Port and Serial interface with diagrams.

16. Describe how a read operation is performed on a PCI bus.

17. Explain Parallel port with diagrams.

18. Sketch neatly Synchronous bus and its operations.

19. Sketch neatly Asynchronous bus and its operations.

20. Difference between Synchronous & Asynchronous buses.

21. Define the terms ‘Cycle Stealing’ & ‘Block Mode’.

22. What is Bus arbitration? Explain different approaches to bus arbitration.

23. Explain how interrupt requests from several IO devices can be communicated to a processor through a single INTR line.

24. Draw the arrangement of a single bus structure & briefly explain about memory mapped I/O.

25. Explain (a) Interrupt Enabling (b) Interrupt Disabling (c) Edge Triggering

26. Draw the arrangement for bus arbitration using a daisy chain & explain.

27. Explain the following with respect to interrupts with diagrams.

(a) Vectored Interrupt

(b) Interrupt Nesting

(c) Simultaneous Request

(d) Interrupt Service Routine

(e) Interrupt Latency

28. Explain with a neat diagram, the hardware components needed for connecting a keyboard to a processor.

29. Explain the Architecture & Protocols w.r.t to USB.

30. List the functions of an I/O Interface.

31. With a block diagram, explain how the printer is interfaced to the processor.

32. Explain the architecture & addressing scheme of USB.

33. With neat diagram explain how to interface printer to the processor.

UNIT 4: Memory System

1. Explain the Internal Organization of a 2M×32 memory module using 512k×8 Static memory chips.

2. Describe Secondary Storage devices with diagrams?

3. Briefly explain any four Non-volatile memory concepts.

4. Explain Direct Mapping & Associative Mapping with neat diagrams.

5. Discuss the Internal Organization of a 2M×8 Asynchronous DRAM chip.

6. Describe the different mapping functions in cache.

7. Difference between SRAM & DRAM, and Explain Advantages & Disadvantages, Characteristics.

8. Explain Synchronous & Asynchronous DRAM with diagrams.

9. Sketch neatly basic memory circuits.

10. With a block diagram, explain the Direct and Set Associative Mapping between cache and main memory.

11. Describe the principles of Magnetic Disk.

12. Draw a diagram & explain the working of 16 MB DRAM chip configured as 2MX8. Also explain any four non-volatile memory concepts.

13. With figure analyse the memory hierarchy in terms of speed, cost & size.

14. With a neat diagram, explain the translation of a virtual address to a physical address.

15. Discuss in detail any one feature of memory design that leads to improved performance of computer.

16. Draw for 1KX1 Memory chip with neat diagram.

17. What is Virtual memory? With a diagram, explain how virtual memory address is translated.

UNIT 5: Basic Processing Unit

1. List out the actions needed to execute the instructions ADD (R3), R1. Write & explain the sequence of control steps for the execution of the same.

2. With a neat block diagram, explain hardwired control unit. Show the generation Zin and end control signals.

3. Write and explain the control sequence for execution of an unconditional branch instruction.

4. With a neat sketch, explain the organization of a micro programmed control unit.

5. Draw & Explain the Single-Bus Organization of a micro programmed control unit.

6. With an example, Explain the field-encoded micro instructions.

7. Draw & explain Fetching a word from memory with timing read operation.

8. Difference between Hardwired & Micro programmed control unit. also explain Single-Bus Organization of data path & control.

9. Explain with neat diagram, basic organization of a micro programmed control unit.

10. Write and explain the control sequence for execution of an unconditional branch instruction.

11. Briefly Explain about Register Transfers with neat diagrams.

12. Explain micro program sequencing with neat diagrams.

13. With an example, Perform an arithmetic or logic operation with block diagram.

14. Construct Wide Branch Addressing Microinstructions with next-Address Field.

15. with the help of diagram explain execution of complete instruction

H.T.No: | | | | | | | | | | |

Course Code No: 20CS3T02

VISHNU INSTITUTE OF TECHNOLOGY (AUTONOMOUS)

II B. Tech I Semester (R20) - Regular Examinations, FEB/MAR – 2022

Computer Organization

(CSE & IT)

Time: 3hours **Max. Marks: 70M**

Note: 1. Answer all the 5 Questions
2. Each Question carries 14 Marks
3. Answer either question from each unit

UNIT – I

1	a	With the help of a neat diagram explain the various components of a digital computer.	L1	CO1	[7M]
	b	Sam wants to execute an instruction ADD. List the various steps involved to perform this operation and the registers that are used.	L2	CO1	[7M]
		(OR)			
2	a	What is a Register? List the different types of registers available in a CPU and their function.	L3	CO1	[7M]
	b	What is a Bus? How many types of busses are available? List the merits and demerits of each bus.	L1	CO1	[4M]
	c	Differentiate between compiler and interpreter and assembler.	L2	CO1	[3M]

UNIT – II

3					
	a	List the different types of instructions that are available with a proper example.	L2	CO2	[7M]
	b	What is an addressing mode? With a proper example explain various addressing modes.	L	CO2	[7M]
		(OR)			
4	a	What is an Instruction format? Evaluate the instruction (A+B) * (C+D) using Two, one, zero addressing formats.	L3	CO2	[7M]
	b	What is meant by Register transfer notation? Represent the following conditional control statement by two register transfer statements with control functions. i)If (p=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3) ii)If (p=1) and (Q=1) then (R1 ← R2),(R4 ← R2) else if (s=1) then (R1 ← R3)	L1	CO2	[4M]
	c	What is the difference between i) Shift and Rotate operations? With a proper example justify your answer.	L	CO2	[3M]

UNIT – III

5	a	What is an Interrupt with example explain: i) Interrupt enabling; ii) Interrupt disabling; iii) Edge triggering.	L1	CO3	[7M]

	b	What is the difference between Asynchronous and Synchronous Bus? Find out the number of characters that are transmitted for a Baud rate 2000 for a i) Synchronous serial transmission ii) Asynchronous serial transmission with two stop bits. iii) Asynchronous serial transmission with one stop bit.	L2	CO3	[7M]
		(OR)			
6	a	What is DMA? Explain how Data transfer will take place in DMA With the help of a diagram.	L3	CO3	[7M]
	b	Discuss the following. i) Peripheral Component Interconnect (PCI) Bus, ii) Universal Serial Bus (USB)	L1	CO3	[7M]
UNIT – IV					
7	a	List the difference between DRAM and SRAM. Find out the hit ratio if the CPU referred memory for 500 times and found data in cache 475 times.	L1	CO4	[4+3M]
	b	Briefly explain any four non-volatile memory concepts.	L2	CO4	[7M]
		(OR)			
8	a	List the difference between RAM and ROM. Mapp the locations from main memory to Cache if the main memory has 40 locations and cache has 10 locations if a direct mapping is used. Main memory Locations 35,09,14,23,20,05 and 40.	L3	CO4	[7M]
	b	Discuss the Virtual memory concept in detail.	L1	CO4	[7M]
UNIT – V					
9	a	List out the various steps involved in the execution of the instruction MUL R1,R2 List the difference between Hardwired control and Micro programmed control..	L1	CO5	[7M]
	b	With a neat diagram explain the Micro programmed control Organization.	L2	CO5	[7M]
		(OR)			
10	a	Write a micro programmed control sequence for the instruction MOV R1 ← R2	L3	CO5	[7M]
	b	What is a control word? Draw the structure of control word and explain each field with a proper example.	L1	CO5	[7M]

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H.T.No: | | | | | | | | | | |

Course Code No: 20CS3T02

VISHNU INSTITUTE OF TECHNOLOGY (AUTONOMOUS)

II B. Tech I Semester (R20) - Supplementary Examinations, July – 2022

Computer Organization

(CSE & IT)

Time: 3hours **Max. Marks: 70M**

Note: 1. Answer all the 5 Questions
2. Each Question carries 14 Marks
3. Answer either question from each unit

UNIT – I

1	a	List the different components available in a Digital computer. Explain each components in detail.	L1	CO1	[7M]
	b	List the difference between DRAM and SRAM.	L2	CO1	[4M]
		How the performance of a computer will be measured?			[3M]
		(OR)			
2	a	What are the different Register available in a computer? Explain the function of each.	L3	CO1	[7M]
	b	Classify the Memories that are available. Explain briefly each of them.	L1	CO1	[7M]

UNIT – II

3	a	What is a machine cycle and Instruction cycle? What are the different Hard ware components that are activated to execute an instruction?	L1	CO2	[7M]
	b	What is an addressing mode? With a proper example explain various addressing modes.	L2	CO2	[7M]
		(OR)			
4	a	What is an Instruction format? Evaluate the instruction (A*B) - (C/D) using zero, Two and Three addressing formats.	L3	CO2	[7M]
	b	What is meant by Register transfer notation? Represent the following conditional control statement by two register transfer statements with control functions. i)If (p=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3) ii)If (p=1) and (Q=1) then (R1 ← R2), (R4 ← R2) else if (s=1) then (R1 ← R3)	L1	CO2	[7M]

UNIT – III

5	a	What is DMA? Explain how Data transfer will take place in DMA With the help of a diagram.	L1	CO3	[7M]
	b	What is the difference between Asynchronous and Synchronous Bus? Find out the number of characters that are transmitted for a Baud rate 5000 for a i) Synchronous serial transmission ii) Asynchronous serial transmission. iii) Asynchronous serial transmission with one stop bit.	L2	CO3	[7M]

(OR)

6		Discuss the following a) Interrupt ii) PCI and iii) USB. [4+5+5]	L3	CO3	[14M]

UNIT – IV

7	a	List the differences between RAM and ROM. What are the different types of ROMs available? Write a note on each.	L1	CO4	[3M] [4M]
	b	What is a cache? Define Hit Ratio. Map the locations from main memory to Cache if the main memory has 40 locations and cache has 10 locations if a direct mapping is used. Main memory Locations -- 35, 09, 14, 23, 20, 05 and 40.	L2	CO4	[2M] [5M]

(OR)

8		Discuss Secondary storage in detail	L3	CO4	[14M]

UNIT – V

9	a	Write a Micro programmed control sequence to execute the following instruction.
		SUB R3,R4
		MUL R5,R3
			L1	CO5	[12M]

	b	List the difference between hardwired control and micro programmed sequence	L2	CO5	[2M]

(OR)

10	a	What is a control word and control memory? Draw the structure of control word and explain each field with a proper example.	L3	CO5	[7M]
	b	What is a Micro operation? What are the different types of micro operations are available? With an example explain each.	L1	CO5	[7M]

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Code: 19CS3T01 **R19** **H.T.NO**

VISHNU INSTITUTE OF TECHNOLOGY (AUTONOMOUS)

II B. Tech I Semester Regular Examinations, March-2021

Computer Organization & Architecture

(CSE)

Time: 3 hours **Max. Marks: 60**

Note: 1. Answer all the 6 Questions
2. Each Question carries 10 Marks
3. Answer either **a or b** from each question

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1(a)	I	Find the 2's complement of the following a)10010 b) 111000 c) 0101010 d) 101010	L2	CO1	[4M]
	II	Explain the components of a computer with the block diagram in detail	L2	CO1	[6M]
		(OR)			
1(b)		Differentiate between Fixed –Point representation & Floating Point representation with an example?	L2	CO1	[10M]
2(a)		Explain the arithmetic logic shift unit and its micro operations with a neat diagram	L2	CO2	[10M]
		(OR)			
2(b)	I	Mention various computer registers and discuss common bus system with neat sketch.	L1	CO2	[5M]
	II	What is RTL? Explain with suitable examples.	L1	CO2	[5M]
3(a)		Multiple (-7)10 with (3)10 by using Booth's multiplication. Give the flow table of the Multiplication	L2	CO3	[10M]
		(OR)			
3(b)	I	Explain the different Instruction formats.	L2	CO3	[5M]
	II	Explain about addition and Subtraction algorithm with an example and draw a flow chart with a neat sketch?	L2	CO3	[5M]
4(a)	I	Explain the various semiconductor memories with its memory Hierarchy.	L2	CO4	[5M]
	II	Differentiate static and Dynamic RAM.	L1	CO4	[5M]
		(OR)			
4(b)		Write short notes on (i)Micro instruction format (ii) Symbolic micro instruction.	L2	CO4	[10M]
5(a)		Explain with the block diagram the DMA transfer in a computer system.	L2	CO5	[10M]
		(OR)			
5(b)		Discuss about Source initiated data transfer and Destination initiated data transfer with flow diagram?	L2	CO5	[10M]
6(a)		Explain Inter Processor Arbitration along with its Serial and Parallel procedure with architecture?	L2	CO6	[10M]
		(OR)			
6(b)	I	Discuss the characteristics of Multiprocessor	L2	CO6	[5M]
	II	Discuss the Multi stage switching network with a neat diagram	L2	CO6	[5M]

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Code: 19CS3T01 **R19** **H.T.NO**

VISHNU INSTITUTE OF TECHNOLOGY (AUTONOMOUS)

II B. Tech I Semester Supplementary Examinations, Oct - 2021

Computer Organization & Architecture

(CSE)

Time: 3 hours **Max. Marks: 60**

Note: 1. Answer all the 6 Questions
2. Each Question carries 10 Marks
3. Answer either **a or b** from each question

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1(a)	I	List the difference between computer Organization and Architecture.	L2	CO	[4M]
	II	What is a Bus? What are different types of Buses available? Explain briefly.	L1	CO	[6M]
		(OR)			
1(b)	I	Draw the CPU and list the various registers available in CPU. Explain the purpose of each.	L1	CO	[6M]
	II	Represent decimal number 8620 in a) BCD b) Excess – 3 code.	L3	CO	[4M]
2(a)	I	What is a control word? Draw the format of control word. The codes for subtraction is 00101, AND operation 01000, Shift right operation is 10000 and for division is 10011 The binary code for R1- 000, R2- 001, R3 – 011 so on….Find out the Micro operation for the following instructions. R1 ← R2 - R3 ii) R3 ← Shr R3 iii) R5 ← R3 / R4	L3	CO	[6M]
	II	Discuss the various Shift Micro operations available.	L1	CO	[4M]
		(OR)			
2(b)	I	Let A = 1010 B = 1100. perform i) Selective set ii) selective complement and iii) selective clear operation.	L3	CO	[6M]
	II	The 8 –bit registers AR, BR, CR, DR initially have the following values. AR = 11110010 BR = 11111111 CR = 10111001 DR = 11101010 Determine the 8 – bit values in each register after the execution of the following sequence of micro operations. i) AR ← AR + BR ii) BR ← BR + 1 ii) iii) CR ← CRDR ∩ (LOGICAL AND)	L3	CO	[4M]
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3(a)		The Data is stored in the stack. Find out the Effective address (EA) and content of EA using the below addressing modes. i) Direct ii) indirect iii) immediate iv) Relative v) Indexed and vi) auto increment Modes. Register R1 = 105, Index register = 5	L4	CO	[10M]

Load AC	Address 105	Next instr	67	99	205	22	700	65	0	209	- - - - - -	324	5	15	78	33	125
100										110		205				209	

(OR)

3(b)	I	With an example explain in detail about the types of Data manipulation Instructions	L1	CO	[6M]
	II	What is an instruction format? Represent the following equation in one instruction format. (a + b) * (c / d) - p	L2	CO	[4M]
4(a)	I	List the difference between SRAM & DRAM	L2	CO	[5M]
	II	What is Cache? Why a Cache is required? The memory is referred 100 times to get the Data. In this 92 times the data is found in cache. Find out the Hit Ratio.	L3	CO	[5M]

(OR)

4(b)	I	A computer uses RAM chips of 1024 x 1 capacity. a) How many chips are needed to provide a memory capacity of 1024 bytes? b) How many chips are needed to provide a memory capacity of 16K bytes?	L3	CO	[4M]
	II	Differentiate between direct mappings and set associative mapping.	L2	CO	[6M]
5(a)	I	How many characters can be transmitted over a 1500 baud line in each of the following mode. a) Synchronous serial transmission b) asynchronous serial transmission with 02 stop bits.	L3	CO	[4M]
	II	Write brief note on the following a) I/O commands b) Isolated and Memory mapped I/O	L1	CO	[6M]

(OR)

5(b)		Explain DMA process in detail.	L1	CO	[10M]
6(a)		Explain a) time shared common bus b) Multi stage Switching Network with a proper diagram.	L1	CO	[10M]

(OR)

6(b)	I	Discuss the difference between tightly coupled and loosely coupled multiprocessors	L1	CO	[4M]
	II	Write short note on a) Synchronous b) Asynchronous Bus.	L1	CO	[6M]

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H.T.No: | | | | | | | | | | |

Course Code No: 20CS3T02

VISHNU INSTITUTE OF TECHNOLOGY::BHIMAVARAM (AUTONOMOUS)

II B. Tech I Semester (R20) - Regular & Supplementary Examinations, February - 2023

Computer Organization
(CSE & IT)

Time: 3 Hours **Max. Marks: 70M**

Note: 1. Answer all the 5 Questions
2. Each Question carries 14 Marks
3. Answer any one question from each unit

UNIT – I

1	a	What is Basic Structure of Computer? List the different types of Computers	L1	CO1	[7M]
	b	Draw the connection between processor and memory and mention the functions of each component in the connection.	L2	CO1	[7M]
		(OR)			
2	a	Explain Bus Structure of a computer with diagram?	L3	CO1	[7M]
	b	What is performance measurement? Explain the overall SPEC rating for the computer in a program suite	L1	CO1	[7M]

UNIT – II

3	a	Define addressing modes. Give the details of different addressing modes.	L1	CO2	[7M]
	b	With a neat diagram, describe the input and output operations	L2	CO2	[7M]
		(OR)			
4	a	Explain different types of arithmetic and Logical Instructions	L3	CO2	[7M]
	b	What is stack frame? Explain a commonly used layout for information in a subroutine stack frame.	L1	CO2	[7M]

UNIT – III

5	a	What are the different methods of DMA? Explain them in brief.	L1	CO3	[7M]
	b	Explain tree structure of USB with split bus operation	L2	CO3	[7M]
		(OR)			
6	a	Explain Peripheral Component Interconnection	L3	CO3	[7M]
	b	Define two types of SCSI controllers.	L1	CO3	[7M]

UNIT – IV

7	a	What is Asynchronous Ram and Synchchronus Ram	L1	CO4	[7M]
	b	Describe the principles of magnetic disk	L2	CO4	[7M]
		(OR)			

8	a	Explain different types of ROMS?	L3	CO4	[7M]
	b	What is virtual memory? With a diagram, explain how virtual memory address is translated.	L1	CO4	[7M]

UNIT – V

9	a	What is Register Transfer Explain with diagram	L1	CO5	[7M]
	b	Draw and explain multiple bus organization. Explain its advantages	L2	CO5	[7M]
		(OR)			
10	a	Explain Single Bus organization	L3	CO5	[7M]
	b	What is Multiple Bus organization Explain with diagram	L1	CO5	[7M]

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