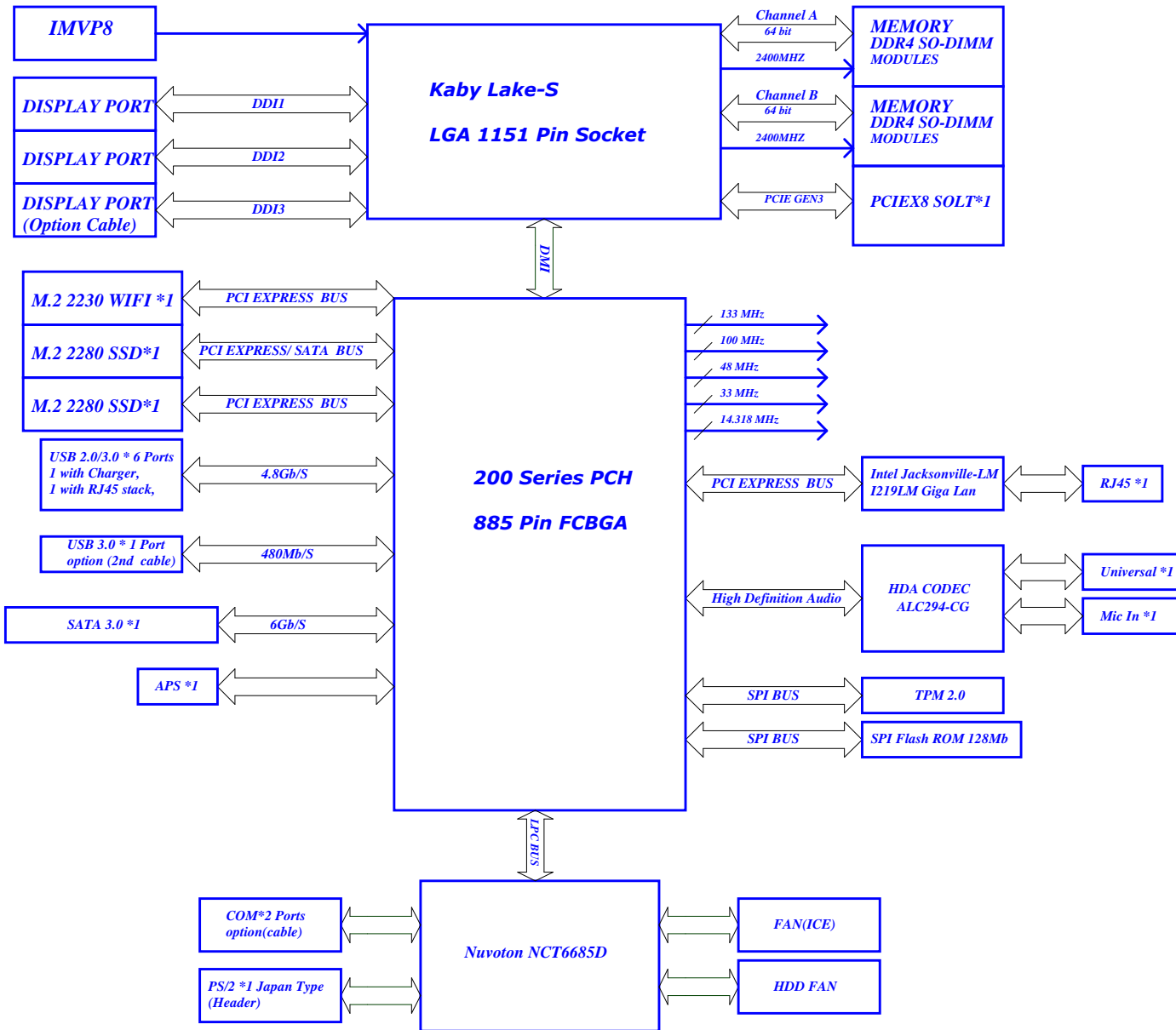


JC113/IQ270IH1

Q270 35W LT SVID/SSID: 17AA/310B
 Q270 65W LT SVID/SSID: 17AA/310C
 B250 35W LT SVID/SSID: 17AA/3111

X03 : 07/12/2016Y



PAGE	TITLE
01	Block Diagram
02	Power Sequence
03	Power Delivery Map
04	CPU-1: MSIC
05	CPU-2: FDI/PCIE/DMI
06	CPU-3: DDR4 CHA
07	CPU-4: DDR4 CHB
08	CPU-5: Power
09	CPU-6: GND
10	DDR4 CHA SO-DIMM1
11	DDR4 CHB SO-DIMM3
12	PCH-1: DMI/ USB/ LPC/ PCIE
13	PCH-2: PCIE/ SATA/ FAN
14	PCH-3: HDA/ RTC/ SMB/ SPI
15	PCH-4: Display
16	PCH-5: Clock
17	PCH-6: Power 1
18	PCH-8: GND
19	CMOS Clear / Battery/ HDR
20	DSW
21	SPI ROM
22	Display Port B
23	Display Port C
24	Display Port D
25	Audio Codec - ALC294-CG
26	Audio Jack Line I-O/ Mic in
27	SIO IT8733F
28	COM Port/ PS/2/ FAN CTRL
29	TPM - TCG 2.0
30	LAN - Jacksonville_i219LM
31	RJ45
32	Rear USB3e ODD
33	Rear USB3 x 2
34	Front USB3 Charger x2
35	INT USB3.0 / INT USB2.0
36	M.2 2230-E WIFI/ BT
37	M.2 2280-M SSD-2
38	M.2 2280-M SSD-1
39	Buzzer/Sata Cable/Debug Port
40	Battery Header
41	PWRGD & Bleed Off
42	PCIEX8
43	Thunderbolt
44	XDP
45	Button/ LED
46	SM BUS/Thermal Sensing/APS
47	Mounting Hole/ PCB/ Metal
48	+20V_S5_ADP
49	+5V_S5/+3V3_S5
50	+3V3_DSW/+5V/+3V3
51	+12V
52	VCORE CONTROLLER
53	VCCIA Output
54	VCCGT Output
55	+1V2_DDR / +0V6_VTT
56	+2V5_VPP
57	+1V0_PCH_PRIME
58	+VCCIO
59	+VCCSA
60	+5V_USB
61	INA300
62	PCH GPIO TABLE
63	STRAPPING PIN
64	SIO GPIO TABLE
65	RESET MAP-CLOCK DIAGRAM
66	SMBUS Block Diagram
67	Change List

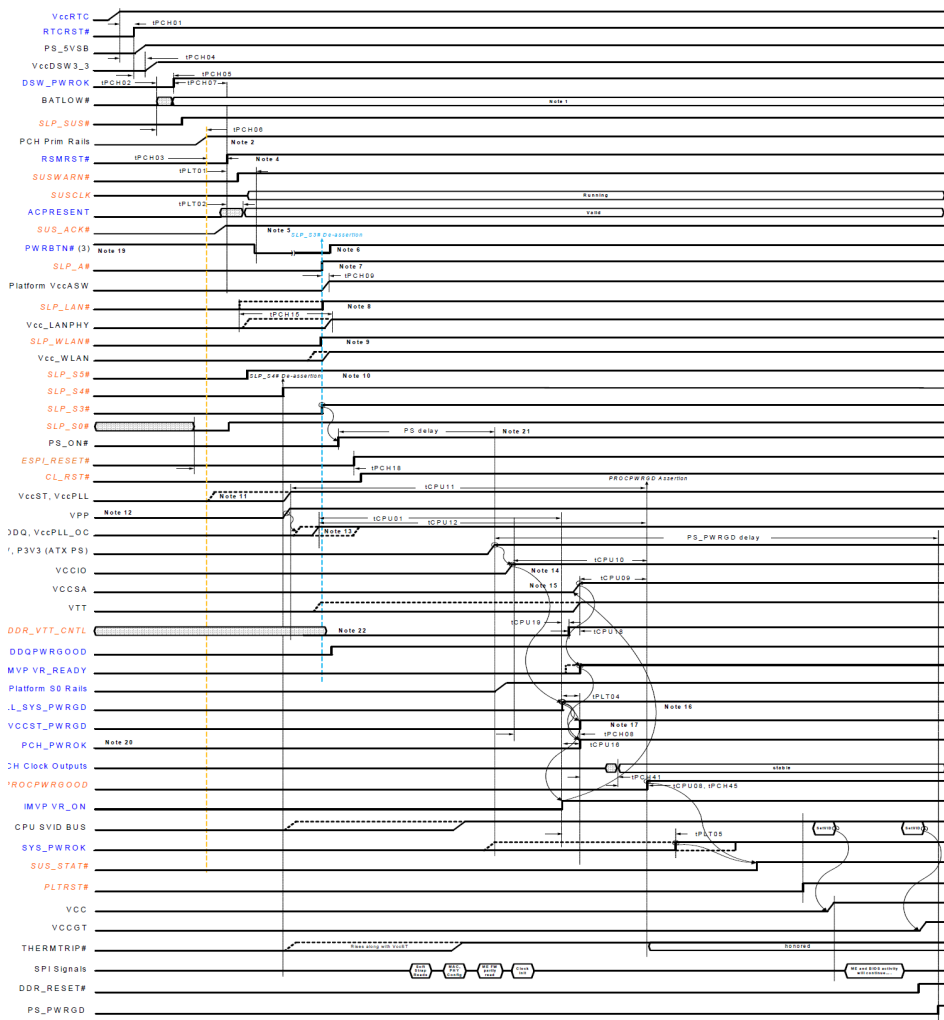


Figure 40-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

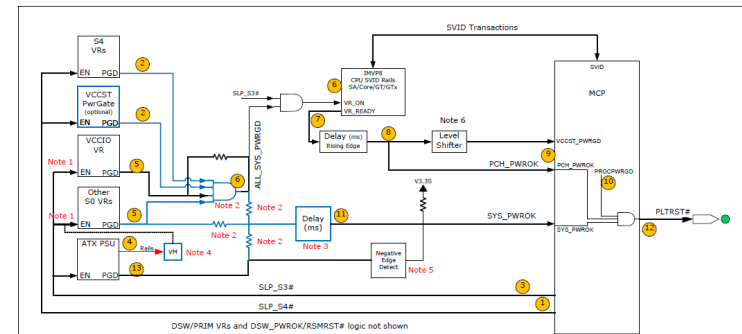


Figure 40-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation

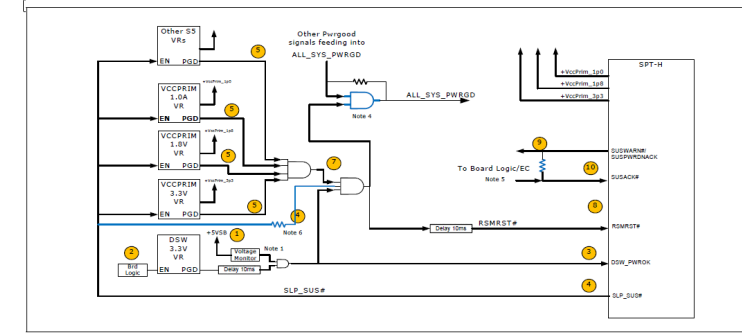


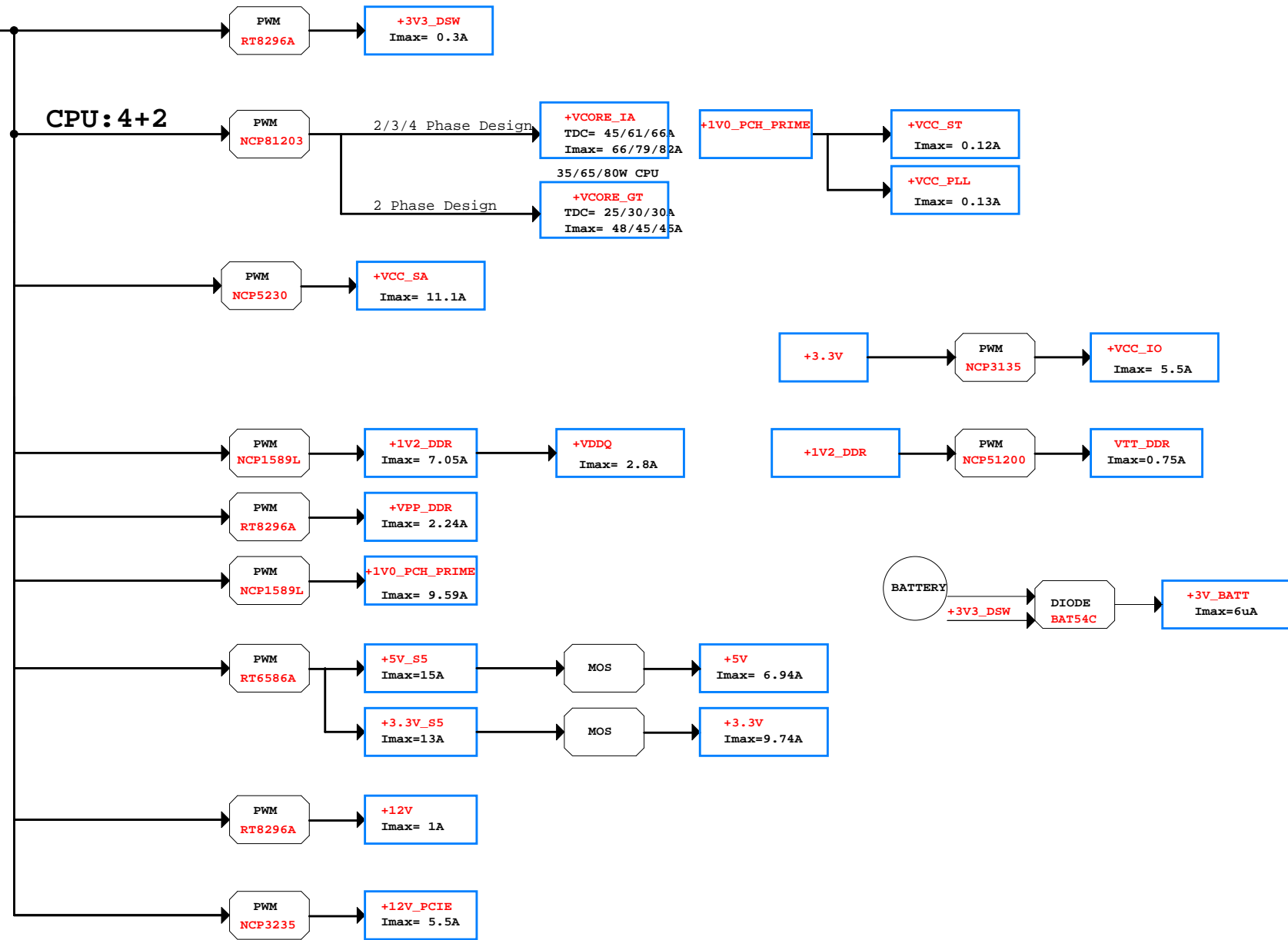
Table 40-3: System with M3 State Supported (Sheet 1 of 2)

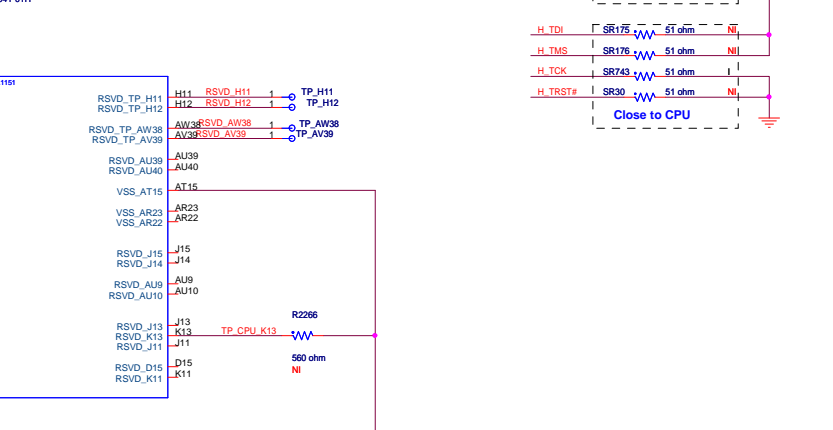
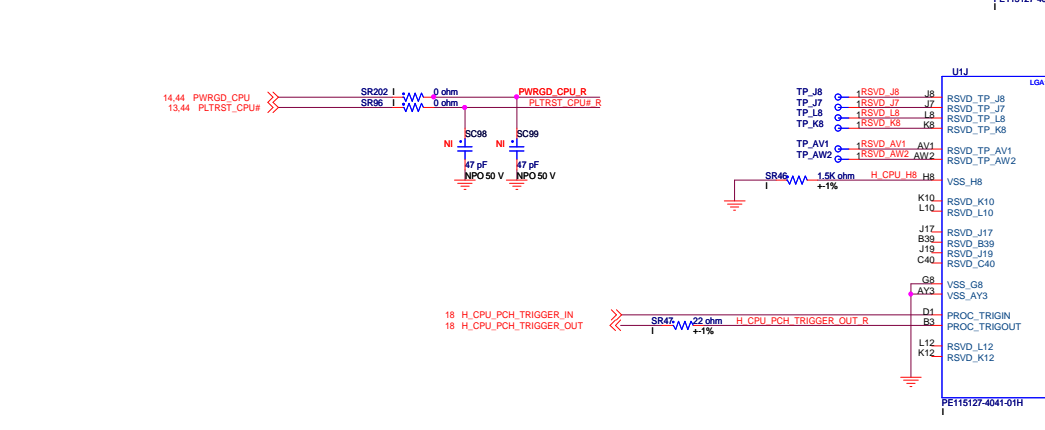
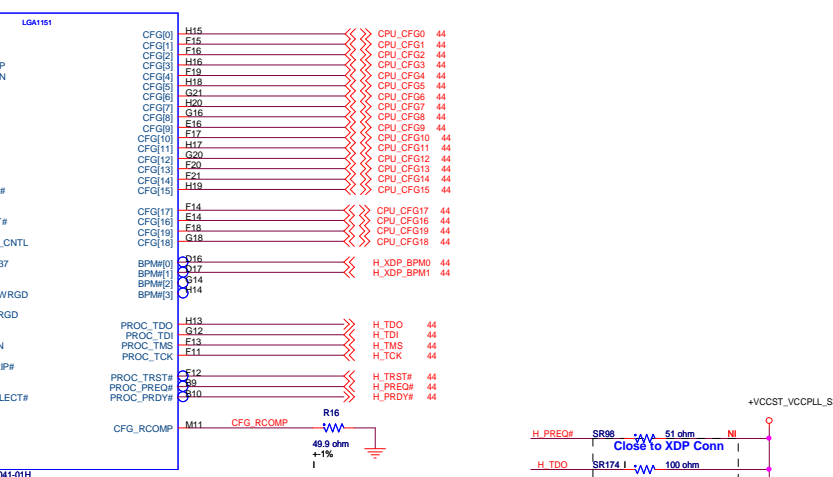
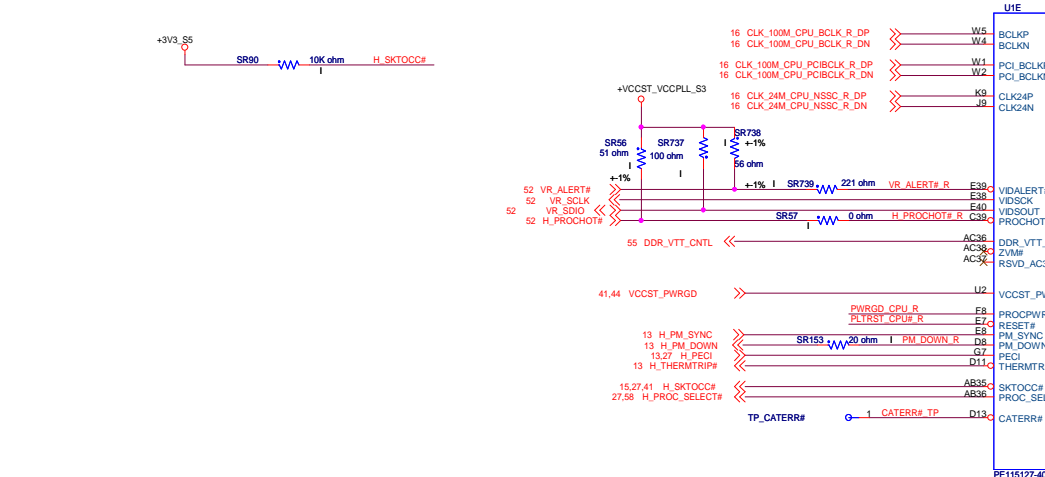
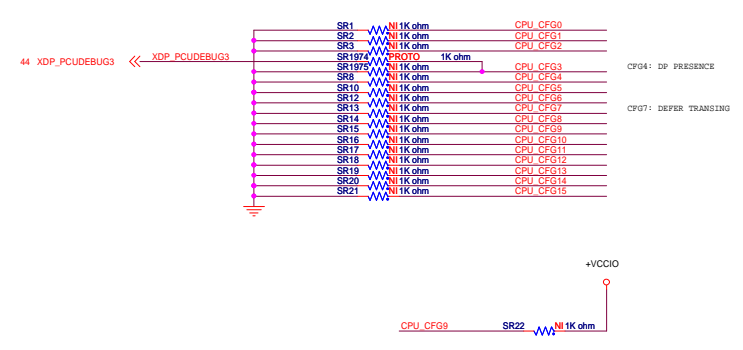
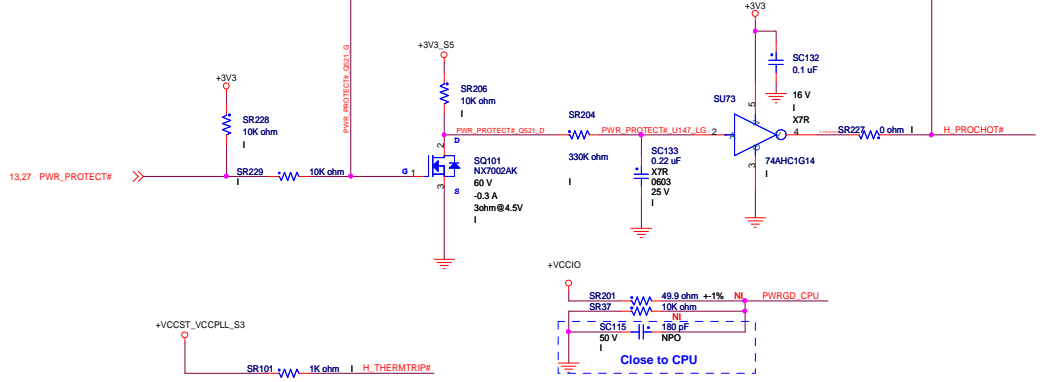
Rails	S0/M0	S3/M3	S4/M3	S5/M3	Sx/M-Off	Deep S3	Deep S4/S5	G3 ¹
RTC Well	ON	ON	ON	ON	ON	ON	ON	ON
PS_SVSB	ON	ON	ON	ON	ON	ON	ON	ON ¹⁴
3.3V_DSW	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC) ¹²	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	ON	ON	ON	ON	ON	OFF	OFF	No Power
V3.3A	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.8A ¹³	ON	ON	ON	ON	ON	OFF	OFF	No Power
V1.0A	ON	ON	ON	ON	ON	OFF	OFF	No Power
VCCOPC_1p8	ON	ON ¹⁵	ON ¹⁵	ON ¹⁵	ON ¹⁵	OFF	OFF	No Power
V3.3M ³	ON	ON ¹¹	ON ¹¹	ON ¹¹	OFF	OFF	OFF	No Power
V1.8M ³	ON	ON ¹¹	ON ¹¹	ON ¹¹	OFF	OFF	OFF	No Power
VDDQ	ON	ON	OFF	OFF	OFF	ON	ON	No Power
V1.8U/V2.5U	ON	ON	OFF	OFF	OFF	ON	OFF	No Power
VCCST	ON	ON	OFF ⁵	OFF ⁵	OFF ⁵	OFF	OFF	No Power
VCCPLL	ON	ON ⁷	OFF ⁵	OFF ⁵	OFF ⁵	OFF ⁵	OFF	No Power
VCCPLL_OC	ON	ON ⁸	OFF	OFF	OFF	OFF	OFF ⁸	No Power
V3.3S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V5.0S	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCC	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT/VCCGTx	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCIO	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCSA	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCOPC	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCOPPIO	ON/OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power
P12V, PSV, P3V3	ON	OFF	OFF	OFF	OFF	OFF	OFF	No Power

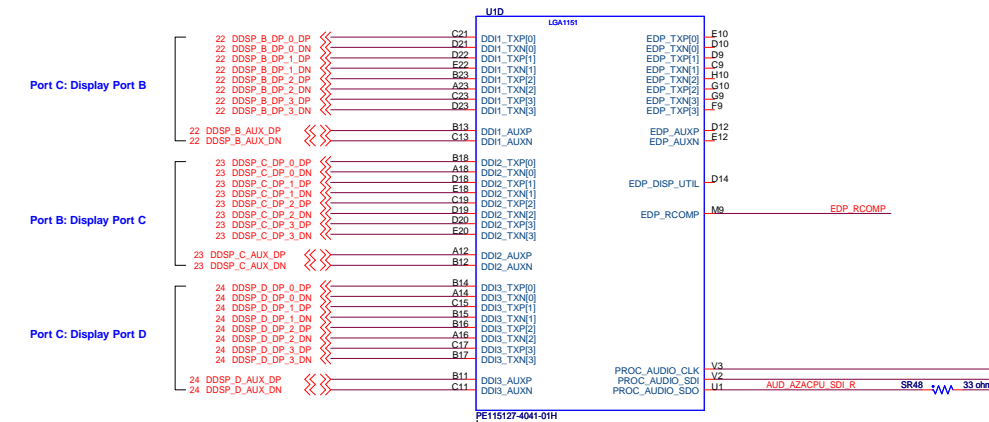
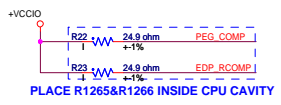
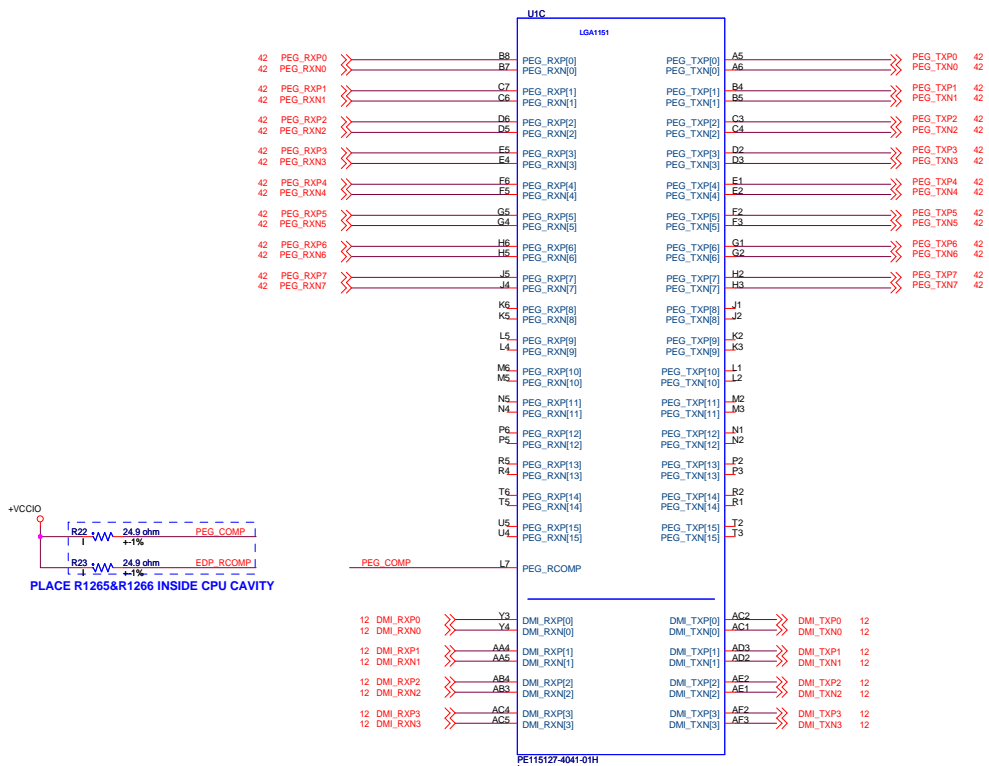
POWER CONN

+20V_S5_ADP
 I_{max}= 3.25A (65W)
 I_{max}= 4.5A (90W)

CPU: 4+2





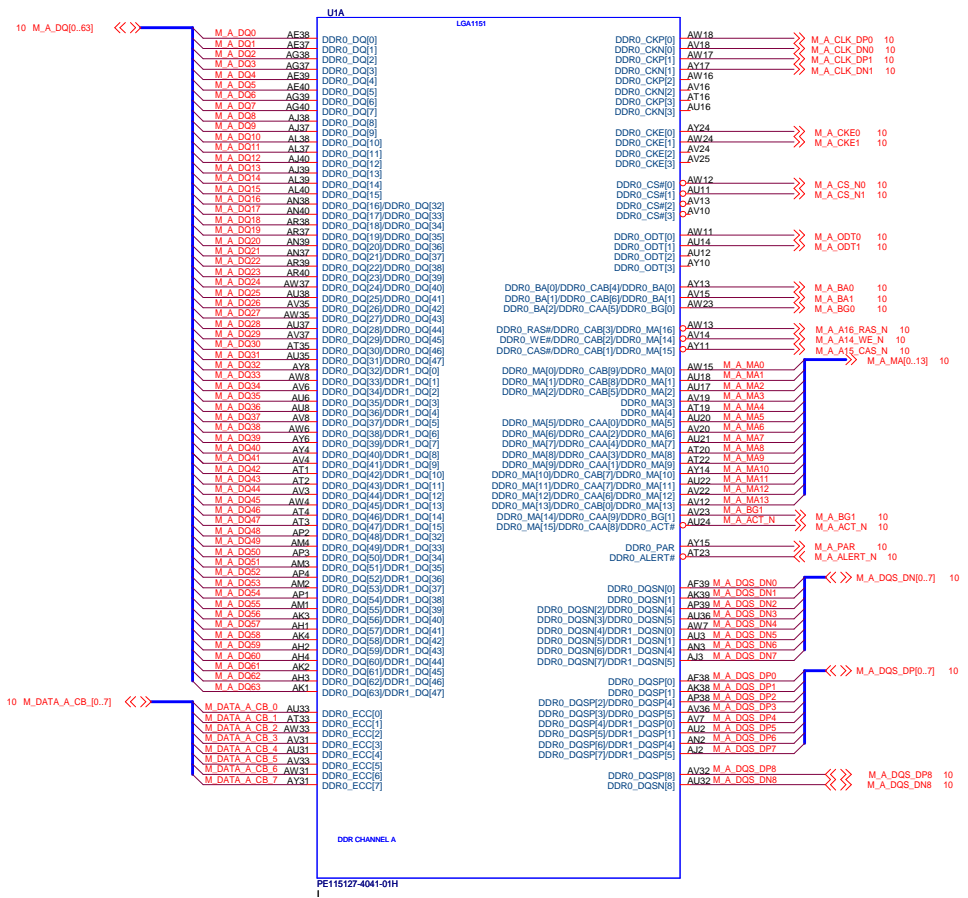


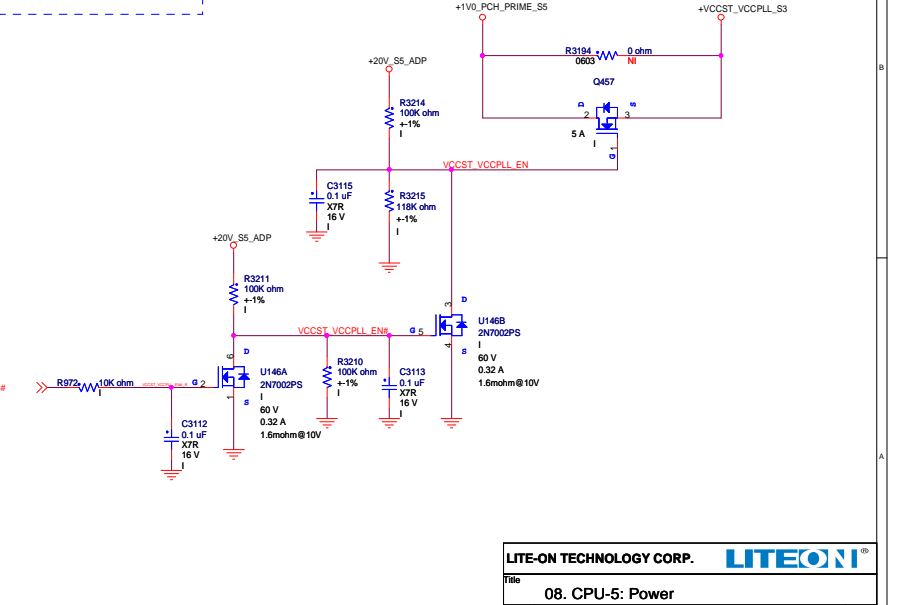
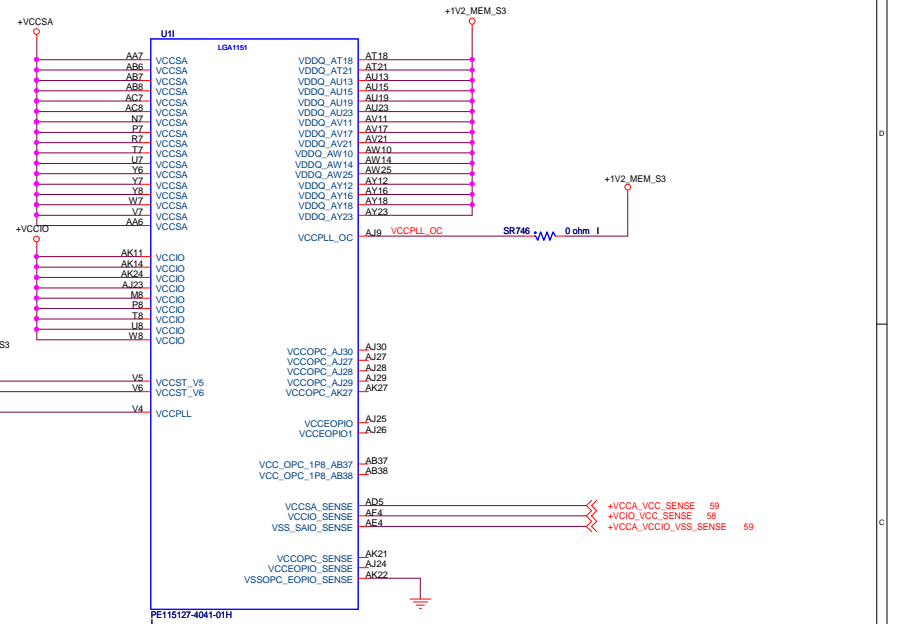
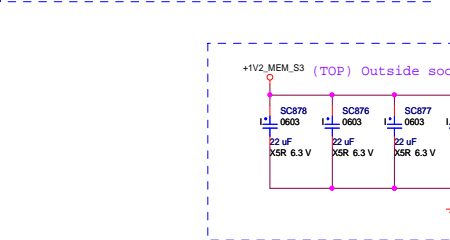
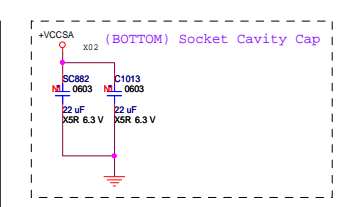
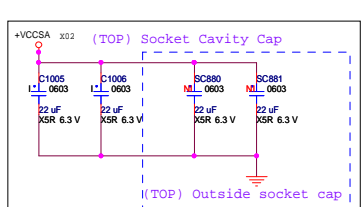
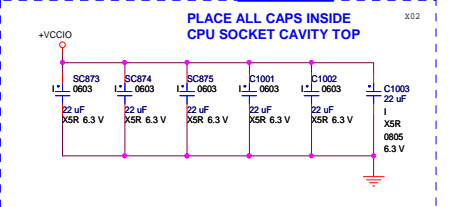
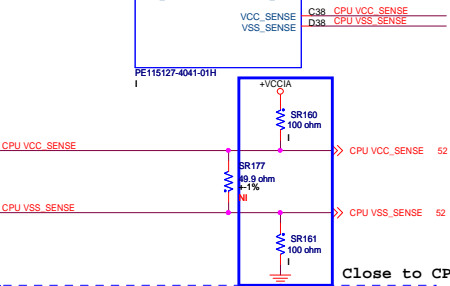
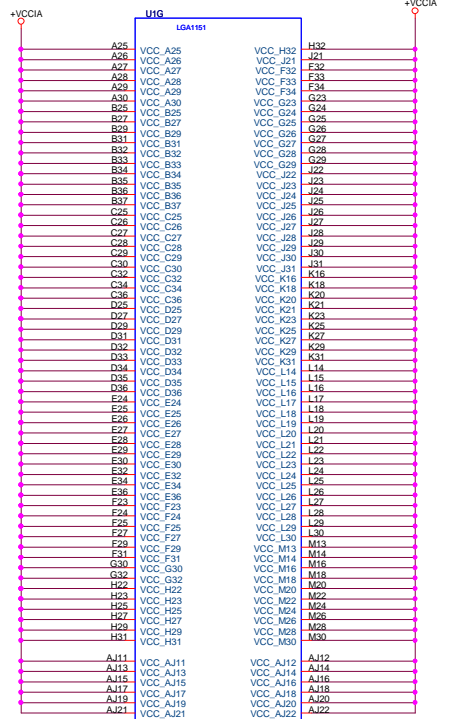
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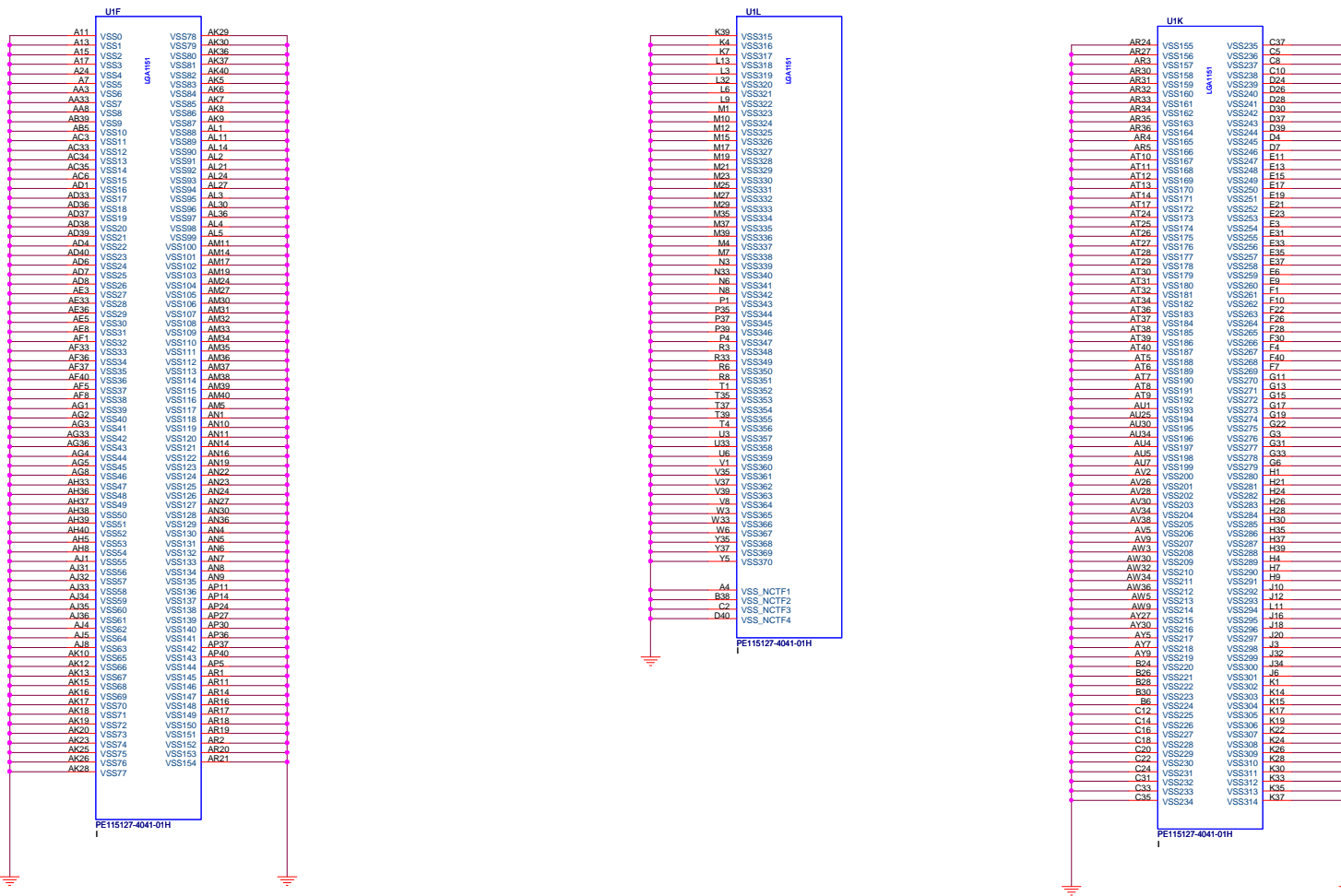
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Size C Document Number JC113 Rev X03

Date: Friday, August 26, 2016 Sheet 5 of 67







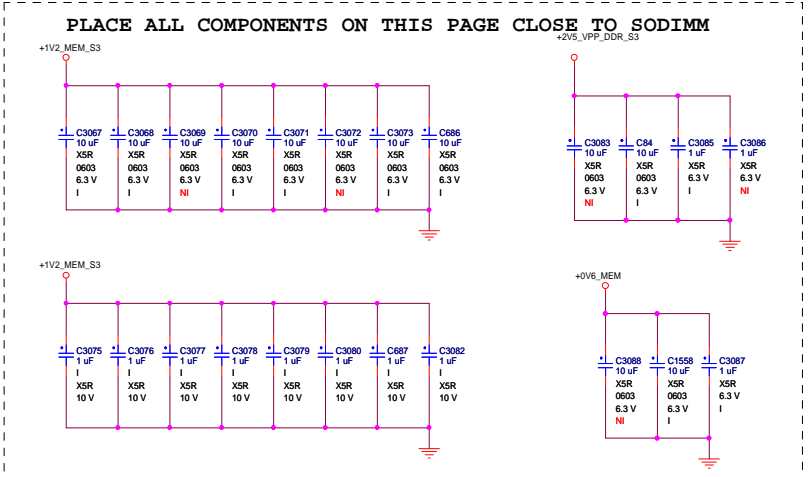
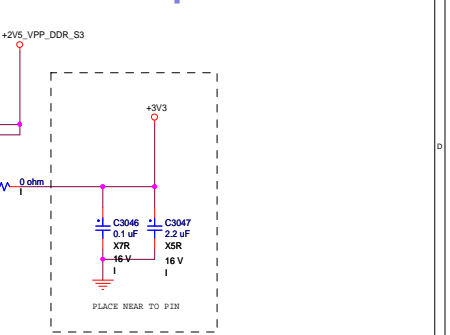
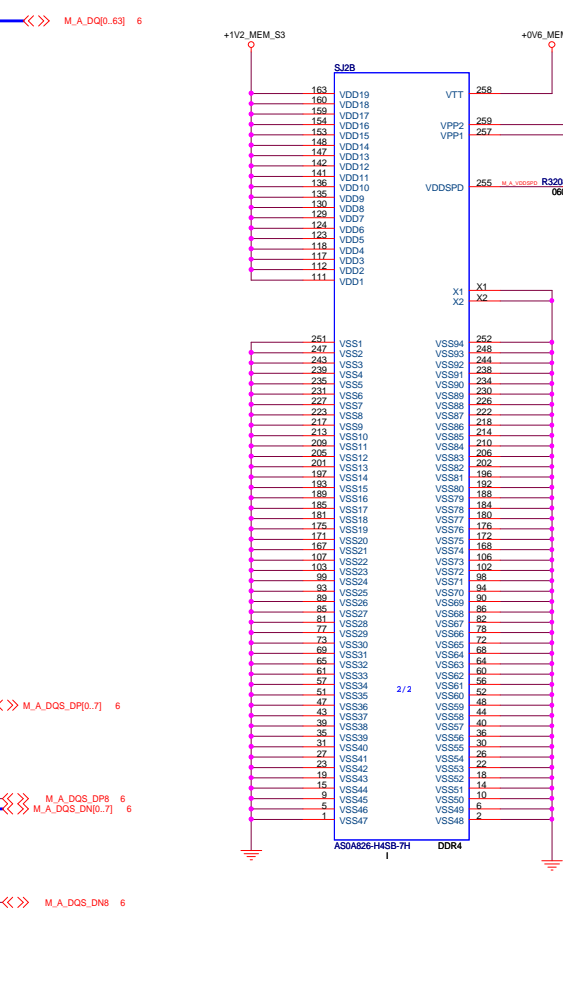
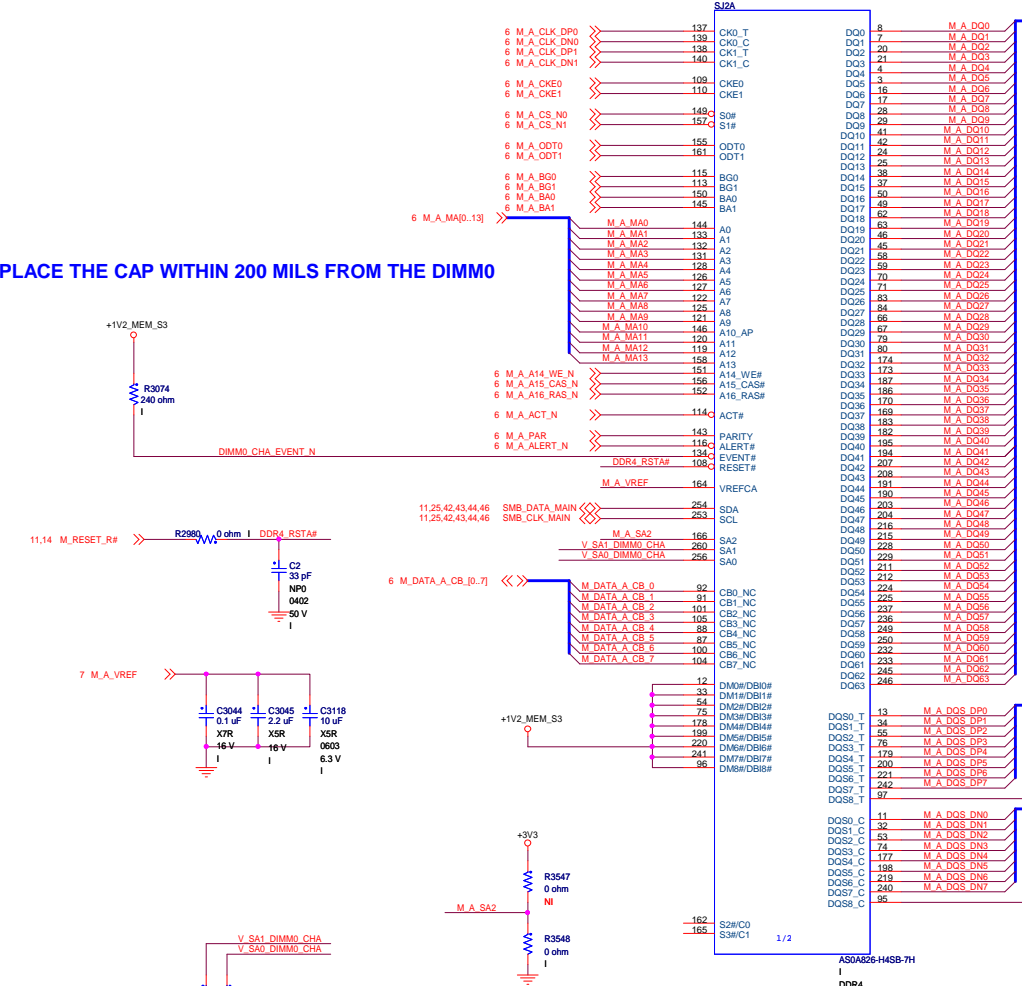
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Title: 09. CPU-6: GND

Size C Document Number JC113 Rev X03

Date: Friday, August 26, 2016 Sheet 9 of 67

PLACE THE CAP WITHIN 200 MILS FROM THE DIMM0

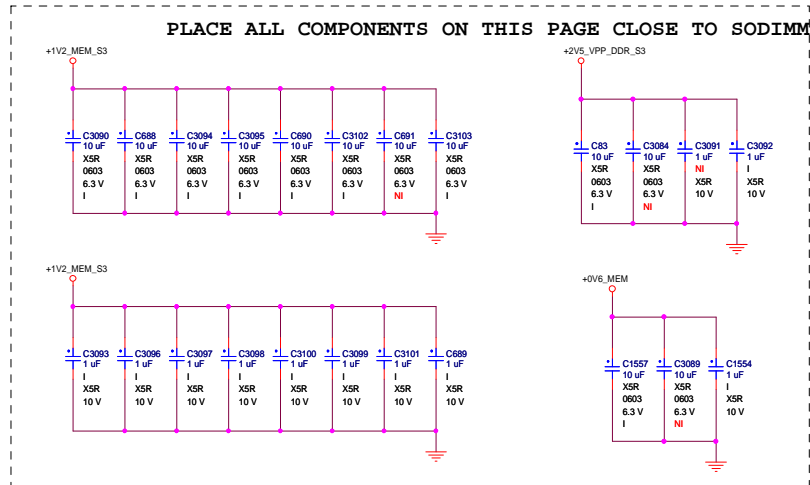
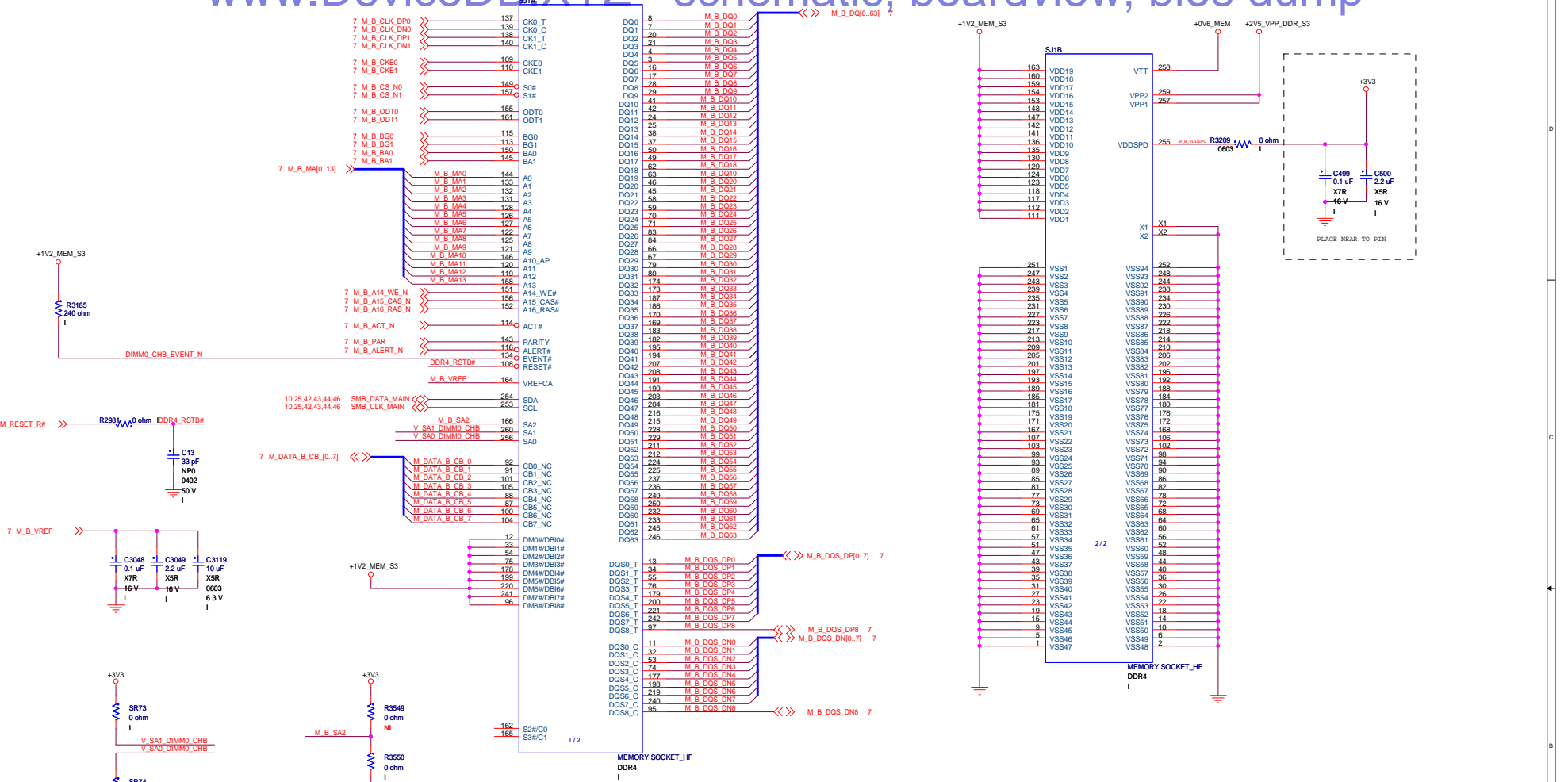


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Title: 10. DDR4 CHA SO-DIMM1

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Date: Friday, August 26, 2016 Sheet 10 of 67

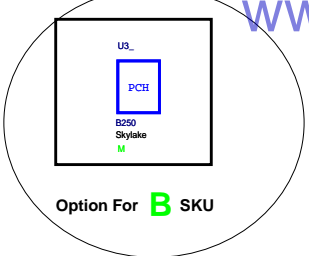


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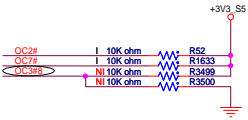
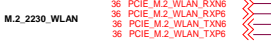
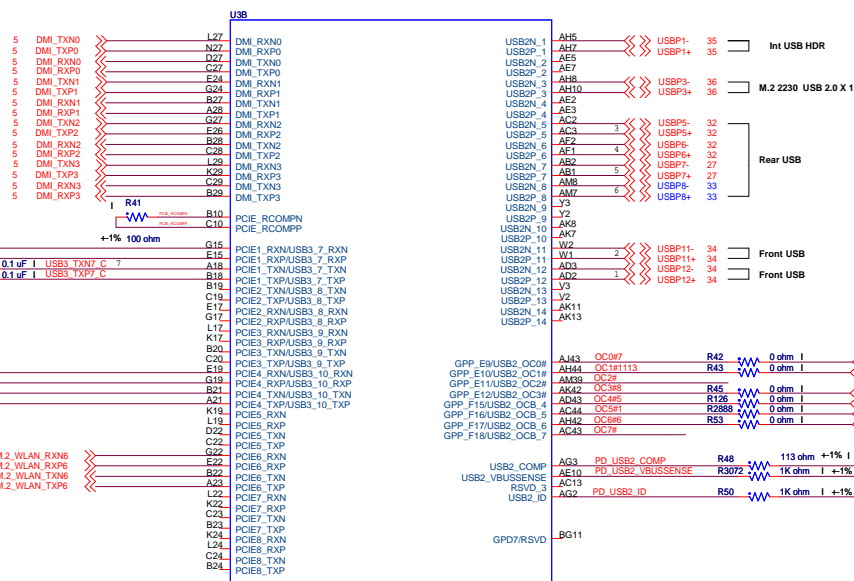
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Size C Document Number JC113 Rev X03

Date: Friday, August 26, 2016 Sheet 11 of 67

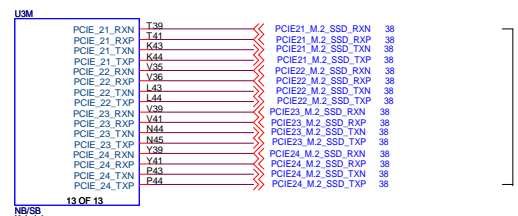
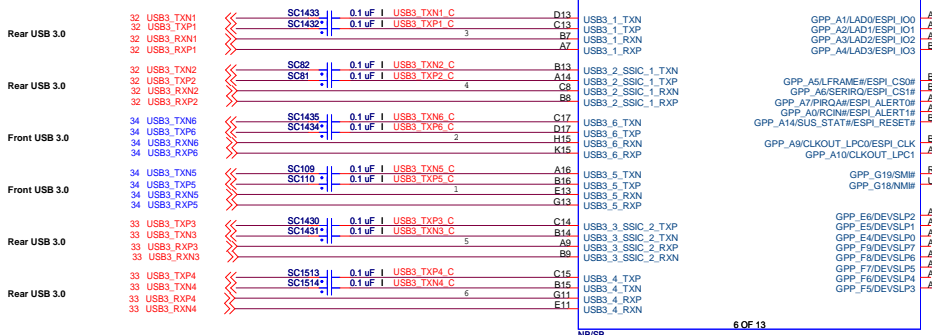


Option For B SKU



2 OF 13

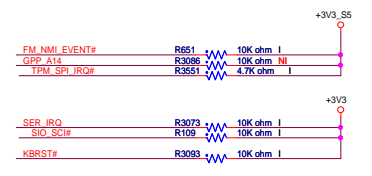
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KabyLake
A0
DUM
Pre-QS Q270

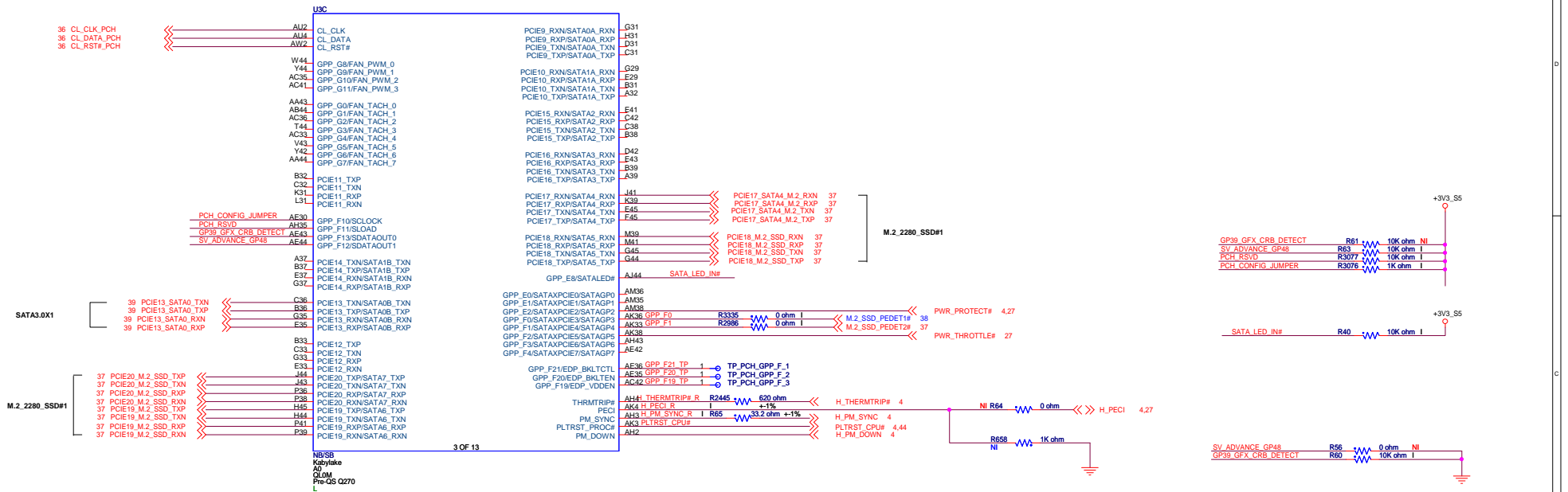


M.2 2280_SSD#2

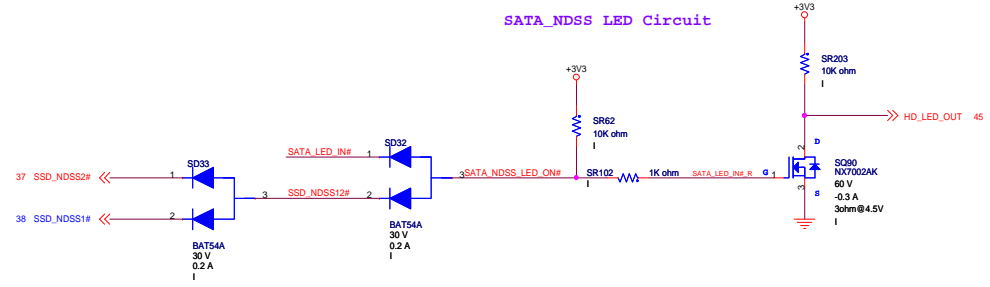
13 OF 13

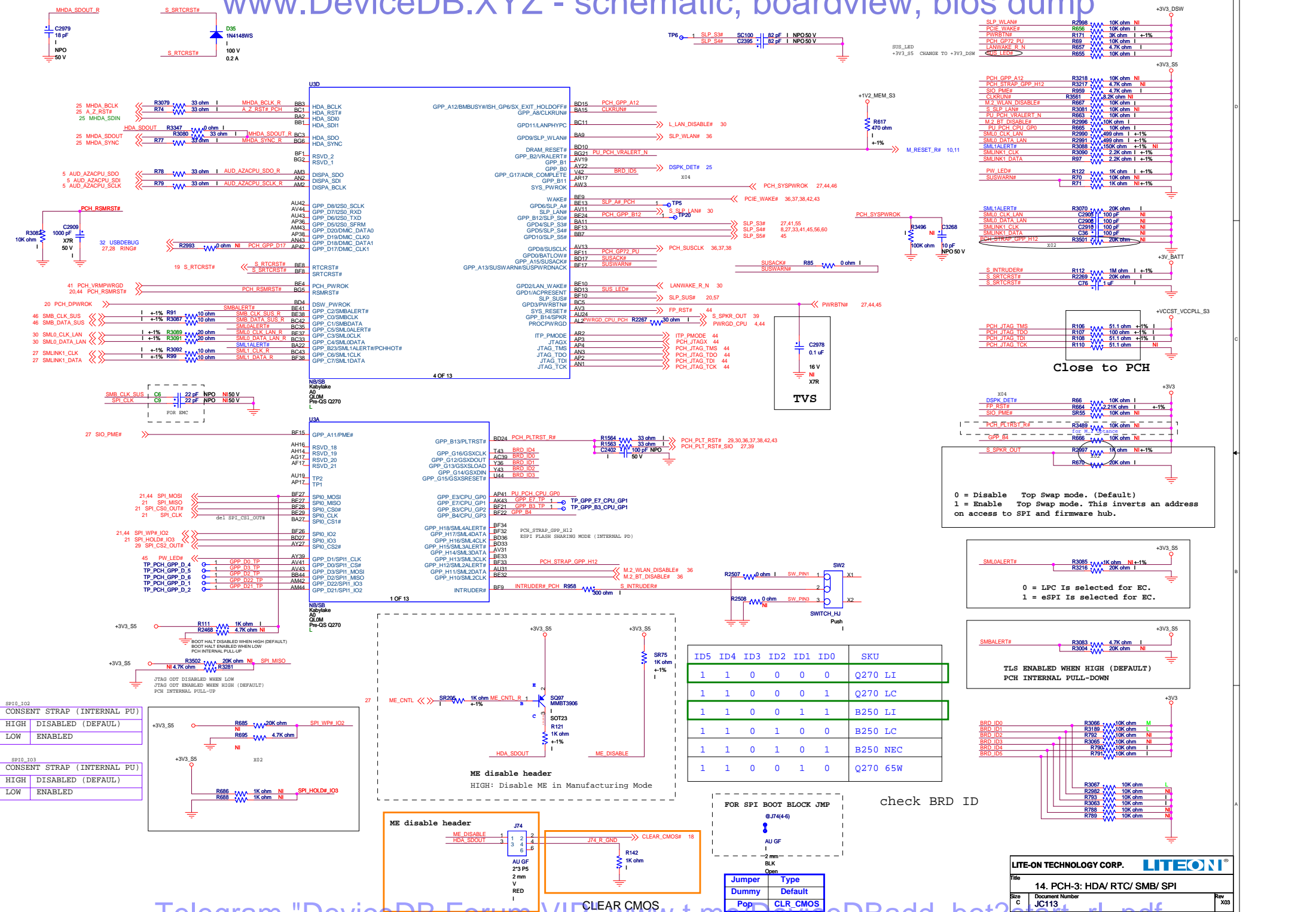
USB
KabyLake
A0
DUM
Pre-QS Q270





SATA_NDSS LED Circuit





Close to PCH

0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode. This inverts an address on access to SPI and firmware hub.

0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

0 = TLS ENABLED WHEN HIGH (DEFAULT)
1 = PCH INTERNAL PULL-DOWN

ID5	ID4	ID3	ID2	ID1	ID0	SKU
1	1	0	0	0	0	Q270
1	1	0	0	0	1	Q270 LC
1	1	0	0	1	1	B250
1	1	0	1	0	0	B250 LC
1	1	0	1	0	1	B250 NEC
1	1	0	0	1	0	Q270 65W

check BRD ID

FOR SPI BOOT BLOCK JMP @J74(4-6)

Jumper	Type
Dummy <td>Default</td>	Default
Pop	CLR_CMOS

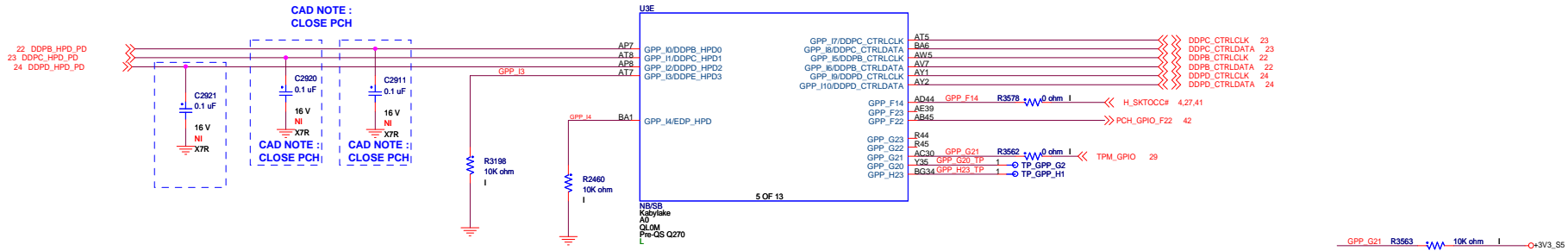
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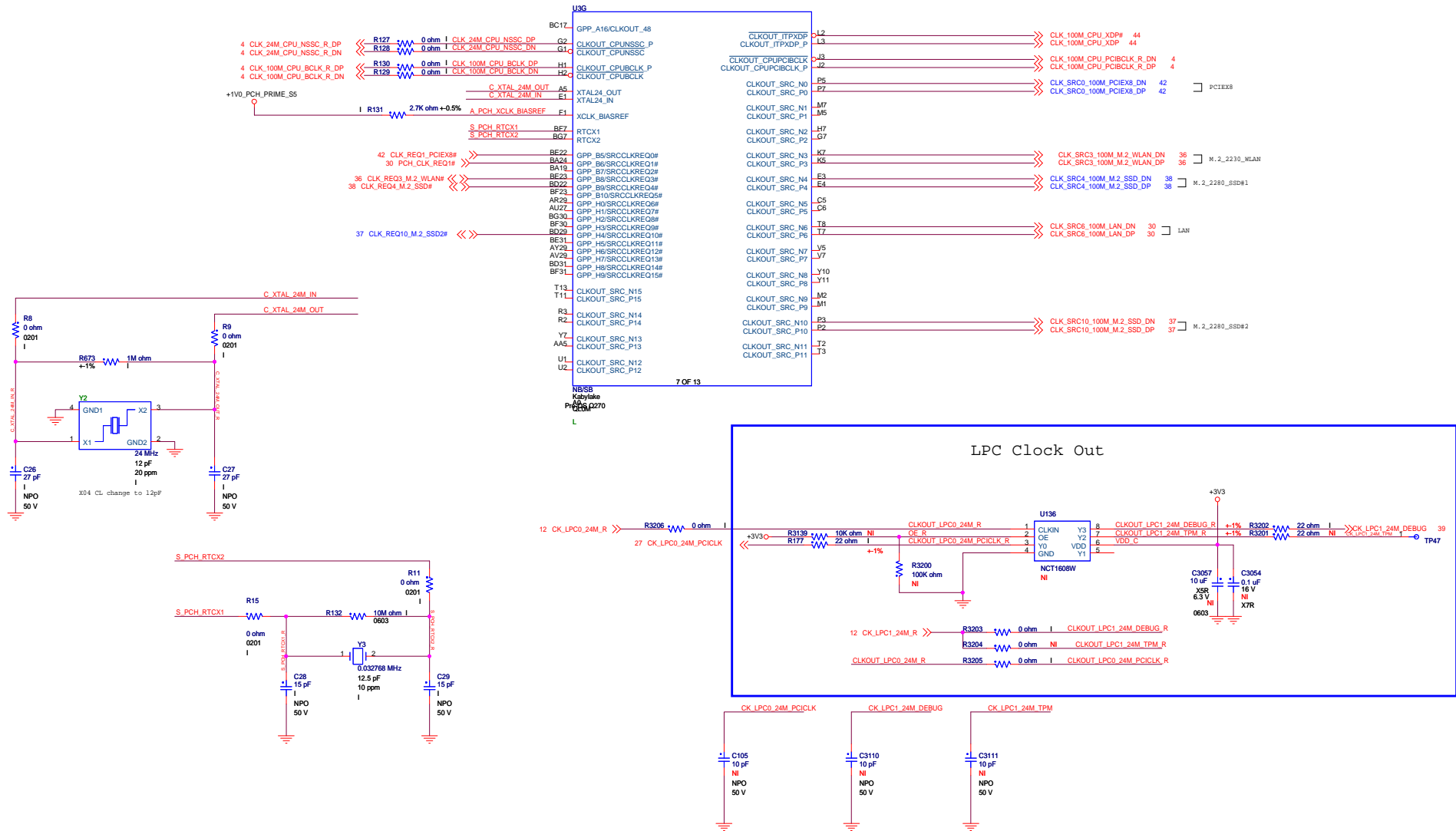
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Document Number: JC113

Date: Friday, August 26, 2016

Page: 14 of 67

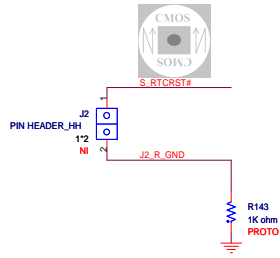
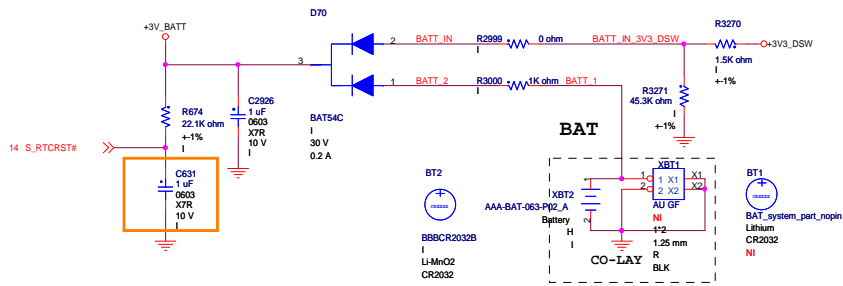




A25	VSS_1	VSS_299	A42
A30	VSS_4	VSS_300	D45
AV38	VSS_297	VSS_301	B044
VSS_157	VSS_302	VSS_302	BE44
AV45	VSS_159	VSS_303	BE45
AV8	VSS_161	VSS_304	BE2
AY11	VSS_163	VSS_305	W29
AY19	VSS_165	VSS_3	A35
VSS_169	VSS_10	VSS_170	BG23
AY4	VSS_171	VSS_171	BG28
VSS_175	VSS_19	VSS_172	BQ32
B3	VSS_176	VSS_173	BQ37
B35	VSS_177	VSS_174	M41
B4	VSS_182	VSS_175	BG40
B41	VSS_184	VSS_176	AV28
BA13	VSS_186	VSS_177	C1
BA17	VSS_188	VSS_178	AA21
BA20	VSS_189	VSS_179	AA28
BA31	VSS_192	VSS_180	AA28
BA4	VSS_194	VSS_181	AA29
BA42	VSS_198	VSS_182	AA28
BC38	VSS_200	VSS_183	AA29
BC39	VSS_204	VSS_184	AA28
BD11	VSS_206	VSS_185	AA29
BD16	VSS_208	VSS_186	AA28
B02	VSS_210	VSS_187	AA29
BD21	VSS_212	VSS_188	AA28
BD25	VSS_214	VSS_189	AA29
F2	VSS_216	VSS_190	AA28
E31	VSS_218	VSS_191	AA29
E9	VSS_220	VSS_192	AA28
F39	VSS_222	VSS_193	AA29
F43	VSS_224	VSS_194	AA28
G4	VSS_226	VSS_195	AA29
G40	VSS_230	VSS_196	AA28
G42	VSS_234	VSS_197	AA29
H27	VSS_236	VSS_198	AA28
H9	VSS_238	VSS_199	AA29
H11	VSS_240	VSS_200	AA28
H19	VSS_242	VSS_201	AA29
H22	VSS_246	VSS_202	AA28
H24	VSS_248	VSS_203	AA29
H27	VSS_250	VSS_204	AA28
H33	VSS_252	VSS_205	AA29
H36	VSS_254	VSS_206	AA28
H42	VSS_256	VSS_207	AA29
H49	VSS_264	VSS_208	AA28
I4	VSS_266	VSS_209	AA29
M38	VSS_270	VSS_210	AA28
M4	VSS_272	VSS_211	AA29
M9	VSS_274	VSS_212	AA28
N13	VSS_276	VSS_213	AA29
N15	VSS_278	VSS_214	AA28
N22	VSS_286	VSS_215	AA29
N24	VSS_288	VSS_216	AA28
N31	VSS_289	VSS_217	AA29
N42	VSS_291	VSS_218	AA28
N49	VSS_293	VSS_219	AA29
P12	VSS_295	VSS_220	AA28
AV35	VSS_155	VSS_221	AA29

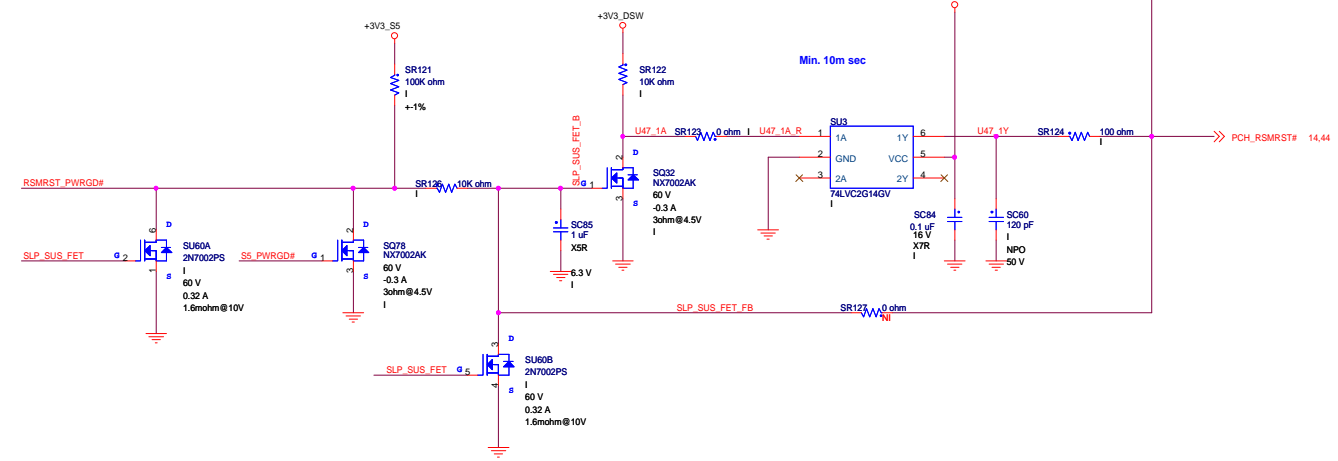
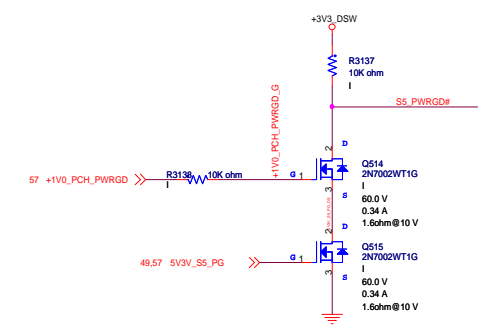
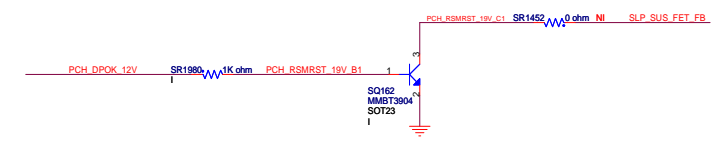
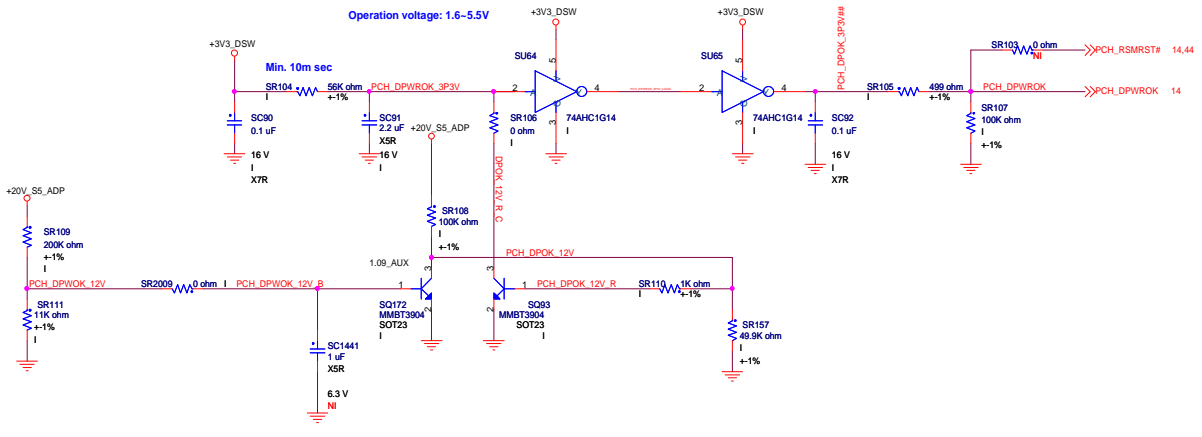
B039	VSS_156	VSS_222	B460
B07	VSS_160	VSS_223	AB21
BE2	VSS_162	VSS_224	AB25
BF43	VSS_164	VSS_225	AB29
BF5	VSS_166	VSS_226	AB4
BG18	VSS_168	VSS_227	AC10
W29	VSS_170	VSS_228	AC11
BG28	VSS_172	VSS_229	AC14
BQ32	VSS_174	VSS_230	AC16
BQ37	VSS_176	VSS_231	AC38
M41	VSS_178	VSS_232	AC4
BG40	VSS_180	VSS_233	AC5
AV28	VSS_182	VSS_234	AC7
C1	VSS_184	VSS_235	AC8
AA21	VSS_186	VSS_236	AD1
AA28	VSS_188	VSS_237	AD18
AA29	VSS_190	VSS_238	AD20
AA28	VSS_192	VSS_239	AD21
AA29	VSS_194	VSS_240	AD25
AA28	VSS_196	VSS_241	AD29
AA29	VSS_198	VSS_242	AD45
AA28	VSS_200	VSS_243	AE11
AA29	VSS_202	VSS_244	AE14
AA28	VSS_204	VSS_245	AE32
AA29	VSS_206	VSS_246	AE38
AA28	VSS_208	VSS_247	AK29
AA29	VSS_210	VSS_248	AK30
AA28	VSS_212	VSS_249	AK32
AA29	VSS_214	VSS_250	AK35
AA28	VSS_216	VSS_251	AK39
AA29	VSS_218	VSS_252	AL4
AA28	VSS_220	VSS_253	K45
AA29	VSS_222	VSS_254	K38
AA28	VSS_224	VSS_255	K36
AA29	VSS_226	VSS_256	K35
AA28	VSS_228	VSS_257	K33
AA29	VSS_230	VSS_258	K3
AA28	VSS_232	VSS_259	K27
AA29	VSS_234	VSS_260	K13
AA28	VSS_236	VSS_261	K11
AA29	VSS_238	VSS_262	AM29
AA28	VSS_240	VSS_263	AM29
AA29	VSS_242	VSS_264	AM33
AA28	VSS_244	VSS_265	AM3
AA29	VSS_246	VSS_266	AM11
AA28	VSS_248	VSS_267	AM13
AA29	VSS_250	VSS_268	AM17
AA28	VSS_252	VSS_269	AM19
AA29	VSS_254	VSS_270	AM24
AA28	VSS_256	VSS_271	AM27
AA29	VSS_258	VSS_272	AM29
AA28	VSS_260	VSS_273	AM32
AA29	VSS_262	VSS_274	AM33
AA28	VSS_264	VSS_275	AM3
AA29	VSS_266	VSS_276	AM1
AA28	VSS_268	VSS_277	AM4
AA29	VSS_270	VSS_278	AM5
AA28	VSS_272	VSS_279	AM6
AA29	VSS_274	VSS_280	AM7
AA28	VSS_276	VSS_281	AM8
AA29	VSS_278	VSS_282	AM9
AA28	VSS_280	VSS_283	AM10
AA29	VSS_282	VSS_284	AM11
AA28	VSS_284	VSS_285	AM12
AA29	VSS_286	VSS_286	AM13
AA28	VSS_288	VSS_287	AM14
AA29	VSS_290	VSS_288	AM15
AA28	VSS_292	VSS_289	AM16
AA29	VSS_294	VSS_290	AM17
AA28	VSS_296	VSS_291	AM18
AA29	VSS_298	VSS_292	AM19
AA28	VSS_300	VSS_293	AM20
AA29	VSS_302	VSS_294	AM21
AA28	VSS_304	VSS_295	AM22
AA29	VSS_306	VSS_296	AM23
AA28	VSS_308	VSS_297	AM24
AA29	VSS_310	VSS_298	AM25
AA28	VSS_312	VSS_299	AM26
AA29	VSS_314	VSS_300	AM27
AA28	VSS_316	VSS_301	AM28
AA29	VSS_318	VSS_302	AM29
AA28	VSS_320	VSS_303	AM30
AA29	VSS_322	VSS_304	AM31
AA28	VSS_324	VSS_305	AM32
AA29	VSS_326	VSS_306	AM33
AA28	VSS_328	VSS_307	AM34
AA29	VSS_330	VSS_308	AM35
AA28	VSS_332	VSS_309	AM36
AA29	VSS_334	VSS_310	AM37
AA28	VSS_336	VSS_311	AM38
AA29	VSS_338	VSS_312	AM39
AA28	VSS_340	VSS_313	AM40
AA29	VSS_342	VSS_314	AM41
AA28	VSS_344	VSS_315	AM42
AA29	VSS_346	VSS_316	AM43
AA28	VSS_348	VSS_317	AM44
AA29	VSS_350	VSS_318	AM45
AA28	VSS_352	VSS_319	AM46
AA29	VSS_354	VSS_320	AM47
AA28	VSS_356	VSS_321	AM48
AA29	VSS_358	VSS_322	AM49
AA28	VSS_360	VSS_323	AM50
AA29	VSS_362	VSS_324	AM51
AA28	VSS_364	VSS_325	AM52
AA29	VSS_366	VSS_326	AM53
AA28	VSS_368	VSS_327	AM54
AA29	VSS_370	VSS_328	AM55
AA28	VSS_372	VSS_329	AM56
AA29	VSS_374	VSS_330	AM57
AA28	VSS_376	VSS_331	AM58
AA29	VSS_378	VSS_332	AM59
AA28	VSS_380	VSS_333	AM60
AA29	VSS_382	VSS_334	AM61
AA28	VSS_384	VSS_335	AM62
AA29	VSS_386	VSS_336	AM63
AA28	VSS_388	VSS_337	AM64
AA29	VSS_390	VSS_338	AM65
AA28	VSS_392	VSS_339	AM66
AA29	VSS_394	VSS_340	AM67
AA28	VSS_396	VSS_341	AM68
AA29	VSS_398	VSS_342	AM69
AA28	VSS_400	VSS_343	AM70
AA29	VSS_402	VSS_344	AM71
AA28	VSS_404	VSS_345	AM72
AA29	VSS_406	VSS_346	AM73
AA28	VSS_408	VSS_347	AM74
AA29	VSS_410	VSS_348	AM75
AA28	VSS_412	VSS_349	AM76
AA29	VSS_414	VSS_350	AM77
AA28	VSS_416	VSS_351	AM78
AA29	VSS_418	VSS_352	AM79
AA28	VSS_420	VSS_353	AM80
AA29	VSS_422	VSS_354	AM81
AA28	VSS_424	VSS_355	AM82
AA29	VSS_426	VSS_356	AM83
AA28	VSS_428	VSS_357	AM84
AA29	VSS_430	VSS_358	AM85
AA28	VSS_432	VSS_359	AM86
AA29	VSS_434	VSS_360	AM87
AA28	VSS_436	VSS_361	AM88
AA29	VSS_438	VSS_362	AM89
AA28	VSS_440	VSS_363	AM90
AA29	VSS_442	VSS_364	AM91
AA28	VSS_444	VSS_365	AM92
AA29	VSS_446	VSS_366	AM93
AA28	VSS_448	VSS_367	AM94
AA29	VSS_450	VSS_368	AM95
AA28	VSS_452	VSS_369	AM96
AA29	VSS_454	VSS_370	AM97
AA28	VSS_456	VSS_371	AM98
AA29	VSS_458	VSS_372	AM99
AA28	VSS_460	VSS_373	AM100
AA29	VSS_462	VSS_374	AM101
AA28	VSS_464	VSS_375	AM102
AA29	VSS_466	VSS_376	AM103
AA28	VSS_468	VSS_377	AM104
AA29	VSS_470	VSS_378	AM105
AA28	VSS_472	VSS_379	AM106
AA29	VSS_474	VSS_380	AM107
AA28	VSS_476	VSS_381	AM108
AA29	VSS_478	VSS_382	AM109
AA28	VSS_480	VSS_383	AM110
AA29	VSS_482	VSS_384	AM111
AA28	VSS_484	VSS_385	AM112
AA29	VSS_486	VSS_386	AM113
AA28	VSS_488	VSS_387	AM114
AA29	VSS_490	VSS_388	AM115
AA28	VSS_492	VSS_389	AM116
AA29	VSS_494	VSS_390	AM117
AA28	VSS_496	VSS_391	AM118
AA29	VSS_498	VSS_392	AM119
AA28	VSS_500	VSS_393	AM120
AA29	VSS_502	VSS_394	AM121
AA28	VSS_504	VSS_395	AM122
AA29	VSS_506	VSS_396	AM123
AA28	VSS_508	VSS_397	AM124
AA29	VSS_510	VSS_398	AM125
AA28	VSS_512	VSS_399	AM126
AA29	VSS_514	VSS_400	AM127
AA28	VSS_516	VSS_401	AM128
AA29	VSS_518	VSS_402	AM129
AA28	VSS_520	VSS_403	AM130
AA29	VSS_522	VSS_404	AM131
AA28	VSS_524	VSS_405	AM132
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AA29	VSS_530	VSS_408	AM135
AA28	VSS_532	VSS_409	AM136
AA29	VSS_534	VSS_410	AM137
AA28	VSS_536	VSS_411	AM138
AA29	VSS_538	VSS_412	AM139
AA28	VSS_540	VSS_413	AM140
AA29	VSS_542	VSS_414	AM141
AA28	VSS_544	VSS_415	AM142
AA29	VSS_546	VSS_416	AM143
AA28	VSS_548	VSS_417	AM144
AA29	VSS_550	VSS_418	AM145
AA28	VSS_552	VSS_419	AM146
AA29	VSS_554	VSS_420	AM147
AA28	VSS_556	VSS_421	AM148
AA29	VSS_558	VSS_422	AM149
AA28	VSS_560	VSS_423	AM150
AA29	VSS_562	VSS_424	AM151
AA28	VSS_564	VSS_425	AM152
AA29	VSS_566	VSS_426	AM153
AA28	VSS_568	VSS_427	AM154
AA29	VSS_570	VSS_428	AM155
AA28	VSS_572	VSS_429	AM156
AA29	VSS_574	VSS_430	AM157
AA28	VSS_576	VSS_431	AM158
AA29	VSS_578	VSS_432	AM159
AA28	VSS_580	VSS_433	AM160
AA29	VSS_582	VSS_434	AM161
AA28	VSS_584	VSS_435	AM162
AA29	VSS_586	VSS_436	AM163
AA28	VSS_588	VSS_437	AM164
AA29	VSS_590	VSS_438	AM165
AA28	VSS_592	VSS_439	AM166
AA29	VSS_594	VSS_440	AM167
AA28	VSS_596	VSS_441	AM168
AA29	VSS_598	VSS_442	AM169
AA28	VSS_600	VSS_443	AM170
AA29	VSS_602	VSS_444	AM171
AA28	VSS_604	VSS_445	AM172
AA29	VSS_606	VSS_446	AM173
AA28	VSS_608	VSS_447	AM174
AA29	VSS_610	VSS_448	AM175
AA28	VSS_612	VSS_449	AM176
AA29	VSS_614	VSS_450	AM177
AA28	VSS_616	VSS_451	AM178
AA29	VSS_618	VSS_452	AM179
AA28	VSS_620	VSS_453	AM180
AA29	VSS_622	VSS_454	AM181
AA28	VSS_624	VSS_455	AM182
AA29	VSS_626	VSS_456	AM183
AA28	VSS_628	VSS_457	AM184
AA29	VSS_630	VSS_458	AM185
AA28	VSS_632	VSS_459	AM186
AA29	VSS_634	VSS_460	AM187
AA28			

BATTERY CIRCUIT

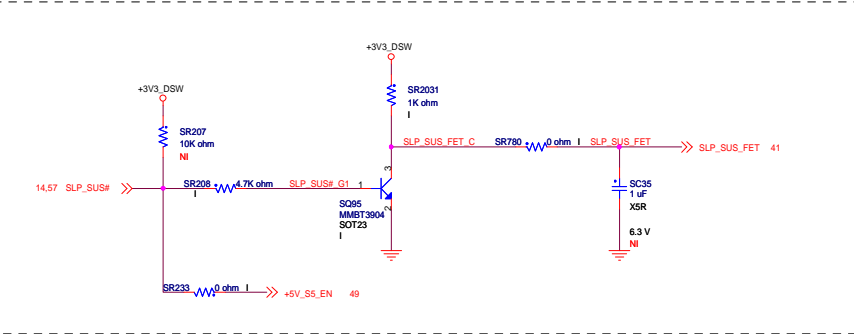


PCH DPWROK

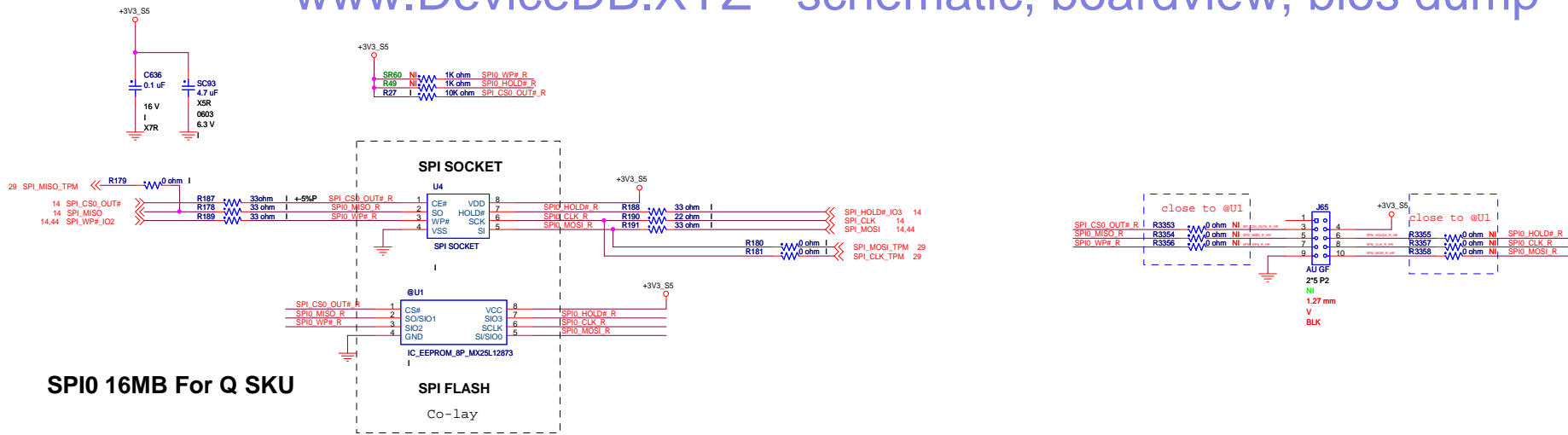
Operation voltage: 1.6-5.5V



DSW CONTROL SIGNAL

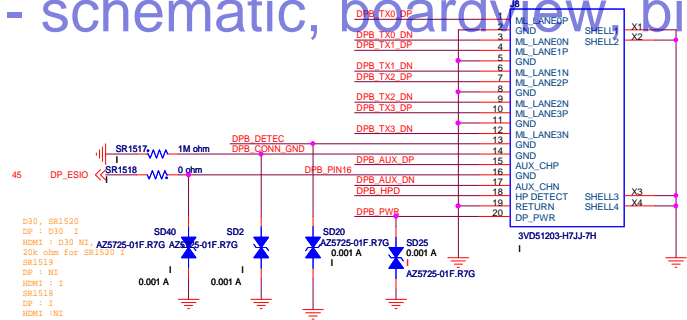
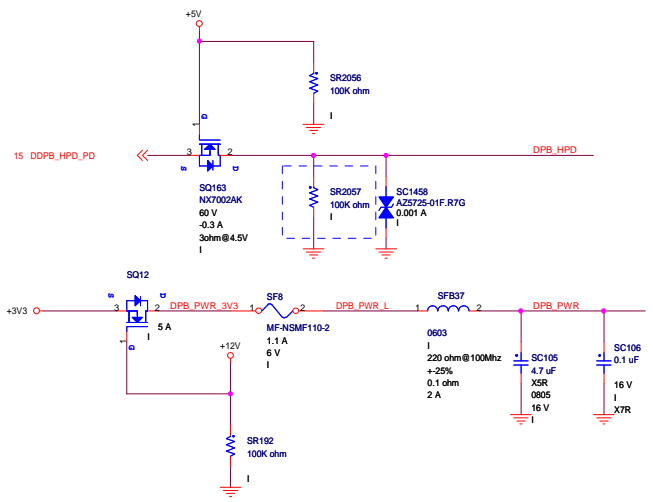


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Title: 20. DSW	
Size C	Document Number JC113
Date: Friday, August 26, 2016	Sheet 20 of 67
Rev X03	



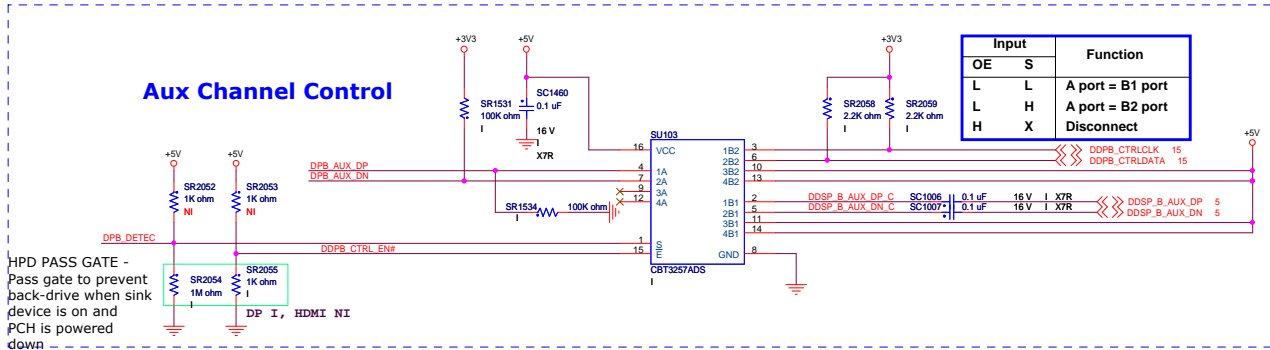
SPI0 16MB For Q SKU

- 5 DDSP_B_DP_0_DP >>> SC1445 0.1 uF 16 V X7R DPB_TX0_DP
- 5 DDSP_B_DP_0_DN >>> SC1446 0.1 uF 16 V X7R DPB_TX0_DN
- 5 DDSP_B_DP_1_DP >>> SC1447 0.1 uF 16 V X7R DPB_TX1_DP
- 5 DDSP_B_DP_1_DN >>> SC1448 0.1 uF 16 V X7R DPB_TX1_DN
- 5 DDSP_B_DP_2_DP >>> SC1449 0.1 uF 16 V X7R DPB_TX2_DP
- 5 DDSP_B_DP_2_DN >>> SC1450 0.1 uF 16 V X7R DPB_TX2_DN
- 5 DDSP_B_DP_3_DP >>> SC1451 0.1 uF 16 V X7R DPB_TX3_DP
- 5 DDSP_B_DP_3_DN >>> SC1452 0.1 uF 16 V X7R DPB_TX3_DN

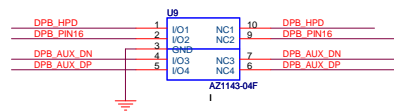
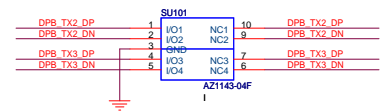
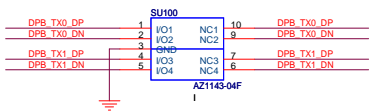


Aux Channel Control

Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

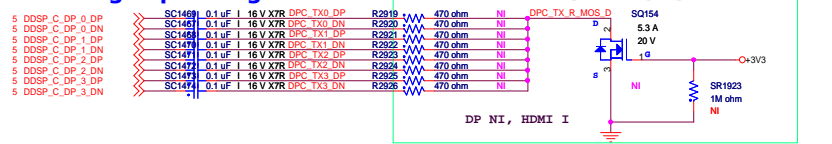


HPD PASS GATE - Pass gate to prevent back-drive when sink device is on and PCH is powered down

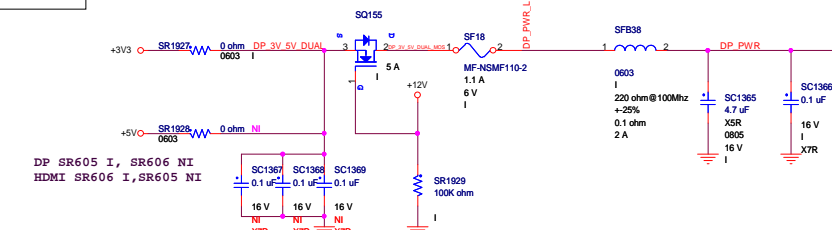
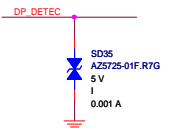
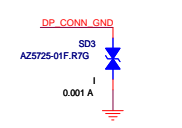
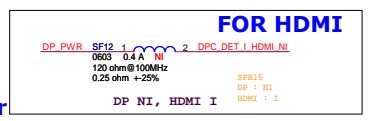
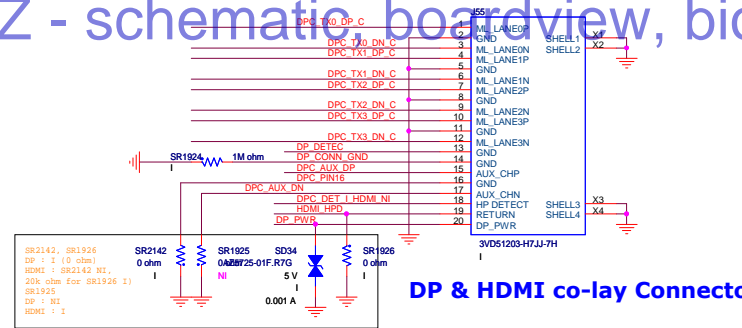


CAD Note : Please place ESD component close to DP connector

HDMI high speed signal level shift



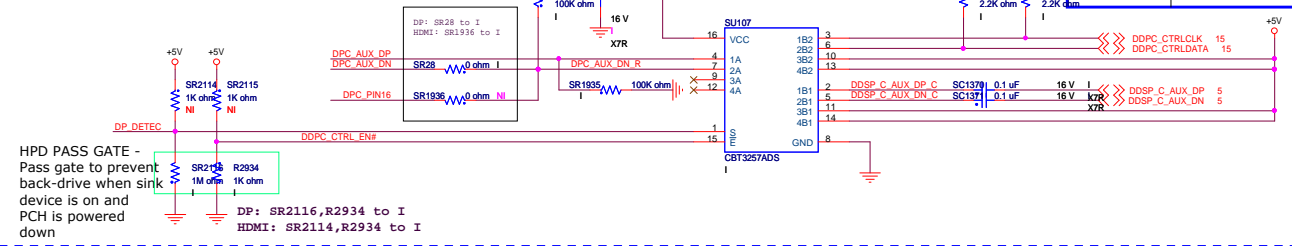
CAD Note : Please place 470 ohm component as short as passable (to bridge the antenna effect)



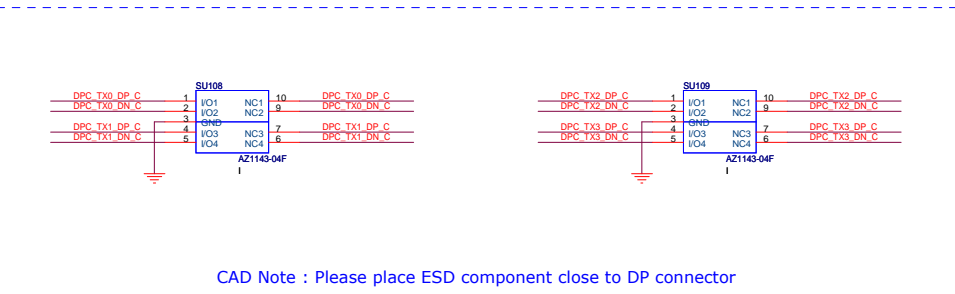
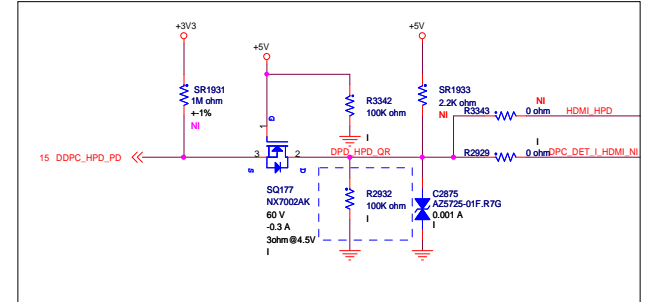
DisplayPort Interoperability

Input	S	Function
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

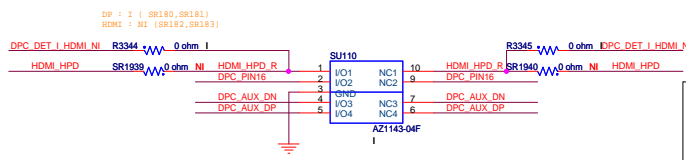
Aux Channel Control



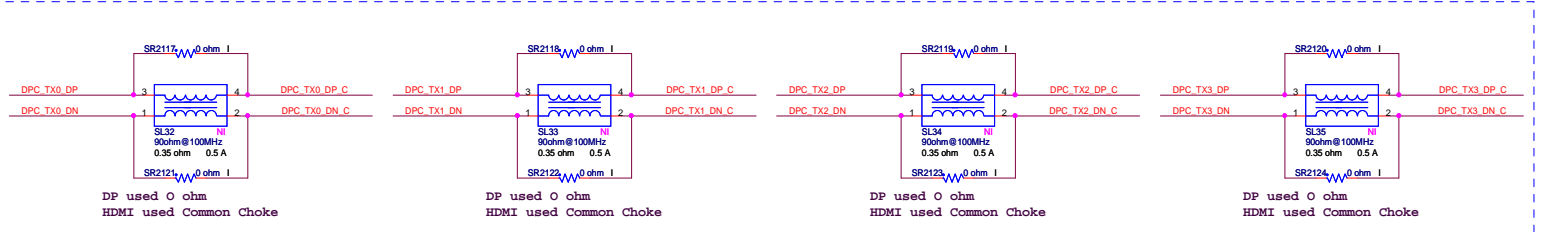
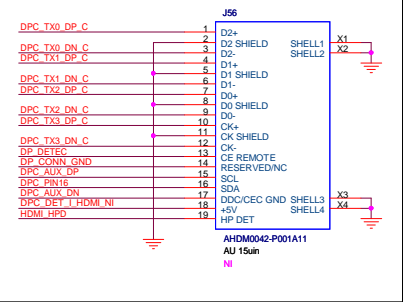
HPD PASS GATE - Pass gate to prevent back-drive when sink device is on and PCH is powered down



CAD Note : Please place ESD component close to DP connector

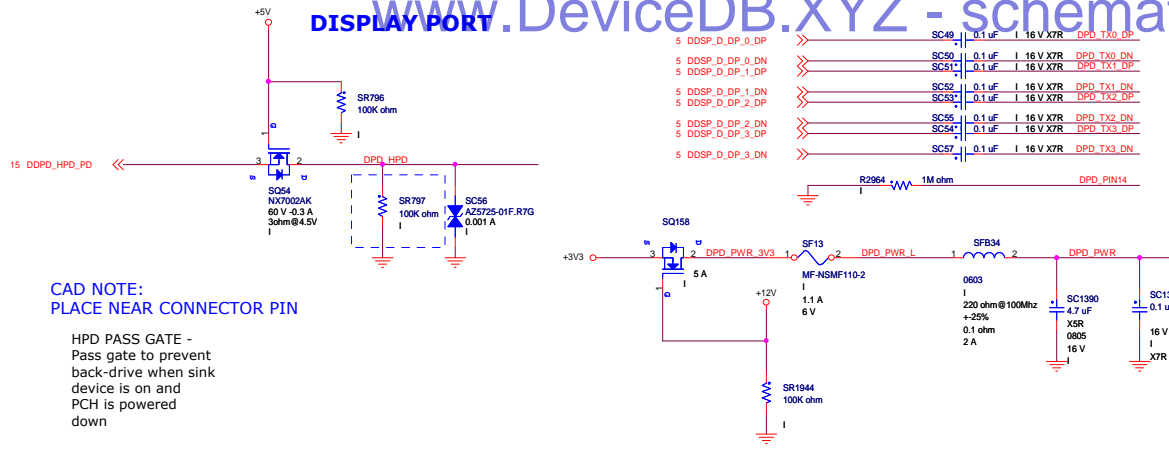


Option for HDMI



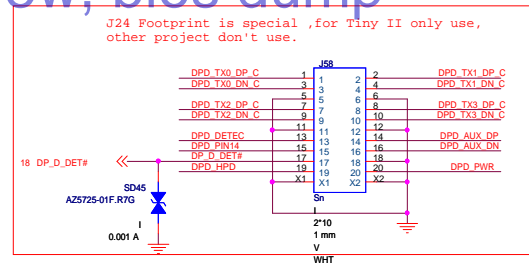
DP used 0 ohm
HDMI used Common Choke

DISPLAY PORT



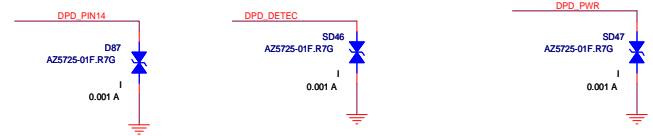
CAD NOTE:
PLACE NEAR CONNECTOR PIN

HPD PASS GATE -
Pass gate to prevent
back-drive when sink
device is on and
PCH is powered
down

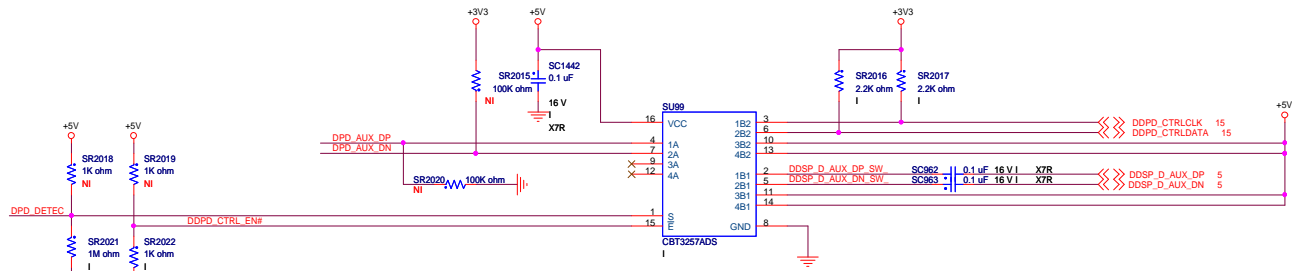


J24 Footprint is special, for Tiny II only use,
other project don't use.

On Cable side Pin17 & Pin 18 need short
DPC_DETEC
L : Connect to Display Port or No Connection
H : Connect to Doungle

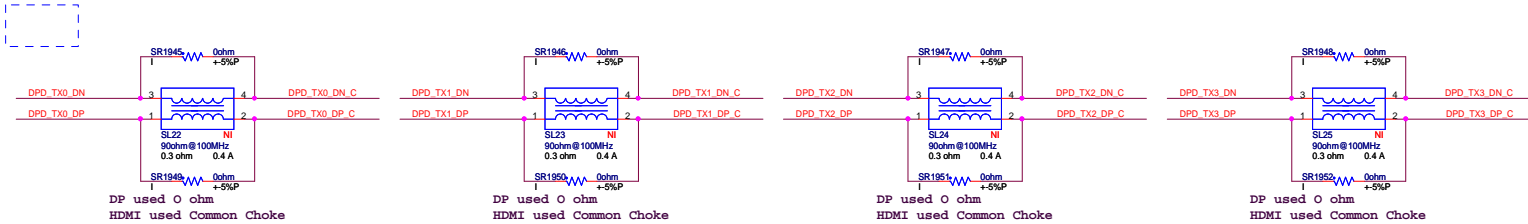
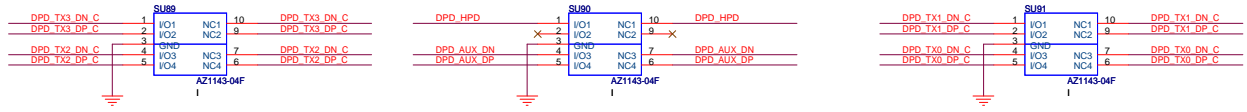


DisplayPort Interoperability



Input		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

CAD Note : Please place ESD component close to DP connector



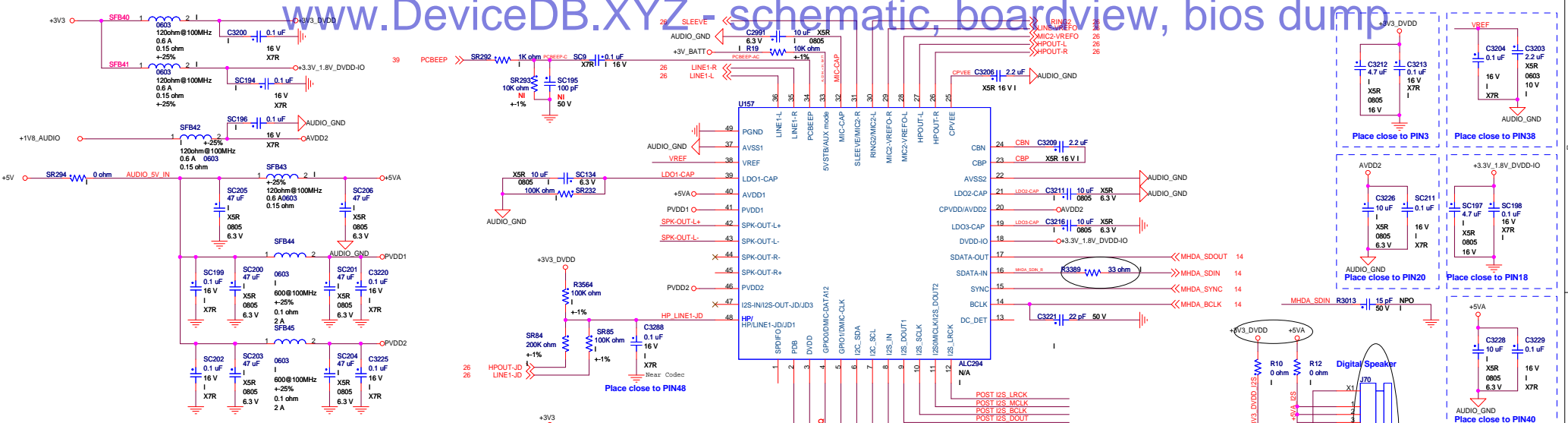
CAD Note : Please place Common Choke component close to J9 pinheader

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Title: **24. Display Port D**

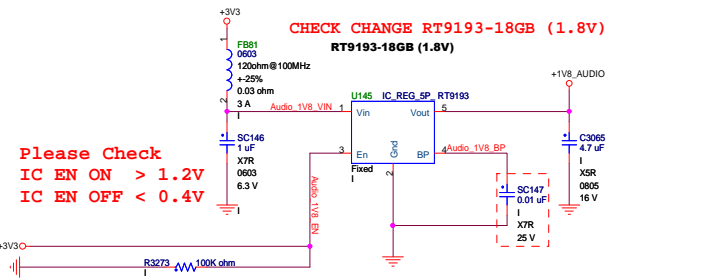
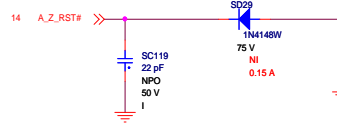
Size C Document Number: **JC113** Rev X03

Date: Friday, August 26, 2016 Sheet 24 of 67

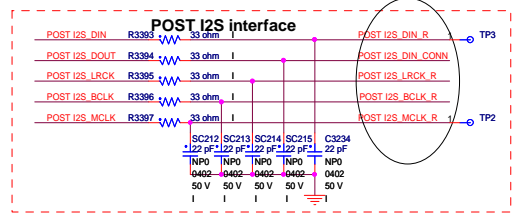
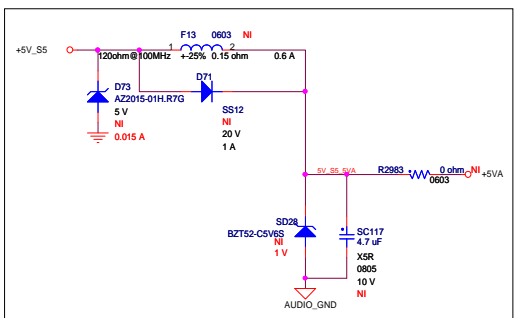


Audio_+1V8

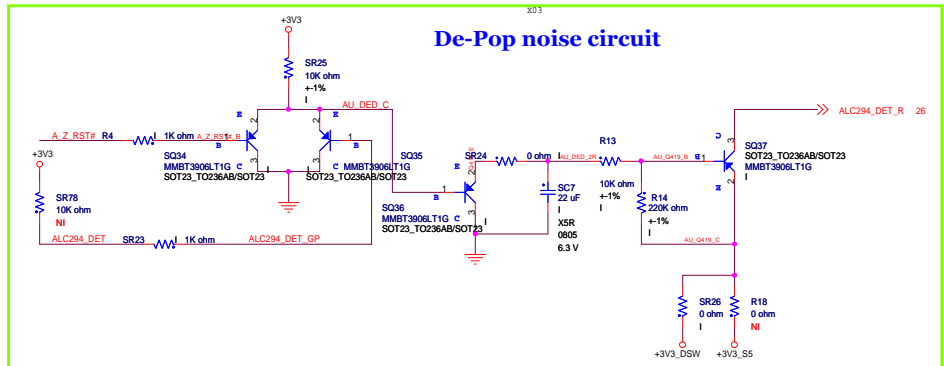
Vin:+3V3_S5
 Vout:+1V8_AUDIO (+1.8V)
 Imax:0.09A
 IC EN ON > 1.5V
 IC EN OFF < 0.4V
 IC current limit:750mA

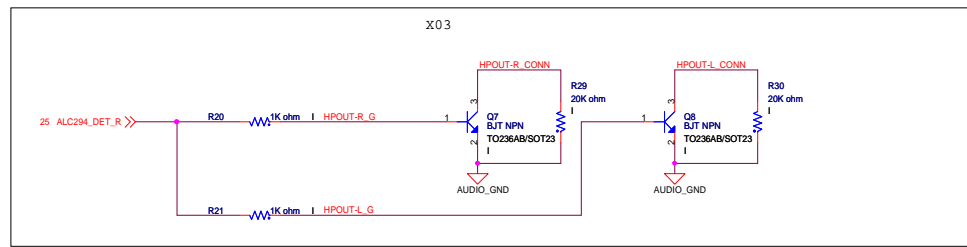
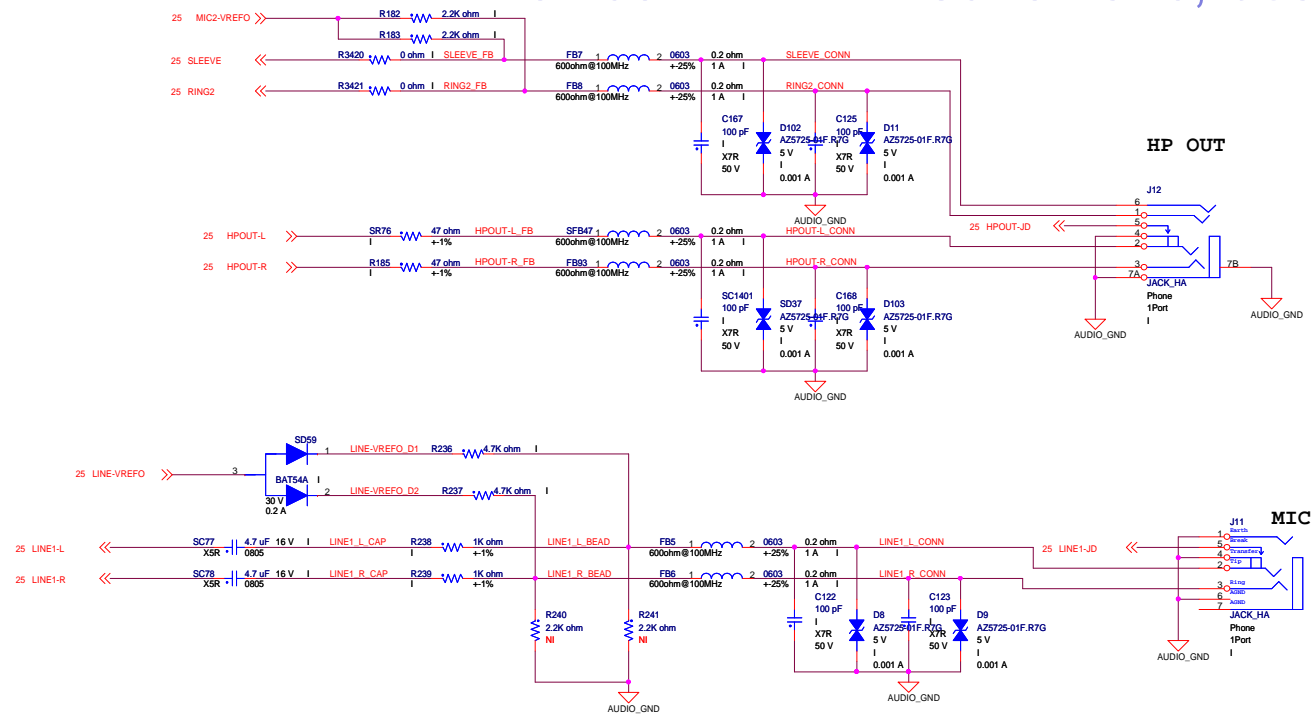


Please Check
 IC EN ON > 1.2V
 IC EN OFF < 0.4V

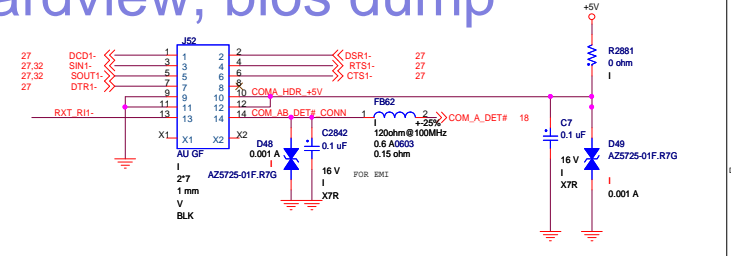
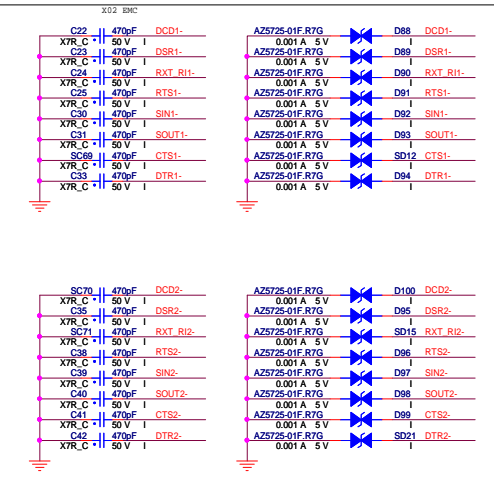
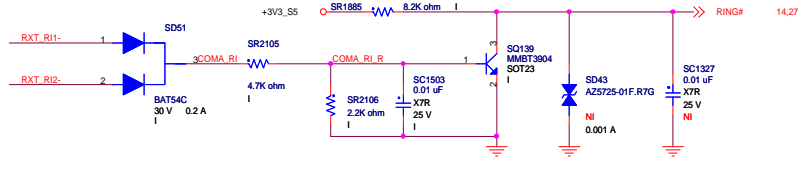


- LAYOUT NOTE: LOCATE NEAR AUDIO CHIP, U157
- LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J12
- LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J11
- LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J10
- TOP SIDE
- LAYOUT NOTE: LOCATE NEAR AUDIO JACK, J10



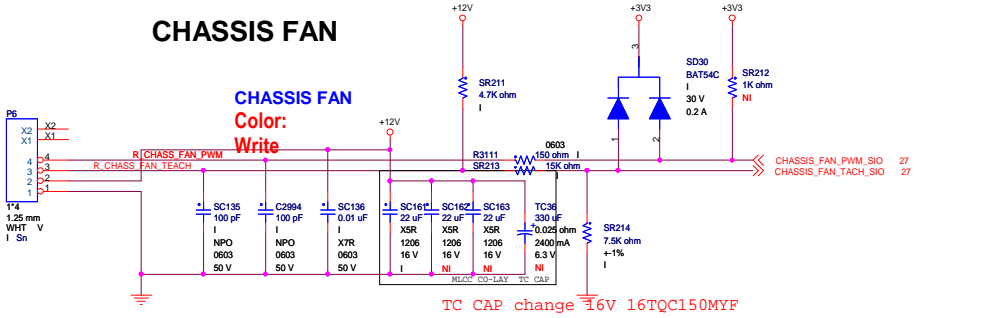


COM PORT HDR x2



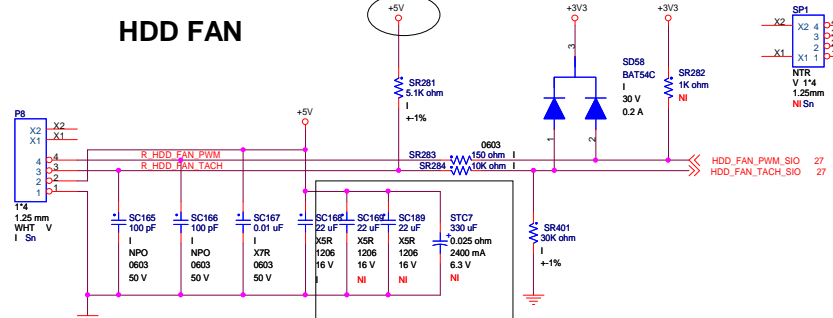
CHASSIS FAN

CHASSIS FAN Color: Write

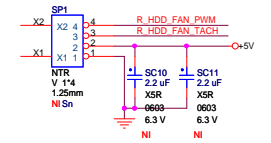


TC CAP change 16V 16TQC150MYF

HDD FAN

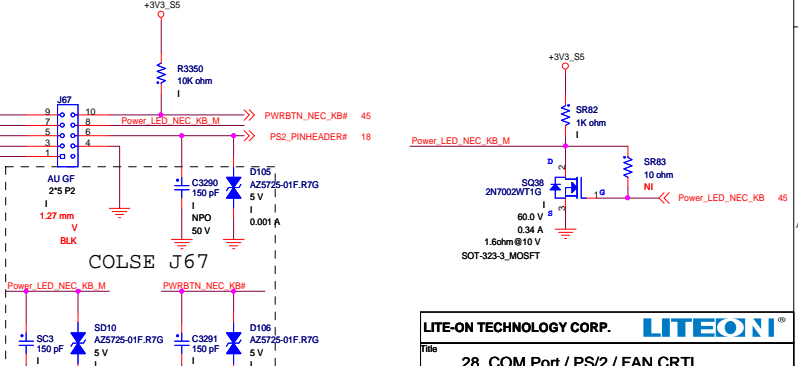
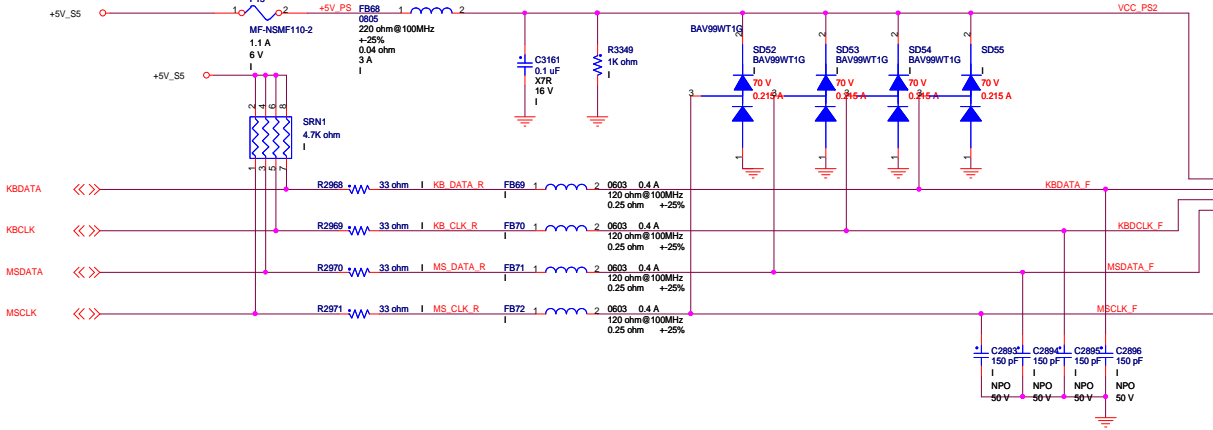


M.2 FAN



PS/2 HDR for NEC SKU

Function	Mouse	NEC Keyboard
PIN	2, 4, 7, 8, 10	1, 2, 3, 4, 6, 7,



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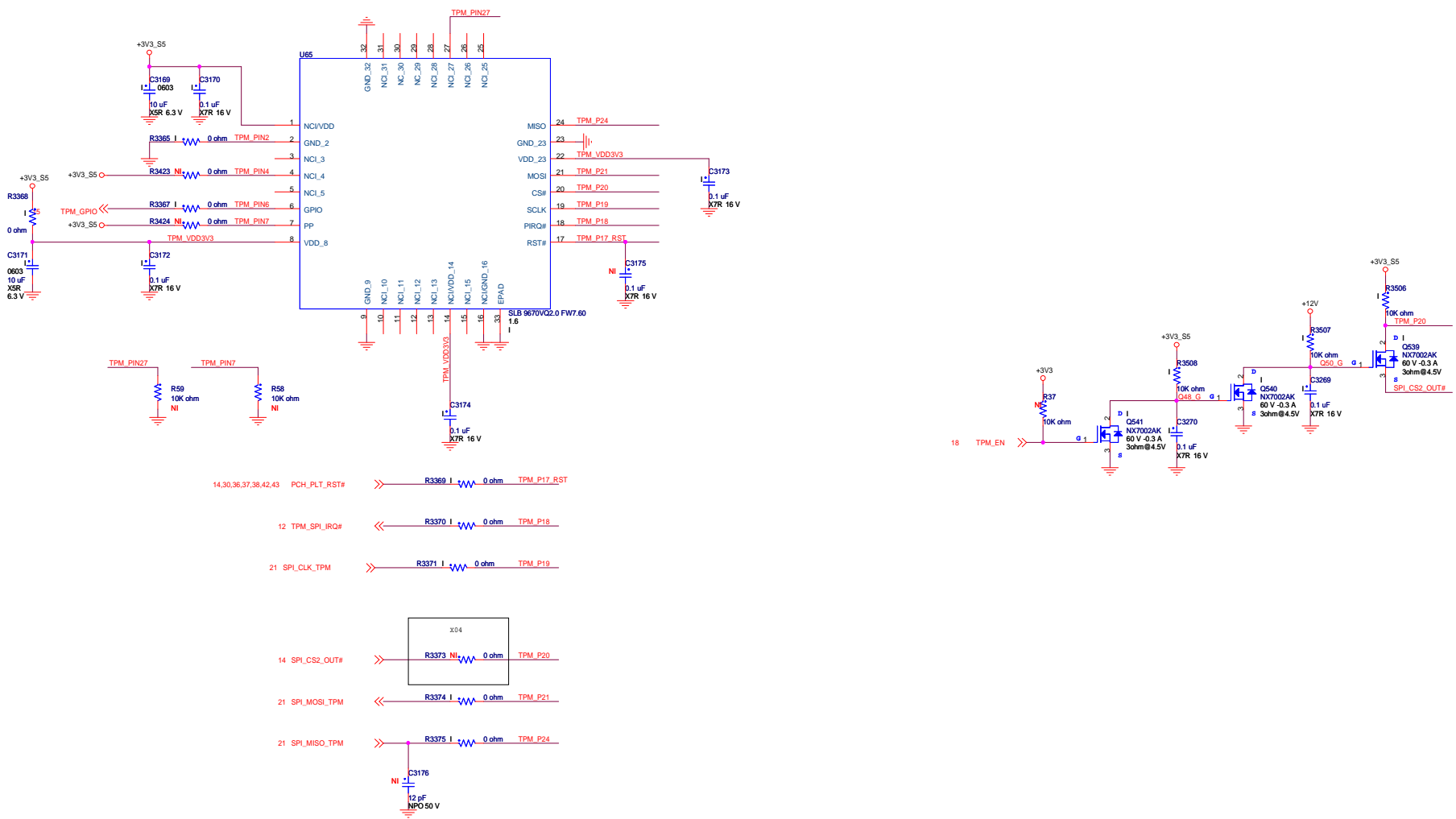
28. COM Port / PS/2 / FAN CTRL

Document Number JC113

Rev X03

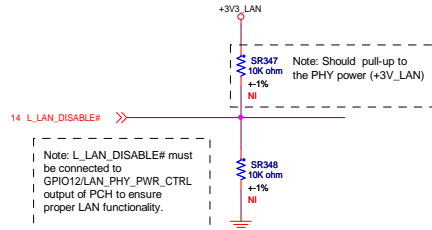
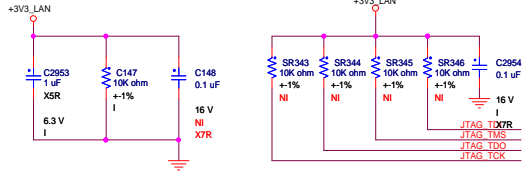
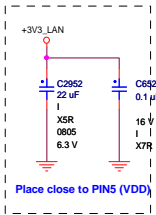
Date: Friday, August 26, 2016 11:58:28 AM

Page 28 of 67



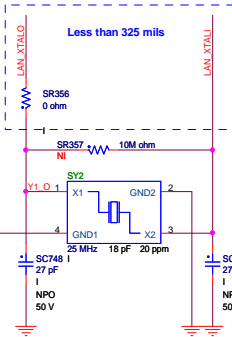
- 14,30,36,37,38,42,43 PCH_PLT_RST# >> R3369 0 ohm TPM_P17_RST
- 12 TPM_SPI_IRQ# << R3370 0 ohm TPM_P18
- 21 SPI_CLK_TPM >> R3371 0 ohm TPM_P19
- 14 SPI_CS2_OUT# >> R3373 0 ohm TPM_P20
- 21 SPI_MOSI_TPM << R3374 0 ohm TPM_P21
- 21 SPI_MISO_TPM >> R3375 0 ohm TPM_P24

BOM	PIN	NCT650LBAYX (SPI)	BT00012901IR-R SLB9670 (SPI)	ST33HTPH2E32AAE8 (SPI)
GND	2		R3365	R3365
GPIO	6	R3367	R3367	
CLKRUN	13			
AD3	15			
IRQ#(R1164)/AD2(R628)	18	R3370	R3370	R3370
CLK	19	R3371	R3371	R3371
CS#(R616)/LPC Frame#(R625)	20	R3373	R3373	R3373
MOSI(R617)/AD1(R626)	21	R3374	R3374	R3374
MISO(R615)/AD0(R624)	24	R3375	R3375	R3375

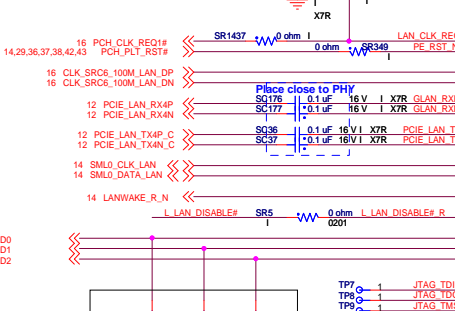


Typical LED configuration

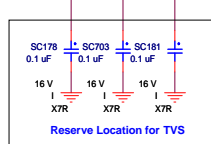
	WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off	Off
On	10Mb Inactive	On	Off	Off	Off
On	10Mb Active	Blinking	Off	Off	Off
On	100Mb Inactive	On	On	Off	Off
On	100Mb Active	Blinking	On	Off	Off
On	1Gb Inactive	On	Off	On	Off
On	1Gb Active	Blinking	Off	On	On



Place close to PHY



31 LED0
31 LED1
31 LED2



Reserve Location for TVS



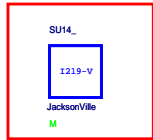
JTAG TDI
JTAG TDO
JTAG TMS
JTAG TCK



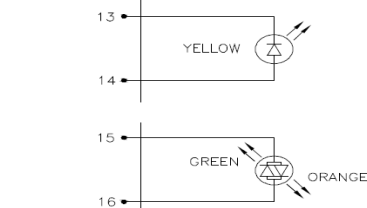
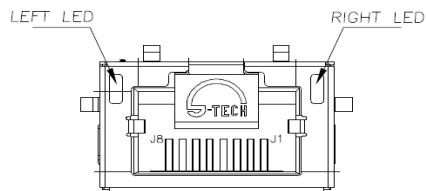
LAN TESTEN



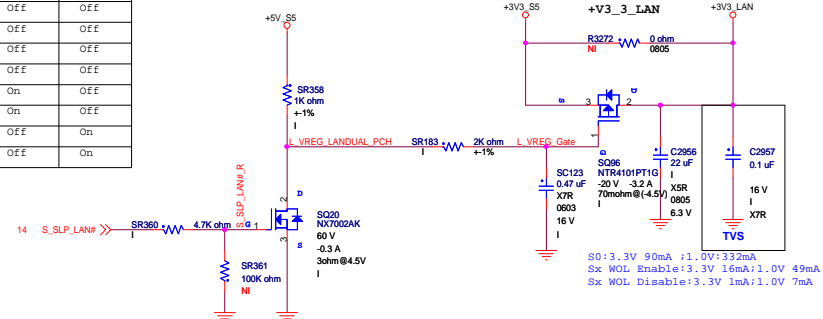
LAN RBIAS

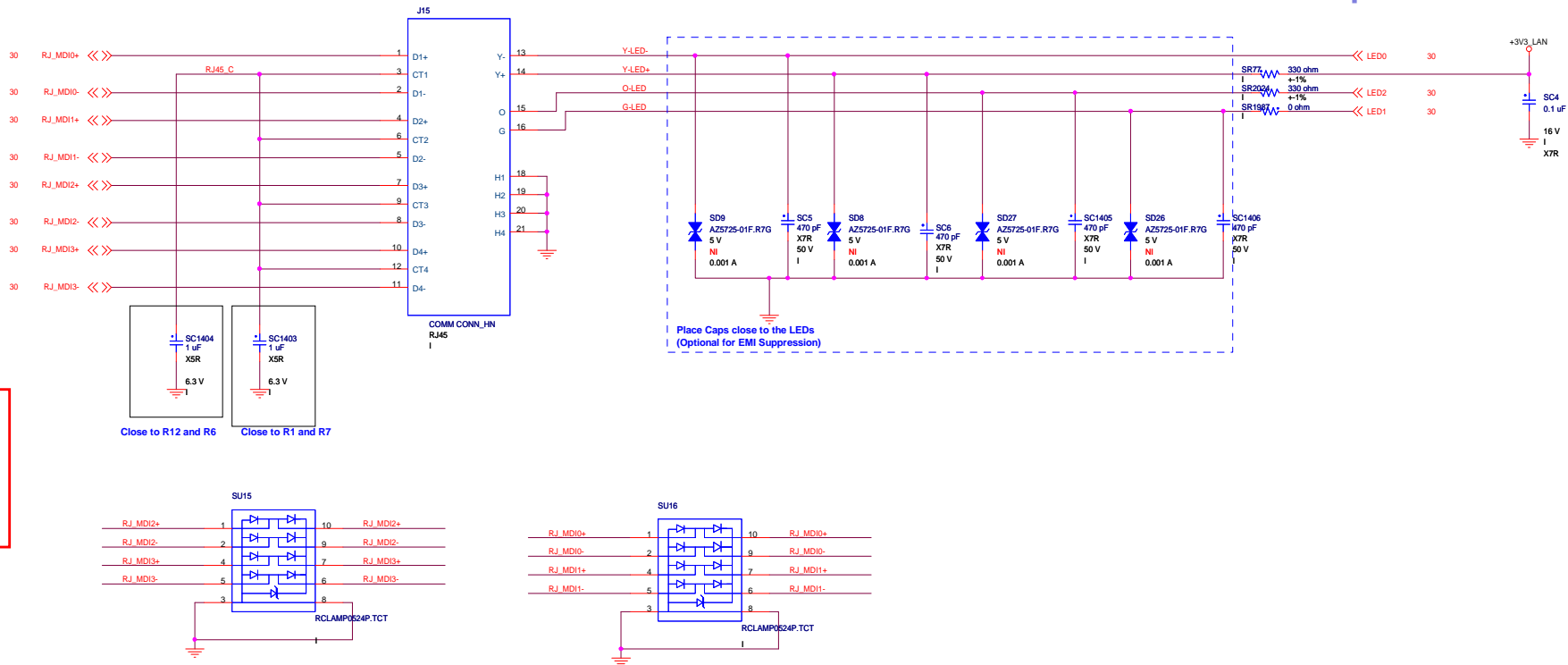


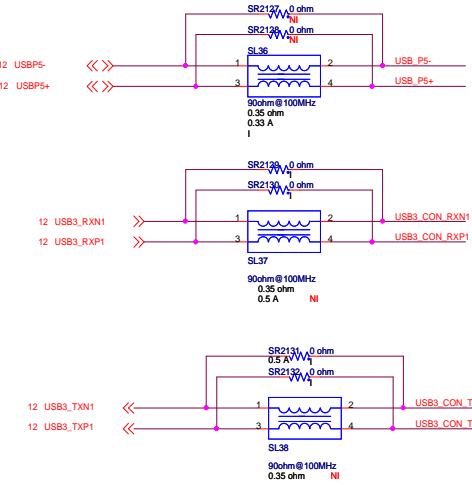
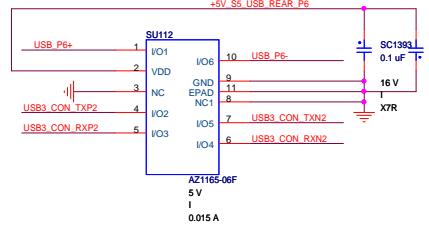
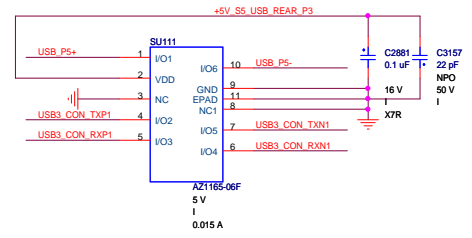
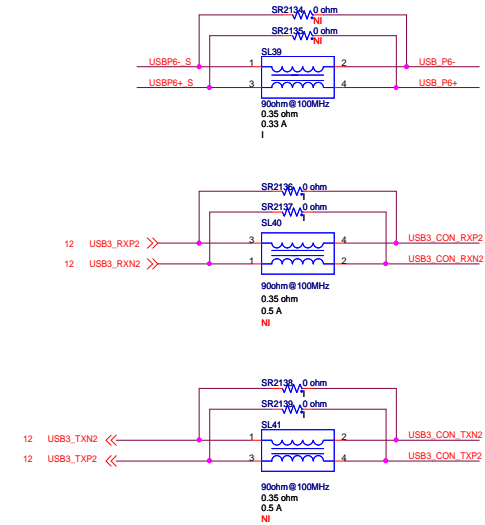
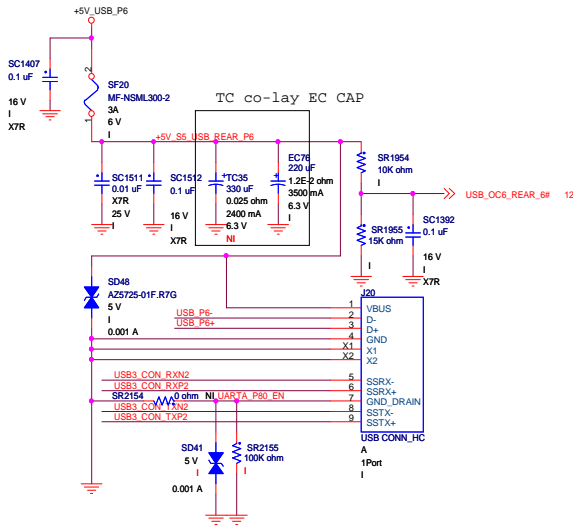
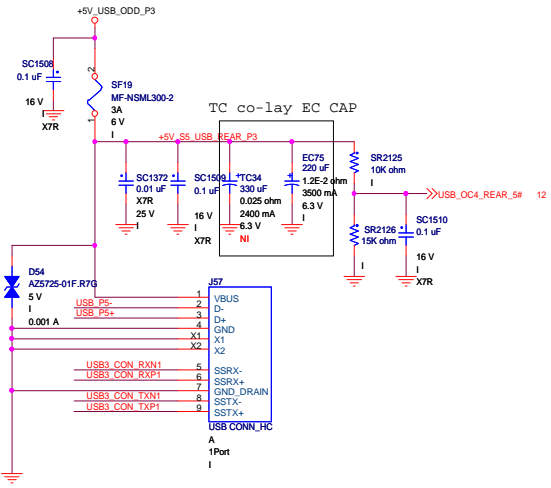
Option For B SKU LAN



	WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off	Off
Off	S3/S4/S5	Off	Off	Off	Off
On	10Mb Inactive	On	Off	Off	Off
On	10Mb Active	Blinking	Off	Off	Off
On	100Mb Inactive	On	On	Off	Off
On	100Mb Active	Blinking	On	Off	Off
On	1Gb Inactive	On	Off	On	Off
On	1Gb Active	Blinking	Off	On	On







For USB Debug Function

14 USBDEBUG >> SR2156 0 ohm I USB_UART_SEL

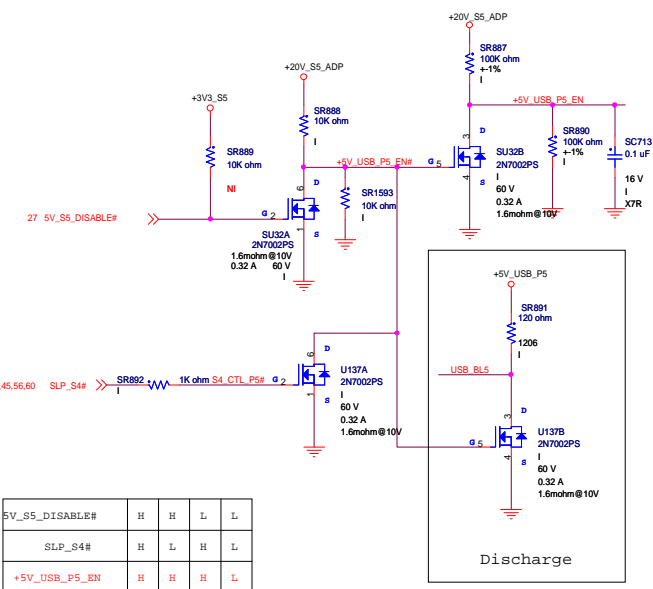
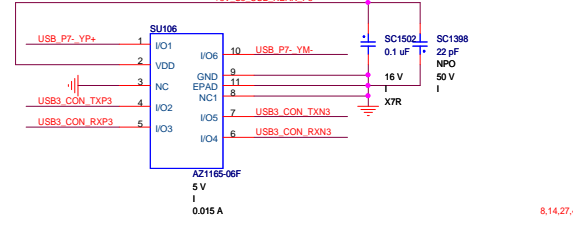
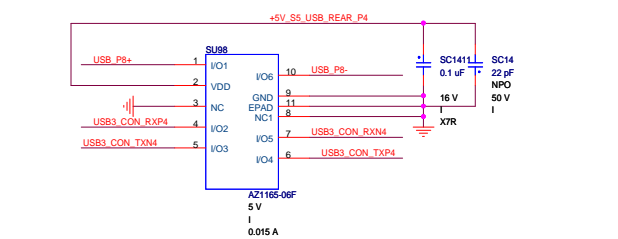
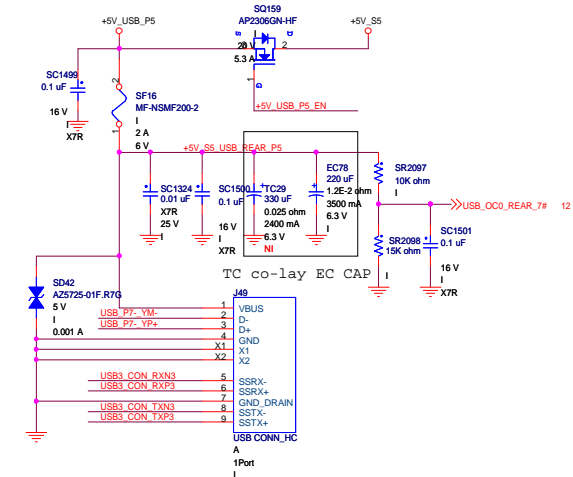
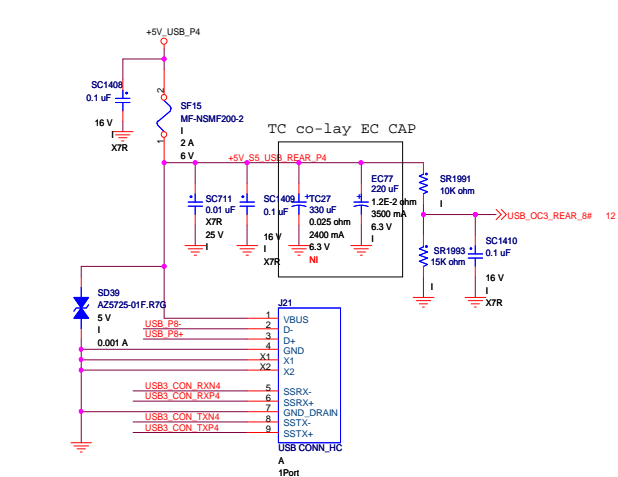
Schematic for USB Debug Function. It shows the SU113 chip (TSUUSB21DRCR IC/SWITCHING) connected to USB P6+, VDD, GND, EPAD, VIO2, VIO3, VIO4, VIO5, VIO6, and USB_UART_SEL. It also shows connections for SOUT1-, SOUT1+, SIN1-, SIN1+, SOUTA_C, SINA_C, and UARTA_P80_EN. The chip is an AZ1165-06F, 5V, 0.015 A.

USBDEBUG	Kernel debug
Set input	DISABLE
Set output Low	ENABLE

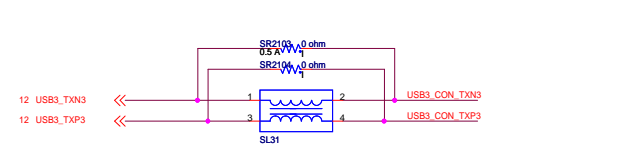
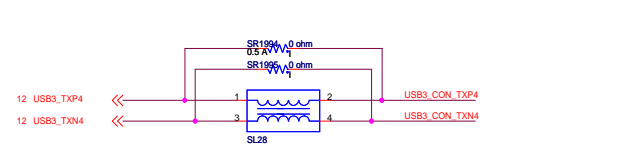
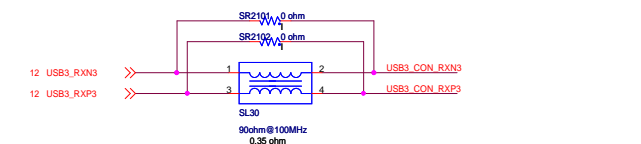
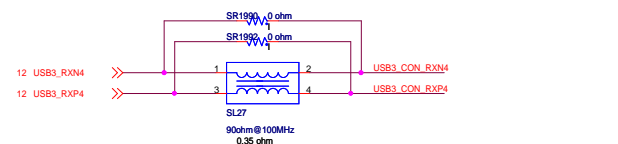
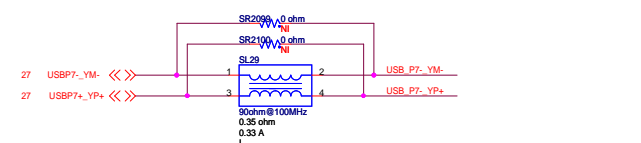
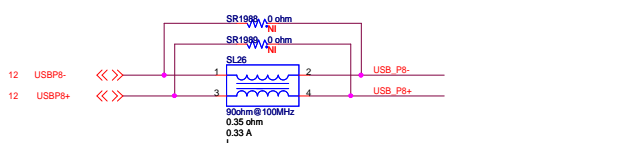
OE#	S	Function
H	X	Disable
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

UARTA_P80_EN	POST 80
L	DISABLE
H	ENABLE

USB P6- SR2160 0 ohm 0201 USB P6- R SR2161 0 ohm 0201 USB P6- S
 USB P6+ SR2162 0 ohm 0201 USB P6+ R SR2163 0 ohm 0201 USB P6+ S



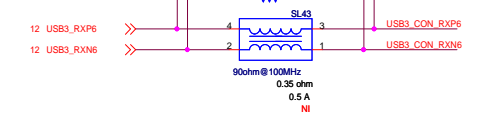
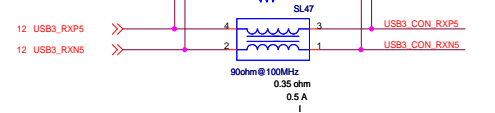
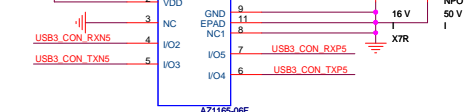
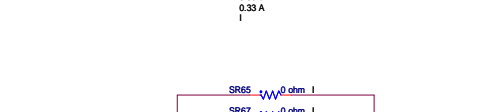
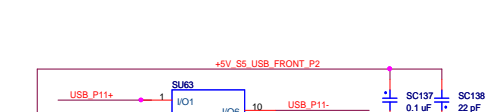
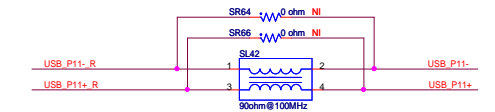
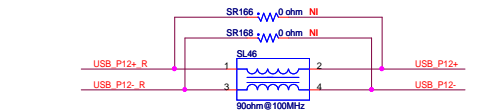
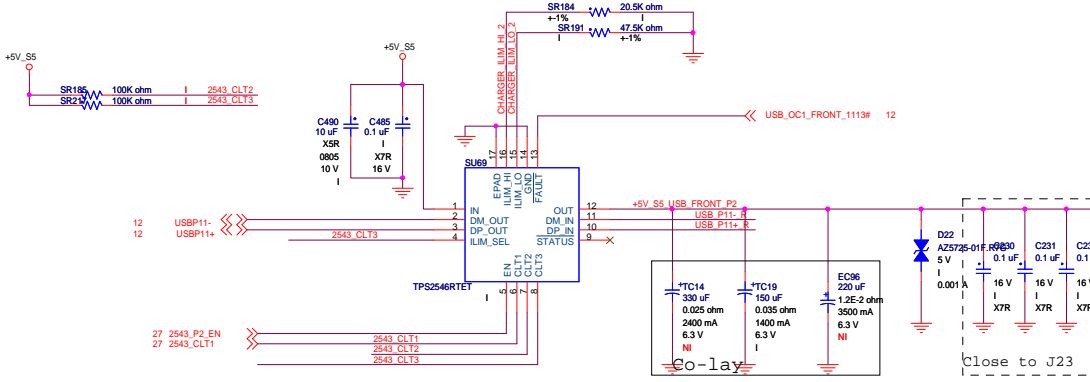
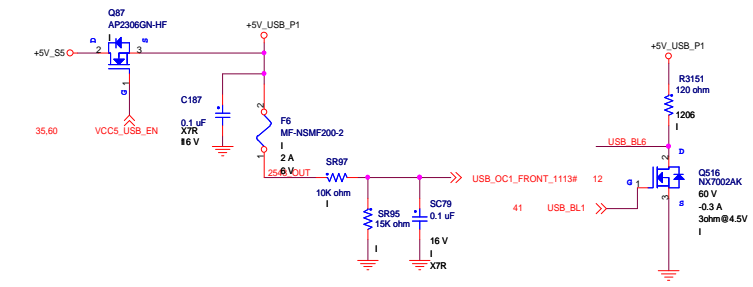
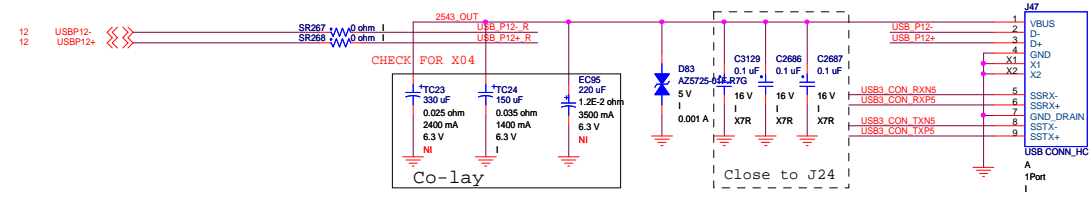
5V_S5_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P5_EN	H	H	H	L

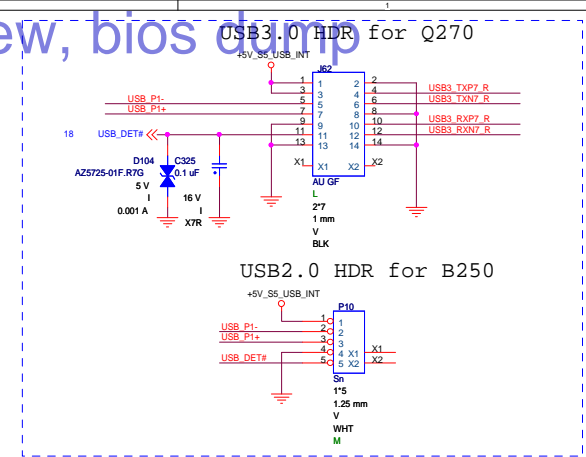


FRONT USB3.0 Charger x 2

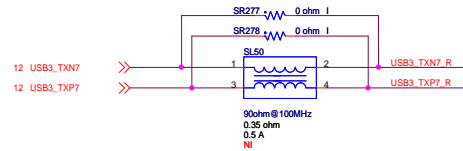
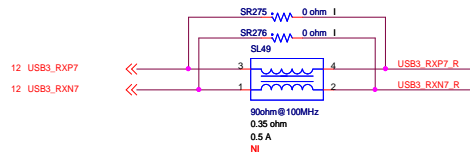
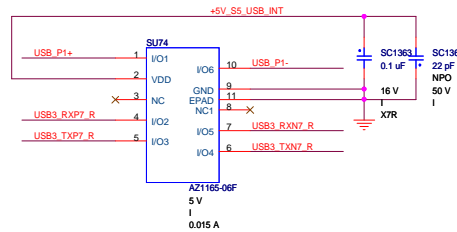
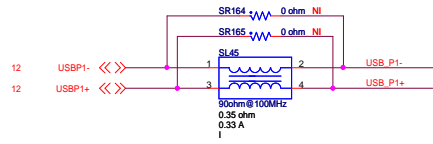
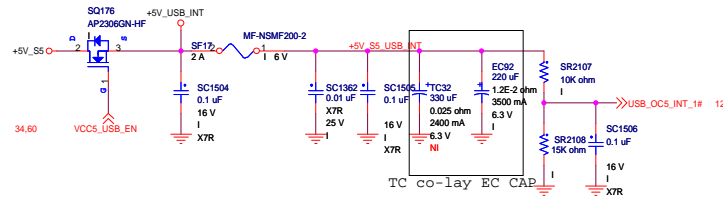
ILIM_HI	20.5K	2.5A	DCP	Tiny S3/S4/S5
			CDP	Tiny S0
ILIM_LO	47.5K	1.1A	SDP	Tiny not support

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	los_pw & ILIM_HI ⁽¹⁾	DCP load present ⁽¹⁾
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present ⁽¹⁾
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP ⁽⁶⁾	ILIM_LO	off
1	1	1	1	CDP ⁽⁶⁾	ILIM_HI	CDP load present ⁽⁶⁾



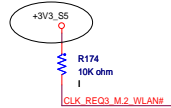
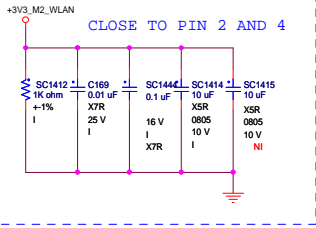


CO-LAY USB3.0&USB2.0 HDR

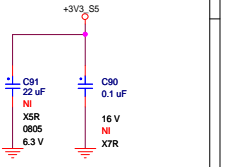
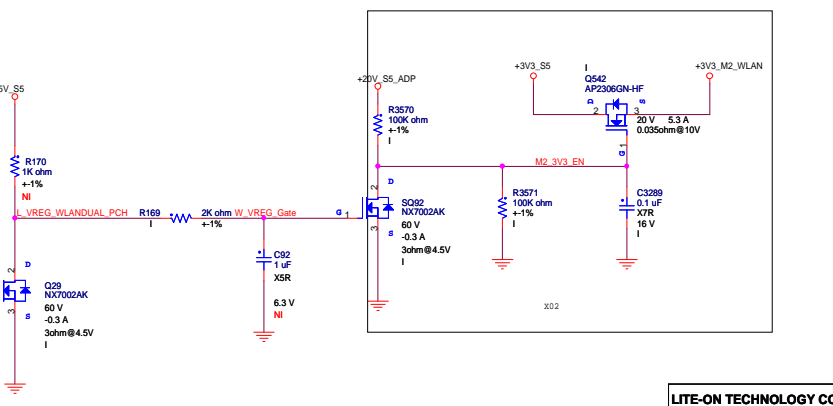
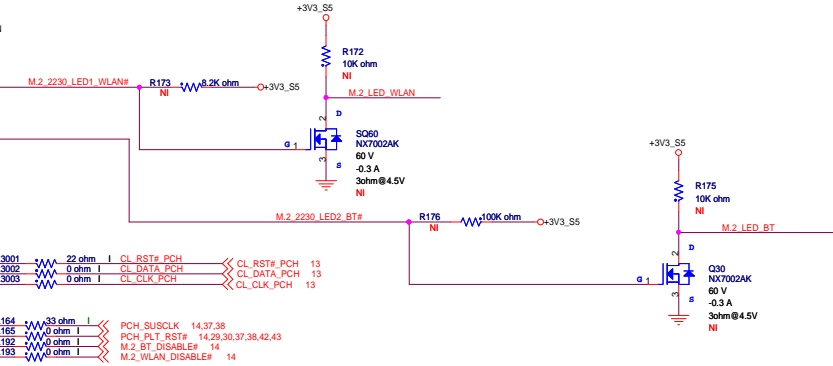
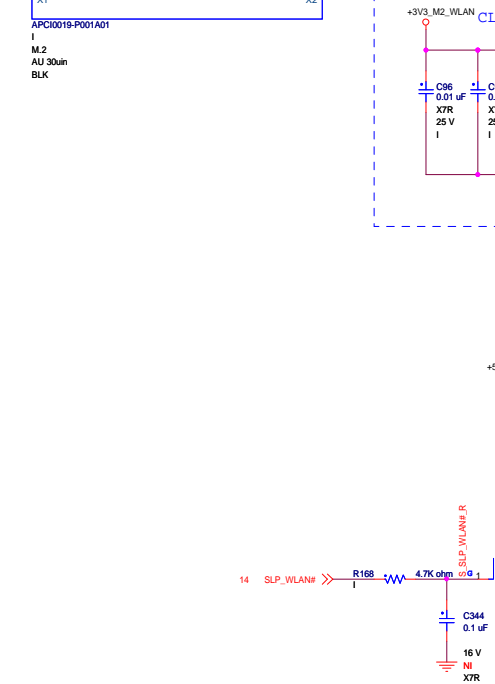
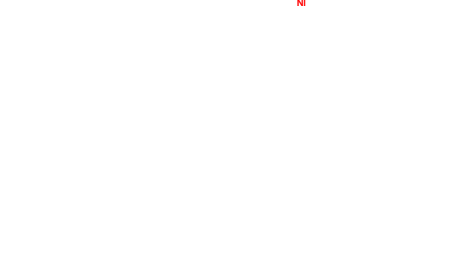
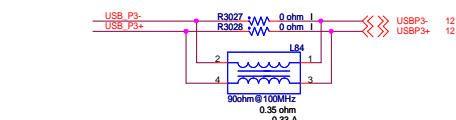
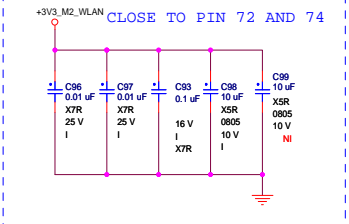
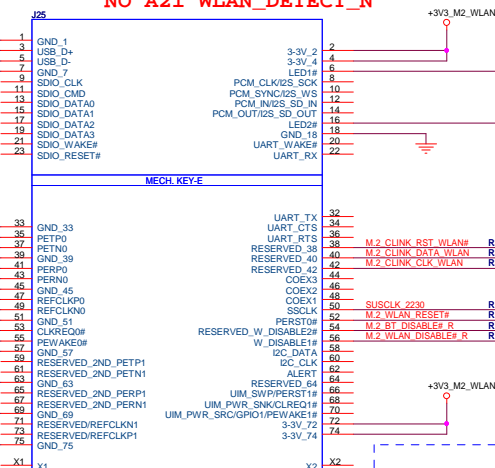
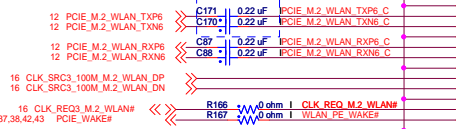


WLAN
M.2 2230 Key-E

NO A21 WLAN_DETECT_N

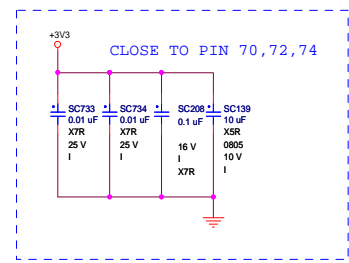
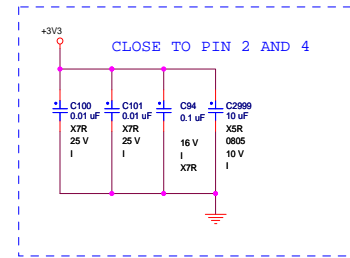
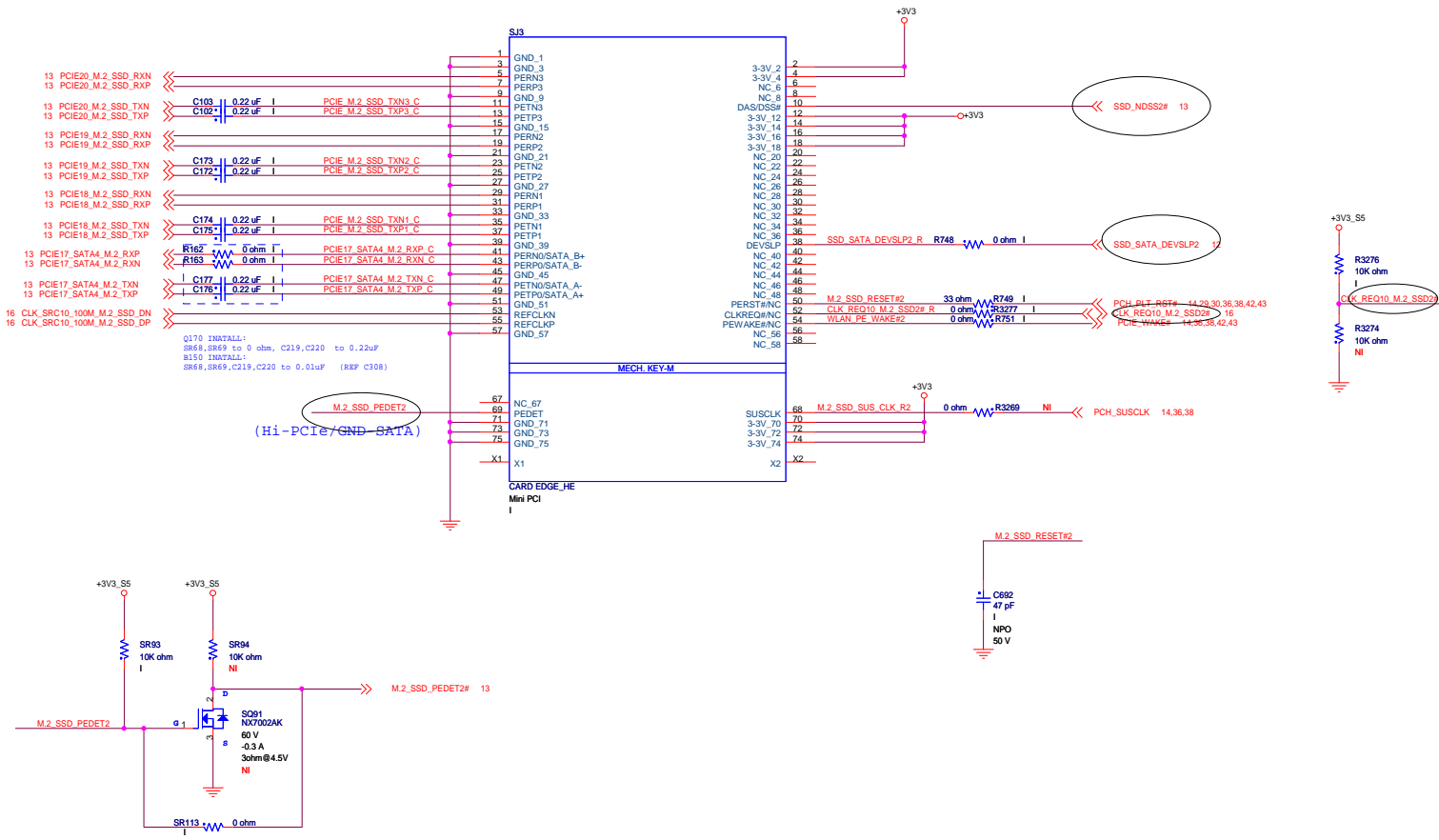


CAD NOTE : PLACE CAPS NEAR PCIE SLOT

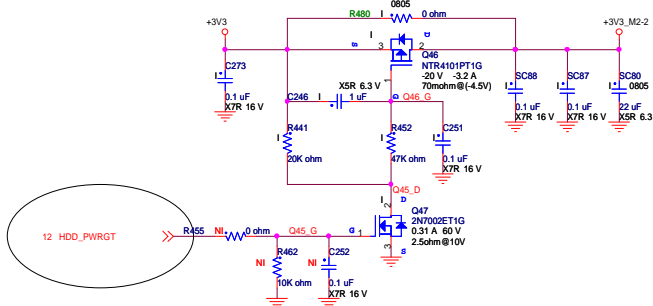
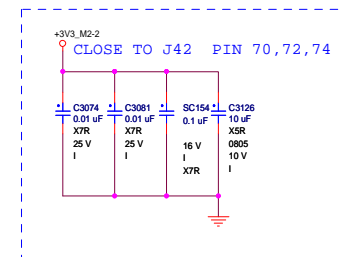
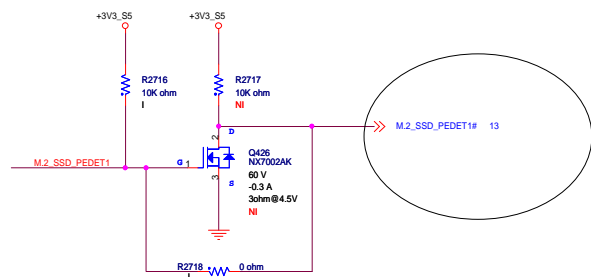
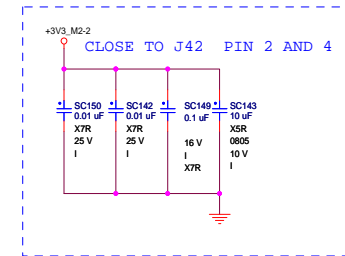
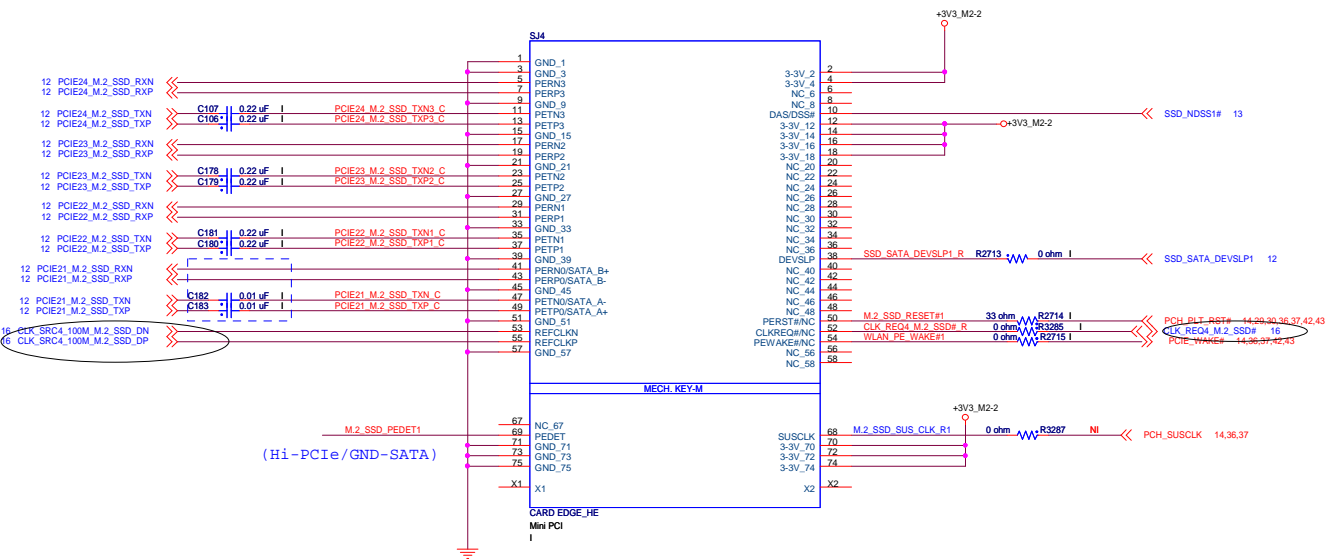


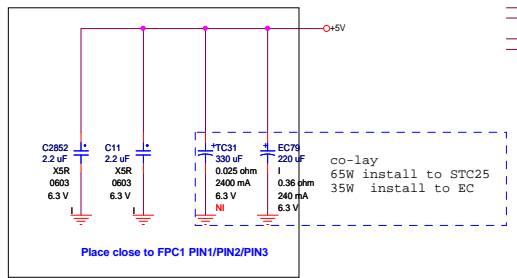
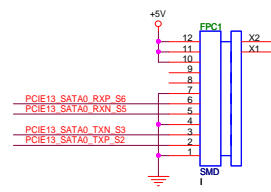
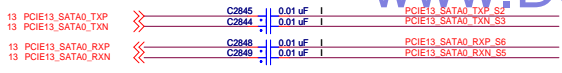
LITE-ON TECHNOLOGY CORP. LITEON	
Title: 36. M.2 2230-E / COM PORT HDR	
Size C	Document Number JC113
Date: Friday, August 26, 2016	Sheet 36 of 67

SSD Card
M.2 2280 Key-M

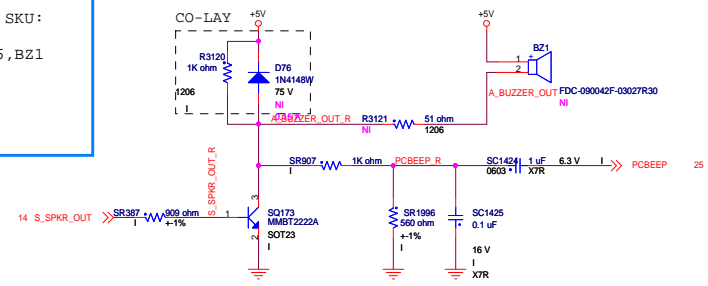


SSD Card
M.2 2280 Key-M



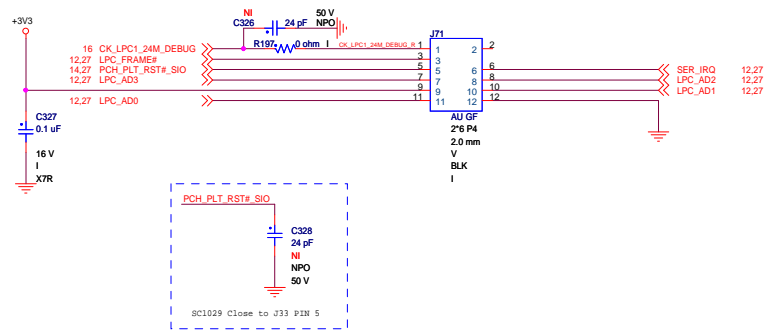


For Google SKU:
 Install
 SD14 ,SR906,BZ1
 Remove
 SR905

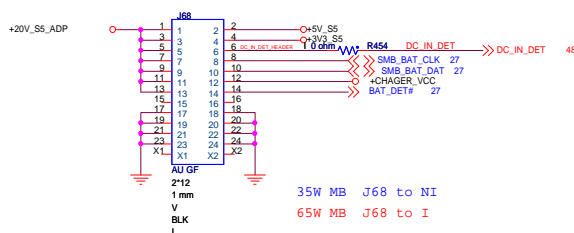


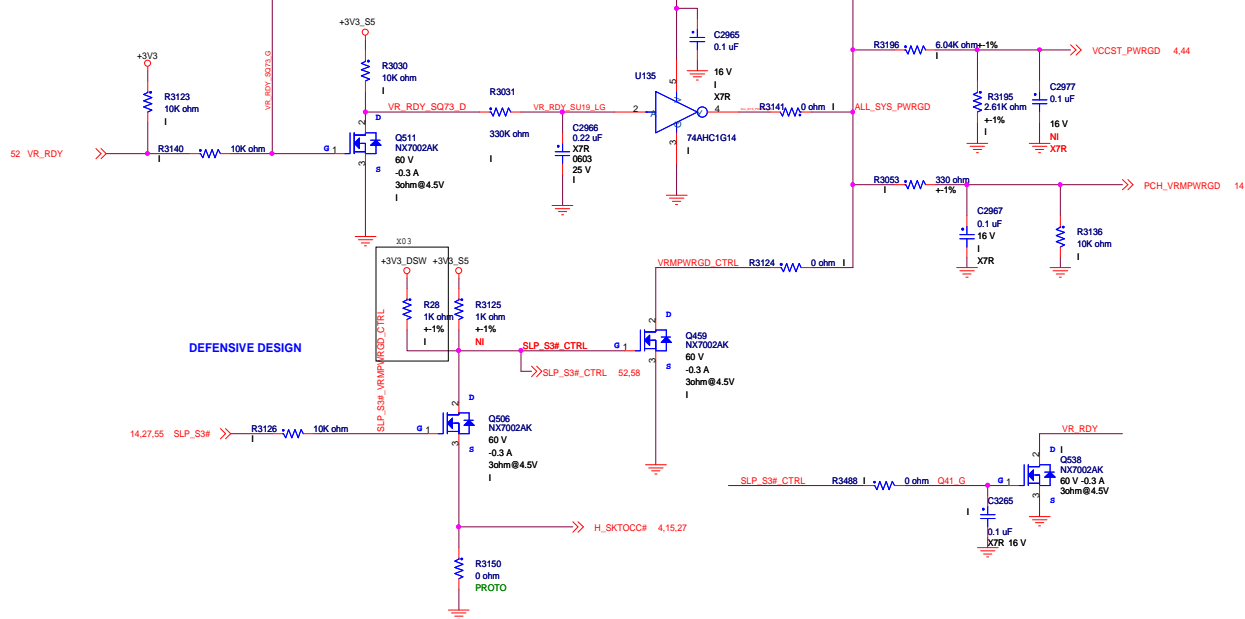
CAD NOTE : PLACE ALL CAPS WITHIN 0.5 INCH OF CONNECTOR

Debug port

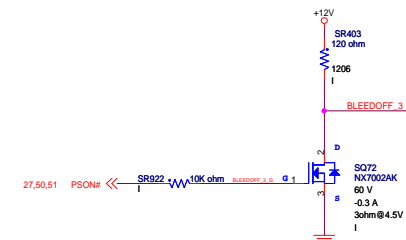


BATTERY/INT PSU Header

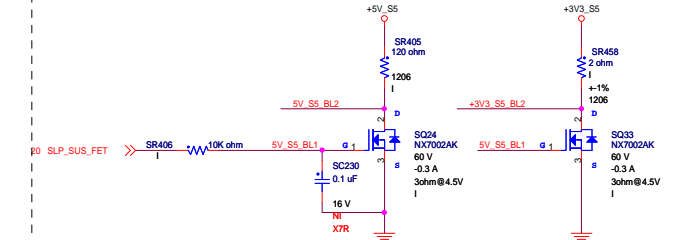




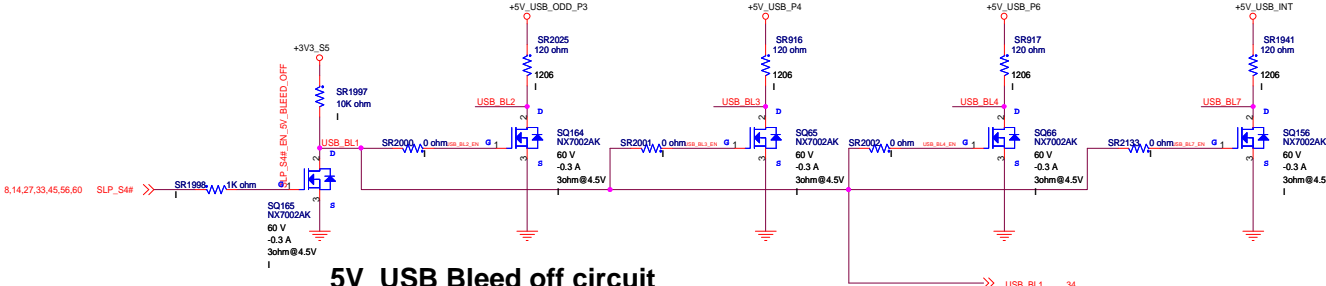
+12V Bleed off circuit



5V_S5 and 3V_S5 Bleed off circuit

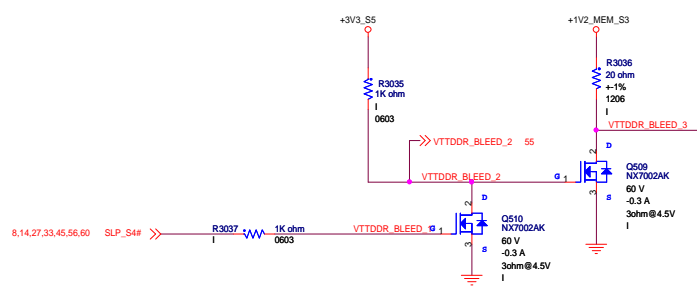


5V_USB Bleed off circuit

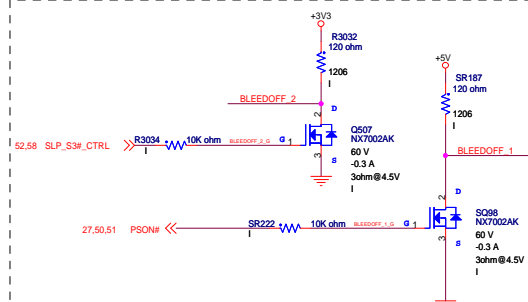


DESIGN NOTE: THESE CIRCUITS ARE USED TO BLEED OFF 1.5V DDR

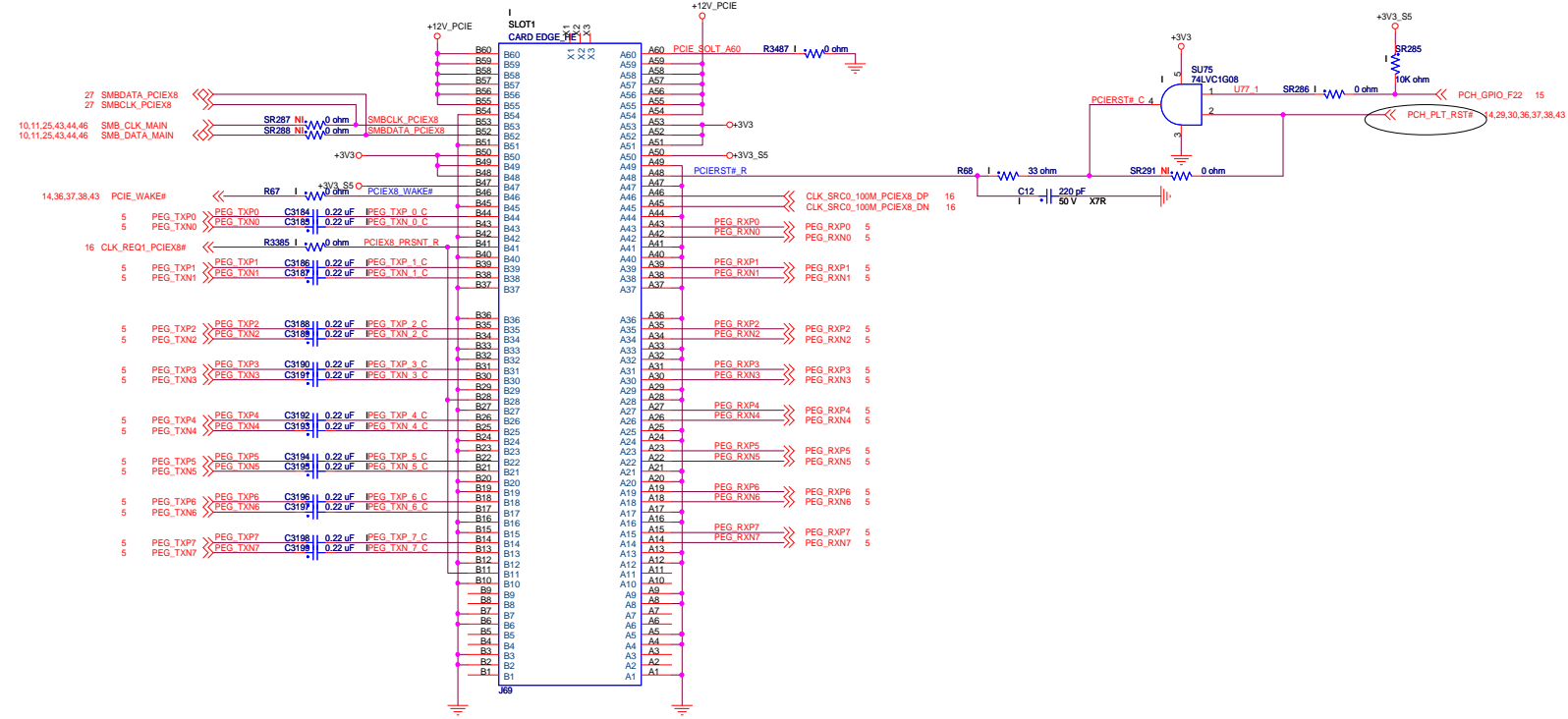
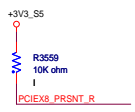
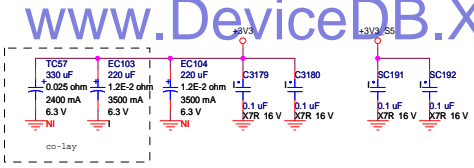
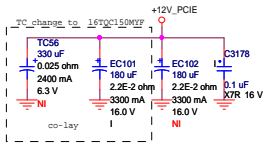
+1V2_MEM Bleed off circuit




5V & 3.3V Bleed off circuit



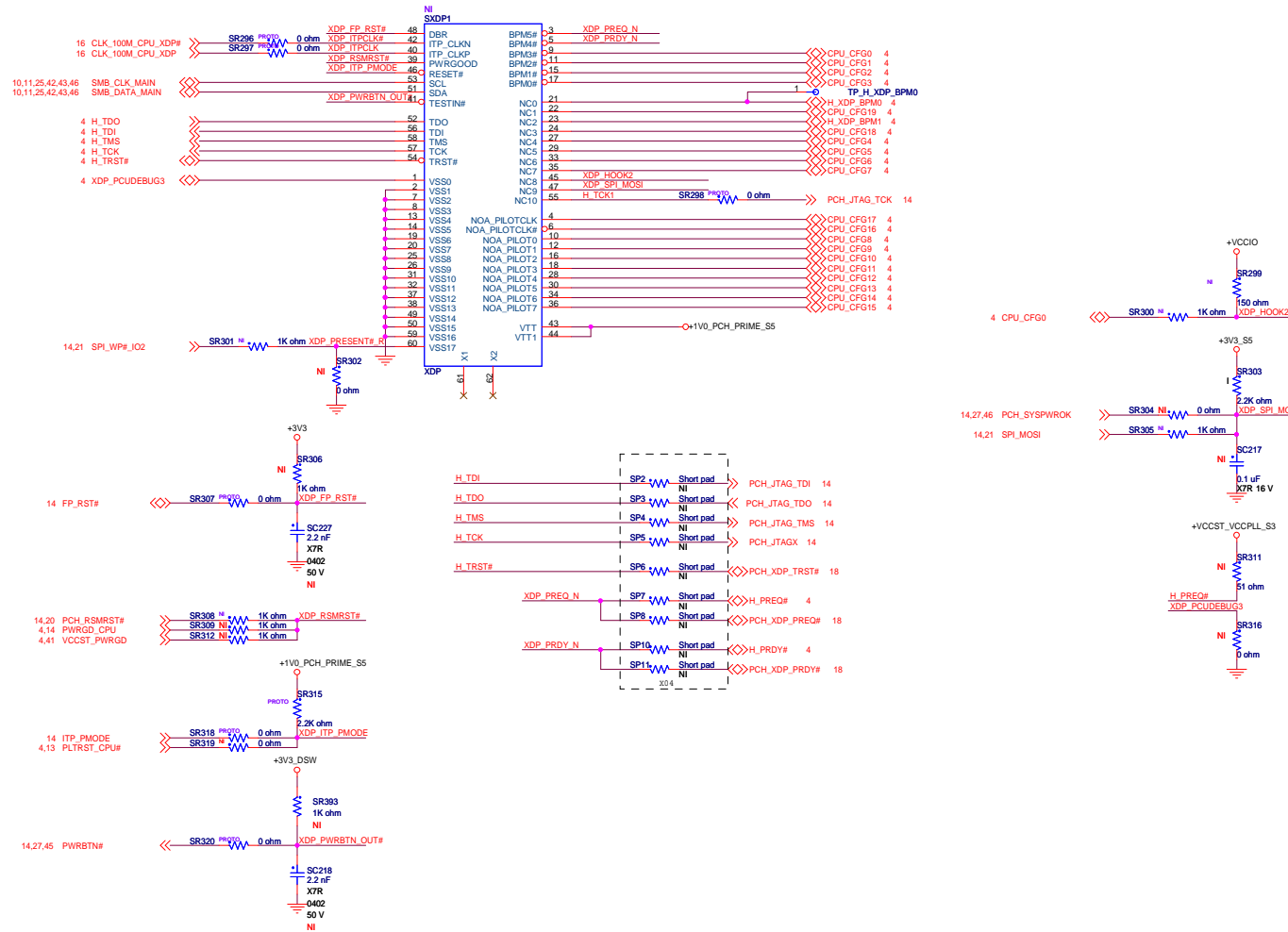
LITE-ON TECHNOLOGY CORP. LITEON	
Title 41. PWRGD & BLEED OFF	
Size C	Document Number JC113
Date	Friday, August 26, 2016
Sheet	41 of 67
Rev	X03



LITE-ON TECHNOLOGY CORP.		LITEON	
Title 42. PCIEX8			
Size C	Document Number JC113	Rev X03	
Date Friday, August 26, 2016	Sheet 42	of 67	

LITE-ON TECHNOLOGY CORP.		
Title		
43. PCIE X8		
Size	Document Number	Rev
C	JC113	X03
Date:	Friday, August 26, 2016	Sheet 43 of 67

Intel XDP Debugging Connector



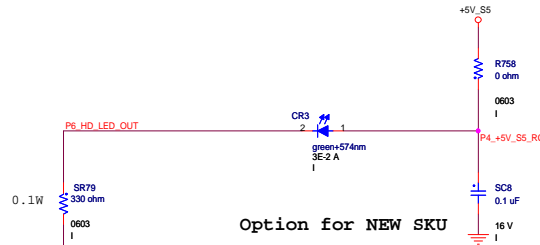
POWER BUTTON & LED

Color	Function
G	HDD

For NEC SKU:
 Remove:
 R765Q, Q42, R762
 SW1
 CR1

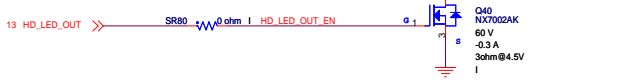
Install:
 R779
 SW1_
 CR1_

Id = 25mA @ 2.8V (SPEC)
 Id = (5V-2.8V) / 330ohm = 5mA
 5mA * 3.2 V = 16 mW
 0.1W (For Current limit R)

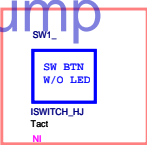
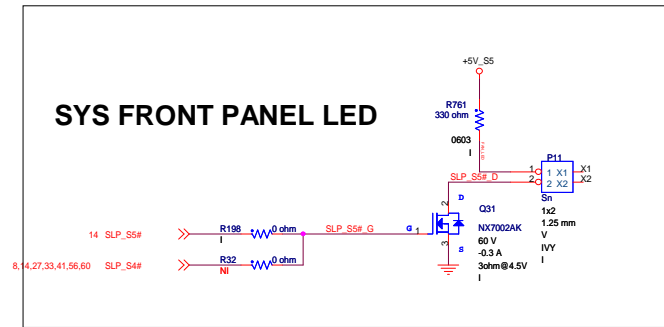


Option for NEW SKU

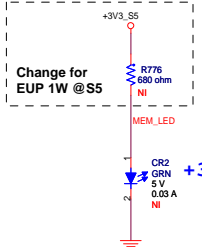
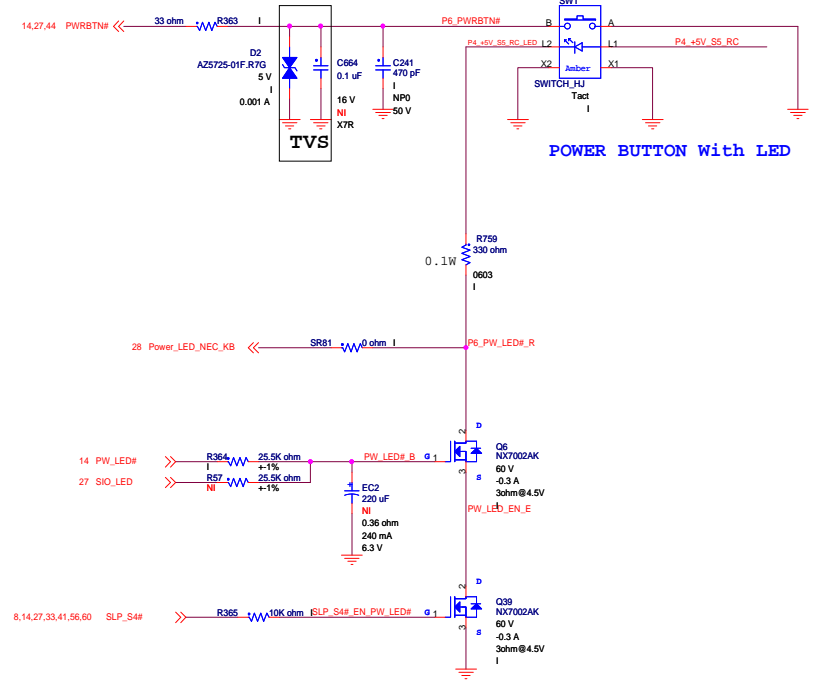
HDD LED



SYS FRONT PANEL LED

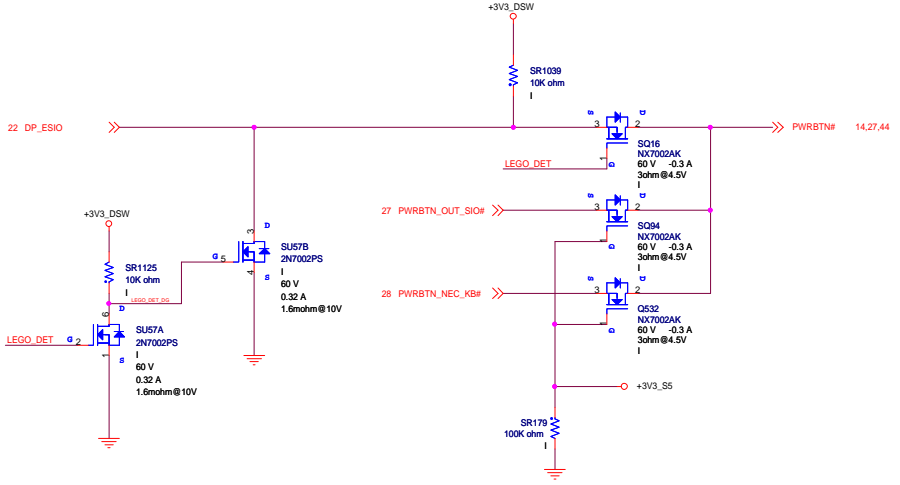
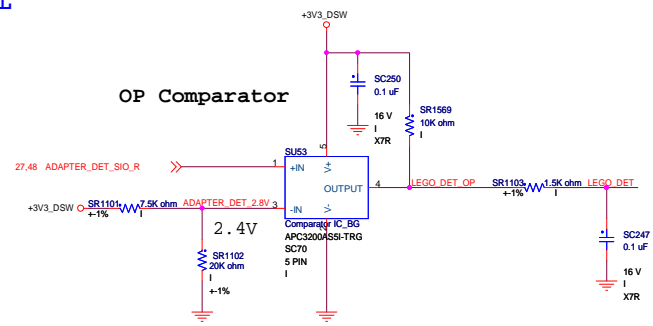


POWER BUTTON With LED



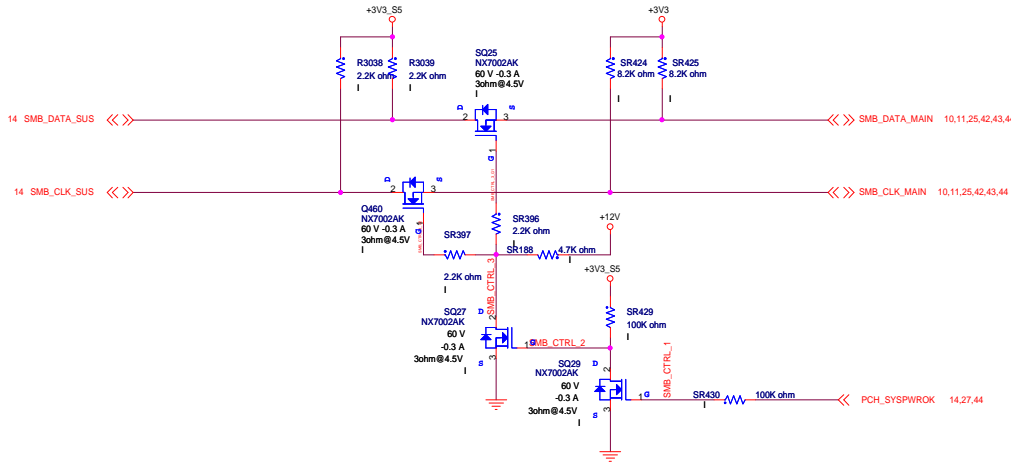
Change for EUP 1W @S5

PCA LED CIRCUITS

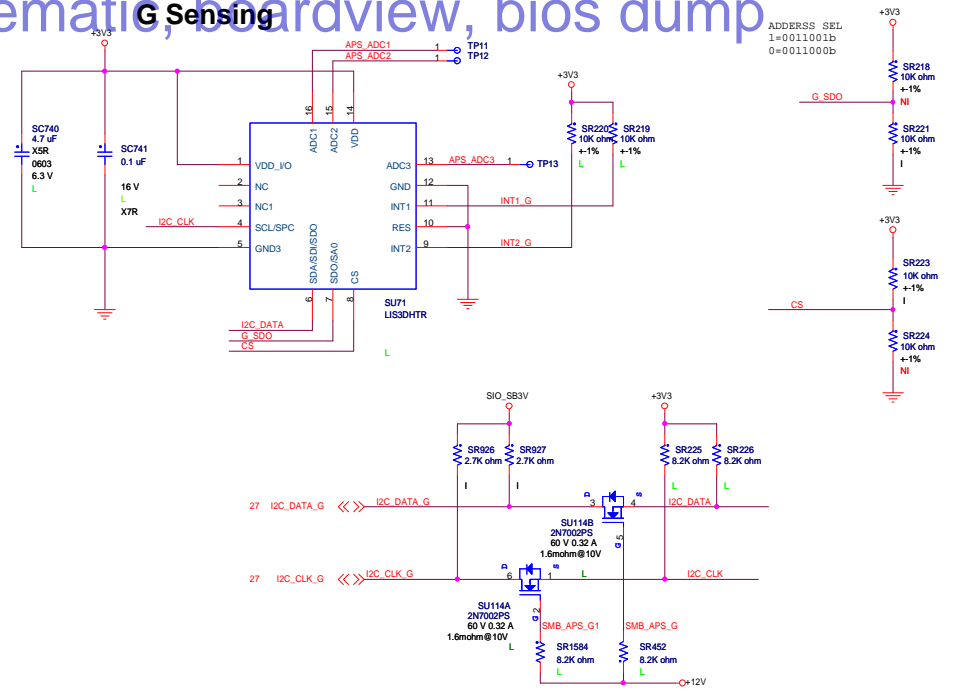


LITE-ON TECHNOLOGY CORP. LITEON	
Title: 45. Button/LED	
Size: C	Document Number: JC113
Date: Friday, August 26, 2016	Rev: X03
Sheet: 45 of 67	

SM Bus

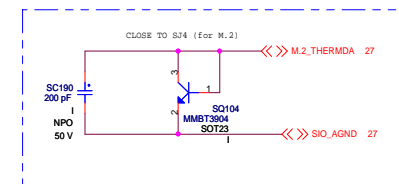
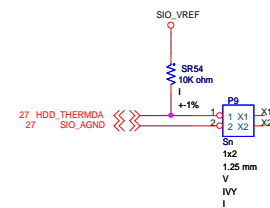
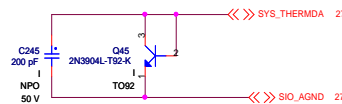
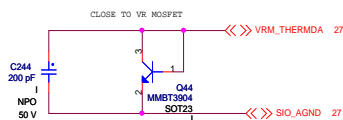


G Sensing



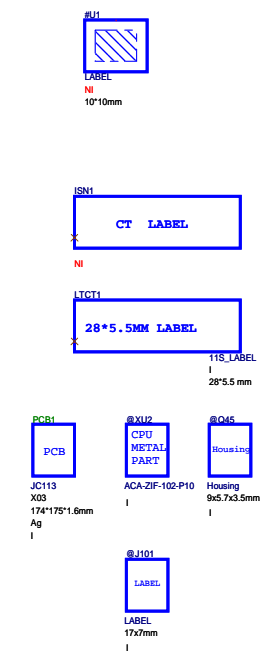
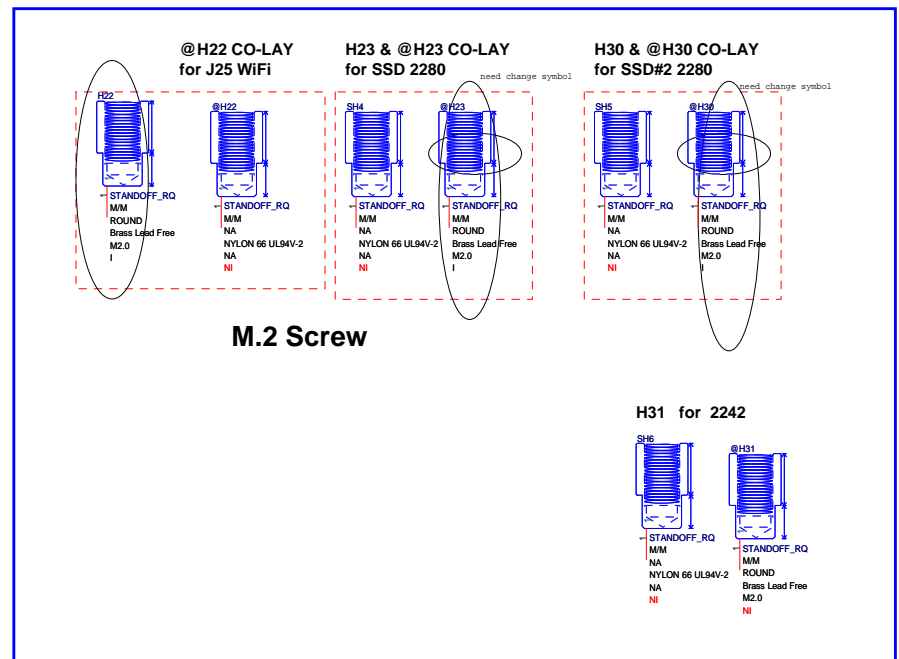
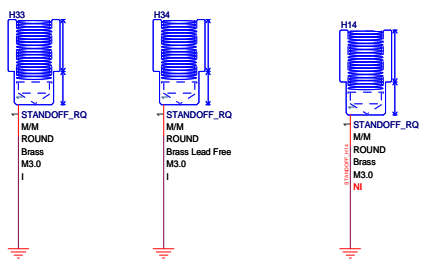
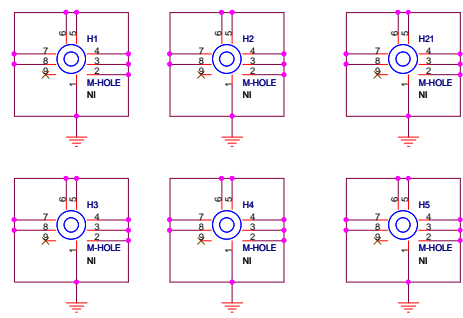
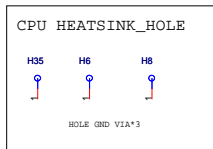
Temperature Sensing

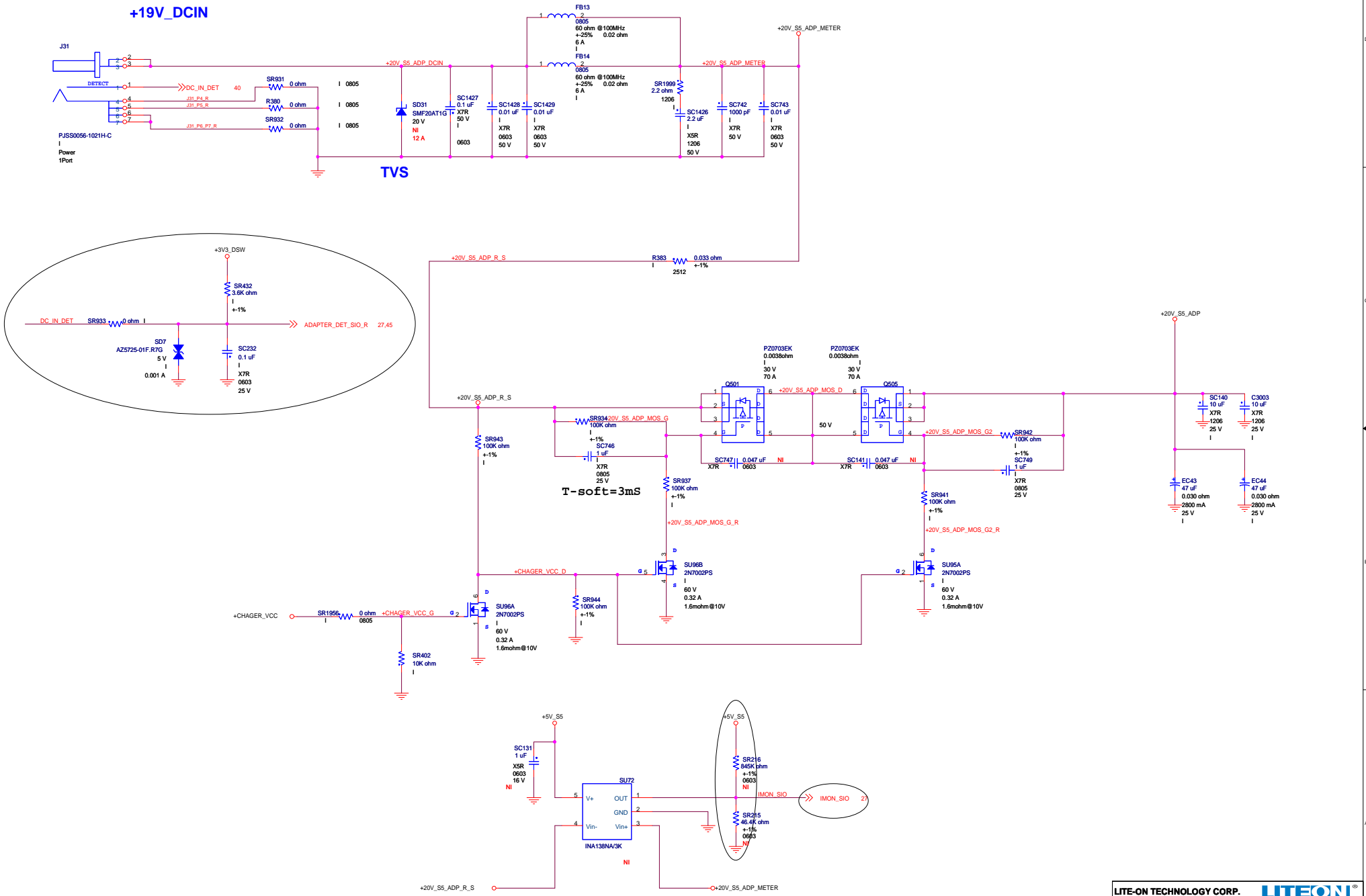
Current Mode



CAD NOTE : Place MLCC Close to Thermal Diode

Acceptable Transistor Component
 ST Micro: MMBT3904
 ON Semiconductor: MMBT3904LT1
 Fairchild Semiconductor: MMBT3904FSCT





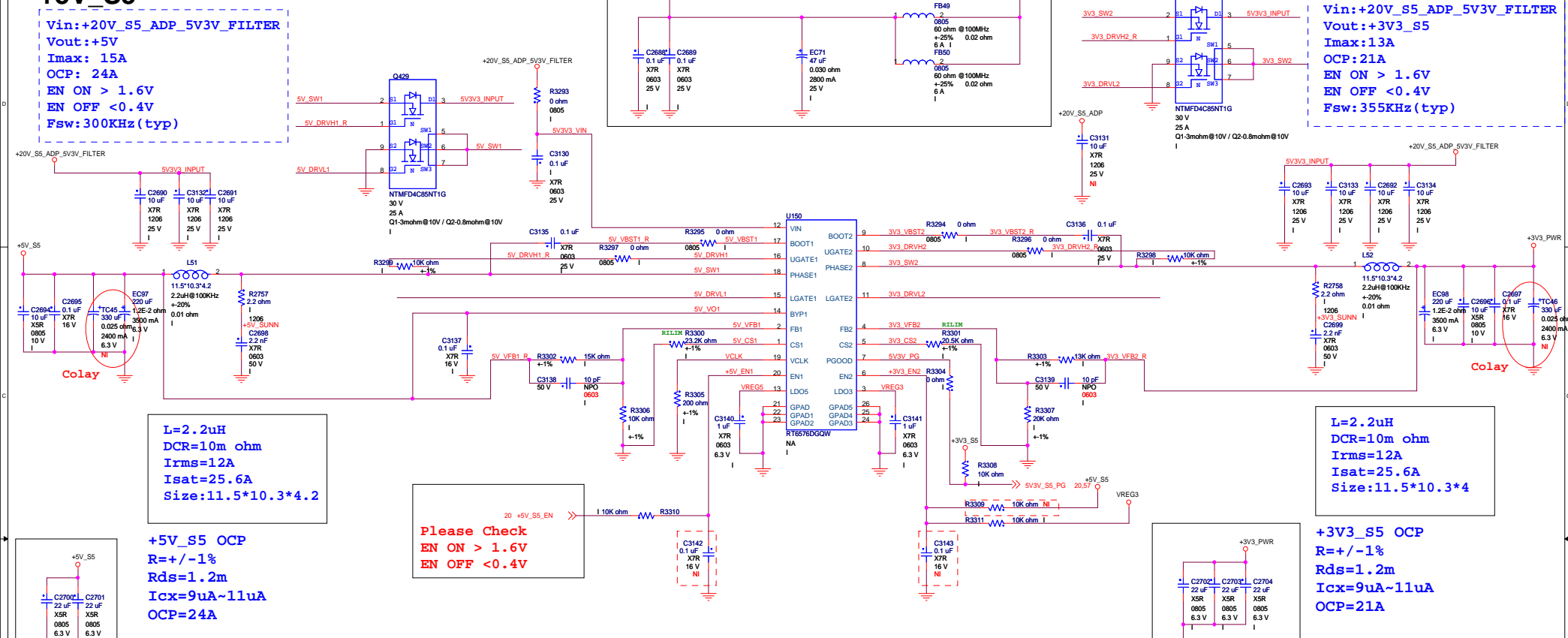
LITE-ON TECHNOLOGY CORP. LITEON	
Title 48.+20V_S5_ADP	
Size C	Document Number JC113
Date	Friday, August 26, 2016
Sheet	48 of 67
Rev	X03

+5V_S5

Vin:+20V_S5_ADP_5V3V_FILTER
 Vout:+5V
 Imax: 15A
 OCP: 24A
 EN ON > 1.6V
 EN OFF < 0.4V
 Fsw: 300KHz (typ)

+3V3_PWR

Vin:+20V_S5_ADP_5V3V_FILTER
 Vout:+3V3_S5
 Imax: 13A
 OCP: 21A
 EN ON > 1.6V
 EN OFF < 0.4V
 Fsw: 355KHz (typ)



L=2.2uH
 DCR=10m ohm
 Irms=12A
 Isat=25.6A
 Size:11.5*10.3*4.2

L=2.2uH
 DCR=10m ohm
 Irms=12A
 Isat=25.6A
 Size:11.5*10.3*4

Please Check
 EN ON > 1.6V
 EN OFF < 0.4V

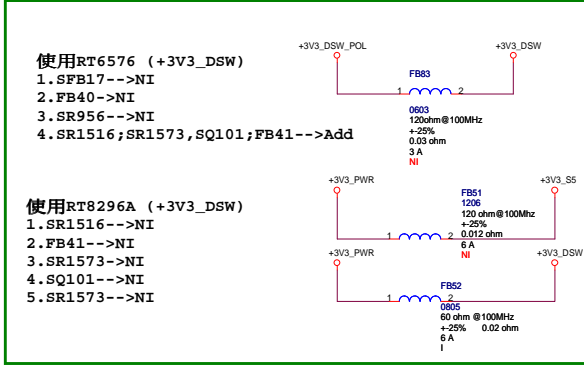
+5V_S5 OCP
 R=+/-1%
 Rds=1.2m
 Icx=9uA~11uA
 OCP=24A

+3V3_S5 OCP
 R=+/-1%
 Rds=1.2m
 Icx=9uA~11uA
 OCP=21A

OCP
 +3V3_S5
 $R_{limit} = I_{limit} * R_{on} * 8 / 10uA = 20.16K$
 +5V_S5
 $R_{limit} = I_{limit} * R_{on} * 8 / 10uA = 23.04K$
 $R_{on} = 1.2m$ $I_{cx} = 10uA$ $R = +/- 1\%$

+3V3_S5
 $\Delta I_L / 2 = 5.43 / 2 = 1.79$

+5V_S5
 $\Delta I_L / 2 = 5.68 / 2 = 2.84$

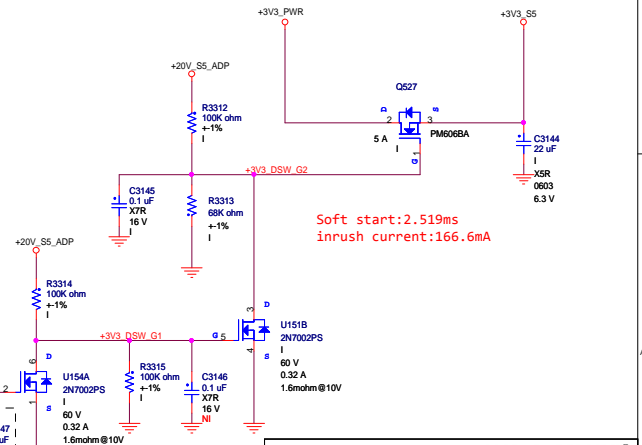


Cin=117uF
 ripple current:13.3A

+5V_S5:
 Cout=220uF
 ripple current:3.5A

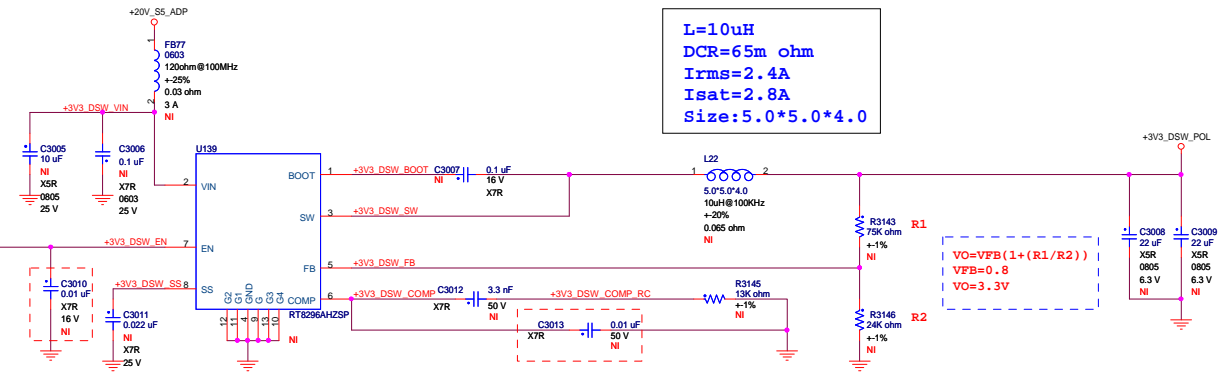
+3V3_S5:
 Cout=220uF
 ripple current:3.5A

+3V3_S5



+3V3_DSW

Please Check
 IC EN ON > 2.7 V
 IC EN OFF < 0.4 V

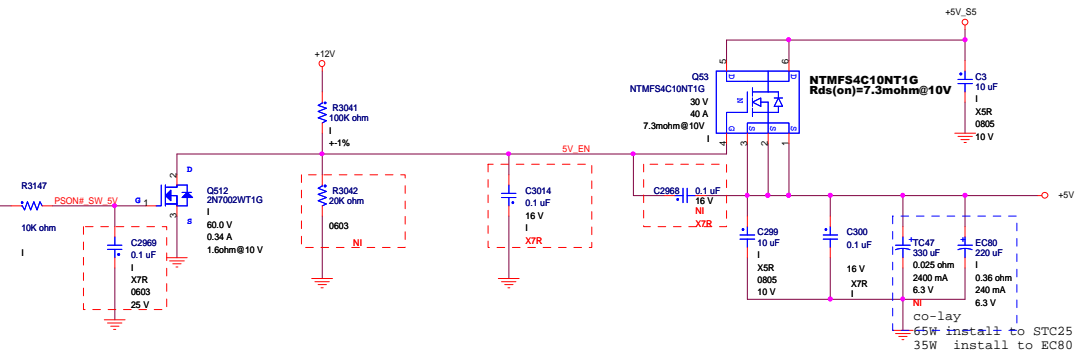


L=10uH
 DCR=65m ohm
 Irms=2.4A
 Isat=2.8A
 Size:5.0*5.0*4.0

+3V3_DSW_POL
 Temp. Max. DC: 0.3A
 OCP: 5.1A
 IC EN ON > 2.7V
 IC EN OFF < 0.4V

+5V

27.41.51 PSON#
 Please Check
 EN OFF > 2.5 V
 EN ON < 1 V

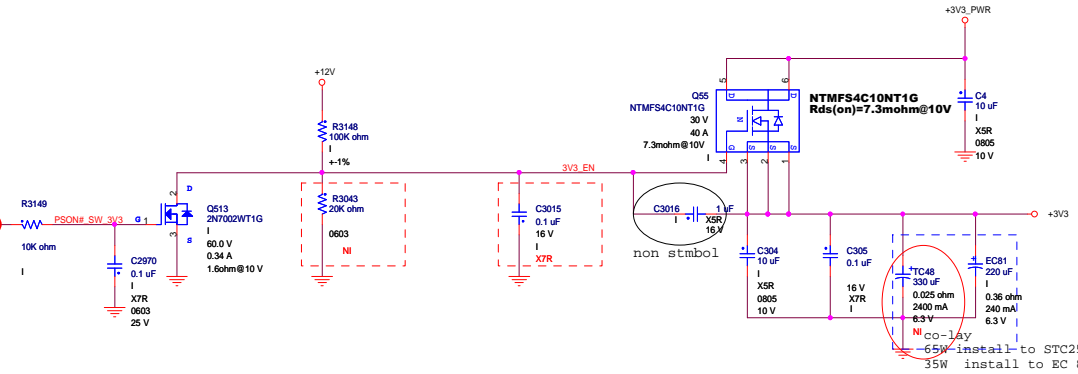


+5V @Imax 6.94A

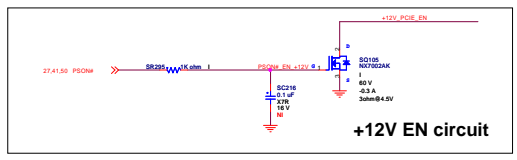
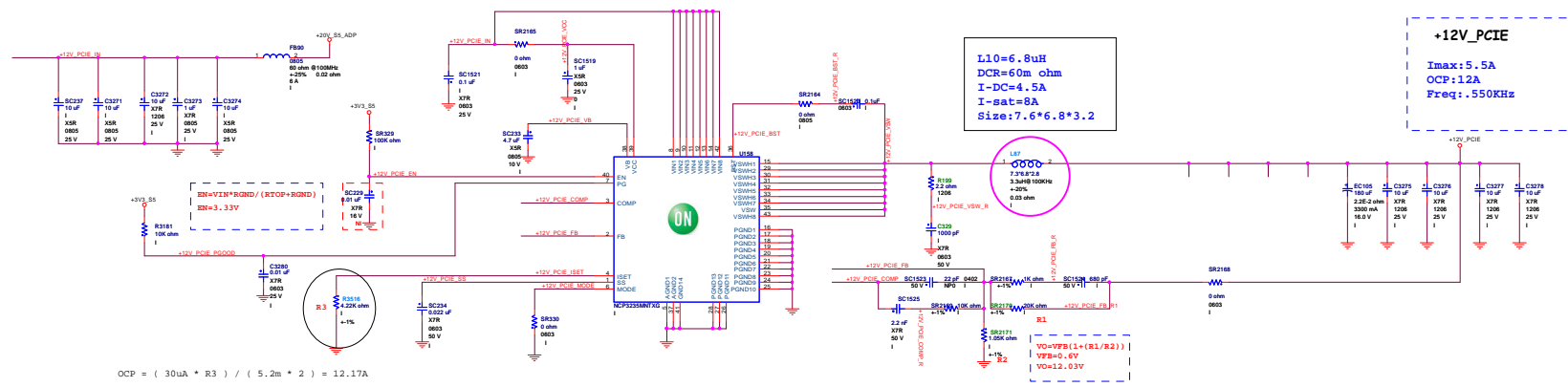
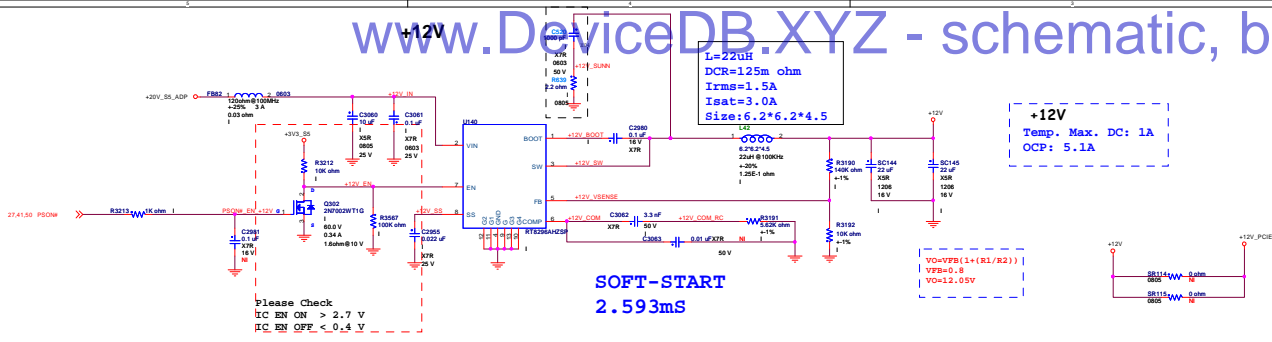
SOFT-START
 +5V: 5.835ms
 +3V3: 3.449ms

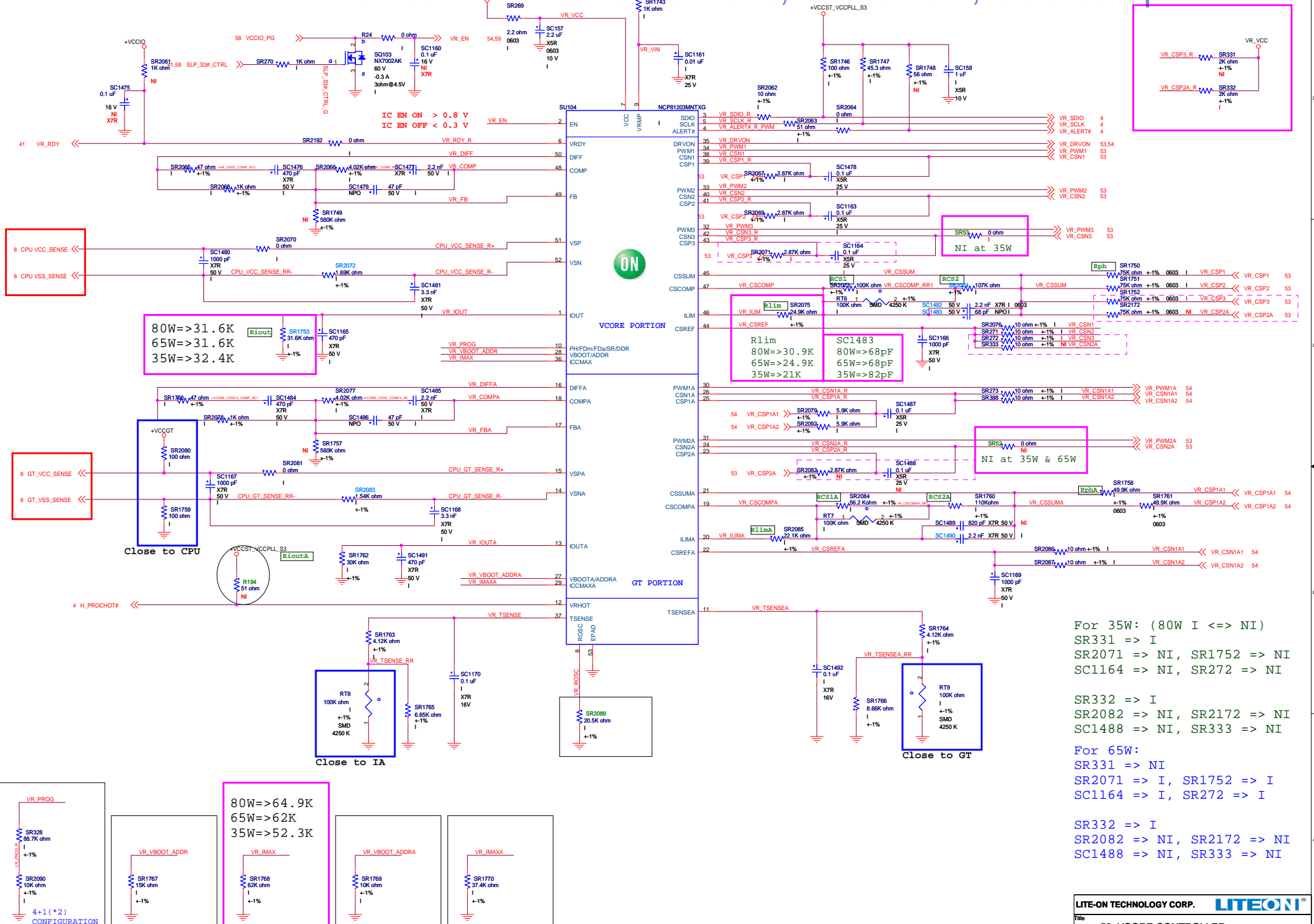
+3V3

27.41.51 PSON#
 Please Check
 EN OFF > 2.5 V
 EN ON < 1 V



+3V3 @Imax 6.74A





8 CPU_VCC_SENSE
8 CPU_VSS_SENSE

8 GT_VCC_SENSE
8 GT_VSS_SENSE

VR_PROG
VR_VBOOT_ADDR
VR_VBOOT_ADDR
VR_IMAX
VR_VBOOT_ADDR
VR_IMAXA

80W=>31.6K
65W=>31.6K
35W=>32.4K

80W=>64.9K
65W=>62K
35W=>52.3K

VR_TSENSEA
VR_TSENSE RR
VR_TSENSEA
VR_TSENSE RR

VR_ILIM
VR_CSREF
VR_ILIM
VR_CSREF

RT9
RT8

NI at 35W & 65W

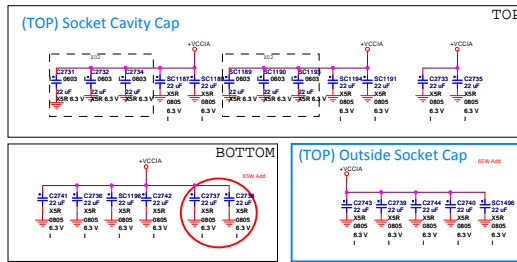
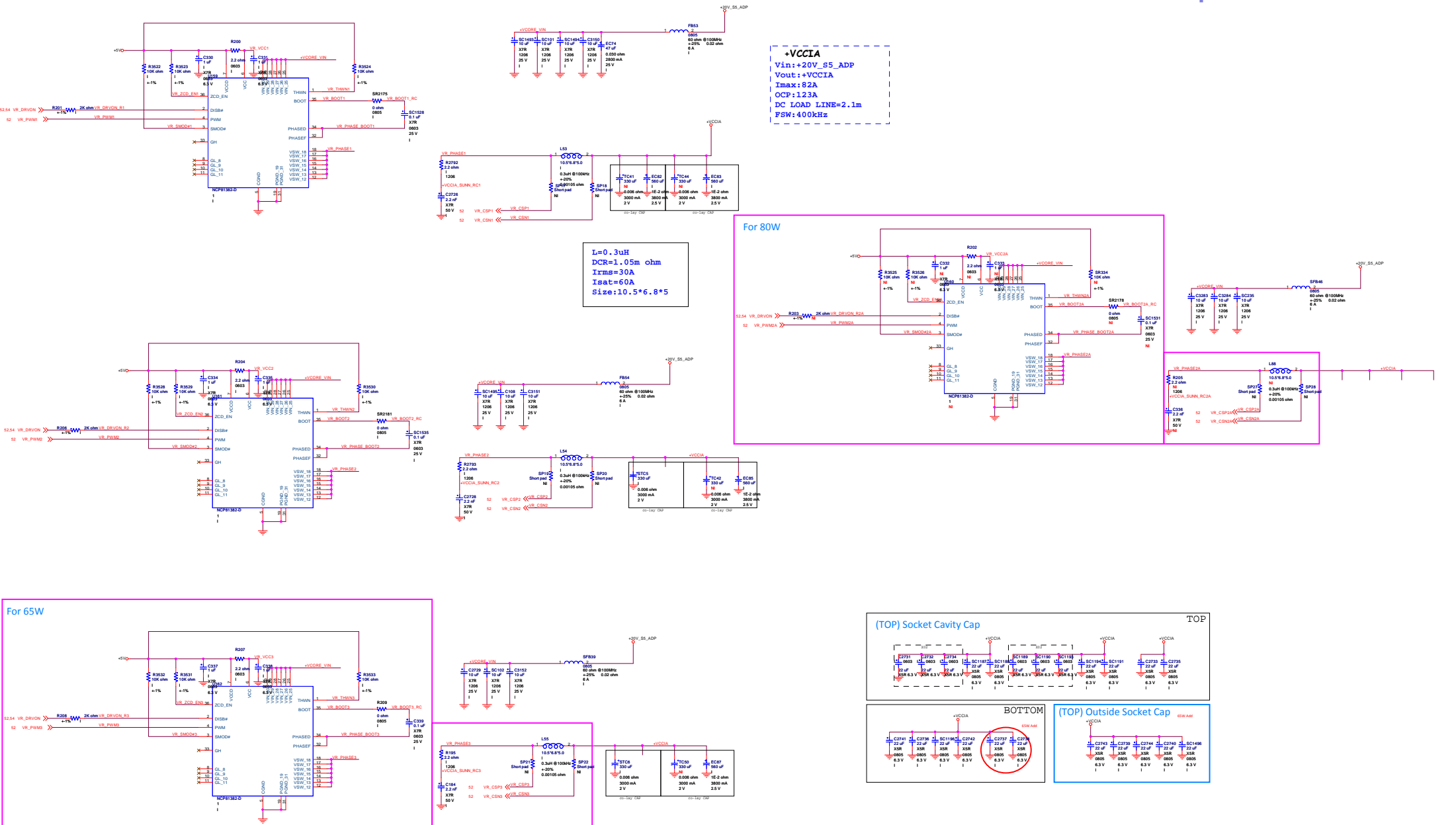
For 35W: (80W I <=> NI)
SR331 => I
SR2071 => NI, SR1752 => NI
SC1164 => NI, SR272 => NI

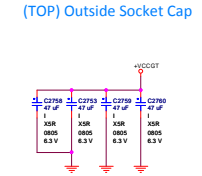
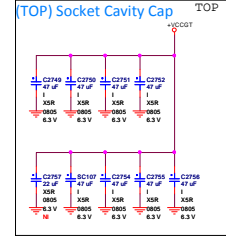
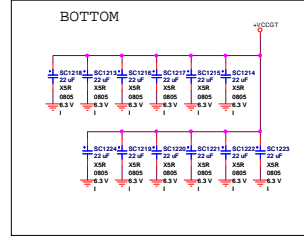
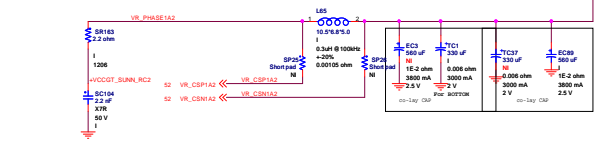
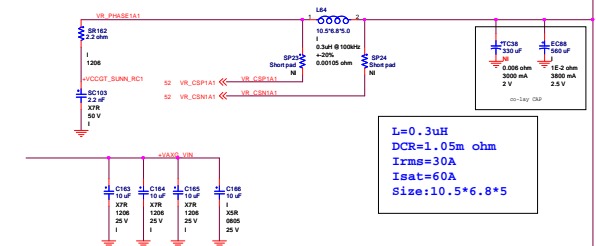
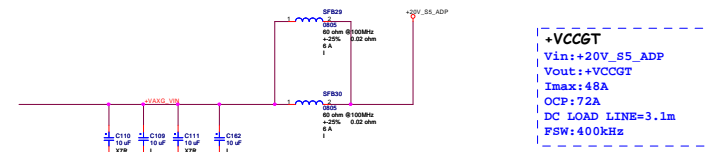
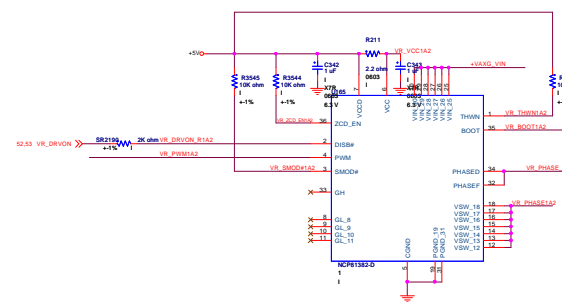
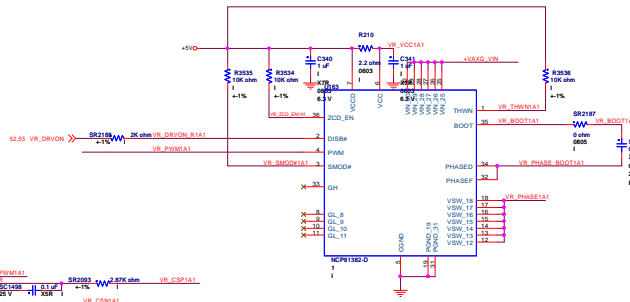
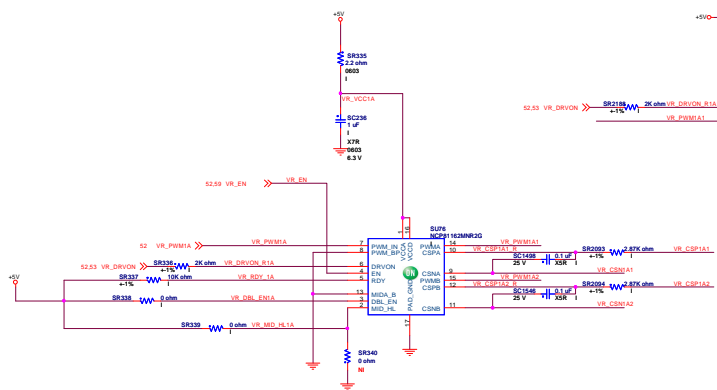
SR332 => I
SR2082 => NI, SR2172 => NI
SC1488 => NI, SR333 => NI

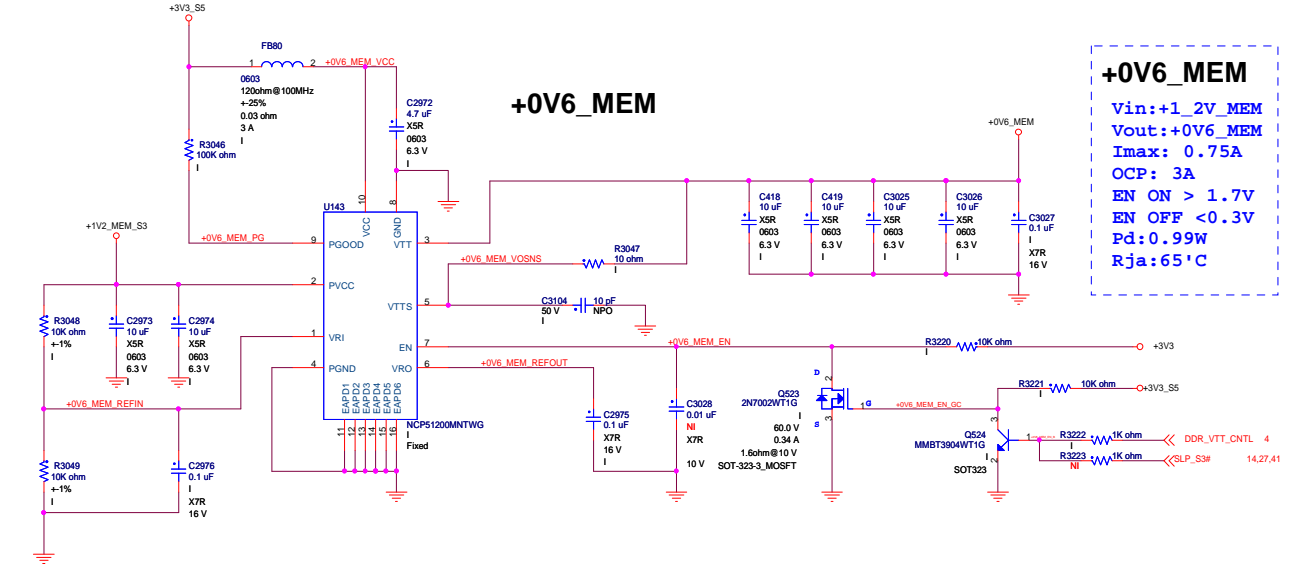
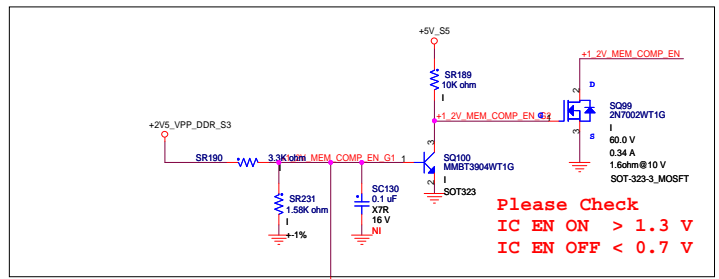
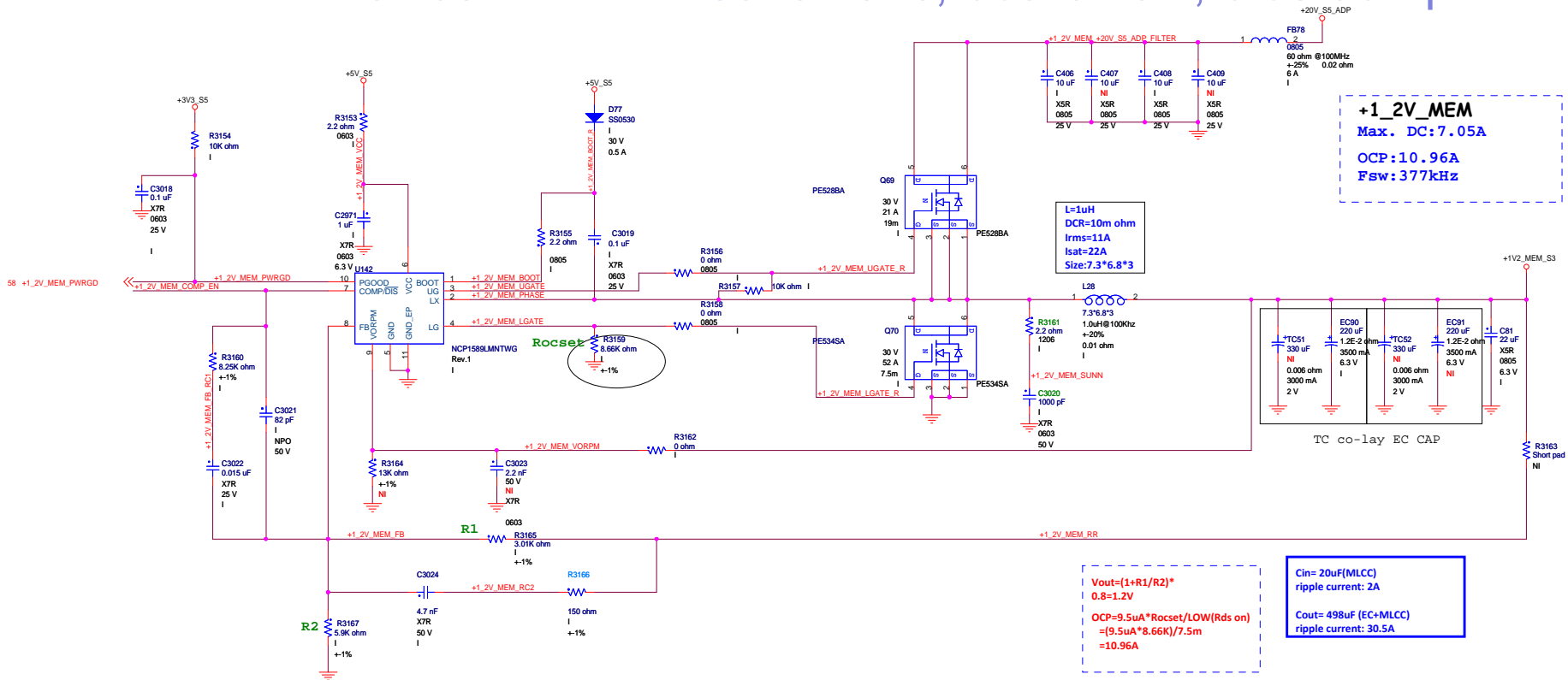
For 65W:
SR331 => NI
SR2071 => I, SR1752 => I
SC1164 => I, SR272 => I

SR332 => I
SR2082 => NI, SR2172 => NI
SC1488 => NI, SR333 => NI

LITE-ON TECHNOLOGY CORP. LITEON	
Title 52. VCORE CONTROLLER	
Size C	Document Number JC110
Date Friday, August 26, 2016	Rev X03
Sheet 52	of 67







LITE-ON TECHNOLOGY CORP.		LITEON
File: 55. +1V2V_DDR / +0V6_VTT		
Size C	Document Number	Rev
	JC113	X03
Date:	Friday, August 26, 2016	Sheet 55 of 67

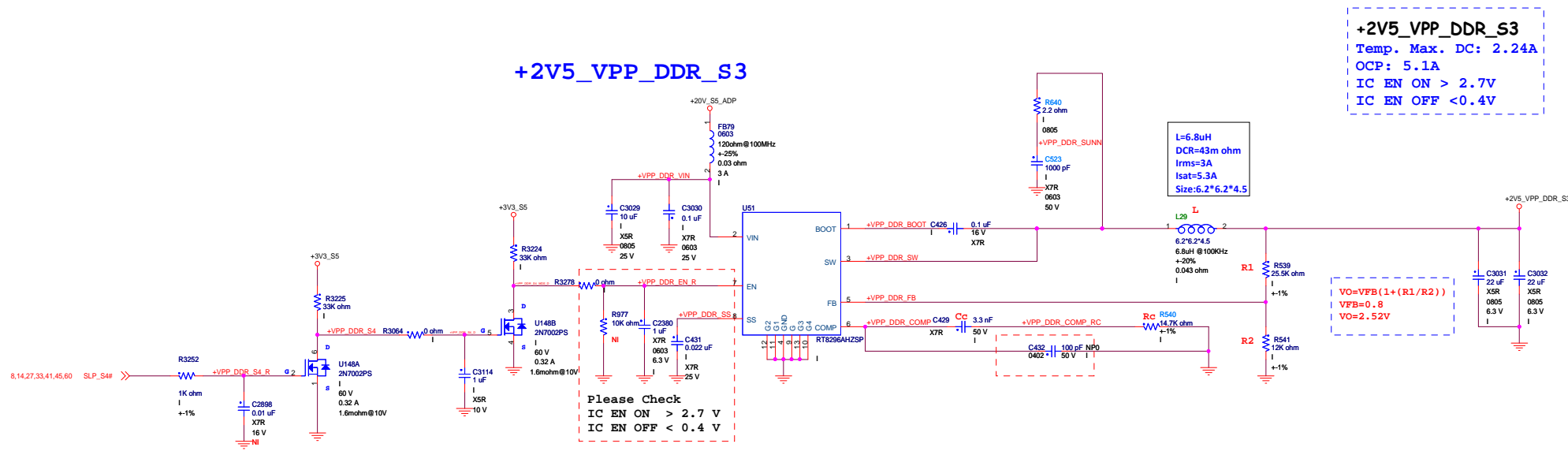
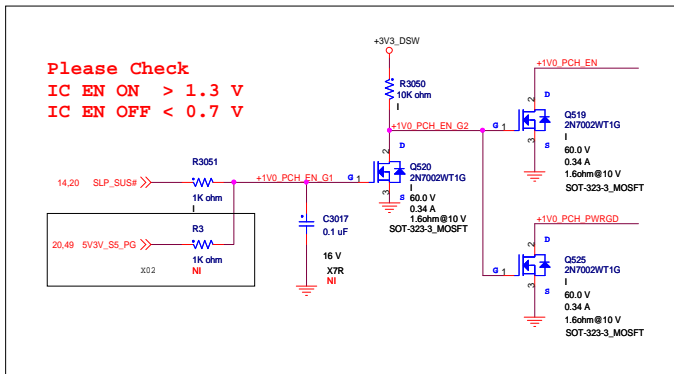
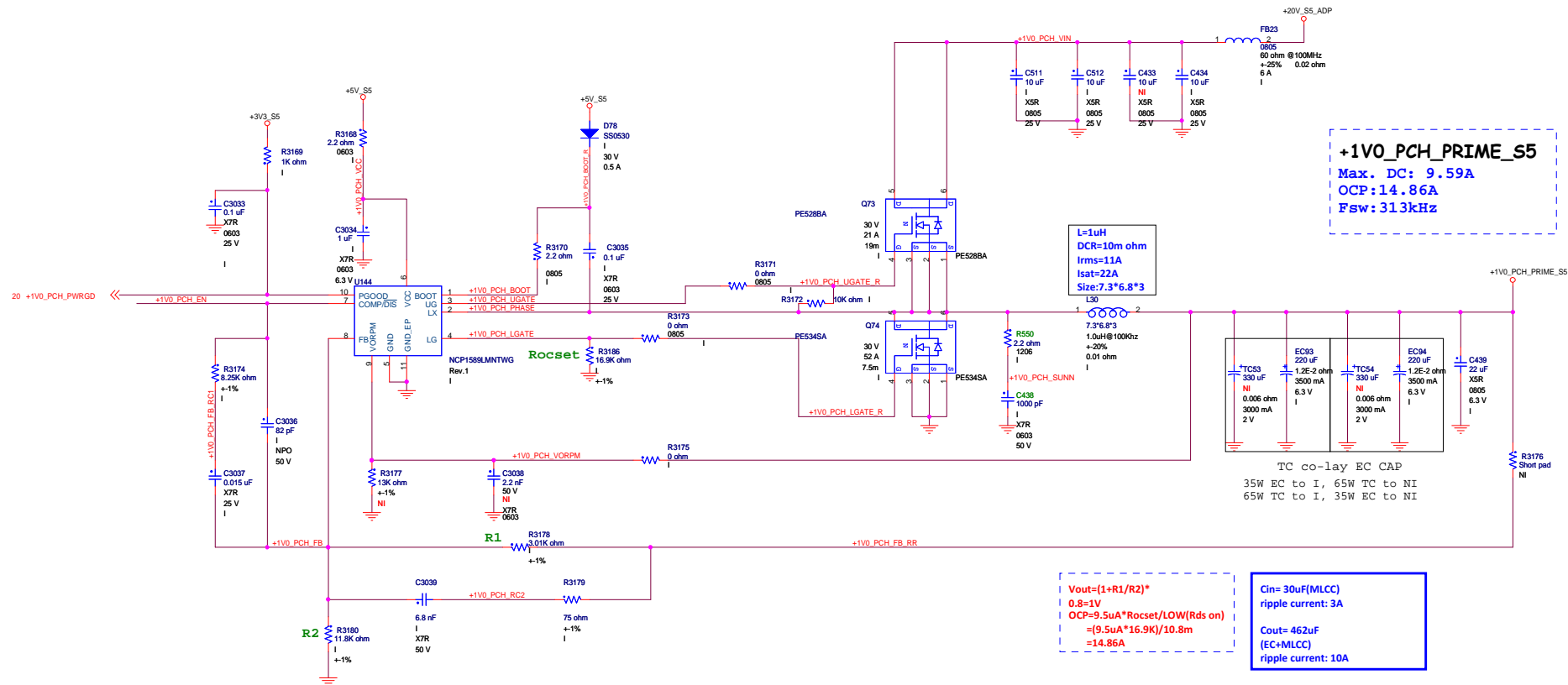
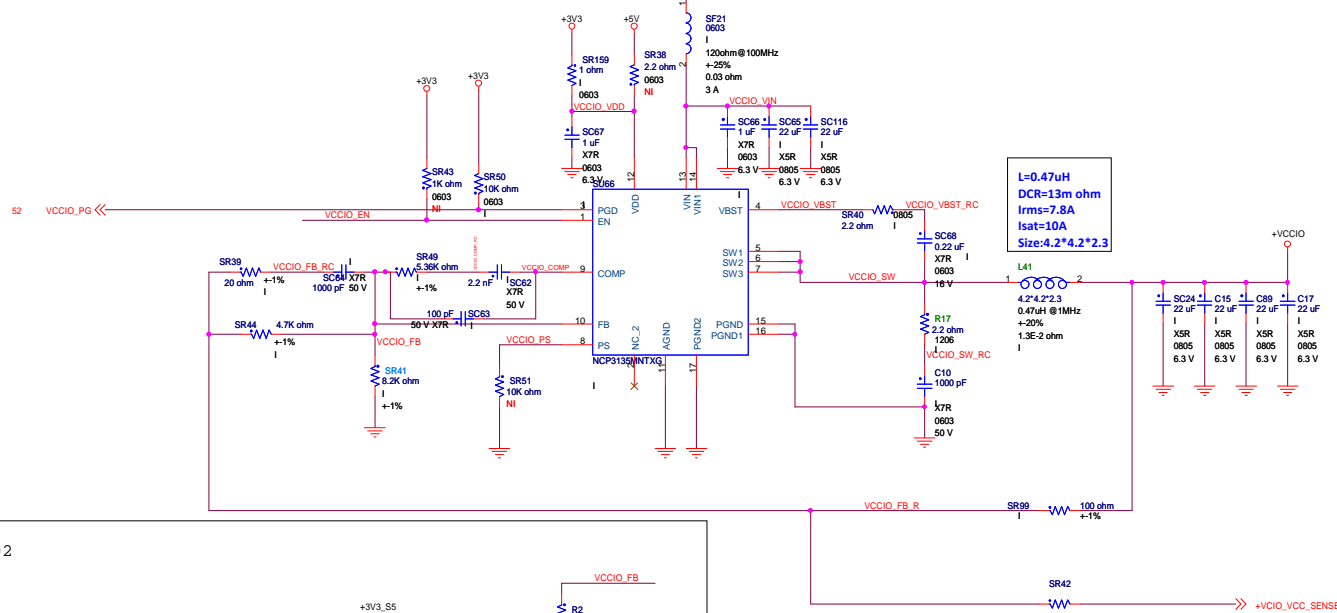


Table 1. Recommended Component Selection

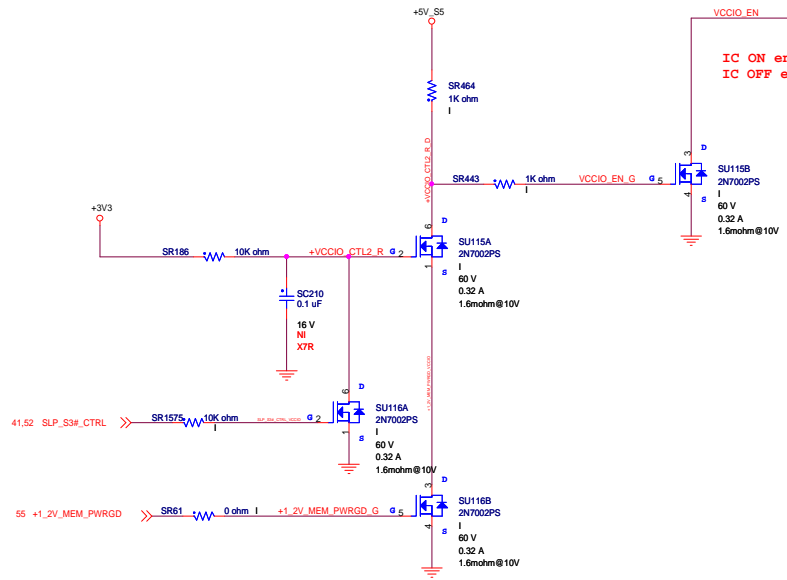
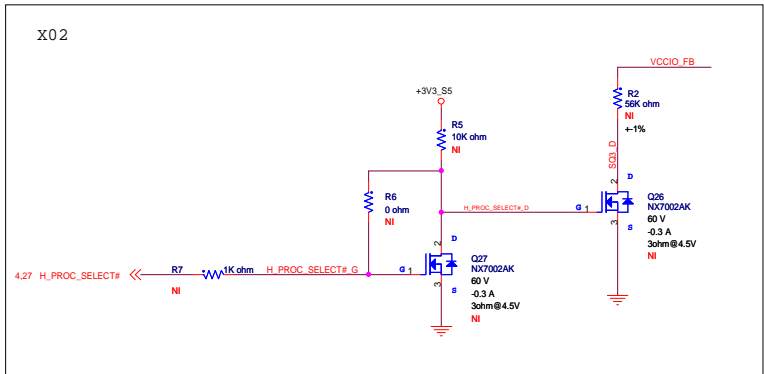
VOUT (V)	R1 (kΩ)	R2 (kΩ)	Rc (kΩ)	Cc (nF)	L (μH)	COUt (μF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2



VCCIO
 Temp. Max. DC: 5.5A
 Vout: 0.95V
 OCP: 6.8A

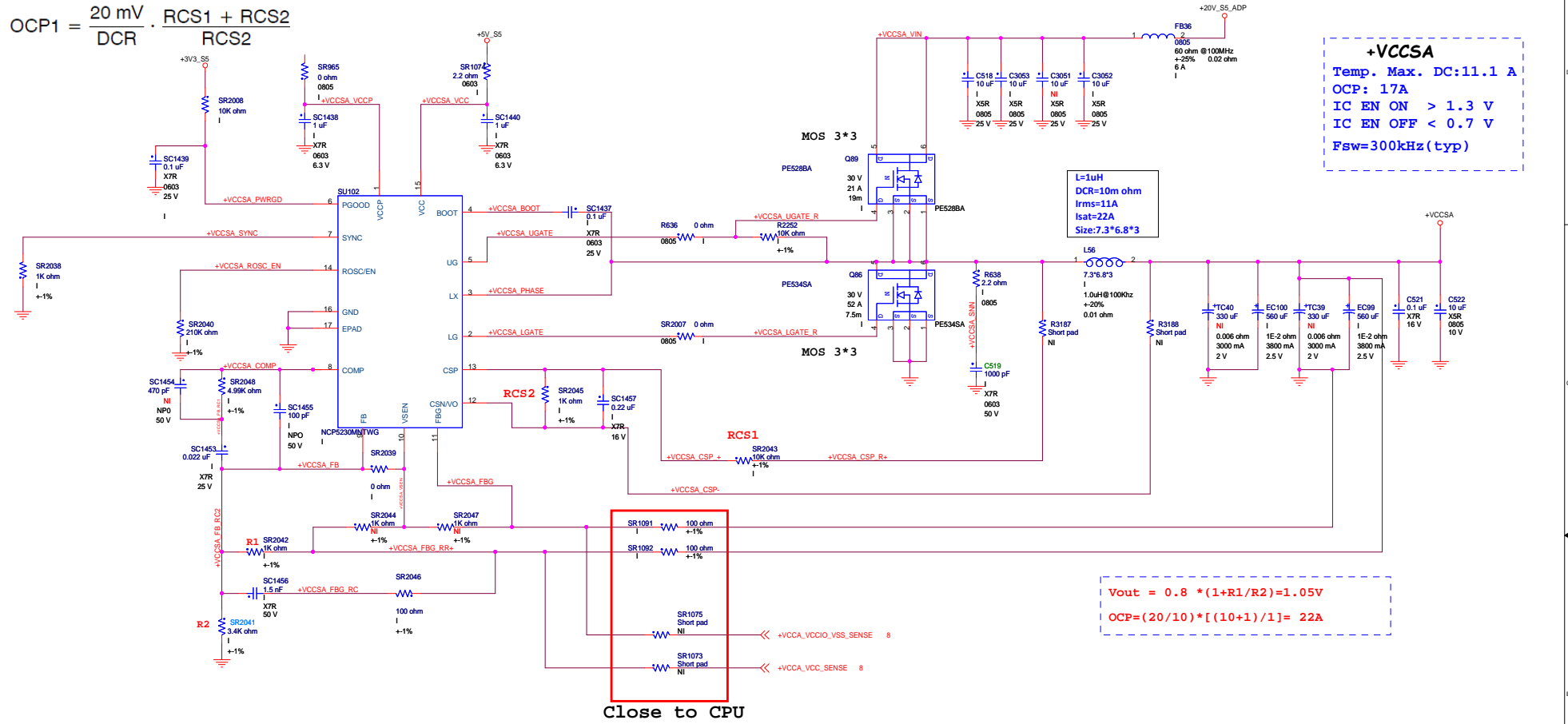


L=0.47uH
 DCR=13m ohm
 Irms=7.8A
 Isat=10A
 Size:4.2*4.2*2.3



IC ON enable >1.18
 IC OFF enable <0.18

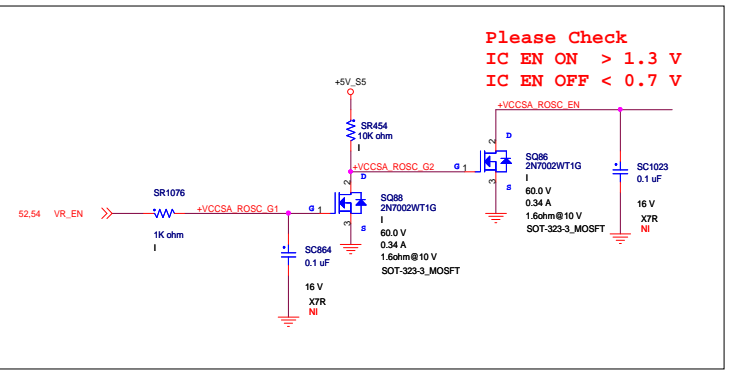
$$OCP1 = \frac{20 \text{ mV}}{DCR} \cdot \frac{RCS1 + RCS2}{RCS2}$$



+VCCSA
 Temp. Max. DC: 11.1 A
 OCP: 17A
 IC EN ON > 1.3 V
 IC EN OFF < 0.7 V
 Fsw=300kHz (typ)

$V_{out} = 0.8 * (1+R1/R2) = 1.05V$
 $OCP = (20/10) * [(10+1)/1] = 22A$

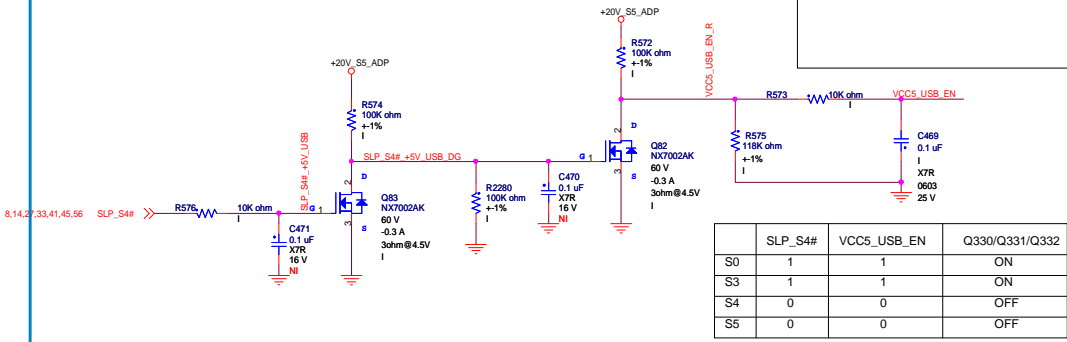
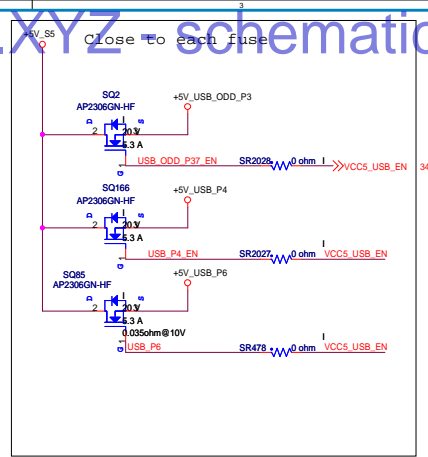
Close to CPU



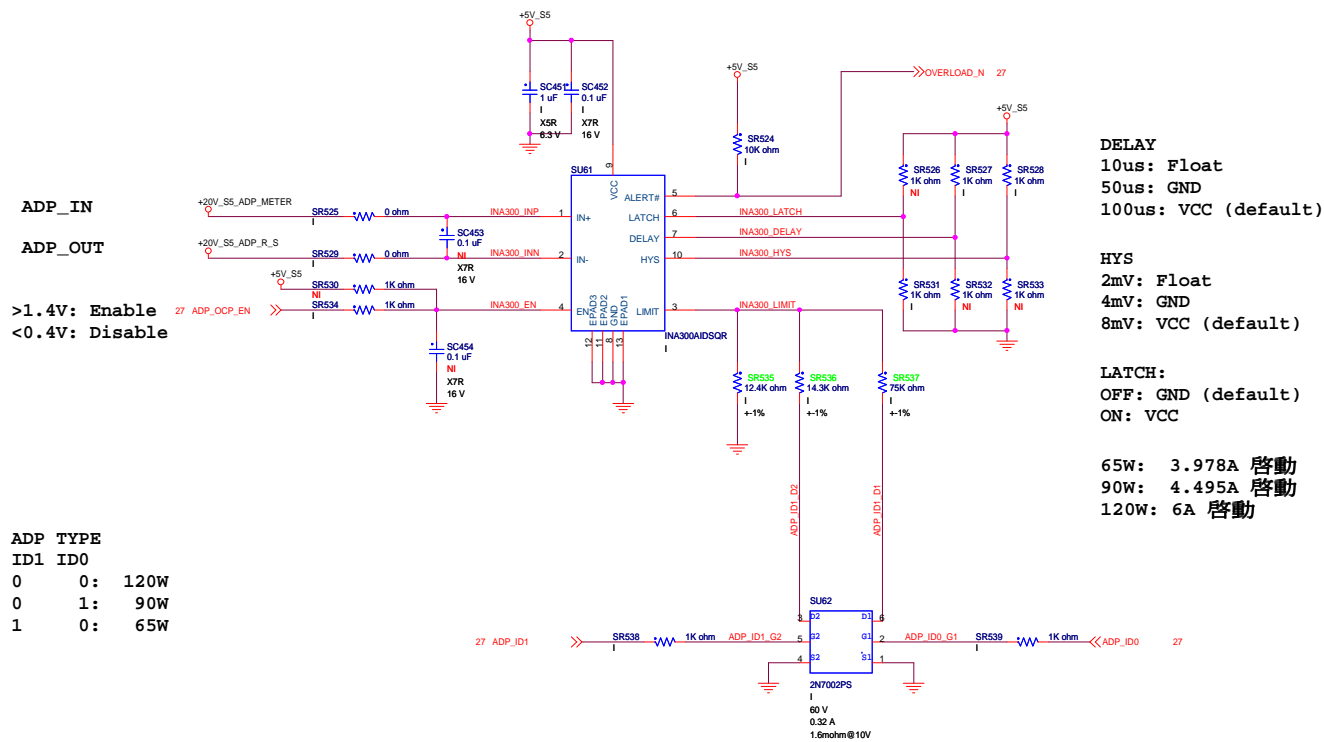
Please Check
 IC EN ON > 1.3 V
 IC EN OFF < 0.7 V

For Google SKU
Keep Q79 ,Q80 ,SQ85 then remove Others

+5V_USB



	SLP_S4#	VCC5_USB_EN	Q330/Q331/Q332
S0	1	1	ON
S3	1	1	ON
S4	0	0	OFF
S5	0	0	OFF



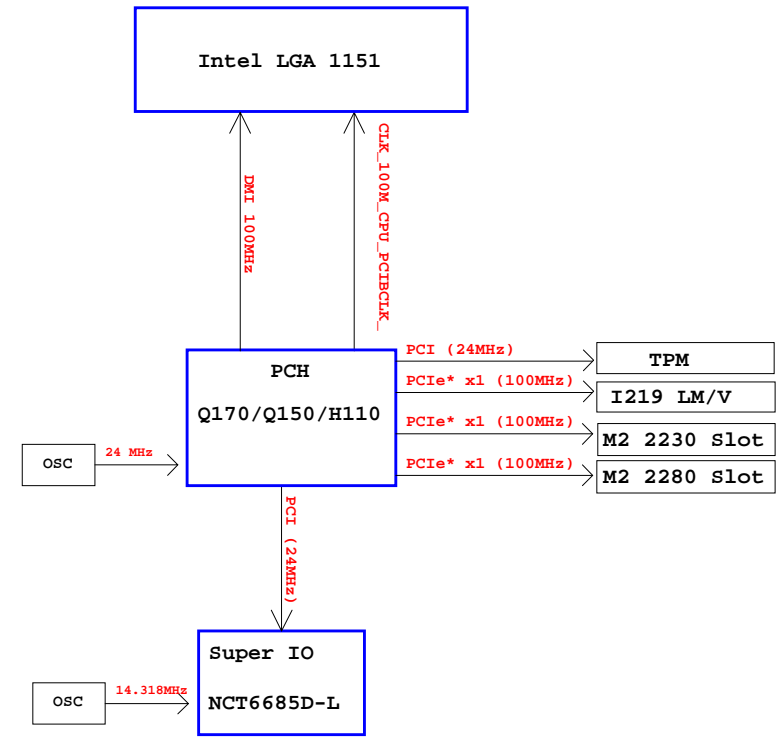
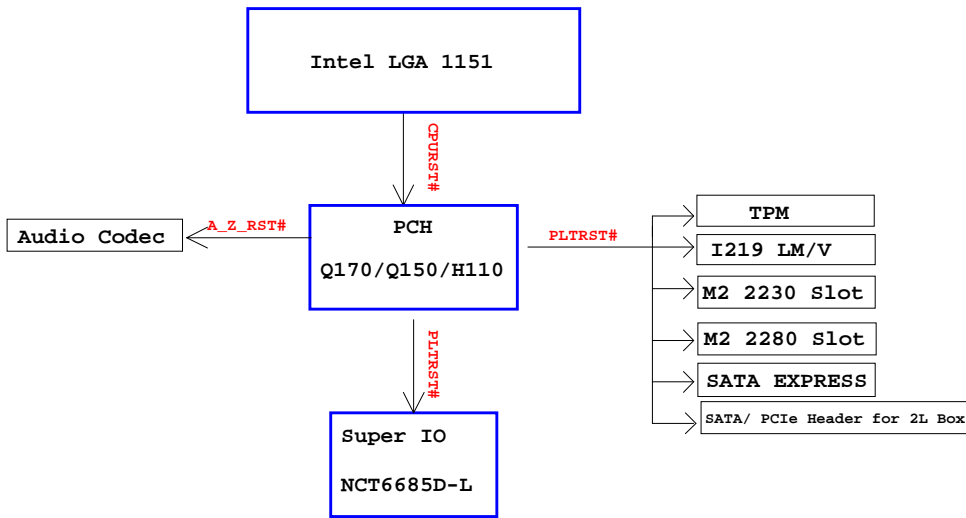
Signal	Usage	When Sampled	Comment
GSP0_MOSI / GPP_B18	NO REBOOT 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Disable "No Reboot" mode 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running IT/XPDP.
SMBALERT# / GPP_C2	TLS CONFIDENTIALITY 0: DISABLE 1: ENABLE (DEFAULT)	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
GSP1_MOSI / GPP_B22	BOOT BIOS STRAP 0: SPI (DEFAULT) 1: ESPI/LPC	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10 Boot BIOS Destination 0 SPI 1 LPC
SML0ALERT# / GPP_C5	ESPI ENABLE STRAP 0: LPC (Default) 1: ESPI	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC is selected for EC. (Default) 1 = eSPI is selected for EC.
SML1ALERT# / PCH0DT# / GPP_B23	EXI BOOT STALLBYPASS STRAP 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H12 / SML2ALERT#	ESPI FLASH SHARING MODE STRAP 0: DISABLE (DEFAULT) 1: SLAVE ATTACHED FLASH SHARING	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	JTAG ODT DISABLE STRAP(DFX) 0: DISABLE 1: ENABLE(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_MOSI	BOOT HALF STRAP(DFX) 0: ENABLE 1: DISABLE (PCH INT PULL-UP)(DEFAULT)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_I02	CONSENT STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
SPI0_I03	PERSONALITY STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

GPIO Group	GPIO	SIO PIN#	In/Out	PWR well	Signal PIN	External PU / PD
GPIO-0	00	3				
	01	4	Native		SIO_LED	
	02	121	Native		HDD_FAN_PWM_SIO	+3V3
	03	122	Native		HDD_FAN_TACH_SIO	+3V3
05	96					
GPIO-1	10	18	Native		LPC_DRQ0#	PU 10K to SIO_3VCC
	11	27	?		A20GATE	
	12	28	Native		KBRST#	
	13	55				
GPIO-2	20	29	Native		CTS1-	
	21	30	Native		DSR1-	
	22	31	Native		RTS1-	
	23	32	Native		DTR1-	
	24	33	Native		SIN1-	
	25	34	Native		SOUT1-	
	26	35	Native		DCD1-	
	27	36	Native		SIO_RIA	
GPIO-3	30	38			NC	
	31	39			NC	
	32	40			NC	
	33	41			NC	
	34	42			NC	
	35	43			NC	
	36	44			NC	
GPIO-4	37	45	GPIO		H_PROC_SELECT#(NI)	PU 4.7K to SIO_SB3V(NI)
	40	47	GPIO		2543_P2_EN	PU 100K to +5V_S5(NI)
	41	48	GPIO		2543_CLT3(NI)	PU 100K to +5V_S5
	42	49	GPIO		2543_EN	
	43	50	GPIO		2543_CLT1	
	44	51	GPIO		OVERLOAD_N	PU 10K to +5V_S5
	45	52	??		ADP_ID0	
	46	53	??		ADP_ID1	
GPIO-5	50	7	Native		CTS2-	
	51	8	Native		DSR2-	
	52	9	Native		RTS2-	
	53	10	Native		DTR2-	
	54	11	Native		SIN2-	
	55	12	Native		SOUT2-	
	56	13	Native		DCD2-	
	57	14	Native		SIO_RIB	

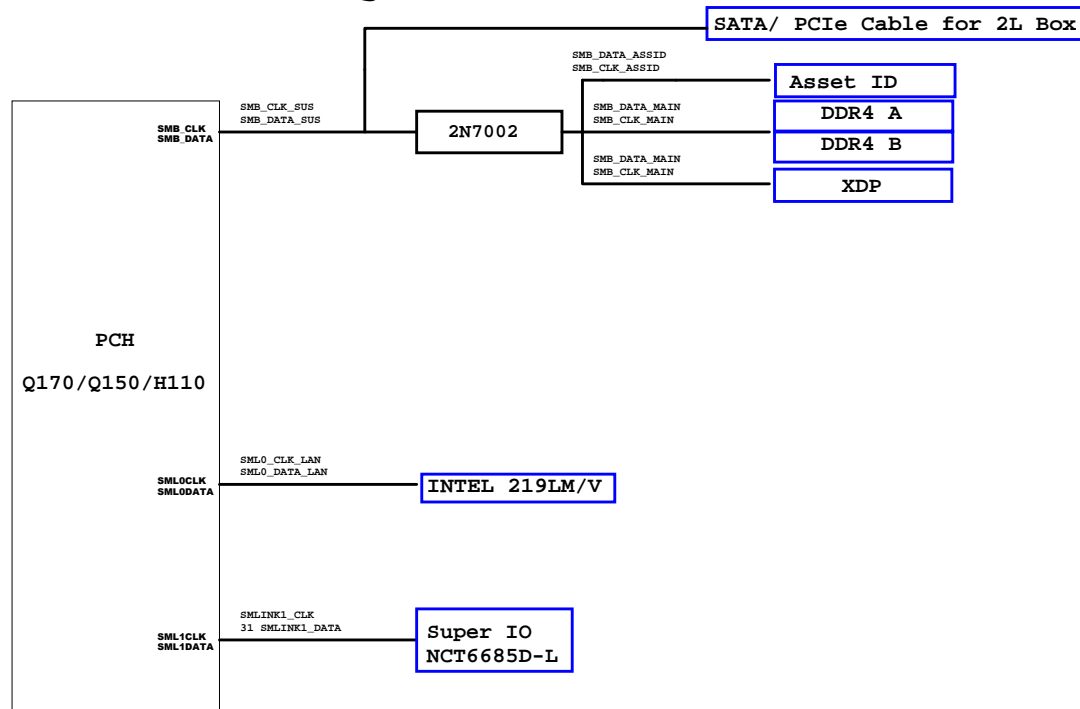
GPIO Group	GPIO	SIO PIN#	In/Out	PWR well	Signal PIN	External PU / PD
GPIO-6	62	76	Native		SMLINK1_DATA	PU 2.2K to +3V3_S5
	63	75	Native		SMLINK1_CLK	PU 2.2K to +3V3_S5
	66	70	GPIO		5V_S5_DISABLE#	PU 10K to +3V3_S5(NI)
	67	100			NC	
GPIO-7	70	95			NC	
	71	98	GPIO		BAT_DET#	PU 4.7K to SIO_SB3V
	72	124	GPIO		PWR_PROTECT#	PU 10K to +3V3
	73	125	GPIO		PWR_THROTTLE#	PU 10K to SIO_SB3V
	74	37			NC	
	75	128	Native		SMB_BAT_CLK	PU 4.7K to SIO_SB3V(NI)
	76	123	Native		SMB_BAT_DAT	PU 4.7K to SIO_SB3V(NI)
	77	102			GPIO77	PD 4.7K
GPIO-8	80	15			NC	
	81	126	Native		CHASSIS_FAN_PWM_SIO	+3V3
	82	127	Native		CHASSIS_FAN_TACH_SIO	+3V3
	83	103			GPIO83	PD 4.7K
	84	104			TINY_ID	PD 4.7K
GPIO-9	85	2	GPIO		SIO_SCI#	PU 10K to +3V3
	90	93	Native		SUSWARN#(NI)	PU 10K to +3V3_S5(NI)
	91	90			NC	
	92	91	Native		SUSACK#(NI)	PU 10K to +3V3_S5(NI)
	93	89	Native		SLP_SUS#(NI)	PU 4.7K to SIO_SB3V
GPIO-EN0	94	88			RING#	PU 4.7K to SIO_SB3V(NI)
	95	74	GPIO		ME_CNTL	
	00	63	Native		PSON#(NI)	PU 4.7K to SIO_SB3V
	01	64	Native		SLP_S3#	
	02	65	?		SIO_PME#	PU 4.7K to SIO_SB3V(NI)
	03	60			PWRBTN_OUT_SIO#	PU 4.7K to SIO_SB3V
	04	61	GPIO		PWRBTN#(NI)	PU 4.7K to SIO_SB3V
	05	83	GPIO		RESETCON#	PU 4.7K to SIO_3VCC
GPIO-EN1	06	84	Native		SLP_S4#	
	07	71	GPIO		DP_ESIO(NI)	PU 4.7K to SIO_SB3V
	10	80	GPIO		PWRGD_PS	PU 4.7K to SIO_3VCC
	11	79			NC	
	12	78	Native		I2C_DATA_G	PU 2.7K to SIO_SB3V
	13	77	Native		I2C_CLK_G	PU 2.7K to SIO_SB3V
	14	81	GPIO		SIO_PWROK0	PU 4.7K to SIO_3VCC
GPIO-EN1	15	82	GPIO		PCH_SYSPWROK	PU 4.7K to SIO_3VCC
	16	73	GPIO		PCH_DPWROK(NI)	PU 2.7K to SIO_SB3V
	17	101	Native		RSMRST_SIO#	PU 4.7K to SIO_SB3V

CLOCK DIAGRAM

RESET MAP




SMBUS Block Diagram



X03

- (1) Add P25,P26 ADD De-Pop noise circuit.
- (2) P10,V_SA1_DIMM0_CHA & V_SA0_DIMM0_CHA add 0ohm to GND
- (3) P74 PCIE X8 swap pin
- (4) P14,combine CLS_COMS & ME DIS 2*5 Header, P19 S_RTCRST# header change 1*2 to NI
- (5) Power:
 - P52:
 - SR2072 => 1.69K
 - SR1753 => 31.6K
 - SR2083 => 1.54K
 - SR2074 => 113K
 - SR2075 BOM
 - SC1482 => 2200pF (0603)
 - SC1483 => 68pF
 - SC1489 => NI
 - SC1490 =>2200pF
 - P54:
 - Botton MLCC => I
 - P58:
 - SR41 => 8.2K
 - P59:
 - SR2041 => 3.4K
- (6) P37, Del C3000,C95,C104
P38, Del SC151,SC152,SC153
- X03 0712**
- (7) P16, ADD R8,R9,R11,R15 0ohm for DCL2.7
P30 ADD SR5 L_LAN_DISABLE# AND ADD SR4 PD to GND for DCL2.7
- (8) P47, H33,H34 Symbol change
- (9) P39, Debug header symbol from 2*9 cjchange to 2*6
- (10) P28,F15 symbol change to1206 size
- (11) P52, SR2060 RENAME TO R24
- (12) P42, PCIEX8 MLCC change to X7R
- (13) USB3.0 connector Housing Color change to BLACK
- X03 0713**
- (14) P10,P11 add C2 ,C13 for DDR4_RST have monotonic at power down
- (15) P26 Q7,Q8,SQ6,SQ8 change to symbol
- (16) P40, J68 2*17 header change to 2*12 header

LITE-ON TECHNOLOGY CORP.			
Title			
67. Change List			
Size	Document Number	Rev	
C	JC113	X03	
Date:	Friday, August 26, 2016	Sheet	67 of 67