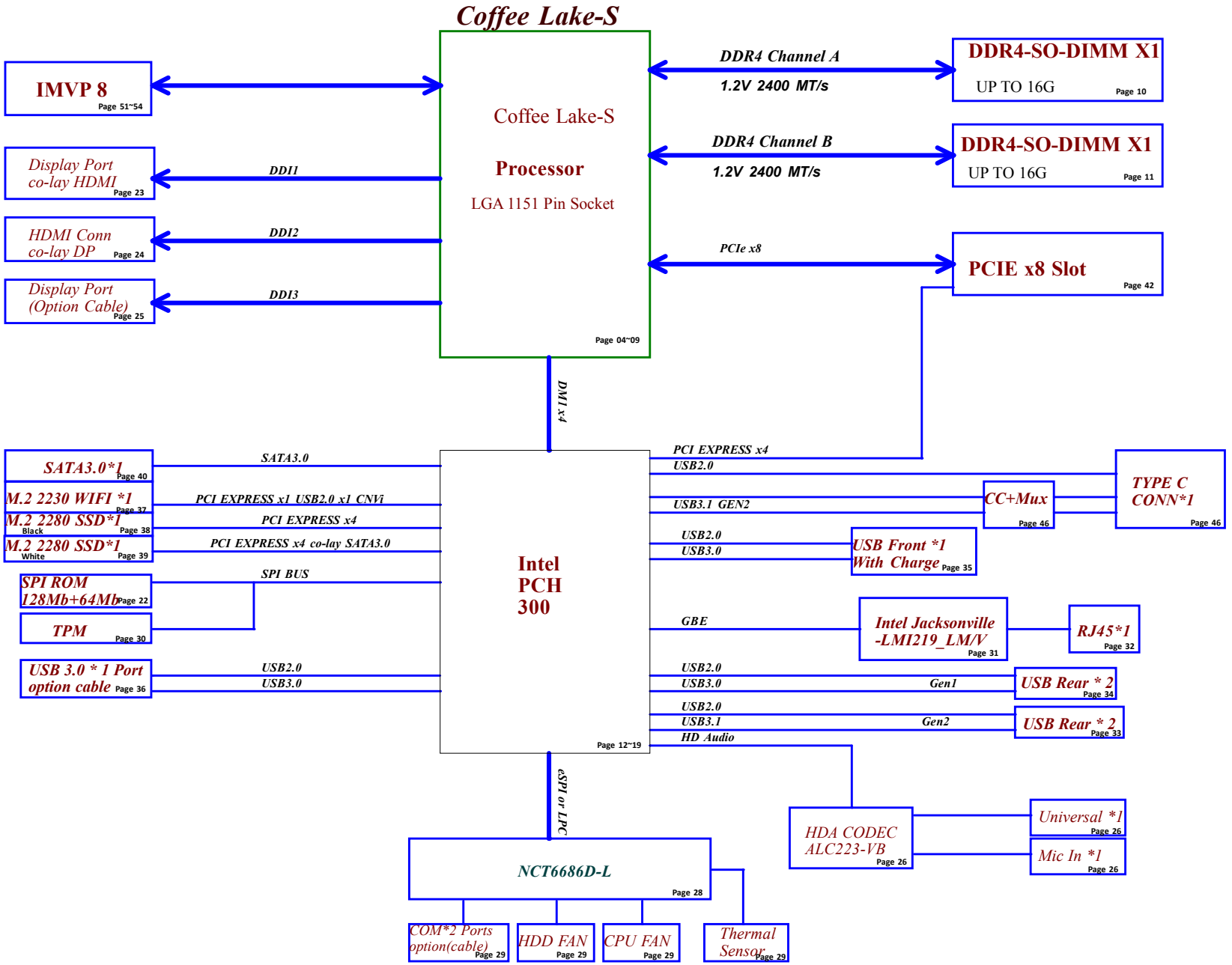
LCFC Confidential

coffee lake MB Schematics Document

2018-01-05

REV:0.7

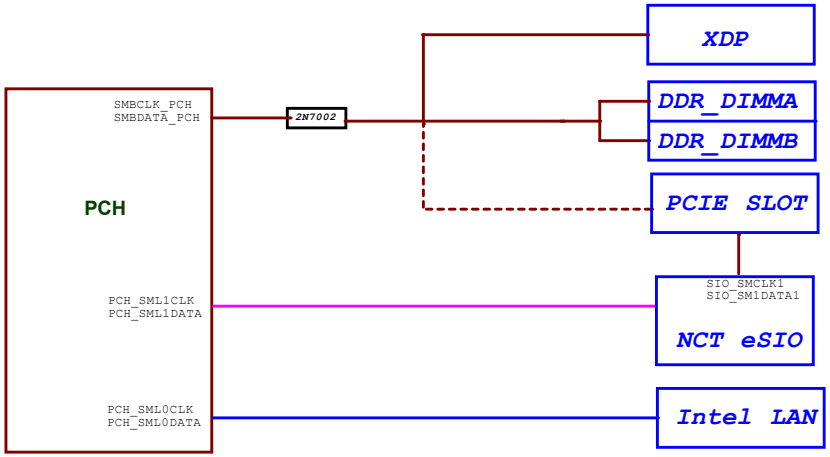
Title	Cover Page	
Size: D	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 1 of 62	



Security Classification	LC Future Center Secret Data		
Issued Date	2017/05/03	Deciphered Date	2018/06/31

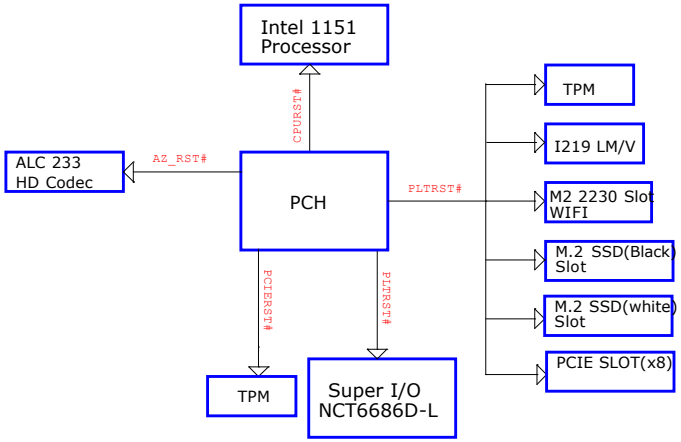
Title	BLOCK DIAGRAM		
Size C	Document Number		Rev 0.7
	Tiny5		
Date:	Friday, January 05, 2018	Sheet 2 of 62	

SMBUS Block Diagram

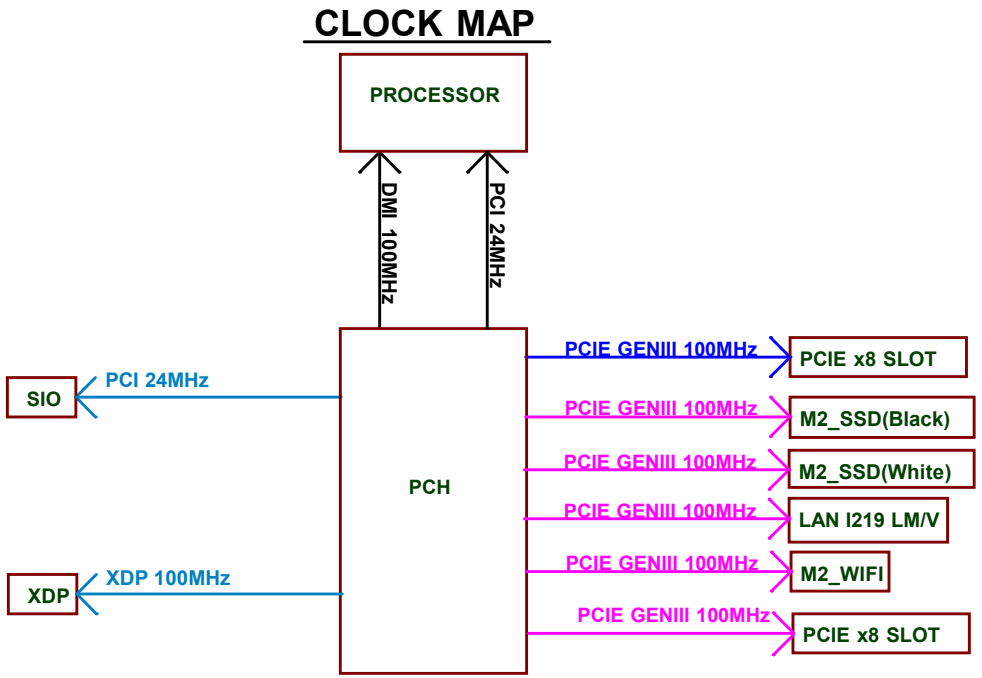


BOM Structure	BTO Item
@	Not stuff
B360@	For B360 SKU
Q370@	For Q370 SKU(M920X,M920Q,NEC Q370), contain USB internal port, 8M SPI ROM
CNVI@	For CNVi part
DIP@	For DIP part
DP1@	For 1st DP colay HDMI port, DP SKU part
DP2@	For 2nd DP colay HDMI port, DP SKU part
HDMI1@	For 1st DP colay HDMI port, HDMI SKU part
HDMI2@	For 2nd DP colay HDMI port, HDMI SKU part
EMC@	For EMC part
EMC_NS@	For EMC nu-stuff part
ESPI@	For eSPI feature part
HD_FAN@	For HDD FAN part,only M920X(Q370) need
LPC@	For LPC(default) part
SSD2@	For M.2 SSD(Black) PCIE part, only M920X(Q370) need
MSATA@	For M.2 SSD(Black) SATA part, only M920X(Q370) need
SSD2PWR@	For M.2 SSD(Black) POWER(Both PCIE and SATA need) part, only M920X(Q370) need
ME@	For ME part
RTD3@	For RTD3 control part
XDP@	For XDP
HD_FAN@	For HDD sensor and FAN
M2_EXP@	For M.2 expand function

RESET MAP



CLOCK MAP

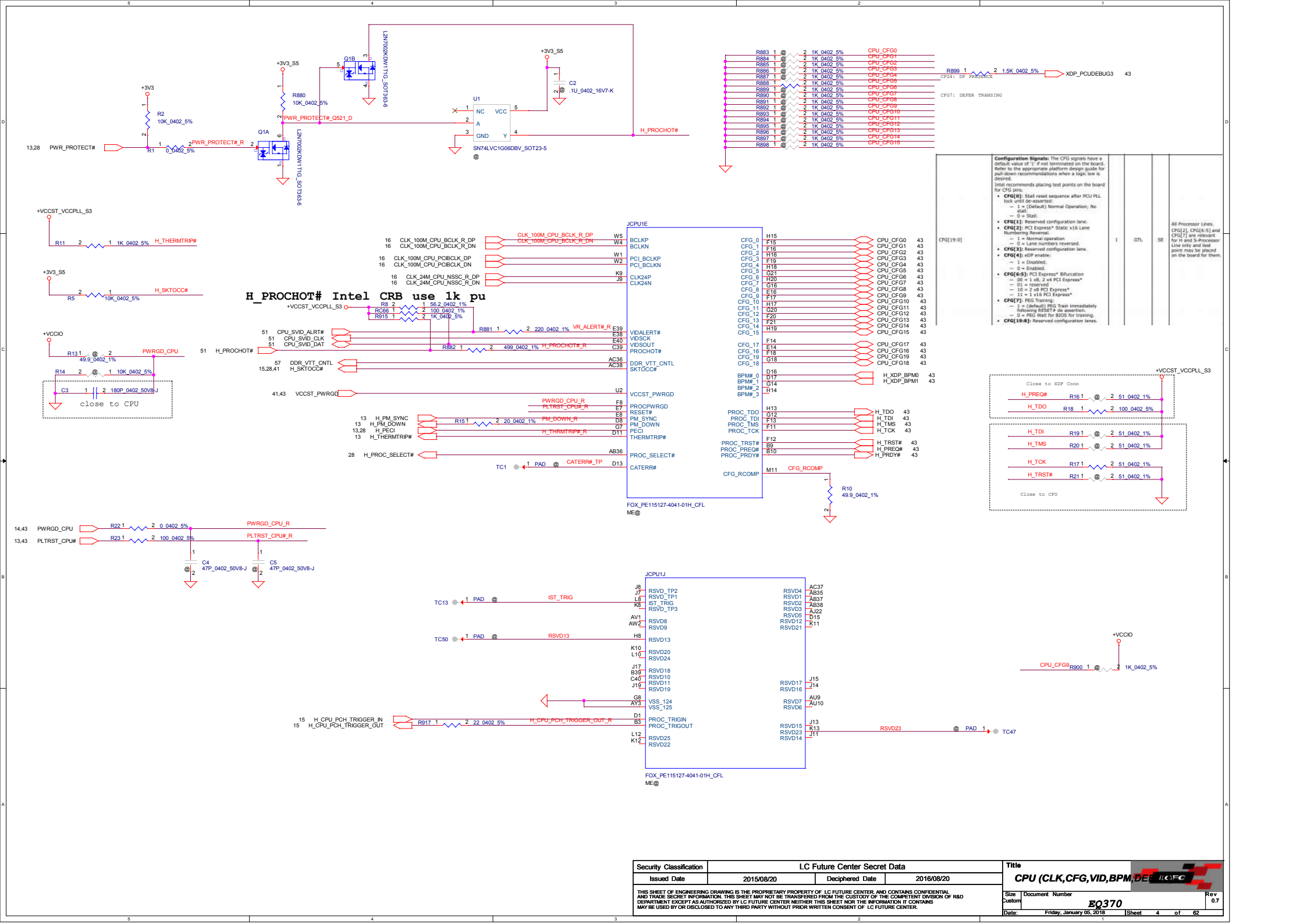


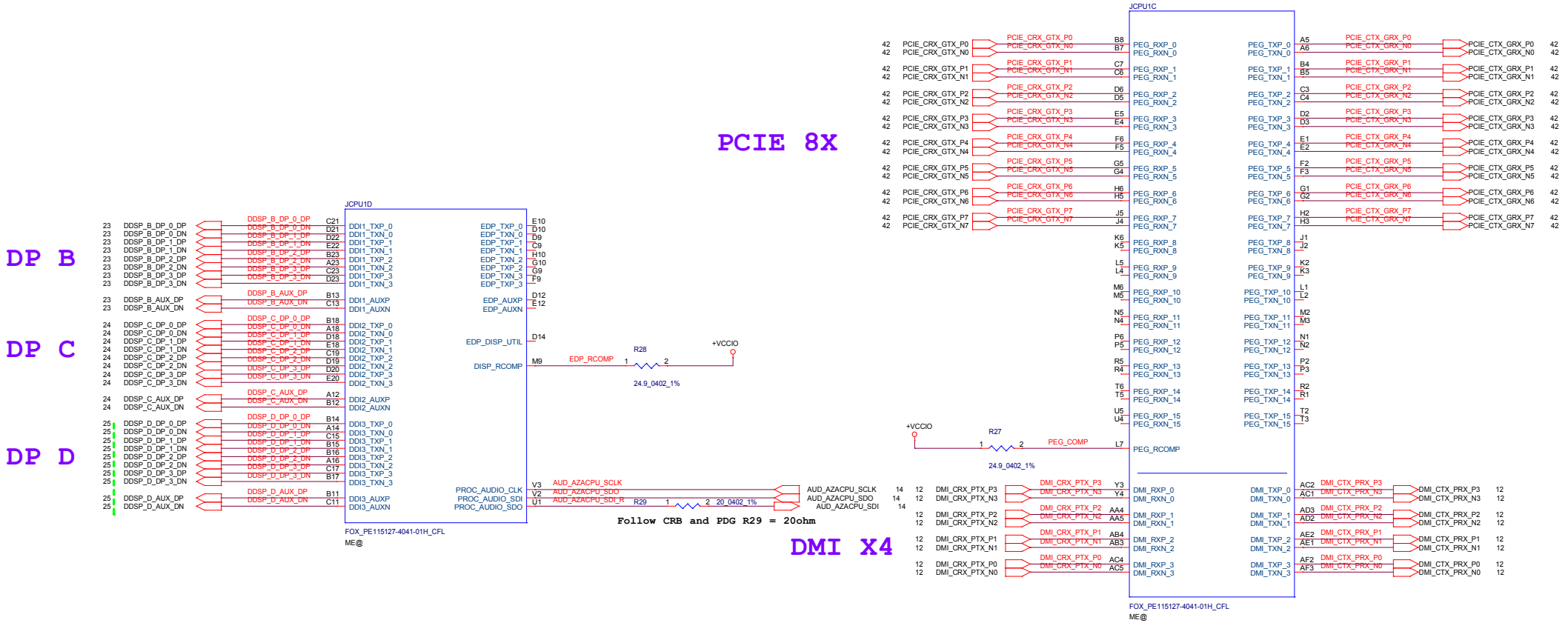
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Notes List**

Size	Document Number	Rev
Custom	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 3 of 62


H_PROCHOT# Intel CRB use 1k pu
JCPU1E
JCPU1J
close to CPU
Close to XDP Conn
Close to CPU
FOX_PE115127-4041-01H_CFL
ME@
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
CPU (CLK,CFG,VID,BPM,DEF
Size
Custom
Document Number
EQ370
Rev
0.7
Date:
Friday, January 05, 2018
Sheet
4
of
62



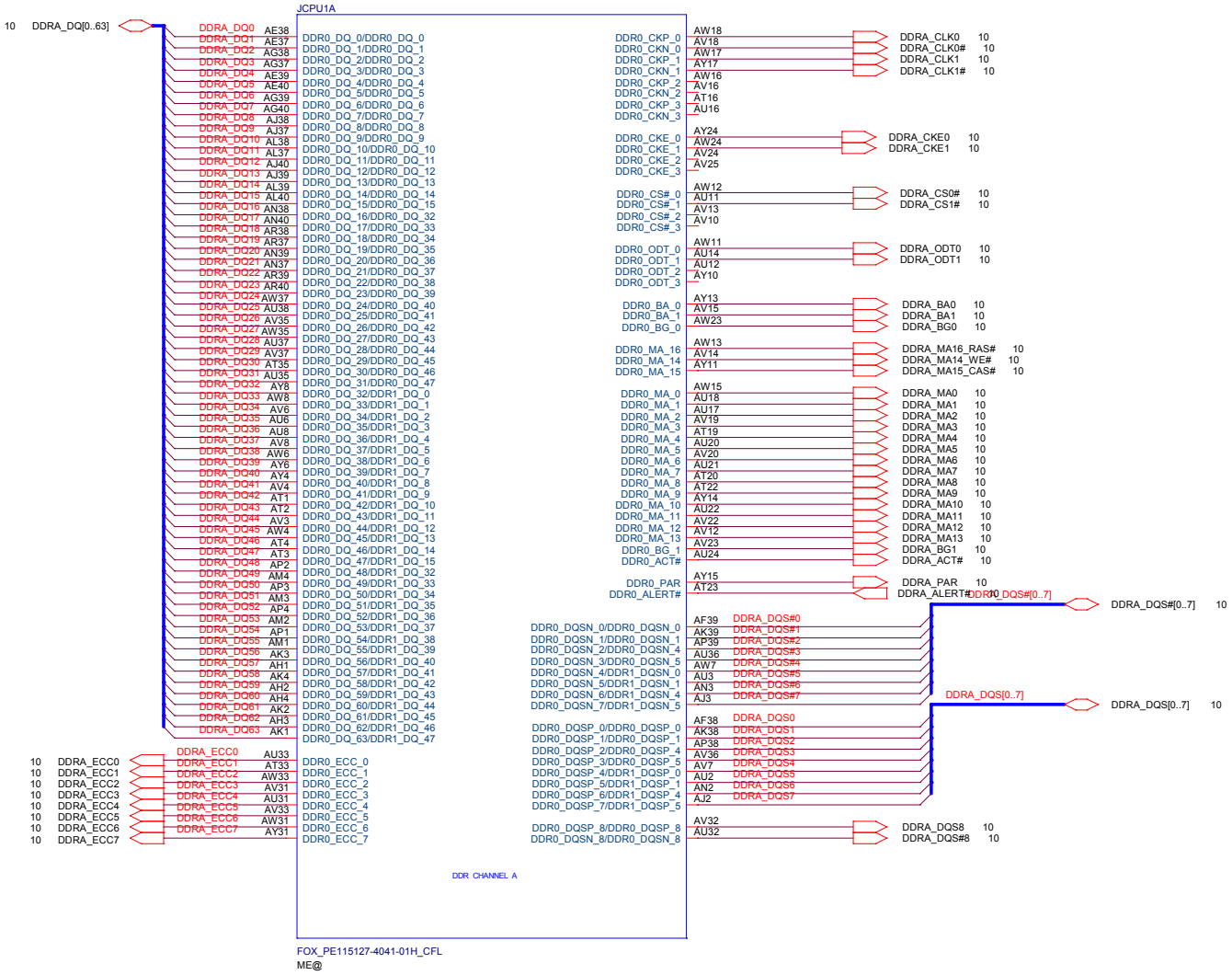
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CPU (PEG,DMI,DDI,EDP)

Size	Document Number	Rev
Custom	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 5 of 62

SO-DIMM DDR4 CHA

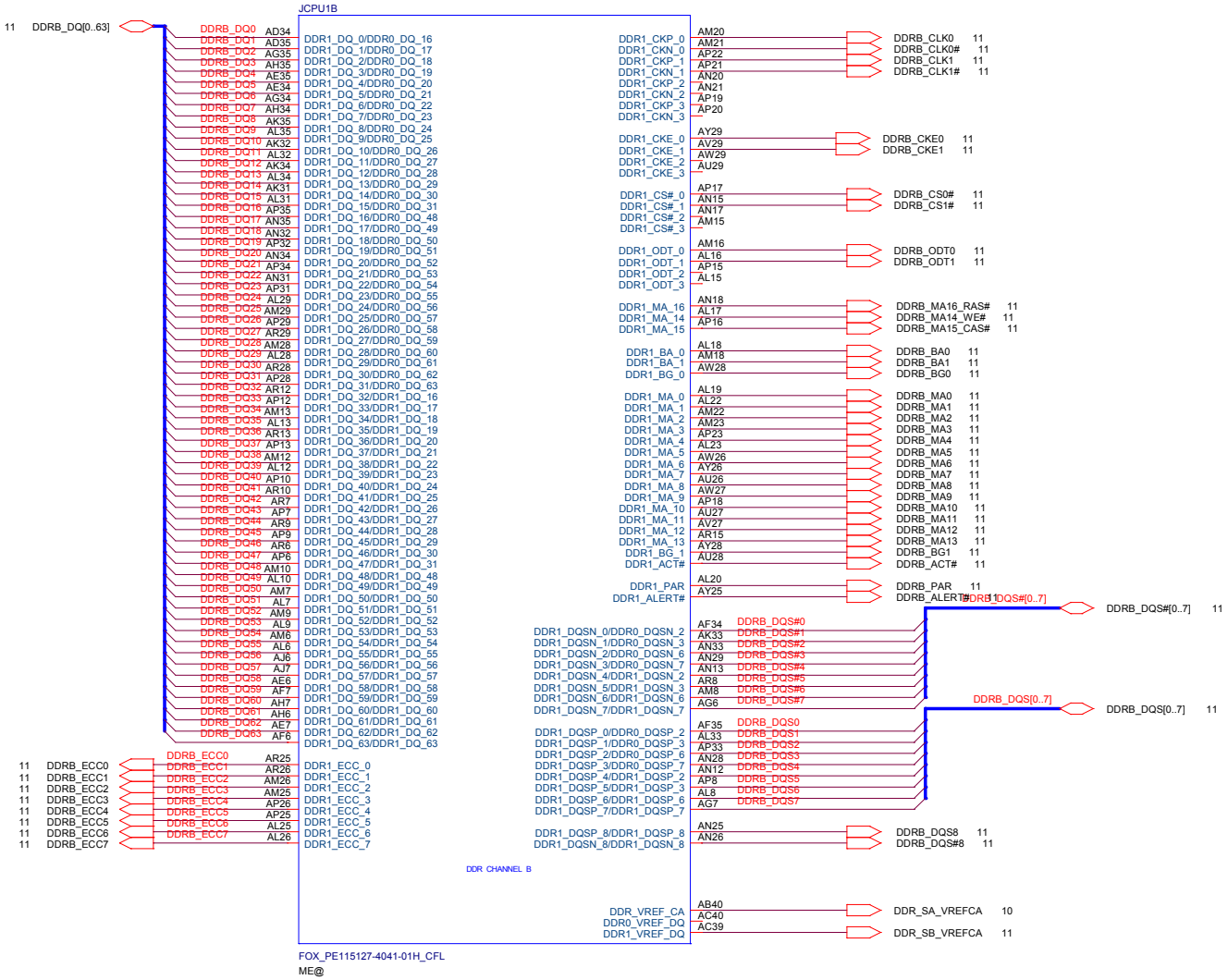


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CPU (DDR4)

Size: Custom	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 6 of 62	

SO-DIMM DDR4 CHB



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CPU (DDR4)

Size: Custom	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 7 of 62	

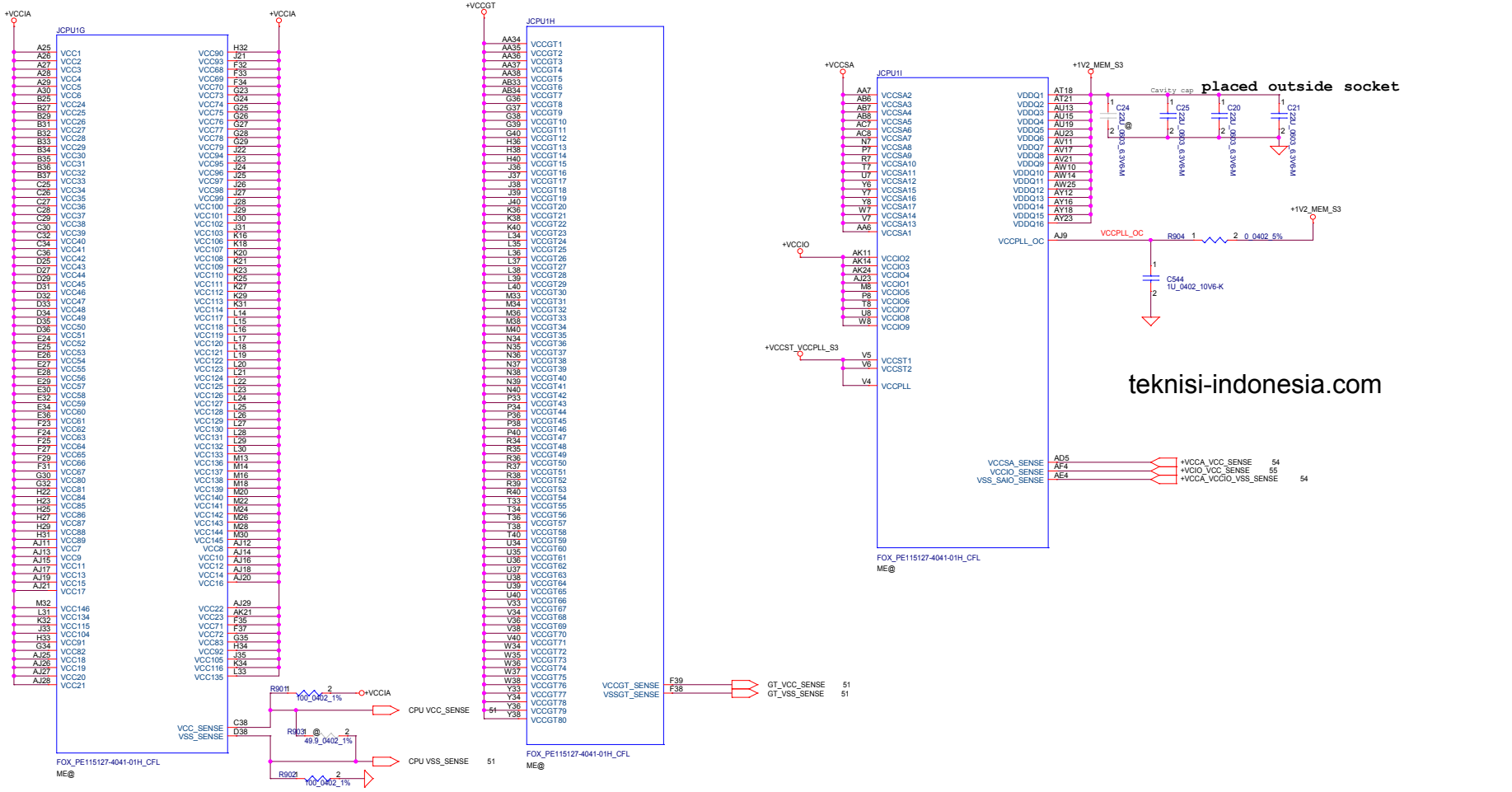


Table 50-3. Decoupling Requirements for CFL S Processor

Domain	Cavity cap	Outside socket cap	Topside/ Bottom side	Placement guideline and notes
Vcc	12x 22uF 0805		Top	
	6x 22uF 0603		Top	
		5x 22uF 0805	Top	
Vcc_{GT}	8x 47uF 0805		Top	
		4x 47uF 0805	Top	
Vcc_{SA}	4x 22uF 0603		Top	
		2x 22uF 0603	Top	
		4x 47uF 0805	Top	
V_{DDQ}		4x 22uF 0603	Top	
Vcc_{IO}	5x 22uF 0603		Top	
	1x 22uF 0805		Top	
Vcc_{ST}	1x 22uF 0805		Top	Merged with VccPLL; VccST and Vcc5TG merged on package. Capacitors placed as close to package as possible
	1x 1uF 0402		Top	
Vcc_{PLL_OC}	1x 1uF 0402		Top	

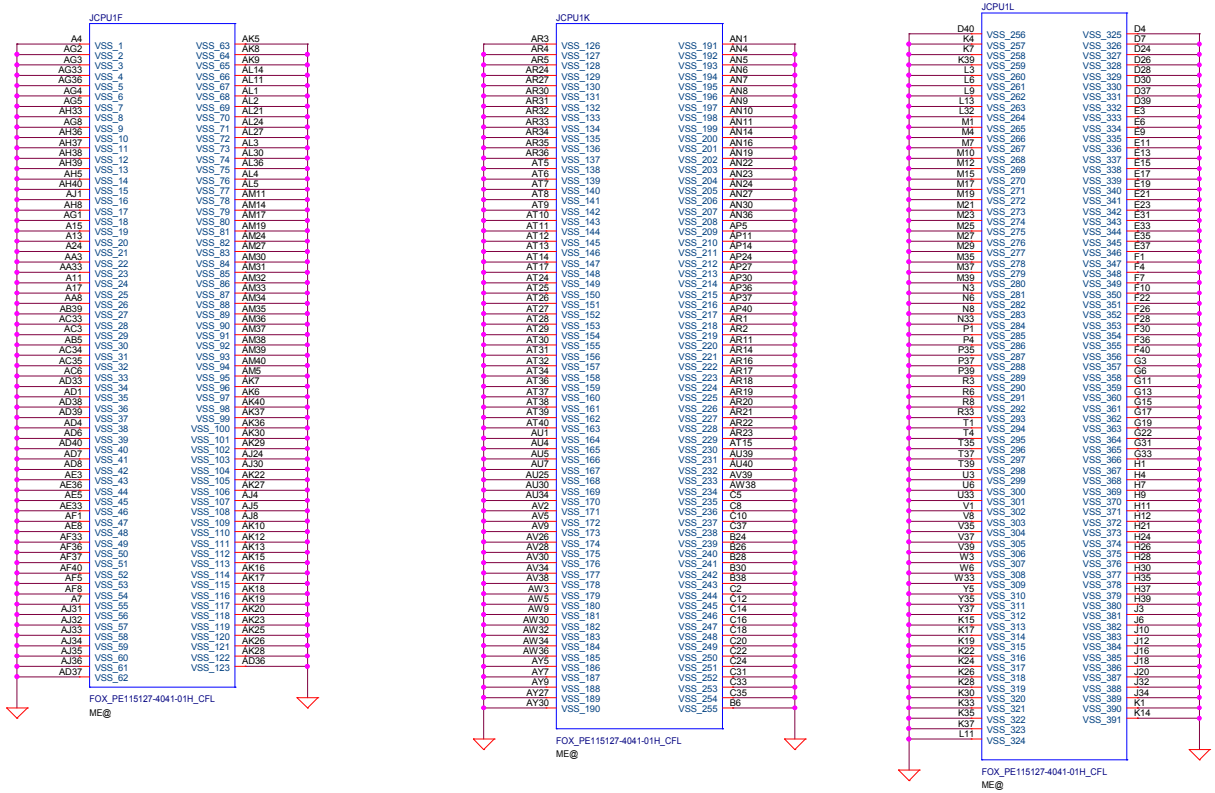
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: **COU(CPU POWER)**

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 | Sheet 8 of 62

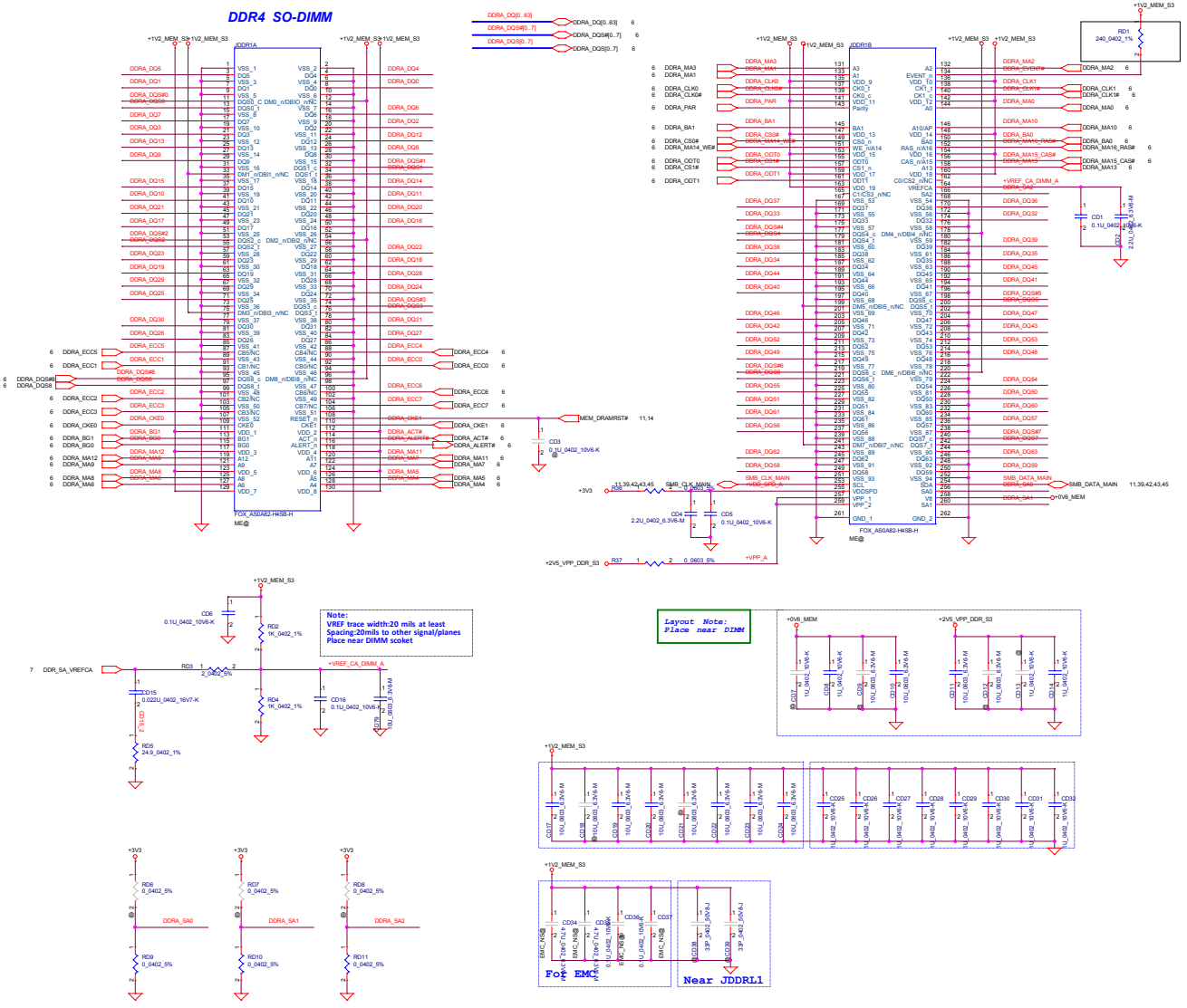


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: CPU(VSS)

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 | Sheet 9 of 62



Need check SPD address

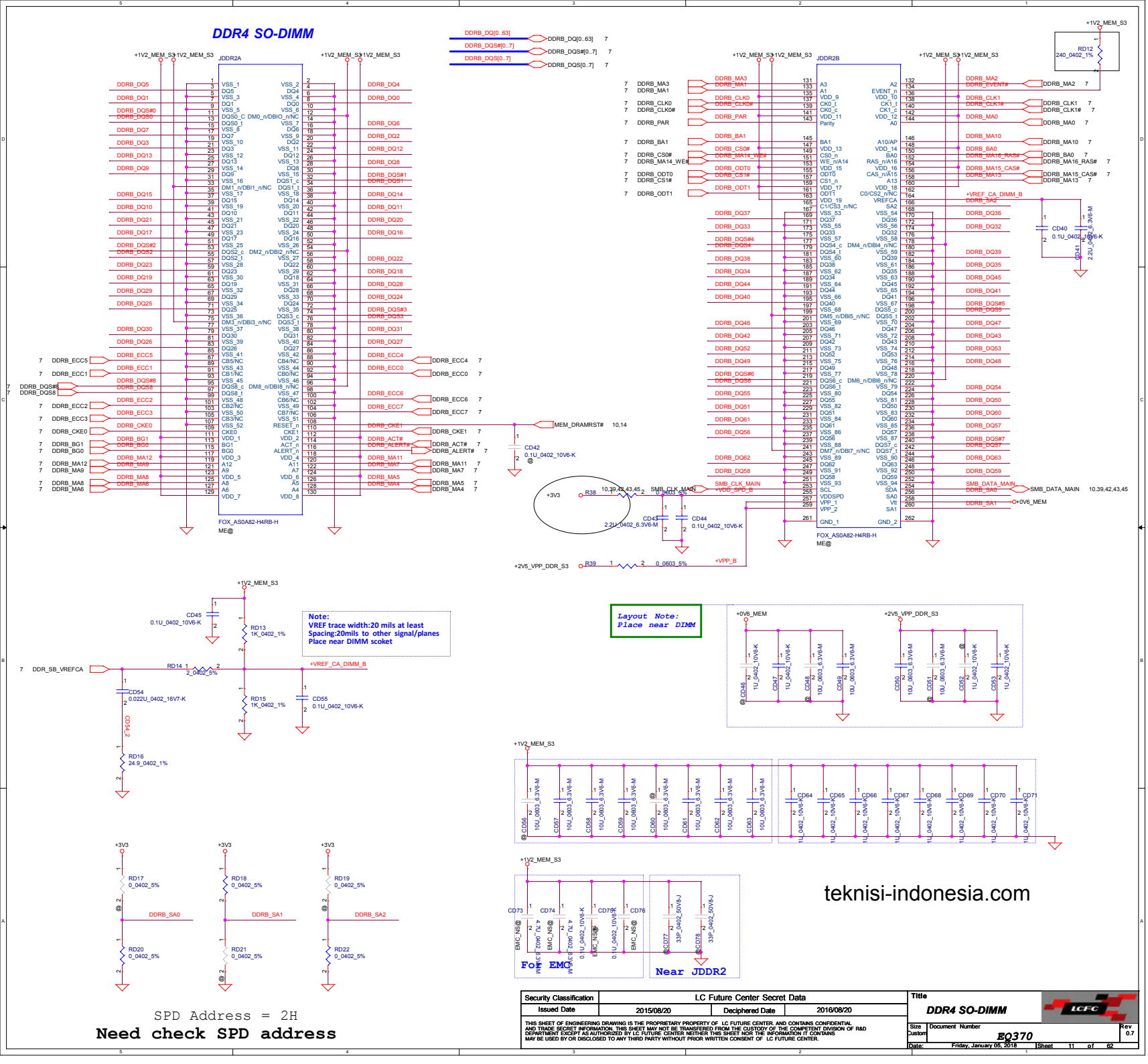
SPD Address = 0H

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	DDR4 SODIMM		
Size	Document Number		Rev
Custom	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet 10 of 62	

DDR4 SO-DIMM

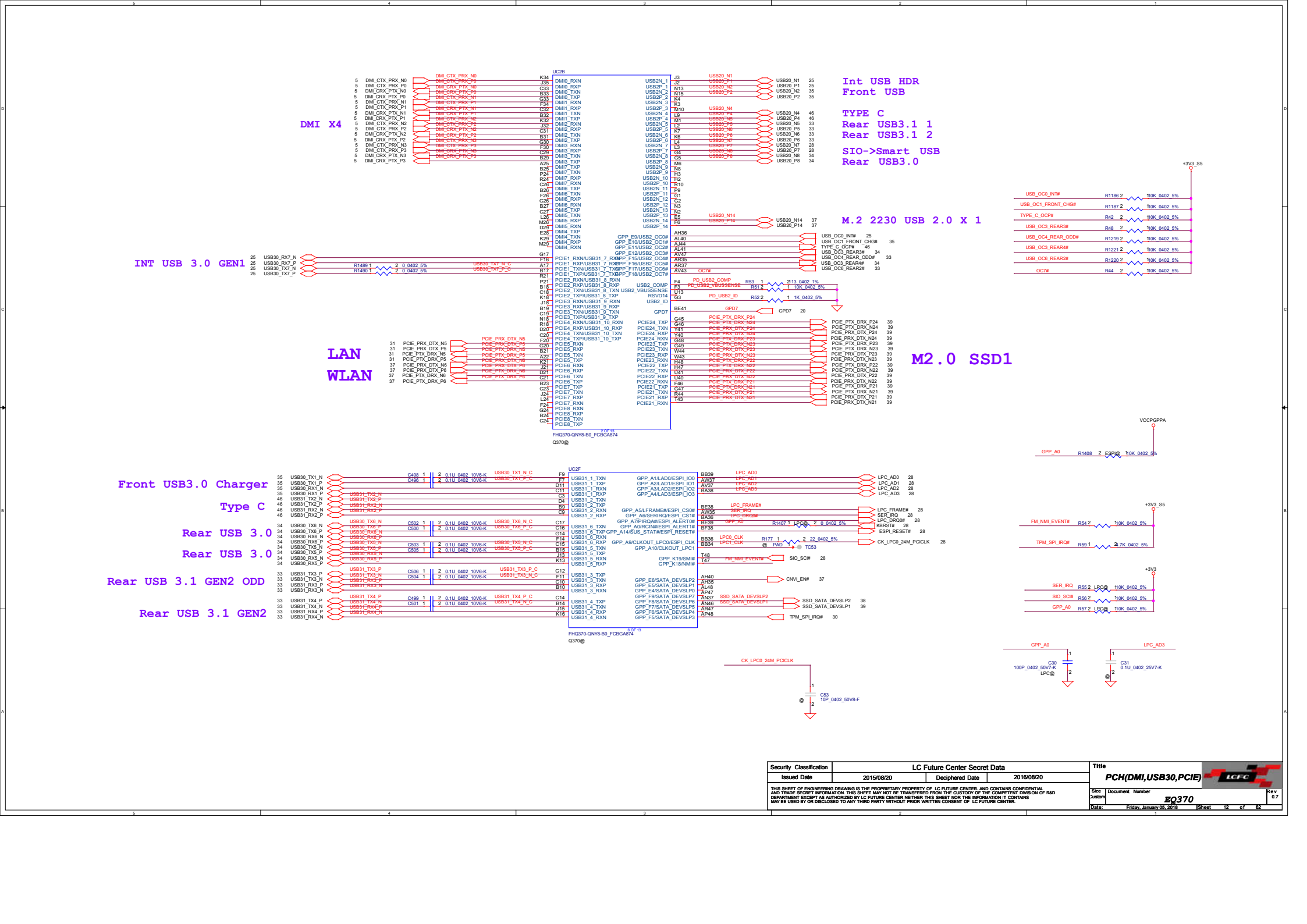


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: DDR4 SO-DIMM

Size	Document Number	Rev
Custom	EQ370	0.7
Date: Friday, January 05, 2018	Sheet 11 of 62	


DMI X4
INT USB 3.0 GEN1
LAN
WLAN
Front USB3.0 Charger
Type C
Rear USB 3.0
Rear USB 3.0
Rear USB 3.1 GEN2 ODD
Rear USB 3.1 GEN2
Int USB HDR
Front USB
TYPE C
Rear USB3.1 1
Rear USB3.1 2
SIO->Smart USB
Rear USB3.0
M.2 2230 USB 2.0 X 1
M2.0 SSD1
UC2B
FHQ370-QNY8-B0_FCBGA874
Q370@
UC2F
FHQ370-QNY8-B0_FCBGA874
Q370@
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
PCH(DMI,USB30,PCIE)
Size
Custom
Document Number
EQ370
Rev
0.7
Date:
Friday, January 05, 2018
Sheet
12
of
82

ID5	ID4	ID3	ID2	ID1	ID0	SKU
1	1	0	0	0	0	Q370 Tiny 65W(M920X)
1	1	0	0	0	1	Q370 Tiny 35W(M920Q)
1	1	0	0	1	0	B360 Tiny 35W(M720Q)
1	1	0	0	1	1	NEC Q370 Tiny 35W (M920q)
1	1	0	1	0	0	NEC B360 Tiny 35W (M720q)
1	1	0	1	0	1	Q370 Tiny 65W(P330)

SATA FFC Cable

PCIEX4 for SLOT

M.2_2280_SSD#2 Black

PCIEX4 for SLOT

PCIEX4 for SLOT

PCIEX4 for SLOT

M.2_2280_SSD#2 Black

Figure 3-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GbE				GbE		SATA 0a	GbE	GbE	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5						
																		SATA 1a	SATA 0b											
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

Desktop PCH HSIO Details (Sheet 1 of 2)

Flex I/O Lane	SKU					
	Q370	H370	Z390	Q360	B360	H310
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1
4	USB3.1 Gen1/Gen2	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1	USB3.1 Gen1	N/A
5	USB3.1 Gen1/Gen2	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1	USB3.1 Gen1	N/A
6	USB3.1 Gen1, PCIe*	USB3.1 Gen1	USB3.1 Gen1,PCIe*	USB3.1 Gen1	N/A	N/A
7	USB3.1 Gen1, PCIe*	USB3.1 Gen1	USB3.1 Gen1, PCIe*	USB3.1 Gen1	N/A	N/A
8	USB3.1 Gen1, PCIe*	PCIe*	USB3.1 Gen1, PCIe*	N/A	N/A	N/A
9	USB3.1 Gen1, PCIe*	PCIe*	USB3.1 Gen1, PCIe*	N/A	N/A	N/A
10	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
11	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
12	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
13	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE	GbE
15	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	N/A
16	PCIe*, SATA 0A	PCIe*, SATA 0B	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	GbE, SATA 0
19	PCIe*, SATA 1B	PCIe*, SATA 0B	PCIe*, SATA 1B	PCIe*, SATA 0B	SATA 1B	SATA 1
20	PCIe*, SATA 2	PCIe*, SATA 1	PCIe*, SATA 2	SATA 2	SATA 2	SATA 2

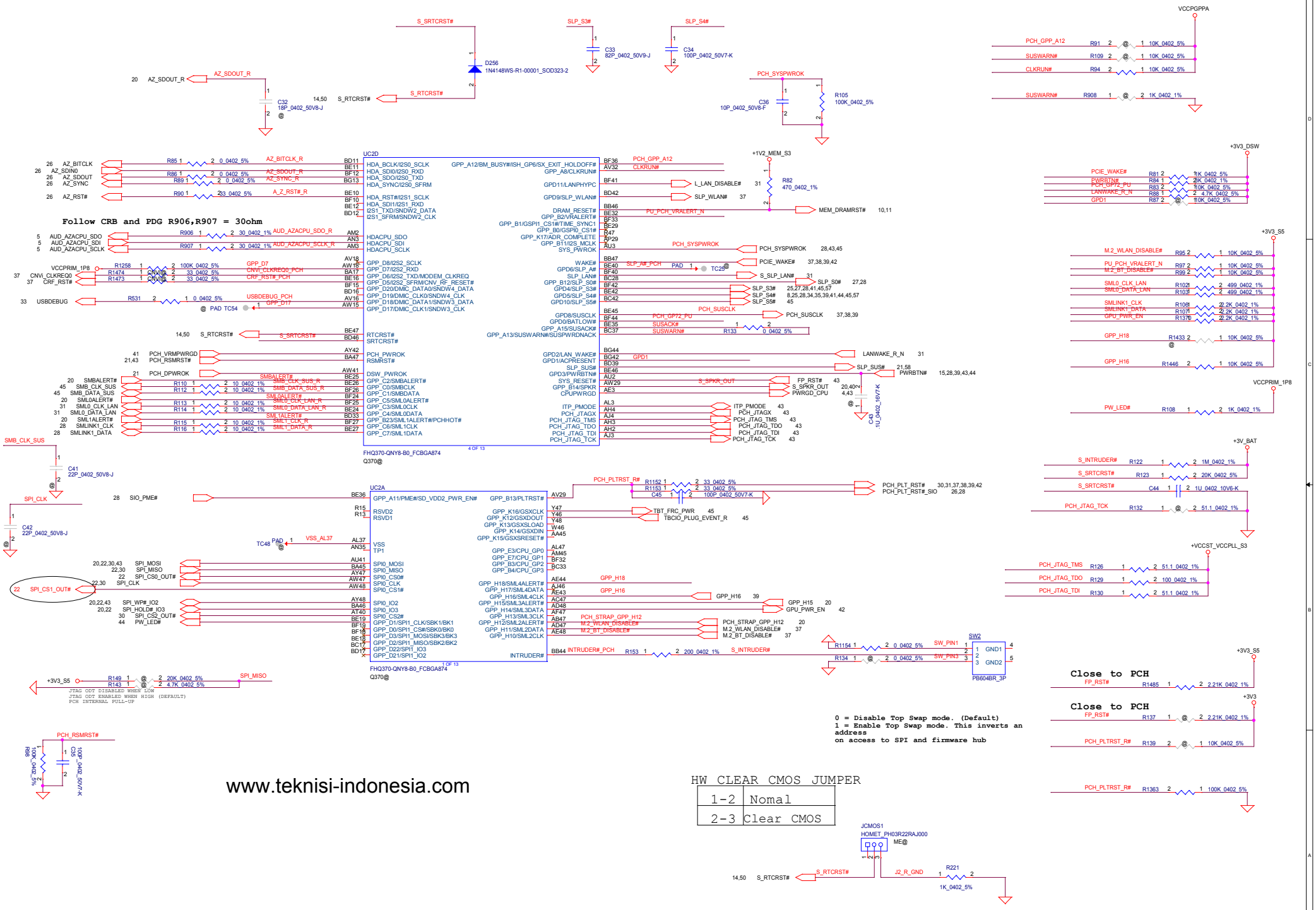
Flex I/O Lane	SKU					
	Q370	H370	Z390	Q360	B360	H310
21	PCIe*, SATA 3	PCIe*, SATA 3	PCIe*, SATA 3	SATA 3	SATA 3	SATA 3
22	PCIe*, SATA 4	SATA 4	PCIe*, SATA 4	SATA 4	SATA 4	N/A
23	PCIe*, SATA 5	SATA 5	PCIe*, SATA 5	SATA 5	SATA 5	N/A
24	PCIe*	PCIe*	PCIe*	N/A	N/A	N/A
25	PCIe*	PCIe*	PCIe*	N/A	N/A	N/A
26	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	N/A
27	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	N/A
28	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	N/A
29	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	N/A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PCH(PCIE,C LINK)

Size	Document Number	Rev
D	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 13 of 62



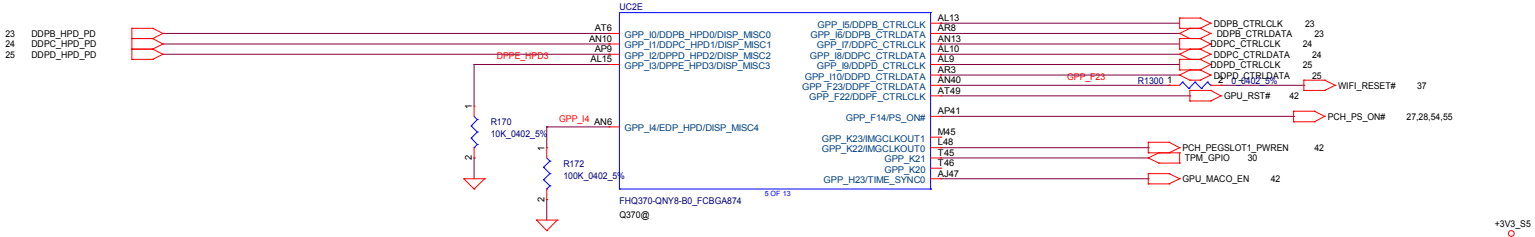
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

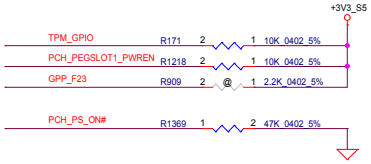
Title: PCH(HDA,JATG,SUMBUS,S

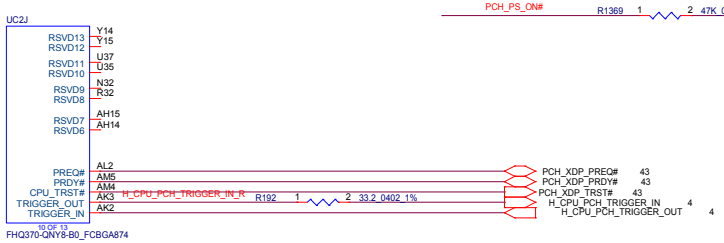
Size	Document Number	Rev
C	EQ370	0.7

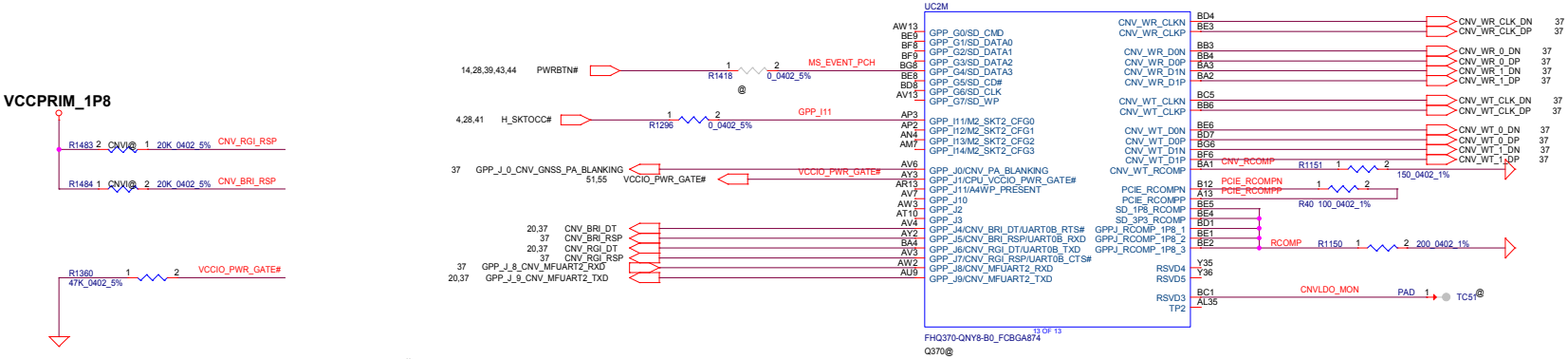
Date: Friday, January 05, 2018 Sheet 14 of 62



Follow CRB GPP_F23 is reserved for WLAN RTD3 reset



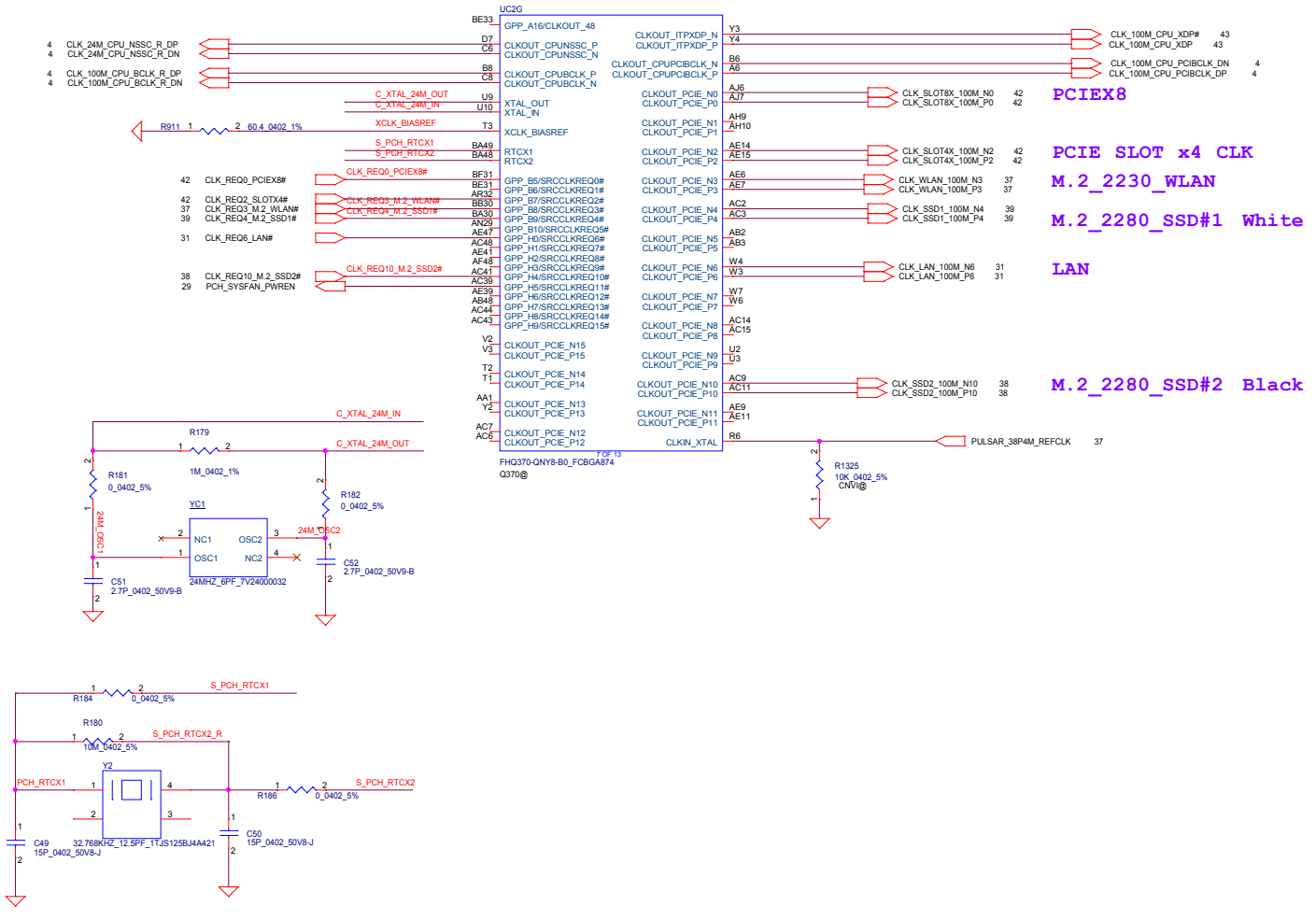




GPP_J9 strap Rising edge of RSMRST#
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail
Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a ' 1' for the proper functionality of the SPI (Flash) I/Os

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PCH(DDP)	
Size: C	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 15 of 62	

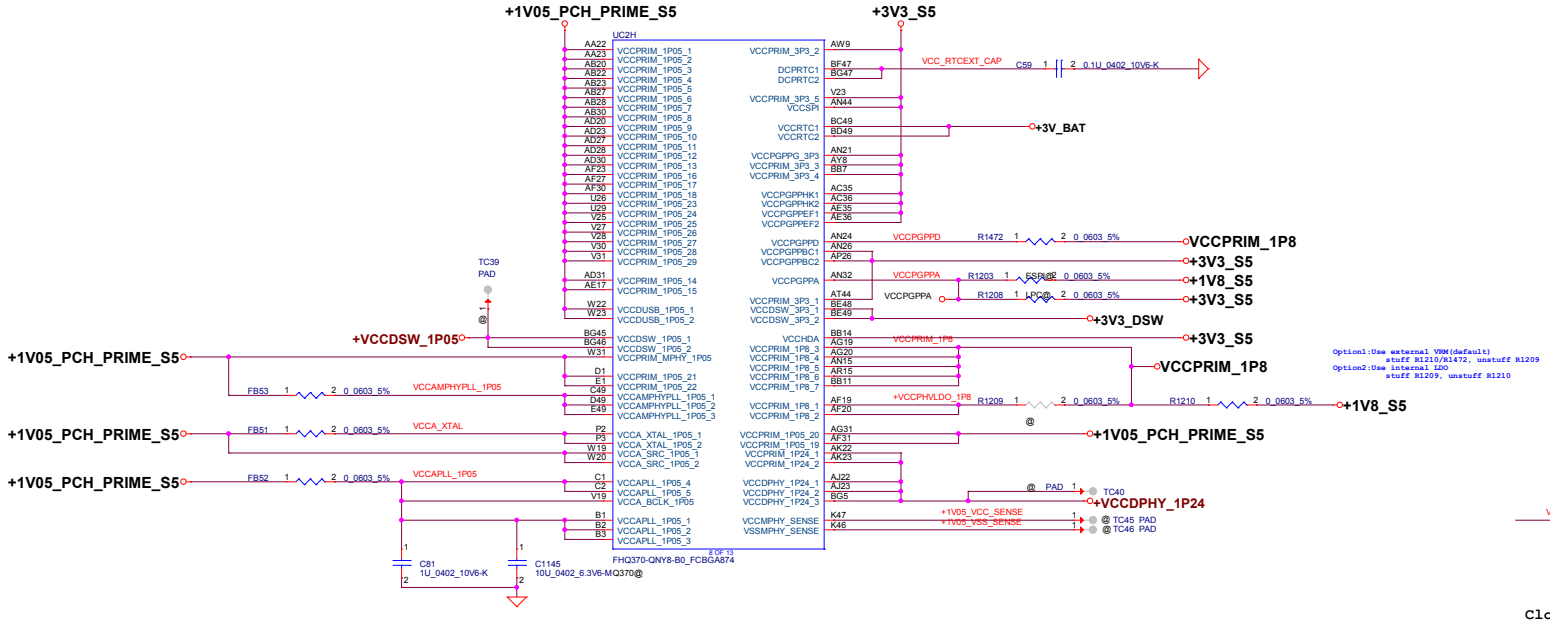


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

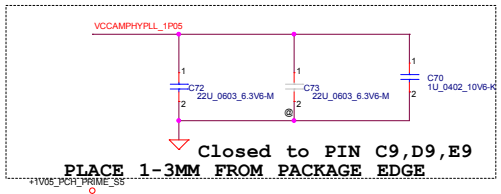
Title: PCH(PCIE CLK,REQ)

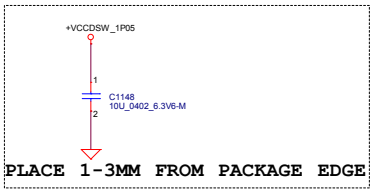
Size	Document Number	Rev
C	EQ370	0.7

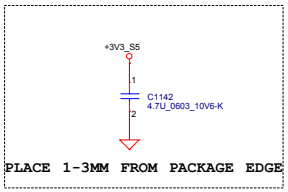
Date: Friday, January 05, 2018 Sheet 16 of 62

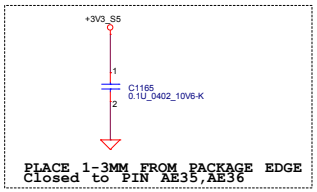


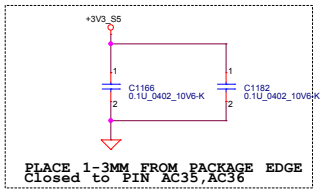
CAP FOLLOW CRB

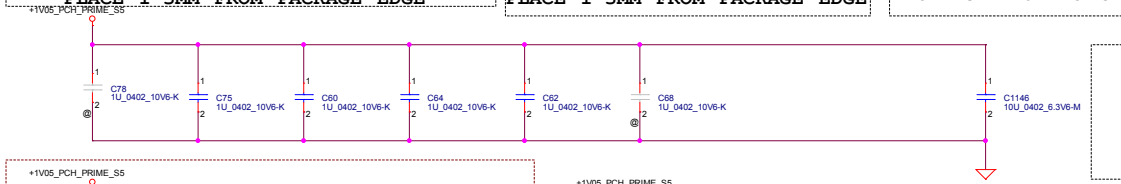


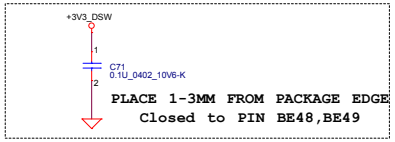


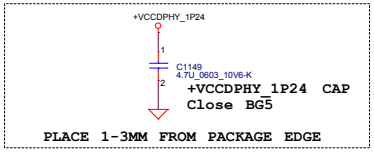


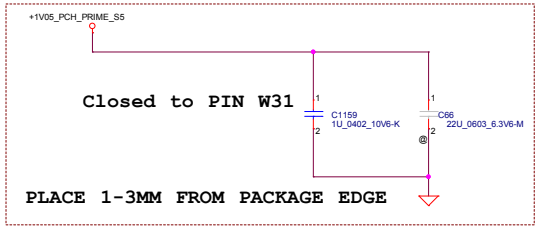


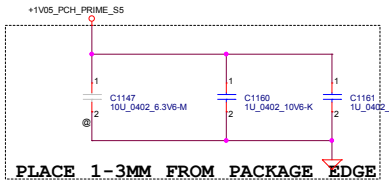


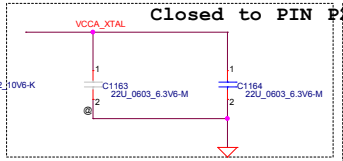


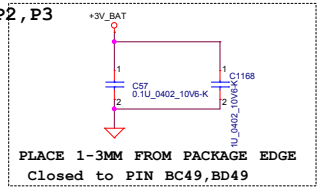


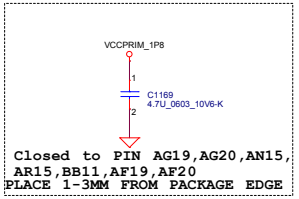












Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PCH(PCH POWER)		
Size	Document Number		Rev
Custom	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet	17 of 62

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PCH(I2C,UART,CPU VSS)

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 18 of 62

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: *PCH(SD,CNV)*

Size	Document Number	Rev
C	*EQ370*	0.7

Date: Friday, January 05, 2018 | Sheet 19 of 62

Rising edge of PCH_PWROK

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode. This inverts an address
on access to SPI and firmware hub

+3V3 — R146 1K_0402_1%

14,40 S_SPKR_OUT — S_SPKR_OUT — R148 1 — 2 20K_0402_5%

Rising edge of PCH_PWROK

REBOOT (INTERNAL PD)

NO REBOOT
0: DISABLE (DEFAULT)
1: ENABLE

+3V3_S5 — R206 4.7K_0402_5%

18 PCH_STRAP_GPP_B18 — R207 1 — 2 1K_0402_5%

Rising edge of PCH_PWROK

BOOT SELECT STRAP
This Signal has a weak internal pull-down.
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI

0 = SPI
1 = LPC

+3V3_S5 — R204 4.7K_0402_5%

18 PCH_STRAP_GPP_B22 — R208 1 — 2 20K_0402_5%

Rising edge of RSMRST#

This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

+3V3_S5 — R155 4.7K_0402_5%

14 SMBALERT# — R156 1 — 2 20K_0402_5%

Rising edge of RSMRST#

This signal has a weak internal pull-down
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

+3V3_S5 — R141 1K_0402_1% ESPI@

14 SML0ALERT# — R145 1 LPC@ — 2 20K_0402_5%

Rising edge of RSMRST#

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V3_S5 — R140 1K_0402_1%

14,22,30,43 SPI_MOSI — R124 1 @ — 2 4.7K_0402_5%

Rising edge of RSMRST#

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V3_S5 — R1259 100K_0402_5%

14 GPP_H15

Rising edge of RSMRST#

GPP_B23 /SML1ALERT# /PCHHOT#
This signal has an internal pull-down.
0 = Disable DCI-OOB
1 = Enable DCI-OOB(Default)

+3V3_S5 — R104 4.7K_0402_5%

14 SML1ALERT#

SPI0_IO2

Rising edge of RSMRST#

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V3_S5 — R136 1K_0402_5%

14,22,43 SPI_WP#_IO2 — SPI_WP#_IO2 — R131 1 @ — 2 4.7K_0402_5%

SPI0_IO3

Rising edge of RSMRST#

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V3_S5 — R161 1K_0402_5%

14,22 SPI_HOLD#_IO3 — R158 2 @ 1 1K_0402_5%

SPI0_IO3

Rising edge of RSMRST#

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY

+3V3_S5

ME_DISABLE — R147 1 — 2 1K_0402_1%

28 ME_CNTL — R144 1 @ — 2 1K_0402_1% — ME_CNTL_R — MMBT3906_SOT23-3 Q1109 — Q1109_C

14 AZ_SDOUT_R — AZ_SDOUT_R — R1234 1 — 2 0_0402_5% — HDA_SDOUT — R1235 1 @ — 2 1K_0402_1%

JP35
ME_DISABLE — 1
HDA_SDOUT — 3
5
1 2
3 4
5 6
R_GND
CLEAR_CMOS# 18
R167 1K_0402_5%
CVILU_CH71062M100-0P
ME@

SW CLEAR CMOS

ME disable header

GPP_H12 /SML2ALERT#

Rising edge of RSMRST#

GPP_H12/SML2ALERT#
This signal has an internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled(Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

+3V3_S5 — R92 4.7K_0402_5%

14 PCH_STRAP_GPP_H12

GPP_J4 /CNV_BRI_DT /UART0_RTS#

Rising edge of RSMRST#

GPP_J4 /CNV_BRI_DT /UART0_RTS# strap Rising edge of RSMRST#
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD
XTAL FREQUENCY SELECTION
1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO

+1V8_S5 — R1251 10K_0402_5%

15,37 CNV_BRI_DT

GPP_J6 /CNV_RGI_DT /UART0_TXD

Rising edge of RSMRST#

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

+1V8_S5 — R1252 20K_0402_5%

15,37 CNV_RGI_DT — R1298 2 @ 1 10K_0402_5%

GPP_J9

Rising edge of RSMRST#

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

+1V8_S5 — R1299 10K_0402_5% @

15,37 GPP_J_9_CNV_MFUART2_TXD — R1256 2 @ 10K_0402_5%

GPD7

Rising edge of DSW_PWROK

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

+3V3_DSW — R1241 1K_0402_5%

12 GPD7

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

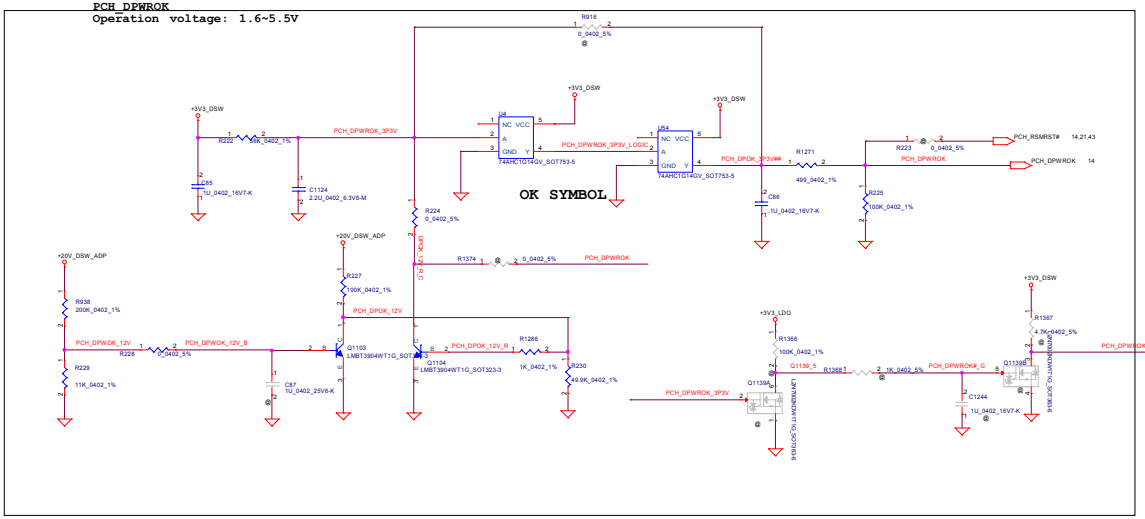
Title: P20-CMOS Clear / HDR

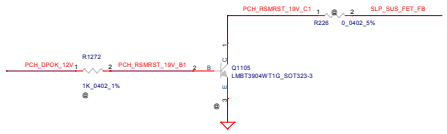
Size	Document Number	Rev
C	EQ370	0.7

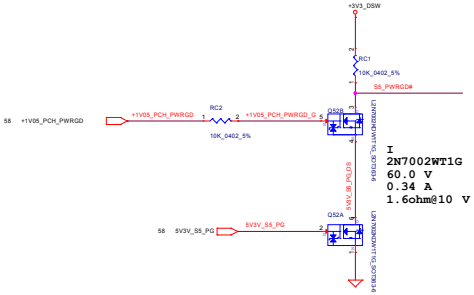
Date: Friday, January 05, 2018 Sheet 20 of 62

PCH_DPWROK

Operation voltage: 1.6~5.5V

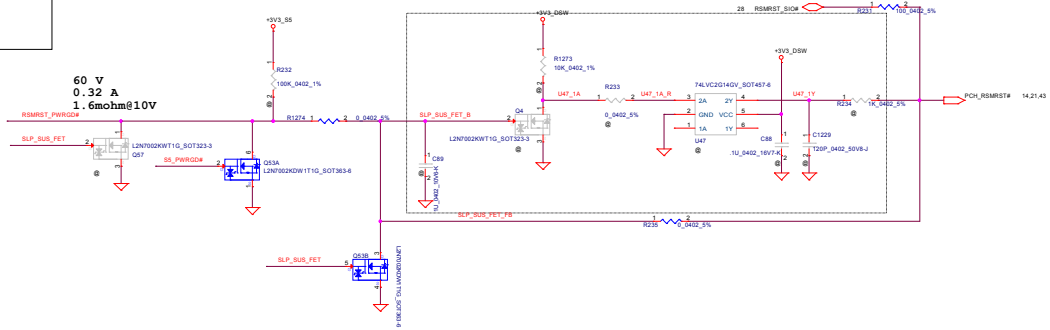




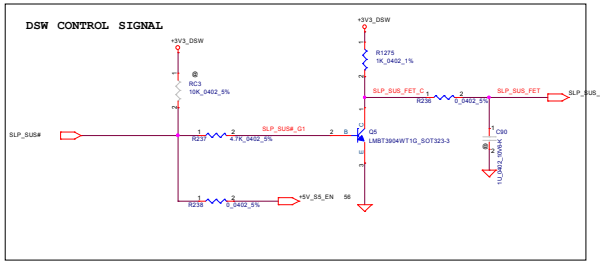


I
2N7002WT1G
60.0 V
0.34 A
1.6ohm@10 V

60 V
0.32 A
1.6mohm@10V



DSW CONTROL SIGNAL



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

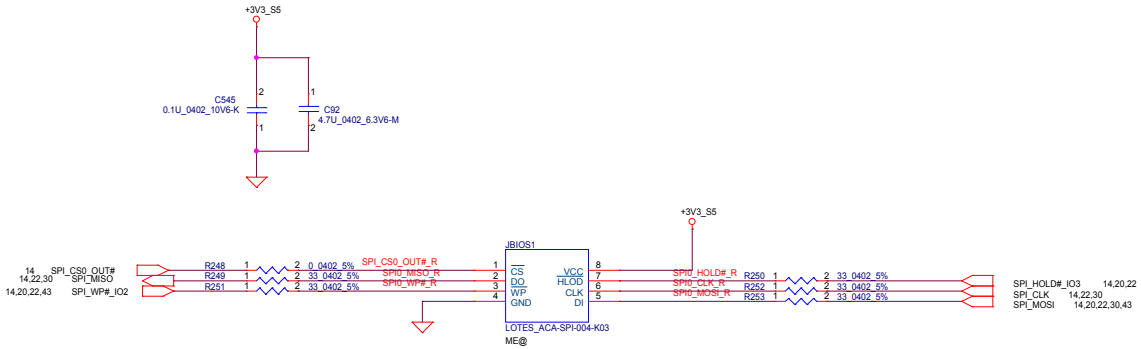
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

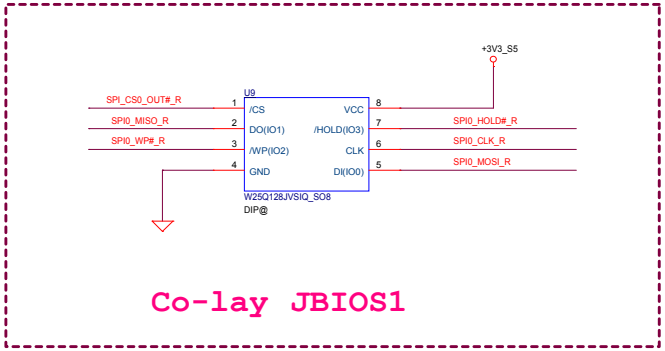
Title: P21-DSW

Size: D | Document Number: E0370 | Rev: 0.7

Date: Friday, January 05, 2018 | Sheet 21 of 62

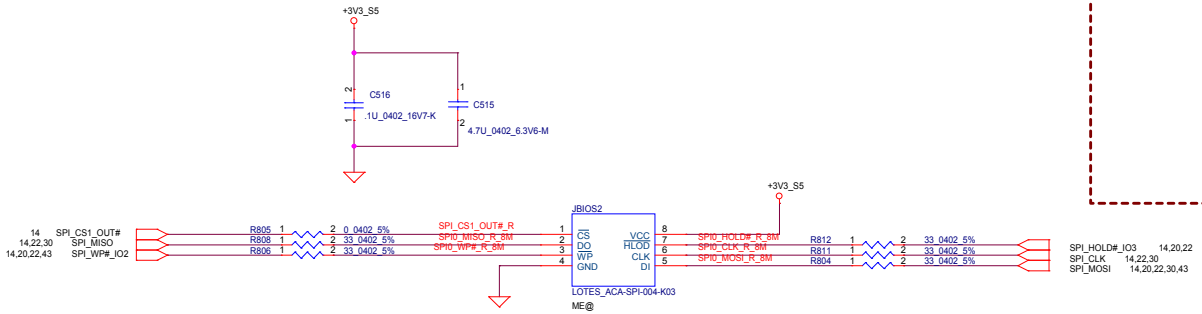
16M ROM

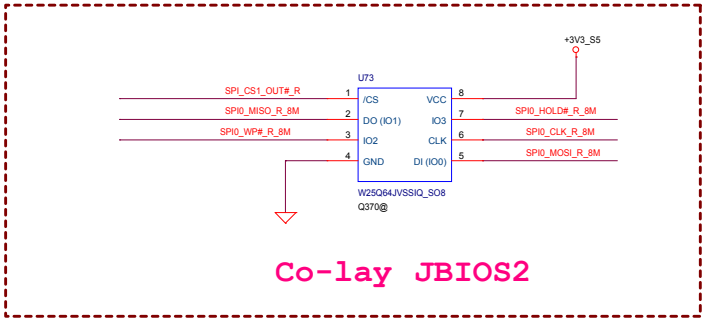




SA00008A300, S IC FL 128M W25Q128JVSIQ SOIC 8P SPI

8M ROM for Q370





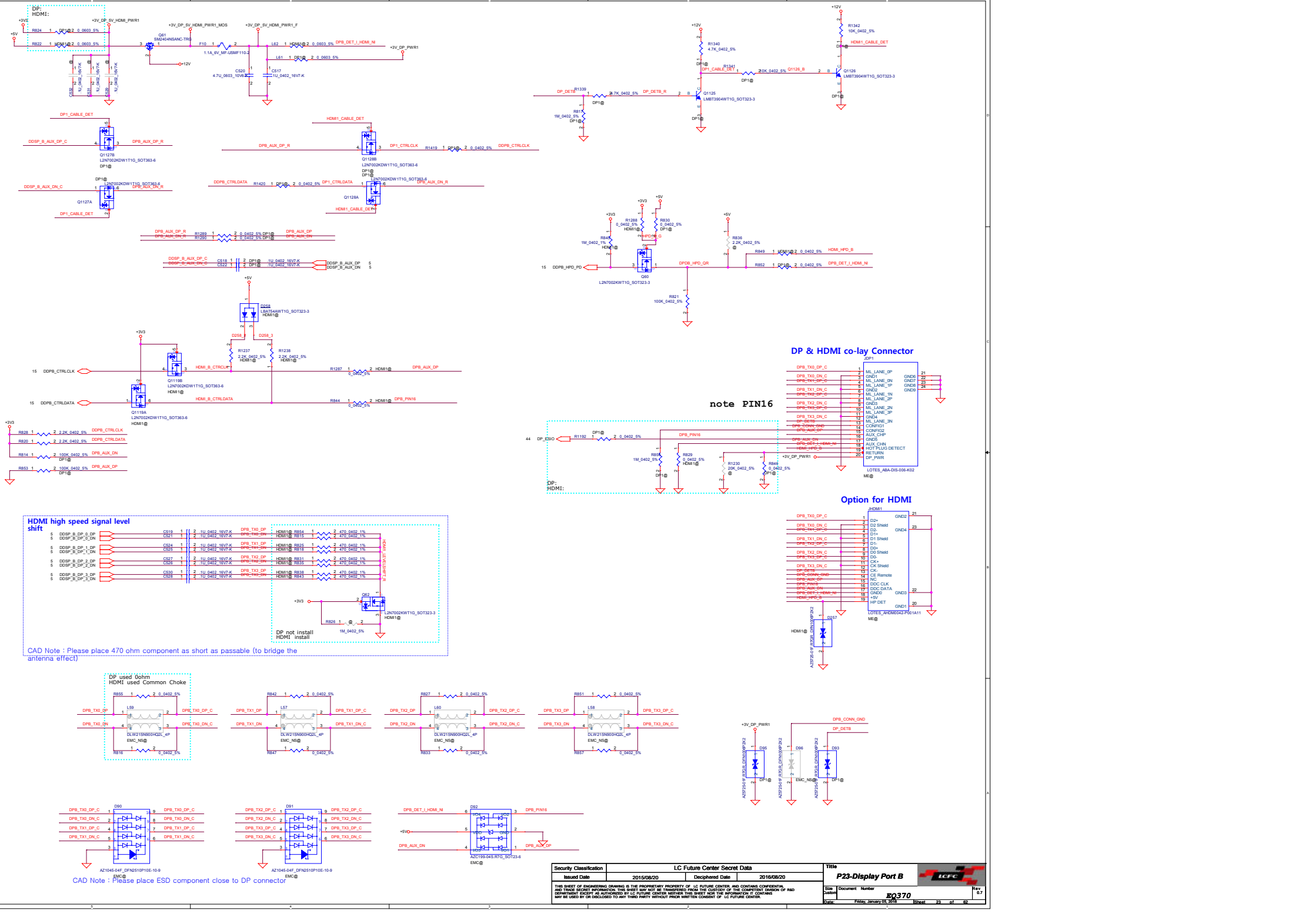
SA000089Z00, S IC FL 64M W25Q64JVSSIQ SOIC 8P 208MIL, A.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: P22-SPI ROM

Size: C | Document Number: EQ370 | Rev: 0.7

Date: Friday, January 05, 2018 | Sheet 22 of 62

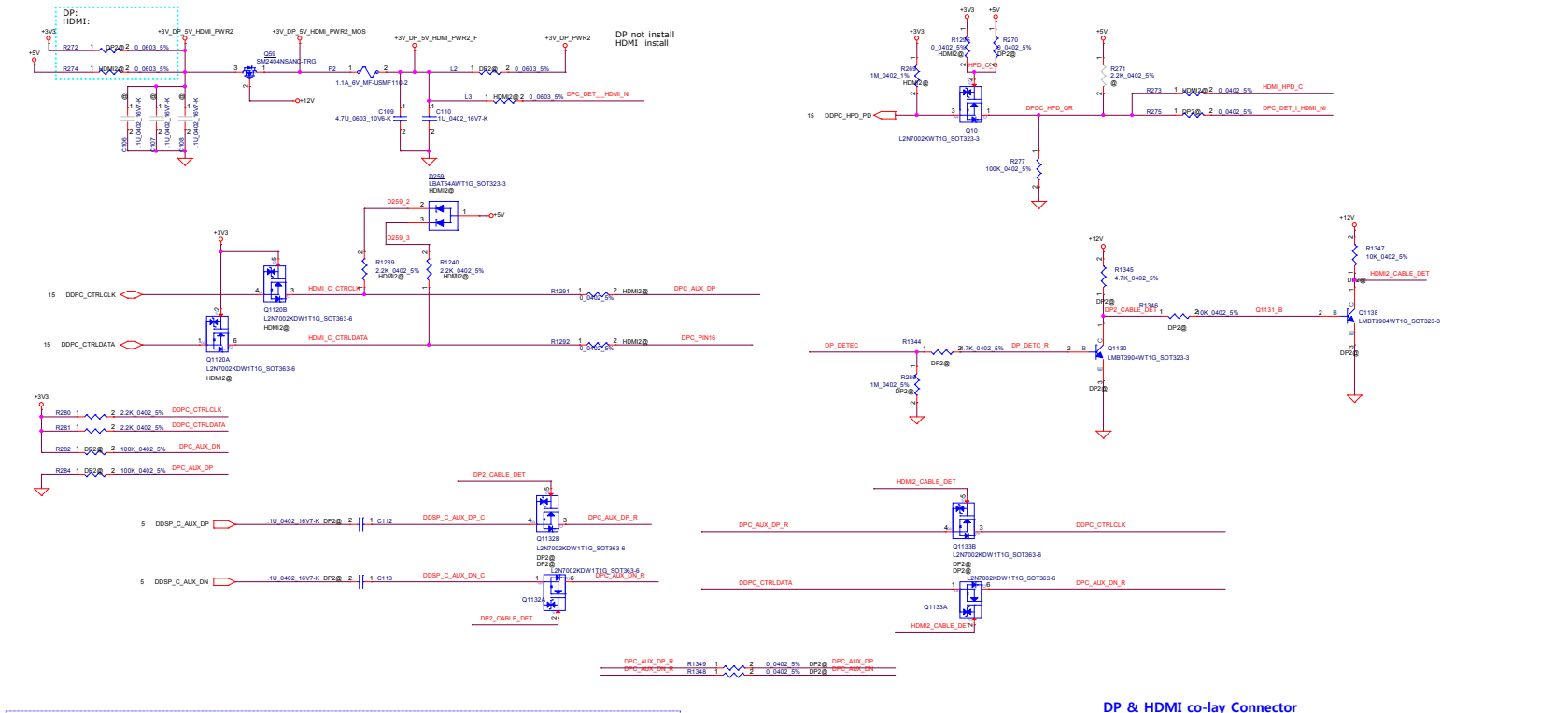


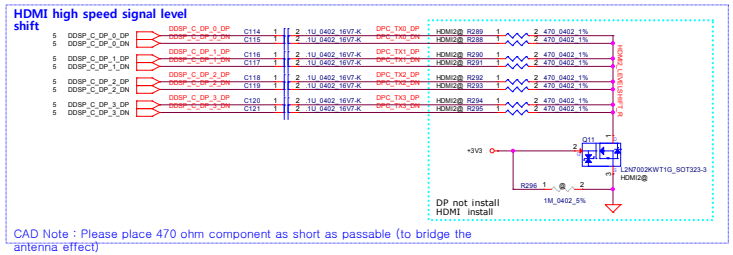
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

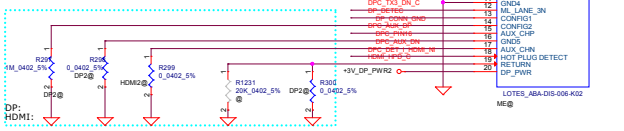
Title: P23-Display Port B

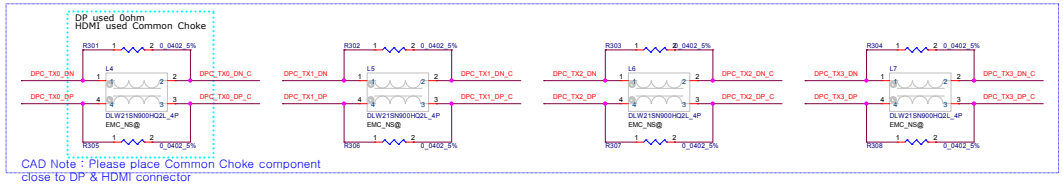
Size: Custom | Document Number: EQ370 | Rev: 0.7

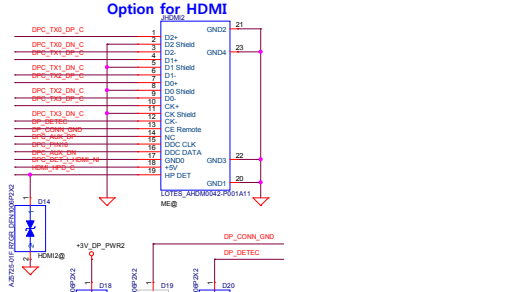
Date: Friday, January 05, 2018 | Sheet 23 of 62

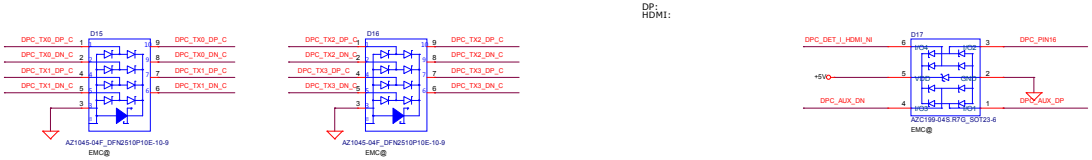












Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **P24-Display Port C**

Size	Document Number	Rev
Custom	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 24 of 62

VCC5_USB_EN
USB_OC0_INT#
VCC5_USB_EN 33,34,35
USB_OC0_INT# 12
C1268 1000P_0402_50V7-K @

COM_A_DET# CONN
R1467 0_0402_5%
COM_A_DET# 18
EMC@ D292 AZ5725-01F.R7GR_DFN1006P2X2
C1270 .1U_0402_10V6-K

R600 0_0402_5%
R602 0_0402_5%
12 USB20_N1
12 USB20_P1
USB_P1-
USB_P1+
U77 DLW21SN900HQ2L_4P EMC_NS@

+5V
R1464 100K_0402_1%
DPD_HPD
R1465 100K_0402_1%
DDPD_HPD_PD
DDPD_HPD_PD 15
Q1157 L2N7002KWT1G_SOT323-3
EMC@ D293 AZ5725-01F.R7GR_DFN1006P2X2

Need relink symble from CIS

JP48

15 DDPD_CTRLCLK
15 DDPD_CTRLDATA
R1462 0_0402_5%
R1463 0_0402_5%
DDPD_CTRLCLK_R
DDPD_CTRLDATA_R
28,33 SOUT1-
28 DTR1-
28 DCD1-
28,33 SIN1-
14,27,28,41,45,57 SLP_S3#
SOUT1-
DTR1-
DCD1-
SIN1-
SLP_S3#
USB_P1-
USB_P1+
+3V3 1A
+5V_S5 1.5A
+5V 0.5A
+12V 0.4A

RXT_RI1- 29
DSR1- 28
RTS1- 28
CTS1- 28
USB30_RX7_N 12
USB30_RX7_P 12
USB30_TX7_N 12
USB30_TX7_P 12
USB_DET#
USB_OC0_INT#
VCC5_USB_EN
COM_A_DET#_CONN
DP_D_DET#
DPD_HPD
SLP_S4#
SLP_S4# 8,14,28,34,35,39,41,44,45,57

5 DDSP_D_AUX_DN
5 DDSP_D_AUX_DP
R1457 0_0402_5%
R1456 0_0402_5%
DDSP_D_AUX_DN_C
DDSP_D_AUX_DP_C
5 DDSP_D_DP_3_DN
5 DDSP_D_DP_3_DP
R1455 0_0402_5%
R1454 0_0402_5%
DDI3_TX3_DN_R
DDI3_TX3_DP_R
DDI3_TX2_DN_R
DDI3_TX2_DP_R
R1453 R1452
DDSP_D_DP_2_DN 5
DDSP_D_DP_2_DP 5
DDI3_TX1_DN_R
DDI3_TX1_DP_R
R1451 R1450
DDSP_D_DP_1_DN 5
DDSP_D_DP_1_DP 5
DDI3_TX0_DN_R
DDI3_TX0_DP_R
R1459 R1458
DDSP_D_DP_0_DN 5
DDSP_D_DP_0_DP 5
0_0402_5%

ELCO_1450470608108291+ ME@

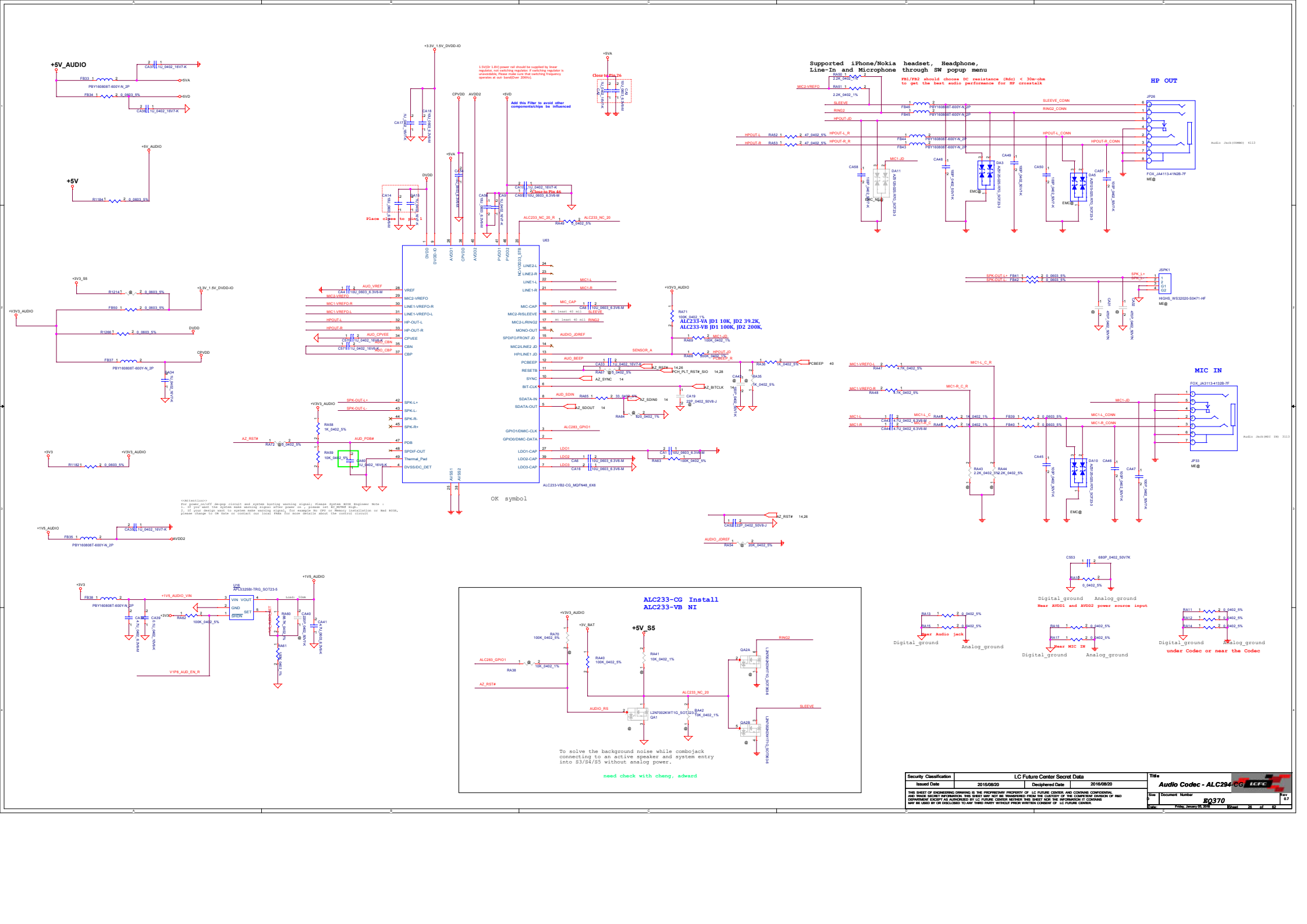
USB_DET# 18
DP_D_DET# 18
EMC@ D291 AZ5725-01F.R7GR_DFN1006P2X2
C1269 0.1U_0402_10V6-K
EMC@ D290 AZ5725-01F.R7GR_DFN1006P2X2
C1271 0.1U_0402_10V6-K

+3V3
R313 100K_0402_5%
DDSP_D_AUX_DN_C
DDSP_D_AUX_DP_C
R317 100K_0402_5%

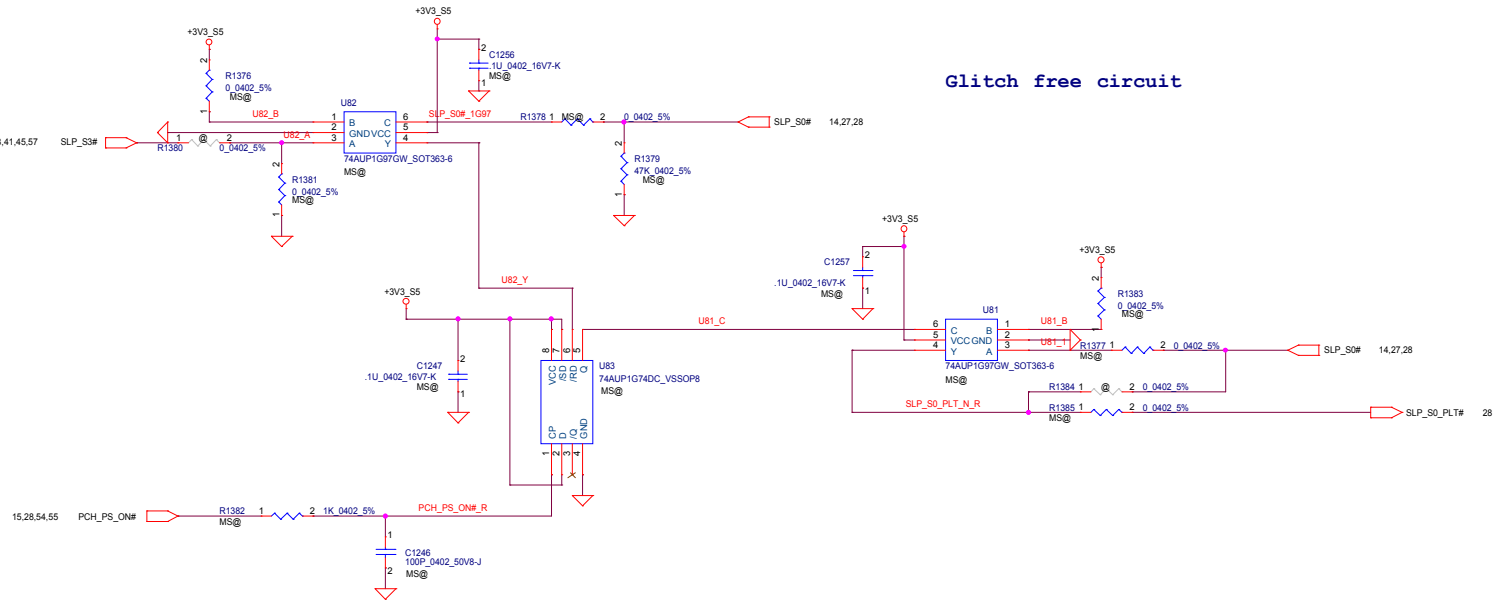
+3V3
R1356 2.2K_0402_5% DDPD_CTRLCLK
R1355 2.2K_0402_5% DDPD_CTRLDATA

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: P25-Display Port D
Size: C
Document Number: EQ370
Rev: 0.7
Date: Saturday, January 06, 2018
Sheet 25 of 62


+5V_AUDIO
+5V
+3.3V_1.5V_DVDD-IO
1.5V(Or 1.8V) power rail should be supplied by linear regulator, not switching regulator. If switching regulator is unavoidable, Please make sure that switching frequency operates at out- band(Over 200Khz).
Close to Pin 26
Add this Filter to avoid other components/chips be influenced
Place close to pin 1
Close to Pin 46
ALC233_NC_20_R
ALC233_NC_20
U63
ALC233-VA JD1 10K, JD2 39.2K,
ALC233-VB JD1 100K, JD2 200K,
ALC233-VB2-CG_MQFN48_6X6
OK symbol
Supported iPhone/Nokia headset, Headphone, Line-In and Microphone through SW popup menu
FB1/FB2 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk
HP OUT
MIC IN
ALC233-CG Install
ALC233-VB NI
+5V_S5
To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.
need check with cheng, adward
Near Audio jack
Near MIC IN
Near AVDD1 and AVDD2 power source input
under Codec or near the Codec
Digital_ground
Analog_ground
Security Classification
LC Future Center Secret Data
Issued Date
2015/08/20
Deciphered Date
2016/08/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
Audio Codec - ALC294-CG
Size
D
Document Number
EQ370
Rev
0.7
Date
Friday, January 05, 2018
Sheet
28
of
62

Glitch free circuit



Mask circuit for VR_ENABLE

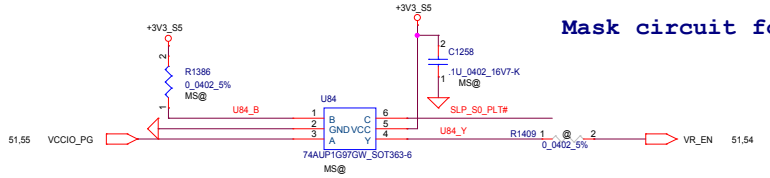
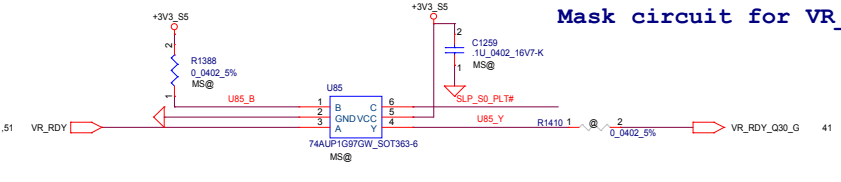


Table 4. Function table[1]

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

[1] H = HIGH voltage level,
L = LOW voltage level.

Mask circuit for VR_READY

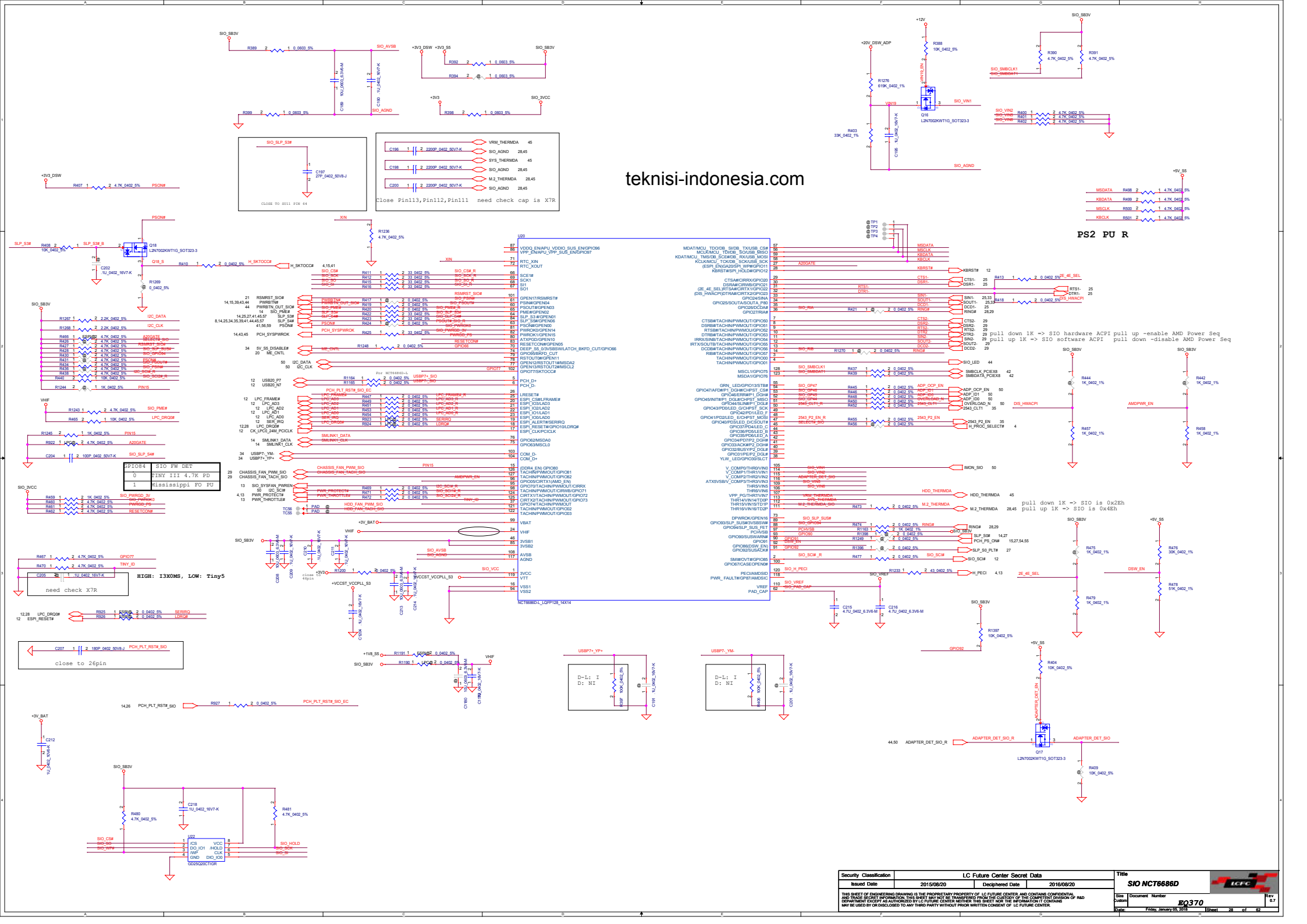


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Audio Jack_Line I-O/ Mic in

Size	Document Number	Rev
C	EQ370	0.7

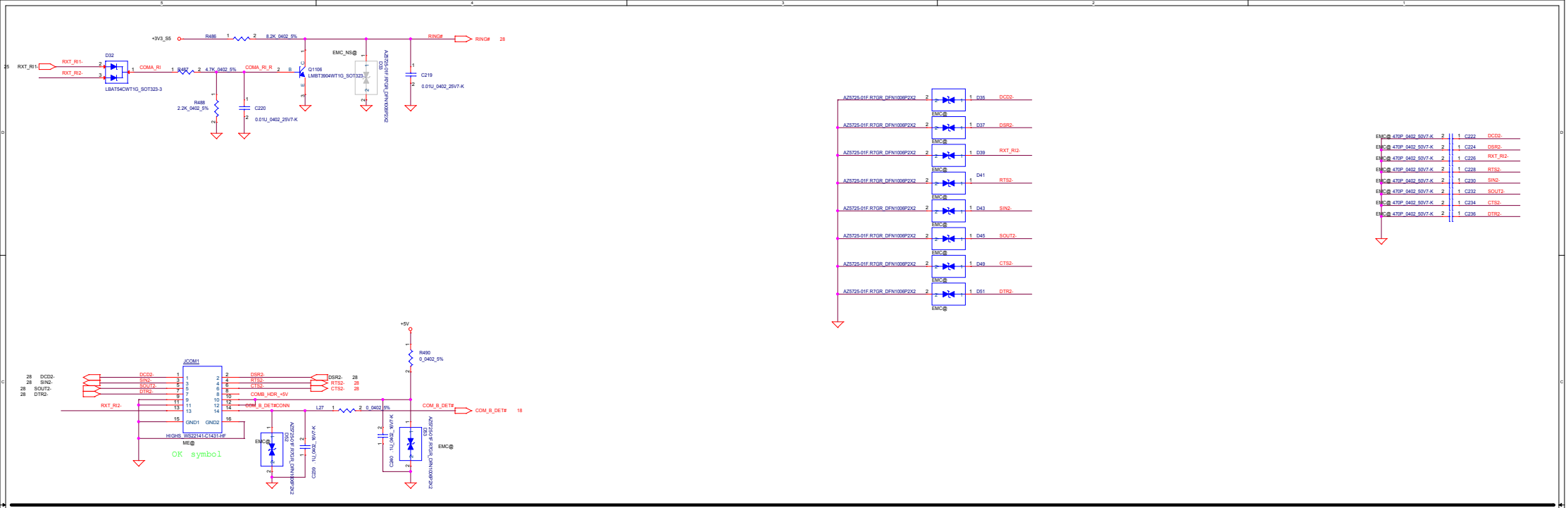
Date: Friday, January 05, 2018 Sheet 27 of 62

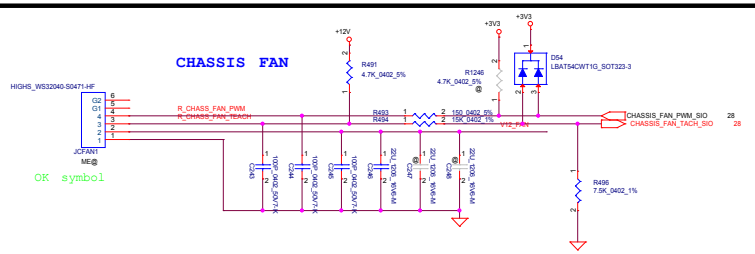


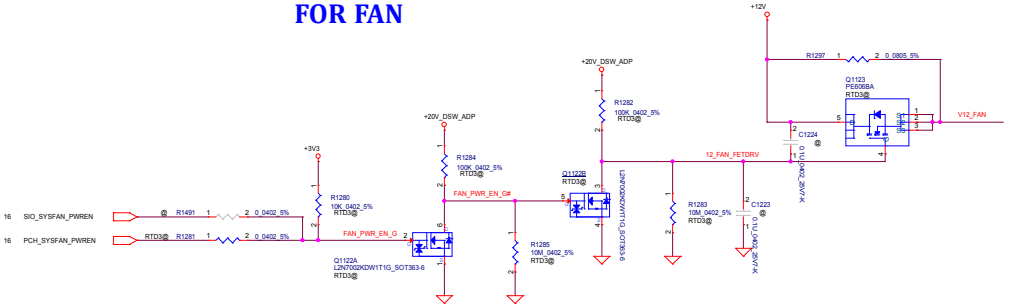
Security Classification	LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date 2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title		
SIO NCT6686D		
Size: Custom	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 28 of 62	



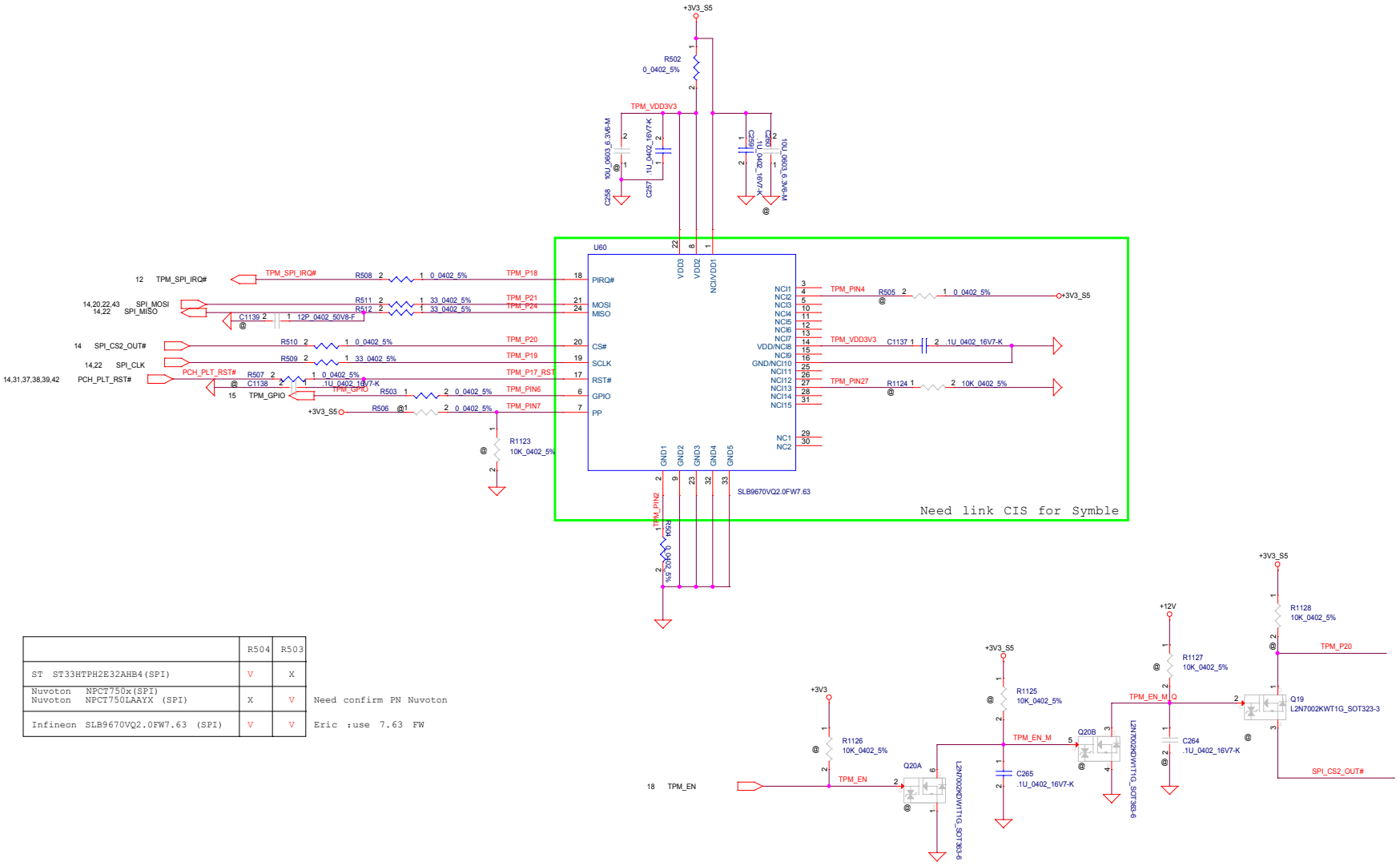




Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: COM Port/ FAN CRTL

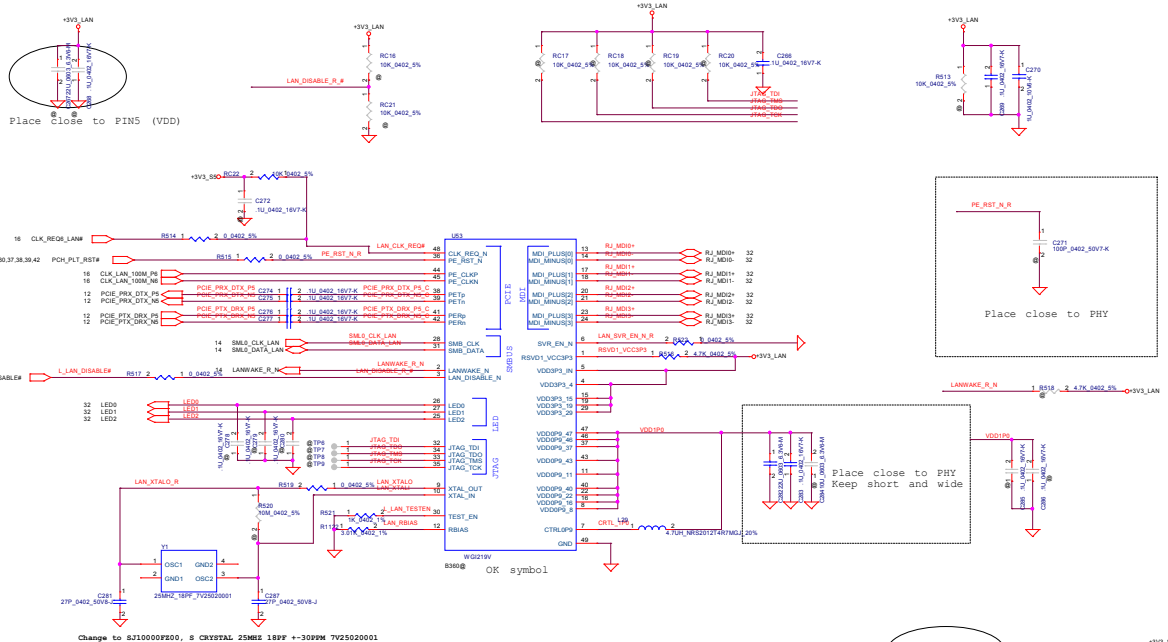
Size: Custom	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 29 of 62	

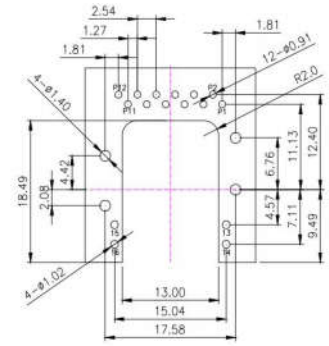


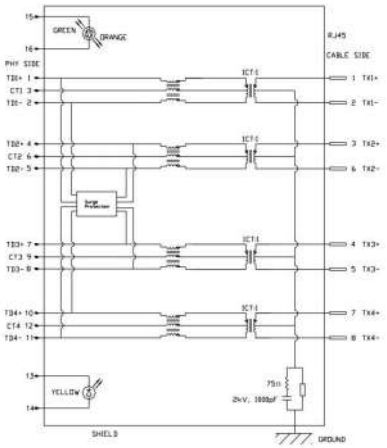
	R504	R503	
ST ST33HTPH2E32AHB4(SPI)	V	X	
Nuvoton NPCT750x(SPI) Nuvoton NPCT750LAAYX (SPI)	X	V	Need confirm PN Nuvoton
Infineon SLB9670VQ2.0FW7.63 (SPI)	V	V	Eric :use 7.63 FW

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

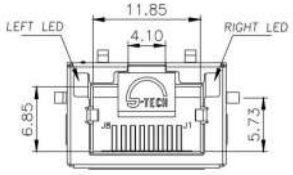
Title	TPM - TCG 2.0		
Size C	Document Number EQ370		Rev 0.7
Date: Friday, January 05, 2018	Sheet 30 of 62		

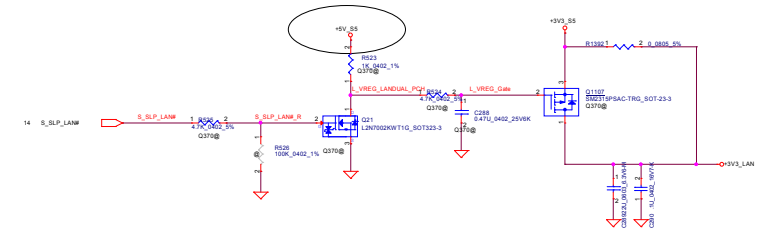






MOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	83/84/85	Off	Off	Off
On	10Mb Inactive	On	Off	Off
On	10Mb Active	Blinking	Off	Off
On	100Mb Inactive	On	On	Off
On	10Mb Active	Blinking	On	Off
On	1Gb Inactive	On	Off	On
On	1Gb Active	Blinking	Off	On



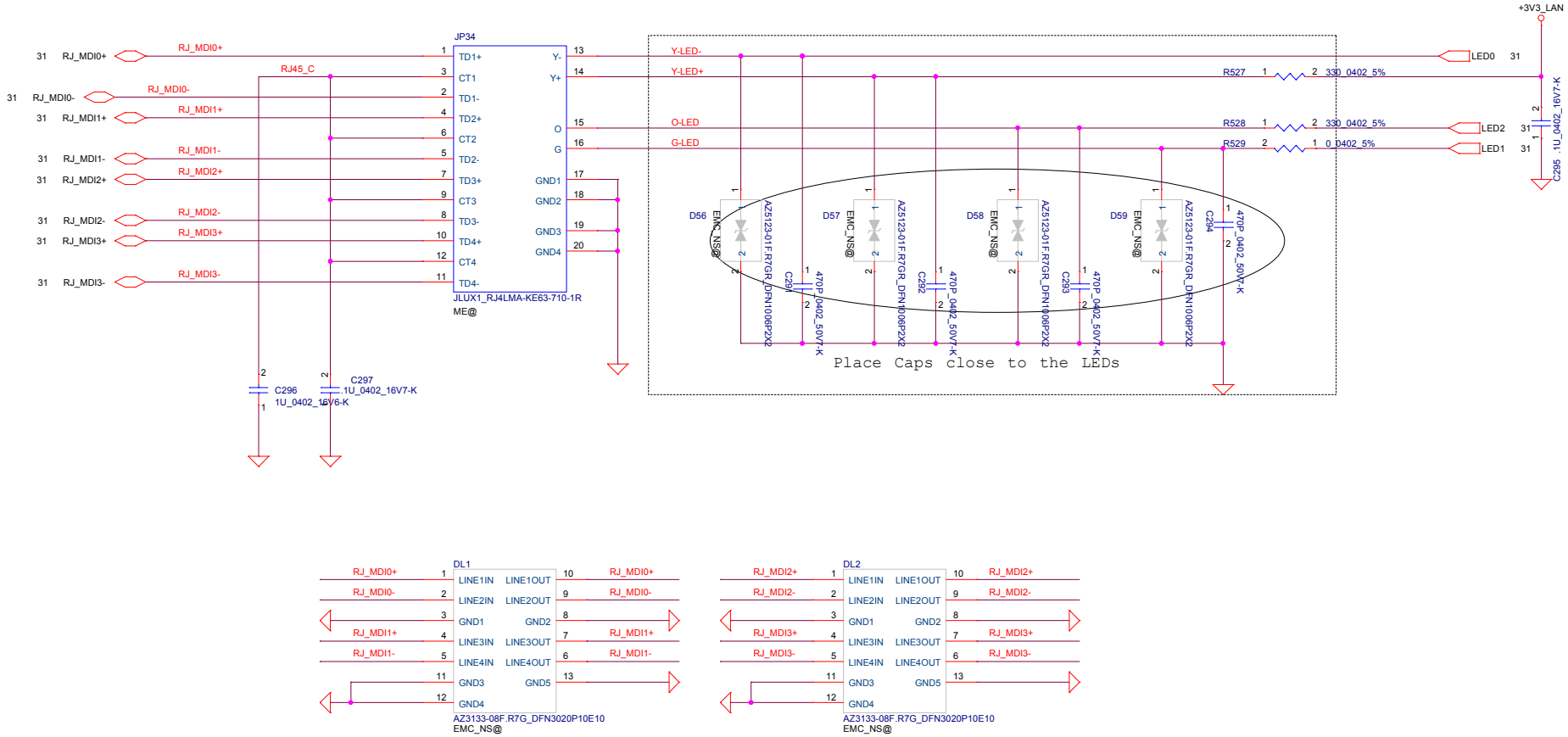


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: LAN - JacksonVille_I219LM

Size: D | Document Number: EQ370 | Rev: 0.7

Date: Friday, January 05, 2018 | Sheet 31 of 62



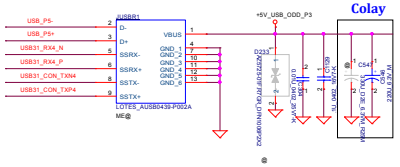
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

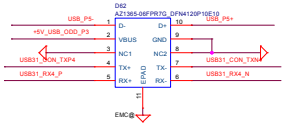
Title: **RJ45**

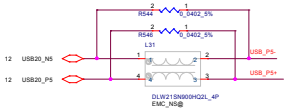
Size: Custom | Document Number: **EQ370** | Rev: 0.7

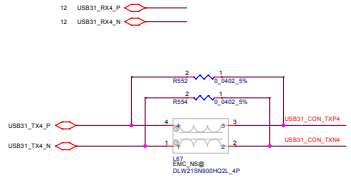
Date: Friday, January 05, 2018 | Sheet 32 of 62

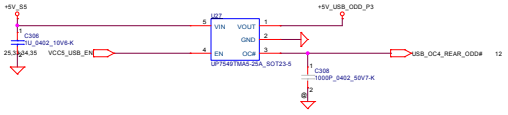
Rear Side USB ODD



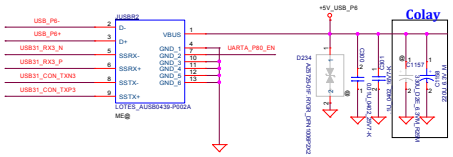


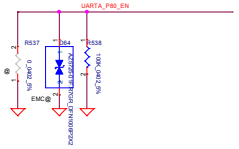


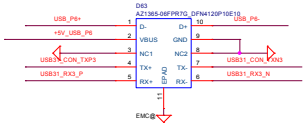


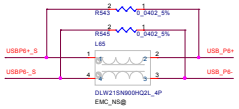


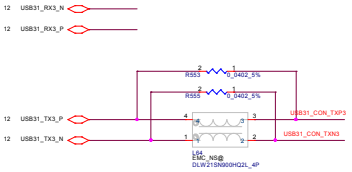
Rear Side USB 3.1 GEN2

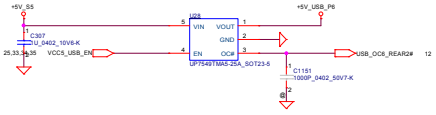




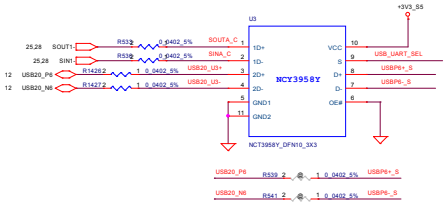








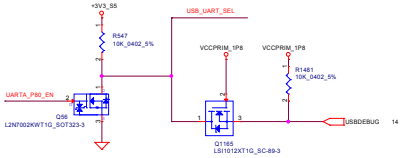
For USB Debug Function



USBDEBUG	Kernel debug
Ref input	Ref input
Ref output low	ENABLE

UART_P80_EN	POST 80
Ref input	DISABLE
Ref output low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) TO 1E(+/-)
L	H	D(+/-) TO 2E(+/-)

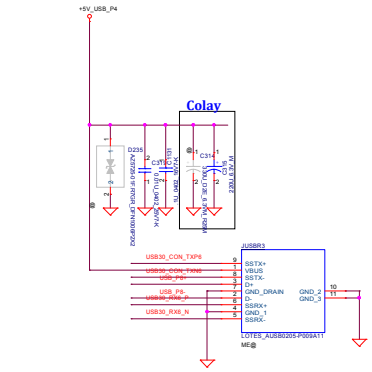


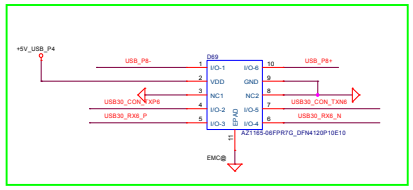
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

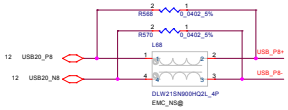
Title	Power sequence block
Size: D	Document Number: EQ370
Date: Friday, January 05, 2018	Sheet 33 of 62

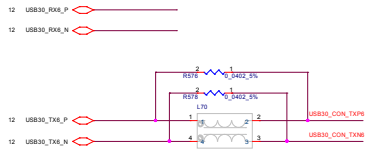
Rev: 0.7

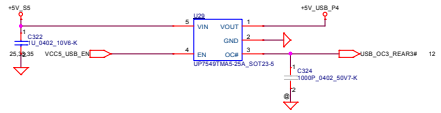
Rear Side USBx2



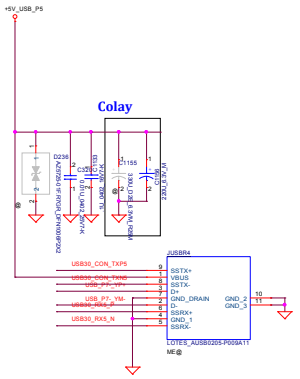


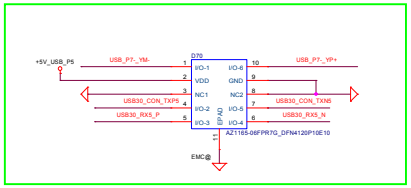


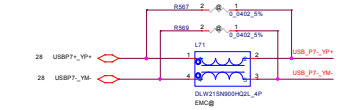


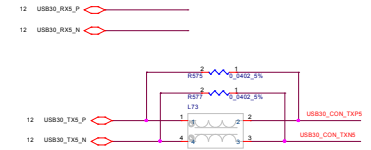


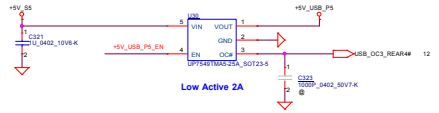
need change footprint



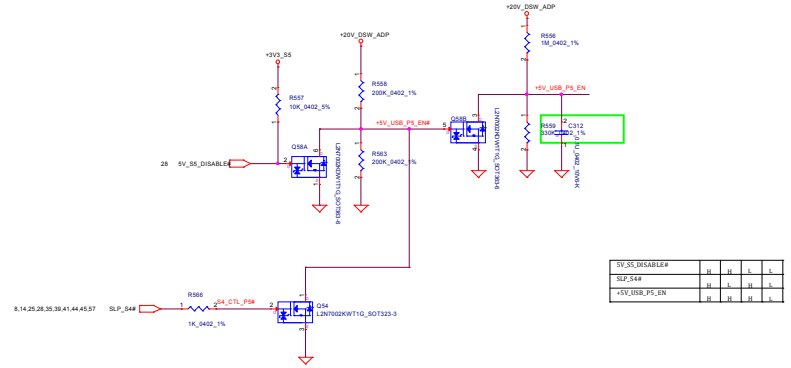








need change footprint



5V_S5_DISABLE#	H	H	L	L
SLP_S4#	H	L	H	L
+5V_USB_P5_EN	H	H	H	L

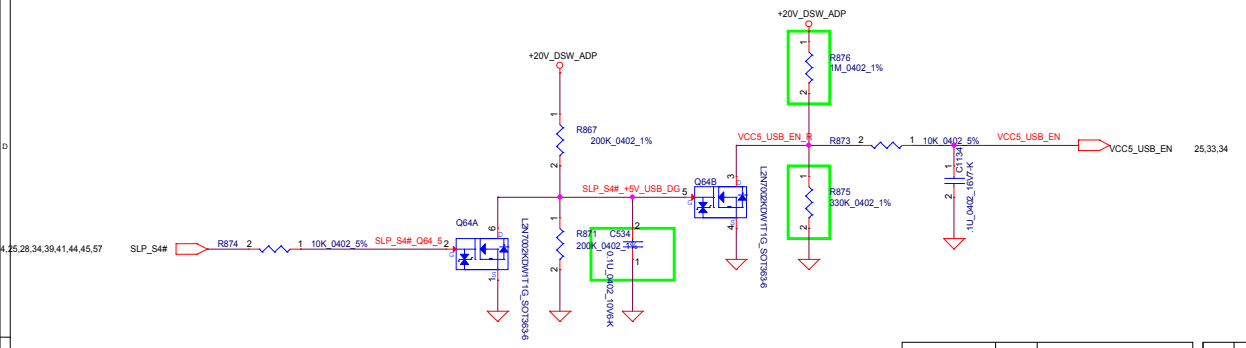
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: Virtual symbol

Size	Document Number	Rev
D	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 34 of 62

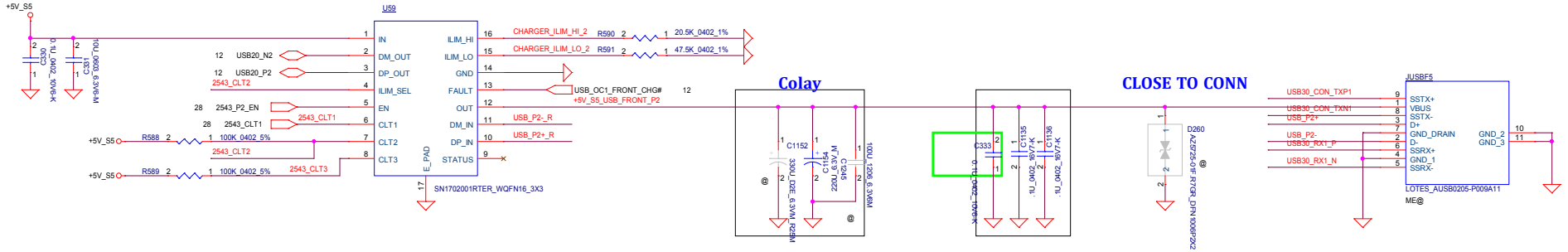


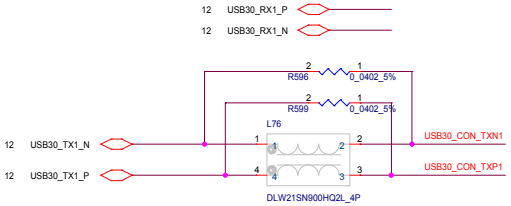
ILIM_HI	20.5K	2.5A
ILIM_LO	47.5K	1.1A

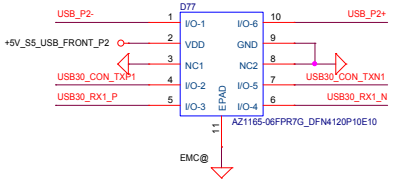
DCP	Tiny S3/S4/S5
CDP	Tiny S0 Tiny not support

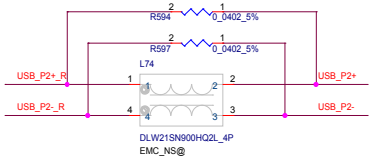
CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
						off
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	I_{OS_PW} & ILIM_HI (1)	DCP load present (2)
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present (3)
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP (4)	ILIM_LO	off
1	1	1	1	CDP (4)	ILIM_HI	CDP load present (5)

FRONT USB3.0 Charger









USB charge

www.teknisi-indonesia.com

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: need change footprint Hole

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 35 of 62

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

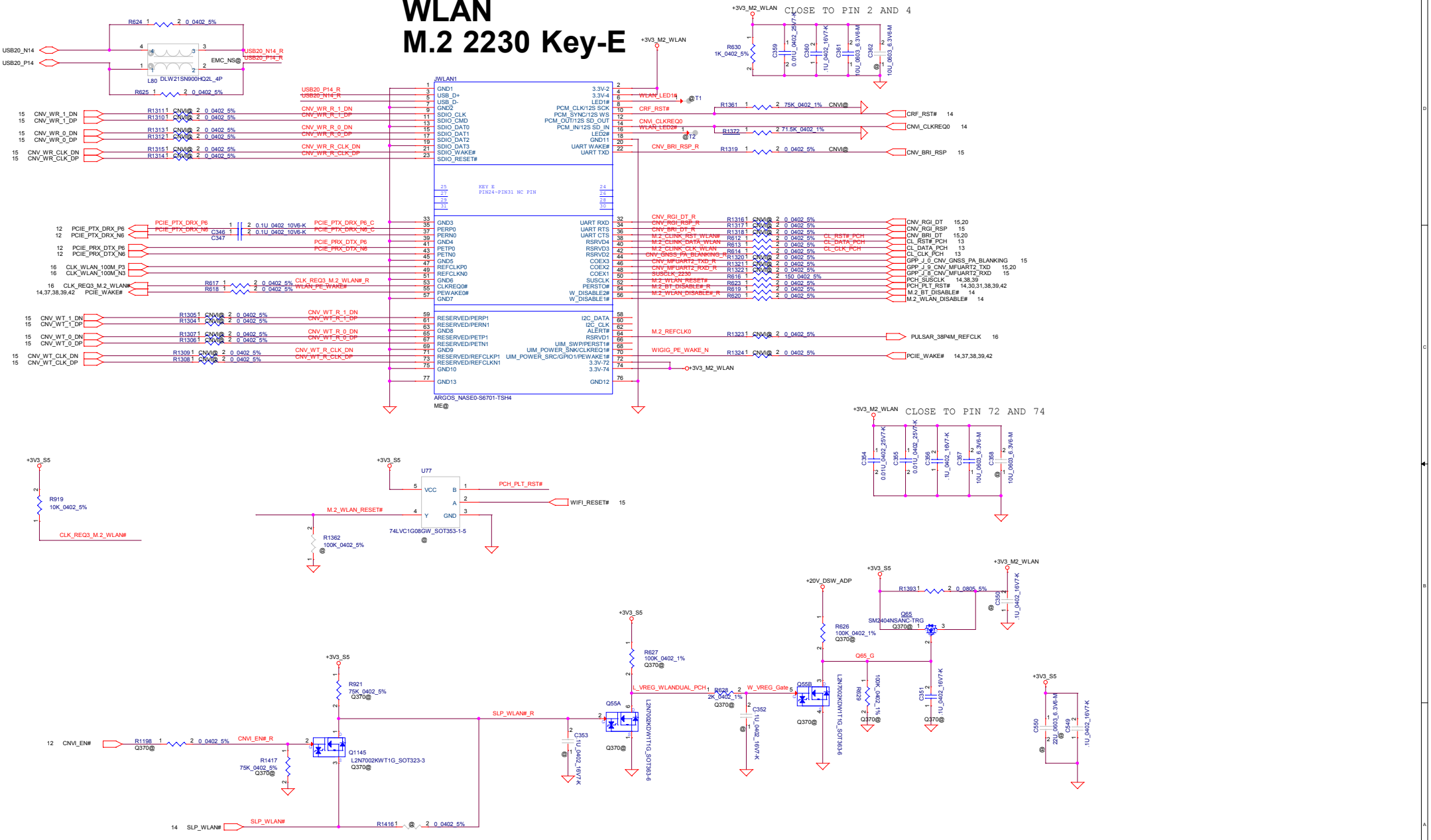
Title

PWR-Power Diagram

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 36 of 62

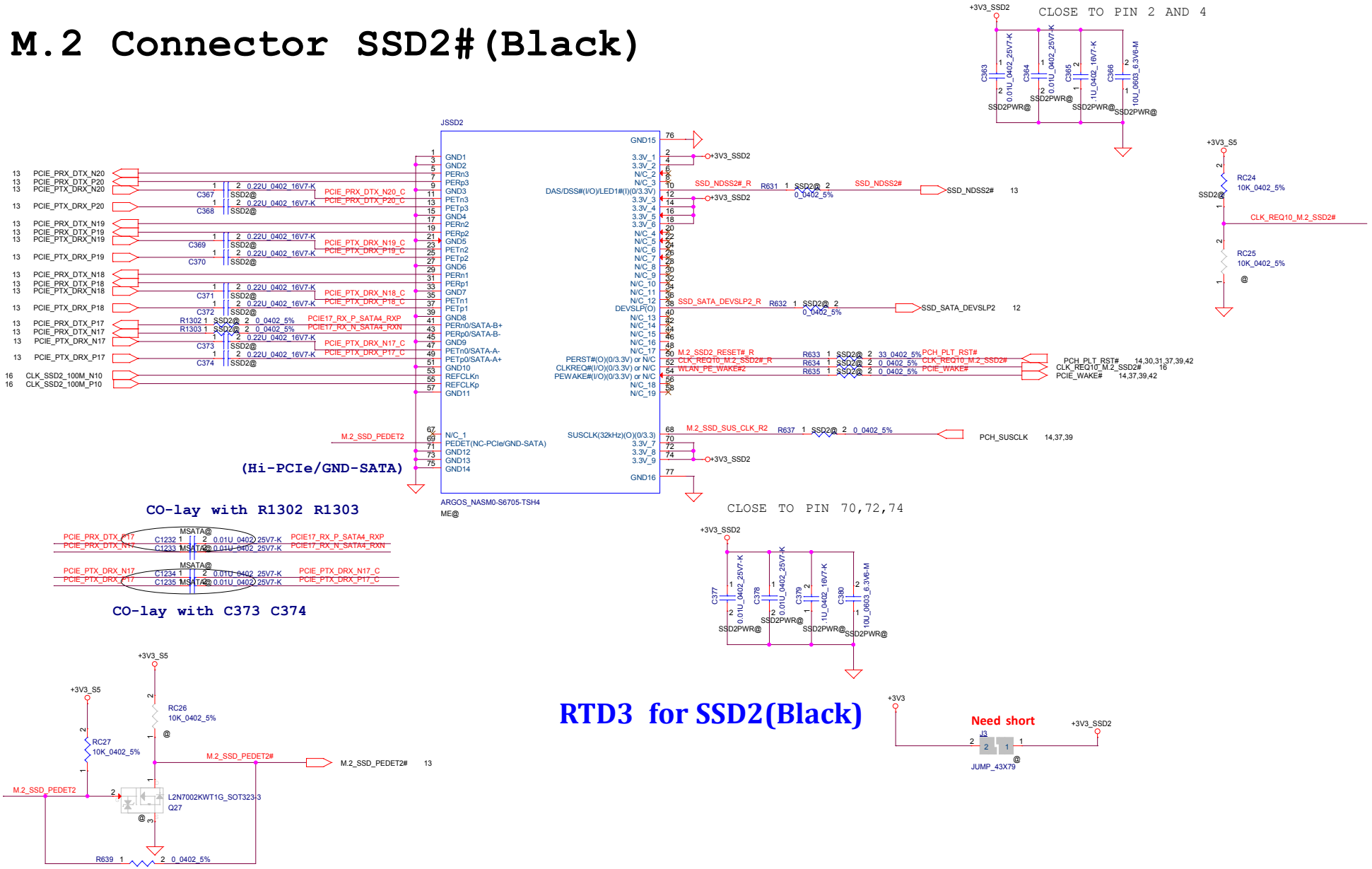
WLAN
M.2 2230 Key-E



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	M.2 2230-E WIFI/ BT		
Size	Custom	Document Number	EQ370
Rev	0.7		
Date:	Friday, January 05, 2018	Sheet	37 of 62

M.2 Connector SSD2#(Black)



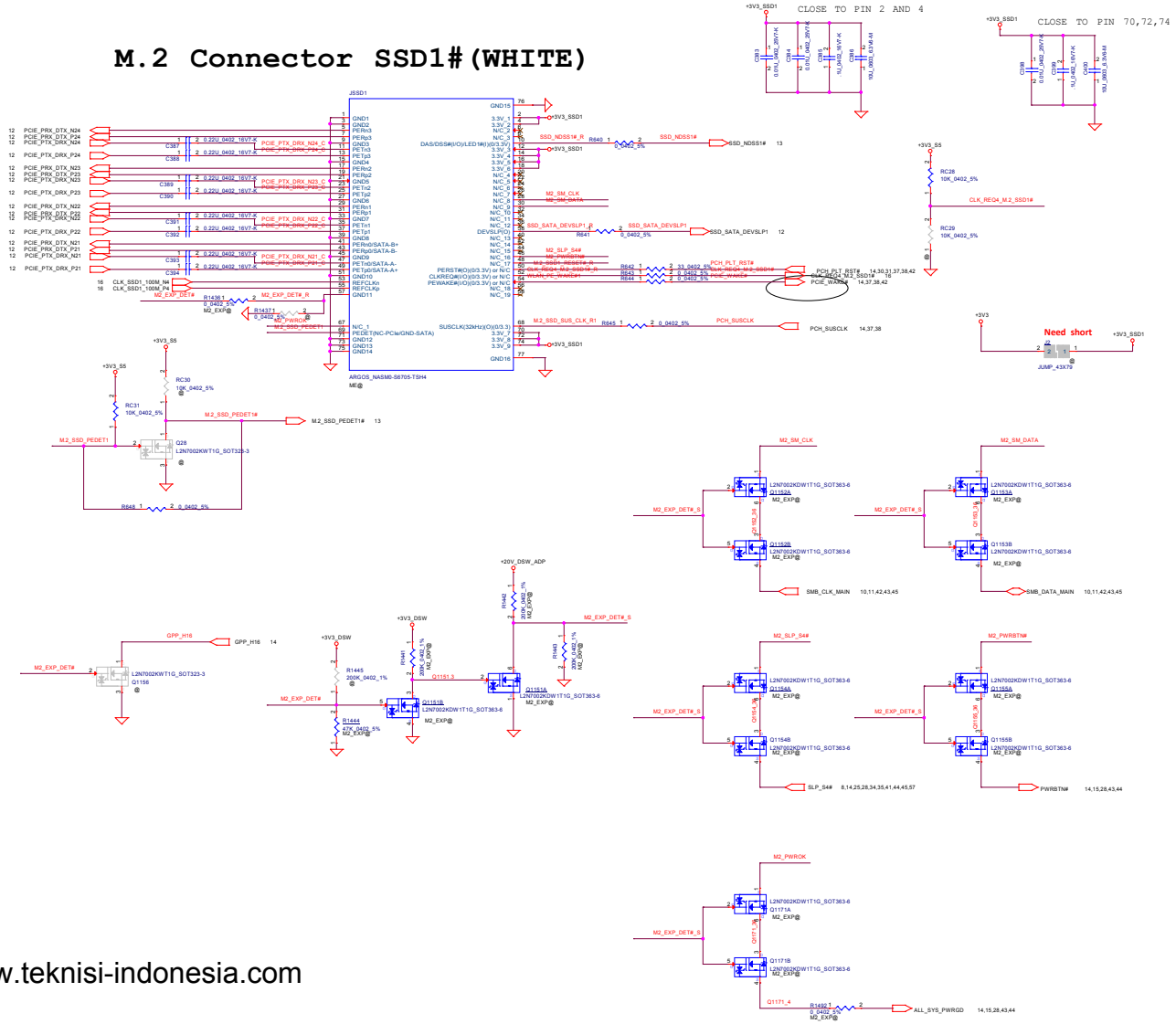
Security Classification	LC Future Center Secret Data	
Issued Date	2015/08/20	Deciphered Date 2016/08/20

Title: M.2 2280-M SSD-2

Size: Custom | Document Number: EQ370 | Rev: 0.7

Date: Friday, January 05, 2018 | Sheet 38 of 62

M.2 Connector SSD1#(WHITE)



www.teknisi-indonesia.com

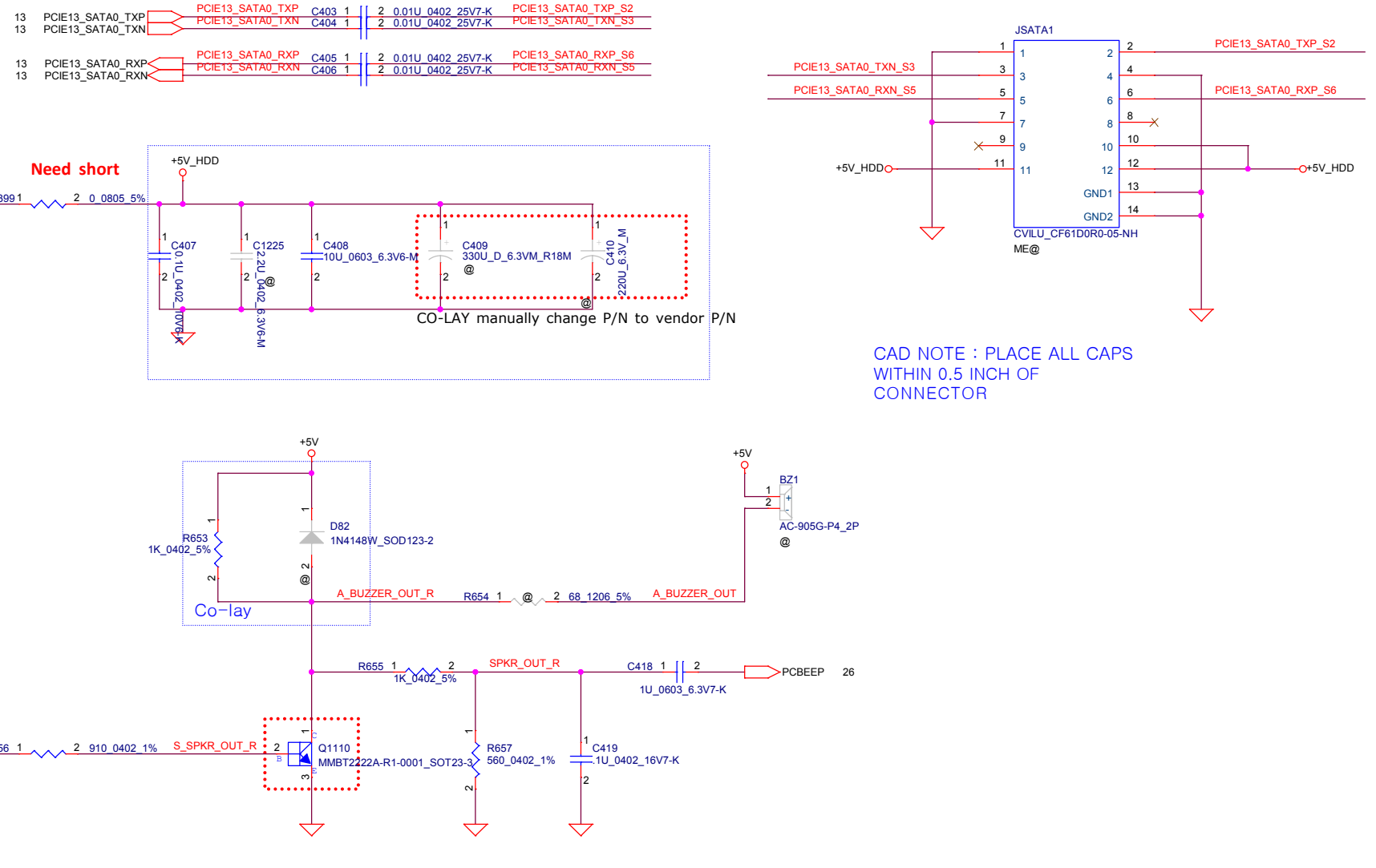
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: M.2 2280-M SSD-1

Size: D | Document Number: EQ370 | Rev: 0.7

Date: Friday, January 08, 2016 | Sheet 39 of 62

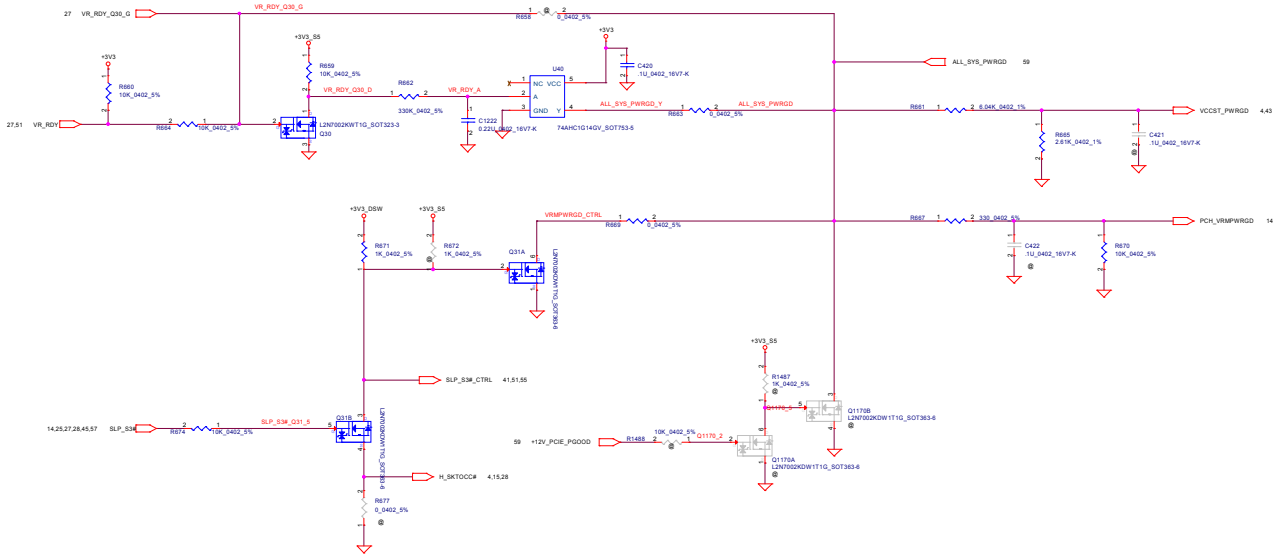


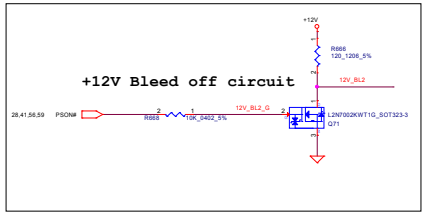
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

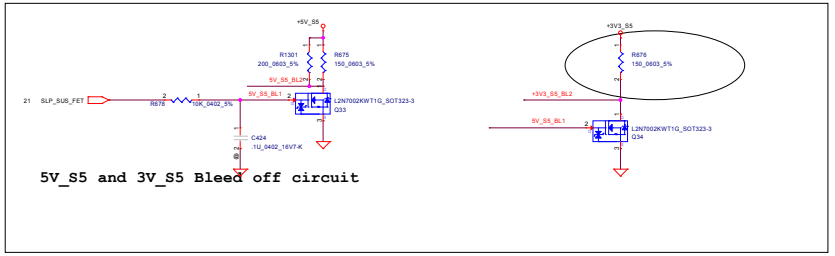
Title: **Buzzer/Sata Cable/Debug P**

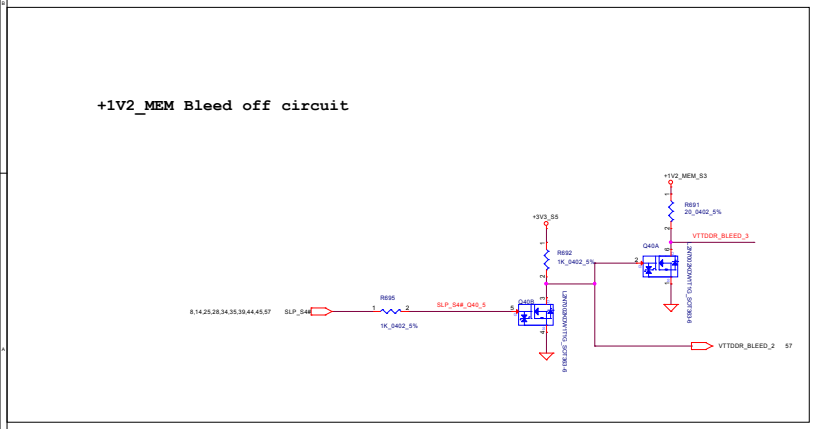
Size	Document Number	Rev
B	EQ370	0.7

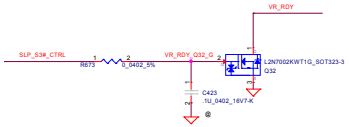
Date: Friday, January 05, 2018 Sheet 40 of 62





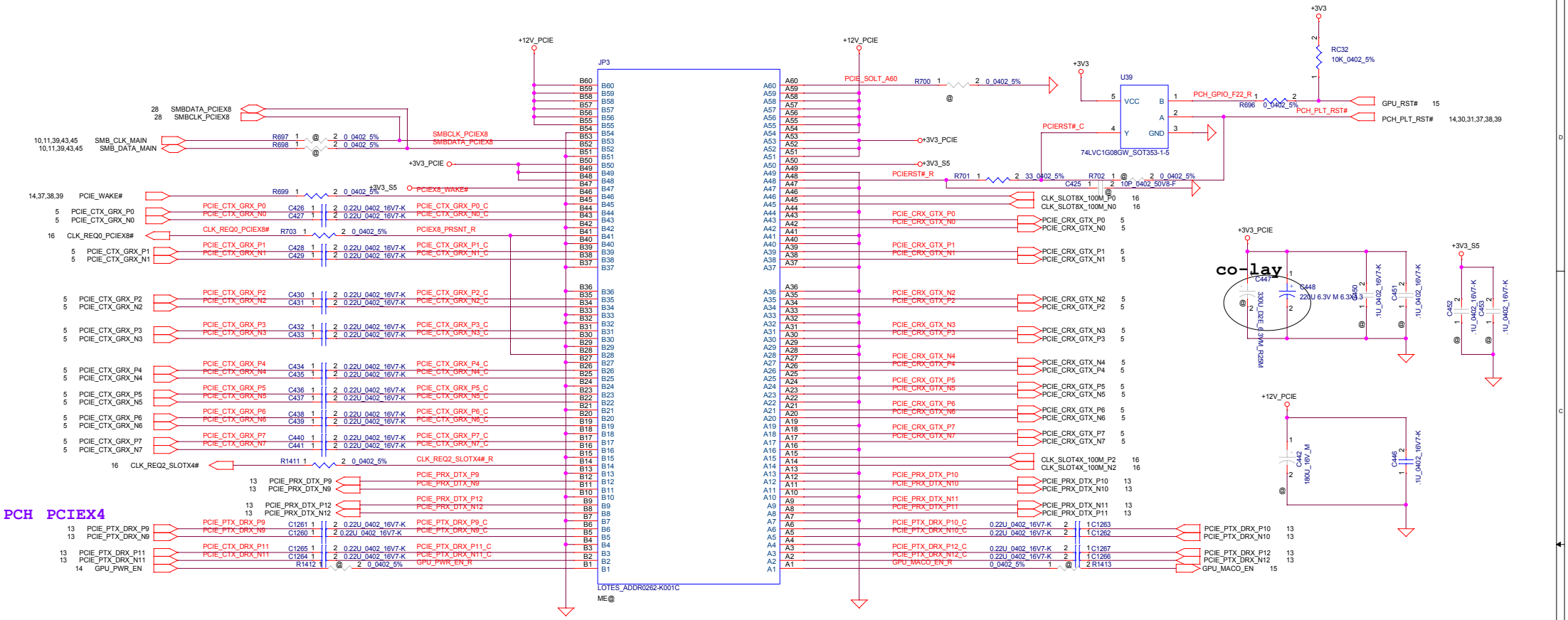






Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

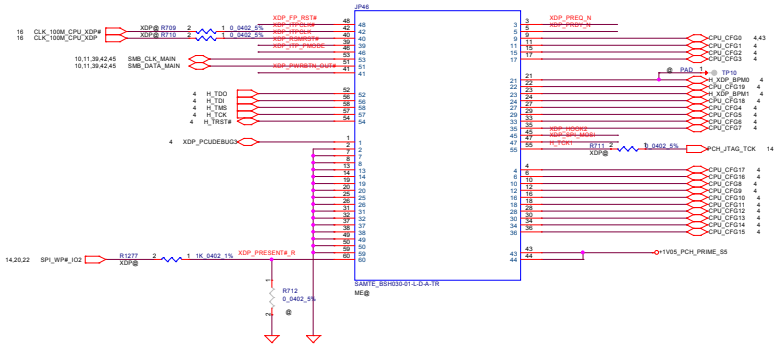
Title	PWRGD & Bleed Off		
Size	Document Number		Rev
D	EQ370		0.7
Date	Friday, January 05, 2018	Sheet 41 of 52	

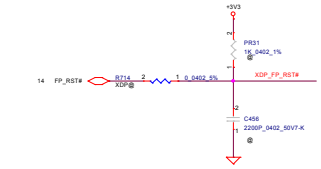


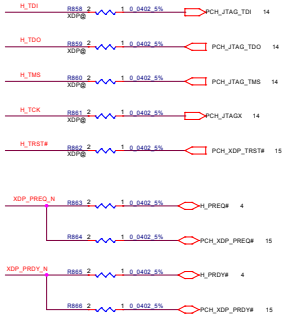
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

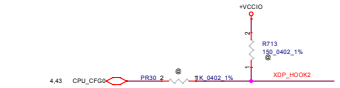
Title	PCIEX8		
Size: Custom	Document Number: EQ370		Rev: 0.7
Date: Friday, January 05, 2018	Sheet 42 of 62		

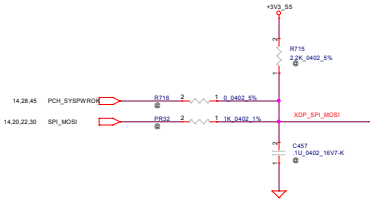
Intel XDP Debugging Connector

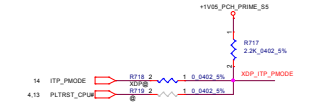


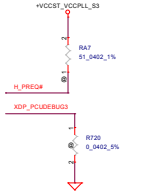


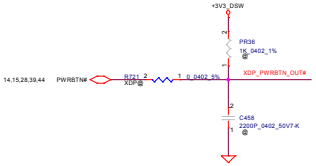












Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	XDP	
Size	Document Number	Rev
D	EQ370	0.7
Date: Friday, January 05, 2018	Sheet 43 of 62	

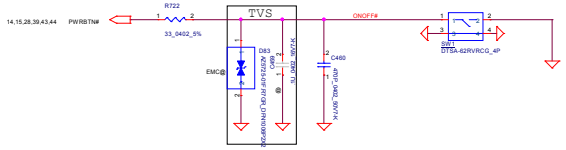
CONTROL PANEL / LED CIRCUITRY

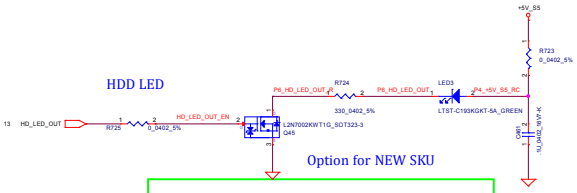
POWER BUTTON & LED

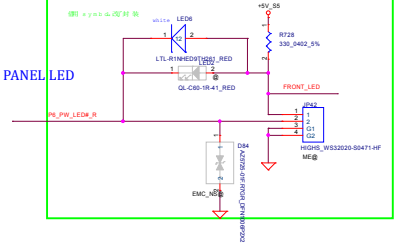
COLOR	Functoin
G	HDD

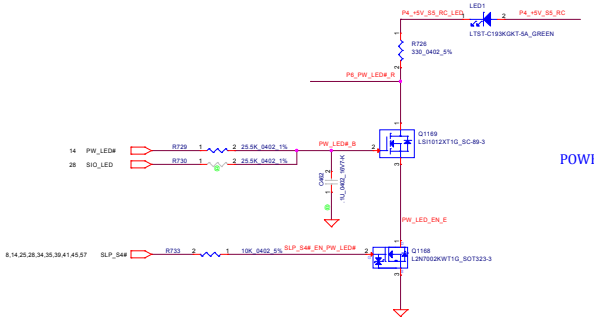
Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 330ohm = 5mA
5m * 3.2 V = 16 mW
0.1W (For Current limit R)

For NEC SKU:
Remove:
R765,Q42,R762
SW1
CR1
Install :
R779
SW1_
CR1_

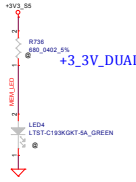


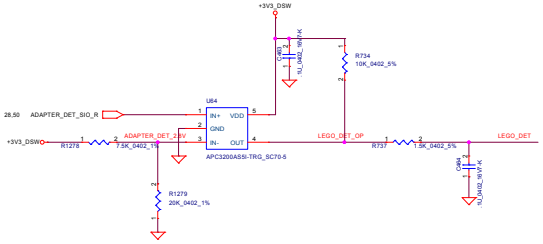


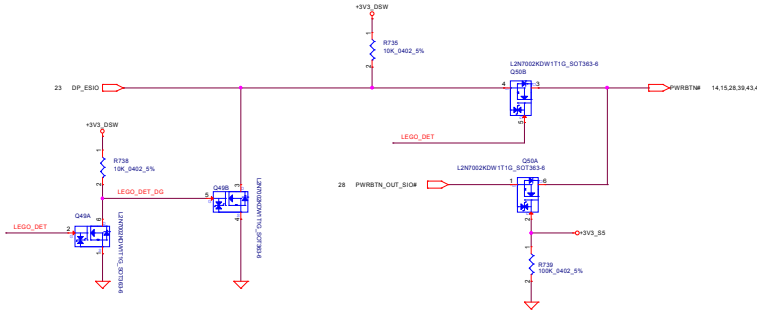




POWER BUTTON With LED







Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

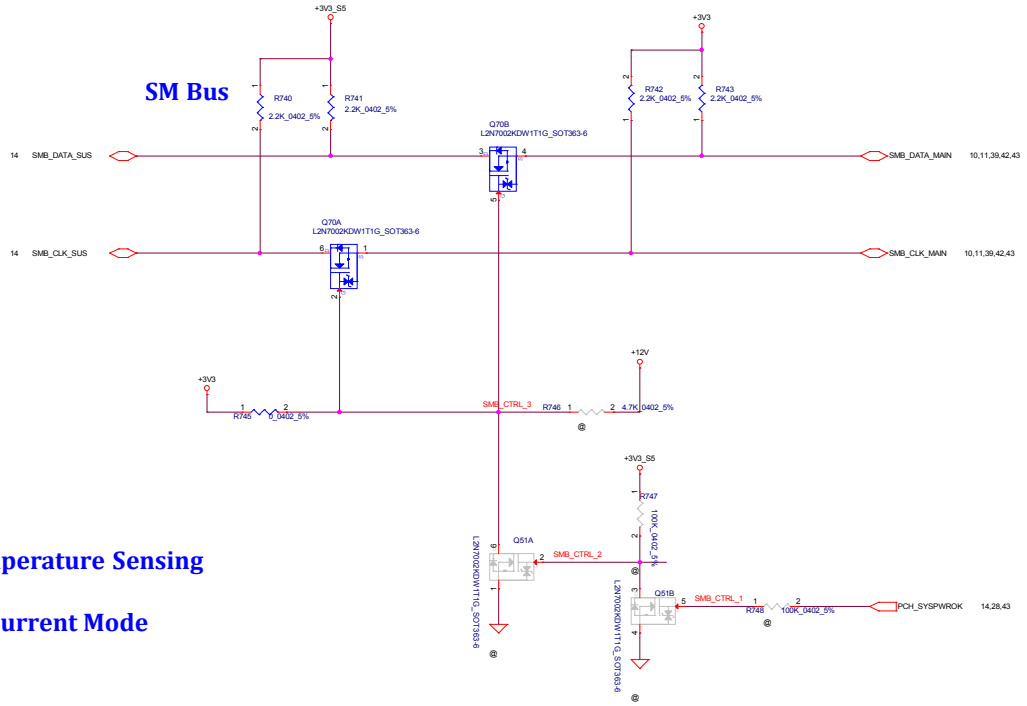
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: **Button/ LED**

Size	Document Number	Rev
D	EQ370	0.7

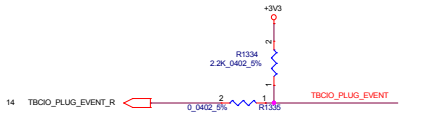
Date: Friday, January 05, 2018 Sheet 44 of 82

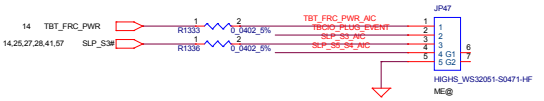
SM Bus



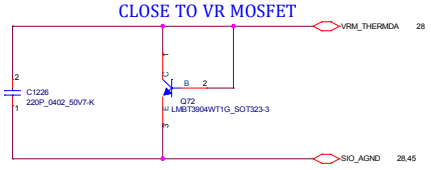
Temperature Sensing

Current Mode



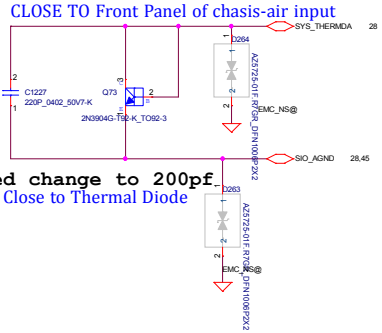


CLOSE TO VR MOSFET



need change to 200pf

CLOSE TO Front Panel of chasis-air input

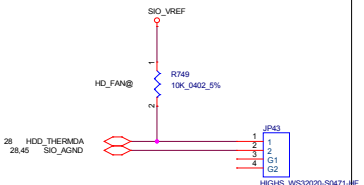


need change to 200pf

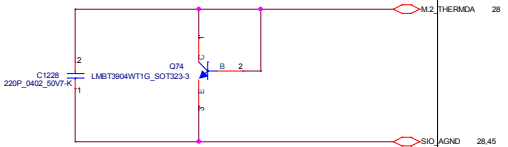
CAD NOTE : Place MLCC Close to Thermal Diode

Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

HDD Thermal sensor



CLOSE TO SJ4 (for M.2)

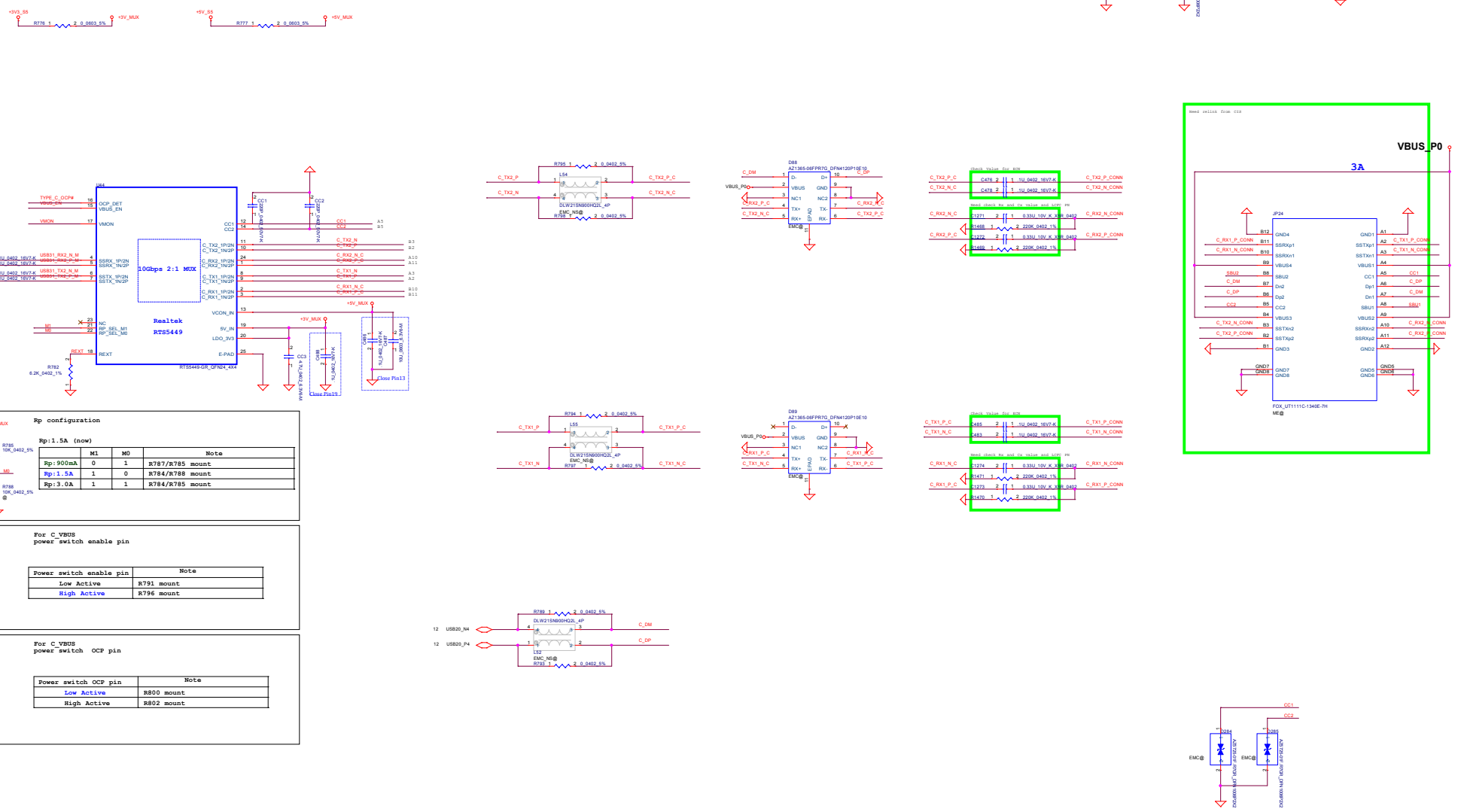


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: SM BUS/Thermal Sensing

Size	Document Number	Rev
Custom	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 45 of 62



Rp configuration	M1	M0	Note
Rp:900mA	0	1	R787/R785 mount
Rp:1.5A	1	0	R784/R788 mount
Rp:3.0A	1	1	R784/R785 mount

For C_VBUS power switch enable pin	Note
Low Active	R791 mount
High Active	R796 mount

For C_VBUS power switch OCP pin	Note
Low Active	R800 mount
High Active	R802 mount

Title: Type-C RTS5449
Size: D | Document Number: EQ370 | Rev: 0.7
Date: Friday, January 05, 2018 | Sheet 48 of 62

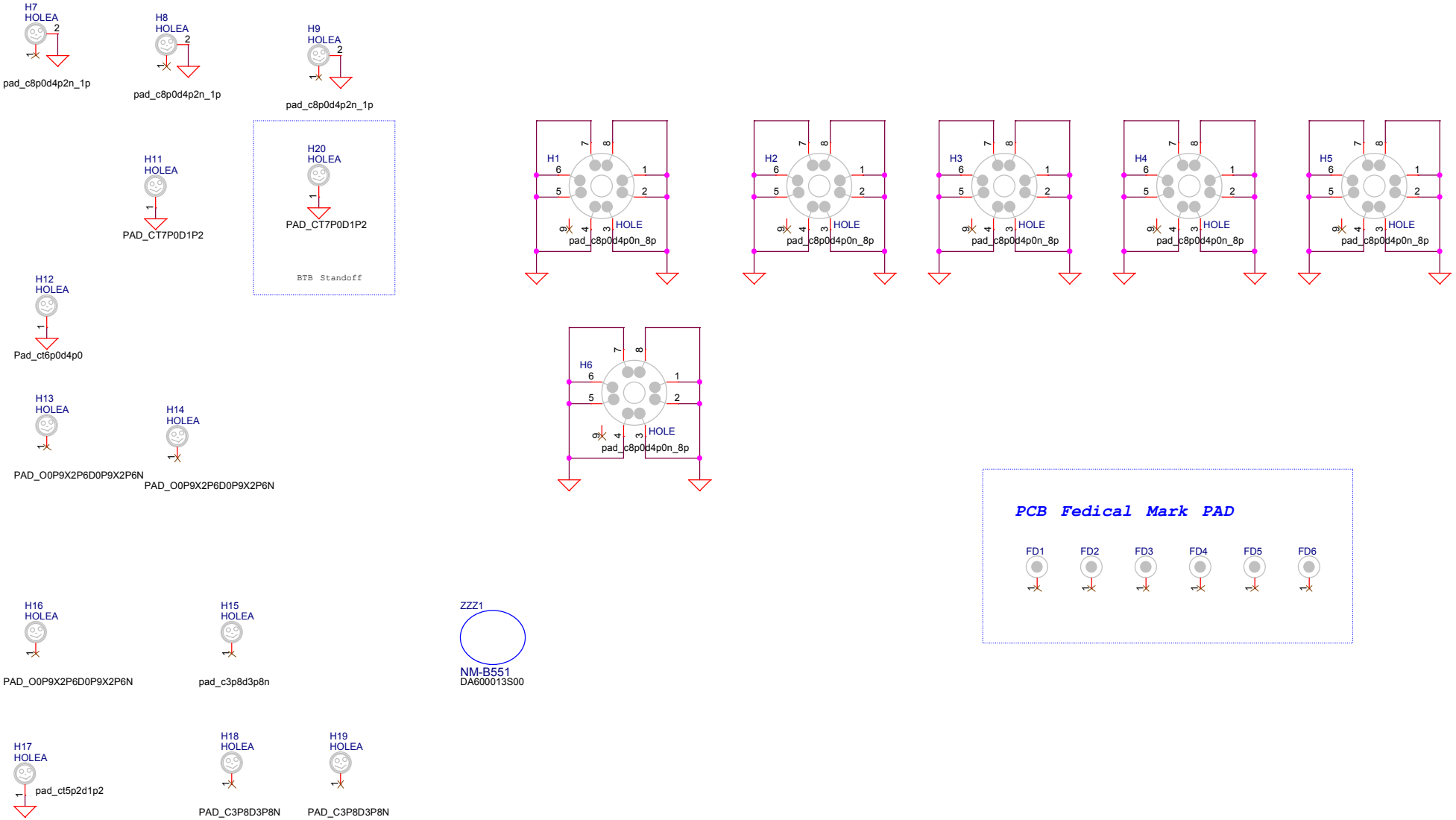
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

RTD3

Size	Document Number	Rev
C	*EQ370*	0.7

Date: Friday, January 05, 2018 | Sheet 47 of 62

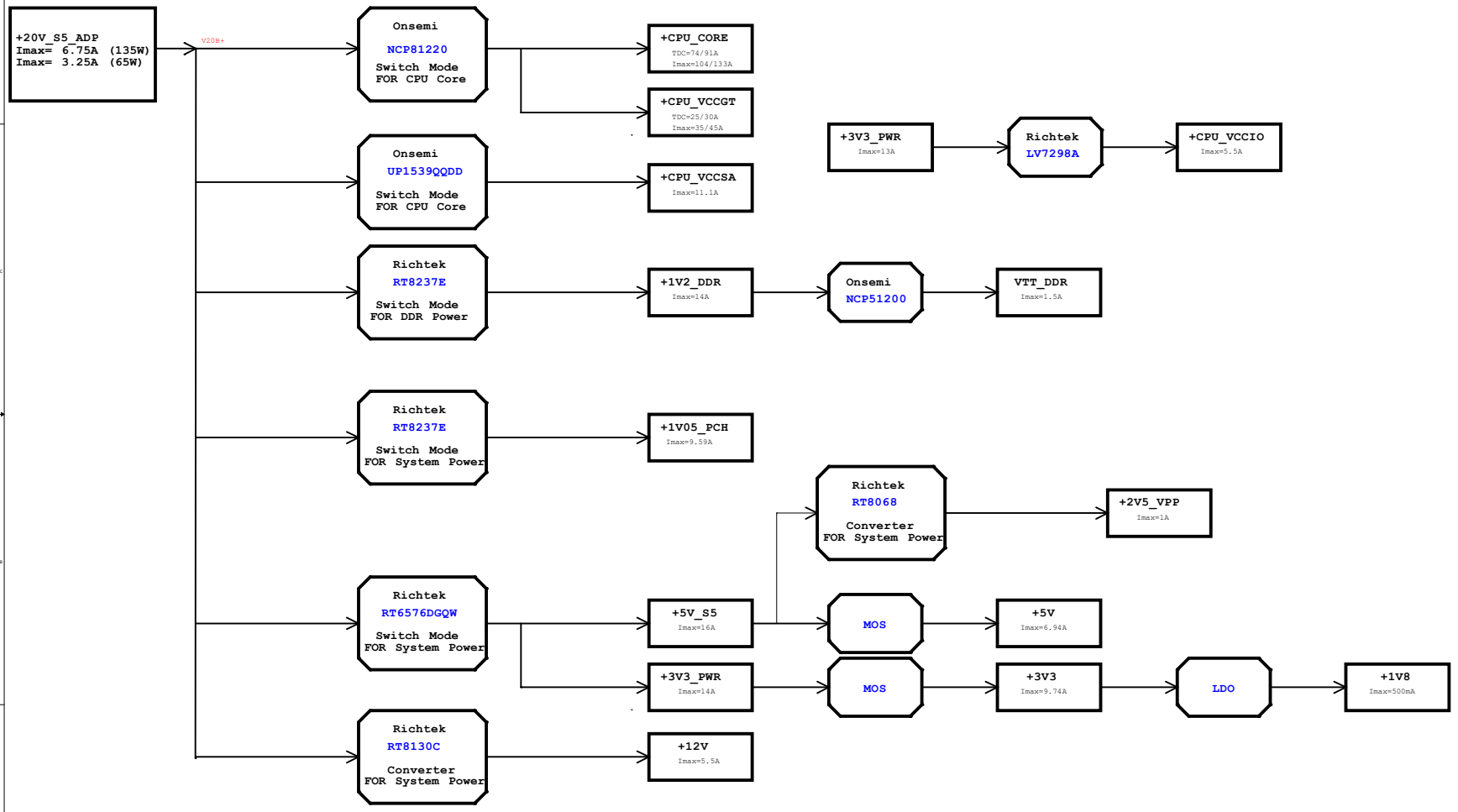


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Mounting Hole/ PCB/ Metal**

Size	Document Number	Rev
B	EQ370	0.7

Date: Friday, January 05, 2018 Sheet 48 of 62



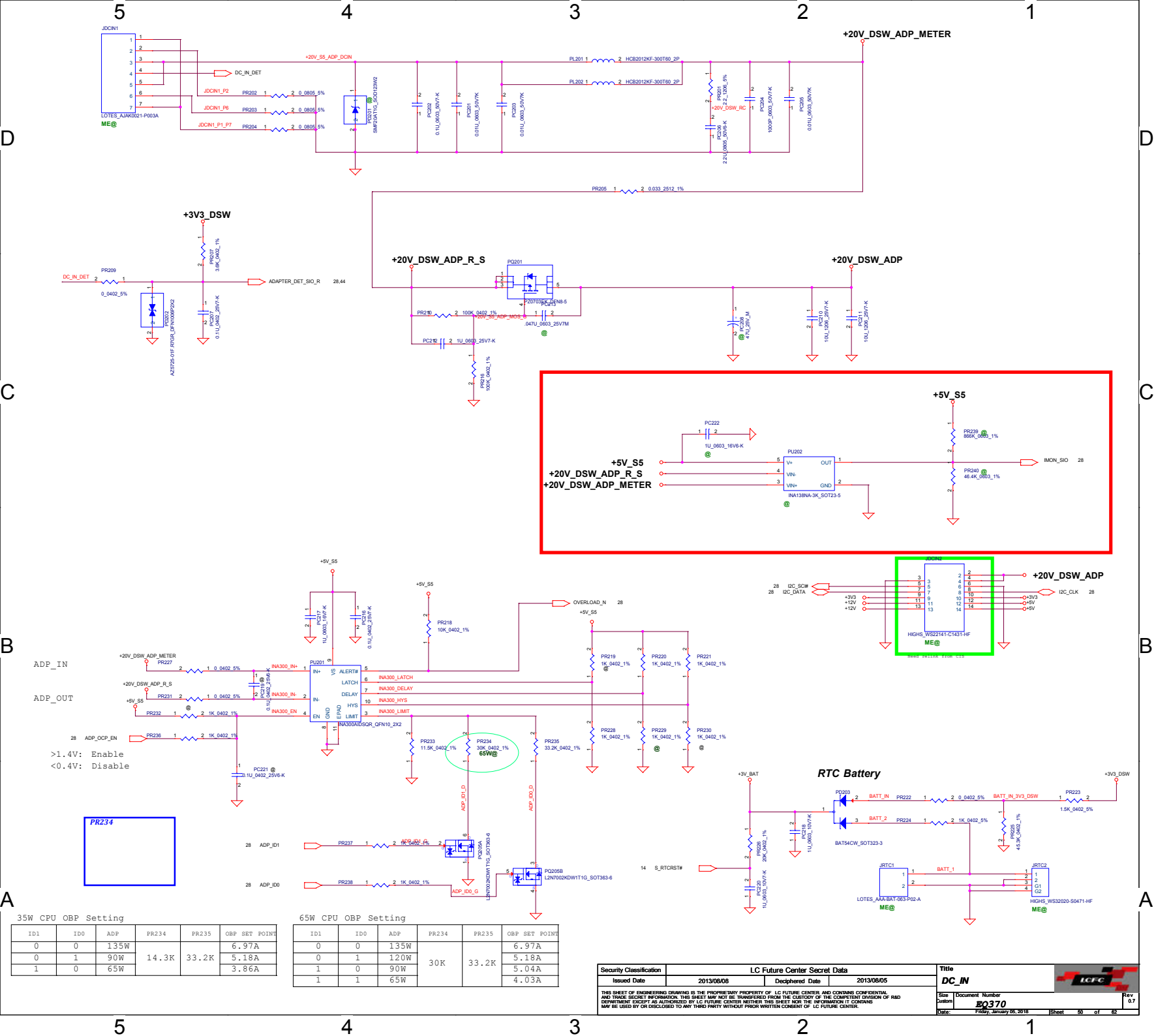
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: **Power Diagram**

Size	Document Number	Rev
D	BQ370	0.7

Date: Friday, January 05, 2018 Sheet 49 of 62



35W CPU OBP Setting

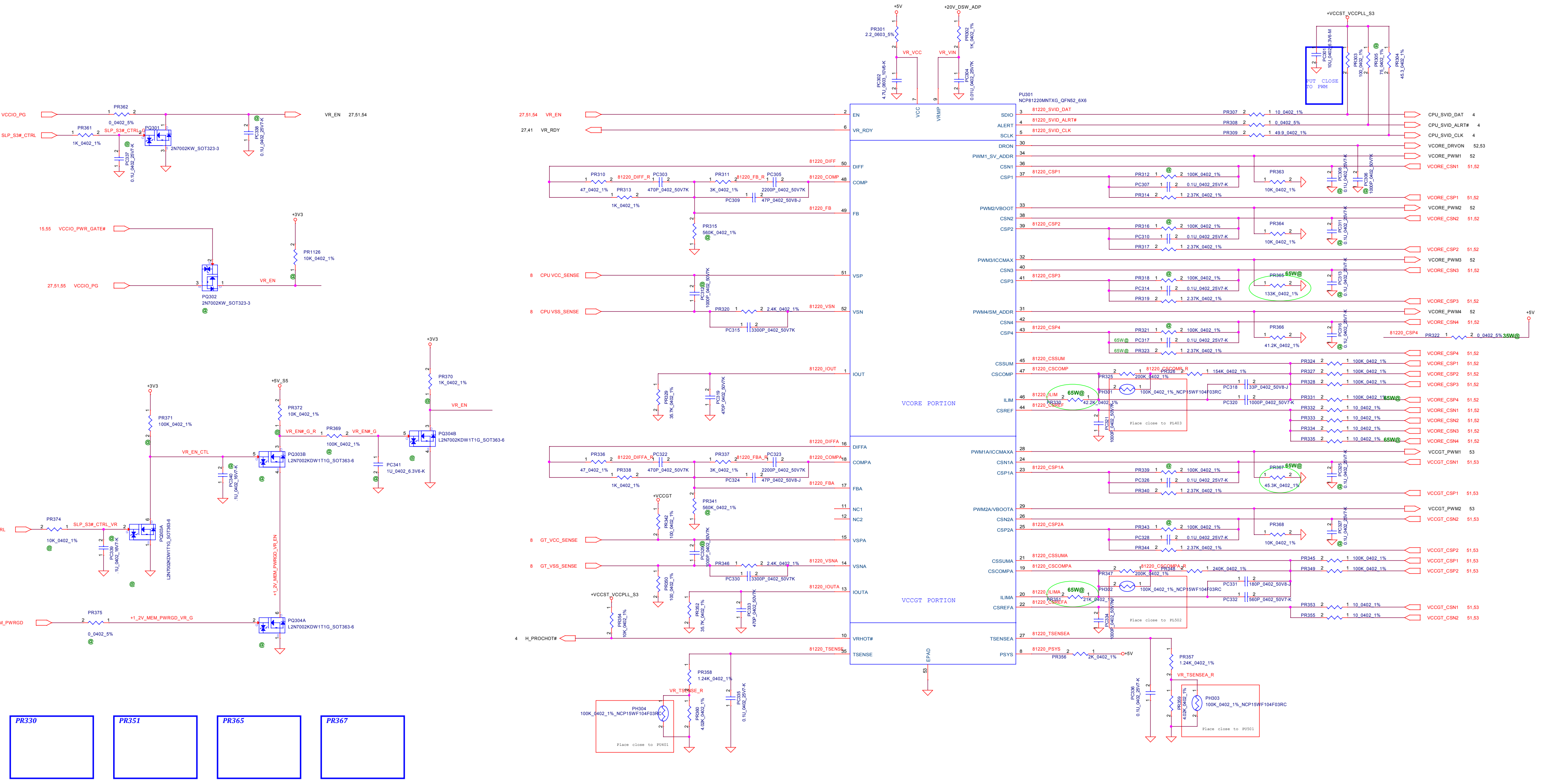
ID1	ID0	ADP	PR234	PR235	OBP SET POINT
0	0	135W	14.3K	33.2K	6.97A
0	1	90W			5.18A
1	0	65W			3.86A

65W CPU OBP Setting

ID1	ID0	ADP	PR234	PR235	OBP SET POINT
0	0	135W	30K	33.2K	6.97A
0	1	120W			5.18A
1	0	90W			5.04A
1	1	65W			4.03A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

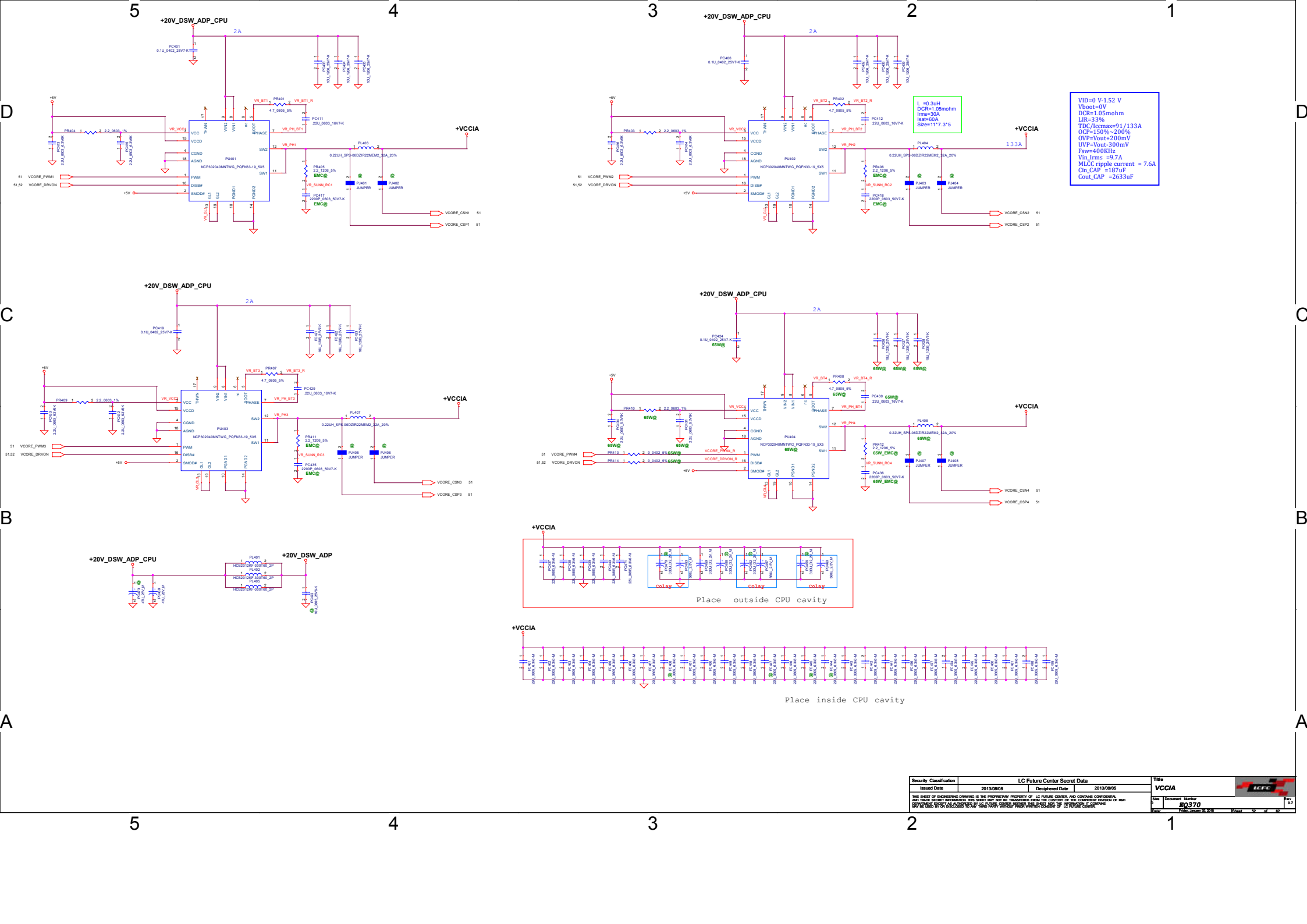
Title	DC_IN		
Size	Document Number		Rev
Custom	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet	50 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: CPU_CORE IC

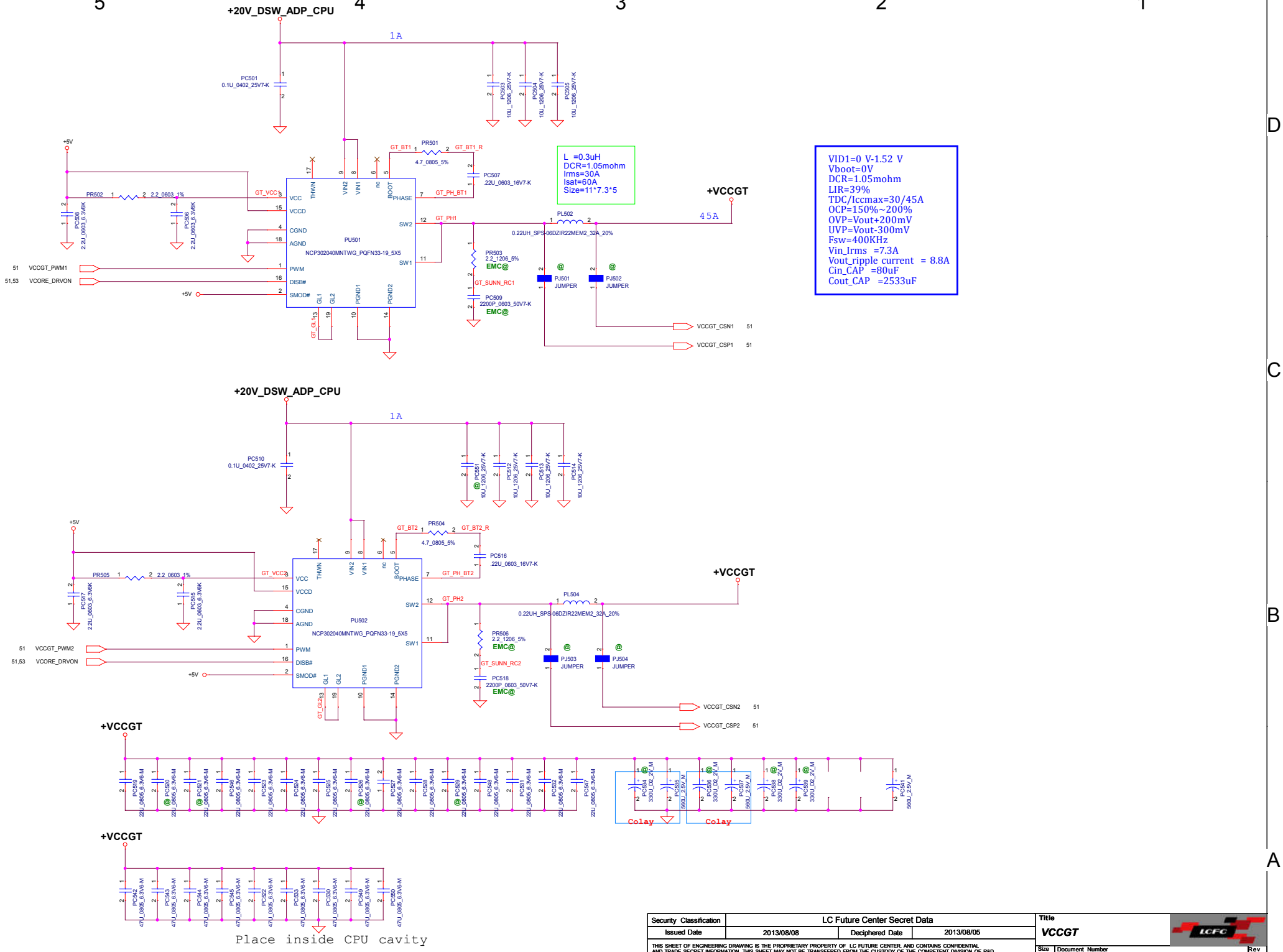
Size: D | Document Number: EQ370 | Rev: 0.7



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

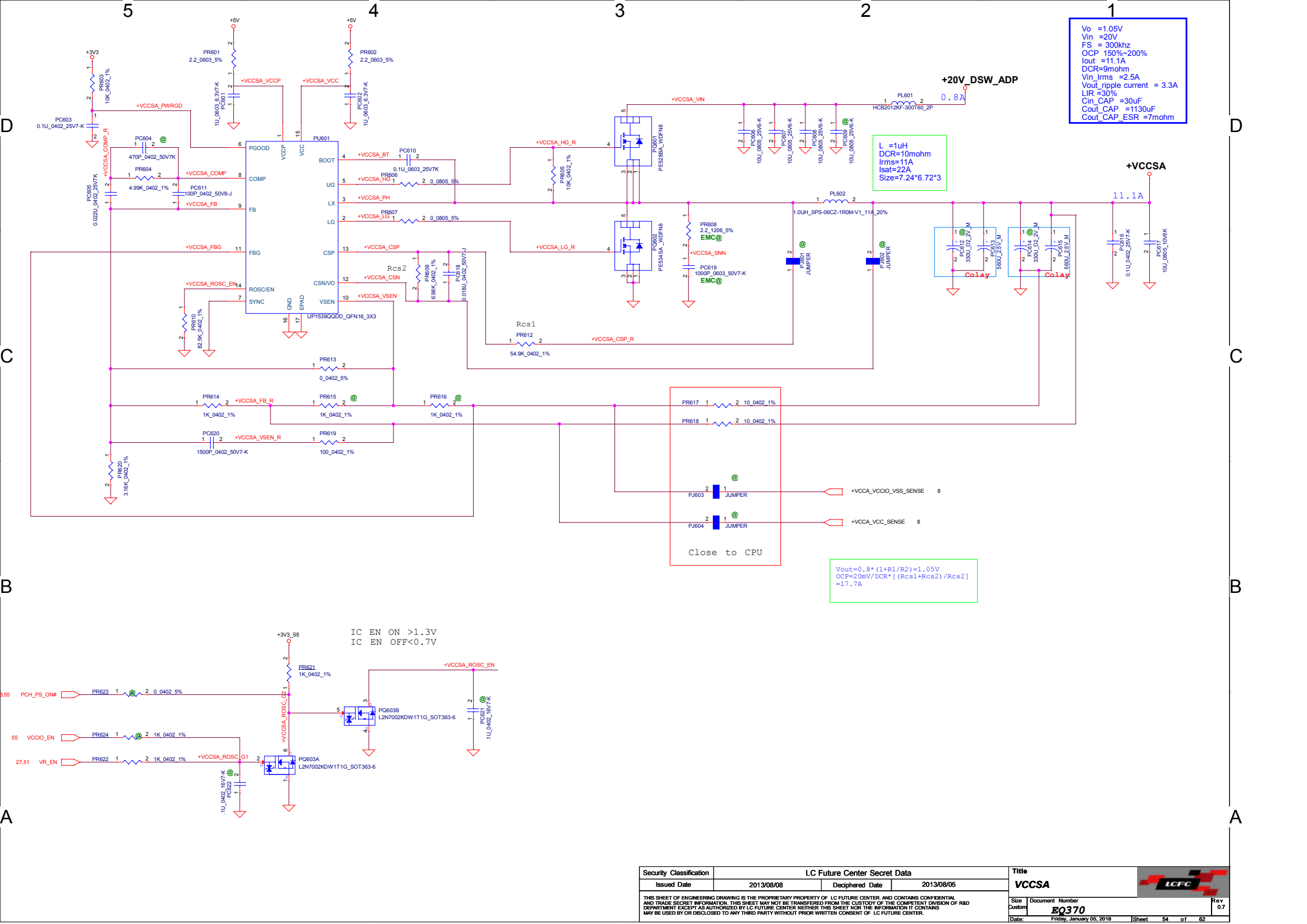
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	VCCIA		
Size	Document Number		Rev
D	BQ370		0.7
Date:	Friday, January 05, 2018	Sheet	52 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

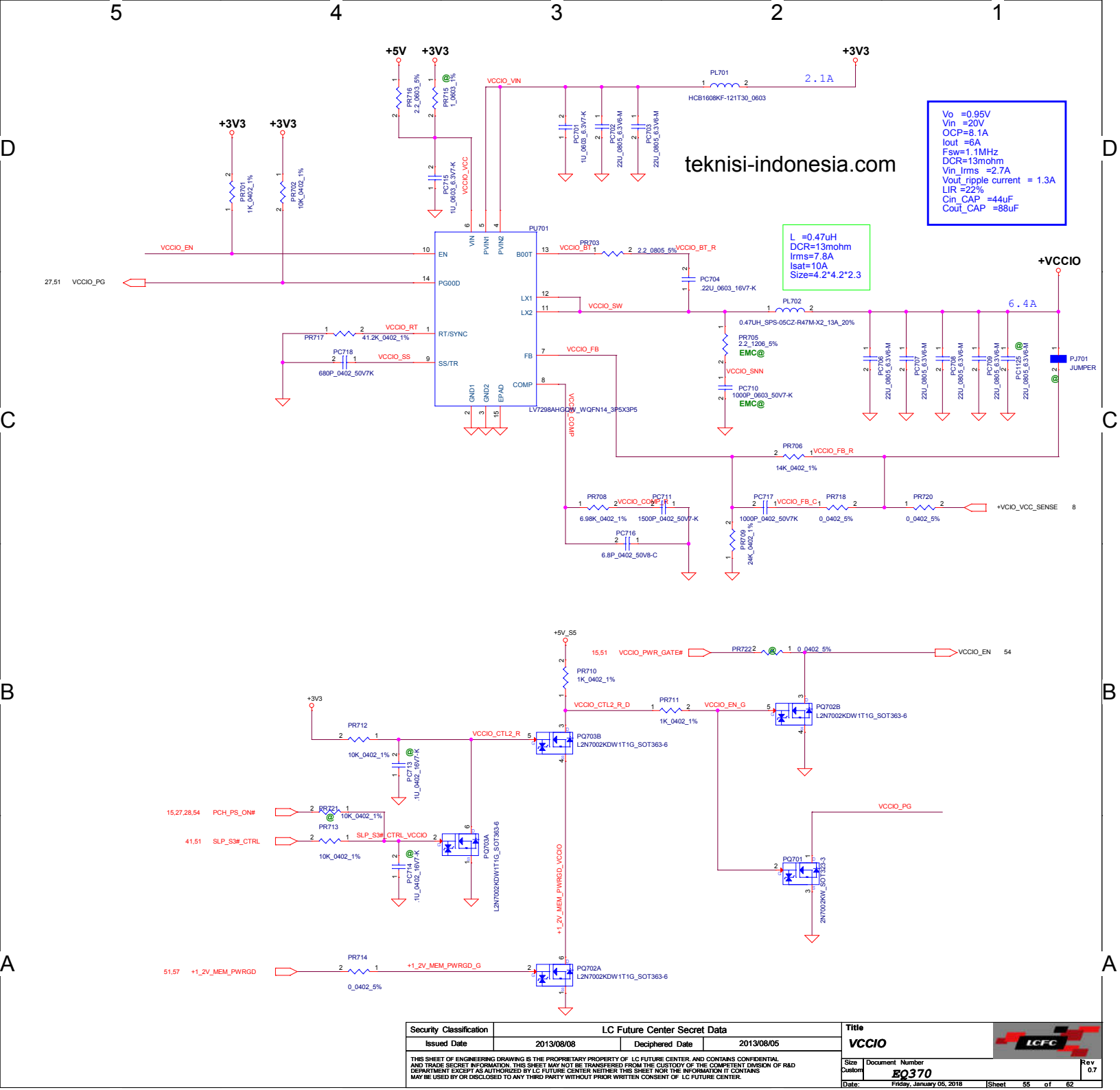
Title	VCCGT		
Size	Document Number		Rev
C	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet	53 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

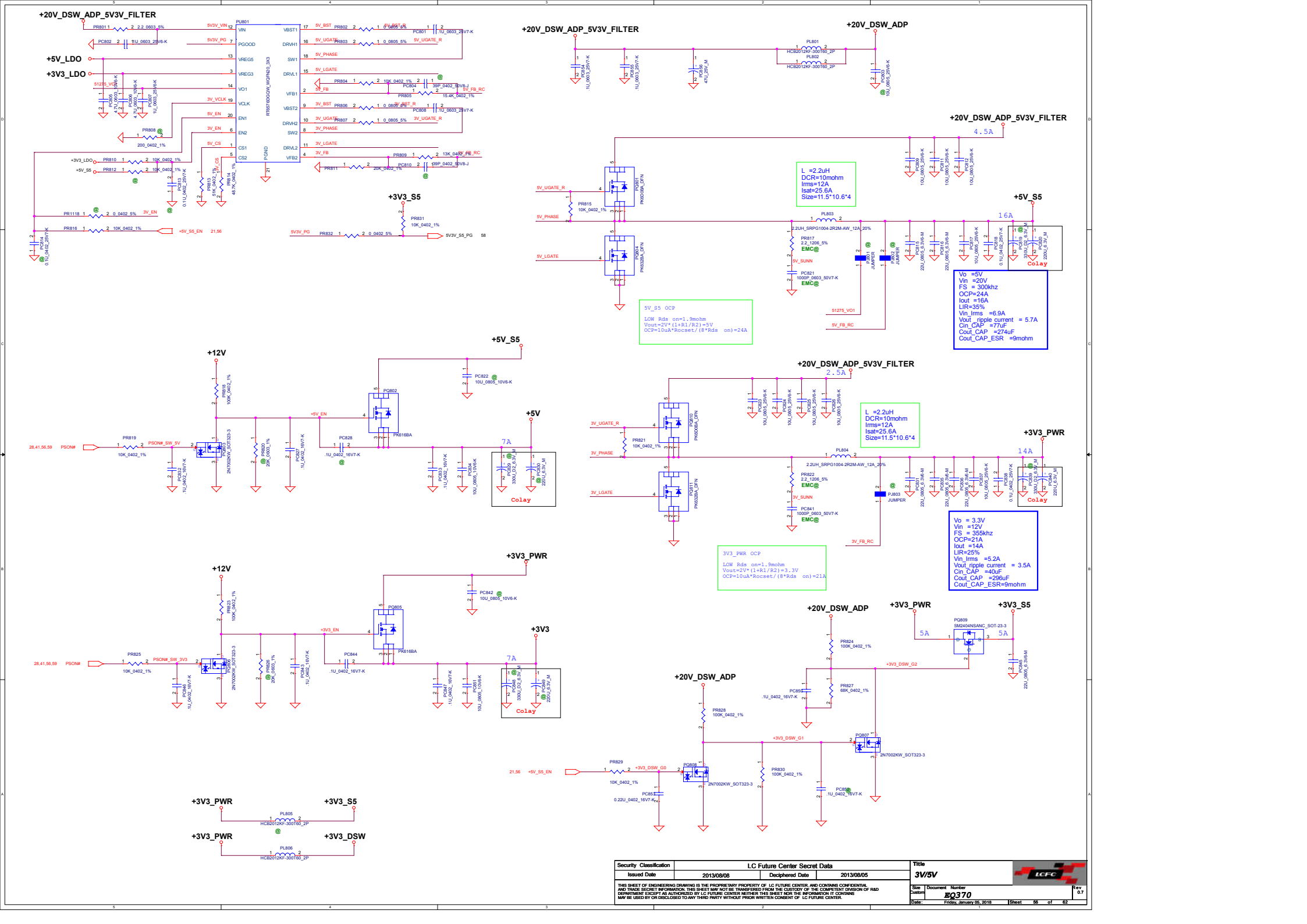
Title	VCCSA		
Size	Document Number		Rev
Custom	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet	54 of 62

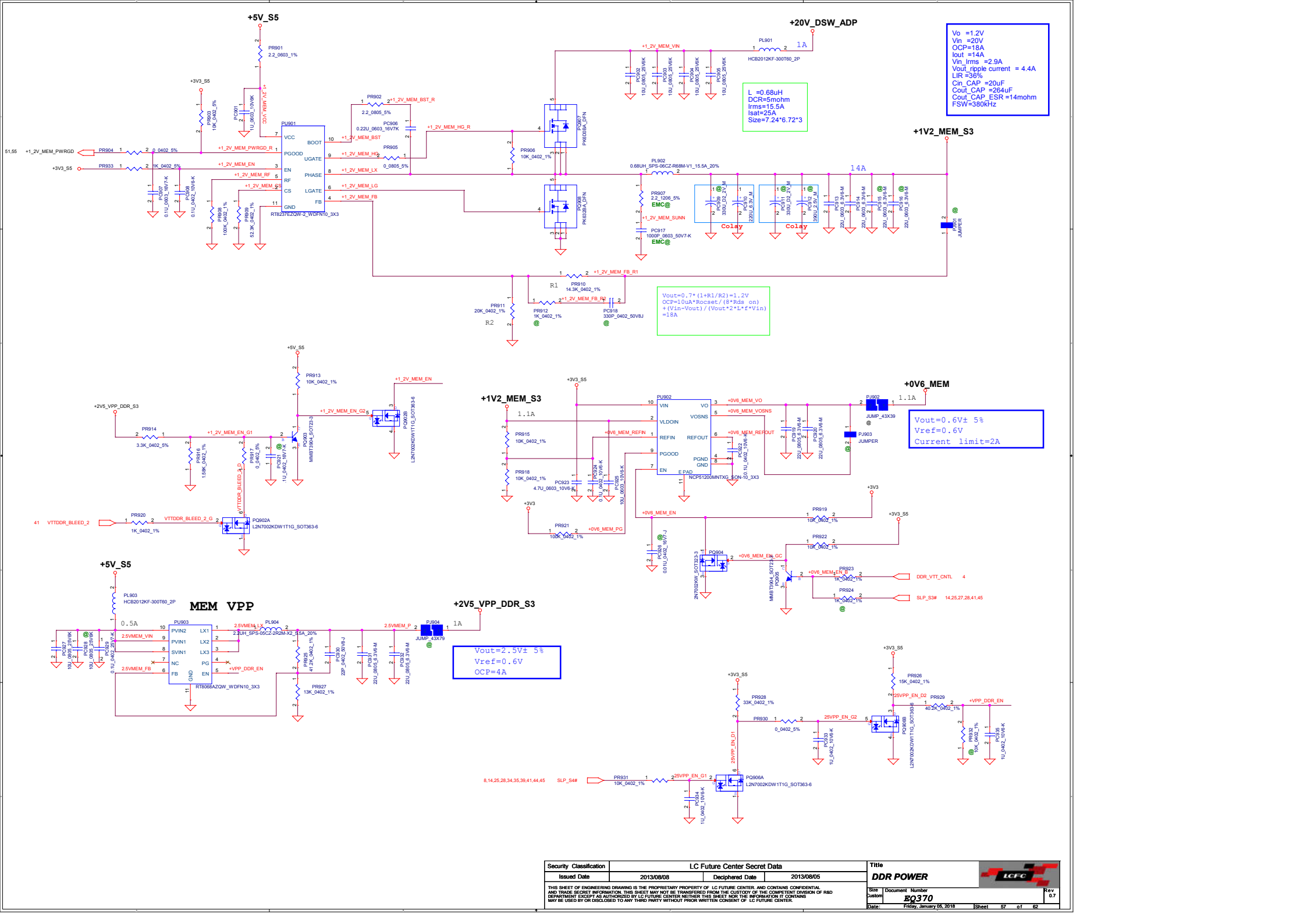


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: VCCIO

Size: Custom	Document Number: EQ370	Rev: 0.7
Date: Friday, January 05, 2018	Sheet 55 of 62	


+20V_DSW_ADP_5V3V_FILTER
+5V_LDO
+3V3_LDO
PU801
RT8576DGQW_WQFN20_3X3
VIN
PGOOD
VREG5
VREG3
VO1
VCLK
EN1
EN2
CS1
CS2
PGND
VBST1
DRVH1
SW1
DRVL1
VFB1
VBST2
DRVH2
SW2
DRVL2
VFB2
5V_BST
5V_UGATE_R
5V_PHASE
5V_LGATE
5V_FB
5V_FB_RC
3V_BST_R
3V_UGATE_R
3V_PHASE
3V_LGATE
3V_FB
3V_FB_RC
5V3V_VIN
5V3V_PG
3V_VCLK
5V_EN
3V_EN
5V_CS
3V_CS
+3V3_S5
+5V_S5
+5V_S5_EN
5V3V_S5_PG
+20V_DSW_ADP
+20V_DSW_ADP_5V3V_FILTER
4.5A
L =2.2uH
DCR=10mohm
Irms=12A
Isat=25.6A
Size=11.5*10.6*4
Vo =5V
Vin =20V
FS = 300khz
OCP=24A
Iout =16A
LIR=35%
Vin_Irms =6.9A
Vout_ripple current = 5.7A
Cin_CAP =77uF
Cout_CAP =274uF
Cout_CAP_ESR =9mohm
5V_S5 OCP
LOW Rds on=1.9mohm
Vout=2V*(1+R1/R2)=5V
OCP=10uA*Rocset/(8*Rds on)=24A
+12V
+5V
2.5A
Vo = 3.3V
Vin =12V
FS = 355khz
OCP=21A
Iout =14A
LIR=25%
Vin_Irms =5.2A
Vout_ripple current = 3.5A
Cin_CAP =40uF
Cout_CAP =296uF
Cout_CAP_ESR=9mohm
3V3_PWR OCP
LOW Rds on=1.9mohm
Vout=2V*(1+R1/R2)=3.3V
OCP=10uA*Rocset/(8*Rds on)=21A
+3V3_PWR
+3V3
+3V3_DSW
+3V3_DSW_G0
+3V3_DSW_G1
+3V3_DSW_G2
+3V3_EN
+5V_EN
PSON#
PSON#_SW_5V
PSON#_SW_3V3
+5V_S5_EN
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
3V/5V
Size
Custom
Document Number
EQ370
Rev
0.7
Date:
Friday, January 05, 2018
Sheet
56
of
62

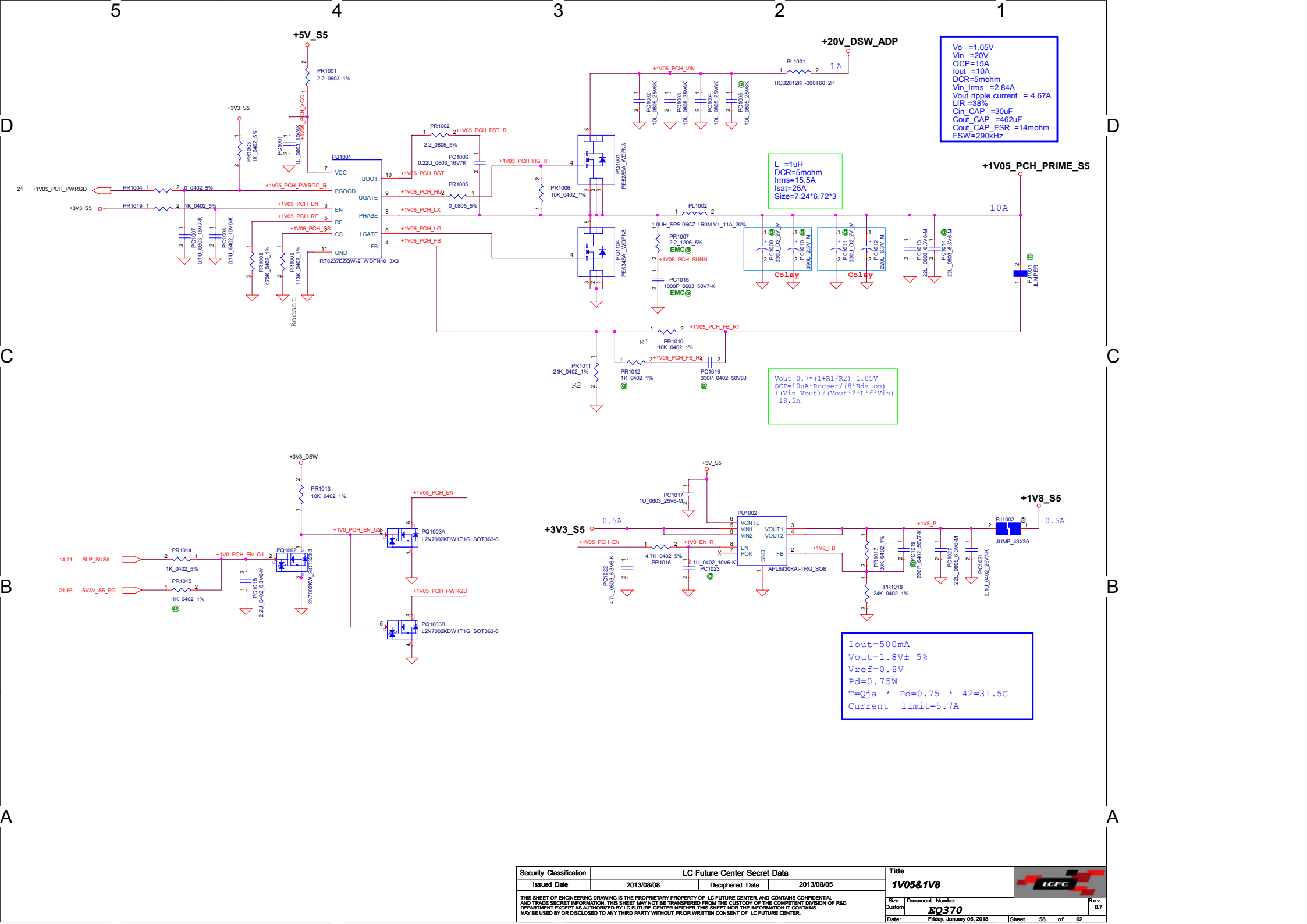


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

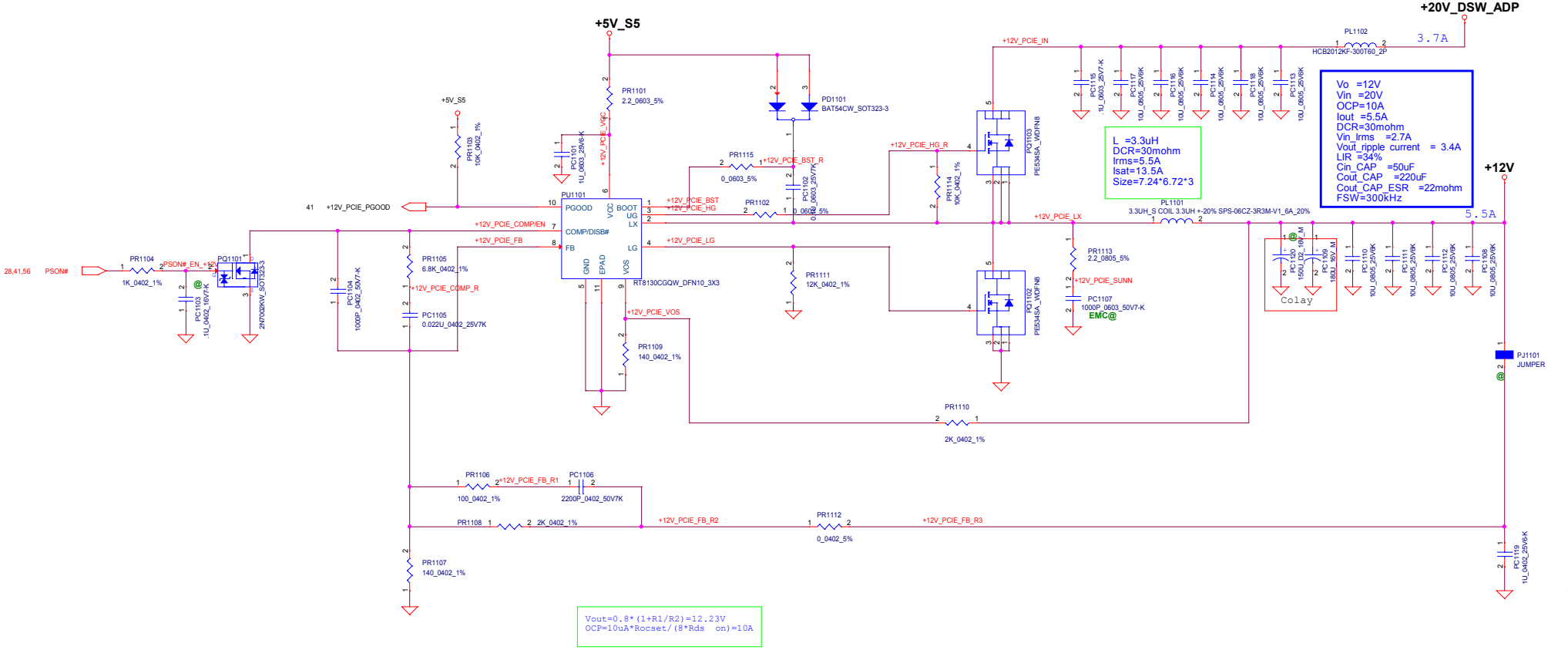
Title: **DDR POWER**

Size	Document Number	Rev
Custom	EQ370	0.7
Date: Friday, January 05, 2018	Sheet 57 of 62	



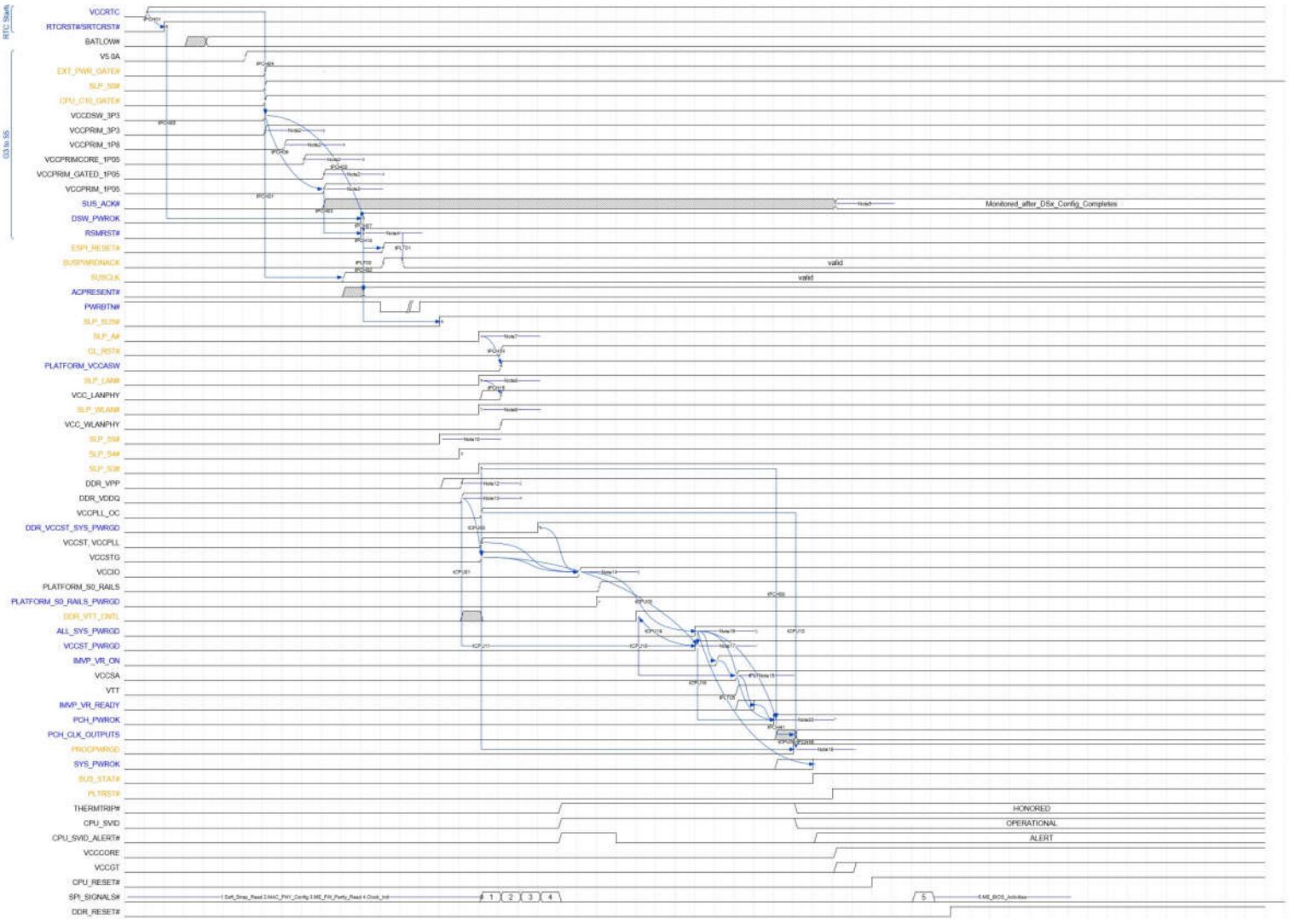
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	1V05&1V8		
Size	Document Number		Rev
Custom	EQ370		0.7
Date:	Friday, January 05, 2018	Sheet	58 of 62



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title			
12V_PCIE			
Size: C	Document Number: EQ370		Rev: 0.7
Date: Friday, January 05, 2018	Sheet 59 of 62		



with Deep Sx support

source	destination		G3	DEEP S5	S0
board	PCH	VBAT			
board	PCH	RTCRST#			
PSU	board	+5VSB_DSW			
board	PCH	+3VSB_DSW			
board	PCH	PCH_DPWROK			
PCH	SIO	PCH_SUSWARN#			
SIO	PCH	PCH_SUSACK#			
PCH	SIO	SLP_SUS#			
board	board	+5V_S5			
board	PCH	+3V3_S5			
board	PCH	+1V0_PCH			
SIO	PCH	RSMRST#			

Security Classification	LC Future Center Secret Data	Title	POWER Sequence
Issued Date	2015/08/20 Deciphered Date 2016/08/20		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D EXCEPT AS AUTHORIZED BY LC FUTURE CENTER MANAGEMENT AND NEITHER IT NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.		Size / Custom	Document Number: BQ370	Rev: 0.7
		Date: Friday, January 06, 2017	Sheet 60 of 65

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_A0	GPP_A0_RCIN_N_ESPI_ALERT1_N	SB3V	Native	KBRST#
GPP_A1	GPP_A1_LAD0_ESPI_IO0	SB3V	Native	LPC_AD0
GPP_A2	GPP_A2_LAD1_ESPI_IO1	SB3V	Native	LPC_AD1
GPP_A3	GPP_A3_LAD2_ESPI_IO2	SB3V	Native	LPC_AD2
GPP_A4	GPP_A4_LAD3_ESPI_IO3	SB3V	Native	LPC_AD3
GPP_A5	GPP_A5_LFRAME_N_ESPI_CS_N	SB3V	Native	LPC_FRAME#
GPP_A6	GPP_A6_SERIRQ	SB3V	Native	LPC_SERIRQ
GPP_A7	GPP_A7_PIRQA_N_ESPI_ALERT0_N	SB3V	Native	LPC_DRQ#0
GPP_A8	GPP_A8_CLKRUN_N	SB3V	Native	CLKRUN#
GPP_A9	GPP_A9_CLKOUT_LPC0_ESPI_CLK	SB3V	Native	LEO_CHIP_CLK
GPP_A10	GPP_A10_CLKOUT_LPC1	SB3V	Native	PCI_CLK_24M
GPP_A11	GPP_A11_PME_N	SB3V	Native	SIO_PME#
GPP_A12	GPP_A12_BMBUSY_N	SB3V	Native	BMBUSY#
GPP_A13	GPP_A13_SUSWARN_N_SUSPWRDNACK	SB3V	Native	PCH_SUSWARN#
GPP_A14	GPP_A14_SUS_STAT_N_ESPI_RST_N	SB3V	Native	SUS_STAT#
GPP_A15	GPP_A15_SUSACK_N	SB3V	Native	PCH_SUSACK#
GPP_A16	GPP_A16_CLKOUT_48	SB3V	Native	N.C
GPP_A17	GPP_A17_ISH_GP7	SB3V	OUT	BT_DISABLE_N
GPP_A18	GPP_A18_ISH_GP0	SB3V	IN	OE#
GPP_A19	GPP_A19_ISH_GP1	SB3V	Native	N.C
GPP_A20	GPP_A20_ISH_GP2	SB3V	OUT	SEL#
GPP_A21	GPP_A21_ISH_GP3	SB3V	IN	WLAN_DETECT_N
GPP_A22	GPP_A22_ISH_GP4	SB3V	IN	COM_GPIO1
GPP_A23	GPP_A23_ISH_GP5	SB3V	IN	LEO_CHIP_GPIO
GPP_B0	GPP_B0	SB3V	Native	N.C
GPP_B1	GPP_B1	SB3V	Native	N.C
GPP_B2	GPP_B2_VRALERT_N	SB3V	Native	PCH_VRALERT#
GPP_B3	GPP_B3_CPU_GP2	SB3V	Native	N.C
GPP_B4	GPP_B4_CPU_GP3	SB3V	Native	N.C
GPP_B5	GPP_B5_SRCCLKREQ0_N	SB3V	IN	PCIEX16_PRSNT2_R2_N
GPP_B6	GPP_B6_SRCCLKREQ1_N	SB3V	Native	PCIECLKREQ1#
GPP_B7	GPP_B7_SRCCLKREQ2_N	SB3V	IN	PCIEX4_SLOT3_PRSNT2_R_N
GPP_B8	GPP_B8_SRCCLKREQ3_N	SB3V	IN	CLK_REQ1_M.2_WLAN_N
GPP_B9	GPP_B9_SRCCLKREQ4_N	SB3V	Native	CLK_REQ1_M.2_SSD#
GPP_B10	GPP_B10_SRCCLKREQ5_N	SB3V	Native	N.C
GPP_B11	GPP_B11	SB3V	Native	N.C
GPP_B12	GPP_B12_SLP_S0_N	SB3V	Native	SLP_S0#
GPP_B13	GPP_B13_PLTRST_N	SB3V	Native	PLTRST#
GPP_B14	GPP_B14_SPKR	SB3V	Native	SPKR
GPP_B15	GPP_B15_GSPI0_CS_N	SB3V	Native	N.C
GPP_B16	GPP_B16_GSPI0_CLK	SB3V	Native	N.C
GPP_B17	GPP_B17_GSPI0_MISO	SB3V	Native	N.C
GPP_B18	GPP_B18_GSPI0_MOSI	SB3V	Native	REBOOT_STRAP
GPP_B19	GPP_B19_GSPI1_CS_N	SB3V	Native	N.C
GPP_B20	GPP_B20_GSPI1_CLK	SB3V	IN	SMI#
GPP_B21	GPP_B21_GSPI1_MISO	SB3V	Native	N.C
GPP_B22	GPP_B22_GSPI1_MOSI	SB3V	IN	BBS_STRAP
GPP_B23	GPP_B23_SML1ALERT_N_PCHHOT_N	SB3V	IN	SMLINK1_ALERT_N
GPP_C0	GPP_C0_SMBCLK	SB3V	Native	SMBCLK_R
GPP_C1	GPP_C1_SMBDATE	SB3V	Native	SMBDATA_R
GPP_C2	GPP_C2_SMBALERT_N	SB3V	Native	TLS_STRAP
GPP_C3	GPP_C3_SML0CLK	SB3V	Native	SML0_CLK
GPP_C4	GPP_C4_SML0DATA	SB3V	Native	SML0_DATA
GPP_C5	GPP_C5_SML0ALERT_N	SB3V	Native	ESPI_STRAP
GPP_C6	GPP_C6_SML1CLK	SB3V	Native	SML1_CLK
GPP_C7	GPP_C7_SML1DATA	SB3V	Native	SML1_DATA
GPP_C8	GPP_C8_UART0_RXD	SB3V	IN	CLR_CMOS
GPP_C9	GPP_C9_UART0_TXD	SB3V	Native	N.C
GPP_C10	GPP_C10_UART0_RTS	SB3V	Native	IBUTTON
GPP_C11	GPP_C11_UART0_CTS_N	SB3V	Native	N.C
GPP_C12	GPP_C12_UART1_RXD_ISH_UART1_RXD	SB3V	IN	PCH_GPIO22
GPP_C13	GPP_C13_UART1_TXD_ISH_UART1_TXD	SB3V	IN	PCH_GPIO23
GPP_C14	GPP_C14_UART1_RTS_N_ISH_UART1_RTS	SB3V	IN	PCH_GPIO21
GPP_C15	GPP_C15_UART1_CTS_N_ISH_UART1_CTS	SB3V	OUT	WLAN_DISABLE_N
GPP_C16	GPP_C16_I2C0_SDA	SB3V	Native	N.C
GPP_C17	GPP_C17_I2C0_SCL	SB3V	Native	N.C
GPP_C18	GPP_C18_I2C1_SDA	SB3V	Native	N.C
GPP_C19	GPP_C19_I2C1_SCL	SB3V	Native	N.C
GPP_C20	GPP_C20_UART2_RXD	SB3V	Native	N.C
GPP_C21	GPP_C21_UART2_TXD	SB3V	Native	N.C
GPP_C22	GPP_C22_UART2_RTS_N	SB3V	Native	N.C
GPP_C23	GPP_C23_UART2_CTS_N	SB3V	Native	N.C

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_D0	GPP_D0_SPI1_CS_N	SB3V	Native	N.C
GPP_D1	GPP_D1_SPI1_CLK	SB3V	OUT	PW_LED_N
GPP_D2	GPP_D2_SPI1_MISO	SB3V	IN	PD_PCH_GPP_D_2
GPP_D3	GPP_D3_SPI1_MOSI	SB3V	IN	PD_PCH_GPP_D_3
GPP_D4	GPP_D4_ISH_I2C2_SDA	SB3V	OUT	SUS_LED_N
GPP_D5	GPP_D5_SSP0_SFRM	SB3V	Native	N.C
GPP_D6	GPP_D6_SSP0_TXD	SB3V	Native	N.C
GPP_D7	GPP_D7_SSP0_RXD	SB3V	Native	N.C
GPP_D8	GPP_D8_SSP0_SCLK	SB3V	Native	N.C
GPP_D9	GPP_D9_ISH_SPI_CS_N	SB3V	Native	N.C
GPP_D10	GPP_D10_ISH_SPI_CLK	SB3V	Native	N.C
GPP_D11	GPP_D11_ISH_SPI_MISO	SB3V	IN	FUSB_G1
GPP_D12	GPP_D12_ISH_SPI_MOSI	SB3V	IN	FUSB_G2
GPP_D13	GPP_D13_ISH_UART0_RXD	SB3V	IN	FUSB_G3
GPP_D14	GPP_D14_ISH_UART0_TXD	SB3V	IN	PS2_PINHEADER_N
GPP_D15	GPP_D15_ISH_UART0_RTS_N	SB3V	IN	LPT_DET#
GPP_D16	GPP_D16_ISH_UART0_CTS_N	SB3V	Native	N.C
GPP_D17	GPP_D17_DMIC_CLK1	SB3V	Native	COM_WAKE#
GPP_D18	GPP_D18_DMIC_DATA1	SB3V	IN	PCH_GPIO_D18
GPP_D19	GPP_D19_DMIC_CLK0	SB3V	Native	N.C
GPP_D20	GPP_D20_DMIC_DATA0	SB3V	Native	N.C
GPP_D21	GPP_D21_SPI1_IO2	SB3V	Native	N.C
GPP_D22	GPP_D22_SPI1_IO3	SB3V	Native	N.C
GPP_D23	GPP_D23_ISH_I2C2_SCL	SB3V	Native	N.C
GPP_E0	GPP_E0_SATAXPCIE0_SATAGP	SB3V	Native	N.C
GPP_E1	GPP_E1_SATAXPCIE1_SATAGP1	SB3V	Native	N.C
GPP_E2	GPP_E2_SATAXPCIE2_SATAGP2	SB3V	Native	N.C
GPP_E3	GPP_E3_CPU_GP0	SB3V	Native	BMC_PCH_SCI_N
GPP_E4	GPP_E4_DEVSLP0	SB3V	Native	BMC_FORCE_SMI_N
GPP_E5	GPP_E5_DEVSLP1	SB3V	Native	N.C
GPP_E6	GPP_E6_DEVSLP2	SB3V	Native	N.C
GPP_E7	GPP_E7_CPU_GP1	SB3V	Native	N.C
GPP_E8	GPP_E8_SATALED_N	SB3V	OUT	SATA_LED#
GPP_E9	GPP_E9_USB2_OC0_N	SB3V	Native	USB_OCP#0
GPP_E10	GPP_E10_USB2_OC1_N	SB3V	Native	USB_OCP#1
GPP_E11	GPP_E11_USB2_OC2_N	SB3V	Native	USB_OCP#2
GPP_E12	GPP_E12_USB2_OC3_N	SB3V	Native	USB_OCP#3
GPP_F0	GPP_F17_USB2_OCB_6	SB3V	Native	PCH_GPIO_F1
GPP_F1	GPP_F1_SATAXPCIE4_SATAGP4	SB3V	IN	M.2_SSD1_PEDET#
GPP_F2	GPP_F2_SATAXPCIE5_SATAGP5	SB3V	Native	PCH_GPIO_F2
GPP_F3	GPP_F3_SATAXPCIE6_SATAGP6	SB3V	Native	N.C
GPP_F4	GPP_F4_SATAXPCIE7_SATAGP7	SB3V	Native	TP20
GPP_F5	GPP_F5_DEVSLP3	SB3V	IN	SPI_SIRQ#
GPP_F6	GPP_F6_DEVSLP4	SB3V	Native	PCH_GPIO_F6
GPP_F7	GPP_F7_DEVSLP5	SB3V	Native	SSD1_SATA_DEVSLP
GPP_F8	GPP_F8_DEVSLP6	SB3V	Native	N.C
GPP_F9	GPP_F9_DEVSLP7	SB3V	Native	USB_DISABLE#
GPP_F10	GPP_F10_SCLOCK	SB3V	OUT	N.C
GPP_F11	GPP_F11_SLOAD	SB3V	OUT	N.C
GPP_F12	GPP_F12_SDATAOUT1	SB3V	OUT	N.C
GPP_F13	GPP_F13_SDATAOUT0	SB3V	OUT	N.C
GPP_F14	GPP_F14	SB3V	IN	SKTOCC#
GPP_F15	GPP_F15_USB2_OCB_4	SB3V	Native	USB_OCP#4
GPP_F16	GPP_F16_USB2_OCB_5	SB3V	Native	USB_OCP#5
GPP_F17	GPP_F17_USB2_OCB_8	SB3V	Native	USB_OCP#8
GPP_F18	GPP_F18_USB2_OCB_7	SB3V	Native	USB_OCP#7
GPP_F19	GPP_F19_EDP_VDDEN	SB3V	Native	N.C
GPP_F20	GPP_F20_EDP_BKLTEN	SB3V	Native	N.C
GPP_F21	GPP_F21_EDP_BKLTCTL	SB3V	Native	N.C
GPP_F22	GPP_F22	SB3V	OUT	PCH_GPIO_F22
GPP_F23	GPP_F23	SB3V	Native	N.C
GPD0	GPD0_BATLOW_N	SB3V_DSW	Native	PCH_BATLOW#
GPD1	GPD1_ACPRESENT	SB3V_DSW	OUT	SUS_LED_N
GPD2	GPD2_LAN_WAKE_N	SB3V_DSW	Native	LAN_WAKE#_C
GPD3	GPD3_PWRBTN_N	SB3V_DSW	Native	PWRBTN#
GPD4	GPD4_SLP_S3_N	SB3V_DSW	Native	SLP_S3#
GPD5	GPD5_SLP_S4_N	SB3V_DSW	Native	SLP_S4#
GPD6	GPD5_SLP_A_	SB3V_DSW	Native	PCH_SLP_A#
GPD7	GPD7_USB2_WAKEOUT_N	SB3V_DSW	Native	N.C
GPD8	GPD8_SUSCL	SB3V_DSW	Native	SUSCLK
GPD9	GPD9_SLP_WLAN_N	SB3V_DSW	Native	N.C
GPD10	GPD10_SLP_S5_N	SB3V_DSW	Native	SLP_S5#
GPD11	GPD11_LANPHYPC	SB3V_DSW	Native	LAN_DISABLE#

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_G0	GPP_G0_FAN_TACH_0	SB3V	IN	CHASSIS_ID1
GPP_G1	GPP_G1_FAN_TACH_1	SB3V	IN	CHASSIS_ID2
GPP_G2	GPP_G2_FAN_TACH_2	SB3V	IN	H_PROCHOT_PCH_N
GPP_G3	GPP_G3_FAN_TACH_3	SB3V	Native	PCH_BMC_FOURCE_INT_N
GPP_G4	GPP_G4_FAN_TACH_4	SB3V	Native	N.C
GPP_G5	GPP_G5_FAN_TACH_5	SB3V	Native	N.C
GPP_G6	GPP_G6_FAN_TACH_6	SB3V	Native	N.C
GPP_G7	GPP_G7_FAN_TACH_7	SB3V	Native	N.C
GPP_G8	GPP_G8_FAN_PWM_0	SB3V	Native	N.C
GPP_G9	GPP_G9_FAN_PWM_1	SB3V	Native	N.C
GPP_G10	GPP_G10_FAN_PWM_2	SB3V	Native	N.C
GPP_G11	GPP_G11_FAN_PWM_3	SB3V	IN	BMC_THROTTLE_N
GPP_G12	GPP_G12_GSXDOUT	SB3V	IN	GPP_G0
GPP_G13	GPP_G13_GSXSLOAD	SB3V	IN	GPP_G1
GPP_G14	GPP_G14_GSXDIN	SB3V	IN	GPP_G2
GPP_G15	GPP_G15_GSXSRESET_N	SB3V	IN	GPP_G3
GPP_G16	GPP_G16_GSXCLK	SB3V	IN	GPP_G4
GPP_G17	GPP_G17_ADR_COMPLETE	SB3V	IN	GPP_G5
GPP_G18	GPP_G18_NMI_N	SB3V	Native	FM_NMI_EVENT_N
GPP_G19	GPP_G19_SMI_N	SB3V	IN	SIO_SCI_N
GPP_G20	GPP_G20	SB3V	Native	BMC_READY
GPP_G21	GPP_G21	SB3V	IN	PCH_GPIO20
GPP_G22	GPP_G22	SB3V	Native	BMC_CARD_DET_R_N
GPP_G23	GPP_G23	SB3V	OUT	VGA_URDBG
GPP_H0	GPP_H0_SRCCLKREQ6_N	SB3V	Native	FM_MEM_THERM_EVENT_LVT3_N
GPP_H1	GPP_H1_SRCCLKREQ7_N	SB3V	Native	FM_NM_THROTTLE_N
GPP_H2	GPP_H2_SRCCLKREQ8_N	SB3V	OUT	FM_CATERR_N
GPP_H3	GPP_H3_SRCCLKREQ9_N	SB3V	Native	PCH_BMC_ALERT
GPP_H4	GPP_H4_SRCCLKREQ10_N	SB3V	Native	N.C
GPP_H5	GPP_H5_SRCCLKREQ11_N	SB3V	Native	N.C
GPP_H6	GPP_H6_SRCCLKREQ12_N	SB3V	Native	N.C
GPP_H7	GPP_H7_SRCCLKREQ13_N	SB3V	Native	N.C
GPP_H8	GPP_H8_SRCCLKREQ14_N	SB3V	Native	N.C
GPP_H9	GPP_H9_SRCCLKREQ15_N	SB3V	Native	N.C
GPP_H10	GPP_H10_SML2CLK	SB3V	OUT	WIRELESS_EN2
GPP_H11	GPP_H11_SML2DATA	SB3V	OUT	WIRELESS_EN
GPP_H12	GPP_H12_SML2ALERT_N	SB3V	Native	FM_ESPI_FLASH_MODE
GPP_H13	GPP_H13_SML3CLK	SB3V	Native	N.C
GPP_H14	GPP_H14_SML3DATA	SB3V	Native	N.C
GPP_H15	GPP_H15_SML3ALERT_N	SB3V	Native	PCH_GPP_H15
GPP_H16	GPP_H16_SML4CLK	SB3V	Native	N.C
GPP_H17	GPP_H17_SML4DATA	SB3V	Native	N.C
GPP_H18	GPP_H18_SML4ALERT_N	SB3V	Native	PCH_GPP_H18
GPP_H19	GPP_H19_ISH_I2C0_SDA	SB3V	Native	N.C
GPP_H20	GPP_H20_ISH_I2C0_SCL	SB3V	Native	N.C
GPP_H21	GPP_H21_ISH_I2C1_SDA	SB3V	Native	N.C
GPP_H22	GPP_H22_ISH_I2C1_SCL	SB3V	Native	N.C
GPP_H23	GPP_H23	SB3V	Native	N.C
GPP_I0	GPP_I0_DDPB_HPD0	SB3V	IN	VGA_DDI3_HPD
GPP_I1	GPP_I1_DDPC_HPD1	SB3V	IN	DP_DDPC_HPD
GPP_I2	GPP_I2_DDPD_HPD2	SB3V	IN	DP_DDPD_HPD
GPP_I3	GPP_I3_DDPE_HPD3	SB3V	IN	U2_BA4
GPP_I4	GPP_I4_EDP_HPD	SB3V	IN	U2_BD7
GPP_I5	GPP_I5_DDPB_CTRLCLK	SB3V	Native	TP30
GPP_I6	GPP_I6_DDPB_CTRLDATA	SB3V	Native	DDPD_CTRLDATA
GPP_I7	GPP_I7_DDPC_CTRLCLK	SB3V	Native	DP_DDPC_CTRLCLK
GPP_I8	GPP_I8_DDPC_CTRLDATA	SB3V	Native	DP_DDPC_CTRLDATA
GPP_I9	GPP_I9_DDPD_CTRLCLK	SB3V	Native	DP_DDPD_CTRLCLK
GPP_I10	GPP_I10_DDPD_CTRLDATA	SB3V	Native	DP_DDPD_CTRLDATA

SIO GPIO (NCT6685D)

GPIO	Signal Name	PIN	Power We	In/Out	Usage
GPIO00	PWMOUT/TACHIN/GPIO00	3	SB3V	IN	FM_CATERR_N
GPIO95	GPIO95/BKFD_CUT	74	SB3V	OUT	ME_CNTL
GPIO85	SMI#/OVT#/GPIO85	2	SB3V	----	SIO_SCI_N
GPIO74	GPIO74 / TACHIN / PWMOUT	37	SB3V	OD	BMC_THROTTLE_N
GPIO77	SKTOCC# / GPIO77	102	SB3V	IN	IS1X0M_BOARDID
GPIO66	P_S5_0 / 3VSBSW / LATCH_BKFD_CUT / GP	70	SB3V	OUT	USB_PS2_PON
GPIO93	3VSBSW#/GPIO93/SLP_SUS#	89	3V_DSW	OUT	SIO_GP93
GPIO94	GPIO94/SLP_SUS_FET	88	3V_DSW	IN	COM_WAKE#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **POWER Sequence**

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 | Sheet 61 of 62

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_A0	GPP_A0_RCIN_N_ESPI_ALERT1_N	SB3V	Native	KBRST#
GPP_A1	GPP_A1_LAD0_ESPI_IO0	SB3V	Native	LPC_AD0
GPP_A2	GPP_A2_LAD1_ESPI_IO1	SB3V	Native	LPC_AD1
GPP_A3	GPP_A3_LAD2_ESPI_IO2	SB3V	Native	LPC_AD2
GPP_A4	GPP_A4_LAD3_ESPI_IO3	SB3V	Native	LPC_AD3
GPP_A5	GPP_A5_LFRAME_N_ESPI_CS_N	SB3V	Native	LPC_FRAME#
GPP_A6	GPP_A6_SERIRQ	SB3V	Native	LPC_SERIRQ
GPP_A7	GPP_A7_PIRQA_N_ESPI_ALERT0_N	SB3V	Native	LPC_DRQ#0
GPP_A8	GPP_A8_CLKRUN_N	SB3V	Native	CLKRUN#
GPP_A9	GPP_A9_CLKOUT_LPC0_ESPI_CLK	SB3V	Native	LEO_CHIP_CLK
GPP_A10	GPP_A10_CLKOUT_LPC1	SB3V	Native	PCI_CLK_24M
GPP_A11	GPP_A11_PME_N	SB3V	Native	SIO_PME#
GPP_A12	GPP_A12_BMBUSY_N	SB3V	Native	BMBUSY#
GPP_A13	GPP_A13_SUSWARN_N_SUSPWRDNACK	SB3V	Native	PCH_SUSWARN#
GPP_A14	GPP_A14_SUS_STAT_N_ESPI_RST_N	SB3V	Native	SUS_STAT#
GPP_A15	GPP_A15_SUSACK_N	SB3V	Native	PCH_SUSACK#
GPP_A16	GPP_A16_CLKOUT_48	SB3V	Native	N.C
GPP_A17	GPP_A17_ISH_GP7	SB3V	OUT	BT_DISABLE_N
GPP_A18	GPP_A18_ISH_GP0	SB3V	IN	OE#
GPP_A19	GPP_A19_ISH_GP1	SB3V	Native	N.C
GPP_A20	GPP_A20_ISH_GP2	SB3V	OUT	SEL#
GPP_A21	GPP_A21_ISH_GP3	SB3V	IN	WLAN_DETECT_N
GPP_A22	GPP_A22_ISH_GP4	SB3V	IN	COM_GPIO1
GPP_A23	GPP_A23_ISH_GP5	SB3V	IN	LEO_CHIP_GPIO
GPP_B0	GPP_B0	SB3V	Native	N.C
GPP_B1	GPP_B1	SB3V	Native	N.C
GPP_B2	GPP_B2_VRALERT_N	SB3V	Native	PCH_VRALERT#
GPP_B3	GPP_B3_CPU_GP2	SB3V	Native	N.C
GPP_B4	GPP_B4_CPU_GP3	SB3V	Native	N.C
GPP_B5	GPP_B5_SRCCLKREQ0_N	SB3V	IN	PCIEX16_PRSNT2_R2_N
GPP_B6	GPP_B6_SRCCLKREQ1_N	SB3V	Native	PCIECLKREQ1#
GPP_B7	GPP_B7_SRCCLKREQ2_N	SB3V	IN	PCIEX4_SLOT3_PRSNT2_R_N
GPP_B8	GPP_B8_SRCCLKREQ3_N	SB3V	IN	CLK_REQ1_M.2_WLAN_N
GPP_B9	GPP_B9_SRCCLKREQ4_N	SB3V	Native	CLK_REQ1_M.2_SSD#
GPP_B10	GPP_B10_SRCCLKREQ5_N	SB3V	Native	N.C
GPP_B11	GPP_B11	SB3V	Native	N.C
GPP_B12	GPP_B12_SLP_S0_N	SB3V	Native	SLP_S0#
GPP_B13	GPP_B13_PLTRST_N	SB3V	Native	PLTRST#
GPP_B14	GPP_B14_SPKR	SB3V	Native	SPKR
GPP_B15	GPP_B15_GSPI0_CS_N	SB3V	Native	N.C
GPP_B16	GPP_B16_GSPI0_CLK	SB3V	Native	N.C
GPP_B17	GPP_B17_GSPI0_MISO	SB3V	Native	N.C
GPP_B18	GPP_B18_GSPI0_MOSI	SB3V	Native	REBOOT_STRAP
GPP_B19	GPP_B19_GSPI1_CS_N	SB3V	Native	N.C
GPP_B20	GPP_B20_GSPI1_CLK	SB3V	IN	SMI#
GPP_B21	GPP_B21_GSPI1_MISO	SB3V	Native	N.C
GPP_B22	GPP_B22_GSPI1_MOSI	SB3V	IN	BBS_STRAP
GPP_B23	GPP_B23_SML1ALERT_N_PCHHOT_N	SB3V	IN	SMLINK1_ALERT_N
GPP_C0	GPP_C0_SMBCLK	SB3V	Native	SMBCLK_R
GPP_C1	GPP_C1_SMBDATE	SB3V	Native	SMBDATA_R
GPP_C2	GPP_C2_SMBALERT_N	SB3V	Native	TLS_STRAP
GPP_C3	GPP_C3_SML0CLK	SB3V	Native	SML0_CLK
GPP_C4	GPP_C4_SML0DATA	SB3V	Native	SML0_DATA
GPP_C5	GPP_C5_SML0ALERT_N	SB3V	Native	ESPI_STRAP
GPP_C6	GPP_C6_SML1CLK	SB3V	Native	SML1_CLK
GPP_C7	GPP_C7_SML1DATA	SB3V	Native	SML1_DATA
GPP_C8	GPP_C8_UART0_RXD	SB3V	IN	CLR_CMOS
GPP_C9	GPP_C9_UART0_TXD	SB3V	Native	N.C
GPP_C10	GPP_C10_UART0_RTS	SB3V	Native	IBUTTON
GPP_C11	GPP_C11_UART0_CTS_N	SB3V	Native	N.C
GPP_C12	GPP_C12_UART1_RXD_ISH_UART1_RXD	SB3V	IN	PCH_GPIO22
GPP_C13	GPP_C13_UART1_TXD_ISH_UART1_TXD	SB3V	IN	PCH_GPIO23
GPP_C14	GPP_C14_UART1_RTS_N_ISH_UART1_RTS	SB3V	IN	PCH_GPIO21
GPP_C15	GPP_C15_UART1_CTS_N_ISH_UART1_CTS	SB3V	OUT	WLAN_DISABLE_N
GPP_C16	GPP_C16_I2C0_SDA	SB3V	Native	N.C
GPP_C17	GPP_C17_I2C0_SCL	SB3V	Native	N.C
GPP_C18	GPP_C18_I2C1_SDA	SB3V	Native	N.C
GPP_C19	GPP_C19_I2C1_SCL	SB3V	Native	N.C
GPP_C20	GPP_C20_UART2_RXD	SB3V	Native	N.C
GPP_C21	GPP_C21_UART2_TXD	SB3V	Native	N.C
GPP_C22	GPP_C22_UART2_RTS_N	SB3V	Native	N.C
GPP_C23	GPP_C23_UART2_CTS_N	SB3V	Native	N.C

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_D0	GPP_D0_SPI1_CS_N	SB3V	Native	N.C
GPP_D1	GPP_D1_SPI1_CLK	SB3V	OUT	PW_LED_N
GPP_D2	GPP_D2_SPI1_MISO	SB3V	IN	PD_PCH_GPP_D_2
GPP_D3	GPP_D3_SPI1_MOSI	SB3V	IN	PD_PCH_GPP_D_3
GPP_D4	GPP_D4_ISH_I2C2_SDA	SB3V	OUT	SUS_LED_N
GPP_D5	GPP_D5_SSP0_SFRM	SB3V	Native	N.C
GPP_D6	GPP_D6_SSP0_TXD	SB3V	Native	N.C
GPP_D7	GPP_D7_SSP0_RXD	SB3V	Native	N.C
GPP_D8	GPP_D8_SSP0_SCLK	SB3V	Native	N.C
GPP_D9	GPP_D9_ISH_SPI_CS_N	SB3V	Native	N.C
GPP_D10	GPP_D10_ISH_SPI_CLK	SB3V	Native	N.C
GPP_D11	GPP_D11_ISH_SPI_MISO	SB3V	IN	FUSB_G1
GPP_D12	GPP_D12_ISH_SPI_MOSI	SB3V	IN	FUSB_G2
GPP_D13	GPP_D13_ISH_UART0_RXD	SB3V	IN	FUSB_G3
GPP_D14	GPP_D14_ISH_UART0_TXD	SB3V	IN	PS2_PINHEADER_N
GPP_D15	GPP_D15_ISH_UART0_RTS_N	SB3V	IN	LPT_DET#
GPP_D16	GPP_D16_ISH_UART0_CTS_N	SB3V	Native	N.C
GPP_D17	GPP_D17_DMIC_CLK1	SB3V	Native	COM_WAKE#
GPP_D18	GPP_D18_DMIC_DATA1	SB3V	IN	PCH_GPIO_D18
GPP_D19	GPP_D19_DMIC_CLK0	SB3V	Native	N.C
GPP_D20	GPP_D20_DMIC_DATA0	SB3V	Native	N.C
GPP_D21	GPP_D21_SPI1_IO2	SB3V	Native	N.C
GPP_D22	GPP_D22_SPI1_IO3	SB3V	Native	N.C
GPP_D23	GPP_D23_ISH_I2C2_SCL	SB3V	Native	N.C
GPP_E0	GPP_E0_SATAXPCIE0_SATAGP	SB3V	Native	N.C
GPP_E1	GPP_E1_SATAXPCIE1_SATAGP1	SB3V	Native	N.C
GPP_E2	GPP_E2_SATAXPCIE2_SATAGP2	SB3V	Native	N.C
GPP_E3	GPP_E3_CPU_GP0	SB3V	Native	BMC_PCH_SCI_N
GPP_E4	GPP_E4_DEVSLP0	SB3V	Native	BMC_FORCE_SMI_N
GPP_E5	GPP_E5_DEVSLP1	SB3V	Native	N.C
GPP_E6	GPP_E6_DEVSLP2	SB3V	Native	N.C
GPP_E7	GPP_E7_CPU_GP1	SB3V	Native	N.C
GPP_E8	GPP_E8_SATALED_N	SB3V	OUT	SATA_LED#
GPP_E9	GPP_E9_USB2_OC0_N	SB3V	Native	USB_OCP#0
GPP_E10	GPP_E10_USB2_OC1_N	SB3V	Native	USB_OCP#1
GPP_E11	GPP_E11_USB2_OC2_N	SB3V	Native	USB_OCP#2
GPP_E12	GPP_E12_USB2_OC3_N	SB3V	Native	USB_OCP#3
GPP_F0	GPP_F17_USB2_OCB_6	SB3V	Native	PCH_GPIO_F1
GPP_F1	GPP_F1_SATAXPCIE4_SATAGP4	SB3V	IN	M.2_SSD1_PEDET#
GPP_F2	GPP_F2_SATAXPCIE5_SATAGP5	SB3V	Native	PCH_GPIO_F2
GPP_F3	GPP_F3_SATAXPCIE6_SATAGP6	SB3V	Native	N.C
GPP_F4	GPP_F4_SATAXPCIE7_SATAGP7	SB3V	Native	TP20
GPP_F5	GPP_F5_DEVSLP3	SB3V	IN	SPI_SIRQ#
GPP_F6	GPP_F6_DEVSLP4	SB3V	Native	PCH_GPIO_F6
GPP_F7	GPP_F7_DEVSLP5	SB3V	Native	SSD1_SATA_DEVSLP
GPP_F8	GPP_F8_DEVSLP6	SB3V	Native	N.C
GPP_F9	GPP_F9_DEVSLP7	SB3V	Native	USB_DISABLE#
GPP_F10	GPP_F10_SCLOCK	SB3V	OUT	N.C
GPP_F11	GPP_F11_SLOAD	SB3V	OUT	N.C
GPP_F12	GPP_F12_SDATAOUT1	SB3V	OUT	N.C
GPP_F13	GPP_F13_SDATAOUT0	SB3V	OUT	N.C
GPP_F14	GPP_F14	SB3V	IN	SKTOCC#
GPP_F15	GPP_F15_USB2_OCB_4	SB3V	Native	USB_OCP#4
GPP_F16	GPP_F16_USB2_OCB_5	SB3V	Native	USB_OCP#5
GPP_F17	GPP_F17_USB2_OCB_8	SB3V	Native	USB_OCP#8
GPP_F18	GPP_F18_USB2_OCB_7	SB3V	Native	USB_OCP#7
GPP_F19	GPP_F19_EDP_VDDEN	SB3V	Native	N.C
GPP_F20	GPP_F20_EDP_BKLTEN	SB3V	Native	N.C
GPP_F21	GPP_F21_EDP_BKLTCTL	SB3V	Native	N.C
GPP_F22	GPP_F22	SB3V	OUT	PCH_GPIO_F22
GPP_F23	GPP_F23	SB3V	Native	N.C
GPD0	GPD0_BATLOW_N	SB3V_DSW	Native	PCH_BATLOW#
GPD1	GPD1_ACPRESENT	SB3V_DSW	OUT	SUS_LED_N
GPD2	GPD2_LAN_WAKE_N	SB3V_DSW	Native	LAN_WAKE#_C
GPD3	GPD3_PWRBTN_N	SB3V_DSW	Native	PWRBTN#
GPD4	GPD4_SLP_S3_N	SB3V_DSW	Native	SLP_S3#
GPD5	GPD5_SLP_S4_N	SB3V_DSW	Native	SLP_S4#
GPD6	GPD5_SLP_A_	SB3V_DSW	Native	PCH_SLP_A#
GPD7	GPD7_USB2_WAKEOUT_N	SB3V_DSW	Native	N.C
GPD8	GPD8_SUSCL	SB3V_DSW	Native	SUSCLK
GPD9	GPD9_SLP_WLAN_N	SB3V_DSW	Native	N.C
GPD10	GPD10_SLP_S5_N	SB3V_DSW	Native	SLP_S5#
GPD11	GPD11_LANPHYPC	SB3V_DSW	Native	LAN_DISABLE#

GPIO	Signal Name	Power Well	IN/OUT	Usage
GPP_G0	GPP_G0_FAN_TACH_0	SB3V	IN	CHASSIS_ID1
GPP_G1	GPP_G1_FAN_TACH_1	SB3V	IN	CHASSIS_ID2
GPP_G2	GPP_G2_FAN_TACH_2	SB3V	IN	H_PROCHOT_PCH_N
GPP_G3	GPP_G3_FAN_TACH_3	SB3V	Native	PCH_BMC_FOURCE_INT_N
GPP_G4	GPP_G4_FAN_TACH_4	SB3V	Native	N.C
GPP_G5	GPP_G5_FAN_TACH_5	SB3V	Native	N.C
GPP_G6	GPP_G6_FAN_TACH_6	SB3V	Native	N.C
GPP_G7	GPP_G7_FAN_TACH_7	SB3V	Native	N.C
GPP_G8	GPP_G8_FAN_PWM_0	SB3V	Native	N.C
GPP_G9	GPP_G9_FAN_PWM_1	SB3V	Native	N.C
GPP_G10	GPP_G10_FAN_PWM_2	SB3V	Native	N.C
GPP_G11	GPP_G11_FAN_PWM_3	SB3V	IN	BMC_THROTTLE_N
GPP_G12	GPP_G12_GSXDOUT	SB3V	IN	GPP_G0
GPP_G13	GPP_G13_GSXSLOAD	SB3V	IN	GPP_G1
GPP_G14	GPP_G14_GSXDIN	SB3V	IN	GPP_G2
GPP_G15	GPP_G15_GSXSRESET_N	SB3V	IN	GPP_G3
GPP_G16	GPP_G16_GSXCLK	SB3V	IN	GPP_G4
GPP_G17	GPP_G17_ADR_COMPLETE	SB3V	IN	GPP_G5
GPP_G18	GPP_G18_NMI_N	SB3V	Native	FM_NMI_EVENT_N
GPP_G19	GPP_G19_SMI_N	SB3V	IN	SIO_SCI_N
GPP_G20	GPP_G20	SB3V	Native	BMC_READY
GPP_G21	GPP_G21	SB3V	IN	PCH_GPIO20
GPP_G22	GPP_G22	SB3V	Native	BMC_CARD_DET_R_N
GPP_G23	GPP_G23	SB3V	OUT	VGA_URDBG
GPP_H0	GPP_H0_SRCCLKREQ6_N	SB3V	Native	FM_MEM_THERM_EVENT_LVT3_N
GPP_H1	GPP_H1_SRCCLKREQ7_N	SB3V	Native	FM_NM_THROTTLE_N
GPP_H2	GPP_H2_SRCCLKREQ8_N	SB3V	OUT	FM_CATERR_N
GPP_H3	GPP_H3_SRCCLKREQ9_N	SB3V	Native	PCH_BMC_ALERT
GPP_H4	GPP_H4_SRCCLKREQ10_N	SB3V	Native	N.C
GPP_H5	GPP_H5_SRCCLKREQ11_N	SB3V	Native	N.C
GPP_H6	GPP_H6_SRCCLKREQ12_N	SB3V	Native	N.C
GPP_H7	GPP_H7_SRCCLKREQ13_N	SB3V	Native	N.C
GPP_H8	GPP_H8_SRCCLKREQ14_N	SB3V	Native	N.C
GPP_H9	GPP_H9_SRCCLKREQ15_N	SB3V	Native	N.C
GPP_H10	GPP_H10_SML2CLK	SB3V	OUT	WIRELESS_EN2
GPP_H11	GPP_H11_SML2DATA	SB3V	OUT	WIRELESS_EN
GPP_H12	GPP_H12_SML2ALERT_N	SB3V	Native	FM_ESPI_FLASH_MODE
GPP_H13	GPP_H13_SML3CLK	SB3V	Native	N.C
GPP_H14	GPP_H14_SML3DATA	SB3V	Native	N.C
GPP_H15	GPP_H15_SML3ALERT_N	SB3V	Native	PCH_GPP_H15
GPP_H16	GPP_H16_SML4CLK	SB3V	Native	N.C
GPP_H17	GPP_H17_SML4DATA	SB3V	Native	N.C
GPP_H18	GPP_H18_SML4ALERT_N	SB3V	Native	PCH_GPP_H18
GPP_H19	GPP_H19_ISH_I2C0_SDA	SB3V	Native	N.C
GPP_H20	GPP_H20_ISH_I2C0_SCL	SB3V	Native	N.C
GPP_H21	GPP_H21_ISH_I2C1_SDA	SB3V	Native	N.C
GPP_H22	GPP_H22_ISH_I2C1_SCL	SB3V	Native	N.C
GPP_H23	GPP_H23	SB3V	Native	N.C
GPP_I0	GPP_I0_DDPB_HPD0	SB3V	IN	VGA_DDI3_HPD
GPP_I1	GPP_I1_DDPC_HPD1	SB3V	IN	DP_DDPC_HPD
GPP_I2	GPP_I2_DDPD_HPD2	SB3V	IN	DP_DDPD_HPD
GPP_I3	GPP_I3_DDPE_HPD3	SB3V	IN	U2_BA4
GPP_I4	GPP_I4_EDP_HPD	SB3V	IN	U2_BD7
GPP_I5	GPP_I5_DDPB_CTRLCLK	SB3V	Native	TP30
GPP_I6	GPP_I6_DDPB_CTRLDATA	SB3V	Native	DDPD_CTRLDATA
GPP_I7	GPP_I7_DDPC_CTRLCLK	SB3V	Native	DP_DDPC_CTRLCLK
GPP_I8	GPP_I8_DDPC_CTRLDATA	SB3V	Native	DP_DDPC_CTRLDATA
GPP_I9	GPP_I9_DDPD_CTRLCLK	SB3V	Native	DP_DDPD_CTRLCLK
GPP_I10	GPP_I10_DDPD_CTRLDATA	SB3V	Native	DP_DDPD_CTRLDATA

SIO GPIO (NCT6685D)

GPIO	Signal Name	PIN	Power We	In/Out	Usage
GPIO00	PWMOUT/TACHIN/GPIO00	3	SB3V	IN	FM_CATERR_N
GPIO95	GPIO95/BKFD_CUT	74	SB3V	OUT	ME_CNTL
GPIO85	SMI#/OVT#/GPIO85	2	SB3V	----	SIO_SCI_N
GPIO74	GPIO74 / TACHIN / PWMOUT	37	SB3V	OD	BMC_THROTTLE_N
GPIO77	SKTOCC# / GPIO77	102	SB3V	IN	IS1X0M_BOARDID
GPIO66	P_S5_0 / 3VSBSW / LATCH_BKFD_CUT / GP	70	SB3V	OUT	USB_PS2_PON
GPIO93	3VSBSW#/GPIO93/SLP_SUS#	89	3V_DSW	OUT	SIO_GP93
GPIO94	GPIO94/SLP_SUS_FET	88	3V_DSW	IN	COM_WAKE#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **POWER Sequence**

Size	Document Number	Rev
C	EQ370	0.7

Date: Friday, January 05, 2018 | Sheet 62 of 62