

A

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D

# BRAKING IO

## POD 5

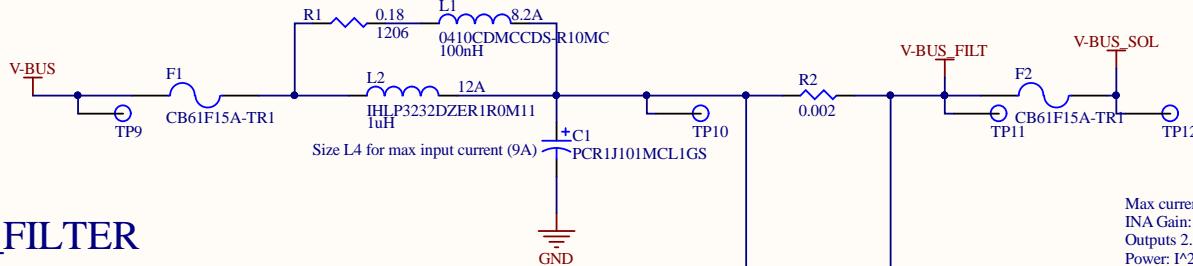
### REV 2

Title <b>Braking IO PCB</b>		Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706	
Engineer:	Revision:	Date: 7/9/2020 Time: 9:02:26 PM Sheet of	

A

A

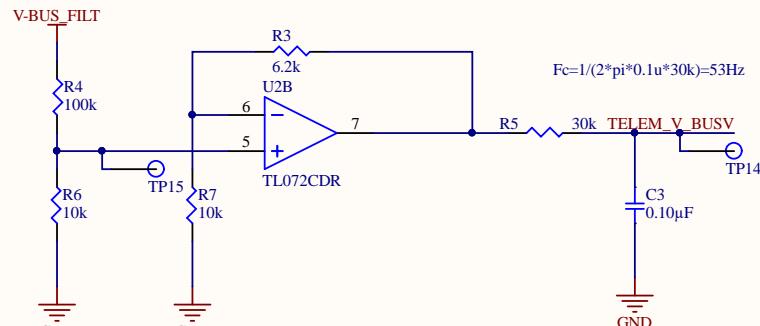
should change upstream fuse to be higher current rating than downstream.



## BUS\_FILTER

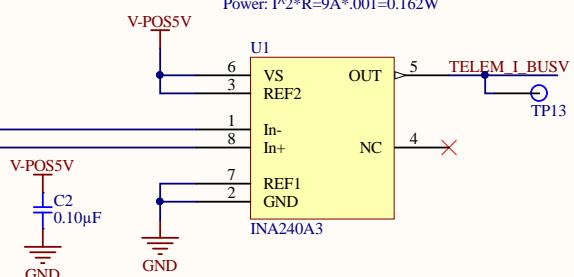
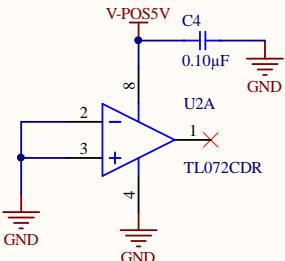
Filter design reference: <http://www.ti.com/lit/an/snva538/snva538.pdf>  
<http://ecee.colorado.edu/~rwe/papers/APEC99.pdf>

Max current draw: 9A > 9A\*0.002Ohm=0.018V  
 INA Gain: 100V/V > 4.3V at Max current  
 Outputs 2.5V when I=0  
 Power:  $I^2 \cdot R = 9A \cdot .001 = 0.162W$



GAIN: 1.62V/V  
 MIN BUS VOLTAGE: 20V -> 2.945V  
 MIN BUS VOLTAGE: 28V -> 4.12V

## VOLTAGE TELEMETRY

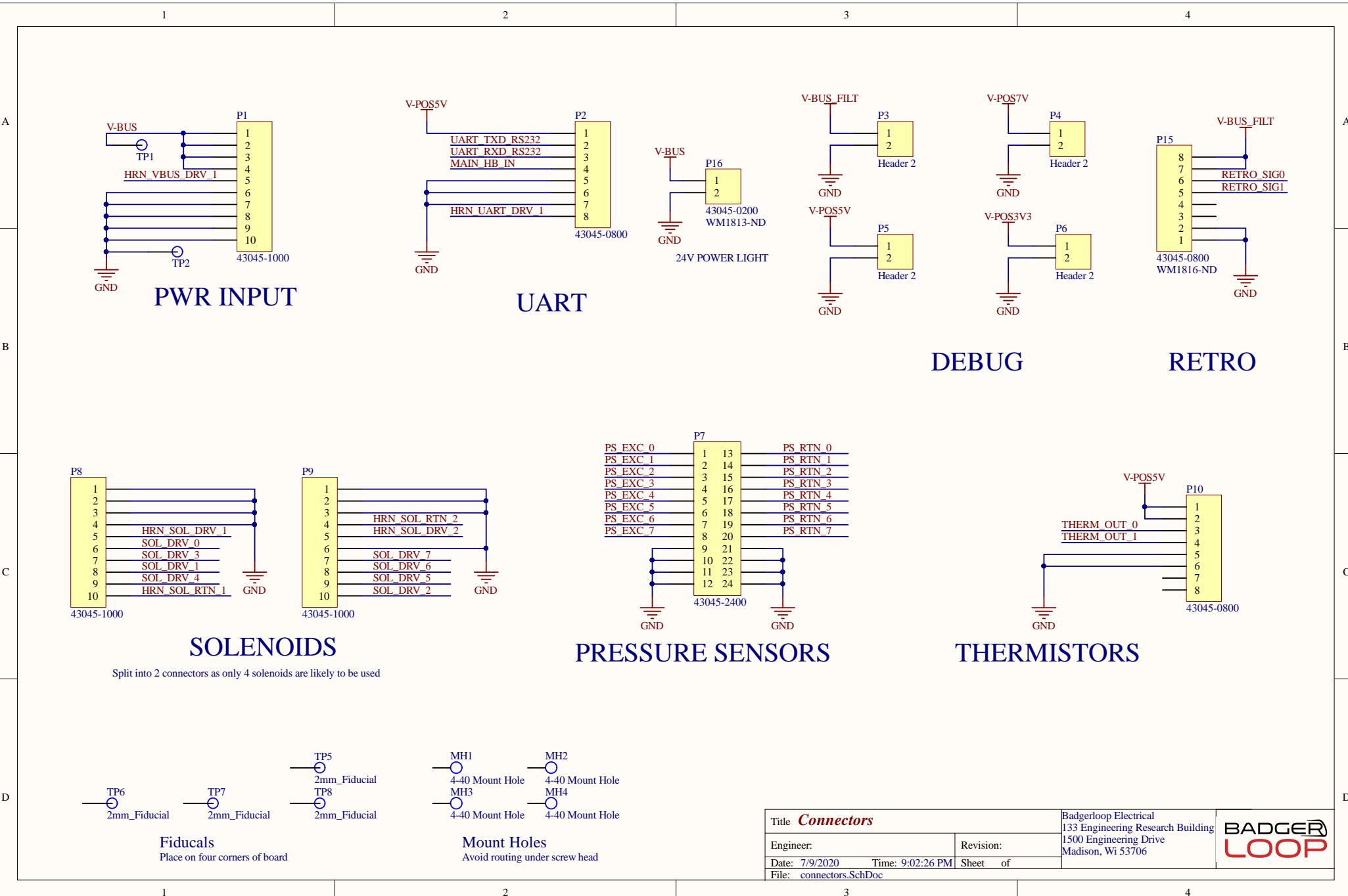


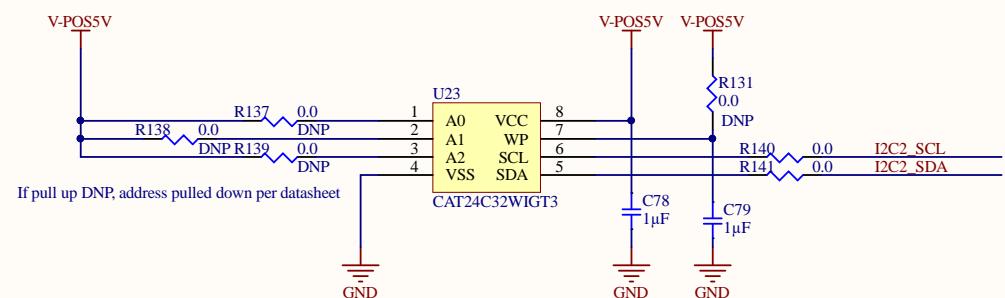
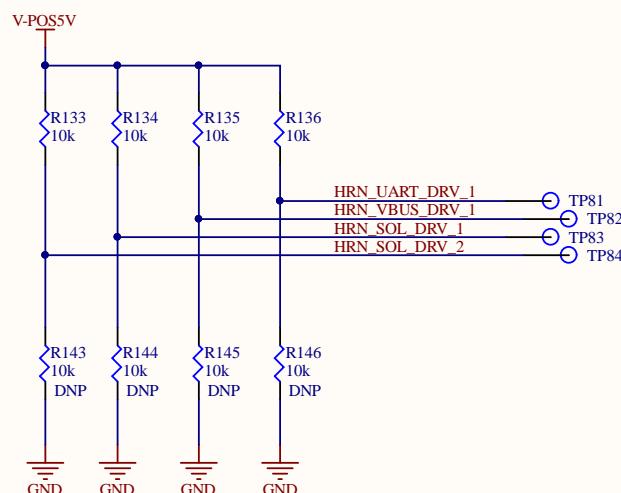
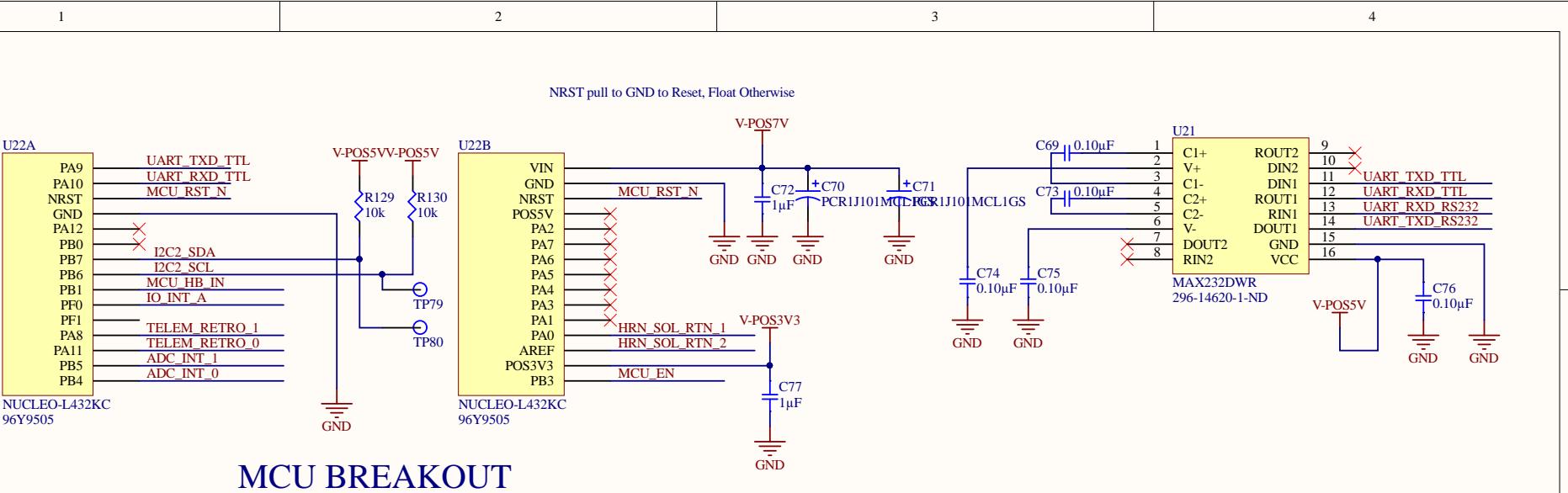
## CURRENT TELE

Max current draw: 9A > 9A\*0.002Ohm=0.018V  
 INA Gain: 200V/V > 3.6V at Max current  
 Power:  $I^2 \cdot R = 4A \cdot .01 = 0.04W$

Title <b>Bus Filter</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 7/9/2020	Time: 9:02:26 PM	1500 Engineering Drive
File: bus_filter.SchDoc		Madison, Wi 53706

**BADGER**  
**LOOP**



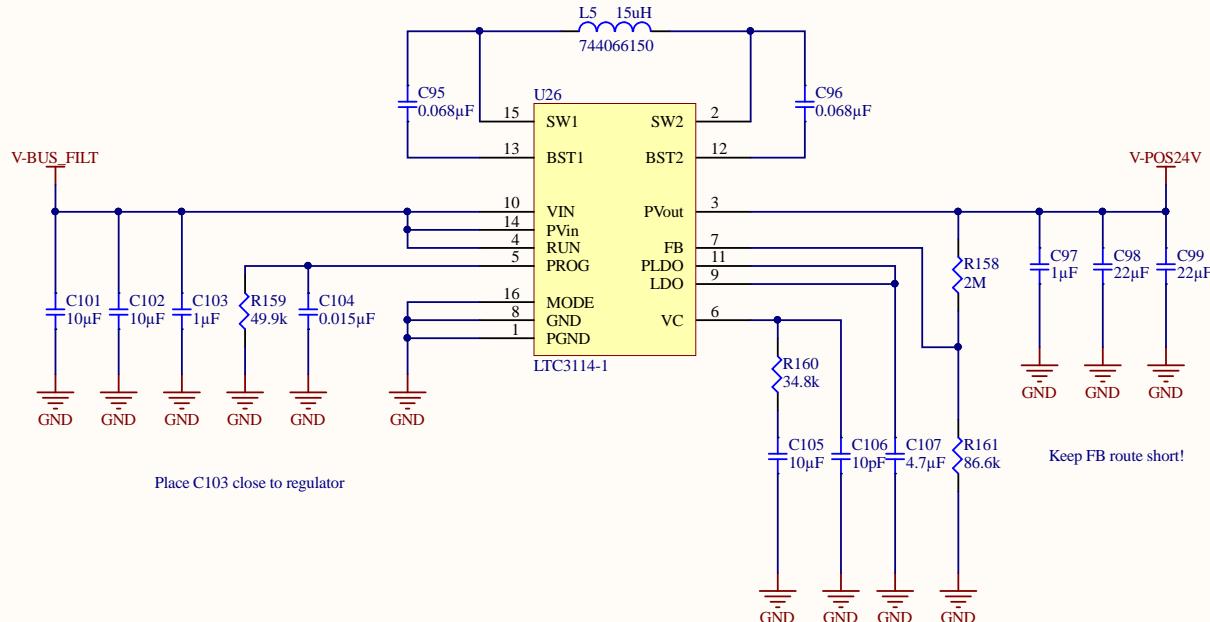


Title <b>Microcontroller</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 7/9/2020	Time: 9:02:26 PM	1500 Engineering Drive
File: mcu.SchDoc		Madison, Wi 53706

**BADGER  
LOOP**

A

A



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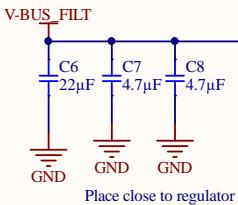
D

Title <b>Power 24V</b>		Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706
Engineer:	Revision:	
Date: 7/9/2020	Time: 9:02:27 PM	Sheet of
File: power_24V.SchDoc		<b>BADGER</b> <b>LOOP</b>

**A**

Notes:  
Follow layout reference design  
Place bypass caps close to regulator  
Keep hot loops as short as possible  
Possible to replace ceramic bulk cap with a tantalum.

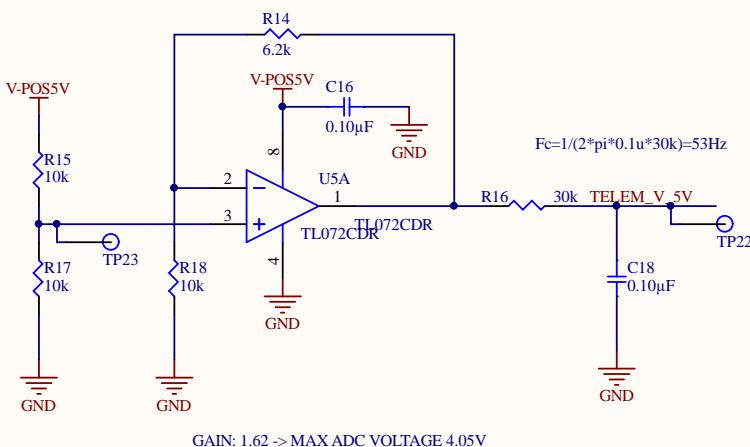
Replace with Tantalum?  
Place close to regulator  
[See https://github.com/badgerloop-software/hardware/tree/master/braking\\_io/design](https://github.com/badgerloop-software/hardware/tree/master/braking_io/design)



## 5V SUPPLY

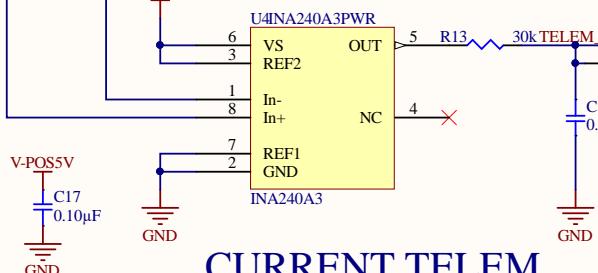
VIN MIN: 8V VIN MAX: 35V  
IOUT MAX: Up to 2A  
 $V_{OUT} = (R_1 * 1.221)(R_2) + 1.221$   
 $V_{OUT} = (10K * 1.221)(3.24K) + 1.221 = 4.989V$  nominal

Keep SNS route short and fat!



GAIN: 1.62 -> MAX ADC VOLTAGE 4.05V

## VOLTAGE TELEMETRY



Max current draw:  $2A \rightarrow 2A * 0.002 \text{ Ohm} = 0.004V$   
INA Gain:  $100V/V \rightarrow 2.9V$  at Max current  
Outputs 2.5V when  $I=0$   
Power:  $P^2 * R = 4A * 0.002 = 0.032W$

## CURRENT TELEM

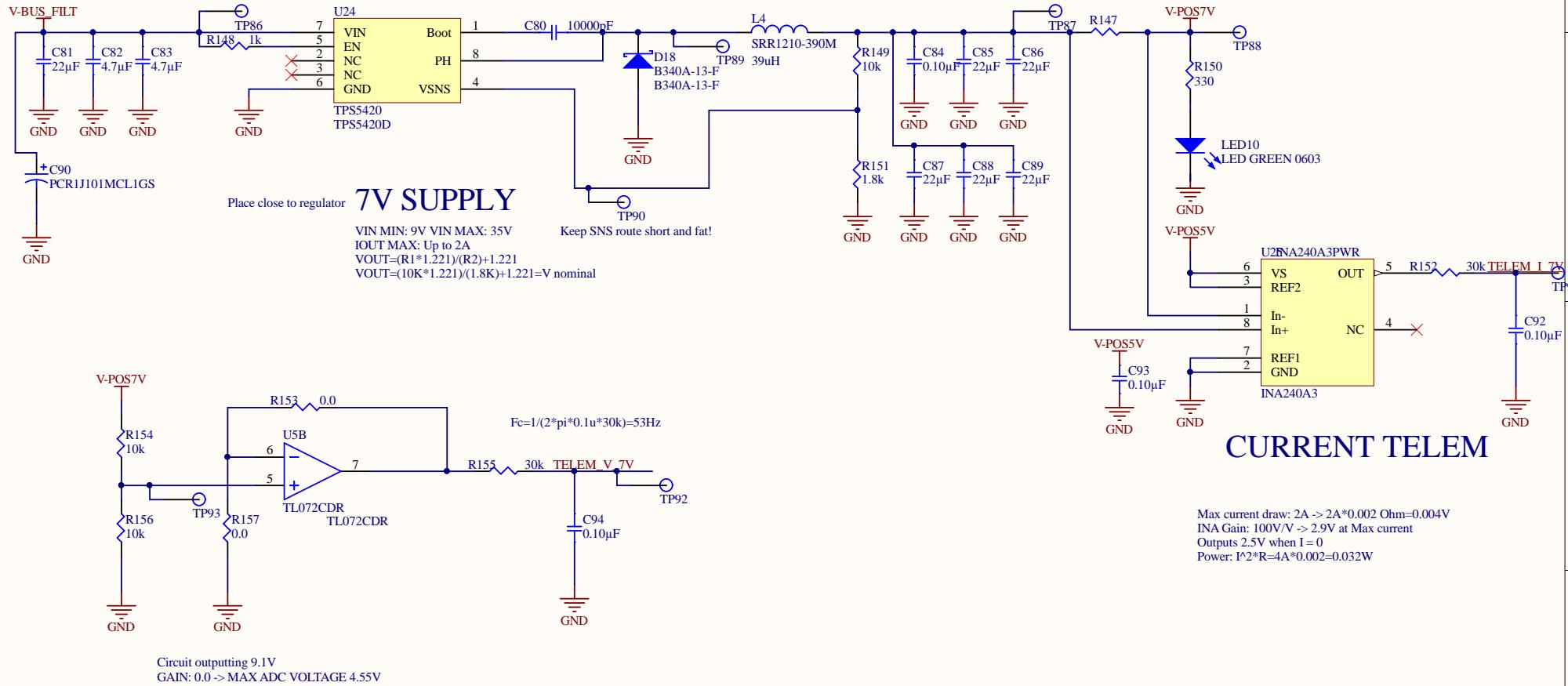
Title	Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706	
Engineer:	Revision:	
Date: 7/9/2020	Time: 9:02:27 PM	Sheet of
File: power_5V.SchDoc		



**A**

Notes:  
Follow layout reference design  
Place bypass caps close to regulator  
Keep hot loops as short as possible  
Possible to replace ceramic bulk cap with a tantalum.

Replace with Tantalum?  
Place close to regulator  
See [https://github.com/badgerloop-software/hardware/tree/master/braking\\_io/design](https://github.com/badgerloop-software/hardware/tree/master/braking_io/design)



Title <b>7V SUPPLY</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 7/9/2020	Time: 9:02:27 PM	1500 Engineering Drive
File: power_7V.SchDoc		Madison, Wi 53706

**BADGER  
LOOP**

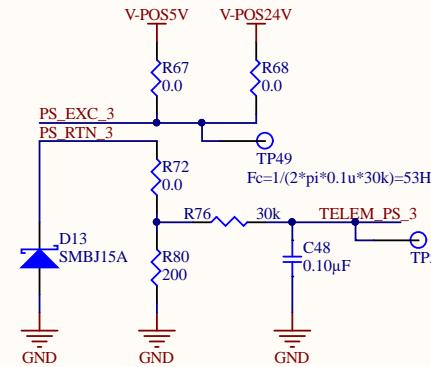
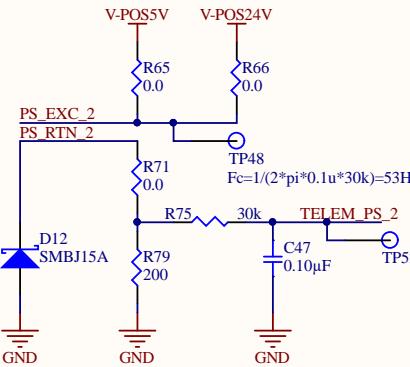
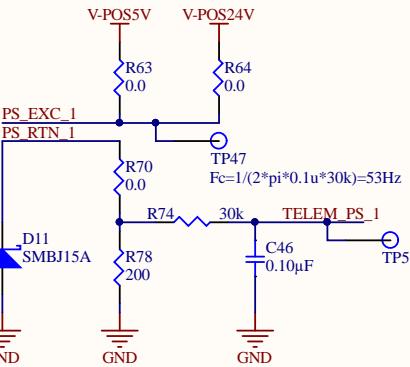
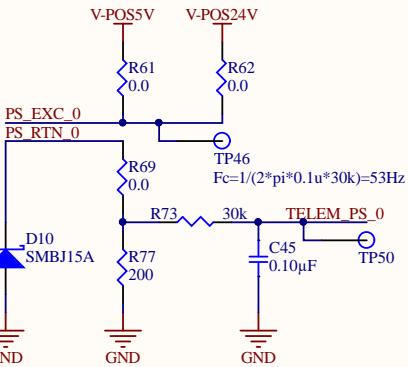
1

2

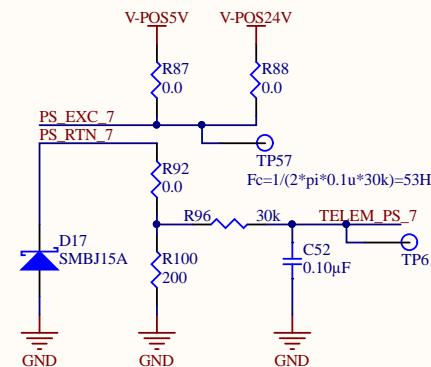
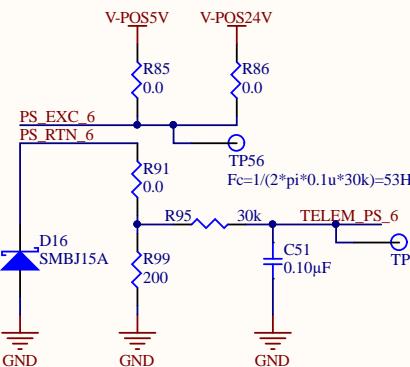
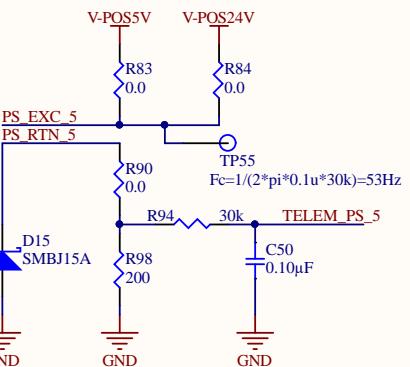
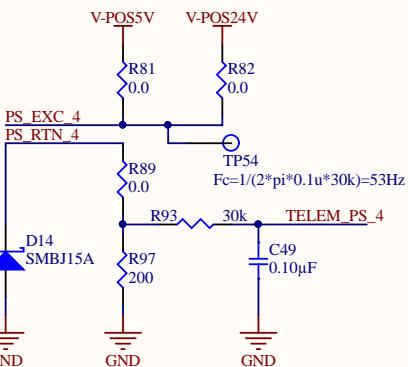
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4

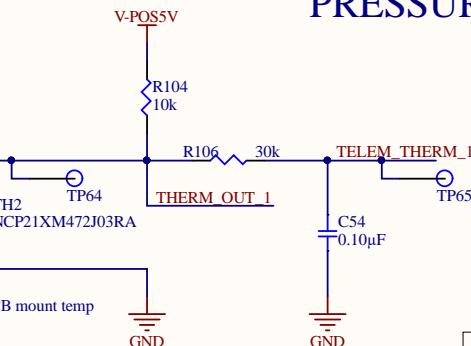
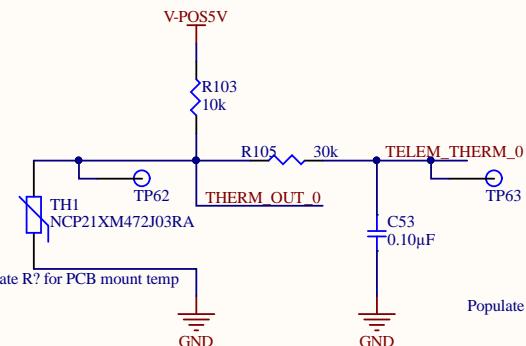
A



B



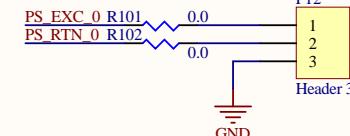
C



## TEMPERATURE

## PRESSURE SENSORS

Populate Bottom resistor for current output  
 Current Min Output: 4mA\*200=800mV  
 Current Max Output: 20mA\*200=4.0V  
 Voltage Min Output: 0.5V  
 Voltage Max Output: 4.5V



Title **Pressure Sensors**

Badgerloop Electrical  
 133 Engineering Research Building  
 1500 Engineering Drive  
 Madison, Wi 53706

**BADGER**  
**LOOP**

Engineer:

Revision:

Date: 7/9/2020 Time: 9:02:27 PM

Sheet of

File: pressure.SchDoc

1

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A

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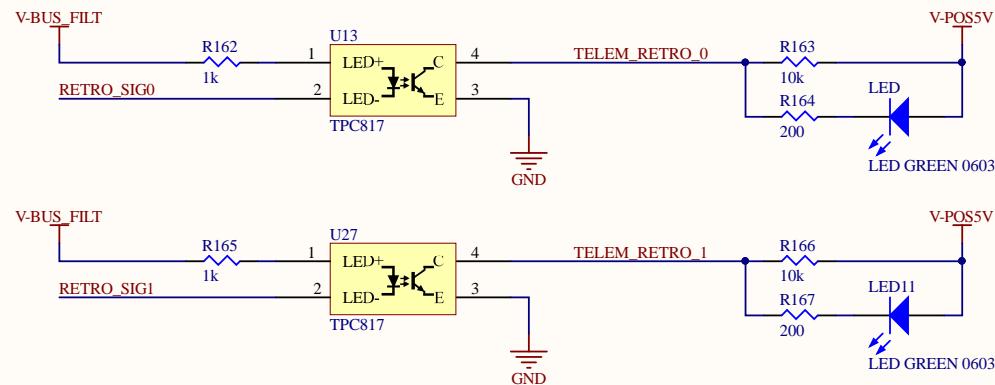
B

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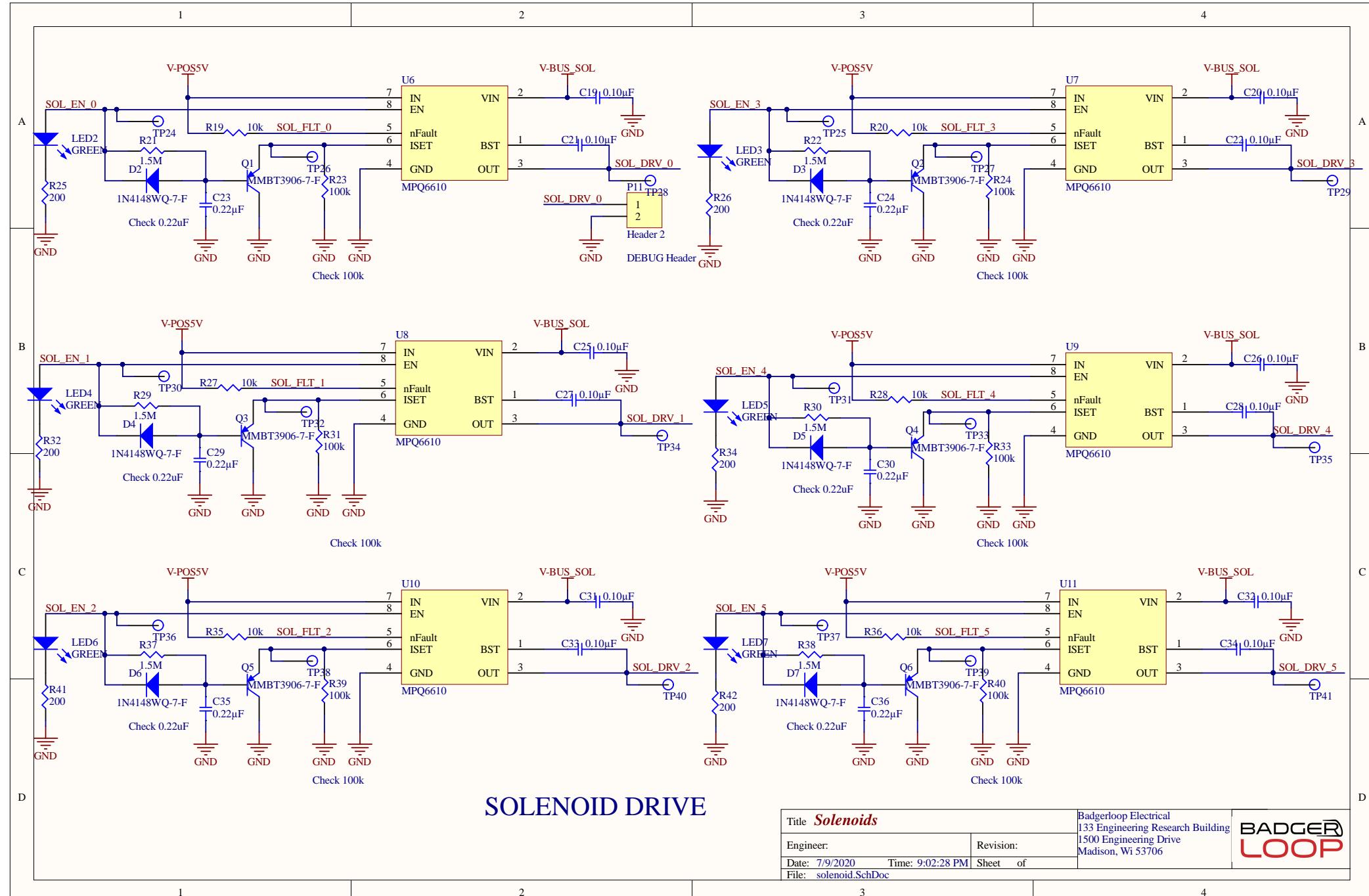
D

D



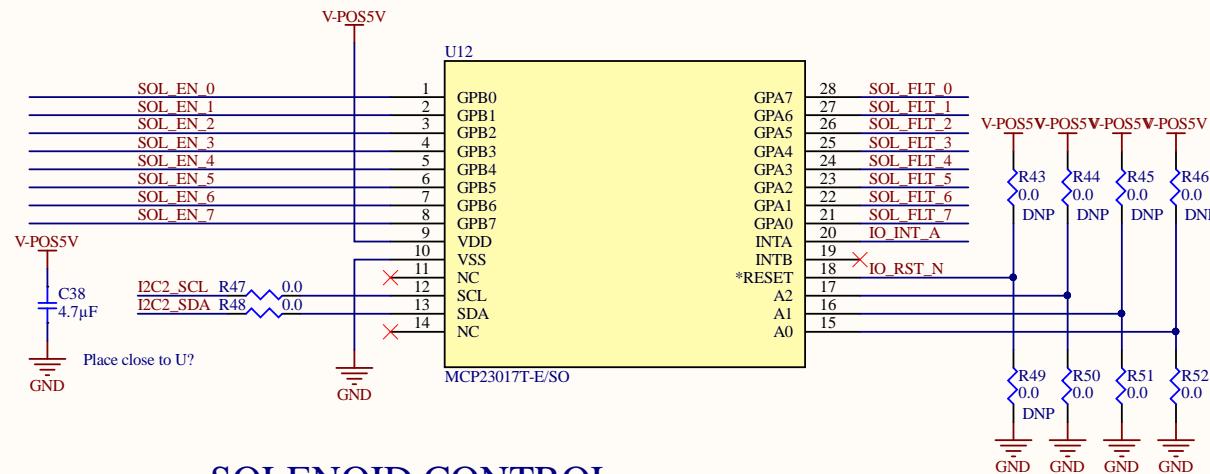
Title <b>Retro</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 7/9/2020	Time: 9:02:28 PM	1500 Engineering Drive
File: retro.SchDoc		Madison, Wi 53706

**BADGER**  
**LOOP**

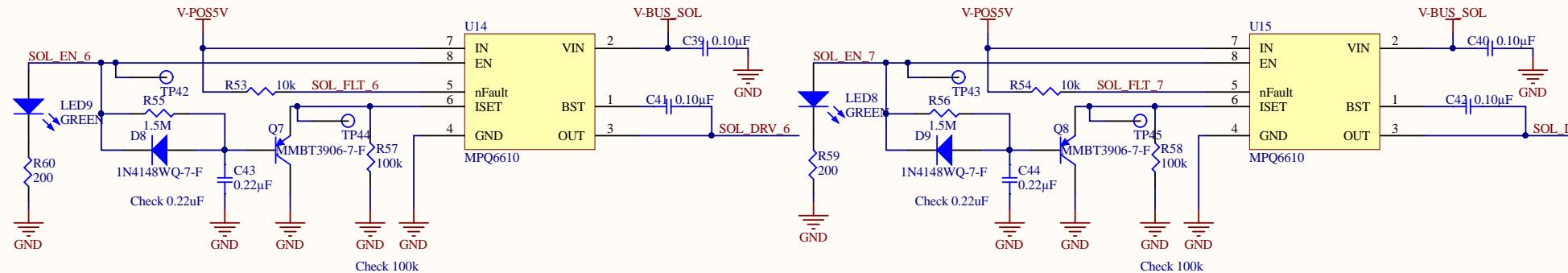


Title <b>Solenoids</b>		Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706
Engineer:	Revision:	
Date: 7/9/2020	Time: 9:02:28 PM	Sheet of
File: solenoid.SchDoc		<b>BADGER</b> <b>LOOP</b>

A



C



### Title *Solenoid Control*

Engineer:	Revision:	Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706
Date: 7/9/2020	Time: 9:02:28 PM	Sheet of
File: solenoid_drv.SchDoc		<b>BADGER LOOP</b>

1 2 3 4

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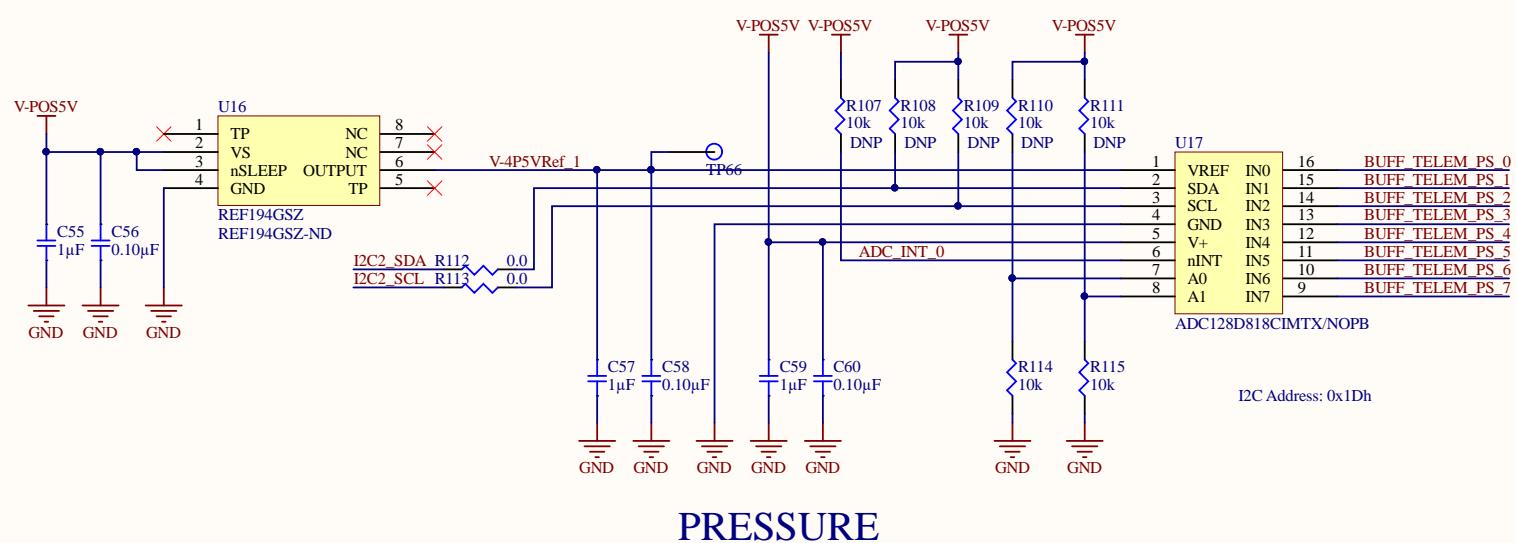
D

A

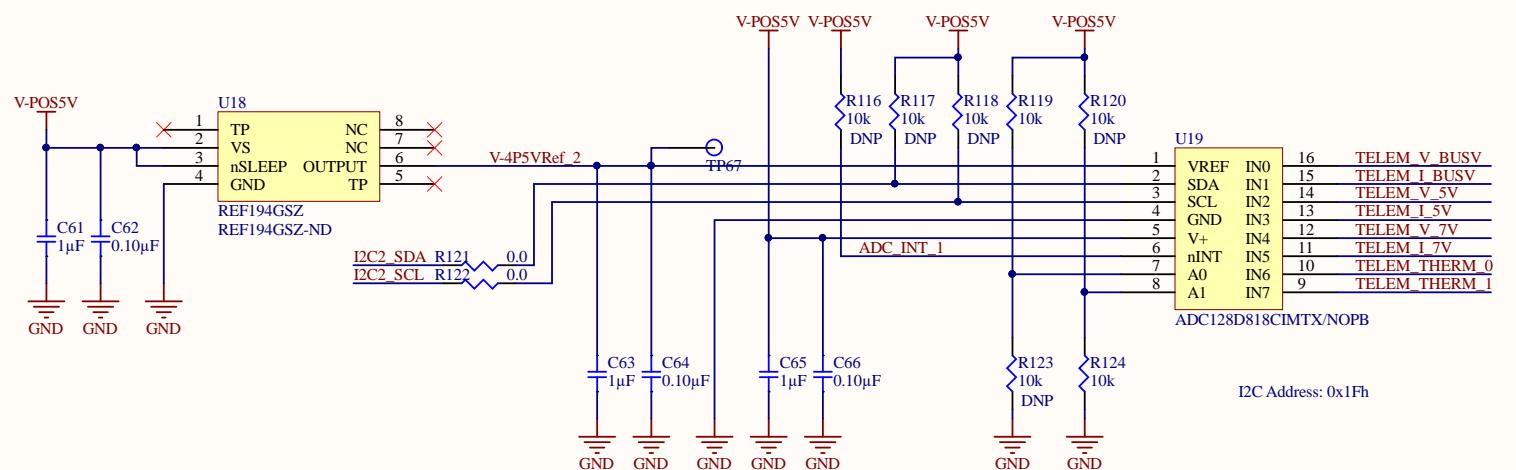
B

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## PRESSURE



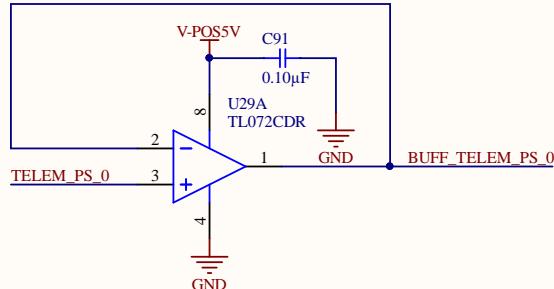
## RAIL AND TEMPERATURE

Title <b>ADC</b>		Badgerloop Electrical 133 Engineering Research Building 1500 Engineering Drive Madison, Wi 53706
Engineer:	Revision:	
Date: 7/9/2020	Time: 9:02:28 PM	Sheet of
File: <a href="#">telemetry_adc.SchDoc</a>		<b>BADGER</b> <b>LOOP</b>

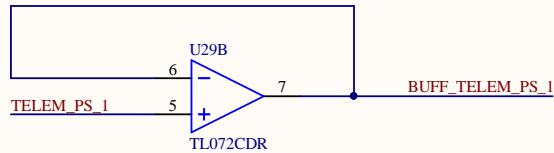
1 2 3 4

## Analog Unity Gain Buffers

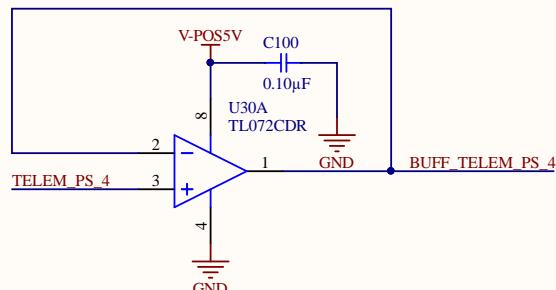
A



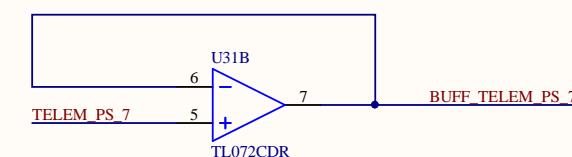
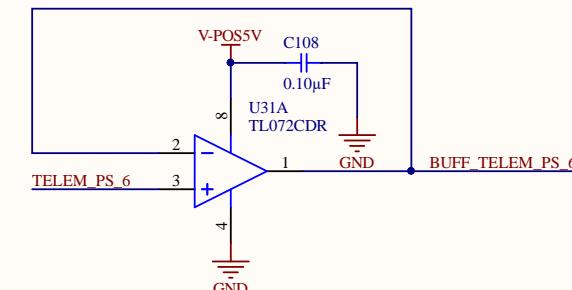
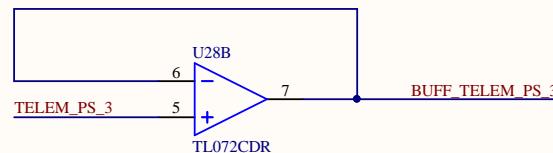
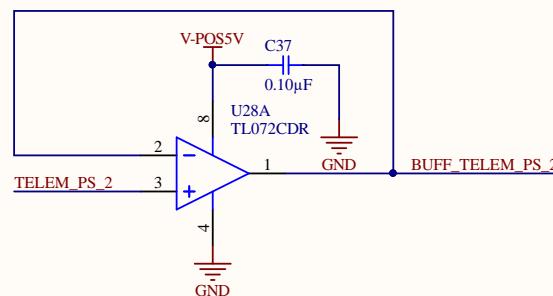
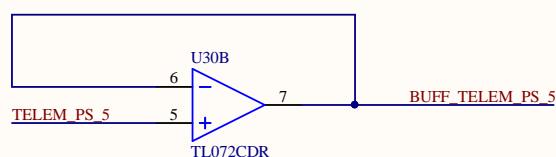
B



C



D



Title: <b>Unity Gain Buffer</b>			<i>Badgerloop 133 Engineering Research Building Madison, WI 53715</i>	<b>BADGER LOOP</b>
Size: A4	Number:	Revision:		
Date: 7/9/2020	Time: 9:02:28 PM	Sheet of		
File: C:\Users\Windows PC\Desktop\Badgerloop\git_repos\hardware\braking_io\unity_gain_buffer.SchDoc				

A

A

B

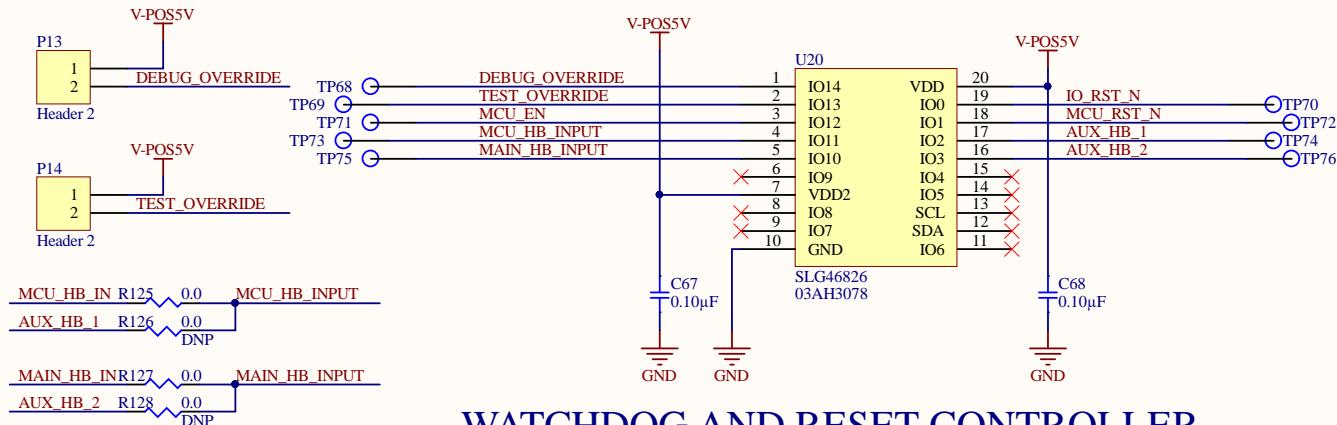
B

C

C

D

D



## WATCHDOG AND RESET CONTROLLER

### DEBUG

IO pin selection is arbitrary. Can be adjusted internally for better layout  
Currently- Inputs on Left, outputs on right

Modes of operation:  
Debug: EN signal is always on when SLG has power  
Populate Jumper 1  
Test: 10Hz signal internal signal is recirculated to mimic heartbeat  
Populate Jumper 2  
Operation: U2 expects 10Hz heartbeat. If no heartbeat for 1s after 20s Power on reset  
MCP\_RST\_N will fall and MCU\_RST\_N will pulse for 200ms

Silego Image here:  
<https://github.com/badgerloop-software/hardware/blob/master/silego/watchdog.gp6>

Silego Image PDF Outputs:

Title <b>Watchdog</b>		Badgerloop Electrical
Engineer:	Revision:	133 Engineering Research Building
Date: 7/9/2020	Time: 9:02:29 PM	1500 Engineering Drive
File: watchdog.SchDoc		Madison, Wi 53706

A

A

B

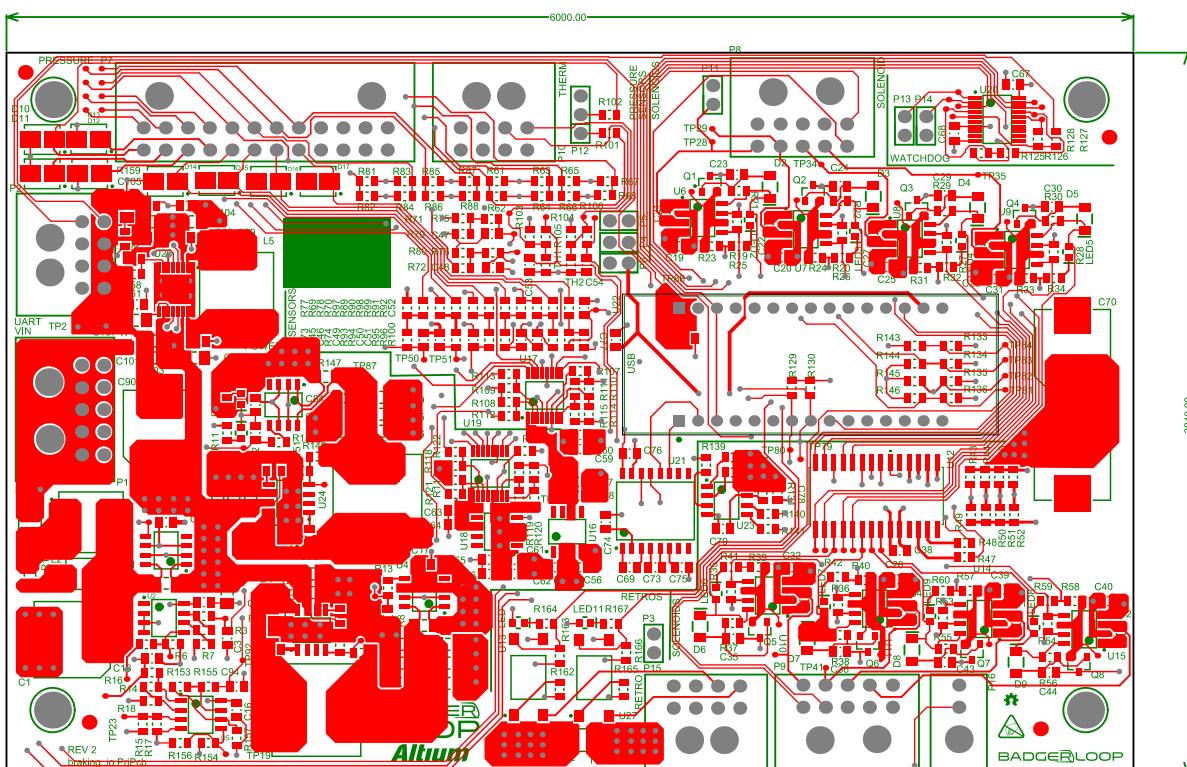
B

C

C

D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 2	FR-4	18.70mil	4.9	
5	GND	Copper	1.40mil		
6	Dielectric 1	FR-4	18.70mil	4.9	
7	PWR	Copper	1.40mil		
8	Dielectric 3	FR-4	18.70mil	4.9	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
7/9/2020

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO:  
Braking Input Output Controller

REV:  
A

SCALE:  
1:1

A

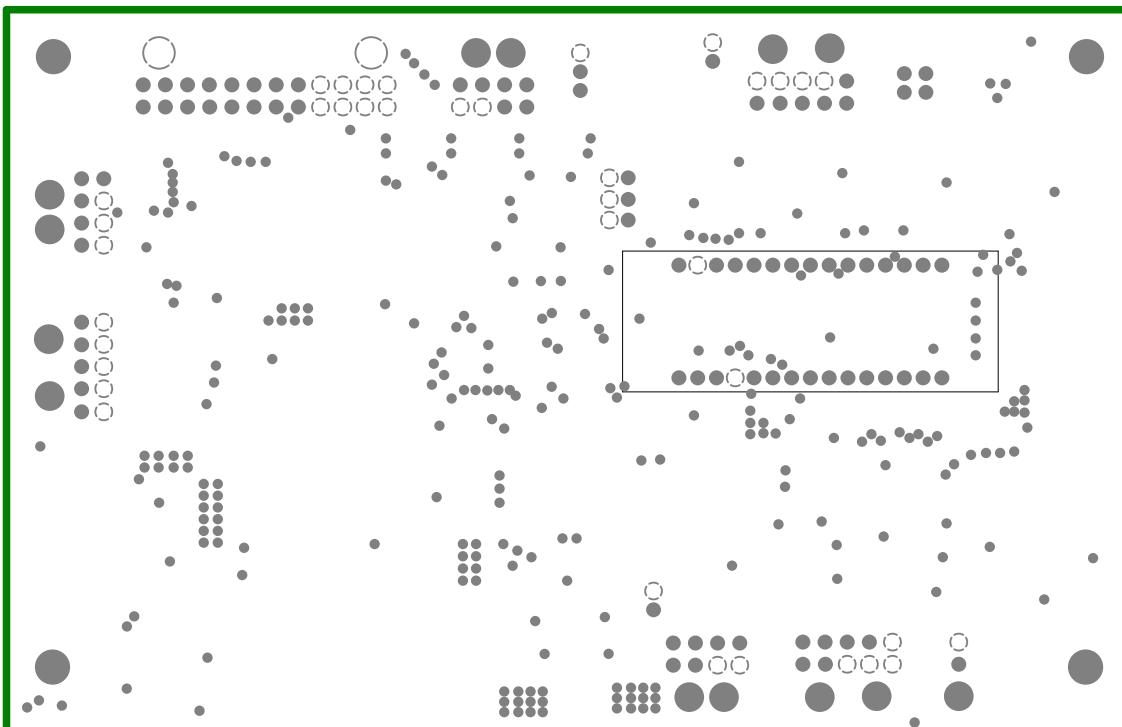
A

B

B

C

C



**BADGER  
LOOP**  
Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
7/9/2020

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO:  
Braking Input Output Controller

REV:  
A

SCALE:  
1:1

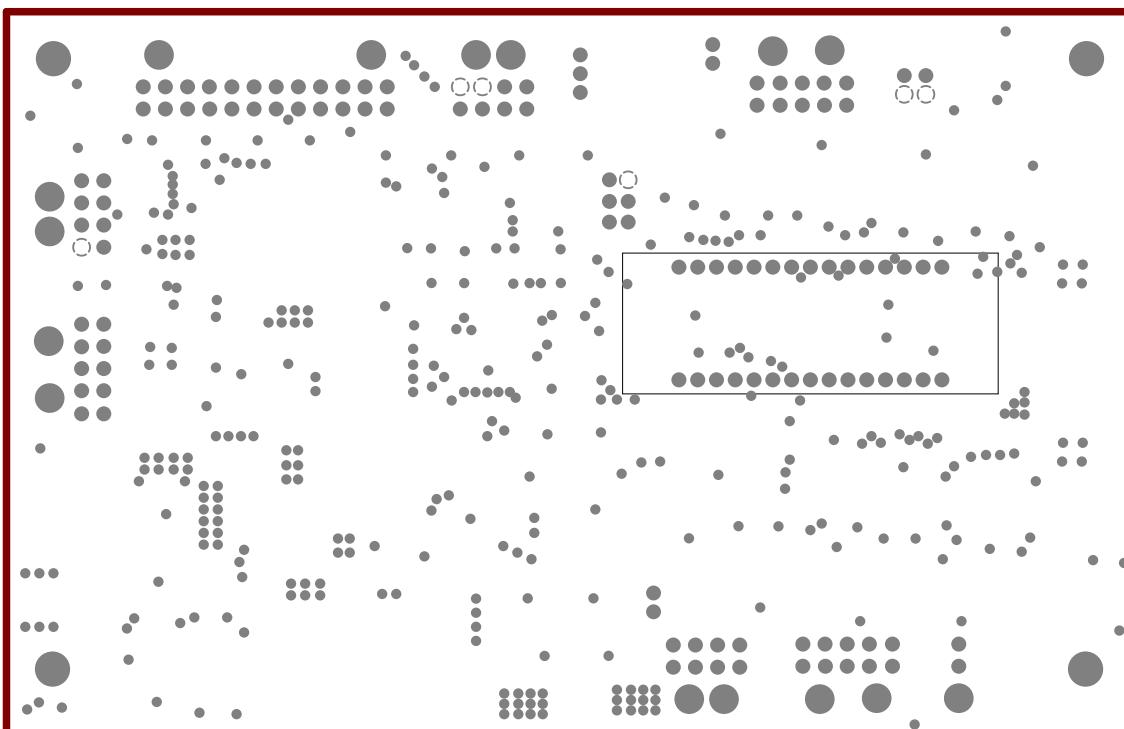
A

A

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 2	FR-4	18.70mil	4.9	
5	GND	Copper	1.40mil		
6	Dielectric 1	FR-4	18.70mil	4.9	
7	PHR	Copper	1.40mil		
8	Dielectric 3	FR-4	18.70mil	4.9	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

B

B



C

C

**BADGER  
LOOP**  
Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
7/9/2020

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO:  
Braking Input Output Controller

REV:  
A

SCALE:  
1:1

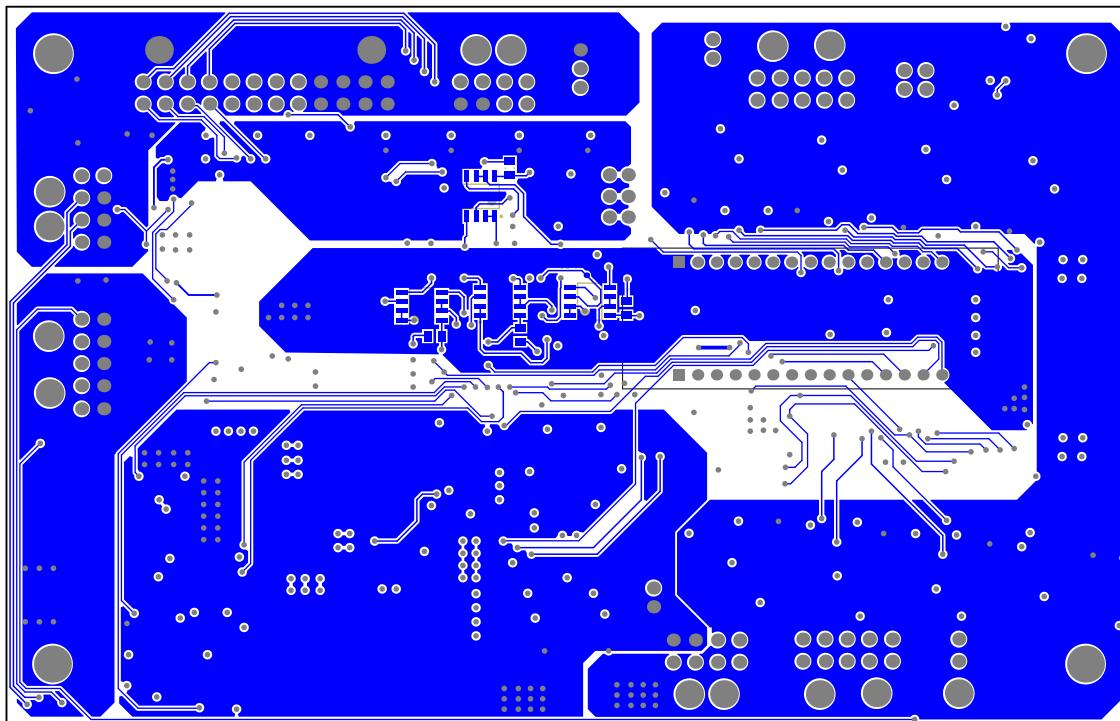
A

A

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 2	FR-4	18.70mil	4.9	
5	GND	Copper	1.40mil		
6	Dielectric 1	FR-4	18.70mil	4.9	
7	PHR	Copper	1.40mil		
8	Dielectric 3	FR-4	18.70mil	4.9	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

B

B



C

C

**BADGER  
LOOP**

Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
7/9/2020

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO:  
Braking Input Output Controller

REV:  
A

SCALE:  
1:1

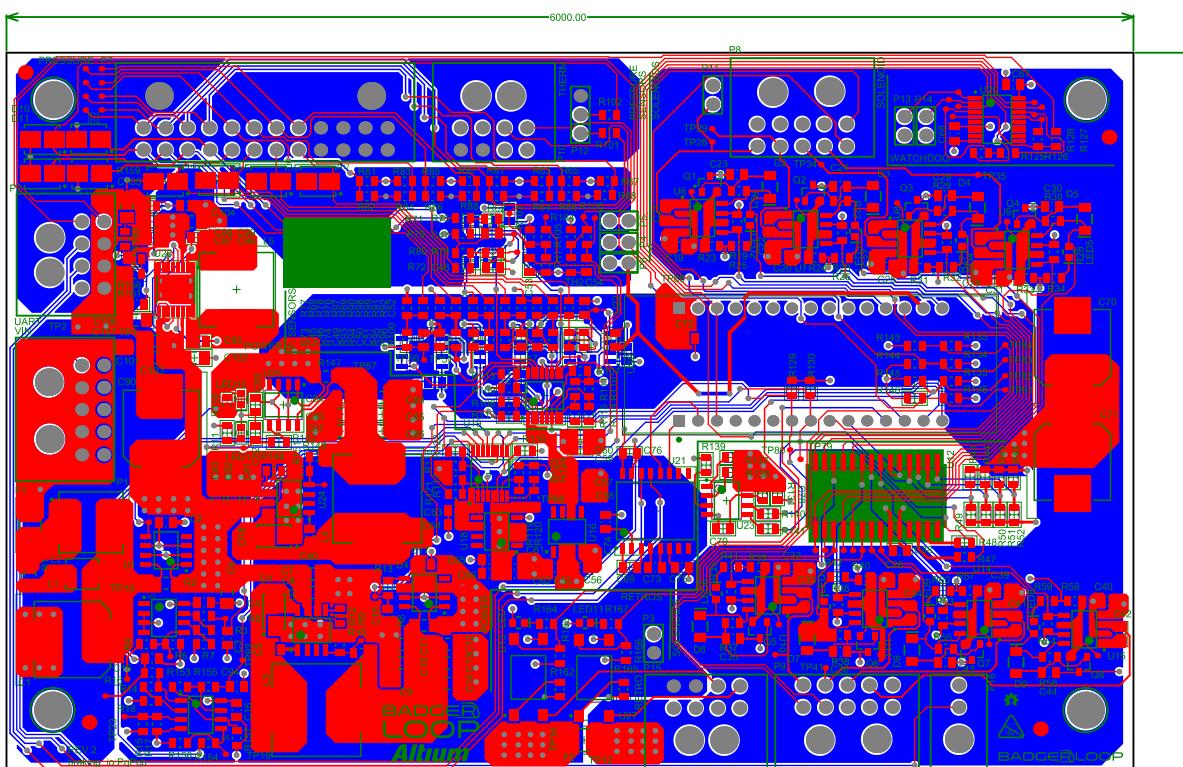
A

A

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 2	FR-4	18.70mil	4.9	
5	GND	Copper	1.40mil		
6	Dielectric 1	FR-4	18.70mil	4.9	
7	PHR	Copper	1.40mil		
8	Dielectric 3	FR-4	18.70mil	4.9	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

B

B



C

C

**BADGER  
LOOP**  
Badgerloop  
ERB Room 133  
1400 Engineering Drive  
Madison, WI 53706

ENGINEER: RCastle, BTobin,  
JESlinger,  
SRiggleman

PCB DESIGNER:  
RCastle, BTobin

DATE:  
7/9/2020

FILE NAME:  
braking\_io.PcbDoc

TITLE:  
**braking\_io.PcbDoc**

PART NO:  
Braking Input Output Controller

REV:  
A

DWG NO:  
SCALE:  
1:1