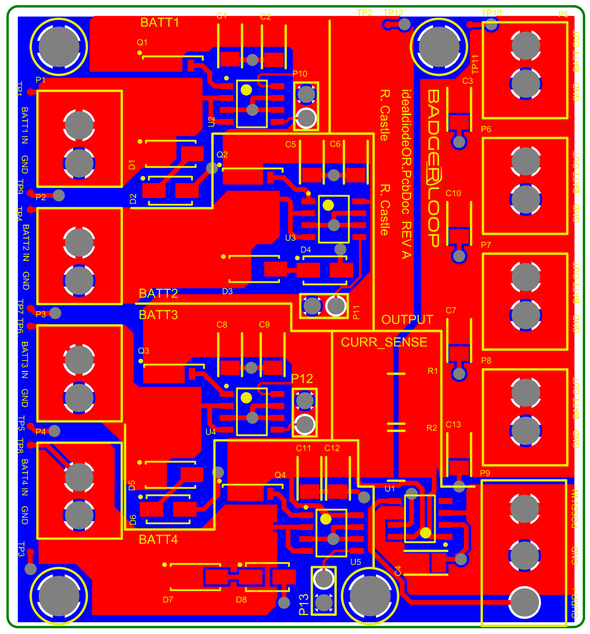
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
▽	24	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v127h71
⊠	8	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c180h100
□	19	59.06mil (1.500mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c300h150
✡	4	102.36mil (2.600mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)
	55 Total							

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				



Bottom Layer

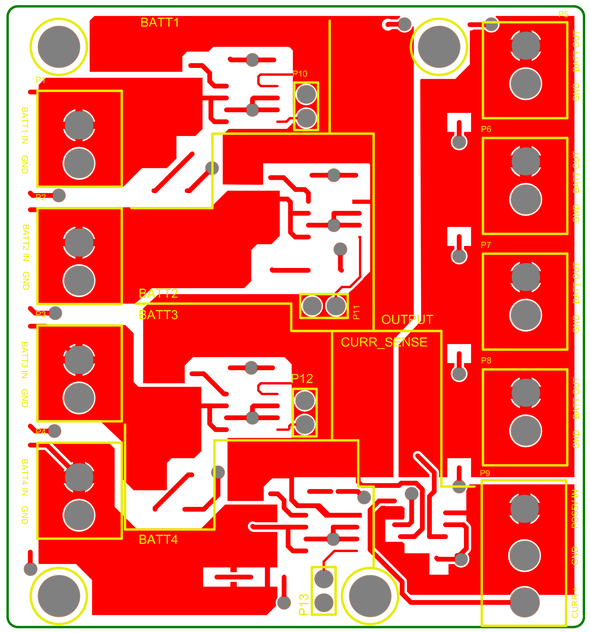
1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
   a. Green Solder Mask Top
   b. Green Solder Mask Bottom
   c. White Silkscreen Top
   d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. Vias are to be covered by soldermask (tented)

Components with througholes are P1, J1, J2, J6, P2, P10, P21, MH1-MH6
All other holes are Vias

BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

ENGINEER: R. Castle	TITLE: idealdiodeOR.PcbDoc		
PCB DESIGNER: R. Castle			
DATE: 1/21/2019	PART NO.: P4_EL_LV_001_IdealDiodeRevA	REV: REV A	
FILE NAME: idealdiodeOR.PcbDoc	DWG NO:	SCALE: 1:1	



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DATE: 1/21/2019	PART NO.: P4_EL_LV_001_IdealDiodeRevA	REV: REV A	
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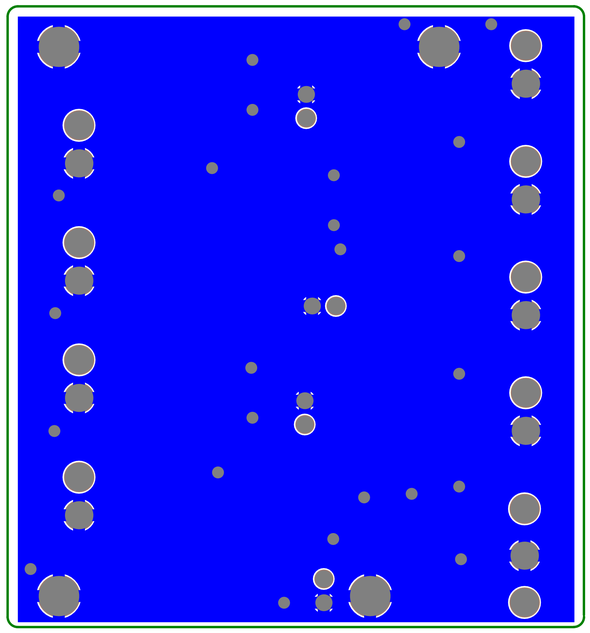

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