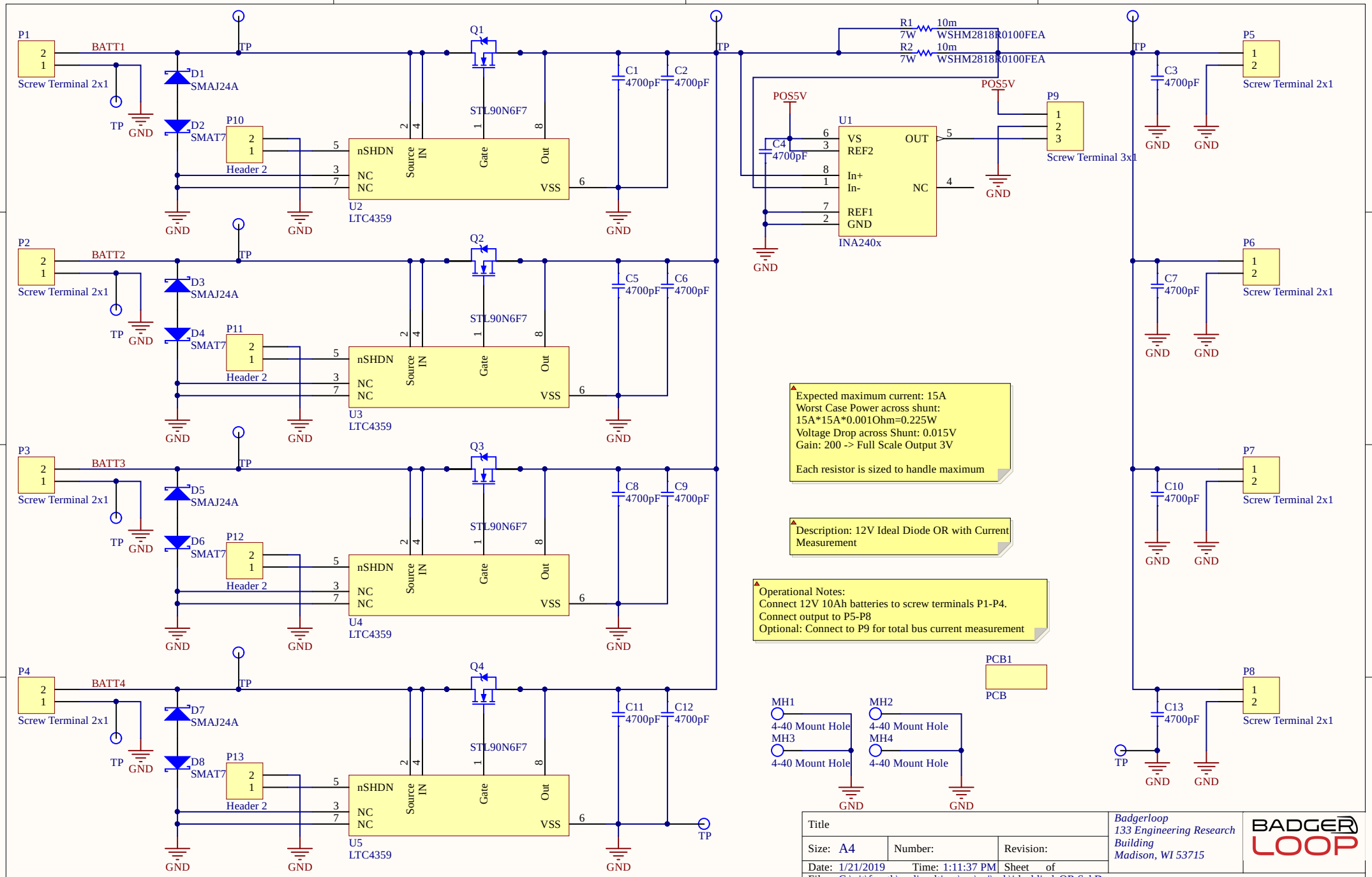
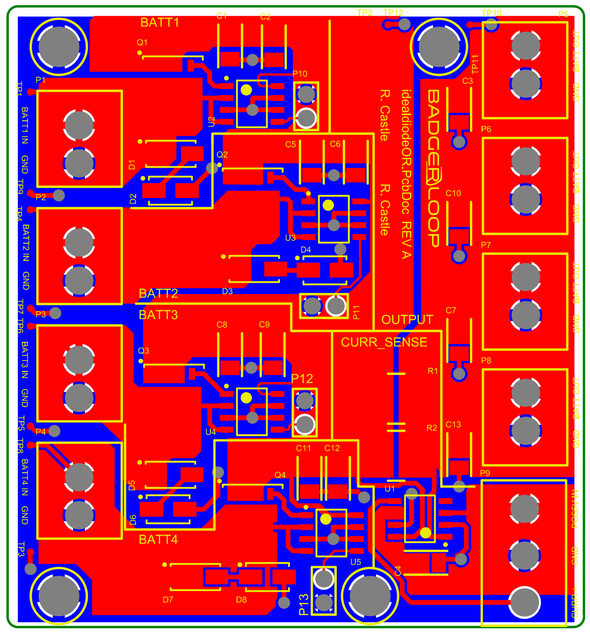

P1
Screw Terminal 2x1
BATT1
D1
SMAJ24A
D2
SMAT7
P10
Header 2
Q1
STL90N6F7
C1
4700pF
C2
4700pF
U2
LTC4359
nSHDN
NC
NC
Source
IN
Gate
Out
VSS
P2
BATT2
D3
SMAJ24A
D4
SMAT7
P11
Header 2
Q2
STL90N6F7
C5
4700pF
C6
4700pF
U3
LTC4359
P3
BATT3
D5
SMAJ24A
D6
SMAT7
P12
Header 2
Q3
STL90N6F7
C8
4700pF
C9
4700pF
U4
LTC4359
P4
BATT4
D7
SMAJ24A
D8
SMAT7
P13
Header 2
Q4
STL90N6F7
C11
4700pF
C12
4700pF
U5
LTC4359
TP
GND
R1
10m
7W
WSHM2818R0100FEA
R2
10m
7W
WSHM2818R0100FEA
POS5V
C4
4700pF
U1
VS
REF2
In+
In-
REF1
GND
OUT
NC
INA240x
P9
Screw Terminal 3x1
P5
Screw Terminal 2x1
C3
4700pF
P6
Screw Terminal 2x1
C7
4700pF
P7
Screw Terminal 2x1
C10
4700pF
P8
Screw Terminal 2x1
C13
4700pF
Expected maximum current: 15A
Worst Case Power across shunt:
15A*15A*0.001Ohm=0.225W
Voltage Drop across Shunt: 0.015V
Gain: 200 -> Full Scale Output 3V
Each resistor is sized to handle maximum
Description: 12V Ideal Diode OR with Current Measurement
Operational Notes:
Connect 12V 10Ah batteries to screw terminals P1-P4.
Connect output to P5-P8
Optional: Connect to P9 for total bus current measurement
PCB1
PCB
MH1
4-40 Mount Hole
MH2
4-40 Mount Hole
MH3
4-40 Mount Hole
MH4
4-40 Mount Hole
Title
Size: A4
Number:
Revision:
Date: 1/21/2019
Time: 1:11:37 PM
Sheet of
File: C:\git\fourth\podiv-altium\src\prj\sch\idealdiodeOR.SchDoc
Badgerloop
133 Engineering Research Building
Madison, WI 53715
BADGER LOOP

| Symbol | Count | Hole Size | Plated | Hole Type | Drill Layer Pair | Via/Pad | Pad Shape | Template |
|---|---|---|---|---|---|---|---|---|
| ▽ | 24 | 28.00mil (0.711mm) | PTH | Round | Top Layer - Bottom Layer | Via | Rounded | v127h71 |
| ⊠ | 8 | 39.37mil (1.000mm) | PTH | Round | Top Layer - Bottom Layer | Pad | Rounded | c180h100 |
| □ | 19 | 59.06mil (1.500mm) | PTH | Round | Top Layer - Bottom Layer | Pad | Rounded | c300h150 |
| ✡ | 4 | 102.36mil (2.600mm) | PTH | Round | Top Layer - Bottom Layer | Pad | Rounded | (Mixed) |
| | 55 Total | | | | | | | |

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| 1 | Top Overlay | | | | |
| 2 | Top Solder | Solder Resist | 0.40mil | 3.5 | |
| 3 | Top Layer | Copper | 1.40mil | | |
| 4 | Dielectric 1 | FR-4 | 12.60mil | 4.8 | |
| 5 | Bottom Layer | Copper | 1.40mil | | |
| 6 | Bottom Solder | Solder Resist | 0.40mil | 3.5 | |
| 7 | Bottom Overlay | | | | |




Bottom Layer

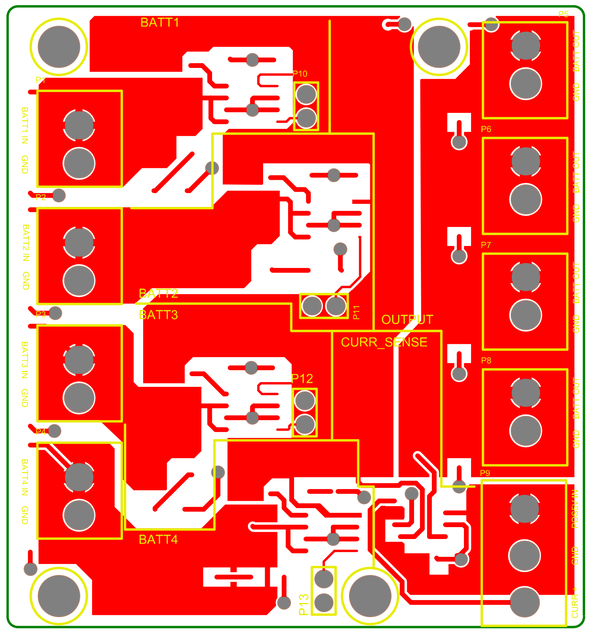
1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
   a. Green Solder Mask Top
   b. Green Solder Mask Bottom
   c. White Silkscreen Top
   d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. Vias are to be covered by soldermask (tented)

Components with througholes are P1, J1, J2, J6, P2, P10, P21, MH1-MH6
All other holes are Vias


BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706


| | | | |
|---|---|---|---|
| ENGINEER: R. Castle | TITLE: idealdiodeOR.PcbDoc | | |
| PCB DESIGNER: R. Castle | | | |
| DATE: 1/21/2019 | PART NO.: P4_EL_LV_001_IdealDiodeRevA | REV: REV A | |
| FILE NAME: idealdiodeOR.PcbDoc | DWG NO: | SCALE: 1:1 | |




Top Layer

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4. Coloring:
   a. Green Solder Mask Top
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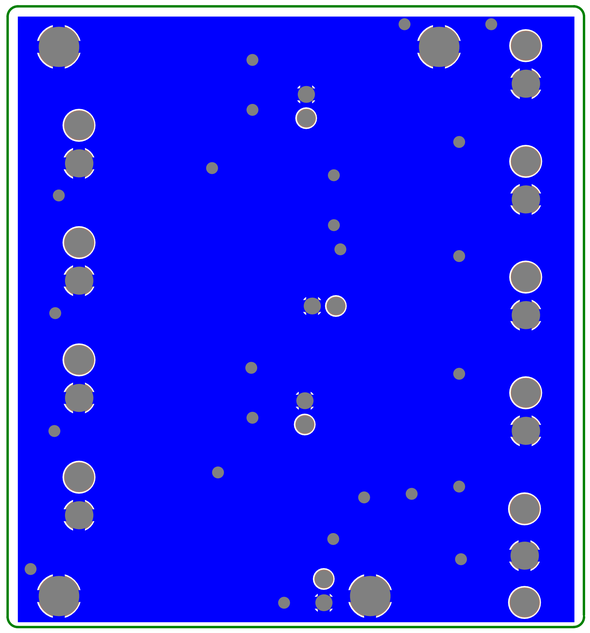
All other holes are Vias

BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

| | | | |
|---|---|---|---|
| ENGINEER: R. Castle | TITLE: idealdiodeOR.PcbDoc | | |
| PCB DESIGNER: R. Castle | | | |
| DATE: 1/21/2019 | PART NO.: P4_EL_LV_001_IdealDiodeRevA | REV: REV A | |
| FILE NAME: idealdiodeOR.PcbDoc | DWG NO: | SCALE: 1:1 | |



Bottom Layer

1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
   a. Green Solder Mask Top
   b. Green Solder Mask Bottom
   c. White Silkscreen Top
   d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. Vias are to be covered by soldermask (tented)
   Components with througholes are P1, J1, J2, J6, P2, P10, P21, MH1-MH6
   All other holes are Vias

BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

| | | | |
|---|---|---|---|
| ENGINEER: R. Castle | TITLE: idealdiodeOR.PcbDoc | | |
| PCB DESIGNER: R. Castle | | | |
| DATE: 1/21/2019 | PART NO.: P4_EL_LV_001_IdealDiodeRevA | REV: REV A | |
| FILE NAME: idealdiodeOR.PcbDoc | DWG NO: | SCALE: 1:1 | |

BATT1
BATT2
BATT3
BATT4
OUTPUT
CURR_SENSE
idealdiodeOR.PcbDoc REV A
R. Castle
R. Castle
BADGERLOOP
P1
P2
P3
P4
P6
P7
P8
P9
P10
P11
P12
P13
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
R1
R2
U1
U2
U3
U4
U5
Q1
Q2
Q3
Q4
D1
D2
D3
D4
D5
D6
D7
D8
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP11
TP12
BATT1 IN
BATT2 IN
BATT3 IN
BATT4 IN
GND
BATT OUT
POSSV IN
CURR +