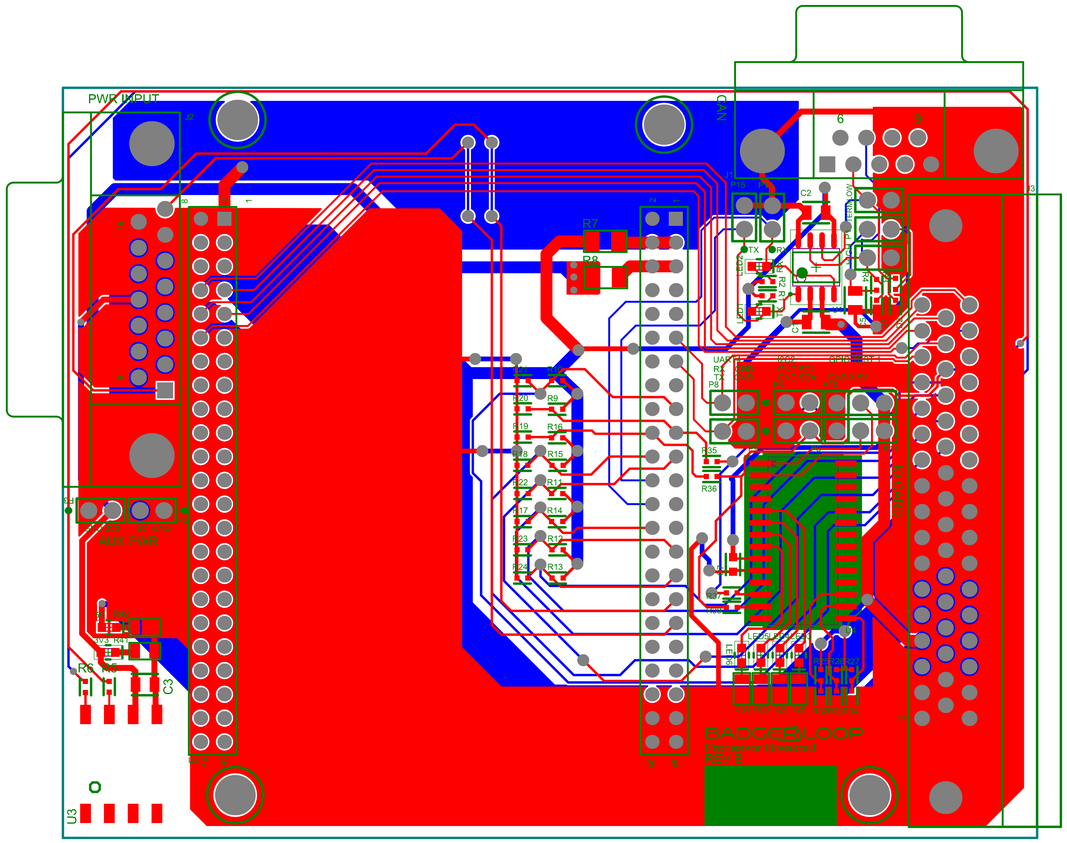
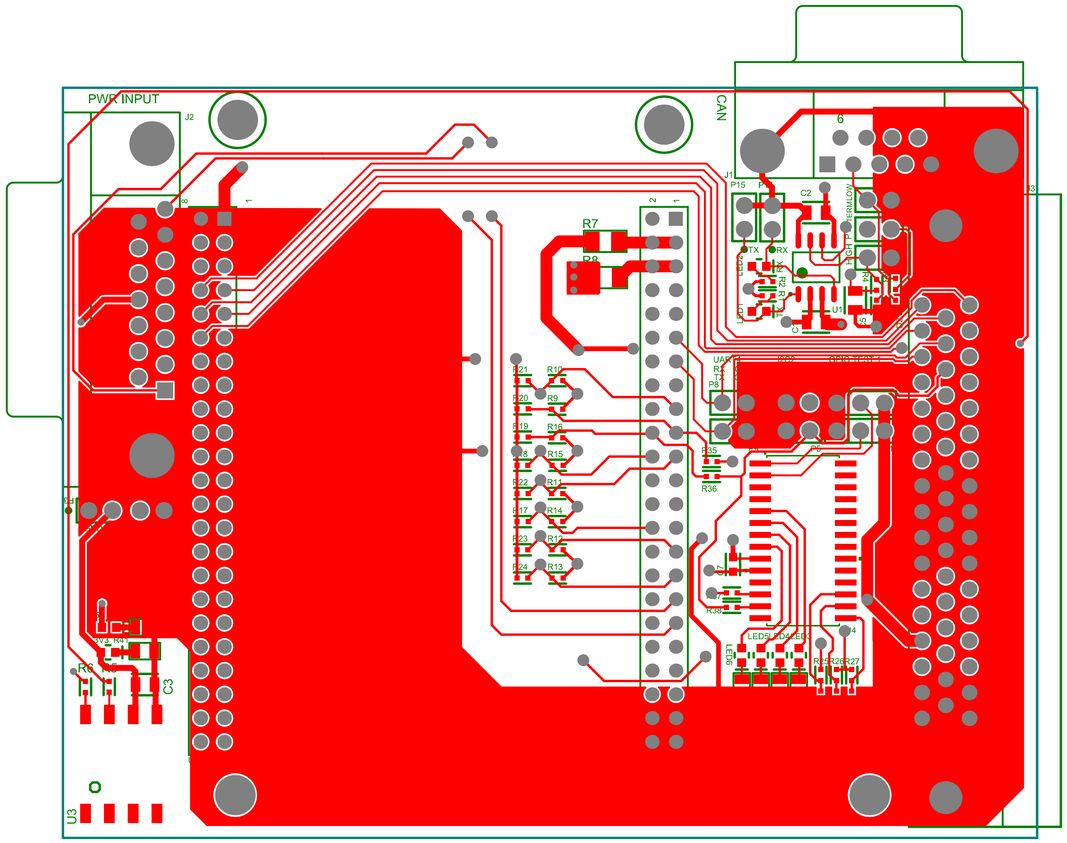
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
□	8	15.00mil (0.381mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v76h38
▼	38	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v127h71
✿	92	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
✡	28	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c180h100
○	24	42.91mil (1.090mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
◇	50	43.31mil (1.100mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c165h110
▣	4	116.00mil (2.946mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c430hn295
⊠	2	122.05mil (3.100mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c351h310
✡	2	125.20mil (3.180mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c480h318
▽	2	128.35mil (3.260mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c476h326
	250 Total							

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				



Bottom Layer

BADGER LOOP Badgerloop ERB Room 133 1400 Engineering Drive Madison, WI 53706	ENGINEER: R. Castle	TITLE: processor_pcb.PcbDoc	
	PCB DESIGNER: R. Castle		
	DATE: 3/23/2019	PART NO.: P4_LV_Processor	REV: A
	FILE NAME: processor_pcb.PcbDoc	DWG NO:	SCALE: 1:1



Top Layer

BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

ENGINEER: R. Castle	TITLE: processor_pcb.PcbDoc		
PCB DESIGNER: R. Castle			
DATE: 3/23/2019	PART NO.: P4_LV_Processor	REV: A	
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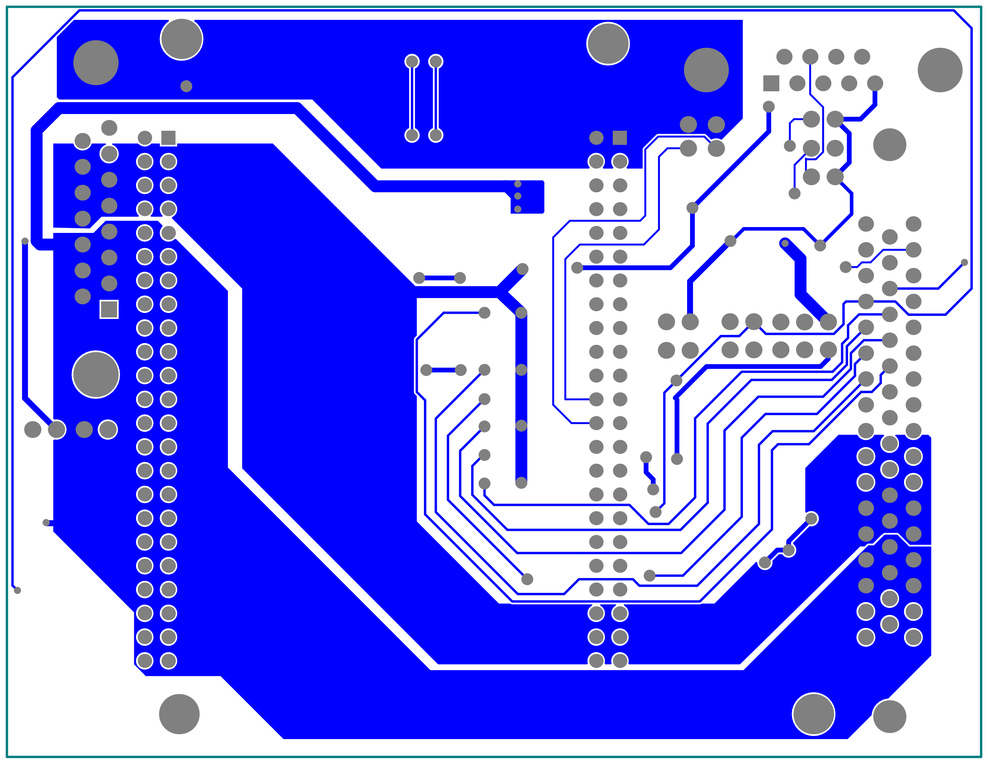

Bottom Layer

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