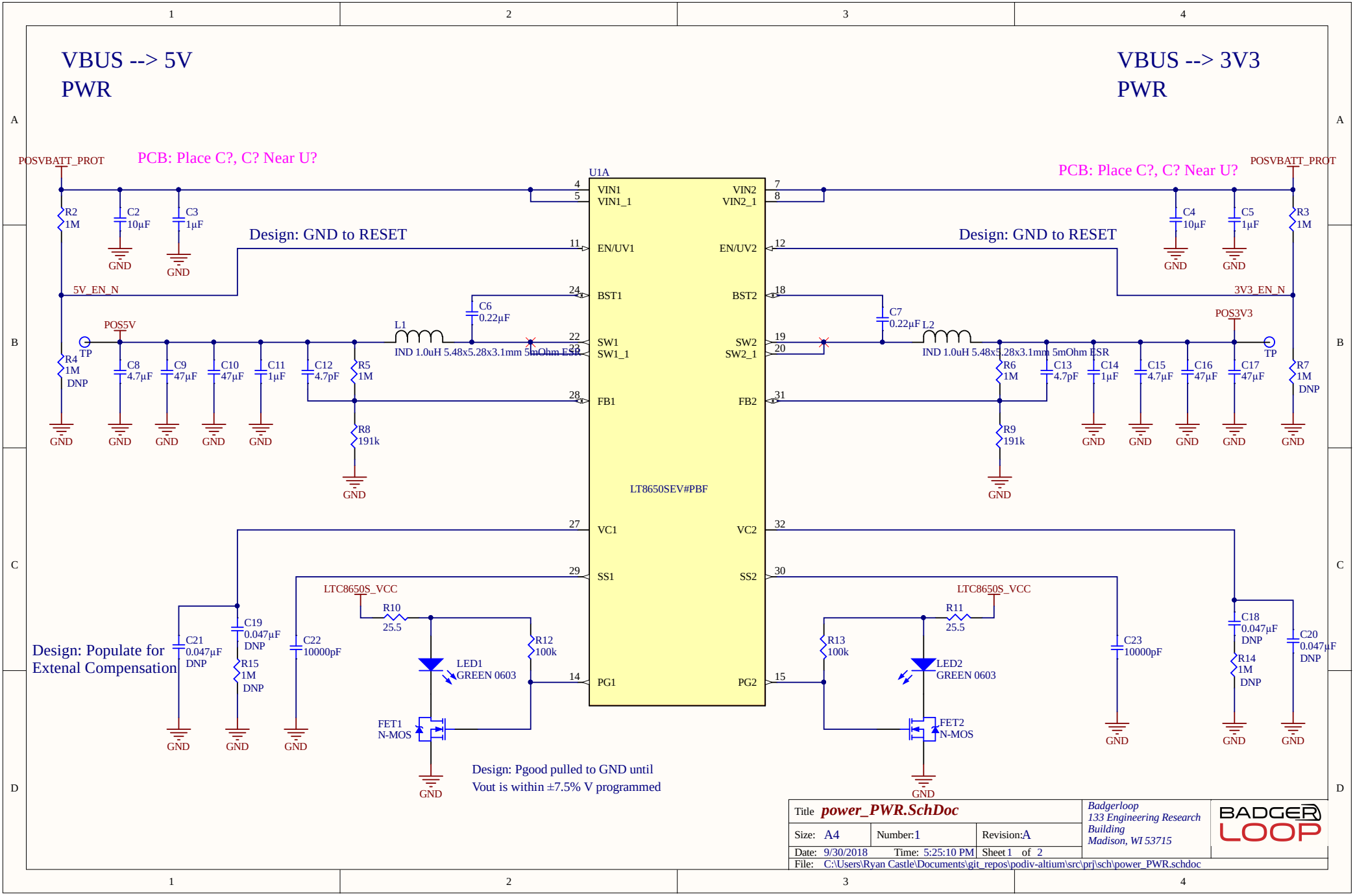
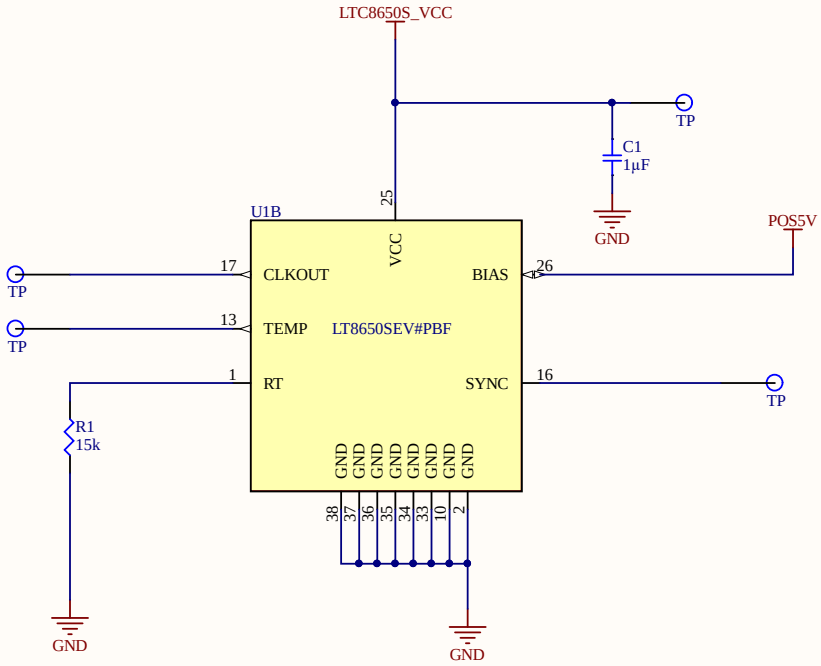
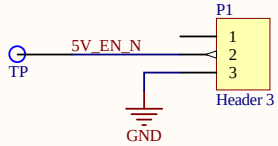

VBUS --> 5V
PWR
VBUS --> 3V3
PWR
POSVBATT_PROT
PCB: Place C?, C? Near U?
U1A
VIN1
VIN1_1
VIN2
VIN2_1
EN/UV1
EN/UV2
BST1
BST2
SW1
SW1_1
SW2
SW2_1
FB1
FB2
VC1
VC2
SS1
SS2
PG1
PG2
LT8650SEV#PBF
Design: GND to RESET
5V_EN_N
3V3_EN_N
POS5V
POS3V3
L1
L2
IND 1.0uH 5.48x5.28x3.1mm 5mOhm ESR
R2 1M
C2 10µF
C3 1µF
C4 10µF
C5 1µF
R3 1M
R4 1M DNP
C6 0.22µF
C7 0.22µF
R5 1M
R6 1M
R7 1M DNP
R8 191k
R9 191k
C8 4.7µF
C9 47µF
C10 47µF
C11 1µF
C12 4.7pF
C13 4.7pF
C14 1µF
C15 4.7µF
C16 47µF
C17 47µF
TP
GND
LTC8650S_VCC
R10 25.5
R11 25.5
R12 100k
R13 100k
LED1 GREEN 0603
LED2 GREEN 0603
FET1 N-MOS
FET2 N-MOS
C18 0.047µF DNP
C19 0.047µF DNP
C20 0.047µF DNP
C21 0.047µF DNP
C22 10000pF
C23 10000pF
R14 1M DNP
R15 1M DNP
Design: Populate for Extenal Compensation
Design: Pgood pulled to GND until Vout is within ±7.5% V programmed
Title power_PWR.SchDoc
Size: A4
Number: 1
Revision: A
Date: 9/30/2018
Time: 5:25:10 PM
Sheet 1 of 2
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PWR.schdoc
Badgerloop
133 Engineering Research Building
Madison, WI 53715
BADGER LOOP

VBUS --> 5V
VBUS --> 3V3
CONTROL

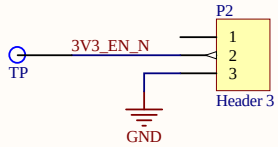
Design: Soft-Start Time TBD
Design: Switching Frequency 2MHz
Design: FCM W/O SSM OR SYNC

Design: LT8650S
Vout1: 5V 4A
Vout2: 3.3V 4A





Operation: Float *_EN_N
TO ENABLE, GND TO DISABLE



TODO: Should we do a 3 input OR Gate for PGoods?

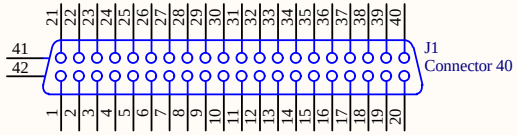
Title	***power_CTL.schdoc***		*Badgerloop 133 Engineering Research Building Madison, WI 53715*
Size: A4	Number: 1	Revision: A	
Date: 9/30/2018	Time: 5:25:10 PM	Sheet 1 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_CTL.schdoc			

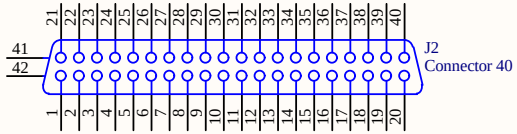
MH1
#10 Mount Hole

MH2
#10 Mount Hole

MH3
#10 Mount Hole

MH
#10 Mount Hole





Title	***nav_main_connector.schdoc***		
Size: A4	Number: 1	Revision: A	
Date: 9/30/2018	Time: 5:25:10 PM	Sheet 2 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_main_connector.SchDoc			

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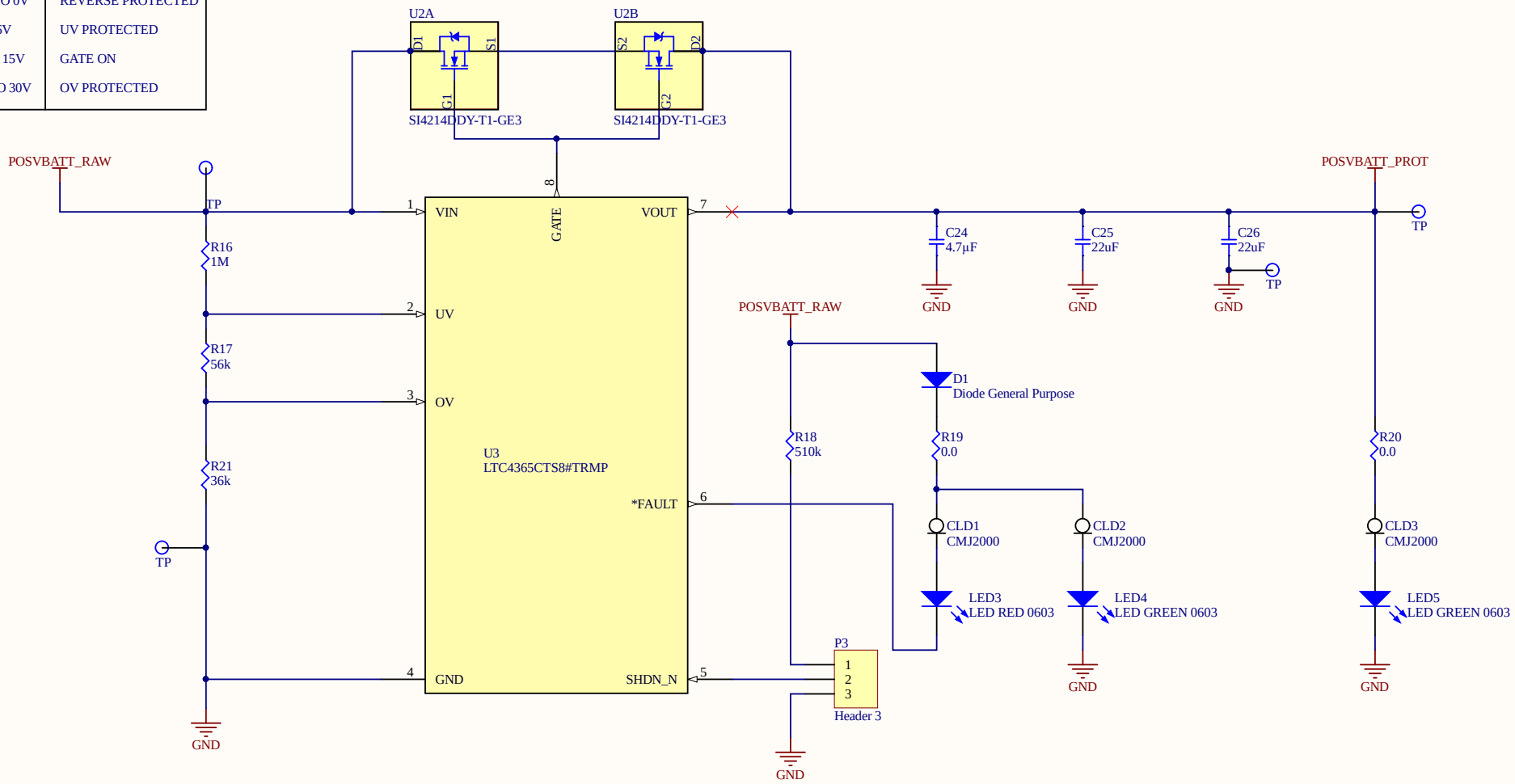
BADGER LOOP

DESIGN:

VIN	VOUT
-30 TO 0V	REVERSE PROTECTED
0 to 6V	UV PROTECTED
6 TO 15V	GATE ON
15 TO 30V	OV PROTECTED



Title	***power_PROTECTION.SchDoc***		
Size: A4	Number:	Revision:	
Date: 9/30/2018	Time: 5:25:10 PM	Sheet of	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PROTECTION.SchDoc			

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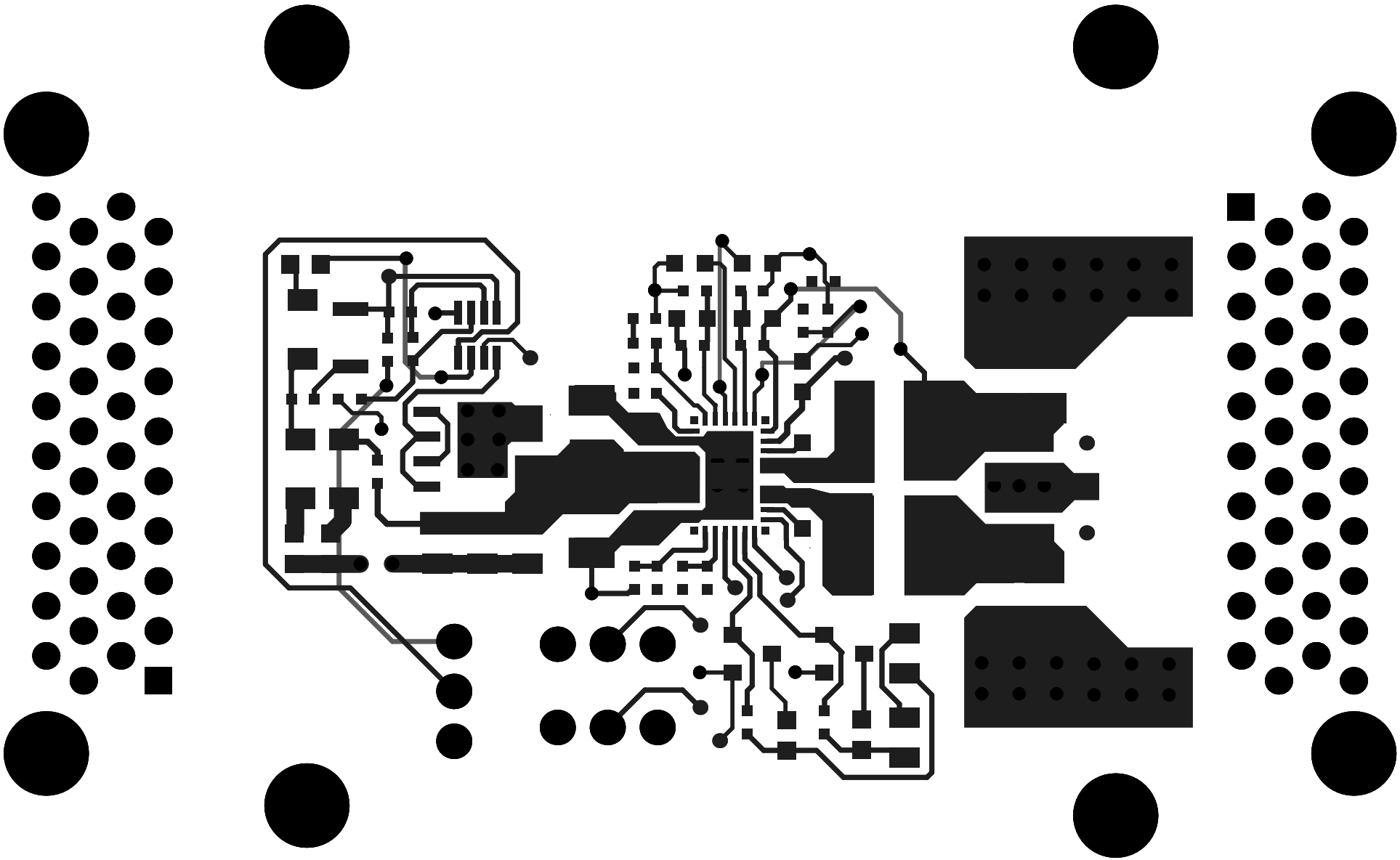
BADGER LOOP



Bill of Materials

Source Data From: power_project.PrjPCB
Project: power_project.PrjPCB
Variant: None

Calculate Pricing
Resize Rows/Shade

Creation Date: 9/30/2018 5:25:21 PM
Print Date: 30-Sep-18 5:25:44 PM
Production Quantity: 1
Currency <none>

Unhide/Hide Supplier 1
Unhide/Hide Supplier 2
Unhide/Hide Assem Manf

Reference	Designator	Description	Manufacturer	#Column Name Erro	Quantity	#Column Name Error:Supplier 1	#Column Name Err	#Column Name Err	Supplier Unit Price 1	Supplier 1 Subtotal	#Column Name Error:Supplier 2	#Column Name Erro	#Column Name Error:	Supplier Unit Price 2	Supplier 2 Subtotal	#Column Name Error	#Column N	#Column N	Assem Unit	Assem Sub
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					84					$ -					$ -					$ -

Approved

Notes