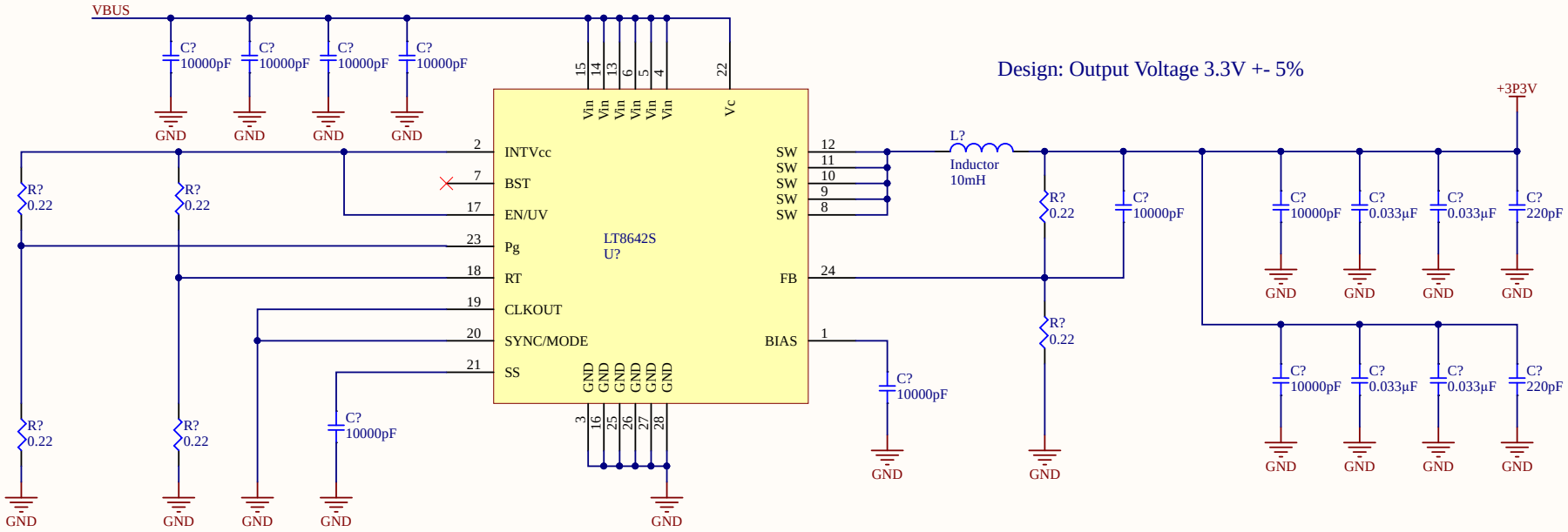
VBUS --> 3.3V

PCB: Place Input Caps near Regulator



Design: Output Voltage 3.3V +- 5%

Design: Soft-Start Time TBD
Design: Switching Frequency TBD
Design: No Sync

Title	POS3P3V.schdoc		
Size: A4	Number:1	Revision:A	
Date: 9/18/2018	Time: 9:46:51 PM	Sheet 1 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\POS53V3.schdoc			

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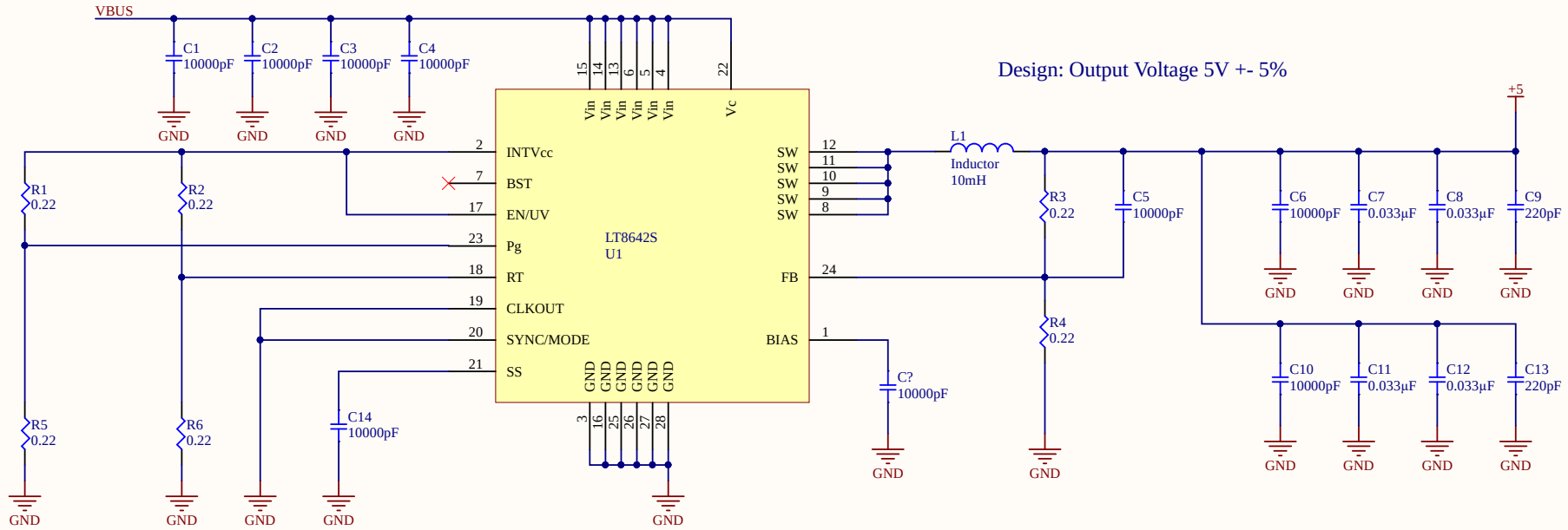
BADGER LOOP

VBUS --> 5V

PCB: Place Input Caps near Regulator



Design: Output Voltage 5V +- 5%

Design: Soft-Start Time TBD
Design: Switching Frequency TBD
Design: No Sync

Title	*POS5V.schdoc*		*Badgerloop 133 Engineering Research Building Madison, WI 53715*
Size: A4	Number:1	Revision:A	
Date: 9/18/2018	Time: 9:46:52 PM	Sheet 1 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\POS5V.schdoc			

Title	*processor_main_connector.schdoc*		
Size: A4	Number:1	Revision:A	
Date: 9/18/2018	Time: 9:46:52 PM	Sheet 2 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\processor_main_connector.SchDoc			

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