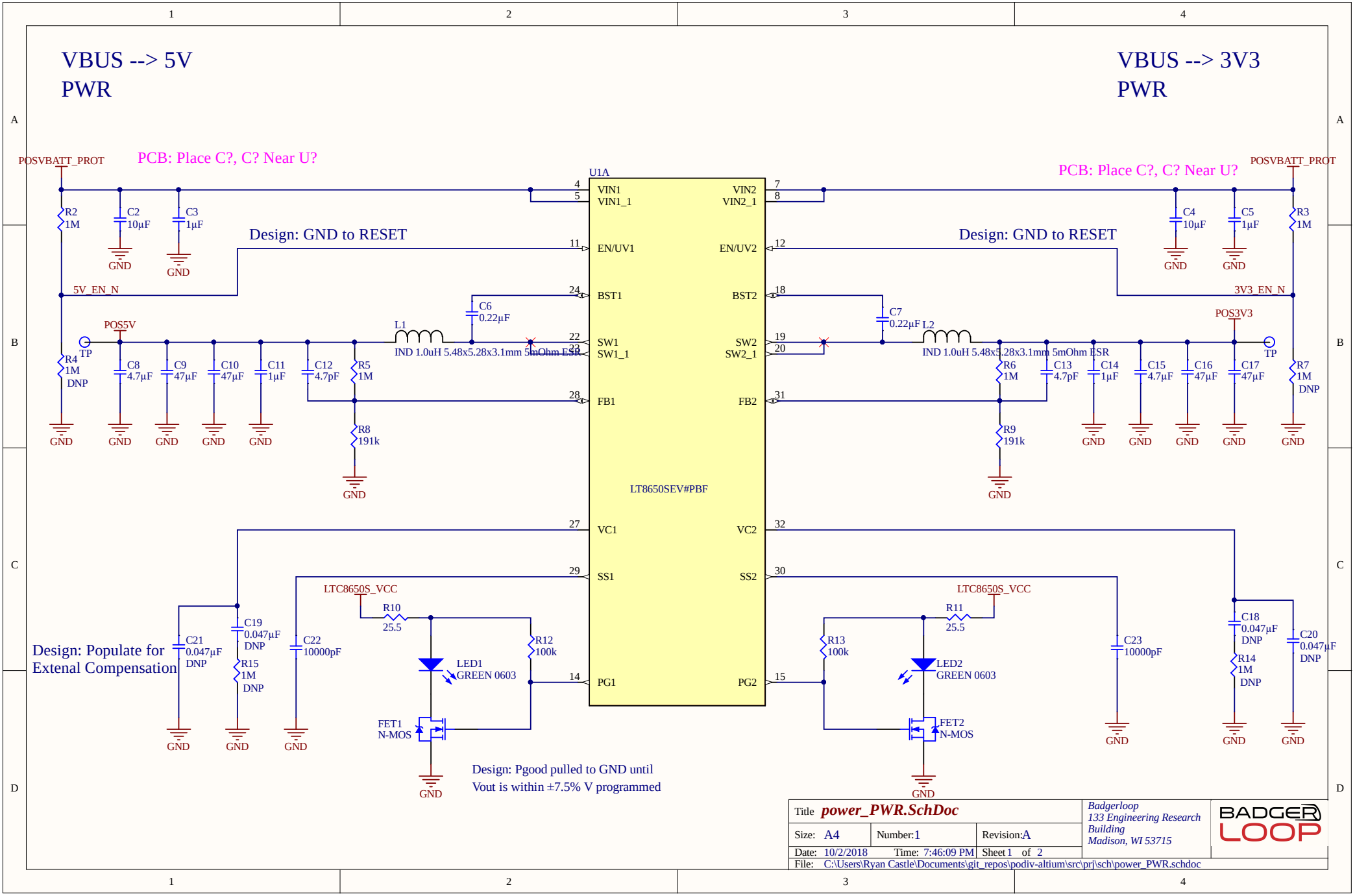
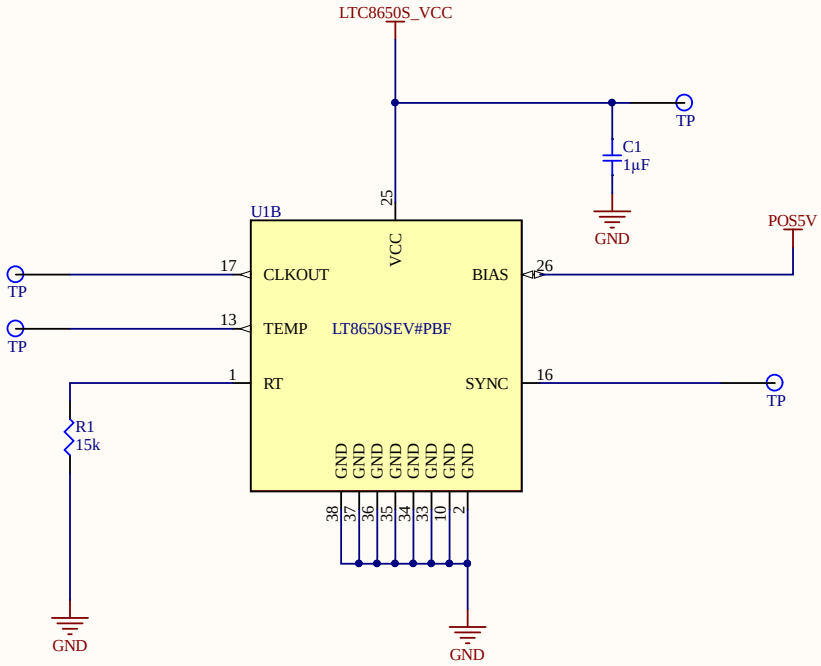


Title	***power_PWR.SchDoc***		
Size: A4	Number: 1	Revision: A	*Badgerloop* *133 Engineering Research Building* *Madison, WI 53715*
Date: 10/2/2018	Time: 7:46:09 PM	Sheet 1 of 2	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PWR.schdoc			

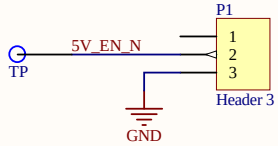
VBUS --> 5V
VBUS --> 3V3
CONTROL

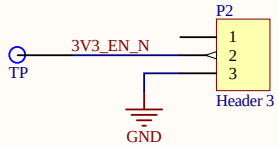
Design: Soft-Start Time TBD
Design: Switching Frequency 2MHz
Design: FCM W/O SSM OR SYNC

Design: LT8650S
Vout1: 5V 4A
Vout2: 3.3V 4A



Operation: Float *_EN_N
TO ENABLE, GND TO DISABLE





TODO: Should we do a 3 input OR Gate for PGoods?

Title	***power_CTL.schdoc***		*Badgerloop 133 Engineering Research Building Madison, WI 53715*
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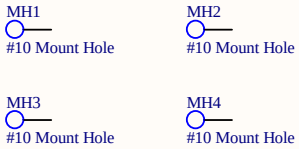
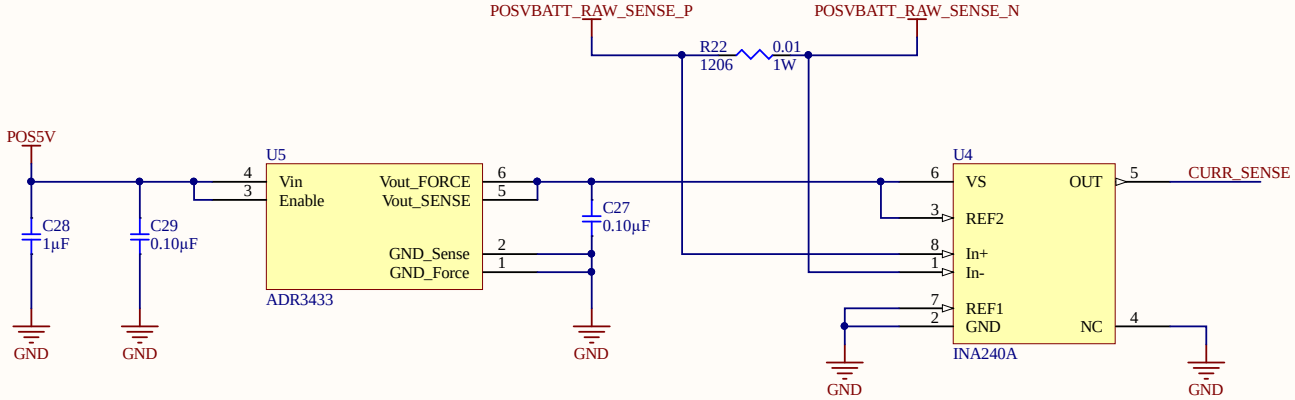
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_CTL.schdoc			

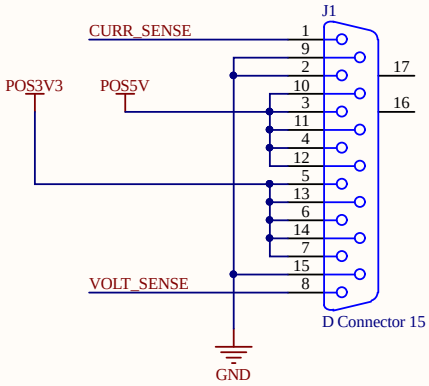


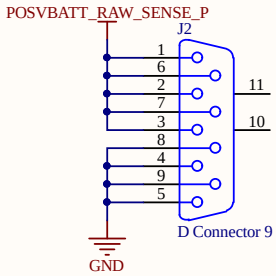
Mount Hole

PCB: Kelvin Connection back to U4

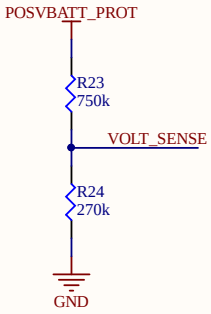


Current Sense





Connector



Current Sense

Note: Tons of better ways to do this...

Title	***nav_main_connector.schdoc***		*Badgerloop* *133 Engineering Research Building* *Madison, WI 53715*
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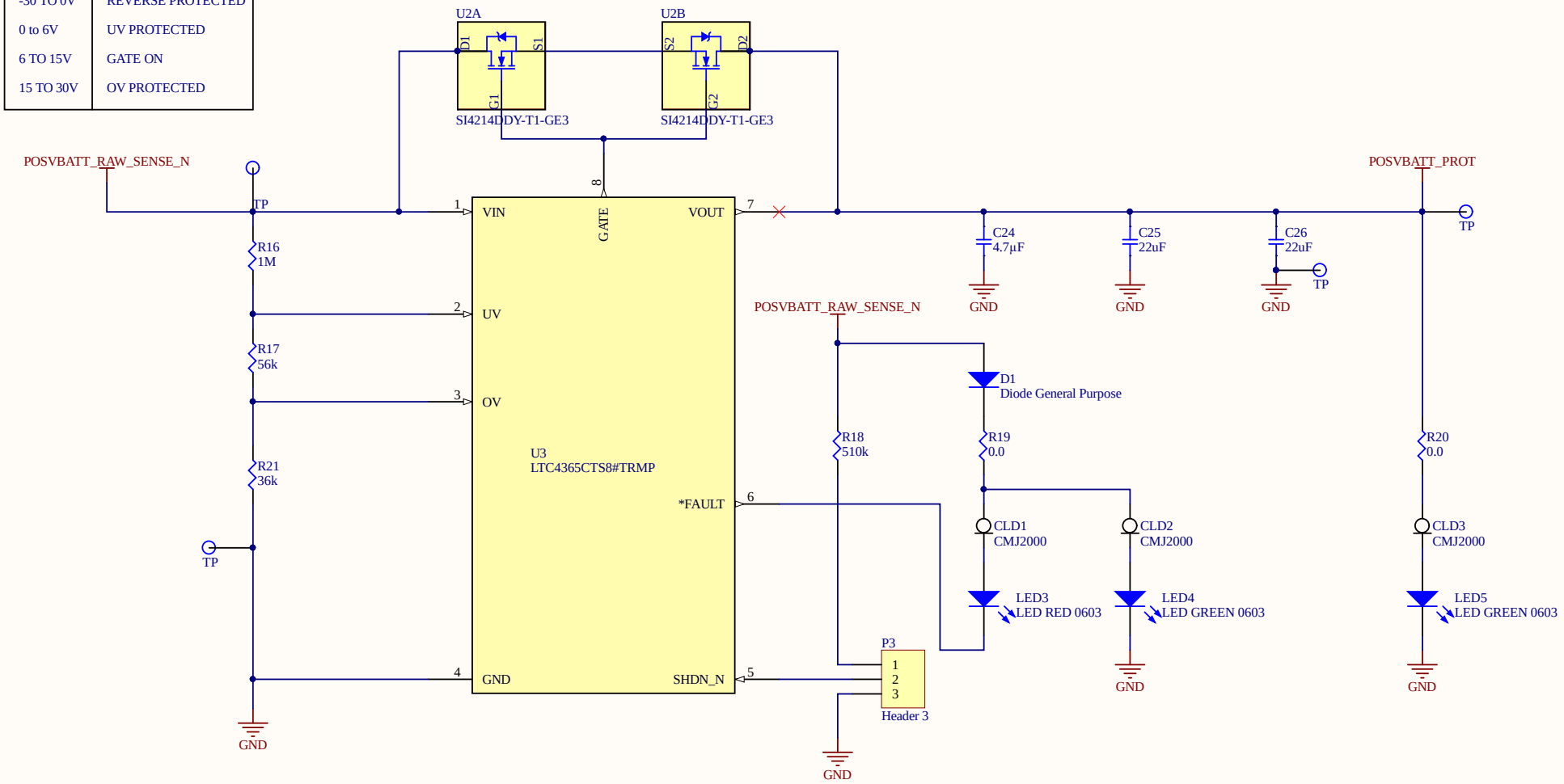
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_main_connector.SchDoc			

DESIGN:

VIN	VOUT
-30 TO 0V	REVERSE PROTECTED
0 to 6V	UV PROTECTED
6 TO 15V	GATE ON
15 TO 30V	OV PROTECTED



Title	***power_PROTECTION.SchDoc***		
Size: A4	Number:	Revision:	
Date: 10/2/2018	Time: 7:46:09 PM	Sheet of	
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PROTECTION.SchDoc			

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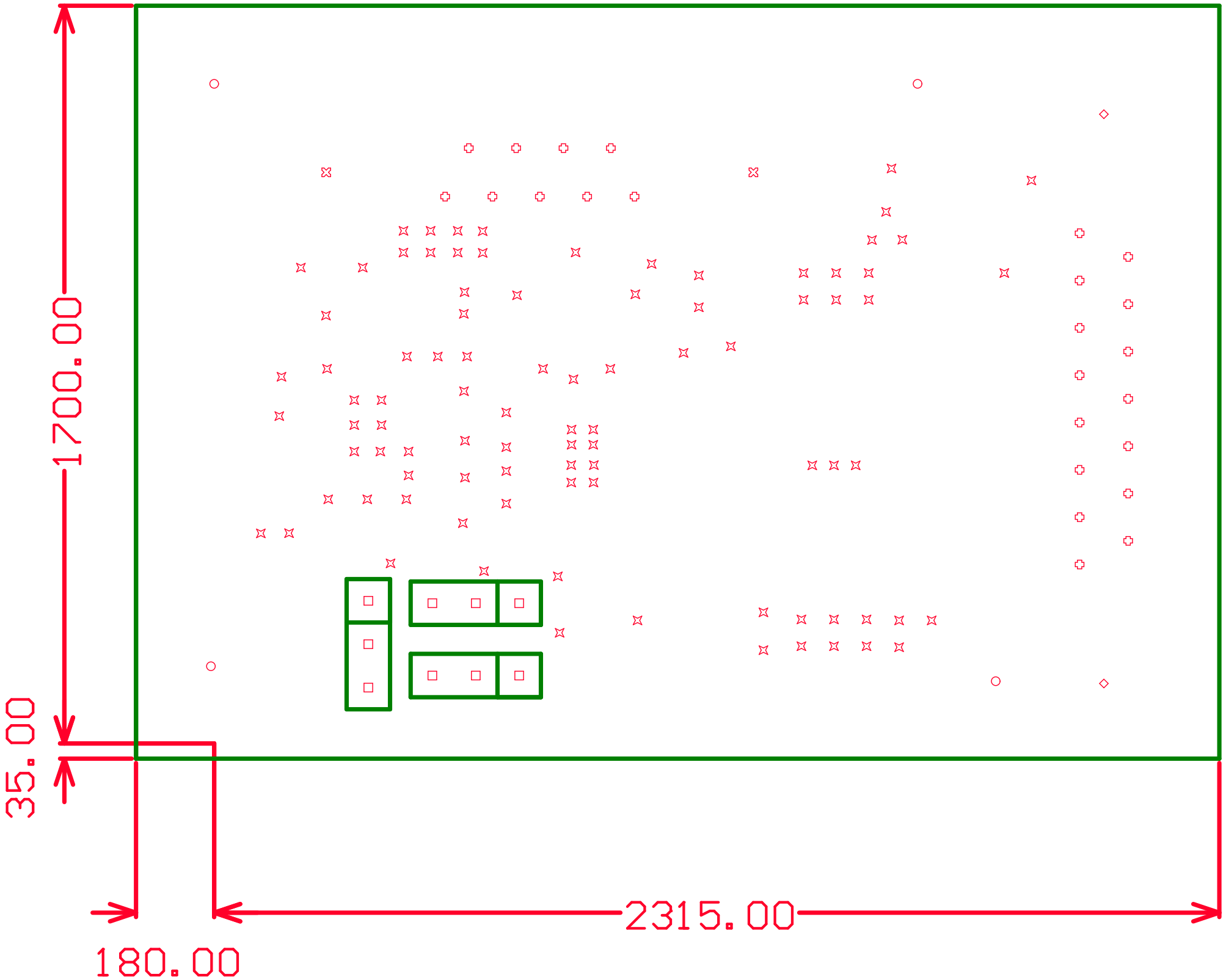
133 Engineering Research Building
Madison, WI 53715

BADGER LOOP


1700.00
35.00
180.00
2315.00