

VBUS --> 5V  
PWR

VBUS --> 3V3  
PWR

PCB: Place C?, C? Near U?

PCB: Place C?, C? Near U?

Design: GND to RESET

Design: GND to RESET

Design: Populate for  
External Compensation

Design: Pgood pulled to GND until  
Vout is within  $\pm 7.5\%$  V programmed

Title <b><i>power_PWR.SchDoc</i></b>		
Size: <b>A4</b>	Number: <b>1</b>	Revision: <b>A</b>
Date: <b>2/4/2019</b>	Time: <b>11:01:31 PM</b> Sheet <b>1</b> of <b>2</b>	
File: <b>C:\git\ fifth\podiv-altium\src\prj\sch\power_PWR.schdoc</b>		

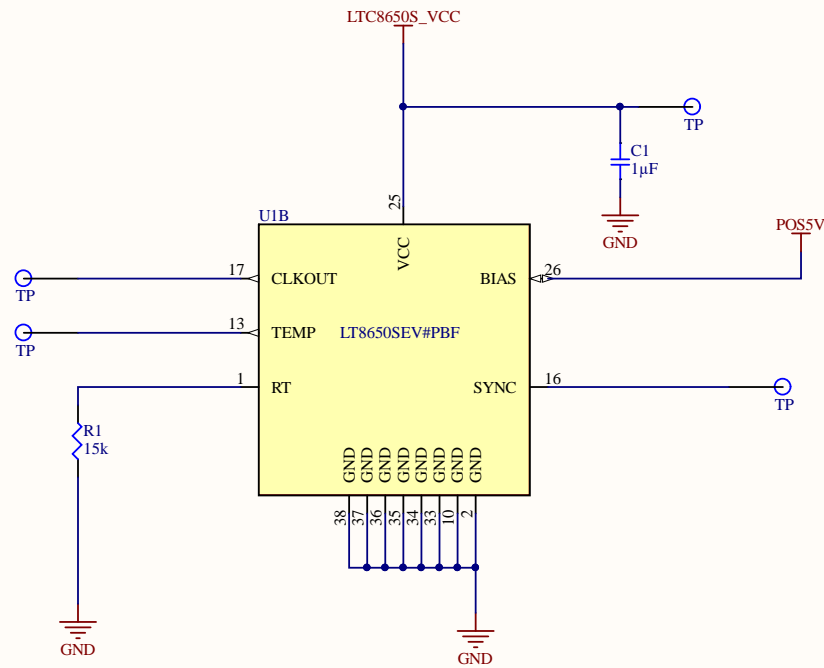
Badgerloop  
133 Engineering Research  
Building  
Madison, WI 53715

**BADGER  
LOOP**

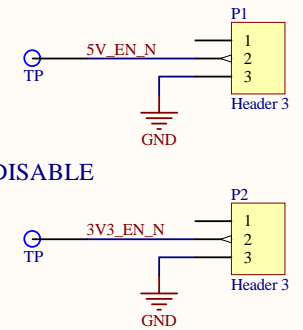
VBUS --> 5V  
VBUS --> 3V3  
CONTROL

Design: Soft-Start Time TBD  
Design: Switching Frequency 2MHz  
Design: FCM W/O SSM OR SYNC


Design: LT8650S  
Vout1: 5V 4A  
Vout2: 3.3V 4A

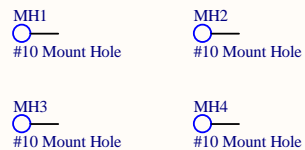


Operation: Float \*\_EN\_N  
TO ENABLE, GND TO DISABLE

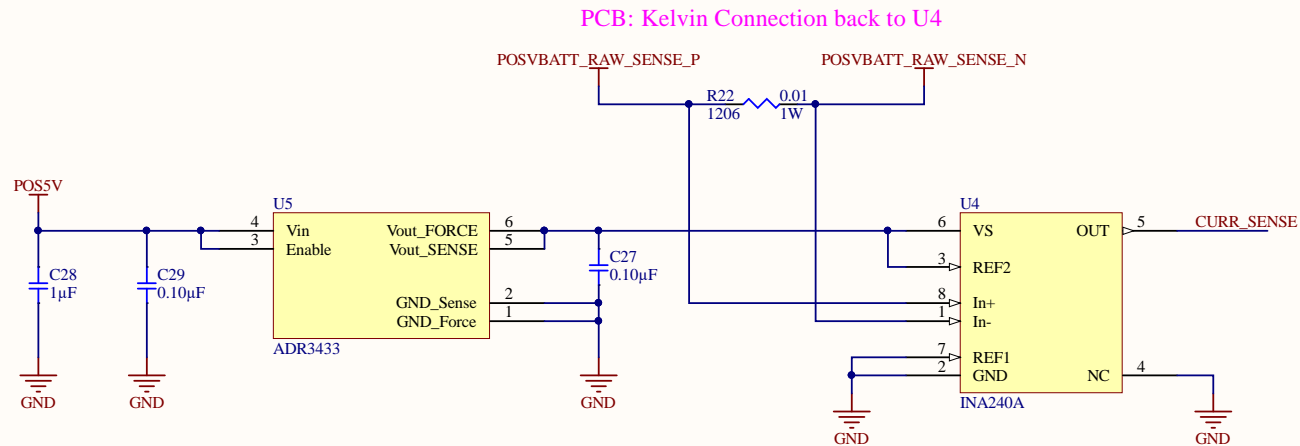


TODO: Should we do a 3 input OR Gate for PGoods?

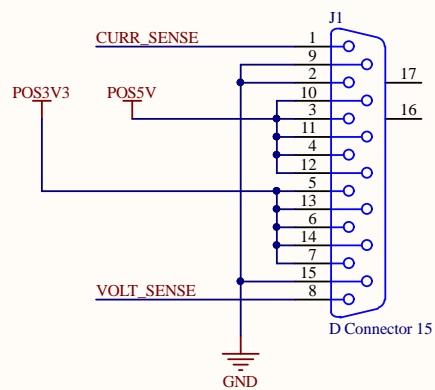
Title <i><b>power_CTL.schdoc</b></i>			Badgerloop 133 Engineering Research Building Madison, WI 53715 
Size: <b>A4</b>	Number: 1	Revision: <b>A</b>	
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File: C:\git\ fifth\podiv-altium\src\prj\sch\power_CTL.schdoc			



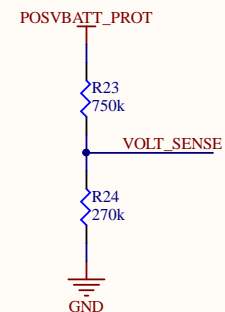
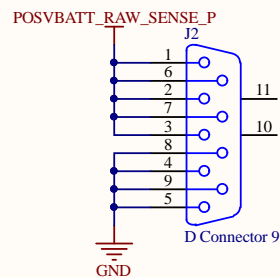
Mount Hole



Current Sense



Connector



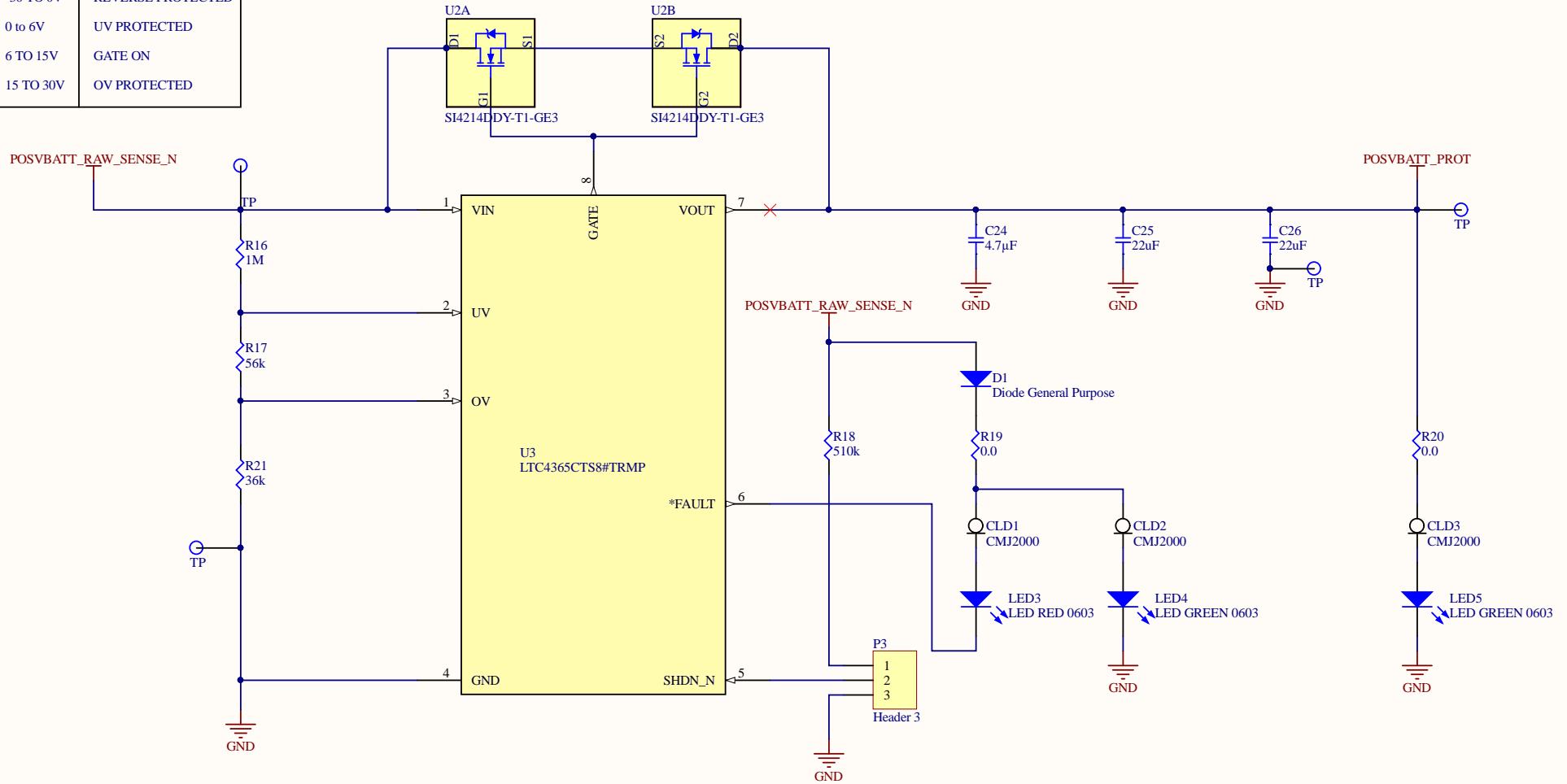
Current Sense

Note: Tons of better ways to do this...

Title <i>nav_main_connector.schdoc</i>			Badgerloop 133 Engineering Research Building Madison, WI 53715  <b>BADGER LOOP</b>
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## DESIGN:

VIN	VOUT
-30 TO 0V	REVERSE PROTECTED
0 to 6V	UV PROTECTED
6 TO 15V	GATE ON
15 TO 30V	OV PROTECTED

Title **power\_PROTECTION.SchDoc**Size: **A4**

Number:

Revision:

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File: C:\git\ fifth\podiv-altium\src\prj\sch\power\_PROTECTION.SchDoc

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