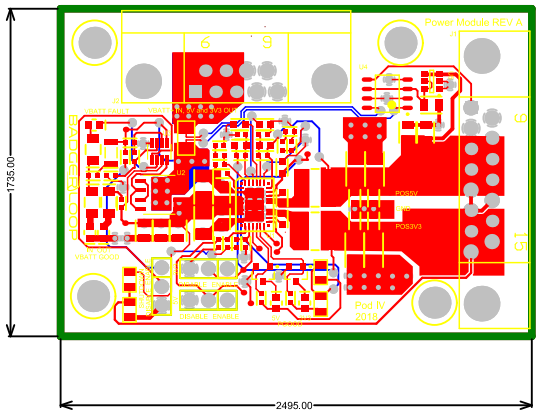
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1_Top	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	L2_GND	Copper	1.42mil		
6	Dielectric 3		5.00mil	4.2	
7	L3_POWER	Copper	1.42mil		
8	Dielectric 4	FR-4	10.00mil	4.2	
9	L4_Bottom	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
   a. Green Solder Mask Top
   b. Green Solder Mask Bottom
   c. White Silkscreen Top
   d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. Vias are to be covered by soldermask (tented)
   Components with througholes are J1, J2, P1-P3, MH1-MH4
   All other holes are vias



BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

ENGINEER: R. Castle	TITLE: power_pcb.PcbDoc		
PCB DESIGNER: R. Castle			
DATE: 2/4/2019	PART NO.: P4_LV_Power	REV: A	
FILE NAME: power_pcb.PcbDoc	DWG NO:	SCALE: 1:1	

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10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
◇	2	125.20mil (3.180mm)	PTH	Round	L1_Top - L4_Bottom	Pad	Rounded	c480h318			
⊠	2	128.35mil (3.260mm)	PTH	Round	L1_Top - L4_Bottom	Pad	Rounded	c476h326			
▽	4	116.00mil (2.946mm)	NPTH	Round	L1_Top - L4_Bottom	Pad	Rounded	c430hn295			
□	9	39.37mil (1.000mm)	PTH	Round	L1_Top - L4_Bottom	Pad	Rounded	c180h100			
⌬	24	42.91mil (1.090mm)	PTH	Round	L1_Top - L4_Bottom	Pad	(Mixed)	(Mixed)			
⌘	90	10.00mil (0.254mm)	PTH	Round	L1_Top - L4_Bottom	Via	Rounded	v69h25			
	131 Total										

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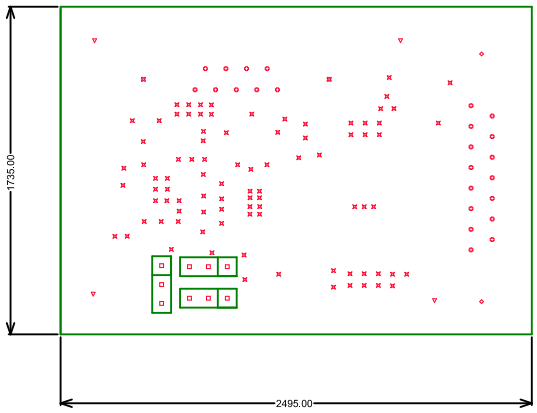

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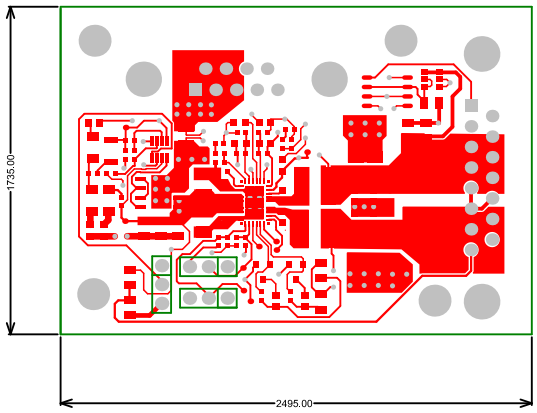

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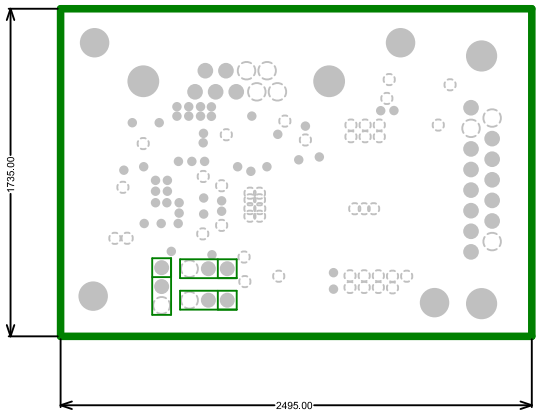

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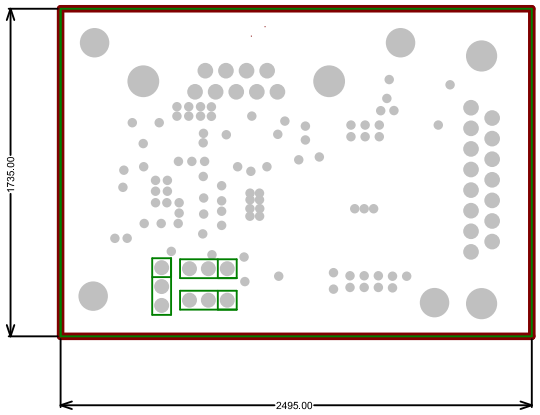

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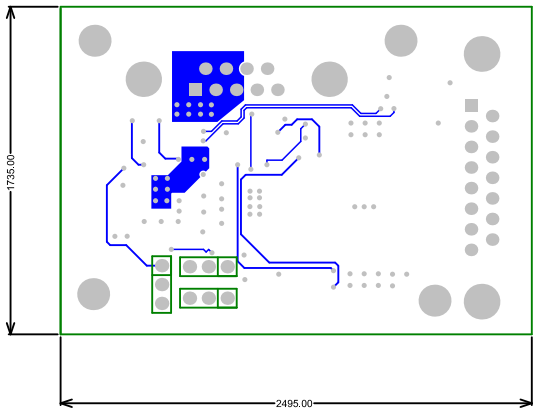

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