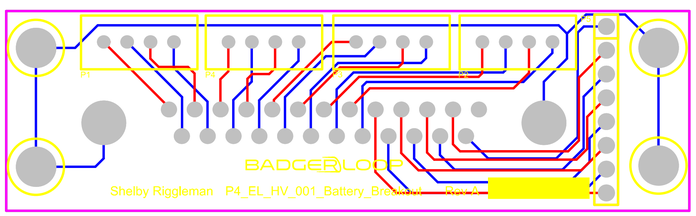
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
□	16	33.00mil (0.838mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c142h84
⊠	8	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c180h100
▽	25	42.91mil (1.090mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c169h109
✪	4	102.36mil (2.600mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c430h260
✡	2	128.35mil (3.260mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c476h326
	55 Total							

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

1. PCB must be 0.030" thick +/- 10%
2. Board Size:
3. Electrical Test
4. Coloring:
   a. Green Solder Mask Top
   b. Green Solder Mask Bottom
   c. White Silkscreen Top
   d. White Silkscreen Bottom
5. Via annular ring clearance is 10mil minimum
6. All holes are plated through holes



BADGER LOOP

Badgerloop
ERB Room 133
1400 Engineering Drive
Madison, WI 53706

ENGINEER: Shelby Riggleman	TITLE: hv_breakout.PcbDoc	
PCB DESIGNER: Shelby Riggleman		
DATE: 1/28/2019	PART NO.: P4_EL_HV_001_Battery_Breakout	REV: Rev A
FILE NAME: hv_breakout.PcbDoc	DWG NO:	SCALE: 1:1

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4	12.60mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
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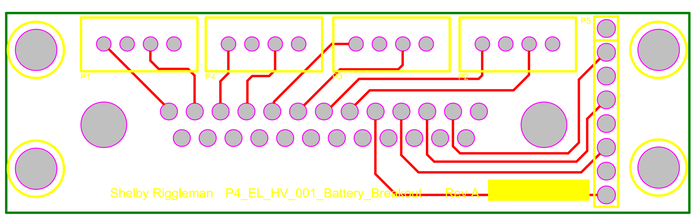

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
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4	Dielectric 1	FR-4	12.60mil	4.8	
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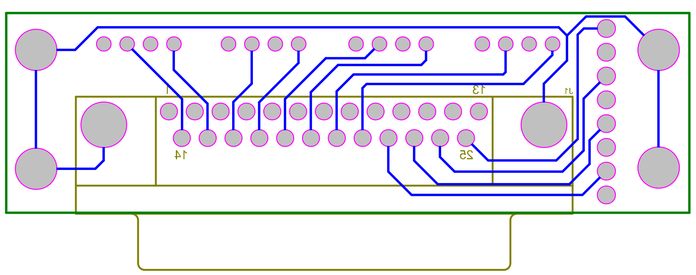

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