
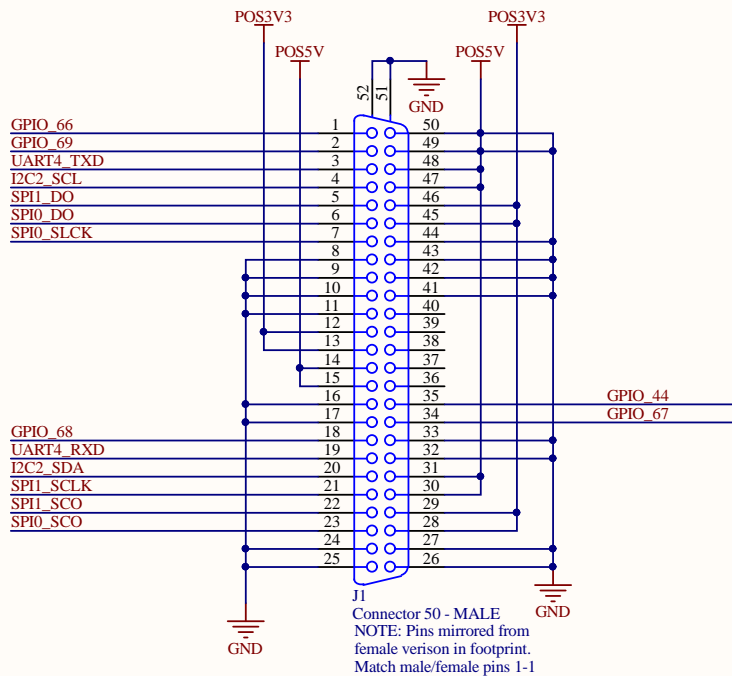
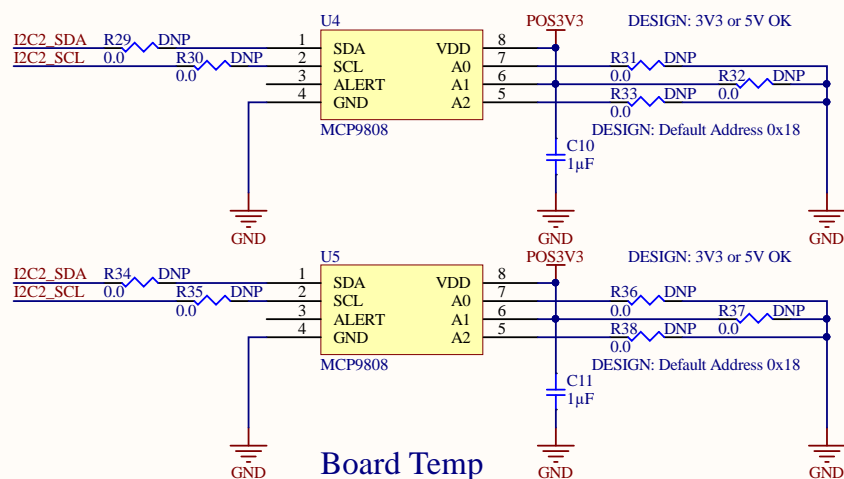


▲ Programmable Interrupt Source:
 DMP Interrupt/Wake On Motion Interrupt
 PLL RDY Interrupt
 I2C Master Input
 Raw Data Ready Interrupt
 FIFO Overflow Interrupt
 FIFO Watermark Interrupt

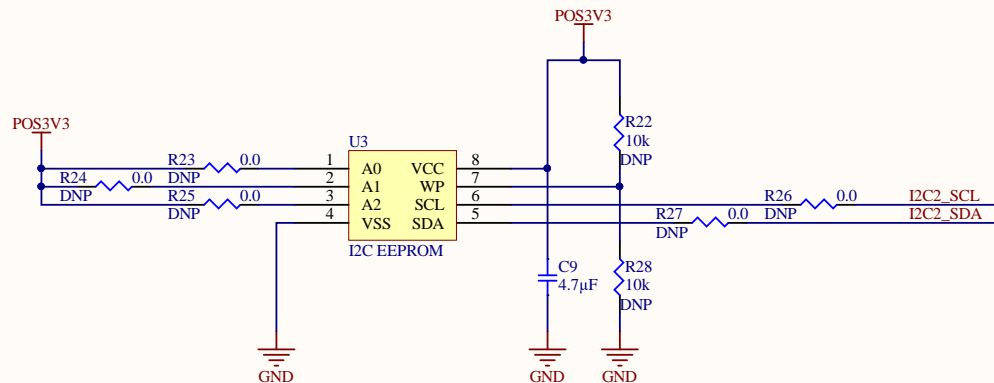
Title <i>nav_io.schdoc</i>			Badgerloop 133 Engineering Research Building Madison, WI 53715	
Size: A4	Number: 1	Revision: A		
Date: 11/15/2018	Time: 11:11:42 PM	Sheet 1 of 2		
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\lv_io_accel.SchDoc				



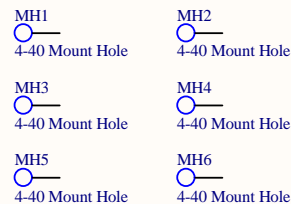
Main Connector




Board Temp




I2C EEPROM



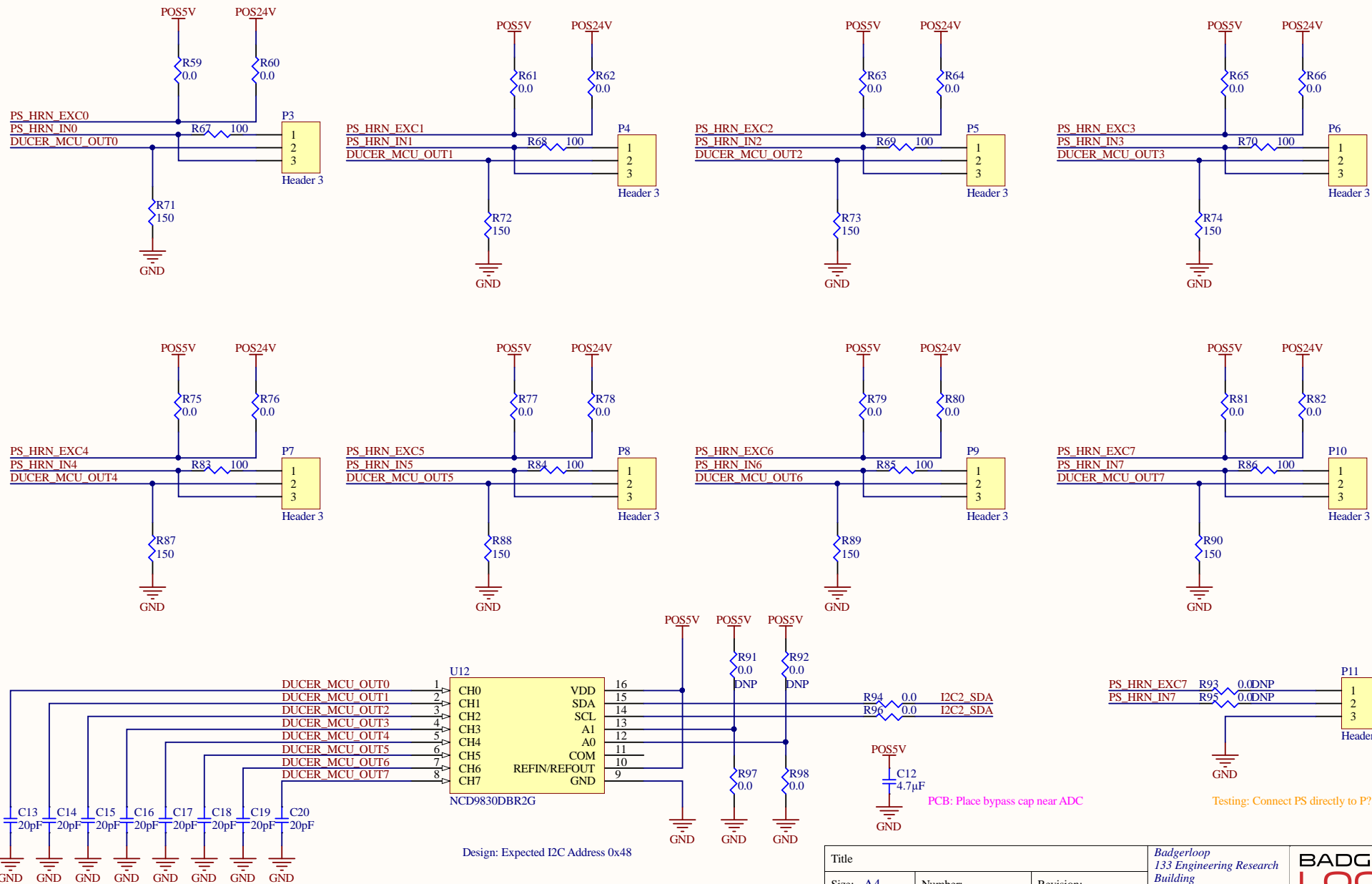
MECHANICAL

Title <i>nav_main_connector.schdoc</i>			Badgerloop 133 Engineering Research Building Madison, WI 53715	
Size: <i>A4</i>	Number: <i>1</i>	Revision: <i>A</i>		
Date: <i>11/15/2018</i>	Time: <i>11:11:42 PM</i>	Sheet <i>2</i> of <i>2</i>		
File: <i>C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\lv_io_main_connector.SchDoc</i>				

	1	2	3	4
A				
B				
C				
D				
	1	2	3	4

Title			Badgerloop 133 Engineering Research Building Madison, WI 53715	
Size: A4	Number:	Revision:		
Date: 11/15/2018	Time: 11:11:42 PM	Sheet of		
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\lv_io_harness.SchDoc				






PCB: Place debouncing caps near ADC

PCB: Place bypass cap near ADC

Testing: Connect PS directly to P?

Design: Expected I2C Address 0x48

Title			Badgerloop 133 Engineering Research Building Madison, WI 53715	
Size: A4	Number:	Revision:		
Date: 11/15/2018	Time: 11:11:42 PM	Sheet of		
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\lv_io_pressure.SchDoc				

