

VBUS --> 5V  
PWR

VBUS --> 3V3  
PWR

PCB: Place C?, C? Near U?


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Design: GND to RESET

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Design: Populate for  
External Compensation

Design: Pgood pulled to GND until  
Vout is within  $\pm 7.5\%$  V programmed

Title <b><i>power_PWR.SchDoc</i></b>			Badgerloop 133 Engineering Research Building Madison, WI 53715	
Size: <b>A4</b>	Number: 1	Revision: <b>A</b>		
Date: 9/30/2018	Time: 11:16:02 PM	Sheet 1 of 2		
File: C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PWR.schdoc				

VBUS --> 5V  
VBUS --> 3V3  
CONTROL

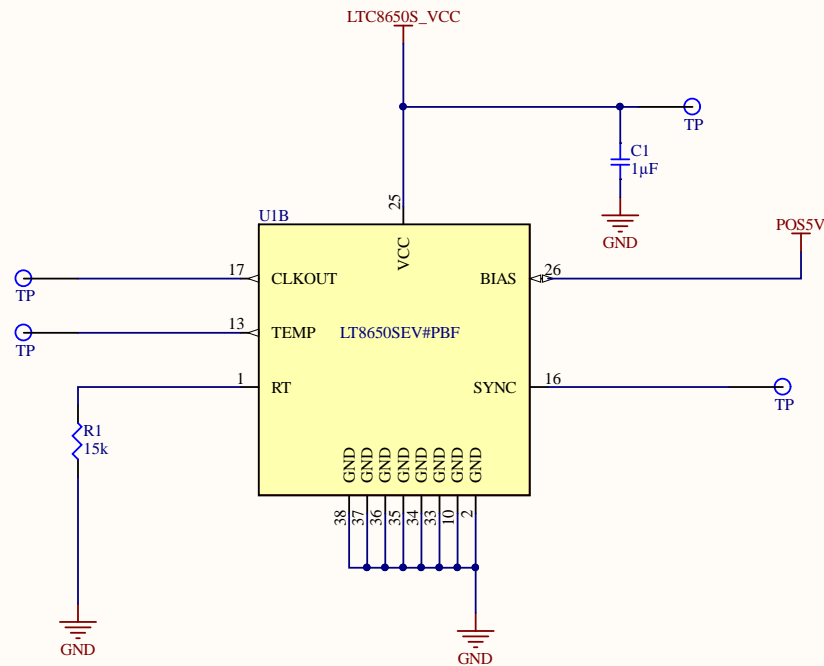
Design: Soft-Start Time TBD  
Design: Switching Frequency 2MHz  
Design: FCM W/O SSM OR SYNC

Design: LT8650S

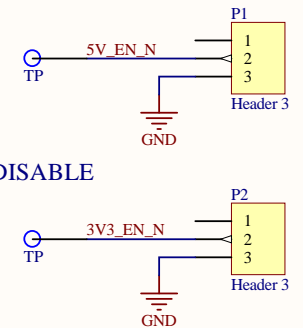
Vout1: 5V 4A


Vout2: 3.3V 4A

TODO: Should we do a 3 input OR Gate for PGoods?



Operation: Float \*\_EN\_N  
TO ENABLE, GND TO DISABLE



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1

2

3

4

A

A

MH1  
#10 Mount Hole

MH2  
#10 Mount Hole

MH3  
#10 Mount Hole

MH4  
#10 Mount Hole

B

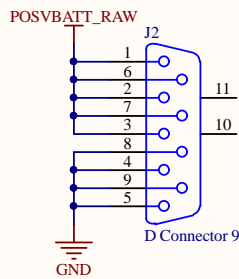
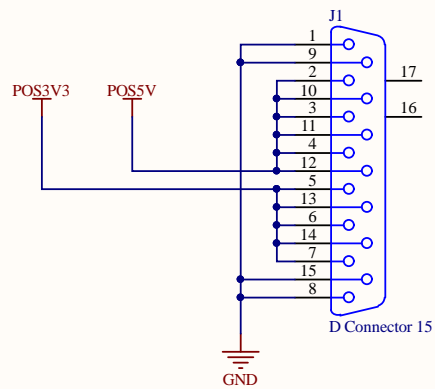
B


C

C

D

D



Title <i>nav_main_connector.schdoc</i>			Badgerloop 133 Engineering Research Building Madison, WI 53715	
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File: <i>C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_main_connector.SchDoc</i>				

1

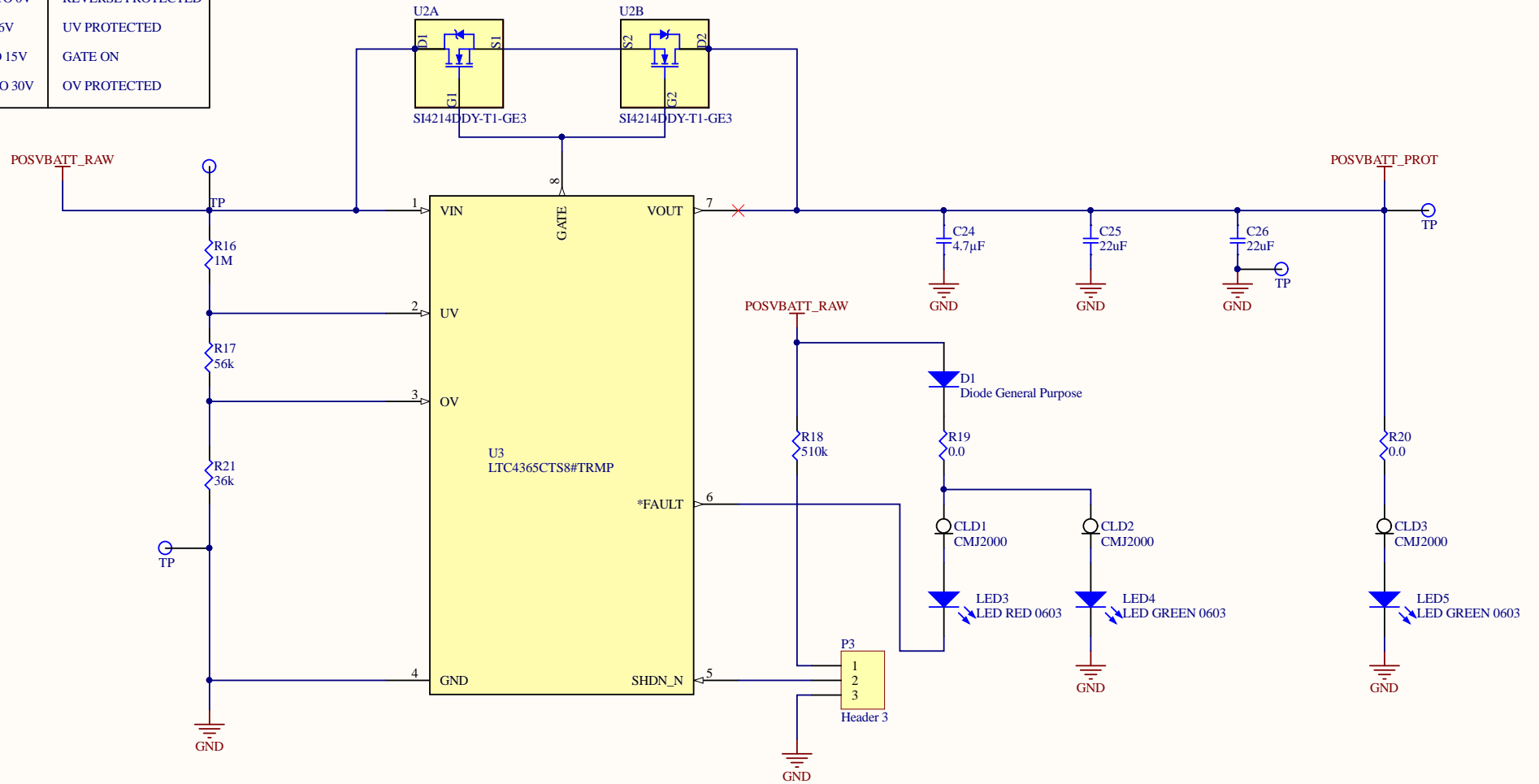
2

3

4

## DESIGN:

VIN	VOUT
-30 TO 0V	REVERSE PROTECTED
0 to 6V	UV PROTECTED
6 TO 15V	GATE ON
15 TO 30V	OV PROTECTED



Title <b><i>power_PROTECTION.SchDoc</i></b>			Badgerloop 133 Engineering Research Building Madison, WI 53715	BAD LC
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File: <b>C:\Users\Ryan Castle\Documents\git_repos\podiv-altium\src\prj\sch\power_PROTECTION.SchDoc</b>				

