**Badgerloop Schematic and PCB Design Review Checklist**

**Project:**

**RE:**

**Peer Reviewer 1:**

**Peer Reviewer 2:**

**Instructor Reviewer (Optional):**

**Industry Reviewer (Optional):**

**Link to Project:**

**Link to Schematic PDF:**

**Link to PCB Output:**

**Schematic Symbols**

|  |  |  |
| --- | --- | --- |
|  | Review | Comments |
|  | Does each component contain at the minimum:   * Manufacturer * Manufacturer P/N * Digkey Link: * Description * Default Designator * Datasheet Link |  |
|  | Verify pin map is correct |  |
|  | Does the symbol represent the actual circuit? For example, a wheatstone bridge package could be represented as discrete resistors in a rectangle for ease of understanding the circuit. Op-Amps too! |  |
|  | Does the symbol align to the grid? Do pins align to gird? |  |
|  | Are symbols located in their appropriate library or does the project use the “Temp” library |  |

**Schematic**

|  |  |  |
| --- | --- | --- |
|  | Review | Comments |
|  | Inputs on left side, outputs on right side (where possible) |  |
|  | Schematic information distributed across sheets (i.e. is it easy to read? Is everything jammed onto one sheet?) |  |
|  | Title blocked filled in? |  |
|  | Are all components on grids? Are all components even spaced, aligned horizontally, vertically, where possible? |  |
|  | Are nets named appropriately? |  |
|  | Are comments used to inform design, pcb, or operation notes? |  |
|  | Is the sheet size 11.0/8.5”? |  |
|  | Are component prefixes appropriate? (R for resistor, C for capacitor) Are they numbered sequentially? |  |
|  | Minimize Diversity: fewer unique parts in the design is preferable for less manufacturing errors, lower BOM cost, and ease of purchasing. |  |
|  | Compile project and ensure that no components are no unwaived DRC. Check that no DRC flags are appropriate |  |
|  | Is there an LTSpice simulation of the circuit? |  |
|  | Are unused pins accessible for future use or debug? |  |
|  | Add pull-ups and pull-downs for pins. DNP the unused component. |  |
|  | Does your circuit behave predictably during startup? |  |
|  | Does sequencing of power supplies matter? |  |
|  | Do capacitors have a path to GND after power-down? |  |
|  | Do all power nets follow the convention 5V, 3V3, LV\_Batt+, etc.? |  |
|  | Is the load at outputs within a safe range? |  |
|  | Are pull-up/pull down resistors sized appropriately? |  |
|  | Are power resistors sized appropriately? |  |
|  | Does your circuit include ESD protection? |  |
|  | Are address pins connected to (sometimes) DNP pull-up/pull-downs? Is there a comment for the expected address on the schematic |  |
|  | Do you have bypass capacitors on all ICs? |  |

**Design for Test**

|  |  |  |
| --- | --- | --- |
|  | Is there a test plan for the board? |  |
|  | Is there a bring-up plan for the board? |  |
|  | Have you contacted PCB and assembly houses during design? |  |
|  | Is Hipot testing required? |  |
|  | Are there GND and power supply test points available? |  |
|  | Are there test pads on critical signals? (Some places recommend 80% of nets to have a test point!) |  |
|  | Breakout NC pins to DNP components |  |
|  | Are all nets named? |  |
|  | Have you defined Net classes? Especially for boards with high and low voltage, high speed, etc. |  |
|  | What test equipment is required for this board? |  |

**Reliability**

|  |  |  |
| --- | --- | --- |
|  | Are transitor maximum rated voltage greater than Vnom / 0.80? |  |
|  | Are maximum rated voltage of capacitors (Vmax) greater than 200% of Vnom? |  |
|  | Is the power rating of resistors greater than Pnominal / 0.75? |  |

**PCB Layout**

|  |  |  |
| --- | --- | --- |
|  | Are board outline, dimensions defined in a BOARD OUTLINE Layer? |  |
|  | Do you have proper mounting holes? |  |
|  | Are mount hole locations agreed upon with mechanical systems? (lock mount hole or other mechanical interfaces) |  |
|  | Are all devices on the top-side? (Optional, but greatly preferred) |  |
|  | Are components aligned? Are diodes and polarized capacitors positioned with their cathodes/poles pointing in the same direction? |  |
|  | Make sure all jumpers, LEDs, connectors, switches, displays, etc. are okayed by mechanical, ok with the system |  |
|  | Is pin 1 of connectors marked? |  |
|  | Is there enough clearance around all components? |  |
|  | Is all silkscreen set to Arial? Refdes should be set to 40mil |  |
|  | Is the badgerloop logo, board name, revision and designer in silkscreen? Doesn’t have to be large |  |
|  | Does the board have or need fiducials or tooling holes? |  |

**Routing**

|  |  |  |
| --- | --- | --- |
|  | Are all traces rated for their expected current? |  |
|  | Avoid vias in pad where possible. |  |
|  | Follow keepout zones around screw heads |  |
|  | Keep 50mil from board edge. |  |
|  | Do your polygons have any “dead copper” or “bottlenecks”? |  |
|  | Do you have a GND plane, Power plane? |  |
|  | Are you using thermal reliefs? |  |
|  | Avoid routing directly between two adjacent SMD pads |  |
|  | Avoid <90 deg routing (Altium’s Acute Angle rule) to avoid acid traps |  |

**Other PCB**

|  |  |  |
| --- | --- | --- |
|  | Is the silkscreen useful? Silk should help you with bringup of the board or operation. Label connectors, configuration jumpers, LED meaning, etc. |  |
|  | Does silkscreen overlap with pads? |  |
|  | Are your through-holes plated? |  |
|  | Did you consolidate your drill sizes? |  |
|  | Did you check with your manufacturer about “Slots” (rectangular holes sometimes used by connectors, components) |  |
|  | Did you generate the proper output drawings, gerbers, and drill drawings? CAM files are good too! |  |
|  | Did you run DRC? |  |
|  | Export as a .STEP file and send to mechanical for integration. |  |

**Bill of Materials**

|  |  |  |
| --- | --- | --- |
|  | Are all your parts exported to the BOM? |  |
|  | Do you require any spare components? |  |
|  | Are there any components that are not on the BOM directly, but should be added (screws, standoffs, fuses, etc) |  |
|  | Do you have a link to all components (digikey) |  |
|  | Do another BOM consolidation Check |  |
|  | Are all components in stock? |  |