BADGERLOOP

Solar Car 1 MPPT Design

Starting Helpful links:

- Solar cell equivalent circuit: https://www.allaboutcircuits.com/technical-articles/circuit-designer-guide-to-photovoltaic-cells-solar-powered-devices/
- Boost converter MPPT simulation: https://www.youtube.com/watch?v=o9BOrAHH5E4
- Discussion on MPPT vs charge controlling: https://electronics.stackexchange.com/questions/519900/understanding-working-of-mppt-charger
- MPPT Charge Controller Reference Design for 12-V, 24-V and 48-V Solar Panels: https://www.ti.com/lit/ug/tiduej8a/tiduej8a.pdf?ts=1635705495282&ref_url=https%253A%252F%252Fwww.google.de%252F
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Preliminary Questions:

Buck or boost converter?

- Contingent on motor voltage: if > 100V or so, want boost, if less consider buck
    - The reason for this is we want to be able to use integrated buck converter IC's on the board for peripheral voltages (i.e. 12V, 3.3V) and these packages rarely are rated for VIN > 80V or so.

How does altering duty cycle of these converters move you along the solar IV curve?

- Buck:
    - Increasing duty cycle approaches short circuit (I increases)
    - Decreasing duty cycle approaches open circuit (I decreases)
- Boost:
    - Increasing duty cycle approaches short circuit (I increases)
    - Decreasing duty cycle approaches open circuit (I decreases)

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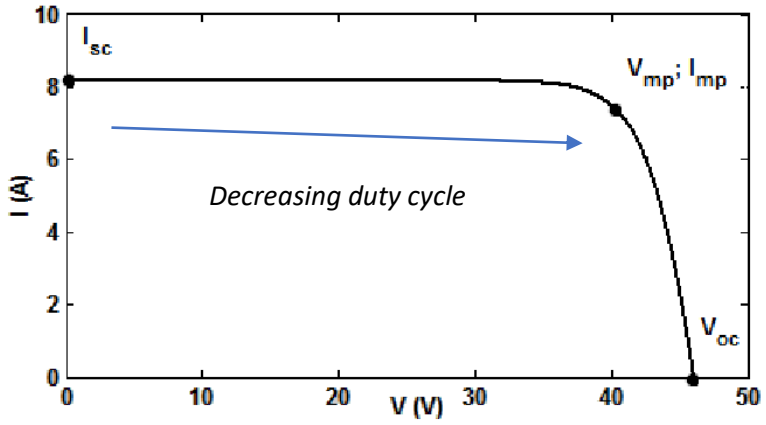
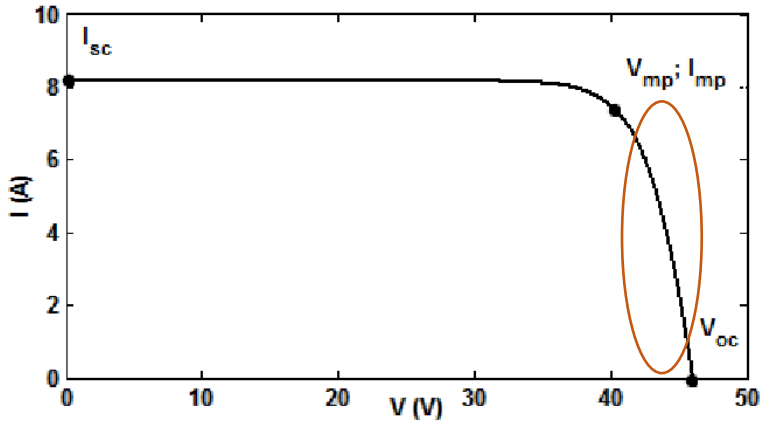


Pictured: Relationship between duty cycle and position on IV curve. Applies to both buck/boost.

Can MPPT buck/boost converter be the same as the charge controller or do we need two with a DC link (large capacitor between the two)?

- In order to ideally use one controller as both, three things must be true/designed for:
    1. Can accurately do pure current control (NOT MPPT) when battery is charging
        - Must be able to distinguish Iload from Icharge
        - Develop charge algorithm to take over MPPT when Iload < Iarray
            - Two scenarios:
                - Iarray – Iload < ideal charge current for current SOC
                    - Continue MPPT
                - Iarray – Iload > ideal charge current for current SOC
                    - Current control necessary
            - To get charging current to decrease, the converter will have to increase the impedance of the converter by altering duty cycle (-*decrease* on buck converter, *decrease* on boost converter) to utilize the decaying nature of current as voltage increases on the IV curve)
                - Must size pack to have max voltage to the voltage to where the minimum desired charging current lies on IV curve (or just max solar array voltage, as voltage is pretty constant at end of the IV curve).



Pictured: Increasing array voltage will decrease input current in a charging scenario.

2. MPP on the solar array side remains unaffected regardless of what the battery voltage is. If the solar array is automatically "brought down" to the battery voltage, MPPT will be moot and we will just have a charger. Due to the rectifying diode or FET with dead-time on a boost converter, the output of the converter should always be >= battery voltage, and the solar array voltage will not be dictated by the battery.
3. We design a **<u>hardware</u>** (NOT SOFTWARE) failsafe shutoff of converter if battery voltage is above certain threshold is implemented
    - Consider a comparator comparing battery voltage to reference voltage that turns off control FET
        - Needs to take into account battery voltage drop under load so battery doesn't charge when at full SOC, but voltage appears lower because discharging : VBat = VBatNominal – (Iout*PackInternalResistance).
        - Potentially set this cutoff threshold to not charge above VBat = VBatNominal – IMaxExpected*PackInternalResistance.

What happens if the maximum power point impedance/duty cycle yields a different output voltage than the battery voltage? If operating at maximum power point, is the output power fundamentally "capped" by the ideal voltage source that is the battery?

This is a question because typically with buck and boost converters with a voltage source Vin, Vout = Vin *(D) and Vout = Vin(1/(1-D)) respectively. (D = duty cycle). At first thought, one might think that if the MPP yields an output voltage at the inductor that is greater than the battery voltage, there is some loss in the difference between the inductor output and the battery when the inductor voltage is "brought down" after passing through the rectifying diode to the battery voltage.

$$V_O = V_{IN}\,D \qquad\qquad V_O = \frac{V_{IN}}{1 - D}$$

Pictured: Ideal buck and boost output voltage transfer functions with voltage src Vin

The answer to this question is best answered by reviewing the fundamentals of inductors. Inductors will do whatever it takes to keep the current flowing in it from changing – creating a voltage across the inductor as necessary to do so. Given this, the inductor will only output as high of a voltage as necessary to keep the current that was flowing in the inductor "charge" state into the battery. There is

no “excess voltage” that is being lost due to a duty cycle that would yield a higher voltage if a resistive load was connected.

Simulation:

In order to answer some of the above questions and get a better understanding of the operation of an MPPT boost converter, a characteristic simulation will be made of a solar array & converter that can be modified to fit desired array parameters.

Links referenced:

- https://www.youtube.com/watch?v=MZ-3HDjwPWw
- https://electronics.stackexchange.com/questions/257253/modeling-a-solar-panel-for-simulations
- http://www.intusoft.com/nlhtm/nl78.htm#The_Solar_Cell_SPICE_Model

Parameters for modeling custom solar array:

Voc = open circuit array voltage

Isc = short circuit array current

I0 = saturation current (of single cell). Hard to derive – informs open circuit voltage. Solar cell saturation current on the order of magnitude of 1e-10. Best derived from test data.

Derived parameters for modeling custom solar array:

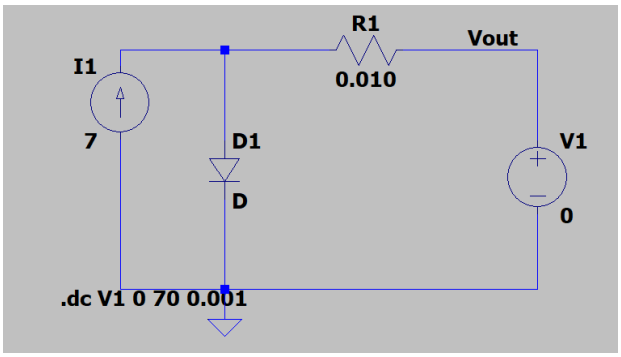
N = emission coefficient $$N = \frac{38.6 V_{OC}}{\ln(I_{SC}/I_0)}$$

XTI = exponent temperature coefficient $$XTI = 3N$$

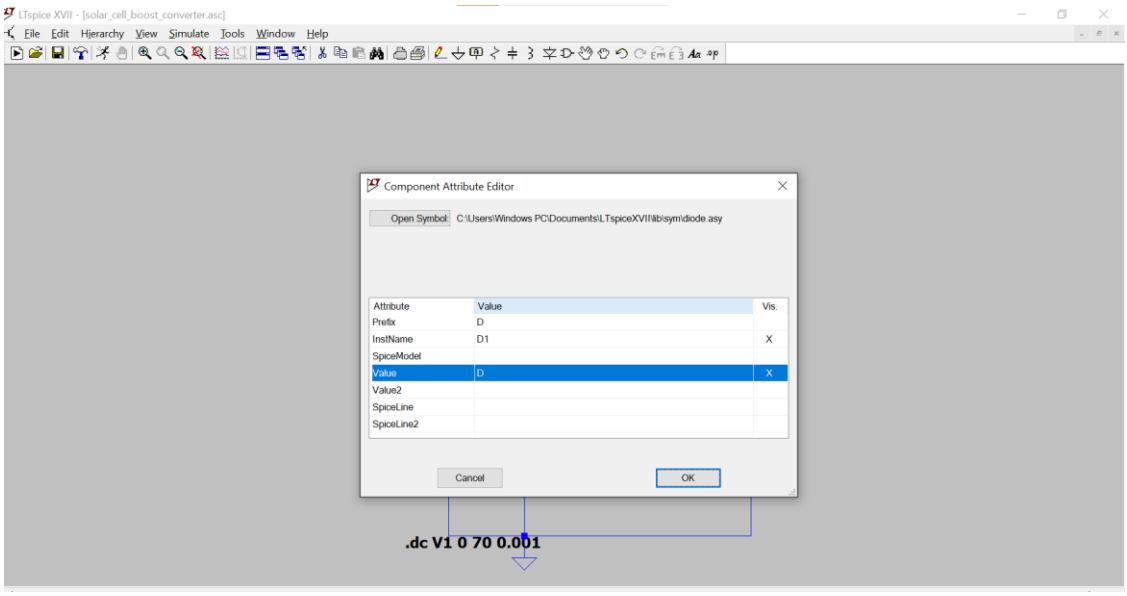
IS = saturation current $$IS = I_0$$

EG = energy gap $$EG = 1.11N$$

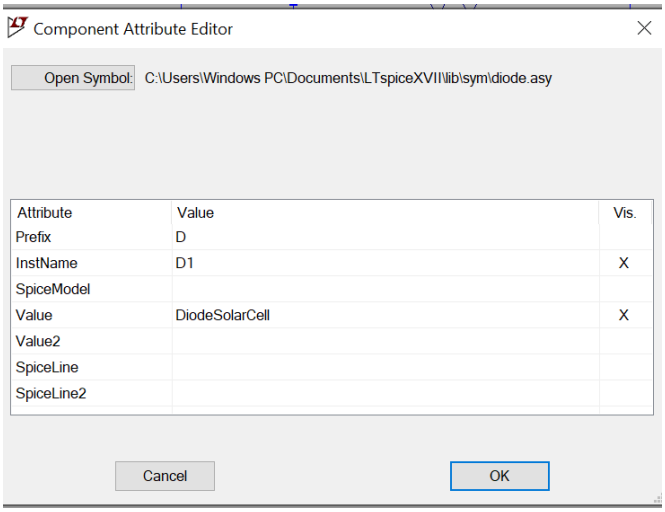
To put these in the equivalent circuit for a solar cell, add a generic diode in the proper location as D1 below:



CTRL + Right click on the diode to bring up this menu:



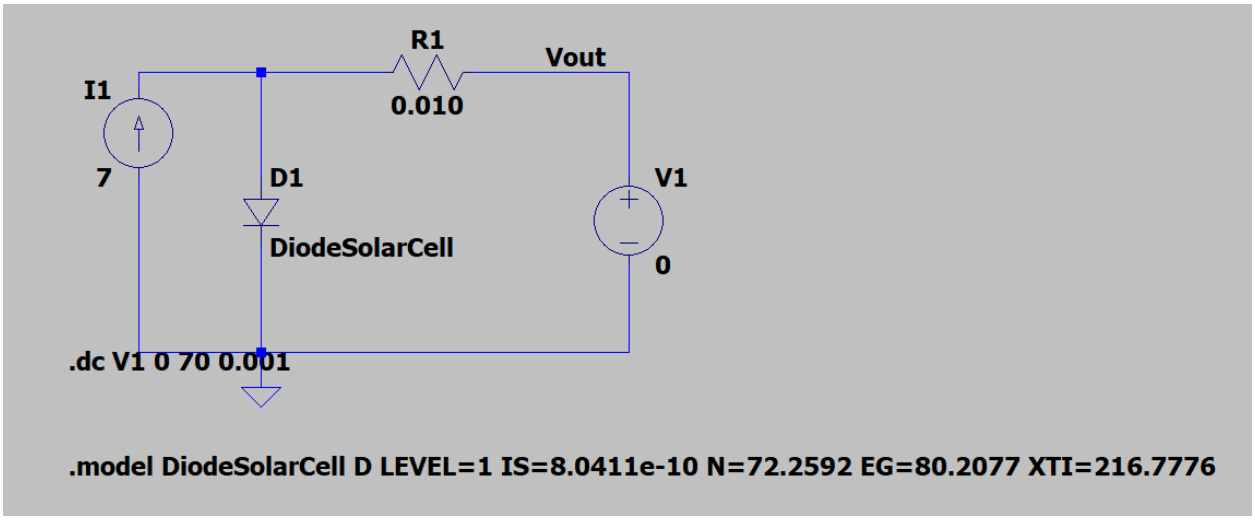
Change the “value” Parameter to the custom name you’d like to call the diode – “DiodeSolarCell here:



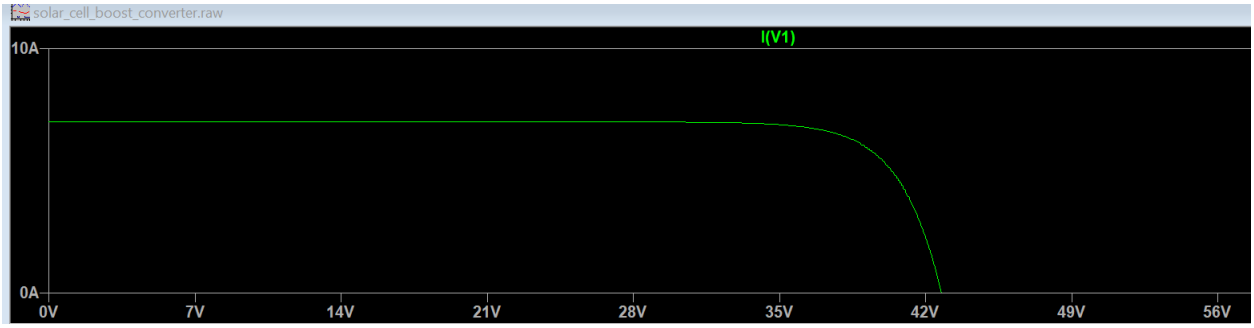
Add a spice directive with the following form to attribute calculated parameters to this diode:

.model <name_you_gave_diode> D LEVEL=1 IS=<calculated IS> N=<calculated_N> EG=<calculated_EG> XTI=calculated_XTI

Example:



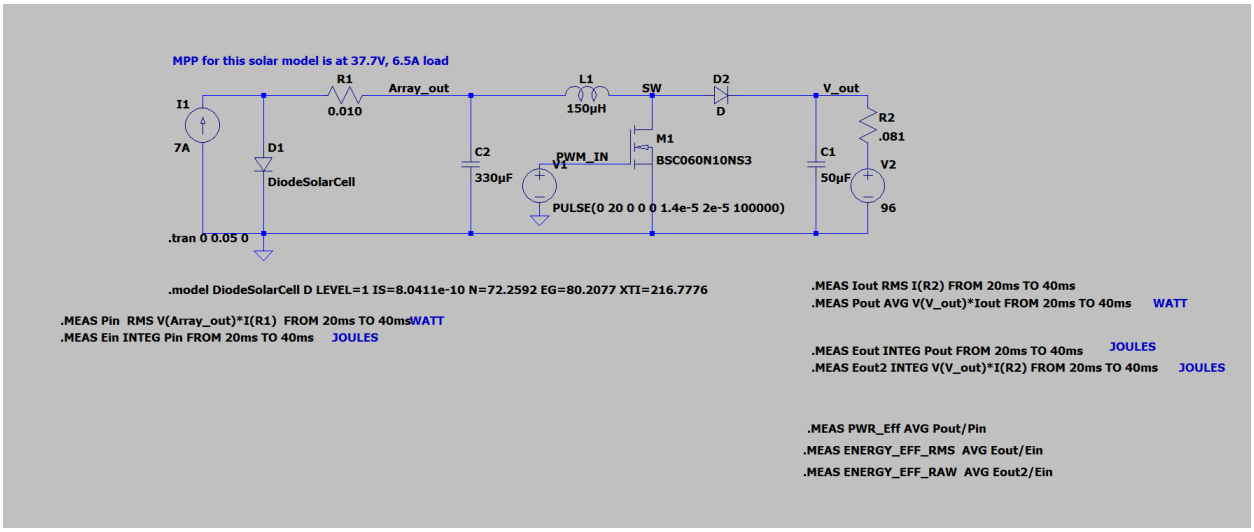
This should result in an I=V curve with the following shape when a dc sweep is ran on the model:



Boost converter simulation:

Hooking up the solar array model to a boost converter topology as shown below is helpful to understand the working principles and waveforms on various nodes of the MPPT. The actual “Maximum

Power-point Tracking” would be a function of the output current of this model (to the battery and load). The dependent variable is the duty cycle of the MOSFET gate drive signal, simulated by V1 here.



Solar array and battery specs

The solar array and battery specs are listed below. The solar array will have 3 individual strings that will be put in parallel to output to the battery pack. The decision for 3 individual strings was made to accommodate initial off the shelf MPPT solutions (found in next section), which have a maximum current rating of 7A, and allows for adequate marigin to boost from the solar array voltage to battery pack voltage (boost ratio > 1.1). In addition, multiple strings allow for individual maximum power-point tracking of each unique string in the event of varying iridescences between the strings (i.e. the back half of the car is in the shade).

- Pack nominal voltage: 96V
- Pack max voltage: 107V
- Number solar strings: 3
- Solar array string open circuit voltage: 57.12V
- Solar array string voltage: 48.72
- Solar array open circuit current per string: 6.34A
- Solar array mpp current per string: 6A
- Solar array mpp power = 876.96W

Solution Space

Elmar Race MPPT

This off the shelf option would allow for a quick, readymade solution for Solar Car 1. It is a boost converter with a minimum boost ratio of 1.1, max output voltage of 165V, and max output current of 7A. The peak conversion efficiency tops out at 99.6%. Perhaps more relevantly, At the maximum power point of our array (48.72V), the Elmar MPPT device shows an efficiency of 98.25%. Given the configuration of our solar array, we would need 1 Elmar MPPT per string, for a total of 3. At the cheapest unit cost of $2588.27, this would put the final BOM exceeding $8000, and proves prohibitively expensive among all of the other costs of building a solar car for the first time.

Custom In House Design

A custom design offers many advantages to an off the shelf solution with an additional assumption of risk. Foremost, a custom design can achieve a BOM of < $800, an order of magnitude more lucrative than the off the shelf solution. In addition to the immense learning opportunity it presents, it also provides more flexibility in the competition and bring-up environment. In the event of a malfunction of the device or user mistakes, a replacement part can be ordered for what is likely under $10, instead of bearing the lead time and cost of an entirely new off the shelf MPPT.

The risks include the additional time of design and testing, along with the novelty of power electronics to Badgerloop as an organization. There could easily be an oversight of a power electronics "gotcha" that requires the spinning of a board and delayed time until the solution is complete. With that being said, most of facets of building a solar car for the first time involve a degree of risk, and a custom MPPT approximates the degree of these risks.

Given the extremely constrained timeline that exists to build a first car within a year, building a converter that matches an off the shelf solution's performance (namely efficiency) exactly will not be the sole determinant of a successful design, while still being the primary directive of the design. With an in house design, improving upon it can be an iterative process and provide learning opportunities to teams of the future for years to come. In order to minimize identified risks, the custom design can approximate the known interface of the Elmar MPPT (12V, GND, CAN) to allow for a swap with an Elmar MPPT in the event the car's MPPT is the critical path in having a working car.

Path & Goals

With the advantages that a custom in-house design provides, and in the ambitious spirit of Badgerloop, an in-house design will be pursued with the following directives:

1) Consolidate these 3 MPPT devices into one sleeker, cheaper, simpler solution.
2) Achieve an efficiency of 97% or greater in design & ideal test conditions.
3) Learn about and implement fundamentals of power conversion and control in the context of a large embedded system.

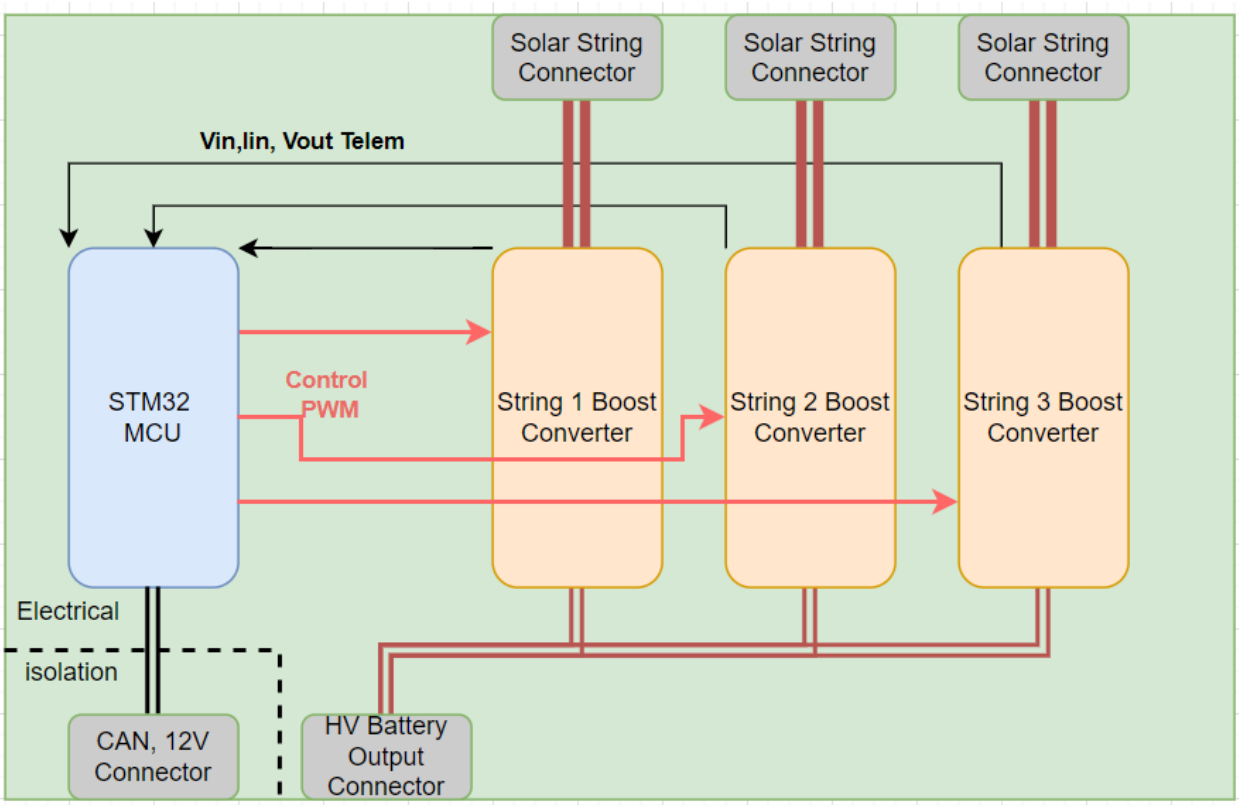
Custom MPPT Design

Helpful links:

- Multiphase (&single phase) boost converter design: https://www.ti.com/seclit/wp/slup323/slup323.pdf
- MOSFET Losses in Switching Power supplies: https://fscdn.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/power_loss_appli-e.pdf
- Boost converter design & power losses: https://www.powerelectronicsnews.com/the-dc-dc-boost-converter-part-2-power-supply-design-tutorial-section-5-2/
- System Design considerations for battery operated system: https://www.ti.com/download/trng/docs/seminar/Topic%206%20-%20DC-DC%20Power%20Conversion%20and%20System%20Design%20Considerations%20for%20Battery%20Operated%20System.pdf

Note: The TI single phase reference paper was heavily cited in development of this design. Additionally, the calculations performed for many of these design decisions were performed and saved in an excel sheet "Converter_calculations.xlsx" saved in the mppt/design directory that cite the source for the pertinent equation.

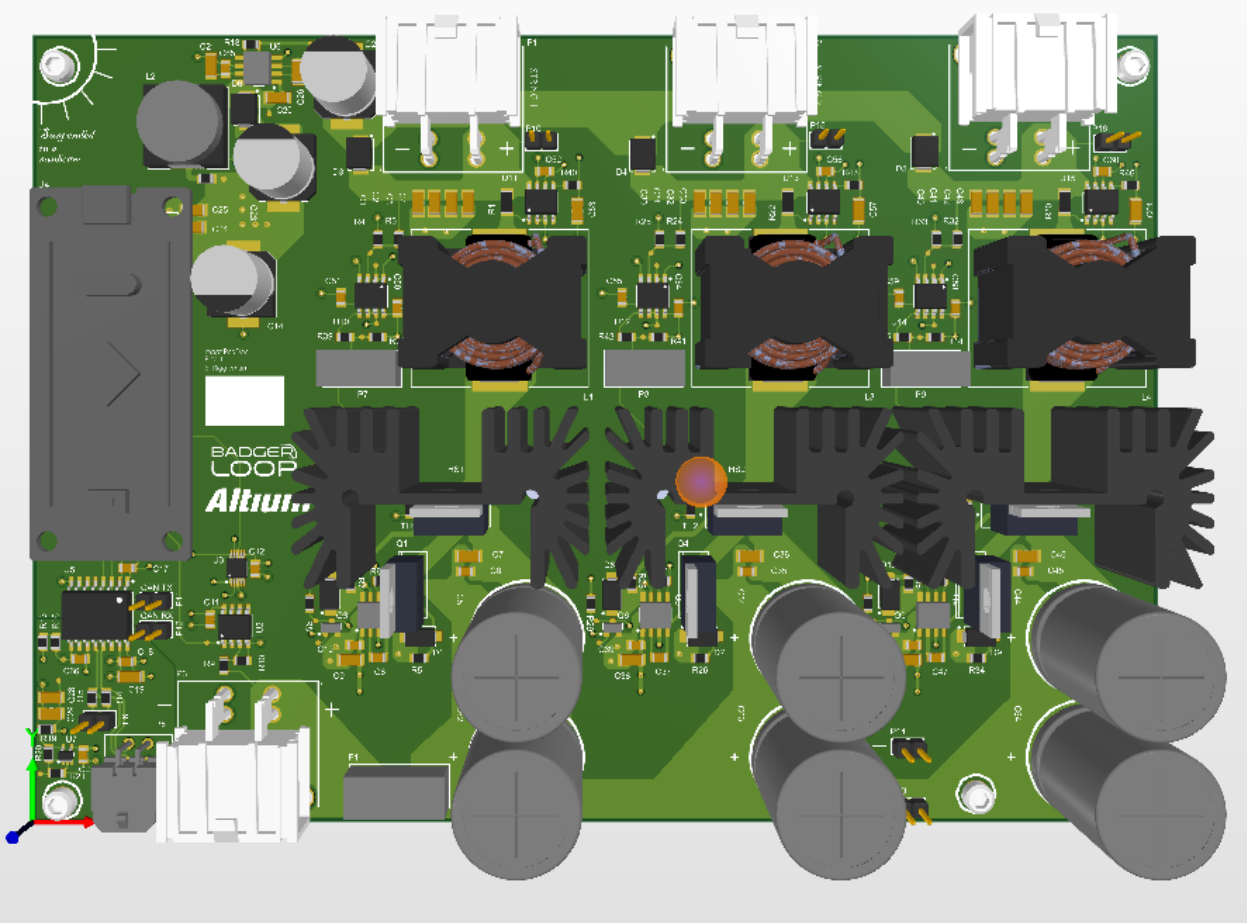
Design Outline:



MPPT Block Diagram

There are three boost converters, one for each solar string. Each converter is capable of operating at the highest solar string values, as well as their maximum power point, for the maximum output power of the solar array of 876W. Each converter is uniquely controlled to its maximum power point by a Nucleo STM32 microcontroller based on telemetry from solar string voltage, solar string current, and battery (output) voltage. The three converters are tied together at the output for the battery. The operating mode for output (battery charging vs MPPT), along with desired on-board telemetry is communicated via a galvanically isolated CAN interface that connects to the rest of the low voltage electrical system.

Final Design:



Final MPPT PCB layout

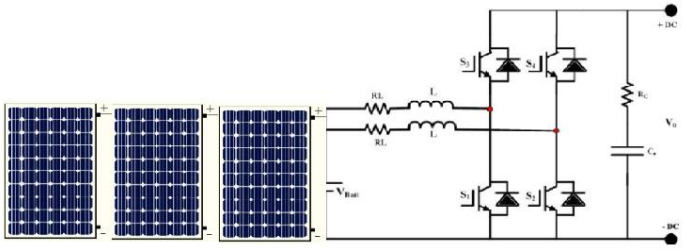
At the completion of this initial design, we are able to predict that the solution will be able to perform at 97.05% efficiency, while being 1/10 the cost of an off the shelf solution, while simultaneously having a smaller form factor (7” x 4.9”) than a necessary grouping of off the shelf solutions.

Boost converter design:

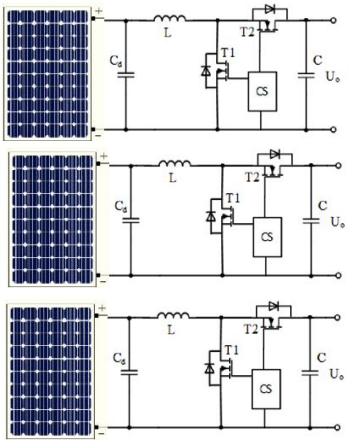
Consideration: Multiphase boost converter

Initially, a multiphase (2 phase) boost converter was considered as a solution for the main power converter. There are some advantages to this path, as per TI “When considering higher output currents, a multiphase boost converter provides many advantages over a single-phase option for higher power boost converters. Advantages are seen in efficiency, thermal performance and size”. With this option, the 3 strings would be fed into a singular dual phase converter, with one output to the battery. There would be 1 power point being “tracked”. After doing initial calculations on this solution, it proved more favorable to transition to a multi string single phase design. The primary reason was too high of switching losses at switching frequency needed to keep the inductor in CCM. Using higher inductance values could allow moving to a smaller frequency (which is what we do on new design) and decrease switching losses, but parts with necessary inductance values with a > 9A saturation current are few, and we want options in supply shortage. In addition, having unique MPPT's per string allows for most

efficient MPPT tracking and prevention of false MPPT peaks when combining multiple strings together if one is shaded.

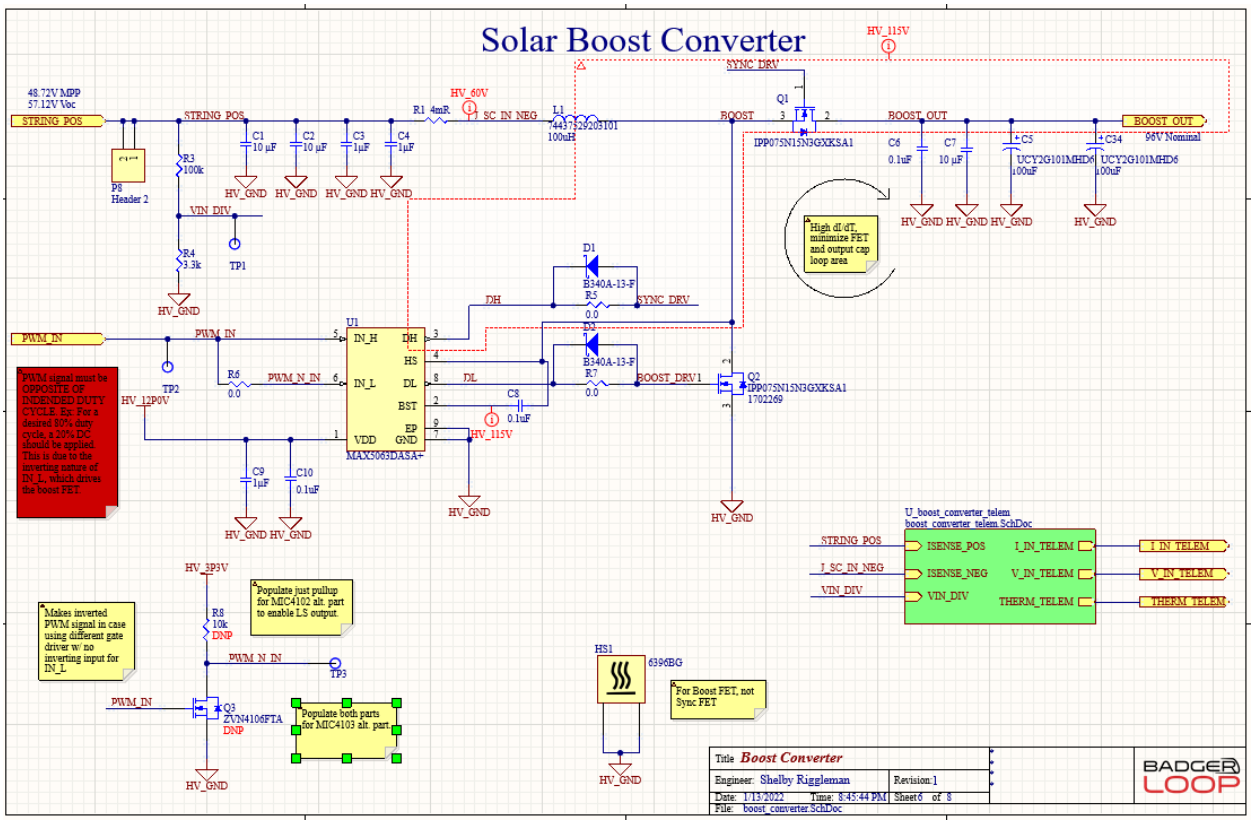


Multiphase configuration



Single phase, 3 string configuration

Single Phase Converter Design:



Instance of MPPT Boost Converter

Operating Frequency:

One of the key variables that dictates converter efficiency is the frequency that the transistors switch (switching frequency). The lower the frequency, the lower the transitional, QRR, QOSS, and inductor AC/Core losses are. Typical switching converter frequencies range from 100kHz to 2MHz. For this converter, a low frequency of 80kHz will be pursued. The consequence of operating at a lower frequency is that a larger inductor needs to be used, since more energy must be stored due to a longer off period where the inductor must be the source of current. This frequency is the same as the PWM signal applied to the gate driver. As frequency decreases, PWM resolution from the STM 32 increases as well. At 80kHz, the PWM signal should have 9 bit or .19% duty cycle step resolution.

PWM frequency versus PWM Resolution

STM32 16-bit timer	PWM resolution	PWM frequency
72 MHz	16 bit	~1.1 kHz
72 MHz	14 bit	~4.4 kHz
72 MHz	12 bit	~17.5 kHz
72 MHz	10 bit	~70 kHz
72 MHz	8 bit	~281 kHz
72 MHz	6 bit	~1.125 MHz
72 MHz	4 bit	~4.5 MHz

STM32 PWM resolution vs frequency

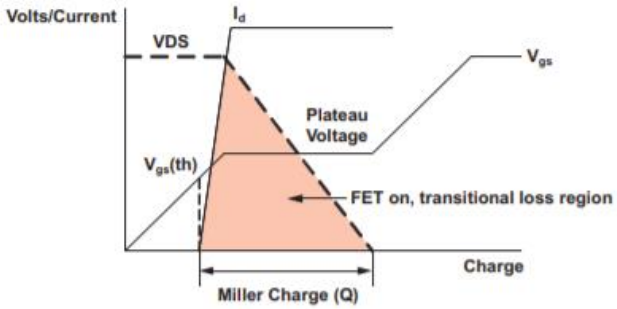
Inductor:

The inductor is chosen to keep it in continuous conduction mode at the operating frequency, while having a saturation current rating exceeding the expected average current. The inductor chosen was 74437529203101 by *Wurth-Elektronic* to satisfy these requirements. It is 100uH and has a 9.4A saturation current with a DCR of 22.9mOhm. This inductance value results in a 2.99A ripple current (50% of DC MPP of 6A).

74437529203101

FET:

The MOSFET is chosen by being within the voltage (100V) and current (7A) spec, along with having low RDSON and low switching charge. The former results in low DC rms losses, while low switching charge allows for quick transition times for minimal loss during the miller plateau.



Transitional region loss in MOSFET (Vth to end of miller plateau)

Additionally, low Qrr (reverse recovery charge) and Qoss (output charge) assist in having low switching losses. Per calculations in the TI boost converter document, QRR is the primary source of losses in this converter, totally 3.6W loss per string.

$$Q_{RR\_Loss} = Q_{RR} \times V_{out} \times n \times F_{SW}$$

QRR loss equation

A TO-220 package FET was chosen for this design due to ease of thermal dissipation (many heatsinks are available for this package), along with compatibility with many other FETs in the event the part is no longer available, whereas D2PAK packages are somewhat more customized.

The part chosen was IPP075N15N3 G, with a RDSON of 7.2mOhm, switching charge of 70nC, QOSS of 179nC, and a Qrr of 478nC.

IPP075N15N3 G

FET Driver:

The primary characteristic looked for in a FET driver was availability and max sink/source current. The max sink/source current is what drives the FETs on and off, so that they can have snappy on and off transitions for low switching losses. A driver with sink source of 2A or greater was pursued for this purpose. Another essential characteristic is that the driver must be able to drive the output voltage + Vgs on the high side FET. For our application this is 100V + 12V = 112V. The FET driver should have a HS voltage output rating in excess of this number.

The gate driver must also have dead-time built in, so that the two transistors are never on at the same time and a shoot through from the battery to ground occurs.

Additionally, a gate driver with an inverting input of the PWM signal is desired, as the two transistors need to be on opposite of one another, and because the PWM signal is the driving signal to drive the boost FET, there must be an inverted copy of it to turn the sync FET on or off in the opposite manner of the boost FET.

The MAX5063DASA+ was the primary part selected for the gate driver. It features built in dead time, an inverting PWM input, and a source/sink drive current of 2A, with a maximum HS gate drive of 125V.

To combat the part shortage, there are 3 alternative parts that share the same footprint as the original that can be substituted in the event that the MAX5063DASA+ is not available. The MAX15019BASA+ is a drop in replacement with a higher sink/source, but was unavailable during initial design. The MIC4102 is a replacement with an inverting input for the LS driver. However, an extra resistor must be populated (noted in schematic sheet) to enable the LS driver. The MIC4103YM is another replacement part with a compatible footprint, but an inverting FET and pullup resistor must be populated (also in the schematic sheet), as there is no internal inversion of the PWM signal.

IMPORTANT NOTE:

Because these gate drivers are used most frequently for buck converters, the high side FET is the "control" FET (i.e. the PWM signal drives the high side FET with a certain duty cycle and is directly related to the desired output voltage). With our boost converter, the low side FET is the control FET, and typical conceptions of how a duty cycle effects the output voltage is with respect to the boost FET. Because of this, the main PWM signal applied to the gate driver from firmware must be the *opposite* of what is intended to be. For example, if one wants an 80% duty cycle on the boost FET, the PWM signal must be 20%, so that when the signal is inverted to the low side driver, it is 80%, and the HS driver is at 20% duty cycle.

Thermal:

The hottest component on the board, and the one necessitating thermal management is the boost FET. The boost FET incurs full transitional losses, QRR losses, and QOSS losses. In our design, the boost FET will be dissipating 5.34W. With a junction-ambient thermal impedance of 62K/W, this would put the device over its 175C rating.

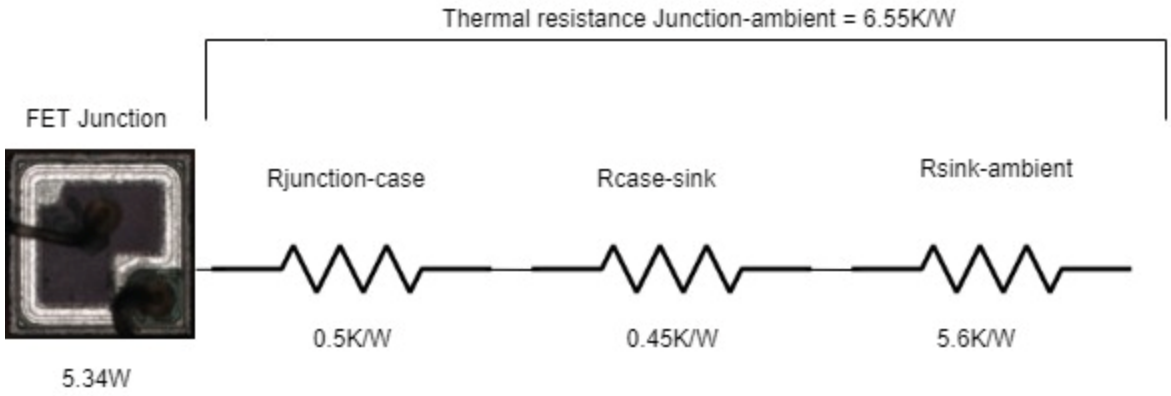
With a target max junction temperature of 125C and an expected maximum ambient temperature 45C, the permissible junction-ambient temperature difference is 80C. Hence, the largest possible thermal impedance that a heatsink can possess is 14.96 K/W. With a derating of 33% to account for the point-load nature of the transistor connection (heat is not evenly applied to the heatsink), we get a maximum thermal impedance from junction to ambient of 9.33 K/W.

With a thermal interface material (TIM) interface between the FET and heatsink, assuming a thermal conductivity of 0.79 W/MC, and an area of application of 0.000112 square meters, and a thickness of .04mm, the thermal resistance between the FET case and the heatsink is 0.45W/K.

In addition, the junction-case thermal impedance is 0.5K/W.

With a 9.33 -0.45 – 0.5 = 8.38K/W desired heatsink thermal impedance, the 6396BG was chosen. It has a natural convection (no airflow) thermal impedance of 5.6K/W.

This results in a maximum expected junction temperature of 89.9C.



Thermal impedances of boost FET with heatsink

6396BG Heatsink

Output Capacitor:

The output capacitor directly affects the voltage ripple on the output, and must also be rated for the full ripple current of the boost converter, as unlike a buck converter, the output sees the a full change from maximal current into the capacitor to full current output *from* the capacitor.

With each string converter having 200uF of capacitance on the output, the max voltage ripple will be 0.115V. There will be two 100uF electrolytic capacitors in parallel with a 1.75A RMS ripple current rating each to absorb and supply the bulk of the expected 2.84 Arms ripple current. In addition, .1uF and 10uF ceramic capacitors will be used to absorb and supply the fast edges of the current due to its lower inductance.

The UCY2G101MHD6 100uF capacitor was selected for the main output capacitor(s).

UCY2G101MHD6

Efficiency:

With the summation of inductor DCR losses, inductor AC/core losses, FET conduction, QOSS, Qrr, transitional losses, MCU losses, and driver losses, there are approximately 25.78 watts being lost as heat on this board. At maximum power-point of 876W, that equates to a 97.05% efficiency for the converter.

Open Questions:

There are a few open questions regarding the boost converter design as follows that are not design prohibitive, but would be good to seek answers to in continued development of this device

1) Why does boost FET incur QRR losses and not sync fet?
2) How does one assess stability of the closed loop system (gain/phase margin)?
3) What are the advantages and disadvantages of operating in continuous conduction mode vs discontinuous conduction mode?