Power Supply Design Seminar

Under the Hood of a Multiphase Synchronous Rectified Boost Converter

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2014 Texas Instruments Power Supply Design Seminar
SEM2100,
Topic 4
TI Literature Number: SLUP323

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Under the Hood of a Multiphase Synchronous Rectified Boost Converter

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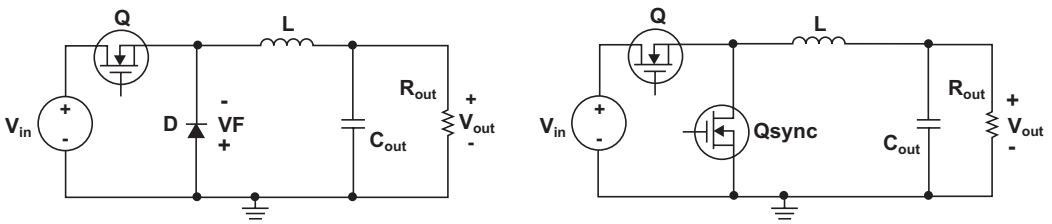
ABSTRACT

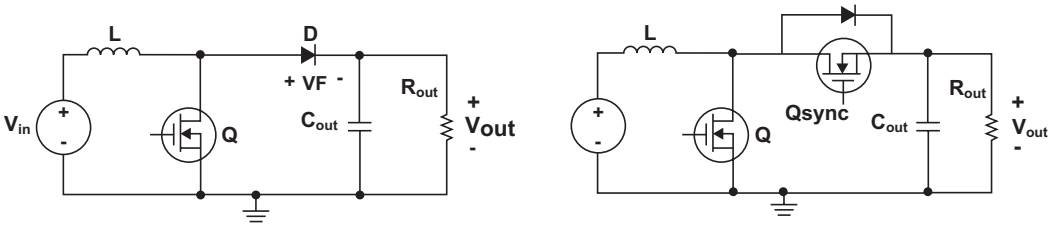
Recent application requirements show a trend toward higher power requirements for boost converters. These requirements often put great emphasis on cost, efficiency, size and dynamic response. With such emphasis on these performance requirements the need for using a multiphase synchronous boost converter arises. Selecting a number of phases can increase component counts and costs, which begs the question, how many phases are needed? What benefit do a given number of phases for a certain power requirement provide? This paper runs through a design example of a multiphase boost showing how interleaving affects cost, efficiency, size and performance.

I. INTRODUCTION

A synchronous boost converter provides a clear advantage in efficiency and thermal performance. The synchronous rectifying MOSFET provides the same advantages in a synchronous boost as it does in a synchronous buck. As in a synchronous buck, the low RDS_{on} of the synchronous MOSFET provides lower conduction losses when compared to a diode in the same application. This is because the RDS_{on} of the MOSFET is low and when multiplying with the square of the RMS current yields significantly lower losses than the average current of the same given waveform multiplied by the forward voltage drop of a particular diode. The commonality is shown below in Figure 1. Greater efficiency and lower temperature rise in the rectifying element is most significant when dealing with higher output currents and output voltages lower than 100 V. The synchronous boost provides these benefits when the output current is higher than approximately 3 A. But, what about output currents that are as high as 10 A or even 20 A? What options does a designer have to optimize the design according to the needs of a particular system? When considering higher output currents, a multiphase boost converter provides many advantages over a single-phase option for higher power boost converters. Advantages are seen in efficiency, thermal performance and size.



(A) Non synchronous buck to synchronous buck

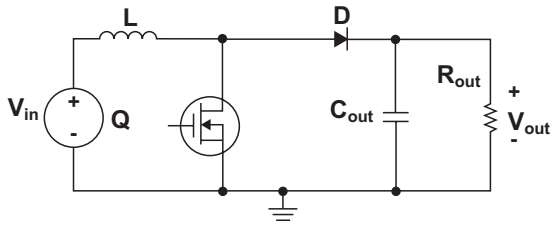


(B) Non synchronous boost to synchronous boost

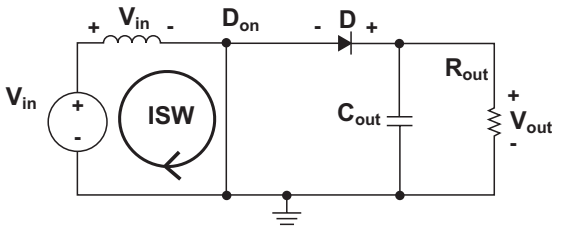
Figure 1 – Non synchronous to synchronous boost.

II. Basic Operation of the Boost Converter

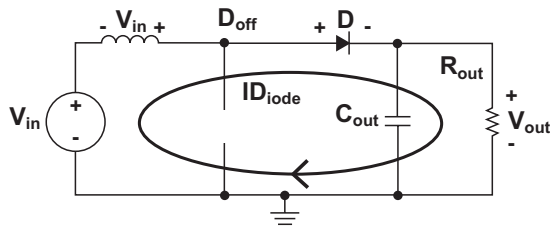
The boost converter temporarily stores energy in the inductor during the "on" period and then releases the stored energy into the output cap and load during the "off" period. The volt-second balance obtains the step-up functionality of the boost across the boost inductor. For example, for a 12 V input when the boost switch is on, the inductor has V_{in} across it. If the boost switch is on for a 50% duty cycle and off for a 50% duty cycle, then the voltage across the boost inductor during the off period (although now reversed in polarity) will be 12 V. This 12 V is superimposed on the V_{in} that is present. This voltage is rectified and stored in the output capacitor. Figure 2 (A, B and C) shows assigned voltage polarities for D_{on} and D_{off} periods that result in a complete cycle in a period of time determined by the switching frequency.



(A) Simple boost diagram



(B) Boost during D_{on} period



(C) Boost during D_{off} period

Figure 2 – Boost operation (non synchronous boost depicted).

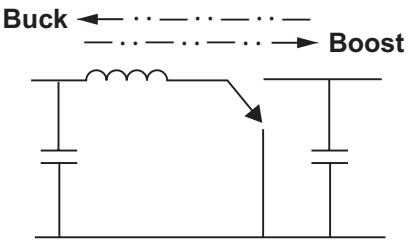


Figure 3 – Canonical schematic [1].

III. Drawing Comparisons Between Buck and Boost

Referring to Figure 3, this concept can be applied to what is known about a buck converter. For example, a boost requirement of 12 V_{in} and 24 V_{out} at 20 A translates to 480 W of power. Viewing this as a buck converter, 480 W of output power becomes 480 W of input power (assuming no losses). 480 W divided by 12 V_{in} yields the input current. The 12 V is considered the output voltage of a buck and the calculated input current is viewed at the output current of a buck. To give a more intuitive grasp, this boost requirement is a buck having 24 V_{in}, 12 V_{out} at 40 A. Attempting to do a 480 W output buck with 40 A of output current may not be the best approach. It is clear that interleaving would provide benefits to this application. Applying the "rules of thumb" common for buck converter designs as outlined above can provide a quick determination of the number of phases needed in a boost application. For example, 20 A to 30 A per phase for low voltage output in a buck translates to low V_{in} for boost, ~6 V and below, and 10 A to 20 A out for higher voltages. Ultimately one should go through calculations to see if the results fit what is needed for a particular design requirement, whether that is highest efficiency, lowest cost or smallest size. What method is applied for a multiphase boost to calculate this? What advantages does interleaving provide? These points will be highlighted later in this paper.

IV. Interleaved Boost Basic Operation

Continuing to look at the above application, now consider it in a two phase interleaved configuration.

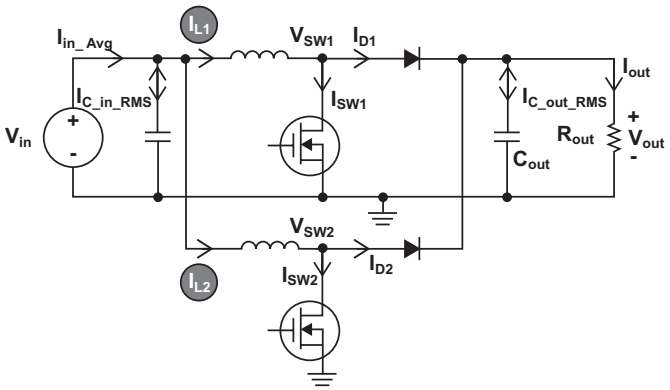
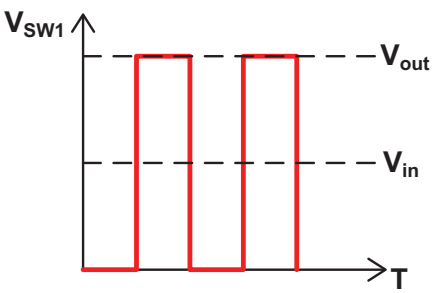


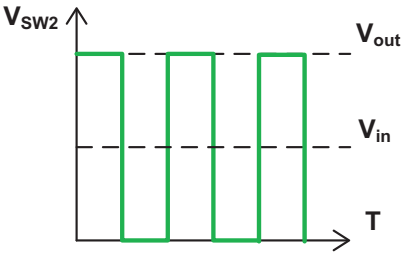
Figure 4 – A dual phase interleaved boost (non synchronous boost depicted).

Note that I_{in_Avg}, I_{out}, $I_{C\_in\_RMS}$ and $I_{C\_out\_RMS}$ are shared for the two interleaved stages, whereas the currents, I_{L1}, I_{L2}, I_{SW1}, I_{SW2}, I_{D1} and I_{D2} are divided by *n* phases, where *n* is the number of phases. In this case, *n* is 2 for two phases and, therefore, the currents are divided by 2. Also, it is very interesting to note that the effective switching frequency of each phase is divided down by *n* number of phases to obtain an identical switching frequency of a single phase approach. For example, when considering a 250 kHz switching frequency of a single phase boost, the switching frequency of each phase can drop to a lower frequency of 125 kHz to obtain an effective system switching frequency of 250 kHz.

V. Timing Diagrams for a Two Phase Interleaved Boost Running at 50% Duty Cycle



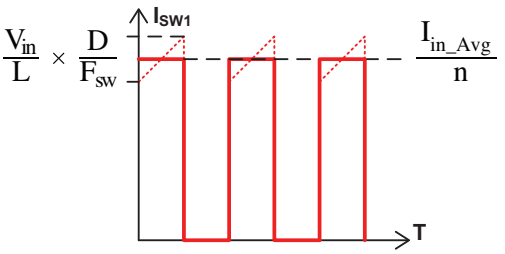
(A)



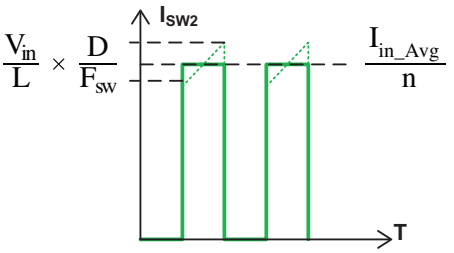
(B)

Figure 5 – Switch node voltage; phase 1 (A) and phase 2 (B).

Note the voltage stress that the boost FET is subjected to is equal to V_{out}. A margin of 10 V to 20 V should be added to V_{out} when selecting the correct VDS Rating of the MOSFET.



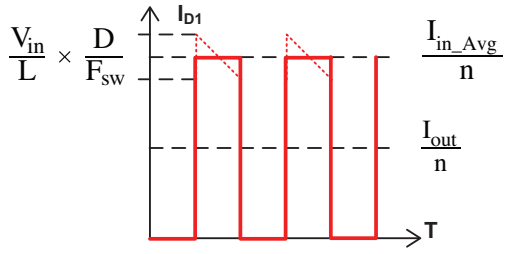
(A)



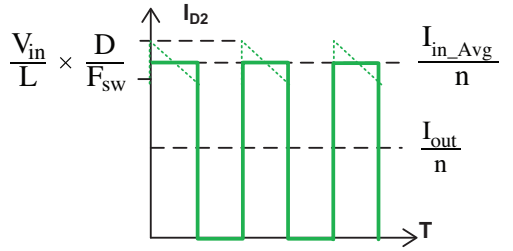
(B)

Figure 6 – Drain current in each FET; phase 1 (A) and phase 2 (B).

Note that the center point of the trapezoid is equal to the average input current divided by *n* number of phases.



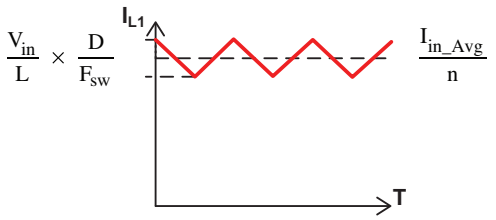
(A)



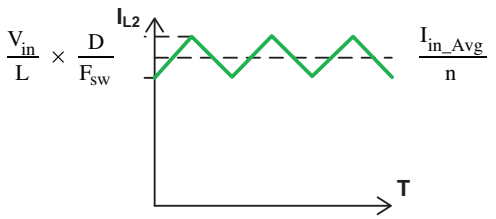
(B)

Figure 7 – Diode current; phase 1 (A) and phase 2 (B).

The center point of the trapezoid is equal to the average input current divided by n number of phases.



(A)



(B)

Figure 8 – Inductor current; phase 1 (A) and phase 2 (B).

The average current in each inductor is equal to the average input current divided by *n* number of phases.

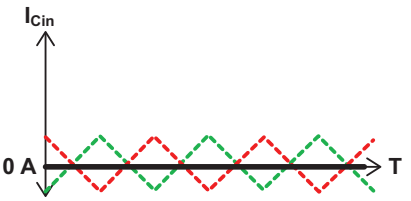


Figure 9 – C_{in} ripple current cancellation occurring at 50% duty for a dual phase boost.

The addition of the two waveforms cancels out the current to 0 A.

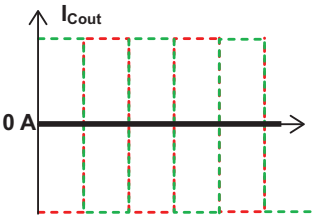


Figure 10 – C_{out} ripple current cancellation occurring at 50% duty for a dual phase boost.

In this particular example the addition of the two waveforms cancels out to 0 A.

VI. Design Examples – Single Phase Approach

Consider now how to calculate the losses in a single phase boost and a dual phase interleaved boost. For this example consider the following specification:

$$14\ V_{in};\ 24\ V_{out}\ @\ 8\ A\ out$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \qquad (1)$$

Equation 1 is the transfer function of a boost topology. Rearranging this equation for D results in:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \qquad (2)$$

So D=0.42 for this particular example. This is the nominal duty cycle for the design. P_{out} equals the output current multiplied by the output voltage, or 192 W for this example. Assuming an efficiency of 93% and

$$P_{in} = \frac{P_{out}}{\eta} \quad (3)$$

P_{in}=206 W. Now that the input power is known, calculating the input current is easy:

$$I_{in\_Avg} = \frac{P_{in}}{V_{in} \times n}$$
$$I_{in\_Avg} = \frac{206\ W}{14\ V \times 1} = 14.7\ A \quad (4)$$

A. Selecting an Inductor for Single Phase

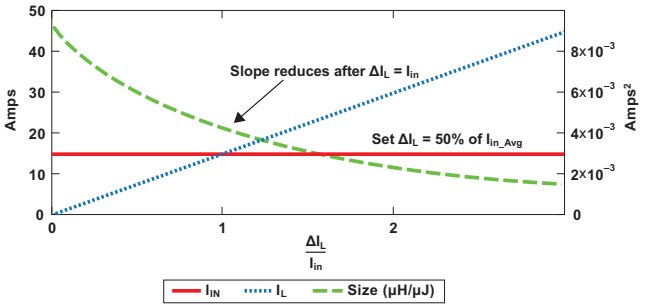


Figure 11 – Graph showing size factor as a function of ΔI_L.

Referring to Figure 11, the red curve is the average input current. The blue curve is the peak inductor current (I_L). The green curve represents the size of the inductor, i.e. µH per µJ (with units of Amps^2). Observing the green curve it is seen that the size of the inductor reduces as the x-axis increases – the peak-to-peak inductor current as a fraction of the average input current (I_{in}). As the ripple current increases by moving along the x-axis, the size of the inductor is reduced. For a small increase in the peak-to-peak inductor current, a steep reduction in the size of the inductor results. The amount of size reduction diminishes for a given increase in peak-to-peak ripple current between 50% and 100% of the average input current. With this understanding, the ripple current is set to 50% of the average input current. The design goal is to keep both the DCR losses and core losses to a minimum while selecting an inductor that is both cost effective and meets the size constraints of the system. The aim is to obtain a good distribution of core losses and DCR losses so that they are approximately equal, although this is not always the case depending on the inductor chosen.

If an input average current of 14.7 A is used, Equation 5 sets the peak-to-peak current in the inductor using the above approach.

$$L = \frac{V_{ind} \times D}{\Delta I_L \times F_{SW}} \quad (5)$$

where F_{sw} is the switching frequency, V_{ind} is V_{in}, and D is the duty.

Setting the peak-to-peak ripple current in the inductor to ~7.5 A yields an inductance of 3 µH. Now the peak current in the inductor is calculated. The saturation current of the inductor needs to be above the calculated peak current level to avoid saturating the inductor.

$$I_{L\_peak} = \frac{\Delta I_L}{2} + I_{in\_Avg} \quad (6)$$

This yields a peak current of 18.5 A. Therefore the saturating current of the inductor selected needs to be greater than this value.

B. Loss Calculations in a Boost

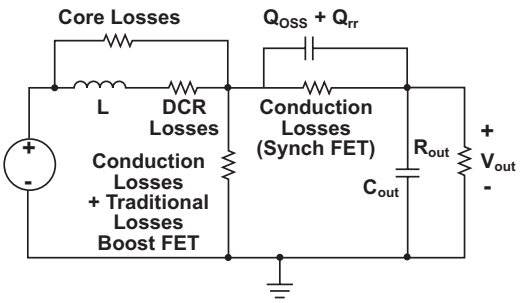


Figure 12 – Synchronous boost losses that will be considered.

i. DCR Losses in Inductor

To calculate the losses in the inductor, the RMS current in the inductor needs to be determined. The inductor current is a triangular waveform. To calculate the RMS current of a triangular waveform use Equation 7:

$$I_{L\_RMS} = \sqrt{I_{in\_Avg}^2 + \frac{\Delta I_L}{\sqrt{12}}^2} \quad (7)$$

This yields an RMS inductor current of 14.9 A RMS.

For this particular example, the XAL1580-302 from Coilcraft was selected. The XAL1580-302 is a 3 µH inductor with a DCR of 3 mΩ max and an I_{SAT} of 43 A for a 30% drop in inductance. It is worth noting that this is a 13.2 mm x 14.1 mm x 7.5 mm inductor. Using Equation 8 with a DCR of 3 mΩ yields a conduction loss of 0.6 W:

$$DCR_{loss} = I_{L\_RMS}^{2} \times DCR \quad (8)$$

If high side current sensing and a current sense resistor are used, the loss calculation is approached in the same manner as described above.

ii. Core Losses

Calculating core losses is less straightforward and requires material information from the supplier. This data is often missing from the datasheets. However, some datasheets will provide a formula that is used to calculate core losses. This typically has the form of Equation 9 below:

$$Coreloss = K_1 \times f^x \times B^y \times V_E \quad (9)$$

Where:

K1 is a constant of the core material

F is the switching frequency in kHz

B is the flux density in kGuass

x is the frequency exponent (given for a specific core material)

y is the flux exponent (given for a specific core material)

$\mathbf{V_E}$ is the effective core volume in cm^3

Equation 9 is insightful and shows that the core loss is dependent on frequency, flux density and core volume in addition to the core material used. In the absence of a core loss equation some suppliers publish a graph used to determine core losses. For this example, Coilcraft's online calculator tool was used. Inputting the LRMS current of 15 A and a peak-to-peak inductor ripple current of 7.5 A into an online calculator tool yields a total loss for the core of 2.6 W. Combining this core loss of 2.6 W with the conduction loss of 0.6 W yields a total loss for the inductor of 3.2 W. This is far too much loss for this size core and, in a practical sense, a larger core that yields less flux density needs to be selected. But for demonstration purposes, this core is used and compared to the two phase approach.

iii. FET Selection

The VDS voltage rating of a potential FET needs to be greater than V_{out} when making a FET selection. When deciding what FET to use for a switching power supply, a designer needs to ensure that the losses incurred in the FET do not exceed the component's maximum rated temperature in a given ambient temperature.

There are two types of losses in particular that contribute significantly to the losses in FETs – conduction losses and transitional losses. The RDS_{on} affects conduction losses while transitional losses are affected by the charge between the FET's gate to source, gate to drain and drain to source.

a. Conduction Losses

Conduction losses are calculated by obtaining the RMS currents in the FETs. Although the ripple currents generated by the boost inductor affect the RMS currents, as an approximation and for simplicity, these currents are ignored. It is sufficient to say that if the ripple current is selected as suggested above, the amount of error the approximation introduces is not significant.

The RMS switch current in the boost FET simply approximates to:

$$I_{FET\_RMS} = \sqrt{D} \times I_{in\_Avg} \quad (10)$$

This yields an RMS current of 8.8 A.

For this example, the Texas Instruments CSD18531 FET was selected. This has an RDSon of 3.5 mΩ for a 10 V Gate drive. The RDSon typically increases with temperature as with all resistances. This example assumes a hot RDSon of 4 mΩ. Applying Equation 11 approximates the conduction losses to be 0.3 W.

$$FET_{Cond} = I_{FET\_RMS}^{2} \times RDS_{on} \quad (11)$$

b. Transitional Losses

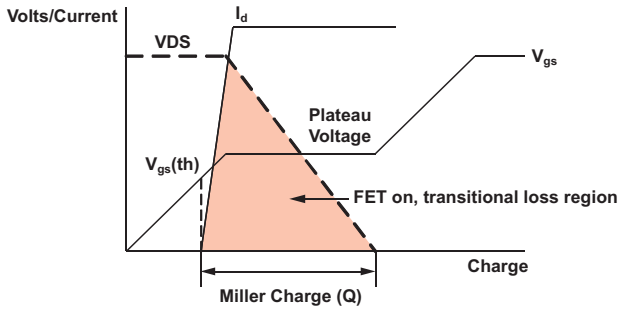


Figure 13 – Transitional losses occurring during the switching on period of the MOSFET.

Transitional losses are dependent on the gate drive strength of the controller as well as the V_{GS} threshold of the MOSFET and the gate charge. This example assumes an average switch on, switch off time of 10 ns, which is considered to be relatively fast.

For estimating the transitional losses Equation 12 is applied:

$$SW_{TRANS\_Loss} = V_{out} \times I_{in\_Avg} \times T_{SLEW} \times F_{SW} \quad (12)$$

This yields transitional losses of ~0.8 W. Adding both conduction losses (0.3 W) and transitional losses (~0.8 W) in the boost FET yields a total power loss of ~1.1 W.

Typically losses much greater than 1 W require heat sinking or require a parallel boost FET to lower the temperature rise as a result of excessive losses. Using parallel FETs, in effect, halves the RDS_{on} and also distributes the heat being generated by the losses. In addition, the FET count now equals that of a dual phase approach without the extra gate drive stage needed for two phases. Using a parallel FET/single gate drive approach is not as advantageous as using a dual phase approach. Doubling the gate charge for a single gate drive stage significantly impacts the slew time (T_{SLEW}) for the two FETs approach and therefore impacts transitional losses, when compared to a dual phase approach [2]

iv. SyncFET Losses

Similar to a synchronous FET in a buck converter, this switch is subject to the benefit of Zero Voltage Switching (ZVS) due to the conduction of the body diode during the dead time and before turning the FET either on or off. This FET has the benefit of only incurring conduction losses. The approximation of RMS current in the sync FET is calculated as follows in Equation 13:

$$I_{FET\_RMS} = \sqrt{1 - D} \times I_{in\_Avg} \quad (13)$$

Using Equation 13 yields an RMS current of 11.2 A. The conduction losses in the synchronous rectifier are 0.44 W, calculated using:

$$FETCond = I_{(FET\_RMS)}^{2} \times RDS_{on} \quad (14)$$

v. Q_{OSS} Losses

Although there are no transitional losses in the boost FET, as previously stated one incurs additional switching losses. Both the boost and sync FET realize switching losses due to the output capacitance. The output capacitance, Q_{OSS}, for the suggested FET is 32 nC. The switching loss in each FET due to Q_{OSS} is

$$Q_{OSSLoss} = \frac{Q_{OSS}}{2} \times V_{out} \times F_{SW} \times n \quad (15)$$

Equation 15 yields a total of 0.2 W of loss for both FETs. If parallel sync FETs are required in certain applications, this clearly puts further stresses on the boost FET. In this case, the single phase approach has additional losses due the increase in Q_{OSS}.

vi. Q_{RR} Losses

When the sync FET turns off during the dead time but before the boost FET turns on, the body diode of the synchronous FET is biased-on. In effect, charge is stored in the PN junction of the body diode. When the boost FET turns on, this stored charge, called the reverse recovery charge (Q_{RR}), is removed before the body diode is reverse biased. These losses are incurred in the boost FET.

For the suggested FET, the Q_{RR} is 100 nC and the Q_{RR} losses incurred in the boost FET due to this Q_{RR} is given by Equation 16.

$$Q_{RR\_Loss} = Q_{RR} \times V_{out} \times n \times F_{SW} \quad (16)$$

This yields Q_{RR} losses of 0.6 W. The total losses in the boost FET therefore are 1.35 W.

vii. IC Losses

Typically a controller has gate drive circuitry to drive the FET gates off and on. The power required to do this is not part of the output power and is considered a loss. The losses the IC will incur due to this gate drive circuitry are shown in Equation 17.

$$I_{C\_Loss} = V_{in} \times n \times \left\{\left(Q_{Gtot} \times F_{SW}\right) + I_Q\right\} \quad (17)$$

Q_{Gtot} in Equation 17 is the total Q_G of all FETs and I_Q is the quiescent current of the controller. The Q_{Gtot} for all FETs selected is 72 nC. The I_Q for the LM5122 is ~4 mA. Therefore the total IC losses for a single phase controller are 0.182 W.

C. CIN_RMS Ripple Currents

For a single phase boost, the RMS ripple current of the input capacitor needs to be able to supply the AC content of the inductor current and it is simply calculated as follows:

$$I_{C\_in\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (18)$$

This results in an RMS ripple current rating requirement for the input capacitor to handle at least 2.1 A. To meet this requirement a 22 µF ceramic input capacitor is selected.

It is worth noting that a low impedance ceramic may cause the input to oscillate. If an input filter is used or if the cables to the power supply are long (therefore increasing parasitic inductance), care must be taken to dampen the input due to these factors. This is usually done by placing an electrolytic capacitor at the input to dampen any oscillations. The selected electrolytic needs to have a capacitance much greater than the ceramics and also its ESR must be relatively high to ensure adequate dampening.

D. Cout RMS Ripple Current Rating

The RMS ripple current in the output capacitor is much higher than the input due to the fact that the output current in a boost is discontinuous. During the D period the diode is reverse biased and the output capacitor delivers the load current.

The RMS ripple current rating for the output capacitor is approximated (ripple currents ignored) as:

$$I_{C\_out\_RMS} \approx I_{out} \times \sqrt{\frac{D}{(1-D)}} \quad (19)$$

This yields a ripple current rating of 6.71 A for C_{OUT}.

Two PCV1E391MCL2GS (aluminum organic polymer) were selected for this example. These are 25 V rated 390 µF capacitors with an RMS ripple current rating of 4.2 A for each capacitor and an ESR of 21 mΩ. The output capacitor also dictates the ripple voltage as well as the compensation to obtain stable loop operation.

For a given ripple voltage requirement of less than 1%, which is less than 240 mV, the needed capacitance is calculated as follows in Equation 20:

$$V_{out\_Ripple} = \sqrt{V_{C\_out\_Ripple}^{\ 2} + V_{C\_out\_Ripple\_ESR}^{\ 2}} \quad (20)$$

The output ripple is made of two components. The first ripple component is because of the charge and discharge currents of the output capacitor. The second ripple component is because of the charge currents creating a voltage drop across the output capacitor's ESR.

The total output ripple voltage is calculated using the following equations:

$$V_{C\_out\_Ripple} = \frac{\Delta I_{C\_out} \times D}{F_{SW} \times C_{out}} \quad (21)$$

$$I_{Cout} \approx \frac{I_{out}}{n \times (1-D)} \quad (22)$$

n = Phases

$$V_{C\_out\_Ripple\_ESR} = I_{C\_out} \times C_{out\_ESR} \quad (23)$$

$$V_{out\_Ripple} = \sqrt{V_{(C\_out\_Ripple)}^{2} + V_{(C\_out\_Ripple\_ESR)}^{2}} \quad (24)$$

For this paper's example, the total output ripple voltage is ≈147 mV.

E. Loop Stability Analyses

A simplified control to output transfer function for a current mode boost power and modulator stage is given below in Equation 25.

A_{VC} is the DC gain of the loop, ω_R is the right half plane zero, ω_Z is the load zero formed by C_{out} and its ESR, ω_P is the load pole formed by C_{out} and R_{out} and ω_L is the inductor pole:

$$\frac{\bar{V}_{out}}{\bar{V}_C} = A_{VC} \times \frac{1 - \frac{s}{\omega_R} \times 1 + \frac{s}{\omega_Z}}{1 + \frac{s}{\omega_P} \times 1 + \frac{s}{\omega_L}} \quad (25)$$

$$A_{VC} \approx R_{out} \times n \times \frac{(1-D)}{2 \times R_L} \quad (26)$$

$$R_i = A_{CS} \times R_S \quad (27)$$

$$\omega_R = \frac{R_{out} \times n \times (1-D)^2}{L} \quad (28)$$

$$\omega_Z = \frac{1}{C_{out} \times R_{ESR}} \quad (29)$$

$$\omega_P \approx \frac{2}{C_{out} \times R_{out}} \quad (30)$$

$$\omega_L = \frac{K_M \times R_i}{L} \quad (31)$$

$$K_M \approx \frac{V_{out}}{V_{SLOPE}} \quad (32)$$

V_{SLOPE} is the amount of slope compensation required to avoid sub harmonic oscillation and is set to:

$$V_{SLOPE} = \frac{(V_{out} - V_{in}) \times R_i}{L \times F_{SW}} \quad (33)$$

F. Error Amplifier Stage

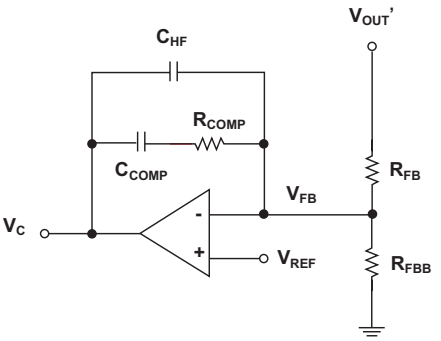


Figure 14 – Type II error amplifier.

The LM5122 has a voltage error amplifier and is used as an example for type II compensation stability analysis as in Figure 14. The strategy presented here requires the top feedback resistor to be selected somewhere between 2 kΩ and 200 kΩ. 10 kΩ is used for this example.

Next, the modulator gain worst case needs to be found. This is at maximum D, which is at the minimum input voltage as well as max load. For the design example here, it is an automotive system so assume the V_{in} minimum operation is 9 V.

$$D_{max} = \frac{V_{out} - V_{in\_Min}}{V_{out}} \quad (34)$$

where D_{max} is 0.625. Now find the worst case modulator gain using Equation 35:

$$G_{M\_Mod} = \frac{1 - D_{max}}{R_I} \quad (35)$$

The LM5122 has a current sense gain of 10 and, assuming a current sense resistor of 4 mΩ, applying Equation 27 yields R_i=40 mΩ. Next, to find the right half plane zero (RHPZ) frequency use Equation 36:

$$RHPZ = \frac{R_{out} \times (1 - D)}{L \times 2\pi} \quad (36)$$

This yields an RHPZ frequency of 52 kHz. The cross over frequency (F_C) is set to RHPZ/4 or ~12.5 kHz for this example. This is the target FC and from this the mid band gain (A_{VM}) is determined using the results from Equations 35 and 36 as shown below:

$$A_{VM} = \frac{\omega_C \times \frac{C_{out}}{n}}{G_{M\_Mod}} \quad (37)$$

This yields an A_{VM} of 4.4. Once the A_{VM} has been determined R_{COMP} is calculated using:

$$R_{COMP} = A_{VM} \times R_{FBT} \quad (38)$$

This yields an R_{COMP} of 44 kΩ.

To calculate C_{COMP} use the following equation knowing that the zero should be placed at approximately ω_{ZEA}:

$$C_{COMP} = \frac{1}{R_{COMP} \times \omega_{ZEA}} \quad (39)$$

where:

$$\omega_{ZEA} = \frac{\omega_C}{10} \quad (40)$$

This yields a capacitance of ~2.8 nF. Given that the nearest available value is 2.7 nF, that is what is chosen for this example.

Finally, set the high frequency pole to the RHPZ frequency:

$$C_{HF} = \frac{1}{R_{COMP} \times \omega_{HF}} \quad (41)$$

where:

$$\omega_{HF} = \omega_R$$

This yields a C_{HF} of 68 pF.

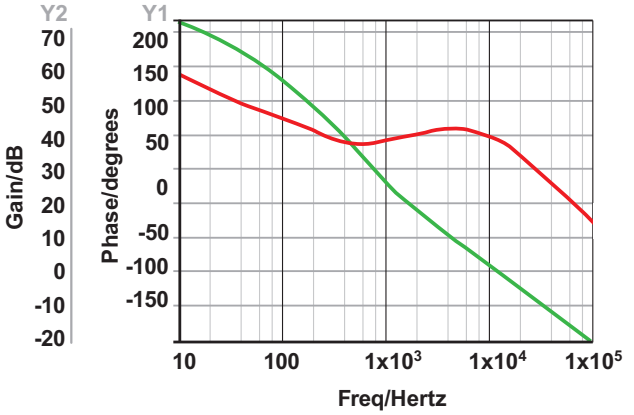


Figure 15 – Simulation results.

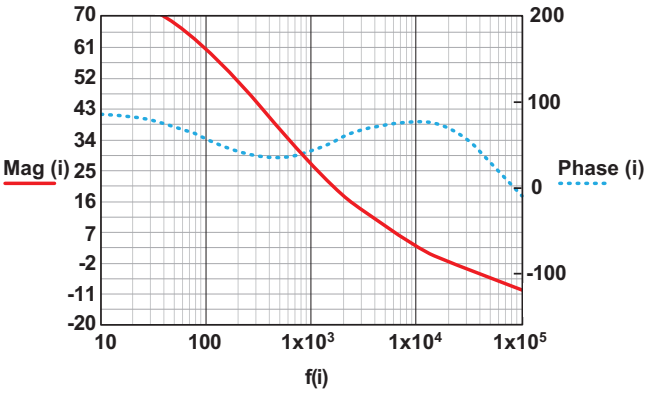


Figure 16 – MathCAD results.

The above results are produced from the calculated values. Some good correlations from the approximations used can be seen. The simulation shows a crossover frequency of ~13 kHz and a PM of ~50 degrees. MathCAD results in Figure 16 show an FC of ~13 kHz and a PM of 75 degrees. Both results, although approximations, show stable results. Gain bandwidth (GBW) of the error amplifier affects the results and needs bench verification. For simplicity this is not used in the MathCAD calculations, hence some discrepancies between the phases on the simulation versus the MathCAD result. This discrepancy is because the pole skews results from a phase perspective while the gain error due to the pole is insignificant, hence matching crossovers.

VII. Design Examples – Two Phase Approach

As mentioned earlier the switching frequency can be divided down by a factor of two to obtain the same effective switching frequency of the power supply. By implementing this approach the switching frequency of each phase is now set to 125 kHz. The simplest approach for the two phase calculations is to split the currents by the number of phases and then run through the calculations as before in the single phase approach. Care must be taken when calculating the input RMS ripple currents and output RMS ripple current ratings for the input and output capacitors. Different equations must be applied to correlate to the interval the boost is operating in, for example for the two phase approach, different equations must be applied when $D < 0.5$ and when $D > 0.5$ as will be detailed later. The duty cycle remains the same as the single phase but the Tperiod/2 staggers the timing of each duty between the phases. In the case of the 2 phase approach this means that the duty between the phases is staggered by 180 degrees.

The duty cycle in the two phase case is 0.42 as before. The power at the output is the same as before also. However the average input current of the phases is:

$$I_{in\_Avg} = \frac{P_{in}}{V_{in} \times n} \tag{42}$$

This yields an average input current for each phase of 6.8 A. Setting the peak-to-peak ripple current in the inductor to ~3.5 A and using Equation 5 yields an inductance of 15 µH. In addition, Equation 6 yields a peak current of 8.4 A. The ISAT of the inductor must be greater than 8.4 A to avoid saturation of the inductor.

Recall that a 3 µH inductor was selected for the single phase example with a saturation current rating requirement of about 18.5 A. Now for the two phase example a much higher inductance is required due to the lower effective input current and, more significantly, due to the drop in the switching frequency per phase. The size impact is not as bad as it appears at first because the ISAT is now significantly lower than the single phase example. For this example a Coilcraft SER1390-153 is used with a size of 13.5 mm x 13.5 mm x 9 mm. This is a core volume of 2 x 1640 mm^3 vs. 1 x 1300 mm^3 for the single phase. If size is of more importance than efficiency, then keeping the switching frequency the same in the two phase approach yields much lower core volumes for the dual phase approach.

A. DCR Losses in Inductor -- Two Phase Approach

To calculate the RMS current in the inductor use Equation 7. This yields ~7 A RMS current with ~14 mΩ DCR. Equation 8 yields 0.67 W of conduction loss, which for two phases totals ~1.4 W.

B. Core Losses -- Two Phase Approach

Using the online calculator previously mentioned for 6.9 A of RMS current and a peak-to-peak inductor ripple current of 3.0 A at a switching frequency of 125 kHz yields a core loss of 9 mW, 18 mW total for two inductors. This may appear to be out of place considering the high core losses in the single phase example. However, considering that a much larger inductor is used this significantly reduces the flux density in the core because the currents are now reduced as a result of interleaving. Another significant factor is the reduction in switching frequency, which provides an additional advantage over the single phase approach. The total losses for the inductor will be ~1.4 W total for two phases versus ~3.2 W for the single phase approach, a significant savings.

C. Conduction Losses – Two Phase Approach

The average input current is divided by two because the currents are shared between two phases. The switch RMS current is approximated by Equation 10, yielding an RMS switch current of 4.4 A.

Again, for this example, the CSD18531 FET was selected. This has an RDSon of 3.5 mΩ for a 10 V gate drive. This example assumes a hot RDSon of 4 mΩ.

Using the estimated RDSon and applying Equation 11 (shown here again for convenience):

$$FET_{Cond} = I_{FET\_RMS}^{2} \times RDS_{on} \quad (11)$$

yields approximate losses of 0.08 W, or for two phases 0.16 W.

D. Transitional Losses – Two Phase Approach

Again, for estimating the worst case transitional losses Equation 12 is applied.

$$SW_{TRANS\_Loss} = V_{out} \times I_{in\_Avg} \times T_{SLEW} \times F_{SW} \quad (12)$$

This yields transitional losses of 0.4 W or for two phases a total of 0.56 W.

E. Sync FET Losses – Two Phase Approach

Approximation of the RMS current in the sync FET uses Equation 13:

$$I_{FET\_RMS} = \sqrt{1-D} \times I_{in\_Avg} \quad (13)$$

This yields an RMS current of ~5.3 A. Using this value, the conduction losses in the synchronous rectifier are calculated using Equation 14:

$$FETCond = I_{(FET\_RMS)}^{2} \times RDS_{on} \quad (14)$$

This yields sync FET losses of 0.11 W or total losses for two phases of 0.22 W.

F. Q_{OSS} Losses Reflected in the Boost FET – Two Phase Approach

Q_{OSS} for the FET is 32 nC and the switching loss reflected into the boost FET is again calculated by applying Equation 15:

$$Q_{OSSLoss} = \frac{Q_{OSS}}{2} \times V_{out} \times F_{SW} \times n \quad (15)$$

This yields 0.096 W per phase or a total of 0.192 W and leads to total losses in the boost FET of 0.507 W (0.253W per phase).

G. Q_{RR} Losses Reflected in the Boost FET – Two Phase Approach

Two synchronous FETs are used in a dual phase boost, which result in two Q_{RR}'s so the total Q_{RR} is 200 nC – the switching frequency divided by two yields the same Q_{RR} losses. Using Equation 16 and applying 200 nC at 125 kHz yields Q_{RR} losses incurred in each boost FET to be 0.6 W.

$$Q_{RR\_Loss} = Q_{RR} \times V_{out} \times n \times F_{SW} \quad (16)$$

H. I_C Losses – Two Phase Approach

The Q_G is double for dual phase, the switching frequency is divided by two, and the I_Q is double. Use these values and Equation 17 to calculate the total I_C losses:

$$I_{C\_Loss} = V_{in} \times n \times \left\{\left(Q_{Gtot} \times F_{SW}\right) + I_Q\right\} \quad (17)$$

This yields a total I_C loss for both controllers of 0.33 W.

I. C_{in} RMS Ripple Currents – Two Phase Approach

Ripple current cancelation because of the phase relationships between the two phases significantly reduces the RMS ripple current rating of the input capacitor. The recommended phase relationship for all multiphase designs for optimal current cancellation is 360 degrees/n phases. Figure 17 below shows a comparison of ripple current cancelation for a boost converter with a two phase, three phase and four phase approach using a ΔI_L of 1 A peak-to-peak.

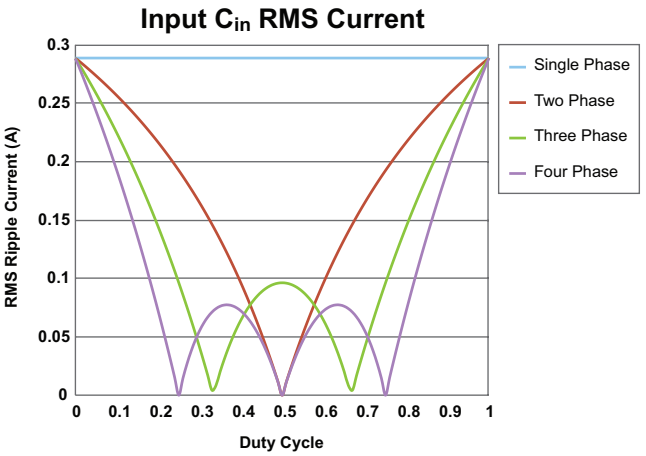


Figure 17 – RMS input ripple current cancellation comparison for 1 phase to 4 phases.

Figure 17 shows the RMS ripple current at the input of a multiphase boost. Comparing the currents between single and two phase, the ripple current at 40% duty cycle (on the x-axis) is around 40% of the ripple current reduction that is gained from using a two phase boost compared to a single phase boost.

As seen in the single phase example previously discussed, the ripple current in the input capacitor is 2.1 A. Using a two phase design for a D < 0.5, the ripple current is equated to:

$$I_{Cin\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \times \frac{(1-2\times D)}{(1-D)} \qquad (43)$$

For a peak-to-peak inductor ripple current of 3 A, this yields a total RMS current of ~0.9 A.

For a single phase approach, multiple capacitors are used in any given design to satisfy a given amount of RMS ripple current. For a two phase approach a clear advantage is realized in size and cost due to the significant reduction in the RMS ripple current. Designers must be cautious when sizing capacitors to satisfy RMS ripple currents – it is advised to allow some margin to allow for mismatch in current sharing that increases the RMS ripple current the capacitor is exposed to from the calculated value.

Condition	Single Phase
$0 < D < 1$	$\frac{\Delta I_L}{\sqrt{12}}$

Condition	Two Phase
$0 < D < 0.5$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{1-2D}{1-D}$
$0.5 < D < 1$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{2D-1}{D}$

Table 1 – RMS input ripple current calculations for a single phase and two phase boost converter.

Condition	Three Phase
$0 < D < 0.33$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{1-3D}{1-D}$
$0.33 < D < 0.66$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{(1-3D) \times (3D-2)}{3D \times (1-D)}$
$0.66 < D < 1$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{3D-2}{D}$

Table 2 – RMS input ripple current calculations for a three phase boost converter.

Condition	Four Phase
$0 < D < 0.25$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{1-4D}{1-D}$
$0.25 < D < 0.5$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{(1-4D) \times (4D-2)}{4D \times (1-D)}$
$0.5 < D < 0.75$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{(3-4D) \times (4D-2)}{4D \times (1-D)}$
$0.75 < D < 1$	$\frac{\Delta I_L}{\sqrt{12}} \times \frac{4D-3}{D}$

Table 3 – RMS input ripple current calculations for a four phase boost converter.

J. C_{OUT} RMS Ripple Current Rating – Two Phase Approach

The cost and size savings from a reduction in the RMS ripple current rating for the output capacitor is significant due to the fact that RMS ripple current in a boost is greater for the output capacitors compared to the input capacitors. Using Equation 44 the RMS ripple current rating is calculated for a two phase boost for D < 0.5.

$$I_{Cout\_RMS} \approx \frac{I_{out}}{\sqrt{2}} \times \frac{\sqrt{D \times (1-2D)}}{(1-D)} \qquad (44)$$

This equation results in 2.5 A of RMS ripple current, compared to 6.71 A in the single phase approach – a ~35% reduction in value!

Figure 18 below shows an approximation of output ripple current cancelation for a boost converter with an I_{out} of 1 A using a single phase, two phase, three phase and four phase approach.

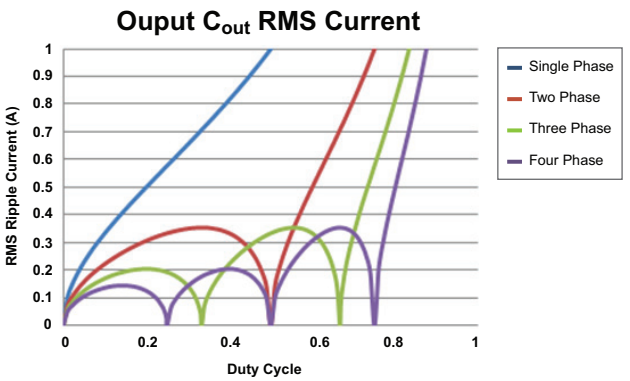


Figure 18 – Approximation of RMS output ripple current cancellation comparison from 1 phase to 4 phases.

Condition	Single Phase
0 < D < 1	$I_{OUT} \times \sqrt{\frac{D}{(1-D)}}$

Condition	Two Phase
0 < D < 0.5	$\frac{I_{OUT}}{\sqrt{2}} \times \frac{\sqrt{D \times (1-2D)}}{(1-D)}$
0.5 < D < 1	$\frac{I_{OUT}}{2} \times \frac{\sqrt{2 \times (2D-1)}}{\sqrt{1-D}}$

Table 4 – RMS output ripple current calculations (approximations) for a single phase and two phase boost converter.

Condition	Three Phase
0 < D < 0.33	$\frac{I_{OUT}}{\sqrt{3}} \times \frac{\sqrt{D \times (1-3D)}}{(1-D)}$
0.33 < D < 0.66	$\frac{I_{OUT}}{3} \times \frac{(3D-2) \times (1-3D)}{(1-D)}$
0.66 < D < 1	$\frac{I_{OUT}}{3} \times \frac{\sqrt{3D-2}}{\sqrt{1-D}}$

Table 5 – RMS output ripple current calculations (approximations) for a three phase boost converter.

Condition	Four Phase
0 < D < 0.25	$\frac{I_{OUT}}{2} \times \frac{\sqrt{D \times (1-4D)}}{(1-D)}$
0.25 < D < 0.5	$\frac{I_{OUT}}{2} \times \frac{\sqrt{(4D-2) \times (1-4D)}}{2 \times (1-D)}$
0.5 < D < 0.75	$\frac{I_{OUT}}{2} \times \frac{\sqrt{(4D-2) \times (3-4D)}}{2 \times (1-D)}$
0.75 < D < 1	$\frac{I_{OUT}}{2} \times \frac{\sqrt{4D-3}}{\sqrt{1-D}}$

Table 6 – RMS output ripple current calculations (approximations) for a four phase boost converter.

1x PCV1E391MCL2GS was selected as the output capacitor for the two phase example. This is a 25 V rated 390 µF capacitor with an RMS ripple current rating of 4.2 A and an ESR of 21 mΩ.

The given ripple voltage requirement is 1%, which is 240 mV. The output capacitance needed is calculated using Equations 20, 21, 22 and 23 and results in 147 mV total ripple voltage for half the capacitance.

K. Stability Consideration for a Multiphase Boost

The simplified control to output transfer function for a current mode boost power and modulator remains the same as presented in Equation 25.

$$\frac{\bar{V}_{out}}{\bar{V}_C} = A_{VC} \times \frac{1-\frac{s}{\omega_R} \times 1+\frac{s}{\omega_Z}}{1+\frac{s}{\omega_P} \times 1+\frac{s}{\omega_L}} \quad (25)$$

However, there are some adjustments that must be made to accommodate the interleaved configuration. A simple method is simply to divide down the C_{out} by n phases, multiply the C_{out}'s ESR by n phases and multiply R_{out} by n phases. C_{out} becomes 195 µF from 390 µF and the ESR becomes 40 mΩ from 20 mΩ. R_{out} becomes 6 Ω from 3 Ω. All other elements are kept the same. With this stability approach the RHPZ is adjusted in Equation 25 using:

$$\omega_R = \frac{R_{out} \times n \times (1-D)^2}{L} \quad (28)$$

where n is the number of phases.

The adjusted RHPZ affects the crossover frequency (F_C). Also R_I changes due to the lower current flowing through each phase. The new RHPZ as dictated by the two phase approach is now ~21 kHz which now forces a cross over frequency at ~5 kHz.

L. Error Amplifier Stage for Two Phase Boost

For stability analysis using type II compensation for a dual phase a resistor value between 2 kΩ and 200 kΩ must be chosen – 10 kΩ is selected for the top feedback resistor in this example. Next, find the modulator gain at the worst case – this is at maximum D, which is at minimum input voltage and also at maximum load. Also assume a V_{in} minimum operation of 9 V. Using

$$D_{max} = \frac{V_{out} - V_{in\_Min}}{V_{out}} \quad (34)$$

yields D_{max} of 0.625. Now find worst case modulator gain using:

$$G_{M\_Mod} = \frac{1-D_{max}}{R_I} \quad (35)$$

The LM5122 has a current sense gain of 10 so applying Equation 20 yields R_i = 10 x Rsense. Assuming a current sense resistor of 8 mΩ, R_i now equals 80 mΩ.

As previously pointed out RHPZ is at ~21 kHz which forces F_C to be ~5 kHz. With this target F_C, the mid band gain (AVM) is calculated using results from Equations 35 and 36, as shown below:

$$A_{VM} = \frac{\omega_C \times \frac{C_{out}}{n}}{G_{M\_Mod}} \quad (37)$$

This yields an AVM of 1. Now calculate R_{COMP} using Equation 38:

$$R_{COMP} = A_{VM} \times R_{FBT} \quad (38)$$

This yields an R_{COMP} of 10 kΩ. Now that R_{COMP} has been calculated, calculate C_{COMP} using the equation below knowing that the zero should be placed approximately at ω_{ZEA}:

$$C_{COMP} = \frac{1}{R_{COMP} \times \omega_{ZEA}} \quad (39)$$

where:

$$\omega_{ZEA} = \frac{\omega_C}{10} \quad (40)$$

This gives a capacitance of ~29 nF. Finally, set the high frequency pole to the RHPZ frequency:

$$C_{HF} = \frac{1}{R_{COMP} \times \omega_{HF}} \quad (41)$$

where:

$\omega_{HF}=\omega_R$

This leads to a CHF of 720 pF, meaning an 820 pF capacitor should be used.

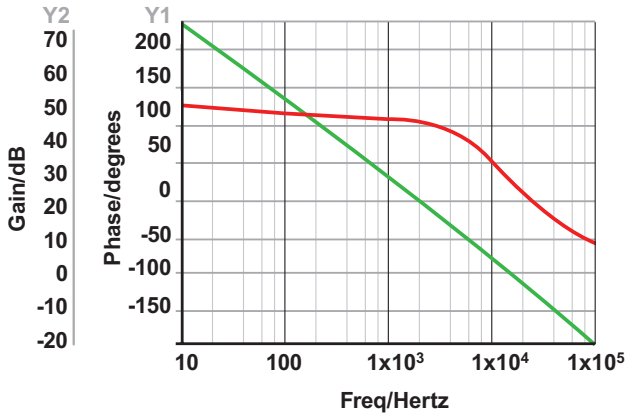


Figure 19 – Two phase simulation results.

The simulation results show an F_C of ~5 kHz and a PM of ~56 degrees.

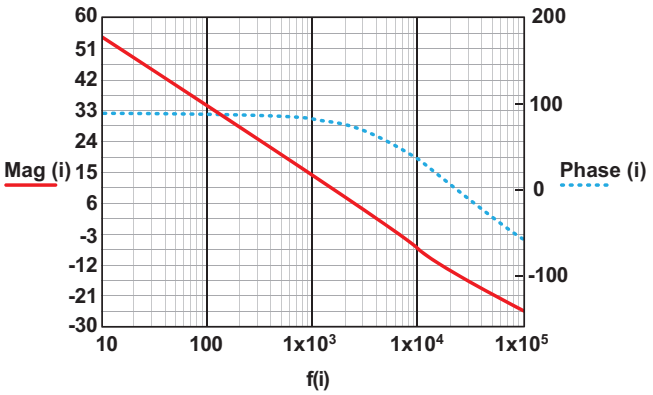


Figure 20 – Two phase MathCAD results.

MathCAD results correlate well to the simulation, showing an FC of ~5 kHz and a PM of ~60 degrees. Again because of approximations used the results do differ some.

VIII. Summary of Results

Table 8 below shows a summary of the values comparing the single phase and two phase approach for the specification used as an example.

Parameter	Single Phase	Two Phase
Per Phase Switching Frequency	250 kHz	125 kHz
Inductance Value	3 µH	15 µH
Isat	15A	9 A
Energy (1/2 L*I^2)	**337.5 µJ**	**1.215 mJ**
Inductor DCR Losses	0.6 W	1.4W Total
Inductor Core Losses	2.6 W	0.018W Total
Rsense	4 mΩ	8 mΩ
Rsense Losses	0.9 W	0.8W Total
Boost FET Conduction Losses	0.3 W	0.16W Total
Boost FET Transitional Losses	0.8W	0.4W Total
FET Qoss Losses	0.2 W	0.2W Total
QRR Losses	0.6 W	0.6 W
Synchronous FET Conduction Losses	0.44 W	0.22 W
IC Losses	0.182 W	0.336 W
Total Losses	**6.097 W**	**3.734 W**
Calculated Efficiency	**~97%**	**~98%**
Cin RMS Ripple Current Rating	2.1 A	0.9 A
Cout RMS Ripple Current Rating	6.7 A	2.5 A
Cin	22 µF	22 µF
Cout	780 µF	390 µF
Fc	**12.5 kHz**	**5 kHz**

Table 7 – Single phase and two phase comparison of key parameters for a 14 V_{in}, 24V_{out} @ 8 A requirement.

Table 8 below shows the component count comparison between the two boards that were built for this paper.

	Part Number	Single Phase	Part Number	Two Phase
MOSFETs	CSD18531Q5A	2	CSD18531Q5A	4
C_{in}	25V Ceramic	1	25V Ceramic	1
C_{out}	PCV1E391MCL2GS	2	PCV1E391MCL2GS	1
Inductor	XAL1580-302	1	SER1390-153	2
I_C	LM5122	1	LM5122	2
R_{sense}	2W Current Sense	1	2W Current Sense	2
Total		8		12

Table 8. Single phase and two phase comparison: key component count.

As is seen in Table 8 the cost of a two phase design approach can potentially increase. However, this is not necessarily definite as it will depend on the design parameters of a given requirement. For example, a design may have many more input capacitors and output capacitors for a single phase than a two phase design, offsetting the component count increase for the IC and FETs needed in the two phase designs. There may also be a need for heat sinks on the single phase, which can be more costly.

A. Test Results

A single phase and a two phase board were built up according to the example specifications given in this paper. Results are compared in terms of cost, size and efficiency for each design.

B. Efficiency and Thermals Comparison

i. Single Phase Efficiency

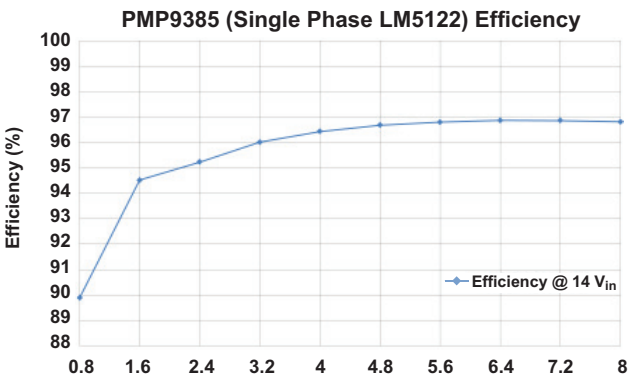


Figure 21 – Single phase efficiency (actual results).

Referring to Table 7, in particular the total losses of ~6.097 W, from this the efficiency of the single phase is approximated to be ~97%. Looking at Figure 21, this correlates very well with actual results taken from a single phase LM5122 evaluation board.

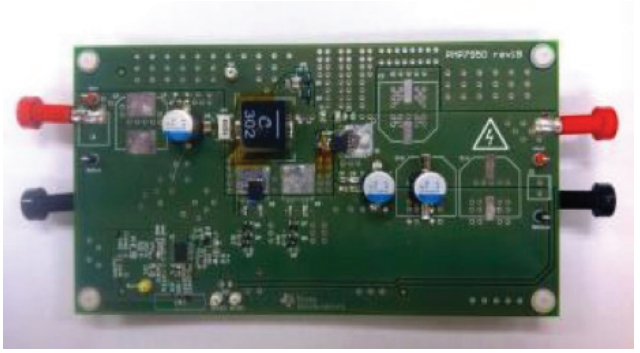


Figure 22 – Single phase board photo: board size is 6.3"x 3.5" (PMP9385).

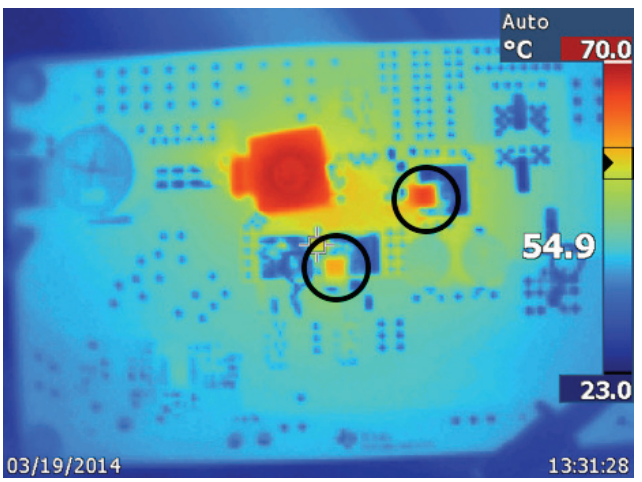


Figure 23 – Single phase board thermal photo.

Figure 23 shows the peak temperature on the board is ~70 °C at an ambient temperature of 20 °C, resulting in a ~40 °C temperature rise. The hottest components are the inductor, sync FET and sense resistor. Also note that due to the extensively large size board, the temperature rise in this particular case seems to be fairly manageable.

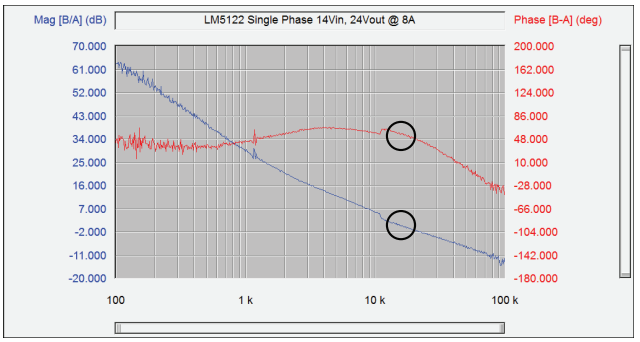


Figure 24 – Bode plot of single phase board at full load.

Figure 24 shows a Bode plot measured from the single phase board using a network analyzer. Cross over was measured to be ~13.5 kHz and the phase margin is ~60 degrees.

ii. Two Phase Efficiency

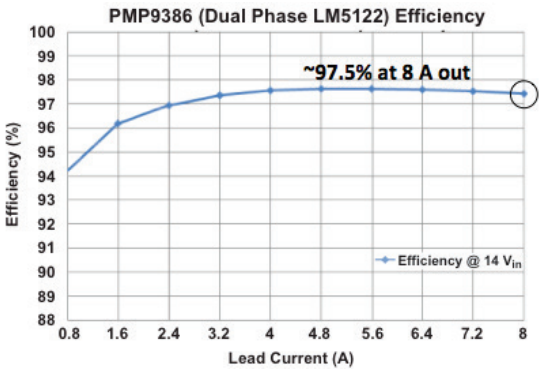


Figure 25 – Two phase efficiency (actual results).

Looking at table 7 again, the total losses for the two phase design are ~3.7 W and from this the efficiency of the two phase design is estimated to be ~ 98%. Figure 25 shows that this correlates well with actual results taken from a single phase LM5122 evaluation board, obtaining an efficiency of ~98% which is a saving of ~2 W.

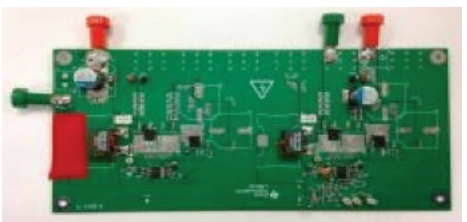


Figure 26 – Two phase board photo: board size is 7.5"x 3.5" (PMP9386).

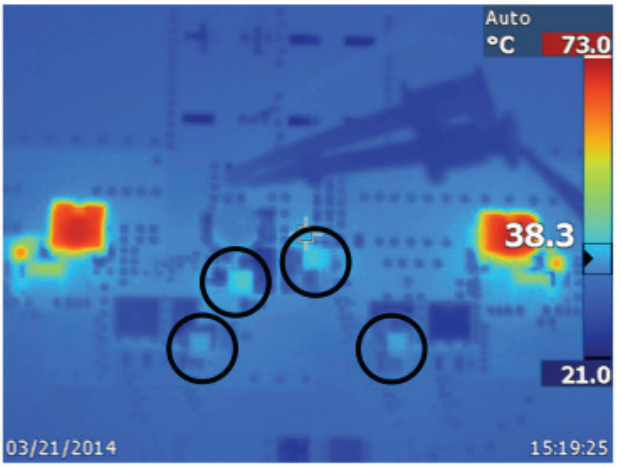


Figure 27 – Two phase board thermal photo.

Figure 27 shows the peak temperature on the board is ~70 °C at an ambient temperature of 20 °C, which results in a ~50 °C temperature rise. In this case, the hottest components are the inductors only. In comparison, the single phase board had heat generated from the FETs and Rsense as well. Also note in Figure 27 that the MOSFETs are very cool, with only ~10 °C temperature rise.

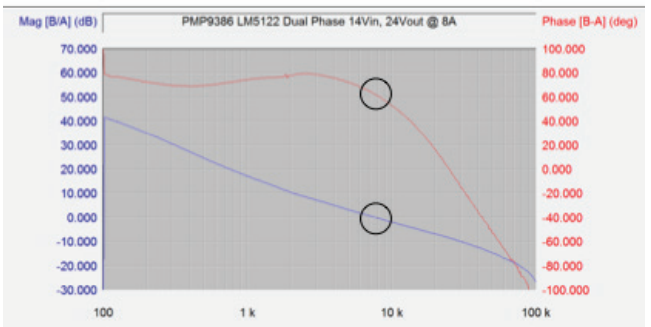


Figure 28 – Bode plot of two phase board at full load.

Figure 28 shows the Bode plot measured from the two phase board using a network analyzer. Cross over was measured to be ~3.5 kHz and the phase margin is ~130 degrees.

IX. Conclusion

This paper has presented a step-by-step approach in order to optimize a single or two phase interleaved boost to meet size, cost and efficiency/thermal performance. Size and cost trade-offs are made when comparing the amount of FETs, capacitors and ICs needed for a given requirement as well as how these selections impact efficiency and thermal performance. A method for compensating a single phase boost and a multiphase boost has also been shown. The results show that significant reduction in heat dissipated in the MOSFETs is realized using a multiphase boost.

X. References

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