Section I [Individual Work]

1) True-False

Print True (T) or False (F), whichever is *more appropriate,* following each statement. Please include in your answer why you believe the answer is true or false. Please be succinct.

(a) During the discharge of an output node (in a logic gate) the energy stored in its capacitance is dumped into ground .

T;

(b) Logical effort g is independent of the size of the transistors in a logic gate.

T: logical effort is related to gate ratios and topology.

(c) Gate leakage of PMOS transistors is lower than NMOS transistors of the same t_{ox}.

T: electron mobility > hole mobility

(d) The larger the transistors in the critical path of a circuit, the lower the delay.

F: $\tau = RC$ Large transistors increase R which increase τ.

(e) The dynamic power dissipation of a NAND gate whose one input is grounded, equals zero.

F: If other input has frequency f between logic 0 or 1, $P_{dynamic} = \alpha C V^2 f$ $P_{dynamic}$ is non-zero.

(f) Method of Logical Effort is used to optimize the power dissipation in a digital CMOS circuit.

F: Method of Logical Effort is used to minimize delay or latency in a CMOS circuit.

(g) High V_t transistors can be used in non-critical paths to save energy.

T: High V_T is used in non-critical path
Low V_T is used in critical path

(h) Instantaneous power is used to determine the wire thickness.

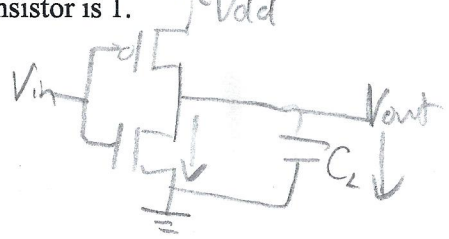
T: $P = IV = \frac{V^2}{R}$ wire thickness $\propto \frac{1}{R}$

(i) A digital circuit sized for minimum delay, has the maximum power consumption.

F: $P = \alpha C V^2 f$ Power consumption is most affected by V_{DD}.

(j) The ratio of the stored energy at the output capacitance of an inverter to the heat dissipated by its PMOS transistor is 1.

T:

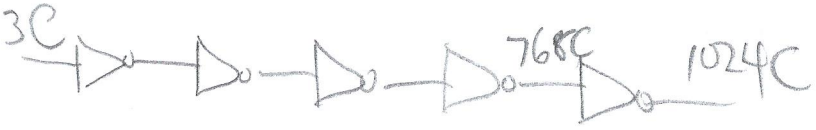


2) Multiple Choice Questions

Print the letter corresponding to the *most appropriate* answer and add an explanation as to why that is the best answer.

(a) If the optimum number of inverters driving a load is 5, and the input capacitance of the first inverter is 3 units, what is the input capacitance of the last inverter?

(b) 15
(b) 768
(c) 48
(d) 1875



$N = \log_4(F) = 5$

$F = 1024$

$4^4 \cdot 3 = 768$

3) If we ignore the parasitic delay of inverters, the optimum stage effort is

(a) 4.
(b) π.
(c) e.
(d) 2.

4) Short-circuit power dissipation is typically about ..... of the total dynamic power?

(a) 10%
(b) 30%
(c) 50%
(d) 70%

Relates to transistor switch, both PMOS/NMOS can be on at the same time

5) Decreasing which parameter among the following is most effective in reducing dynamic power dissipation?

$P_{dynamic} = \alpha C V_{DD}^2 f$

(a) Frequency
(b) Switching activity
(c) Power supply voltage
(d) Effective capacitance

6) If all transistor sizes are the same, and if all inputs are low (i.e. 0), which of the following logic gates has the highest static energy dissipation?

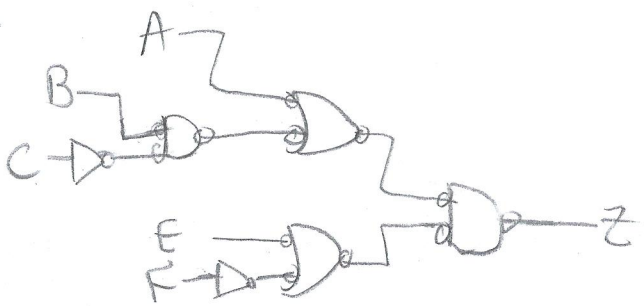
(a) Inverter
(b) NAND
(c) NOR
(d) Tristate inverter

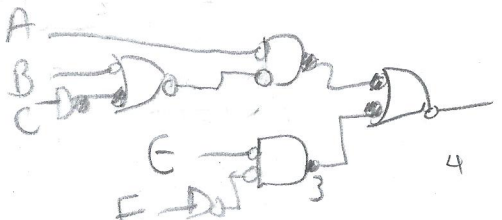
***3)* Logical Effort**

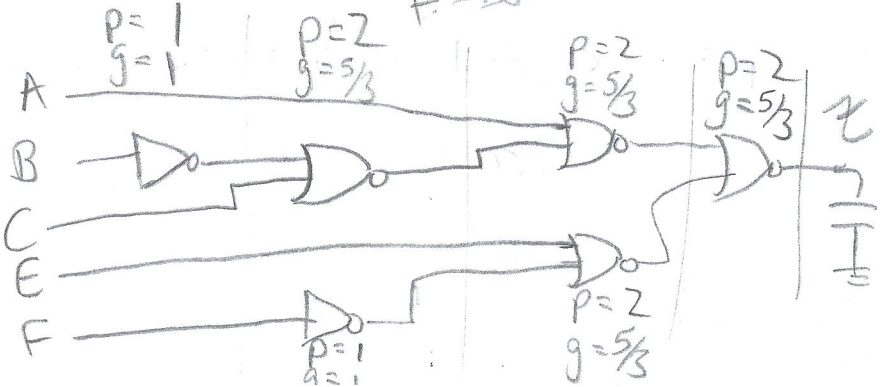
For the conventional CMOS logic gate implementing $Z = (A + B\bar{C})(E + \bar{F})$ find p and g for different inputs.

$Z = (A + B\bar{C})(E + \bar{F})$ $\quad \sim + = \text{NOR}$

$Z = [A \sim + [B \sim + C]] \sim + [E \sim + F]$

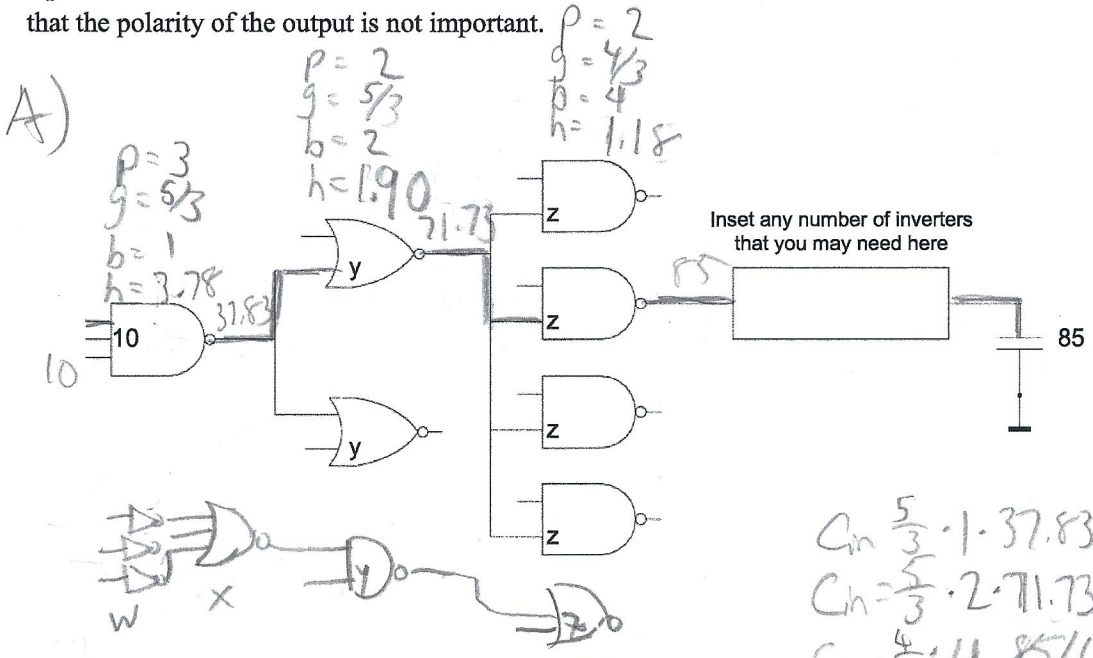






4) Delay Optimization

Consider the following circuit. The input NAND has an input capacitance of 10 units. The output capacitance is equivalent to 85 units. The units can be considered W/L of a transistor with minimum width and length. Assume that the polarity of the output is not important.



$C_{in} = \frac{5}{3} \cdot 1 \cdot 37.83/6.32 = 10$
$C_{in} = \frac{5}{3} \cdot 2 \cdot 71.73/6.32 = 37.83$
$C_{in} = \frac{4}{3} \cdot 4 \cdot 85/6.32 = 71.73$
$C_{in} = gbC_{out}/f_{min}$

A) Beside each logic gate indicate *p*, *g*, *b*, and *h*.

B) Calculate the path effort *F* for the critical path in the circuit.

$F = BGH$
$G = \frac{5}{3} \cdot \frac{5}{3} \cdot \frac{4}{3} = \frac{100}{27}$
$B = 1 \cdot 2 \cdot 4 = 8$
$H = 85/10 = 8.5$
$F = BGH = 8 \cdot \frac{100}{27} \cdot 8.5 = 251.85$
$251.85^{1/3} = 6.32 = f_{min}$

C) Find the optimum number of stages $\hat{N}$ for minimizing the delay in the circuit. Modify the circuit, if necessary to achieve the minimum delay. Revise the parameters *p*, *g*, *b*, and *h* for the logic gates and include inserted inverters.

$N = \log_4 F = \log_4(251.85) = 4$

$F = \pi BGH = (2 \cdot 4)\left(\frac{7}{3} \cdot \frac{4}{3} \cdot \frac{5}{3}\right)(8.5)$
$= 352.60^{1/4} = 4.33$

w	x	y	2p
p = 1	p = 3	p = 2	p = 2
g = 1	g = 7/3	g = 4/3	g = 5/3
b = 1	b = 1	b = 2	b = 4
h = 4.34	h = 1.85	h = 1.62	h = .65

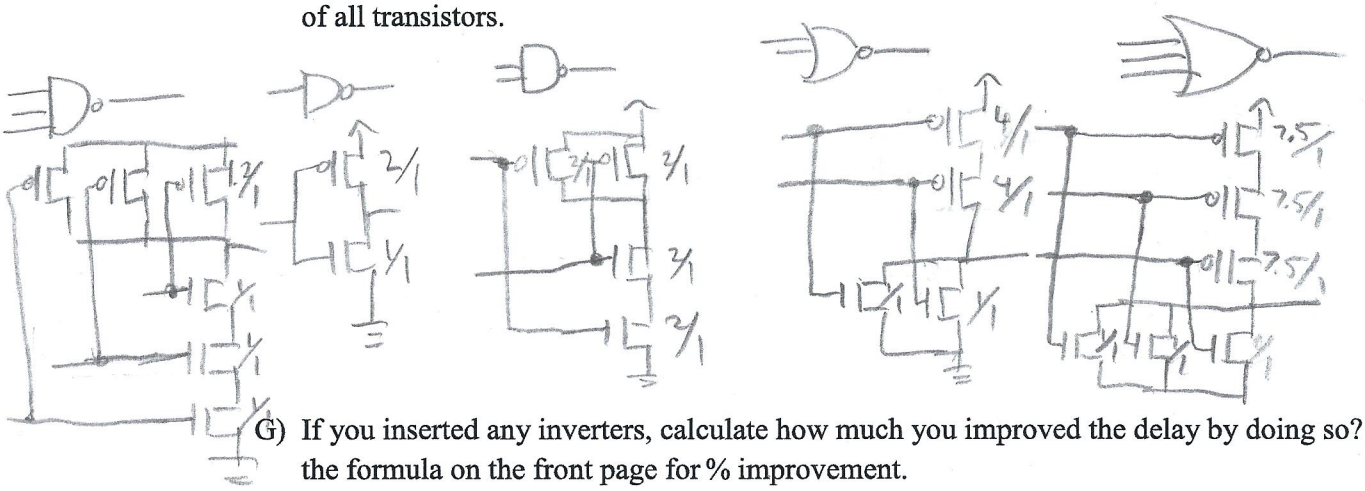
D) Calculate the minimum possible *normalized* and *absolute* delays for the circuit.

Normalized: w, x, y, z: 1, 7/3, 4/3, 5/3
Absolute: w, x, y, z: 1, 7, 4, 5

E) Find the unknown input capacitances for the logic gates, including any inserted inverters.

$C_{inw} = 1 \cdot 1 \cdot 43.43/4.33 = 10$
$C_{inx} = \frac{7}{3} \cdot 1 \cdot 80.6/4.33 = 43.43$
$C_{iny} = \frac{4}{3} \cdot 2 \cdot 130.87/4.33 = 80.60$
$C_{inz} = \frac{5}{3} \cdot 4 \cdot 85/4.33 = 130.87$

F) Draw a schematic diagram of the logic gates in the modified circuit indicating the actual W/L of all transistors.



G) If you inserted any inverters, calculate how much you improved the delay by doing so? Use the formula on the front page for % improvement.

$D = N F^{1/N} + P$

old: $3(251.85)^{1/3} + 3p_{inv} + 2p_{inv} + 2p_{inv} = 25.95$

new: $4(352.60)^{1/4} + 3 + 2 + 2 + 1 = 24.33$

$$\frac{24.33 - 25.95}{25.95} = 6.23\%$$

H) Calculate how much you saved or wasted area (or energy dissipation) by doing so. You may take the total transistor widths as an indication for the area (and energy)?

old: $3\text{NAND} + 2[2\text{NOR}] + [2\text{NAND}]4$

$= 3(1.2 \cdot 8 + 1 \cdot 3) \cdot .6\mu + 2(4 \cdot 8 + 1 \cdot 3) \cdot .6\mu \cdot 2$

$+ 2(2 \cdot 8 + 1 \cdot 3) \cdot .6\mu \cdot 4 = 197.88 \mu m^2$

new $= 3[1\text{NOT}] + 1[3\text{NOR}] + [2\text{NAND}]2 + [2\text{NOR}]4$

$= [3(2 \cdot 8 + 1 \cdot 3) + 3(7.5 \cdot 8 + 1 \cdot 3) + 2(4 \cdot 8 + 1 \cdot 3) \cdot 4$

$+ 2(2 \cdot 8 + 1 \cdot 3) \cdot 4] \cdot .6\mu$

$= 406.8 \mu m^2$

$L_{eff} = .6\mu$

$\frac{\mu_n}{\mu_p} = \frac{8}{3}$

$\mu_p C_{ox} \frac{W_p}{L_p} = \mu_n C_{ox} \frac{W_n}{L_n}$

$\frac{W_p}{W_n} = \frac{8}{3} = \frac{\mu_n}{\mu_p}$

5) Design a *digital modulo-6 counter* with the following characteristics:

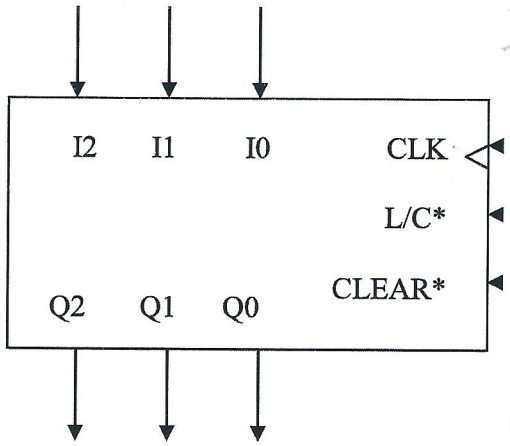
- Three output bits: Q2,Q1,Q0
- Synchronous count – count up on the rising edge of a clock (CLK)
- Synchronous load – load an external input (I2,I1,I0) as the new counter state on the rising edge of CLK
- Asynchronous clear – active-low CLEAR* signal forces the counter state to 000

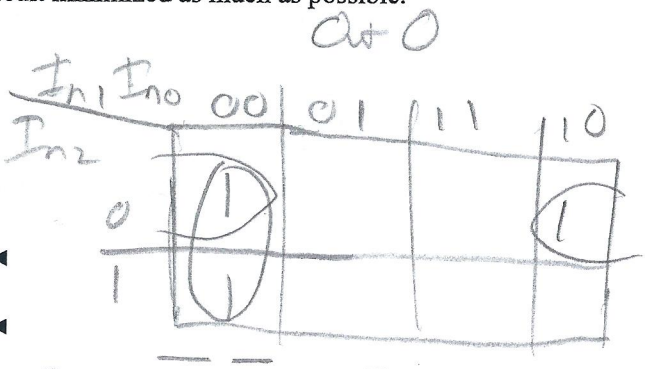
The input/output signals are as follows:

CLK : active-high clock input CLEAR* : active-low clear input
L/C* : high to select load, low to select count I2,I1,I0: parallel data inputs
Q2,Q1,Q0 : parallel data outputs

Your design must use D flip flops and simple logic gates, with the circuit minimized as much as possible. Submit your final schematic diagram and your design work.

In_2	In_1	In_0	Out_2	Out_1	Out_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0





$Out_0 = \overline{In_1}\,\overline{In_0} + \overline{In_2}\,\overline{In_0}$

$Out_1 = \overline{In_2}\,In_1\,\overline{In_0} + \overline{In_2}\,In_1\,\overline{In_0}$

$Out_2 = \overline{In_2}\,In_1\,In_0 + In_2\,\overline{In_1}\,\overline{In_0}$

6) Describe how you would test your counter design.

- What input values will you apply in each clock cycle of the test, and what output values would you expect?
- Indicated the reason for selecting each input pattern (what aspect of the counter design is to be tested?)

L/C 0 | test reset | 1 | test load jump down | 1 | test load jump up | 1 | test load out of bounds
clear 0 | | 1 | | | | | |
I XXX | | | 001 | | 100 | | 111
Q 000 001 010 011 000 001 010 001 010 100 101 000 000

L/C 1 test clear override load.
clear 1
I 100
Q 001 010 000 001