Evolution of transistor technology

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Contents

1. Introduction

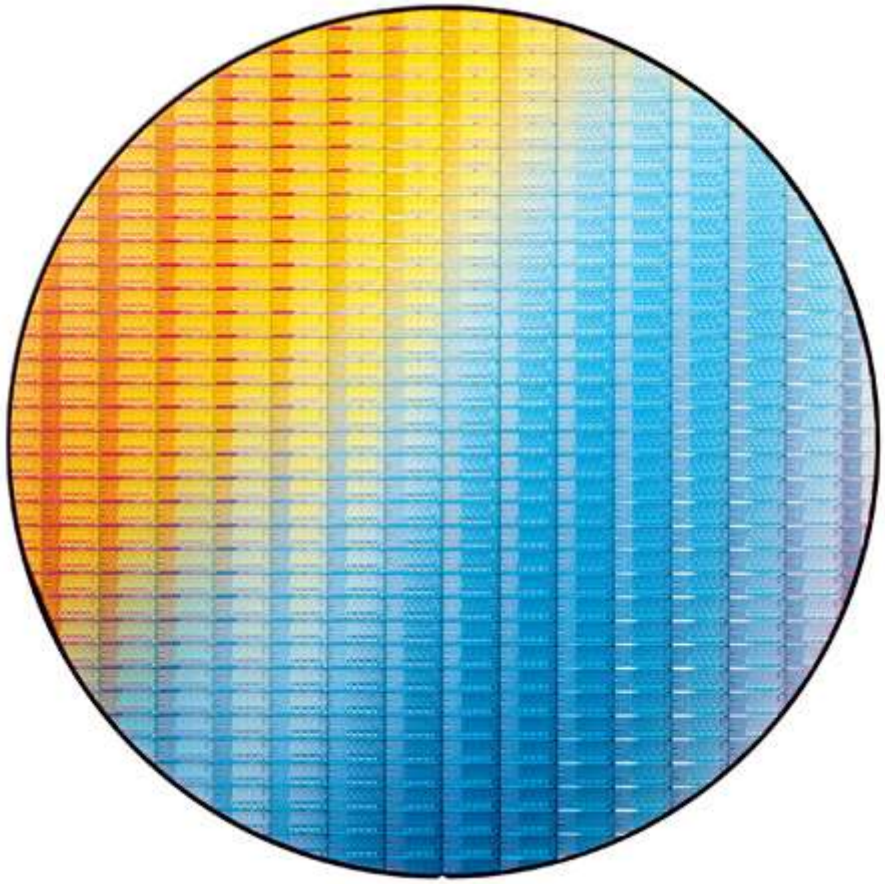
1. Introduction (1)

1. Introduction

Manufacturing of processor chips

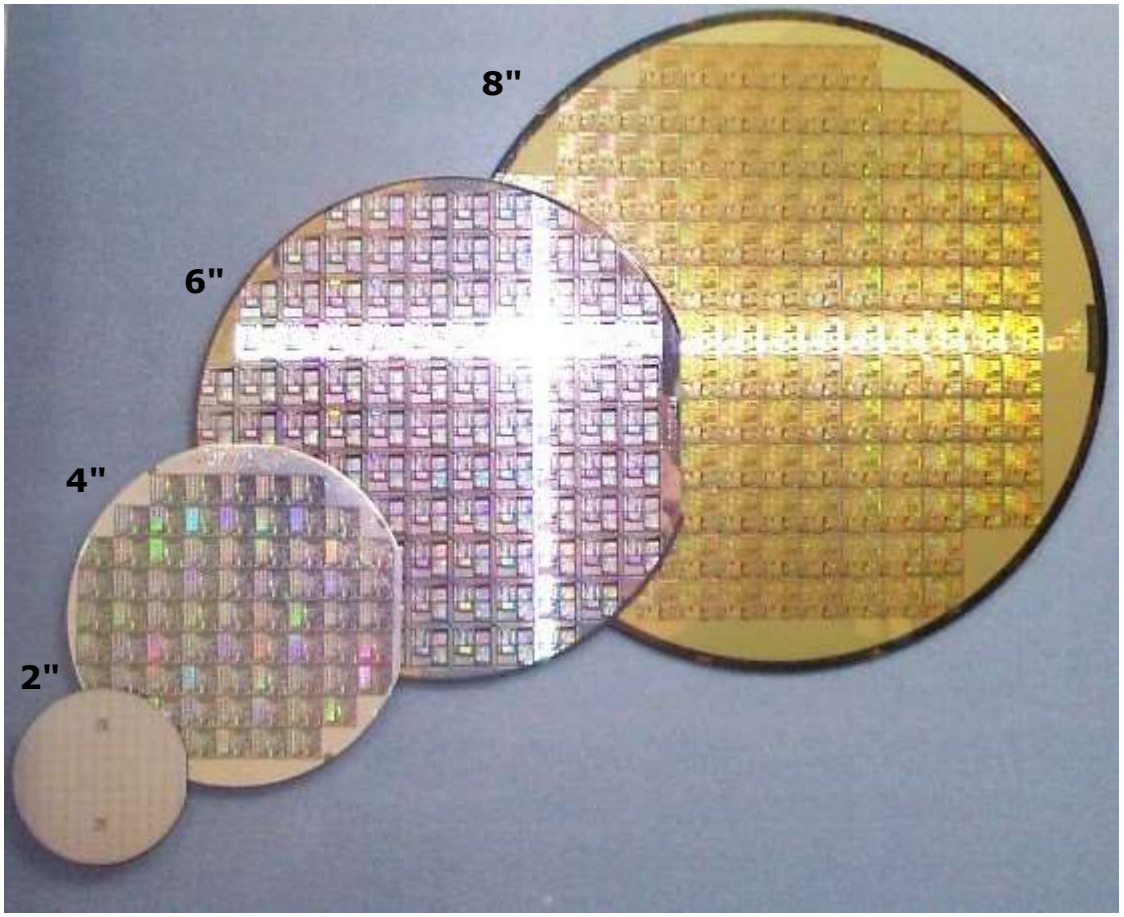
Processor chips are produced on wafers, as seen in the example below.

Example: 22 nm Ivy Bridge chips on a 300 mm wafer [1]



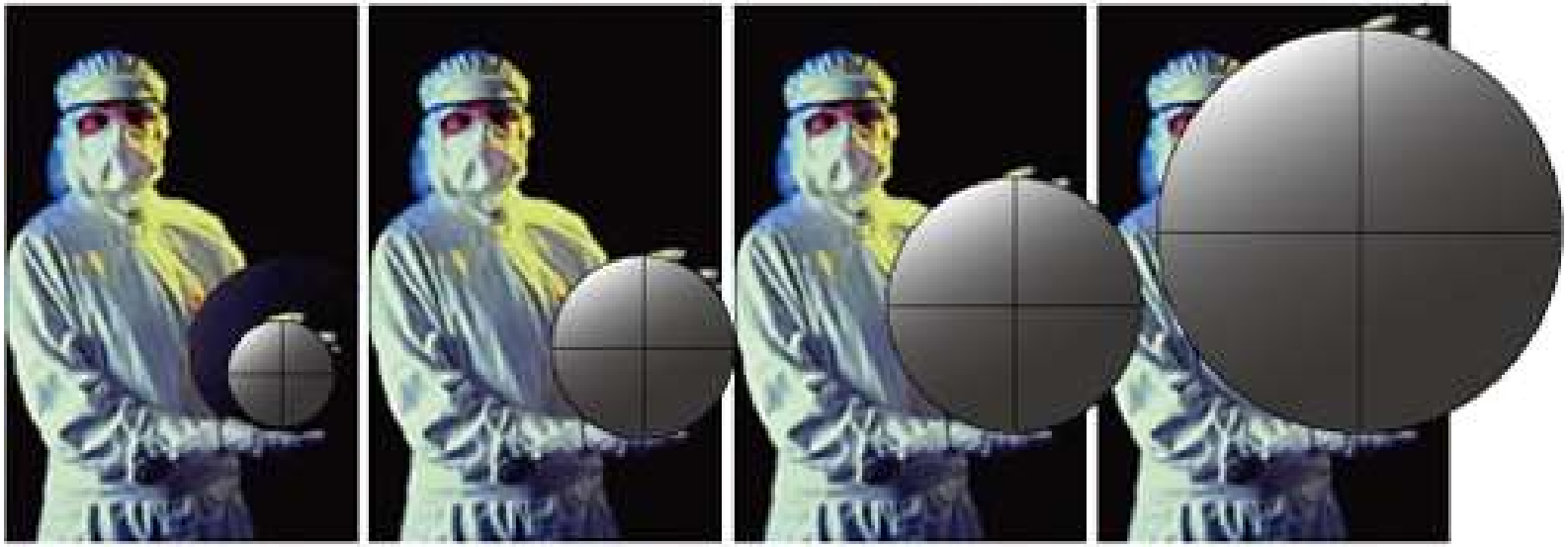
1. Introduction (2)

Early evolution of wafer sizes [2]



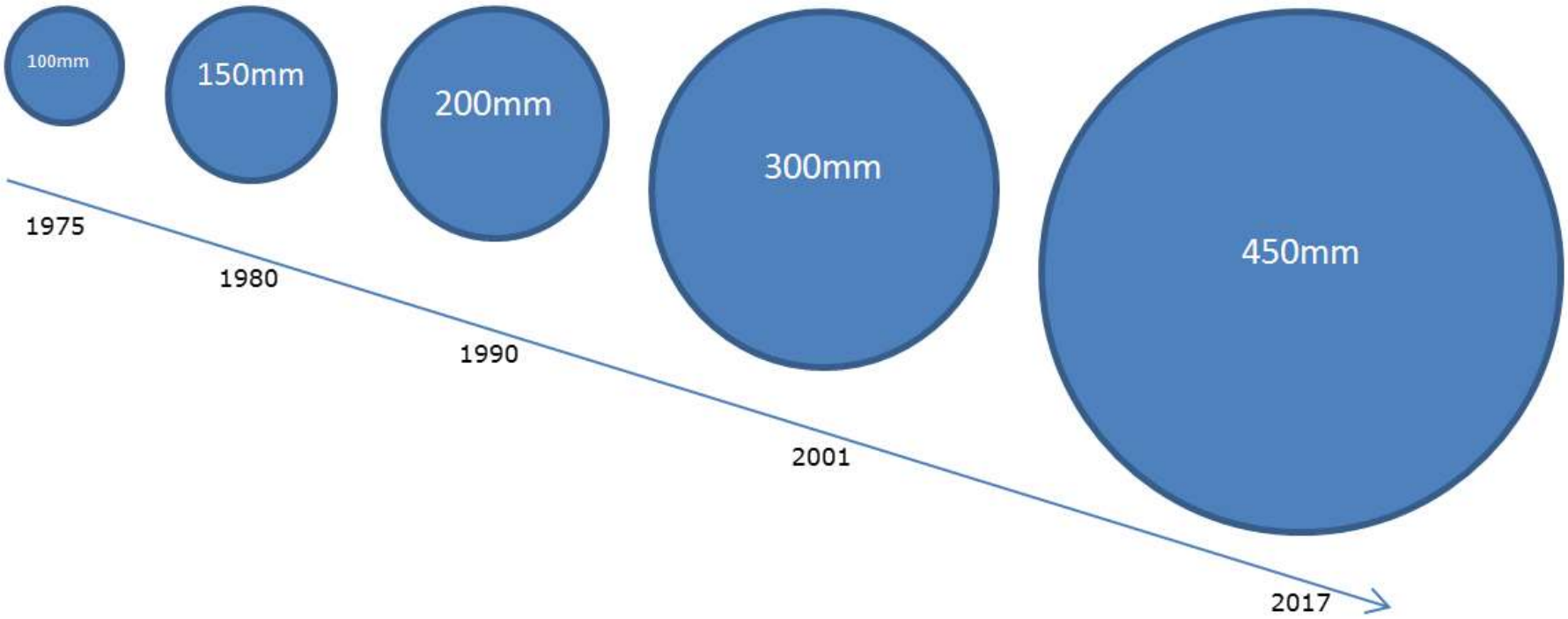
1. Introduction (3)

Subsequent evolution of wafer sizes [3]



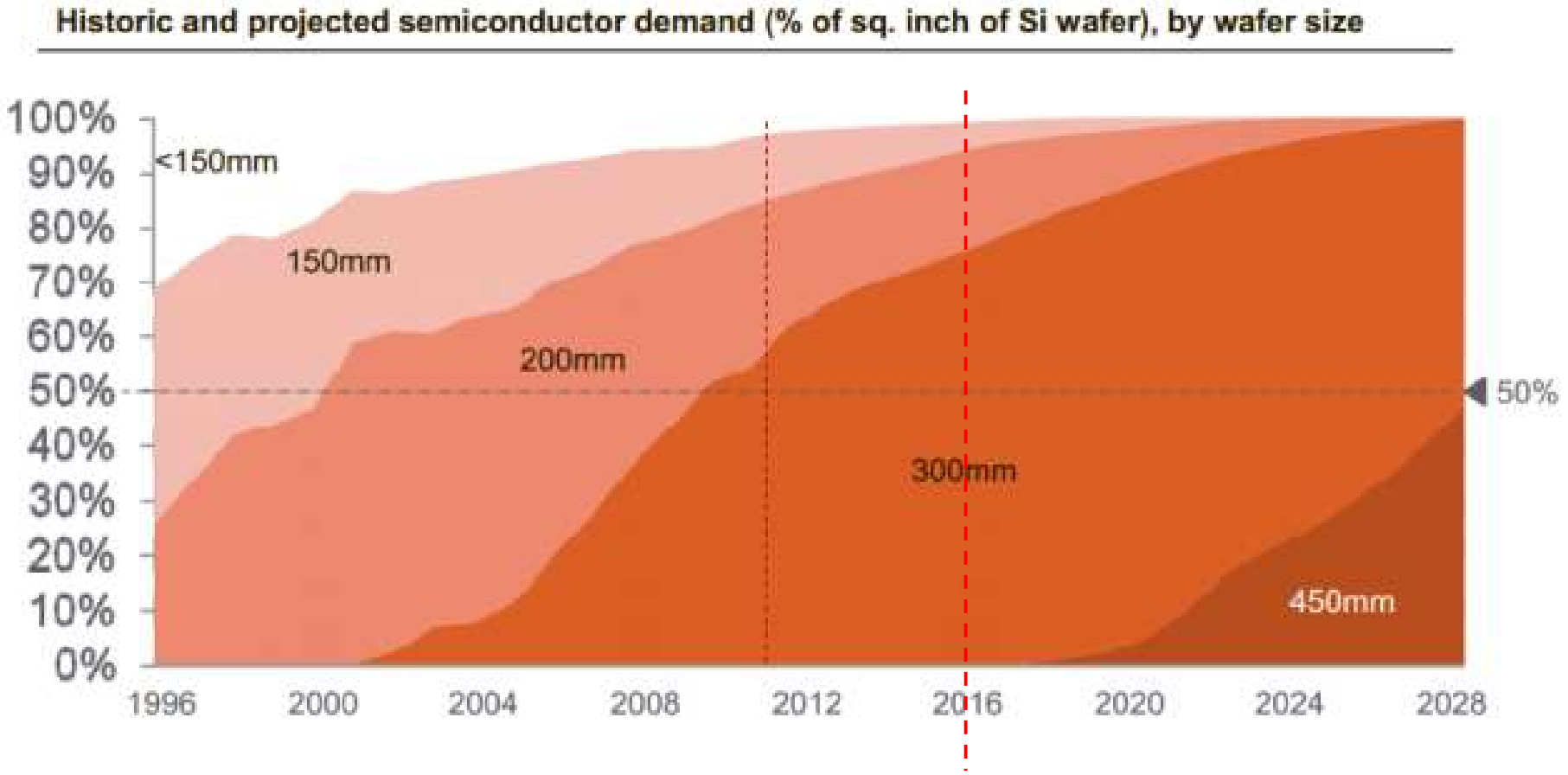
1. Introduction (4)

Introduction dates of larger wafer sizes [4]



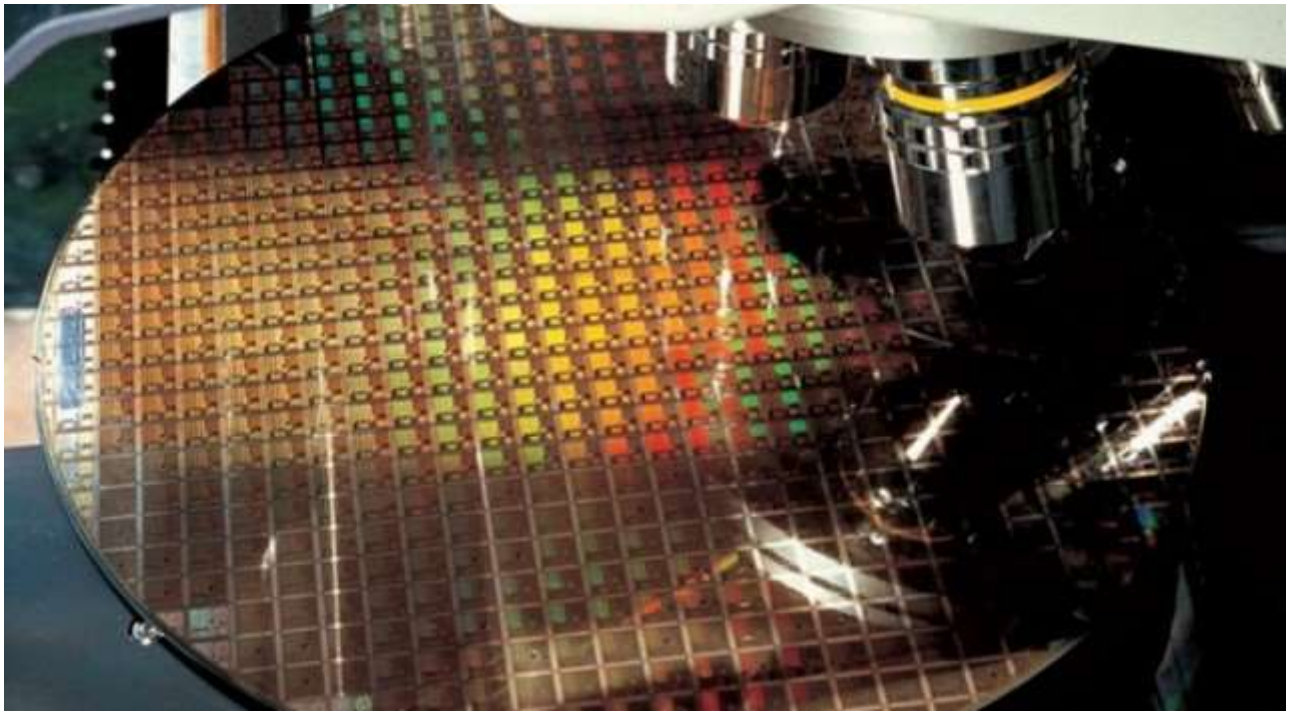
1. Introduction (5)

Historic distribution of wafer sizes actually produced [4]



1. Introduction (6)

Visual checking of chips [5]



1. Introduction (7)

The IC production process

- IC production needs 200 - 300 process steps, based on a number of masks, and includes steps such as diffusion, etching, checkings etc..
- The whole production process lasts about two to three months.
- IC production facilities are called foundries or fabs.

1. Introduction (8)

Internal view of a part of a foundry [6] **-1**

Bird's eye view of a foundry

Figure: Bird's eye view of Globalfoundries Fab 8 in New York (2012) producing 32 nm chips [8]

1. Introduction (12)

Example: Intel's 22 nm foundires [1]

The cost for establishing a foundry

About 3 - 10 billion USD, increasing for smaller feature sizes.

1. Introduction (13)

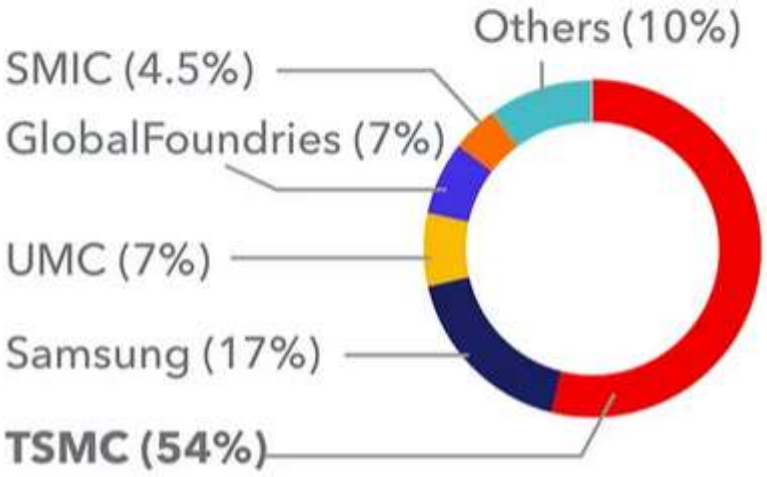
Major integrated circuit foundries [9]

Kw/m: Kilowafer per month in 200 mm equivalents

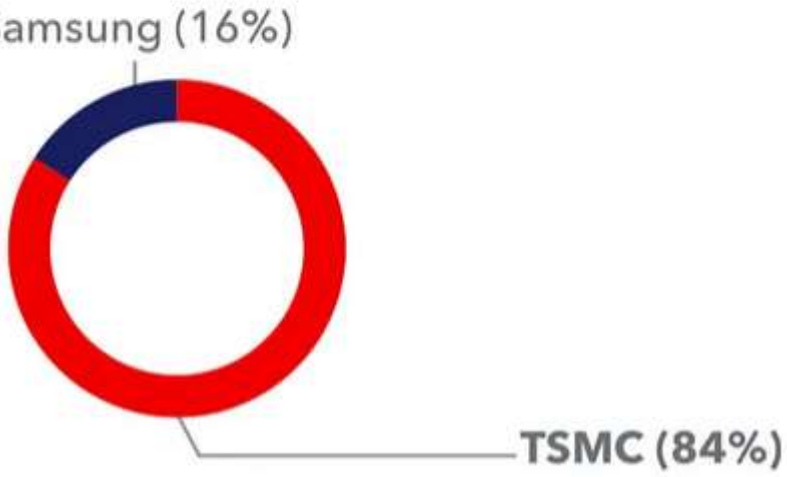
Market share in 2020

TSMC is dominant in the chip foundry market

Share of foundry market



Share of leading-edge market



Leading-edge refers to the smallest chips currently being mass-produced. As of 2021, 5nm chips are considered leading-edge. Anything older than 16nm is described as "trailing-edge". Trailing-edge chips are usually less expensive – and easier to make.

Sources: 'Revenue Ranking of the Global Top 10 Foundries, 3Q20,' TrendForce, BusinessKorea,'How TSMC has mastered the geopolitics of chipmaking,' The Economist.

1. Introduction (16)

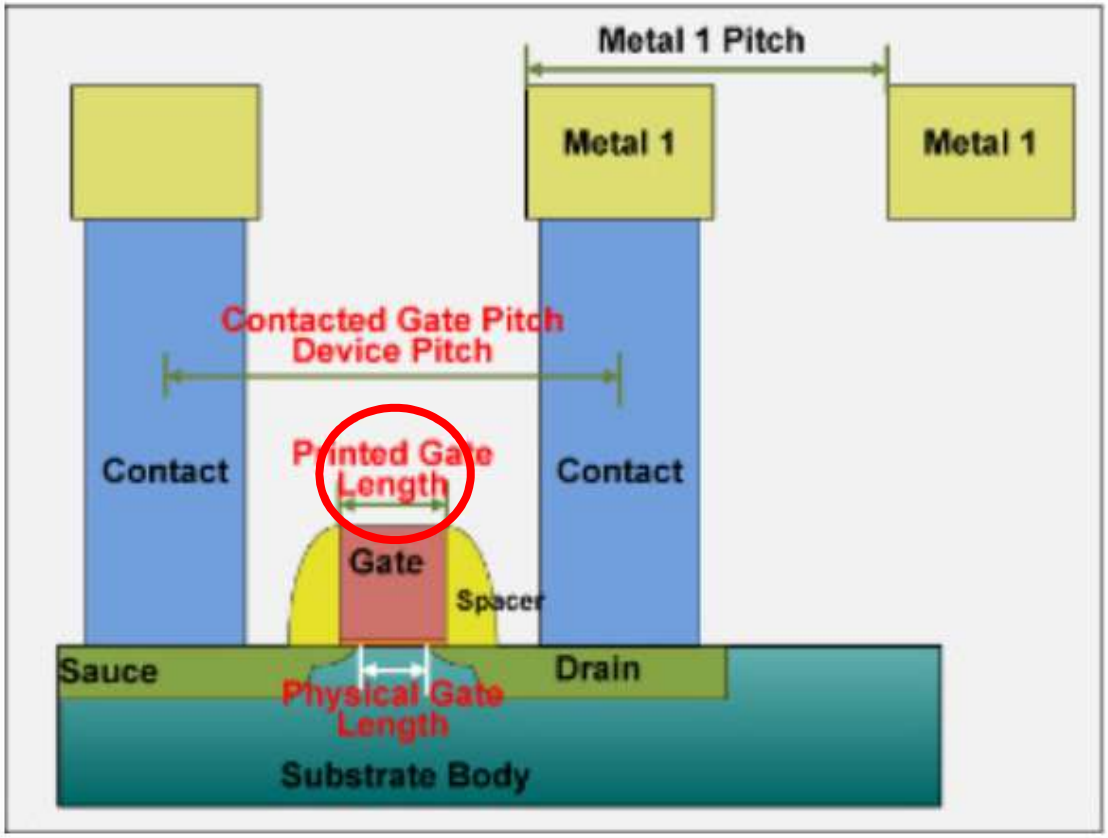
Characterizing process technology

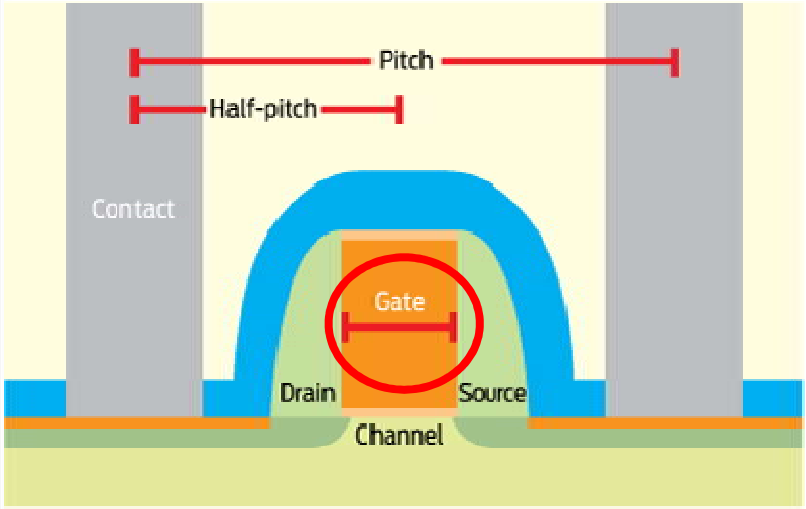
Traditionally, IC process technologies are characterized by the minimum feature size.

Interpretation of the minimum feature size for MOS transistors:

It is the minimum length of the MOS transistor channel between the drain and the source.

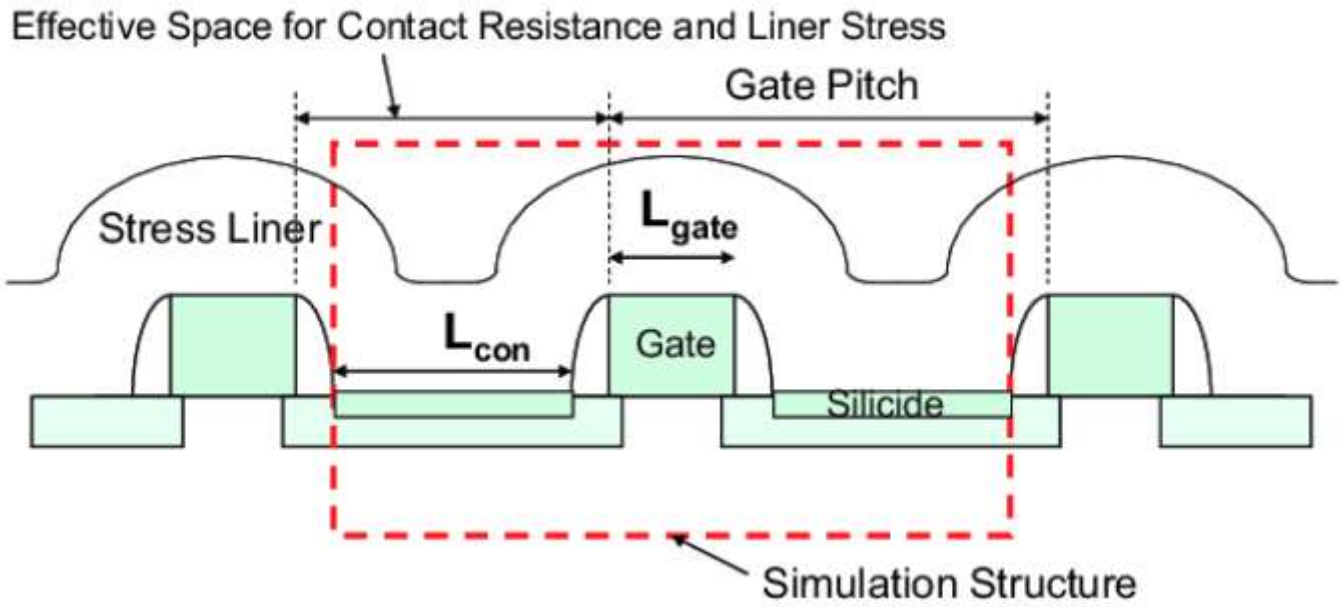
Accordingly, the minimum feature size was interpreted traditionally as the gate length, as indicated below:





Future plans

Process	Gate pitch	Metal pitch	Year
7 nm	60 nm	40 nm	2018
5 nm	51 nm	30 nm	2020
3 nm	48 nm	24 nm	2022
2 nm	45 nm	20 nm	2025
1 nm	42 nm	16 nm	2027



1. Introduction (17)

Recent interpretation of the minimum feature size

Recently, the minimum feature size is interpreted as the technology node.

It identifies the process technology of a given IC foundry (e.g. to be 22 nm or 14 nm node).

Then, process parameters cannot be simple derived from the feature size as before, instead, select parameters relating to the same technology node can differ significantly, e.g. by 20 %, from each other for the same process implemented by different vendors, as seen in the Table below.

Minimum Feature Size

	Intel 22 nm	Intel 14 nm	TSMC 16 nm	Samsung 14 nm
Transistor Fin Pitch	60 nm	42 nm	48 nm	48 nm
Transistor Gate Pitch	90 nm	70 nm	90 nm	84 nm
Interconnect Pitch	80 nm	52 nm	64 nm	64 nm
SRAM Cell Area	.1080 um^2	.0588 um^2	.0700 um^2	.0645 um^2

Table: MOS transistor parameters of different foundries belonging to 14 to 22 nm nodes [5]

1. Introduction (18)

Shortening the minimum feature size in the course of the evolution of IC technology

For process technologies (rougly below 300 nm) the gate length became shorter than the minimum feature size (node), as shown below for Intel's MOS processes.

Gate length
Minimum feature size

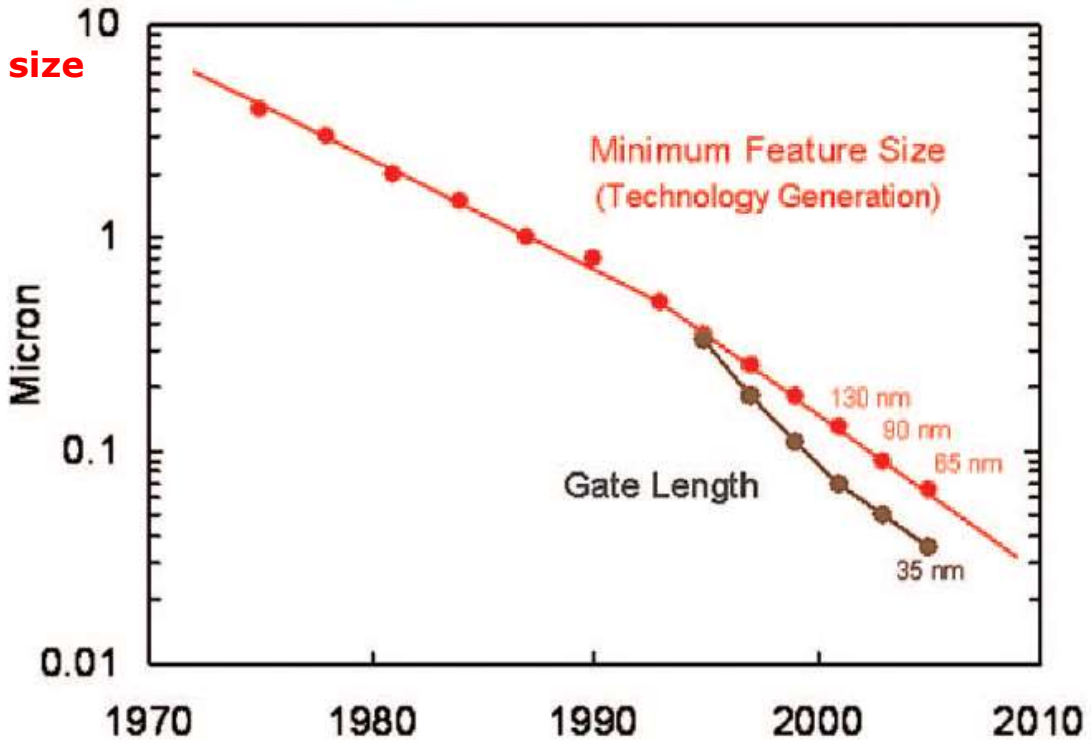
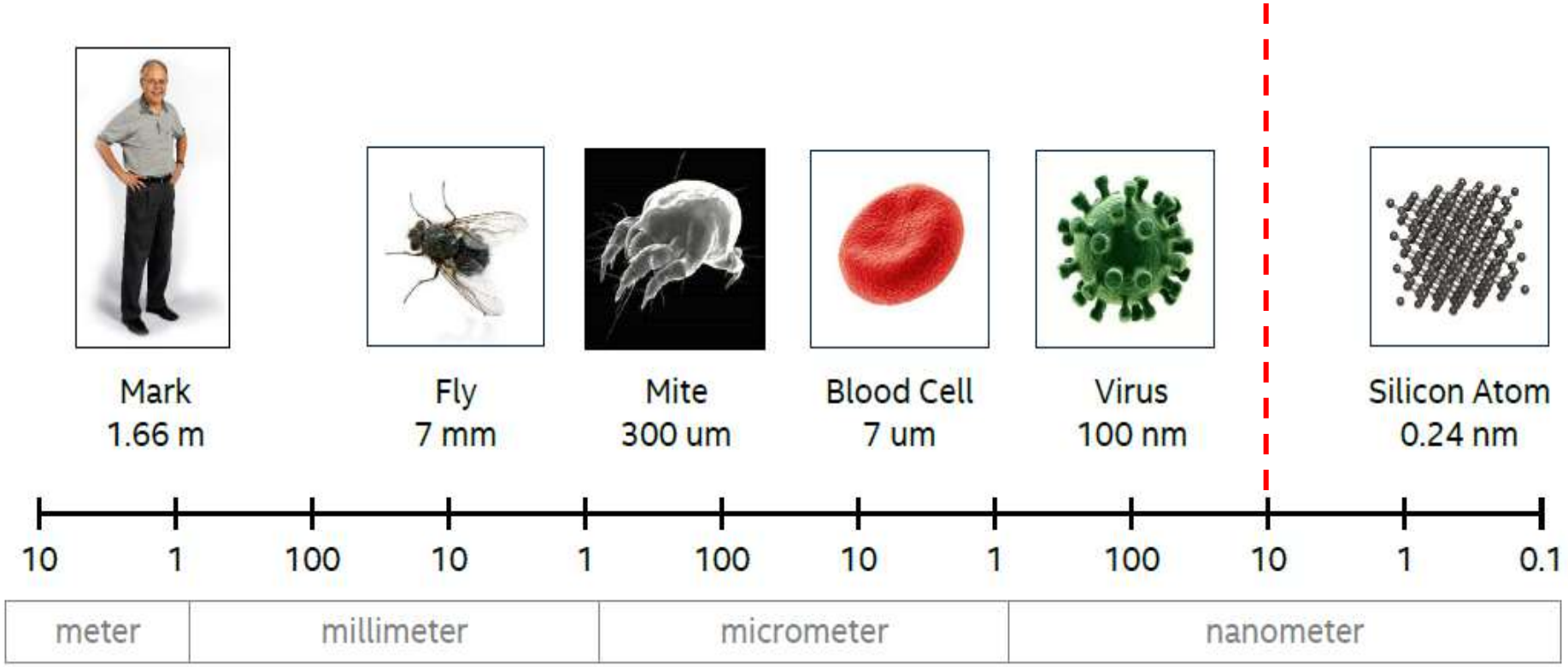


Figure: Gate length in Intel's subsequent MOS technologies [11]

As an example, in Intel's 65 nm technology the gate length amounts only to 35 nm.

Illustrating a feature size of 10 nm [12]



2. Moore’s law (5)

Intel's first 1 Kbit dynamic DRAM chip, the 1103 (Oct. 1970)

Main features:

1 Kx1-bit structure, pMOS technology, 3T (three-transistors per bit) design, two power supplies (+16 V/+19 V), non-multiplexed addressing, 18-pin package.

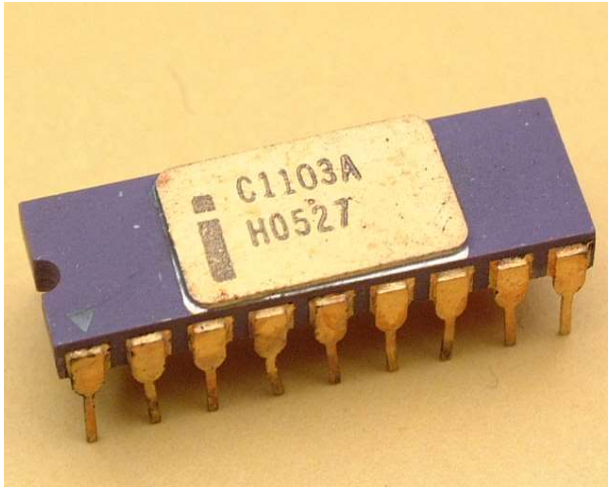


Figure: Intel’s 1103 [17]

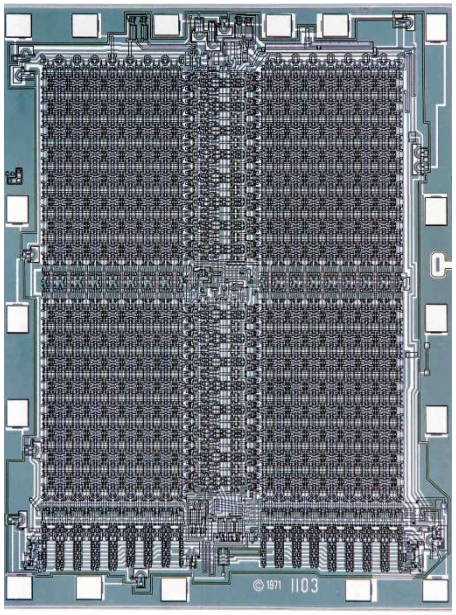


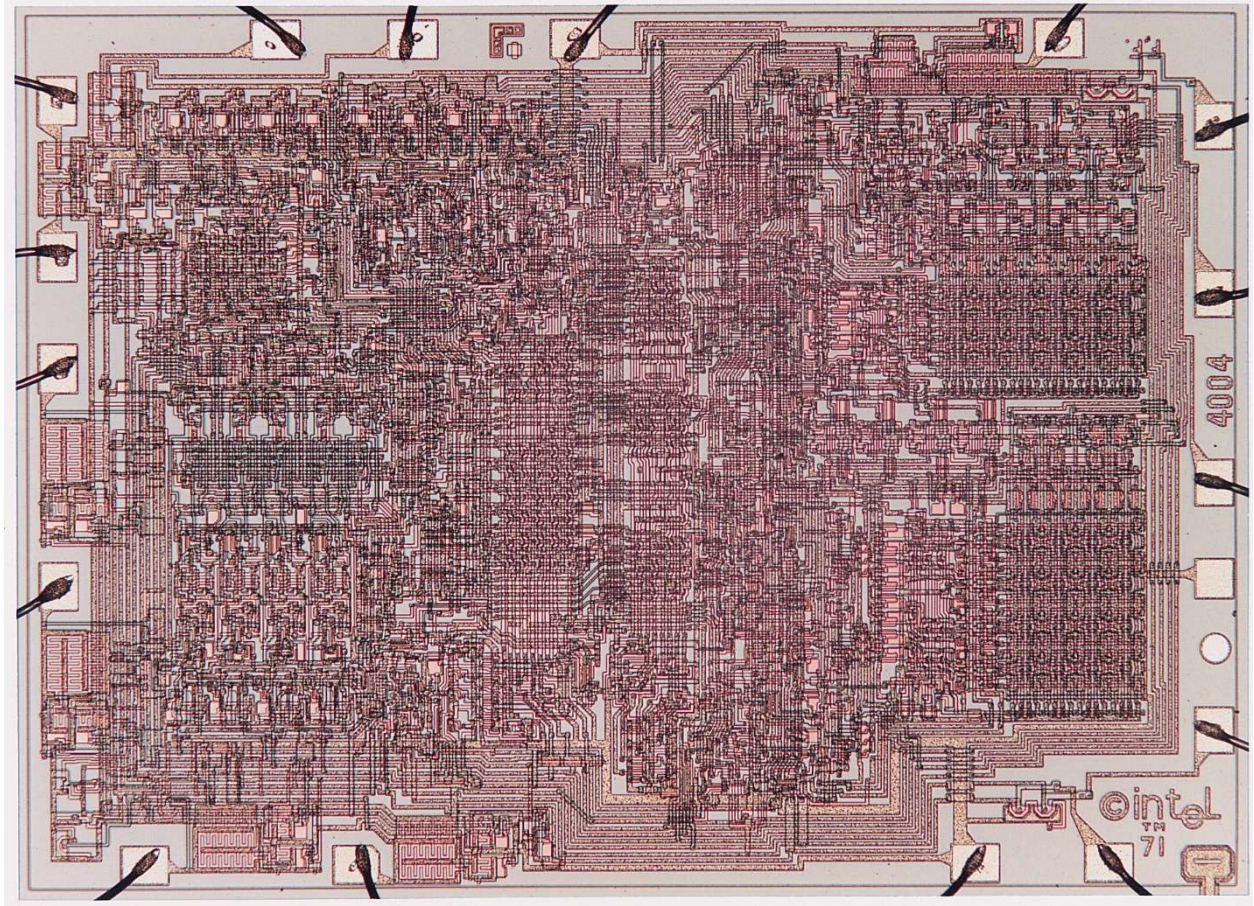
Figure: Die photo of Intel’s 1103 [18]

2. Moore’s law (6)

Intel's first microprocessor, the 4004 [16]

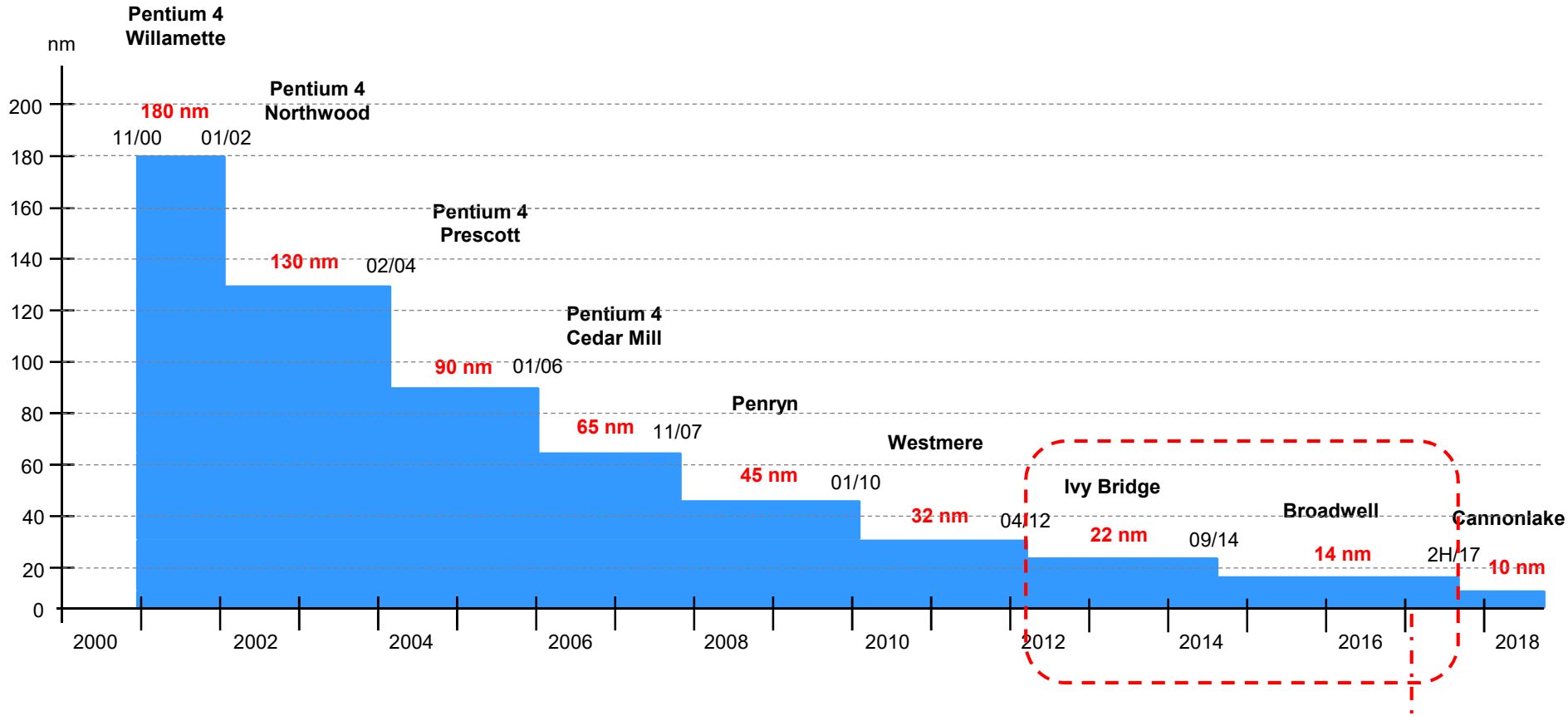
2300
transistors

Introduced:
11/1971



2. Moore's law (12)

Lengthening the cadence of Intel's technology transitions [36]



On Intel's Q2 2015 earnings conference call, on July 16 2015, Krzanich: in the second half of 2017, we expect to launch our first 10-nanometer product, code named Cannonlake.

The last two technology transitions have signaled that our cadence today is closer to 2.5 years than two" [37].

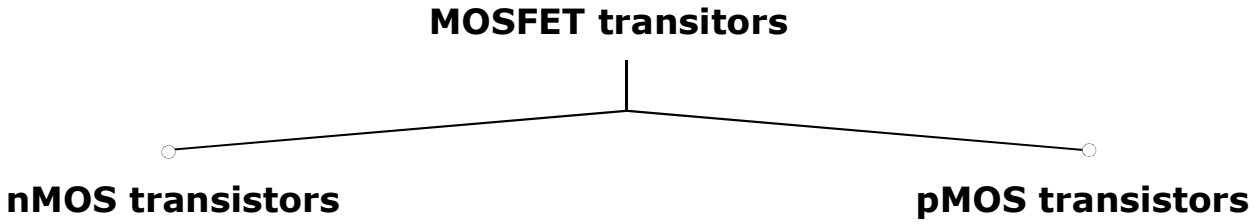
3. Brief introduction to MOSFET transistors

3. Brief introduction to MOSFET transistors (1)

3. Brief introduction to MOSFET transistors

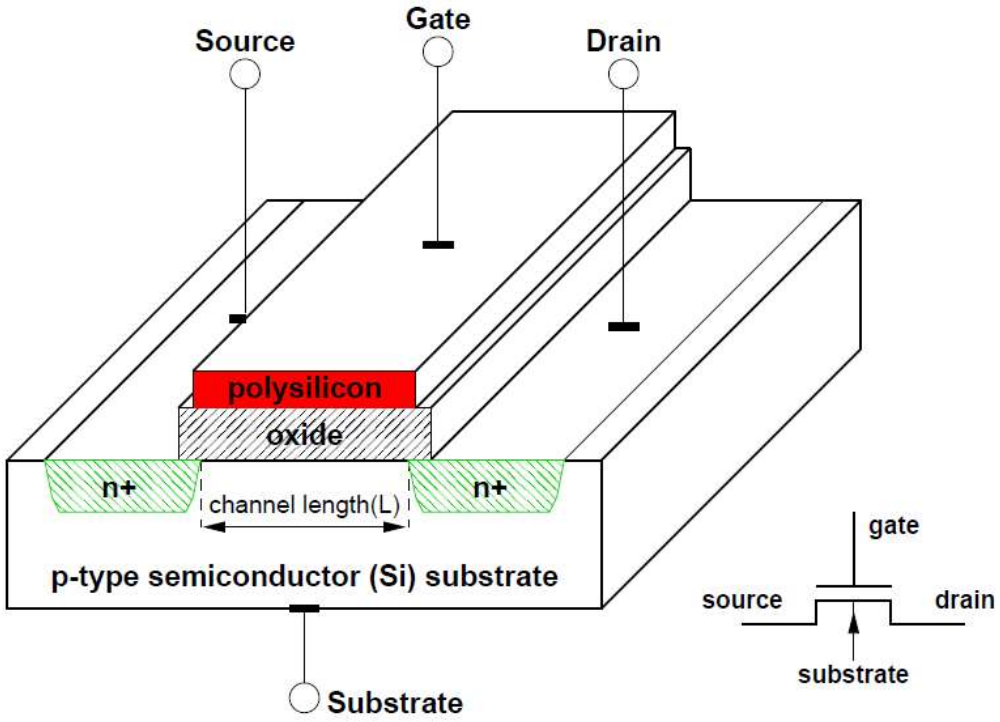
- MOSFET: Metal-OXid-Semiconductor Field-Effect Transistor
- MOSFET is often abreviated as MOS.
- For simplicity, we consider only enhancement mode MOS transistors, as these devices are the most common building elements of microprocessors.

Enhancement mode MOS transistors are off when the gate-source voltage is zero and will be turned on for appropriate positive values of the gate-source input voltage.



3. Brief introduction to MOSFET transistors (2)

Internal structure of the nMOS (nMOSFET) transistor [19]



- The Source and the Drain are implemented as two highly (n+) doped diffusion regions.
- Dpoing (e.g. by arsenid) aims at providing additional free electrons.
- The area in-between forms a channel with controllable conductivity.
- The Gate is built from a conductor, typically polysilicon, and is insulated from the Source-Channel-drain structure by a layer of silicon dioxide (SiO2).
- The voltage between the gate and the substrate induces an electric field which controls the flow of electrons in the channel.

  This gives rise to the name: Field-Effect Transistor (FET).

3. Brief introduction to MOSFET transistors (8)

Remark: Physical background of the operation of the enhancement mode nMOS transistor [19] -1

a) Switched off state

a1) Switched off stated due to VGS < VT (VDS is irrelevant and can be 0)

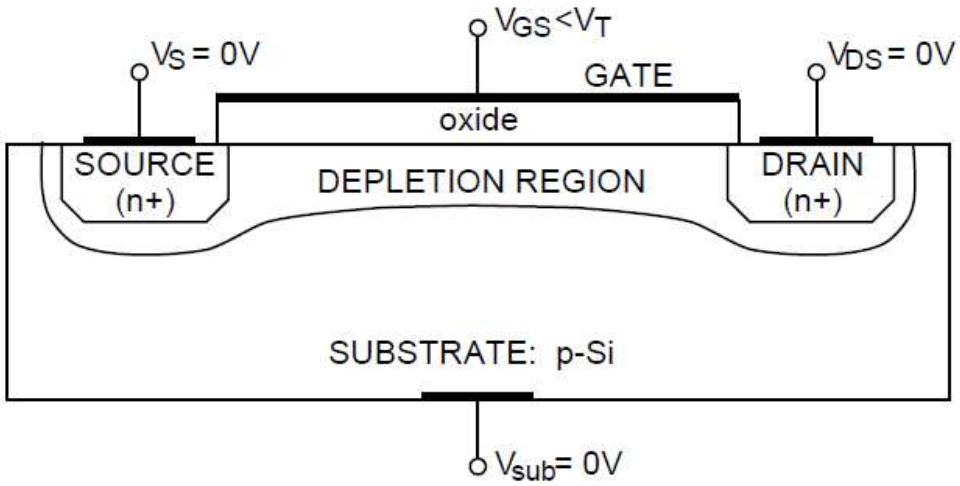


Figure: Formation of a depletion region in an enhancement-mode nMOS FET [19].

- The electric field induced by the gate voltage points down from the gate through the channel.
- This fields repels the majority carriers (that is positive holes) of the p-type substrate, from the channel hence forming a region depleted of carriers as shown in the Figure above.
- As a result, due to the lack of free carriers, no current will flow between the source and the drain in this case, that is, ID = 0.
- The threshold voltage VT depends on the actual fabrication technology and usually is about 0.5V.

4. Evolution of transistor technology

- 4.1 Overview
- 4.2 The scaling law of MOSFET technology
- 4.3 Strained Si technology
- 4.4 The HKMG transistor
- 4.5 FinFET transisitors

4.1 Overview of the evolution of transistor technology

4.1 Overview of the evolution of transistor technology (1)

4.1 Overview of the evolution of transistor technology

Historical data on scaling down IC tecnology [23]

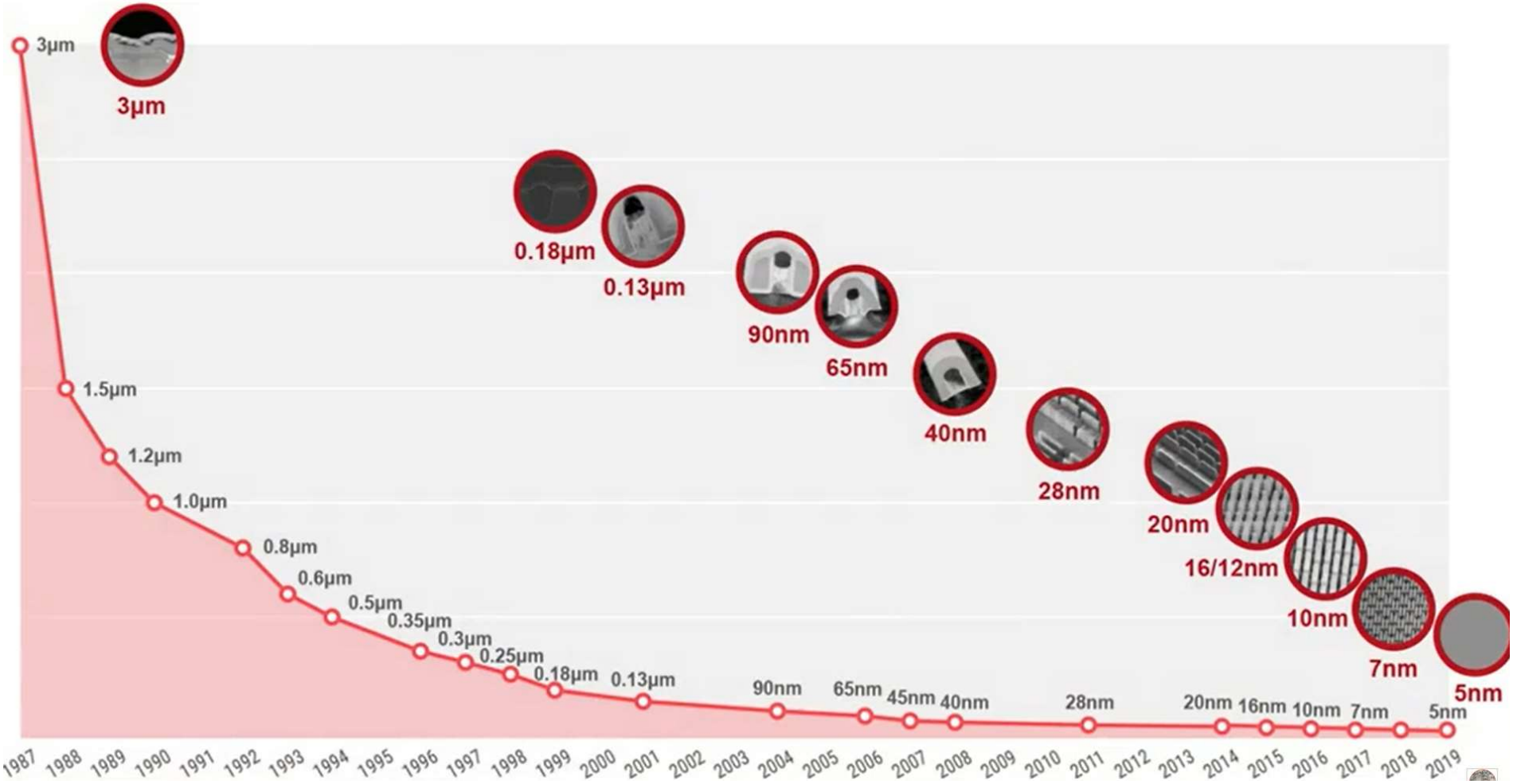
10 µm	1971
6 µm	1974
3 µm	1977
1.5 µm	1982
1 µm	1985
800 nm	1989
600 nm	1994
350 nm	1995
250 nm	1997
180 nm	1999
130 nm	2001
90 nm	2004
65 nm	2006
45 nm	2008
32 nm	2010
22 nm	2012
14 nm	2014
10 nm	*2017*
7 nm	*2019*

Remark

Until recently typically Intel lead the way for scaling down feature sizes.

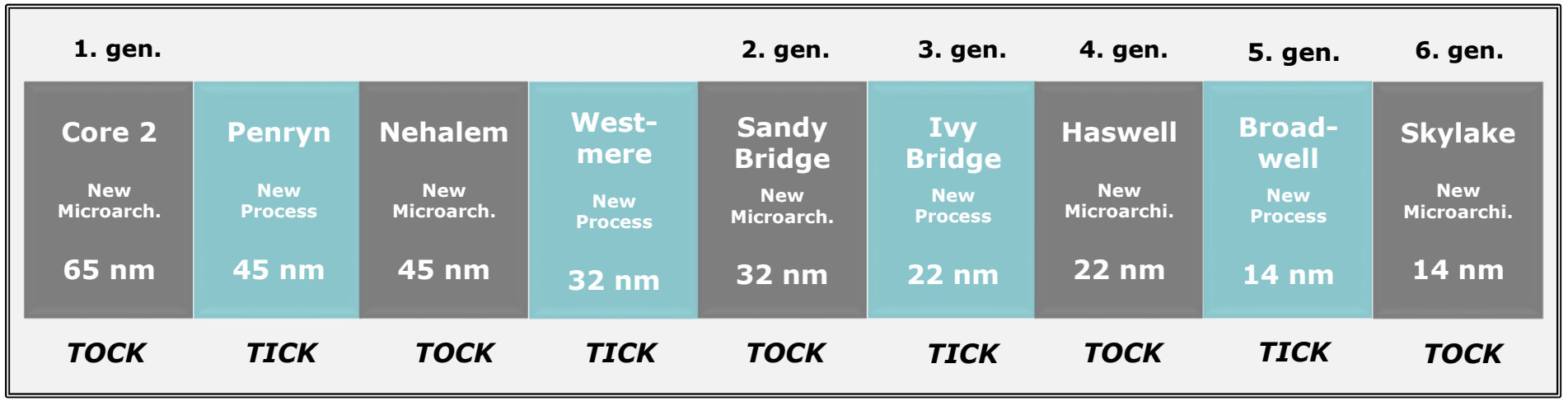
4.1 Overview of the evolution of transistor technology

Gate length roadmap:



4.1 Overview of the evolution of transistor technology (2)

Overview of scaling down feature sizes in Intel's basic microarchitectures (Based on [24])



1/2008

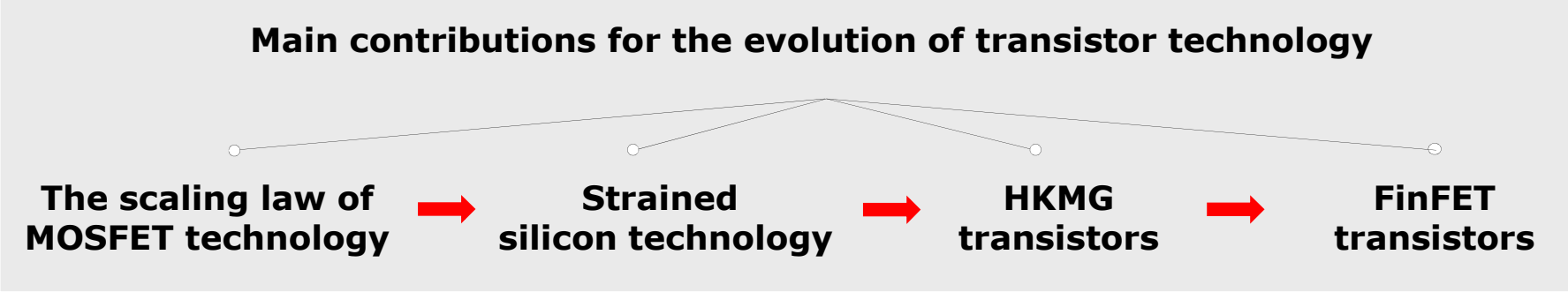
1/2010
Clarkdale

4/2012

9/2014

4.1 Overview of the evolution of transistor technology (3)

Main contributions for the evolution of transistor technology



Used by Intel at

130 nm and before	90/65 nm	45/32 nm	22 nm and below
Section 4.2	Section 4.3	Section 4.4	Section 4.5

Gate-all-around GAAFet transistors

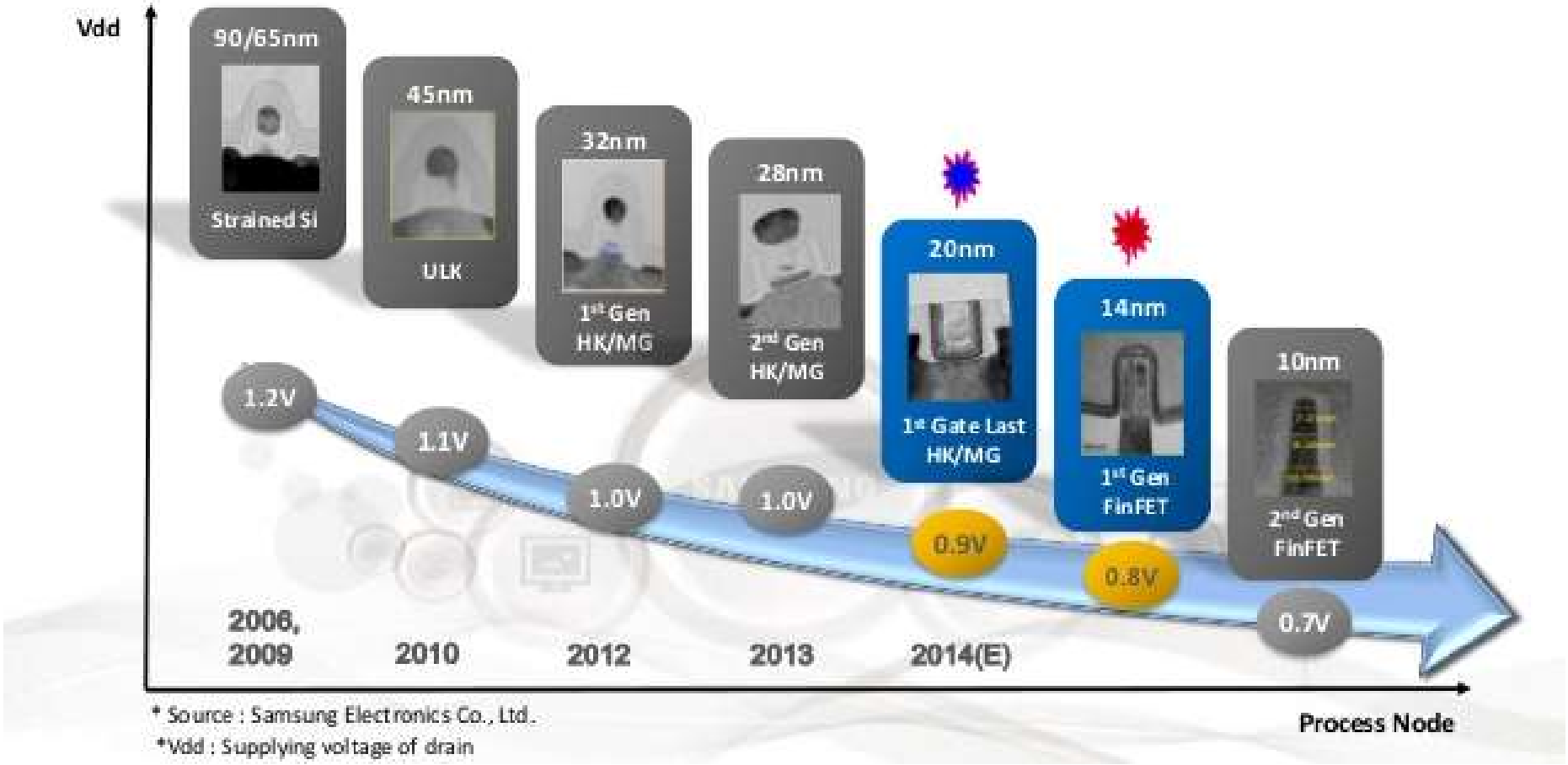
5 nm and below

Section 4.6

MOSFET: Metal Oxid Fied Effect Transistor: MOS Térvezérlésű Tranzisztor

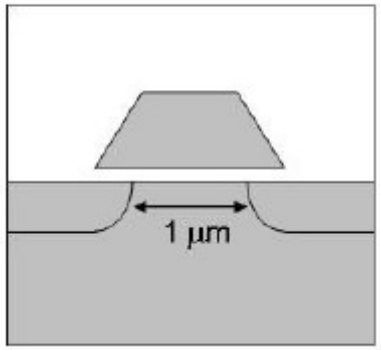
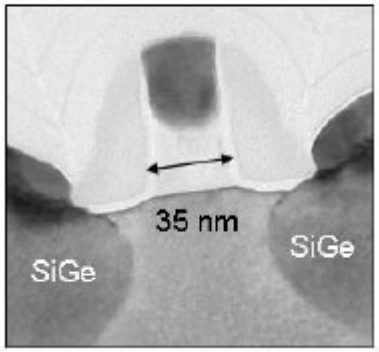
4.1 Overview of the evolution of transistor technology (4)

Decreasing the core voltage (and dissipation) in Samsung's subsequent IC processes [25]



4.2 The scaling law of MOSFET technology (3)

Contrasting scalied down transistor structures from the middle of 1970's to about 2005 [11]

	Transistor structure in the middle of the 1970's	**Intel's 65 nm transistor structure (2005)**
		
Physical Gate Length	>1.0 mm	35 nm
Electrical Channel Length	1.0 mm	<20 nm
Gate Oxide Thickness	35 nm	1.2 nm
Channel Doping	4x1016 cm-3	~1018 cm-3
Operating Voltage	4.0 V	1.2 V

4.3 Strained Si technology

4.3 Strained Si technology

Principle

By using appropriate IC technologies the Si lattice becomes strained, i.e. the distance betwen the Si atoms becomes wider, as indicated in the Figure below.

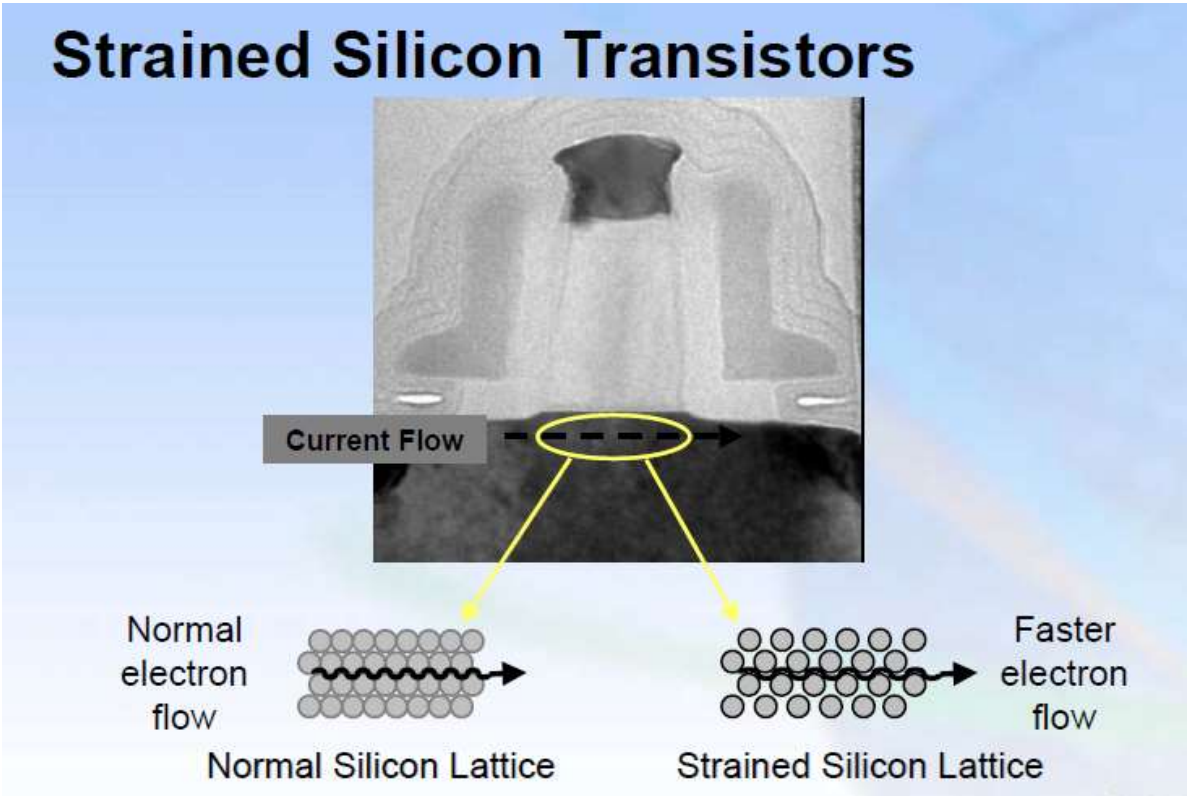


Figure: Principle of the strained Si technology [27]

4.3 Strained Si technology (2)

Benefits and drawbacks of the strained Si technology [27]

Benefits

- It increases electron and hole mobility.
- Greater mobility results in 10-20 % increase drive currents that raises performance.

Drawback

The strained Si process needs a few additional process steps that increase the total process cost by less than 2 %.

4.4 The HKMG transistor

4.4 The HKMG transistor

HKMG means High-k Metal Gate.

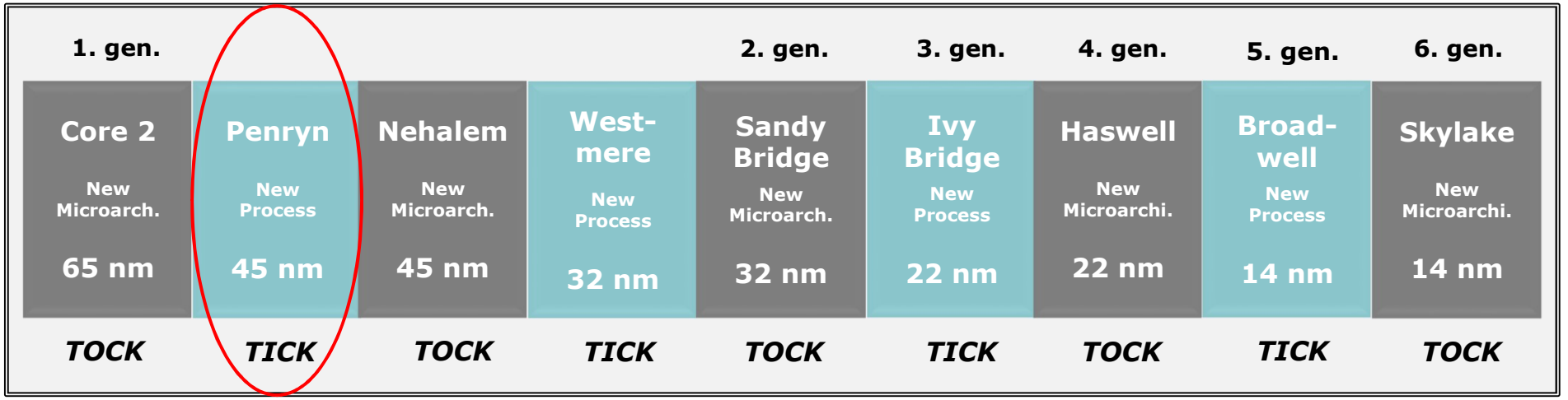


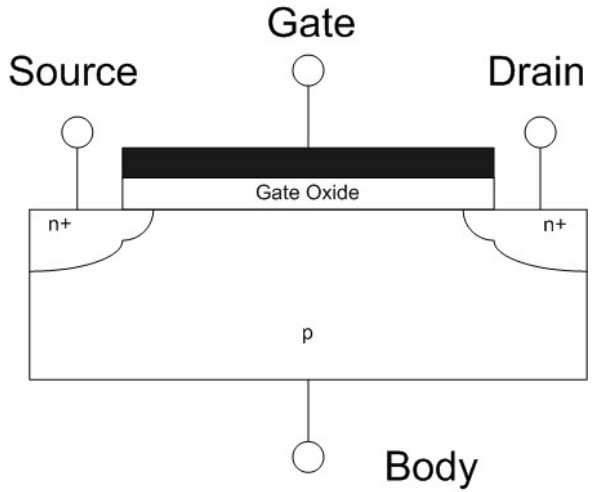
Figure: Intel's Tick-Tock development model (Based on [24])

HKMG transistors has been introduced by Intel along with the Penryn family of processors in 2007.

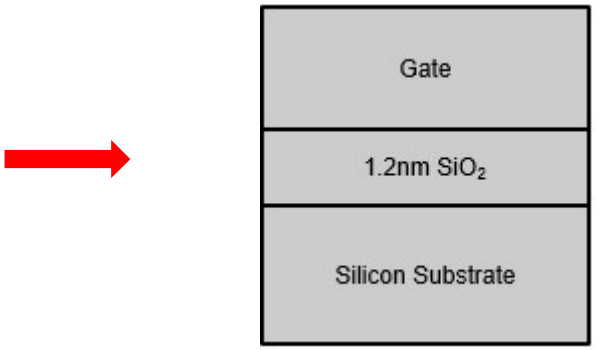
4.4 The HKMG transistor (2)

Limitation of MOSFET scaling in respect to the gate oxid (insulator) layer [28]

Layout of an nMOS transistor



Example iplementation of the gate oxid layer at 90 nm



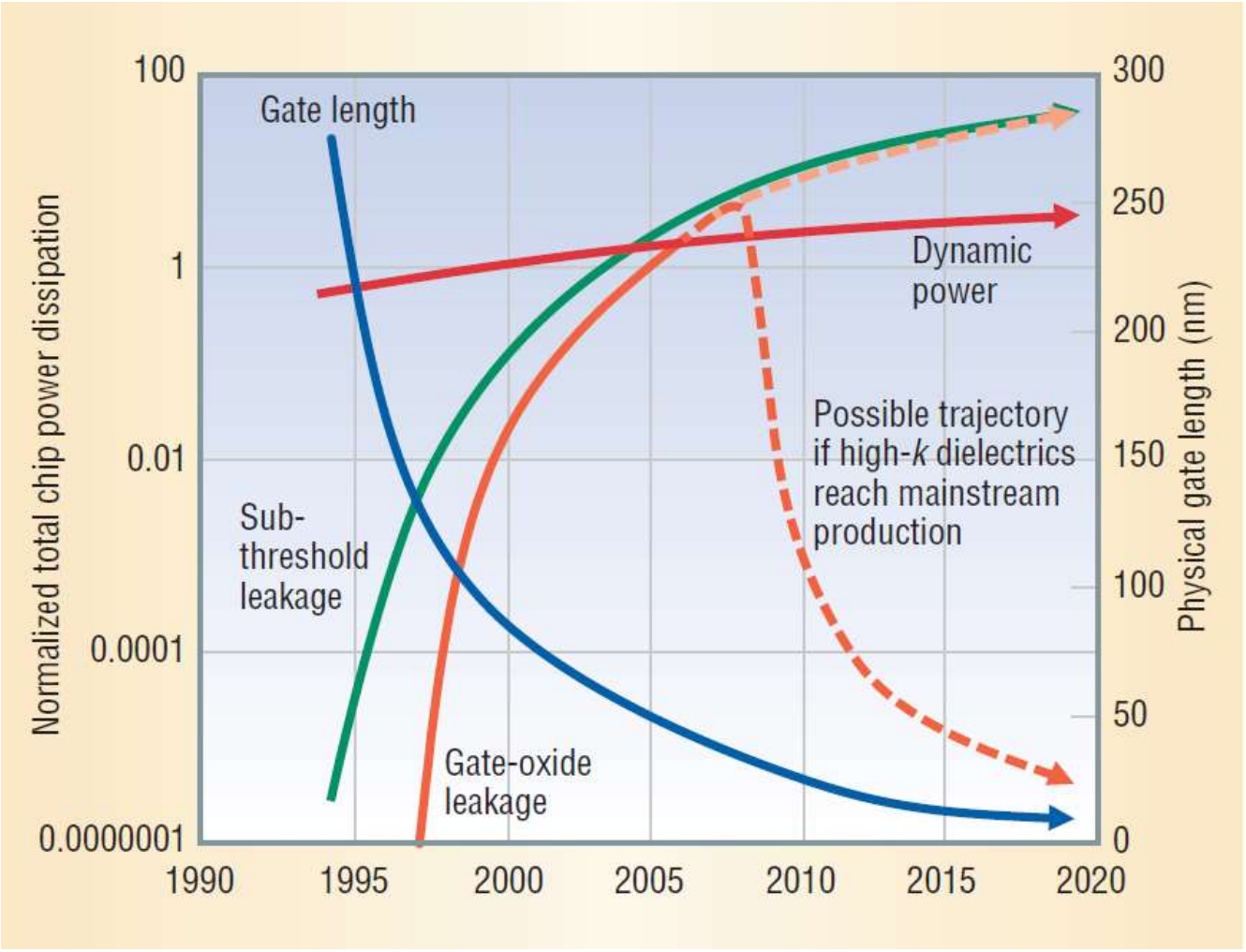
When transistor structures have been scaled down to about 90 or 65 nm the width of the SiO_2 layer became as short as about 1 nm.

However, the distance between SiO_2 molecules is about 0.24 nm so for example a 1.2 nm SiO_2 layer is only about 5-6 SiO_2 molecules wide [29].

As a consequence, while transistor structures were scaled down to the low feature sizes of 90 or 65 nm the leakage current rose drastically, as the next figure shows.

4.4 The HKMG transistor (3)

The need to introduce new transistor design [30]



Sub-threshold = Source-Drain

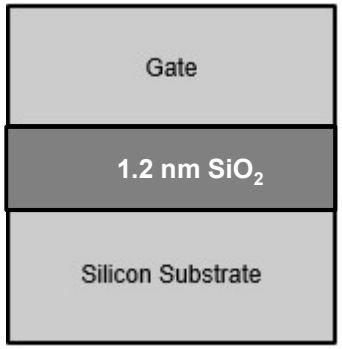
Figure 3.1.1: Dynamic and static power dissipation trends in chips [30]

4.4 The HKMG transistor (4)

Principle of the HKMG transistor [28]

The gate oxide layer in a MOSFET can be modeled as a parallel plate capacitor.
The capacitance *C* of this parallel plate capacitor is given by

$$C = \frac{\kappa \varepsilon_0 A}{t}$$

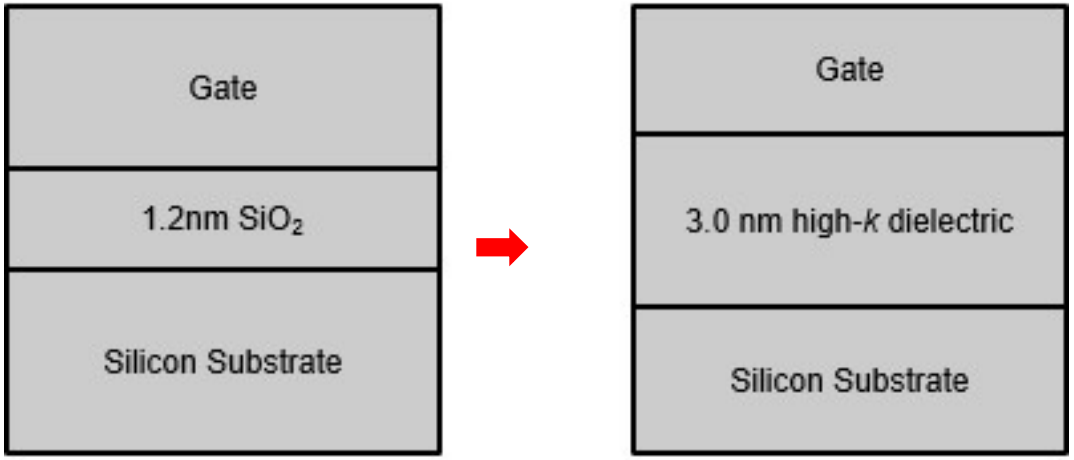


Where
A is the capacitor area
κ is the relative dielectric constant of the material (3.9 for SiO_2 and > 10 for a high k dielectric)
ε_0 is the permittivity of free space
t is the thickness of the capacitor oxide insulator

4.4 The HKMG transistor (5)

Principle of reducing the leakage current [28]

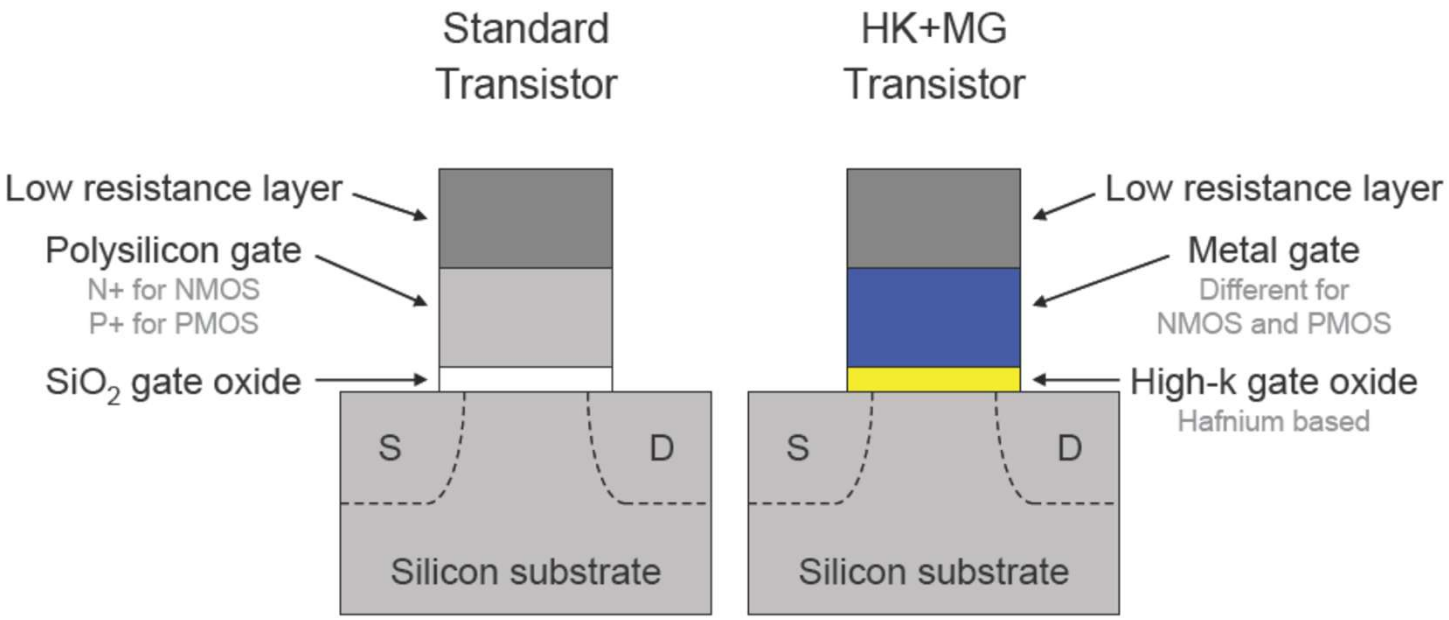
The thin SiO_2 insulator layer can be replaced by a wider high-k dielectric that provides the same or higher capacitance, as shown below.



The wider high-k insulator layer results in considerable less leakage current, as the Figure indicates.

4.4 The HKMG transistor (6)

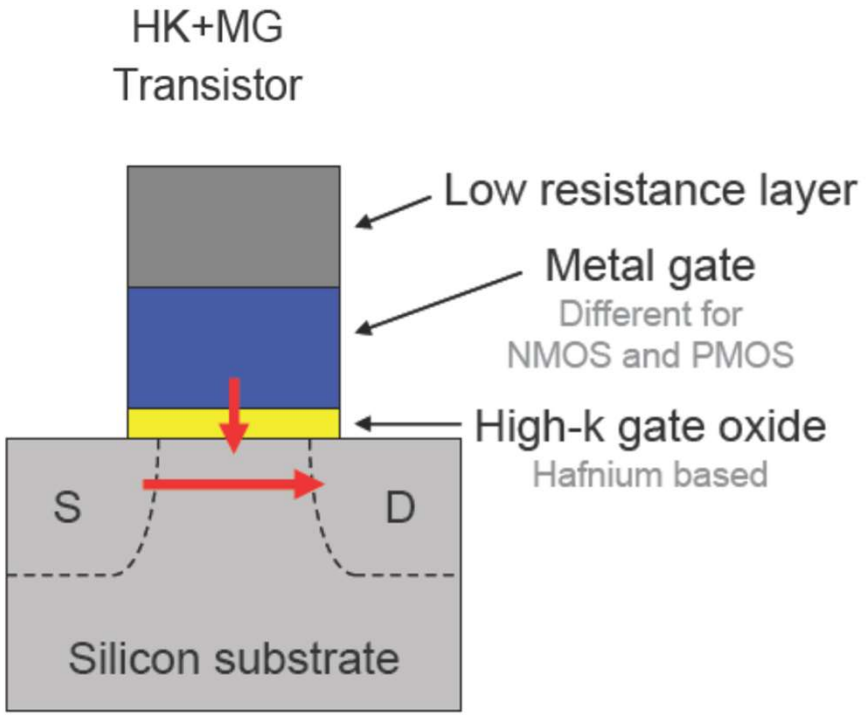
Structure of the HKMG (High-k + Metal Gate) transistor [31]



4.4 The HKMG transistor (7)

Benefits of HKMG transistors [31]

~30%	reduction in transistor switching power
>20%	improvement in transistor switching speed or
>5x	reduction in source-drain leakage power
>10x	reduction in gate oxide leakage power



4.5 FinFET transistors

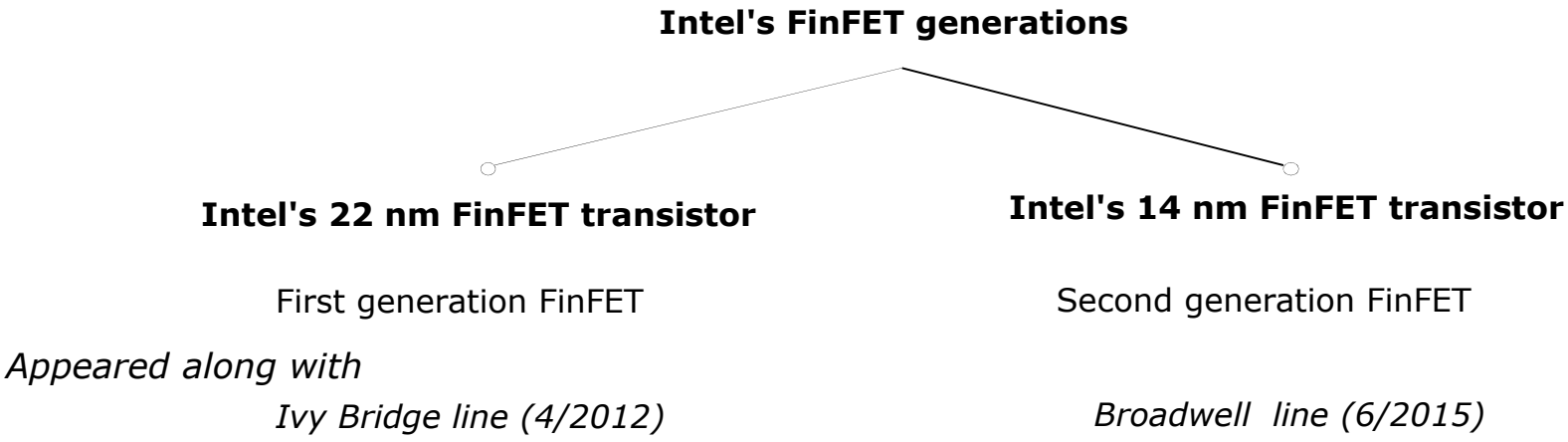
- 4.5.1 Introduction to the FinFET transistors
- 4.5.2 Intel's 22 nm FinFET transistor
- 4.5.3 Intel's 14 nm FinFET transistor

4.5.1 Introduction to the FinFET transistors

4.5.1 Introduction to the FinFET transistors (1)

4.5.1 Introduction to the FinFET transisitors

- The FinFET transistor is termed also as Tri-gate or 3D transistor.
- The term FinFET (Fin Field Effect Transistor) was coined in 1999 by researchers at the University of California, Berkley, nevertheless, first commercial implementations appiered only more than 10 years later in 2012 by Intel under the designation Tri-gate transistor.
- There is no consensus about how to designate MOS tranasistor structures using fins, a few firms like IBM, AMD or the foundries TSMC or GlobalFoundries make use of the term FinFET whereas Intel dubs such transistor structures as Tri-gate transistors.
- Until now Intel developed two generations of FinFET transistors.



4.5.2 Intel's 22 nm FinFET transistor

4.5.2 Intel's 22 nm FinFET transistor (1)

4.5.2 Intel's 22 nm FinFET transistor -1

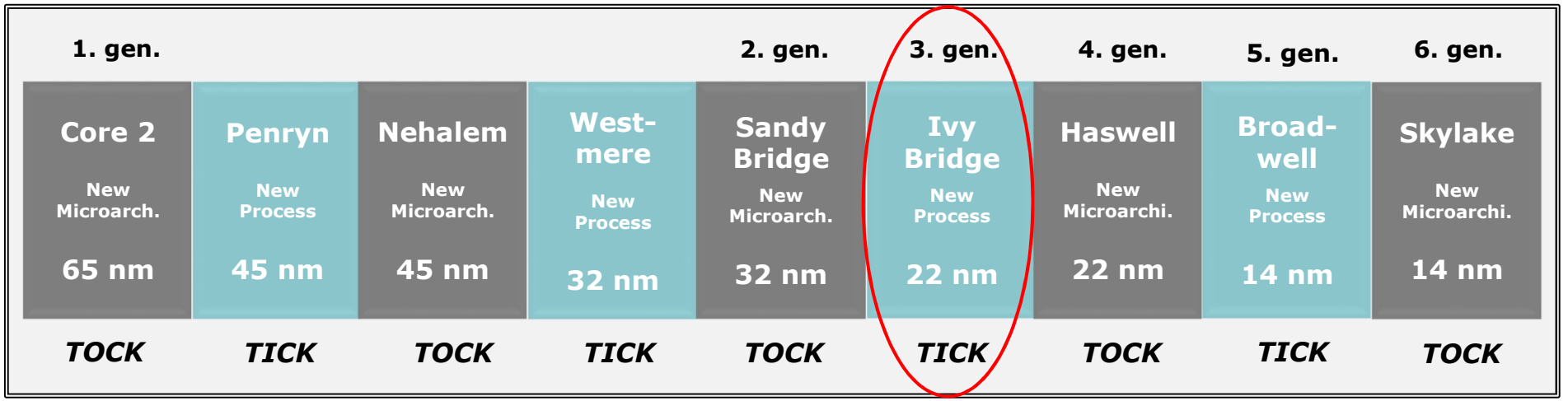
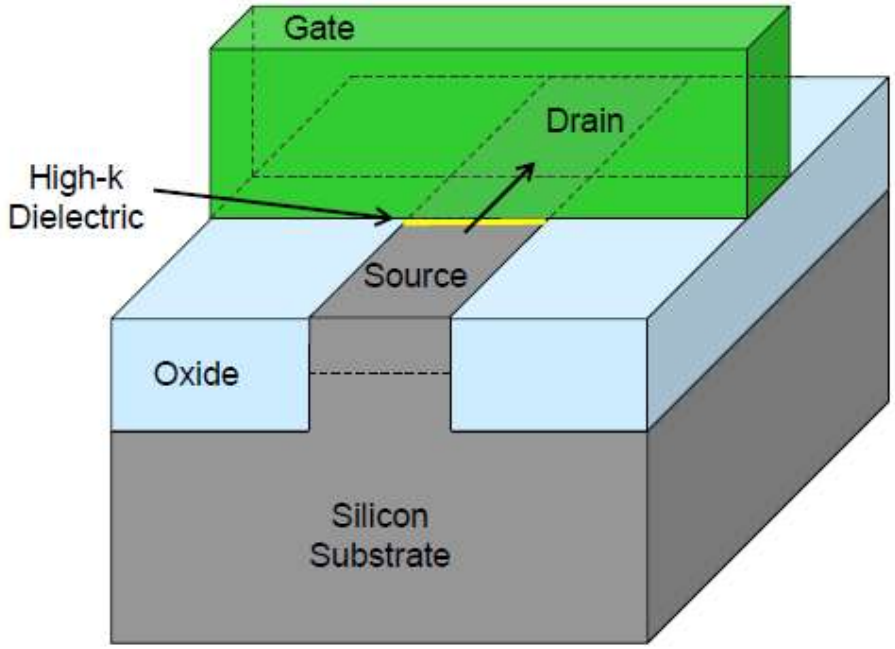


Figure: Intel's Tick-Tock development model (Based on [24])

Introduced along with the Ivy Bridge family of processors in 2012.

4.5.2 Intel's 22 nm FinFET transistor (2)

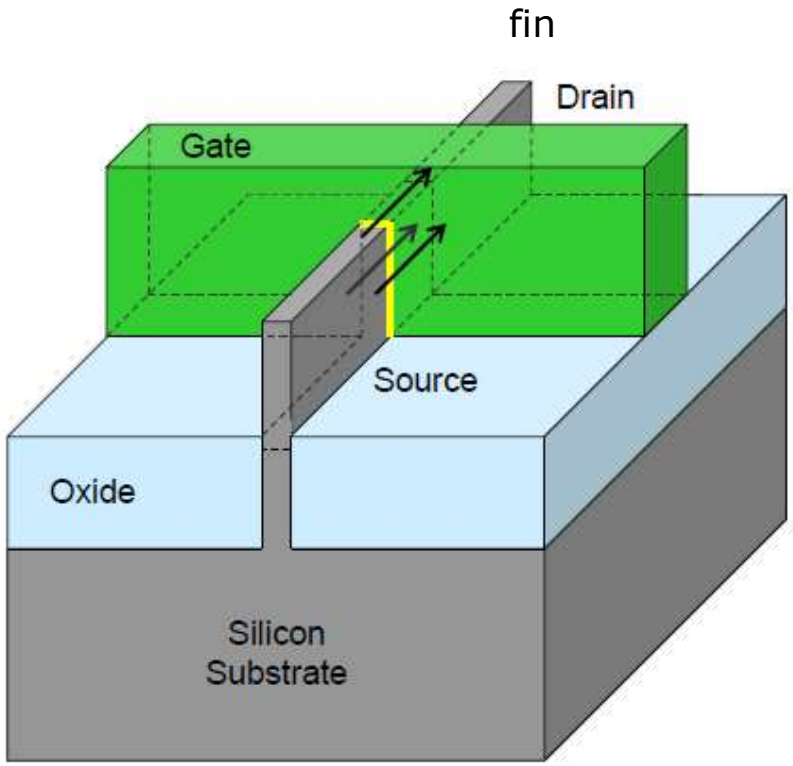
The traditional planar transistor [1]



Traditional 2-D planar transistors form a conducting channel in the silicon region under the gate electrode when in the "on" state

4.5.2 Intel's 22 nm FinFET transistor (3)

The 22 nm FinFET transistor -2 [1]



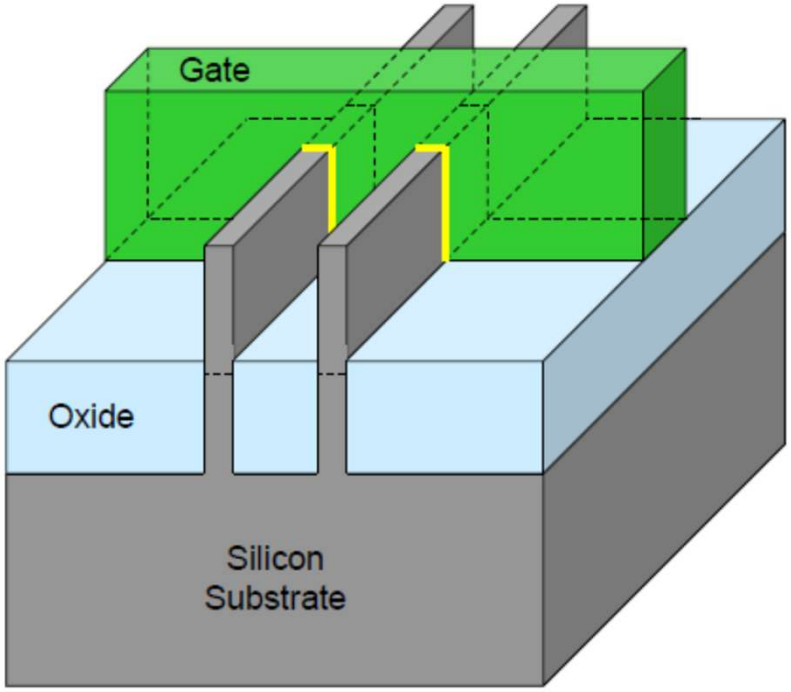
3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

Transistors have now entered the third dimension!

The designation "tri-gate" originates from the fact that now the gate has three sides.

4.5.2 Intel's 22 nm FinFET transistor (4)

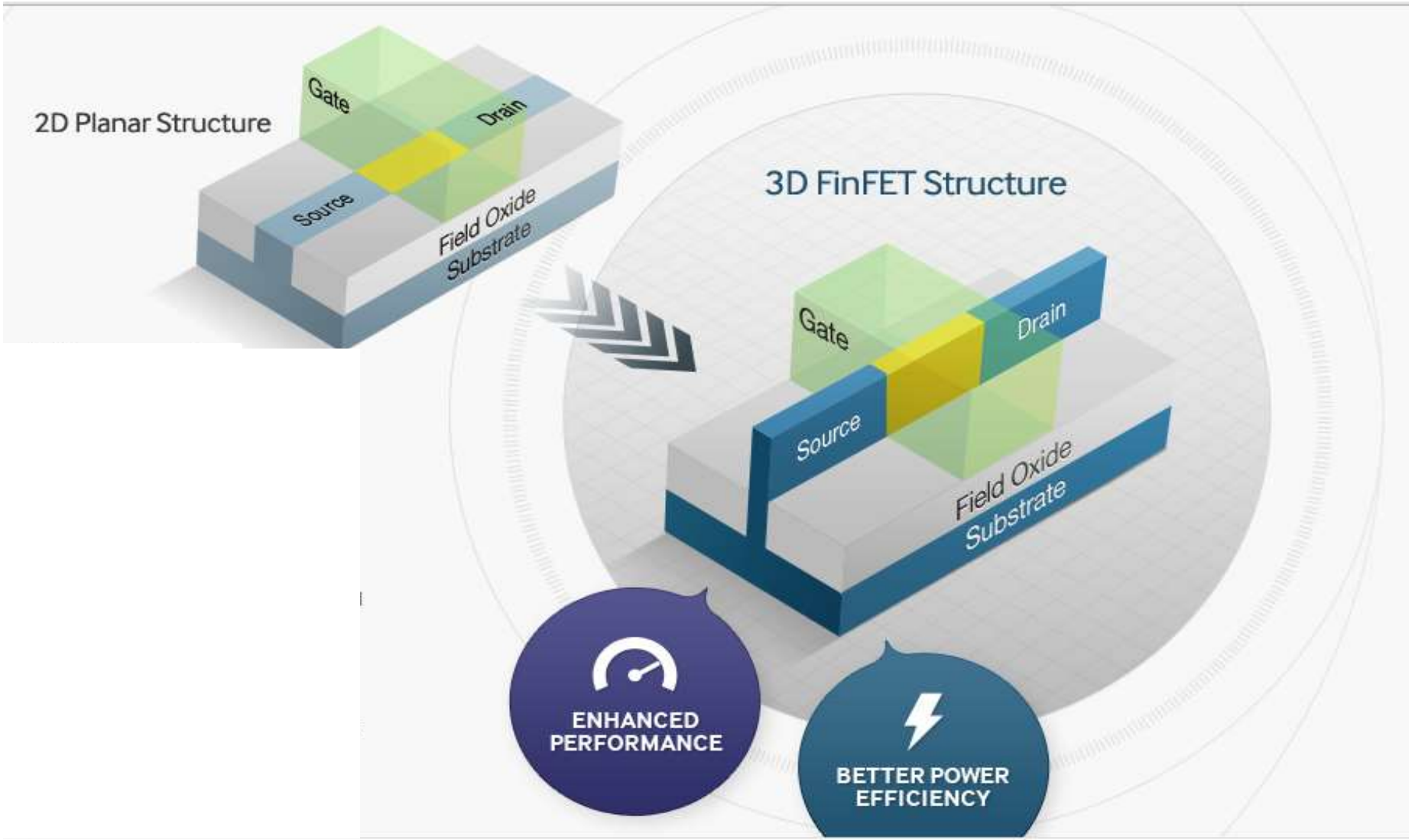
The 22 nm FinFET transistor -3 [1]



Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

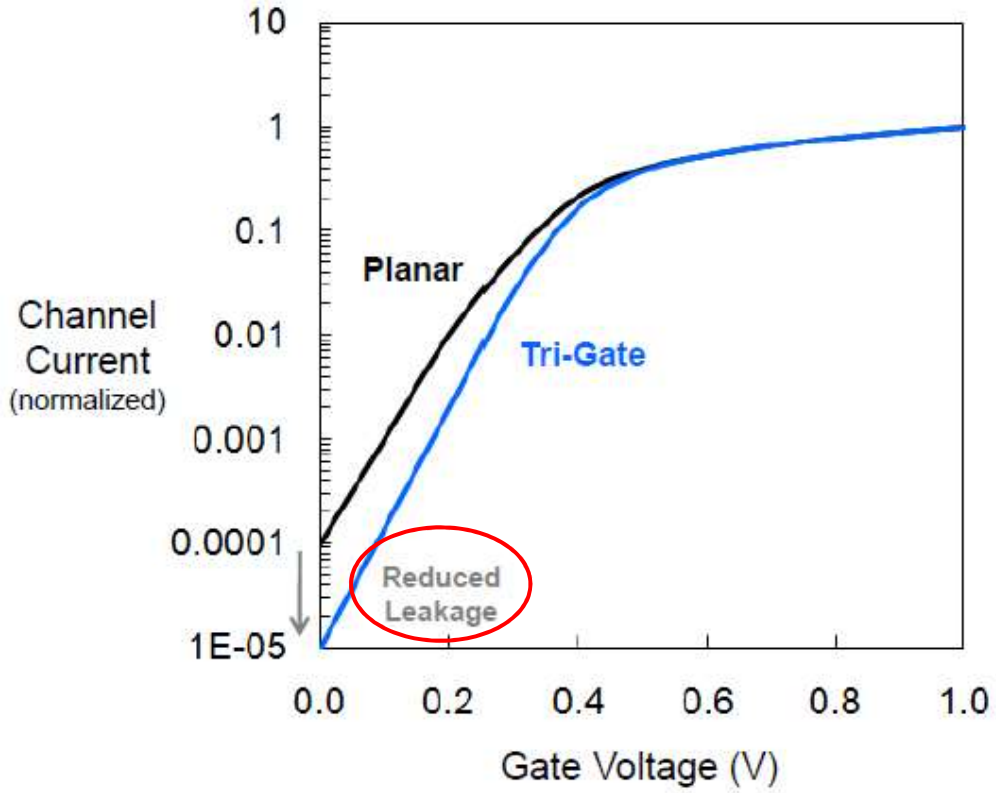
4.5.2 Intel's 22 nm FinFET transistor (5)

Contrasting 2D planar and 3D FinFET transistor structures [38]



4.5.2 Intel's 22 nm FinFET transistor (6)

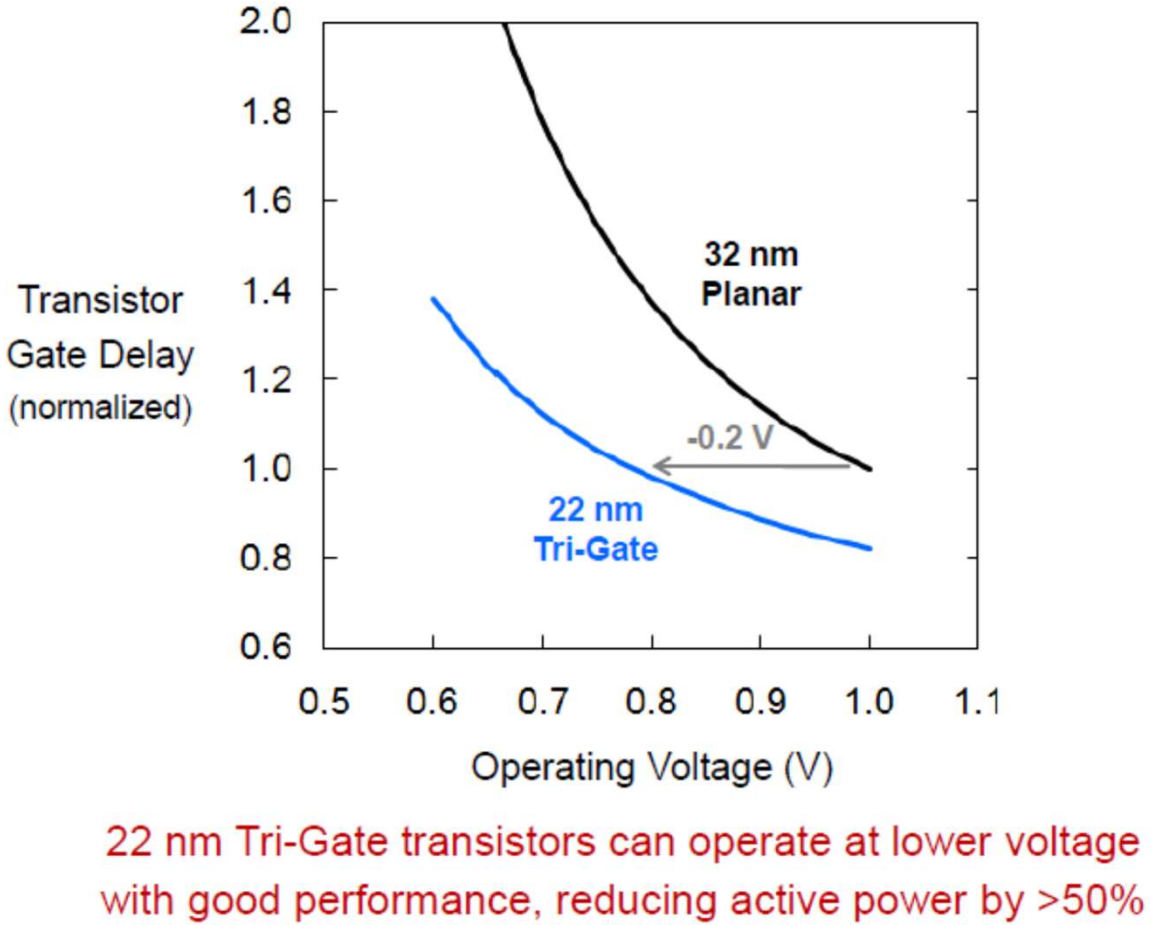
Switching characteristics of the traditional planar and FinFET transistors [1]



The "fully depleted" characteristics of Tri-Gate transistors provide a steeper sub-threshold slope that reduces leakage current

4.5.2 Intel's 22 nm FinFET transistor (7)

Gate delay of the traditional planar and FinFET transistors [1]



22 nm Tri-Gate transistors can operate at lower voltage with good performance, reducing active power by >50%

Gate delay: time difference between output signal and input signal of a gate (n x ps)

4.5.3 Intel's 14 nm FinFET transistor

4.5.3 Intel's 14 nm FinFET transistor (1)

4.5.3 Intel's 14 nm FinFET transistor-1

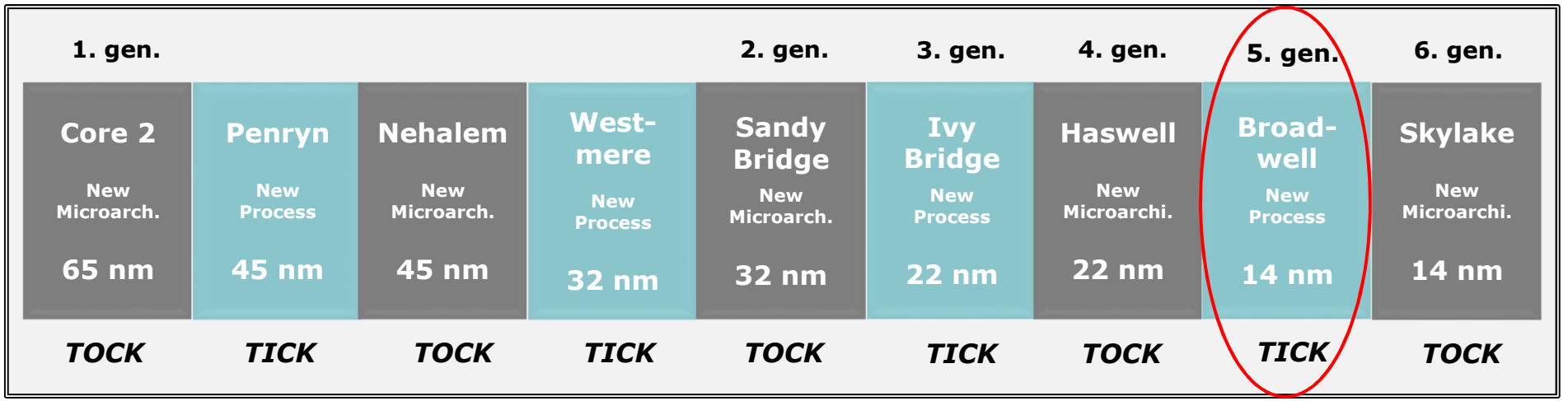
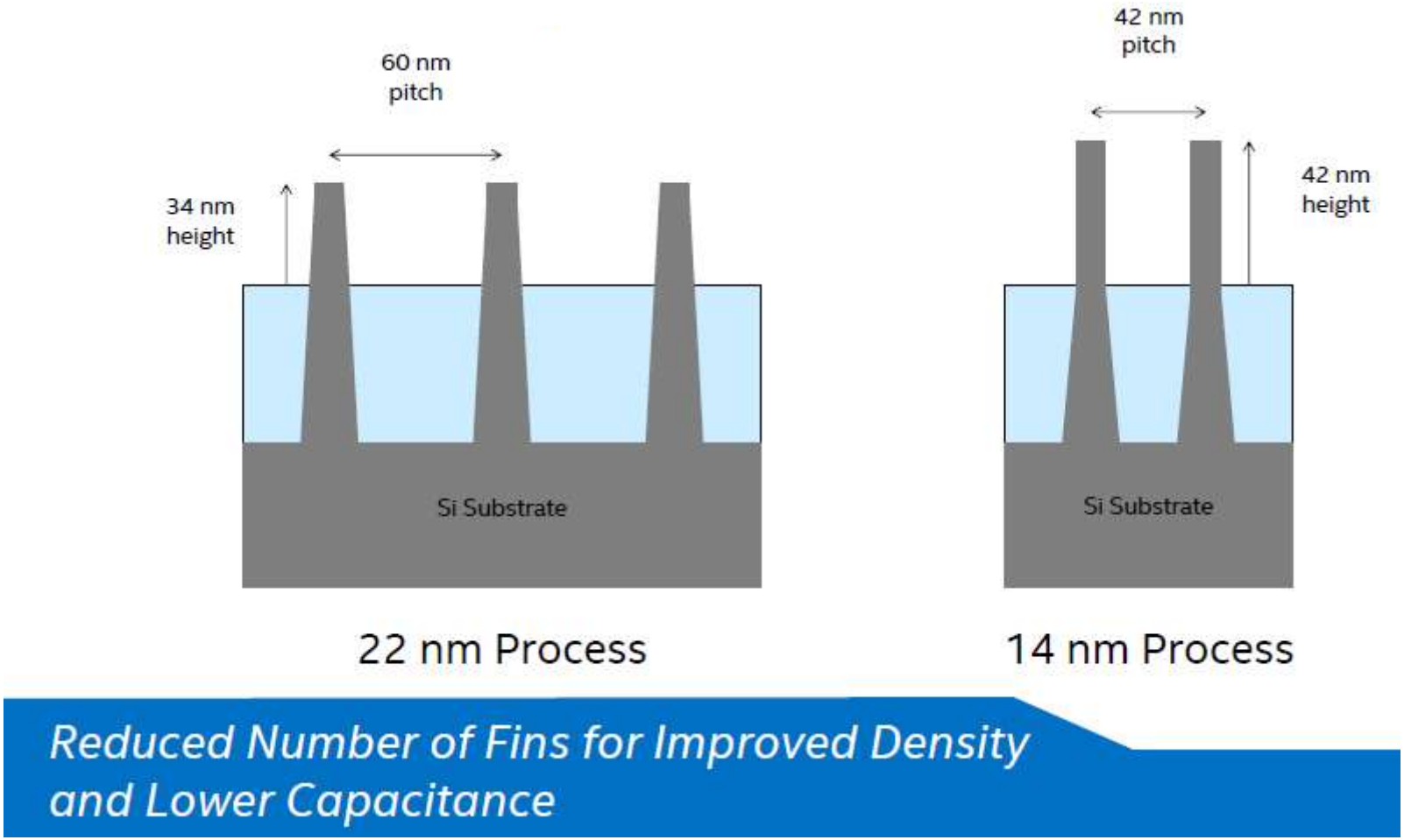


Figure: Intel's Tick-Tock development model (Based on [24])

Introduced along with the Broadwell family of processors in 2014

4.5.3 Intel's 14 nm FinFET transistor (2)

14 nm 2 generation FinFET transistors with fin improvement [12]



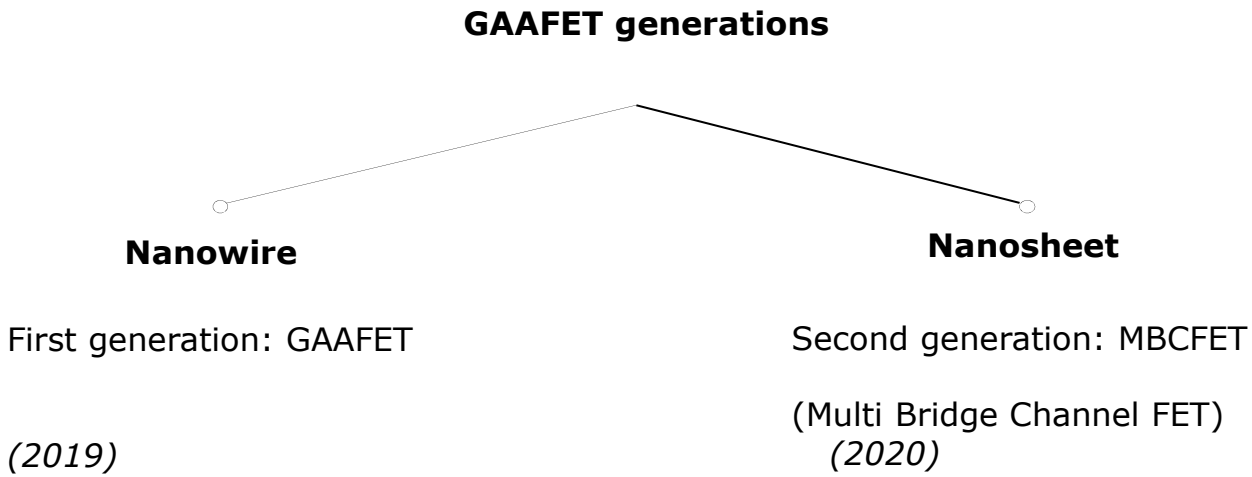
4.6 GAAFET transistor family

- 4.6.1 Introduction to the GAAFET transistors
- 4.6.2 Samsung's 3 nm GAAFET amd MCBFET transistor

4.6.1 Introduction to the GAAFET transistors

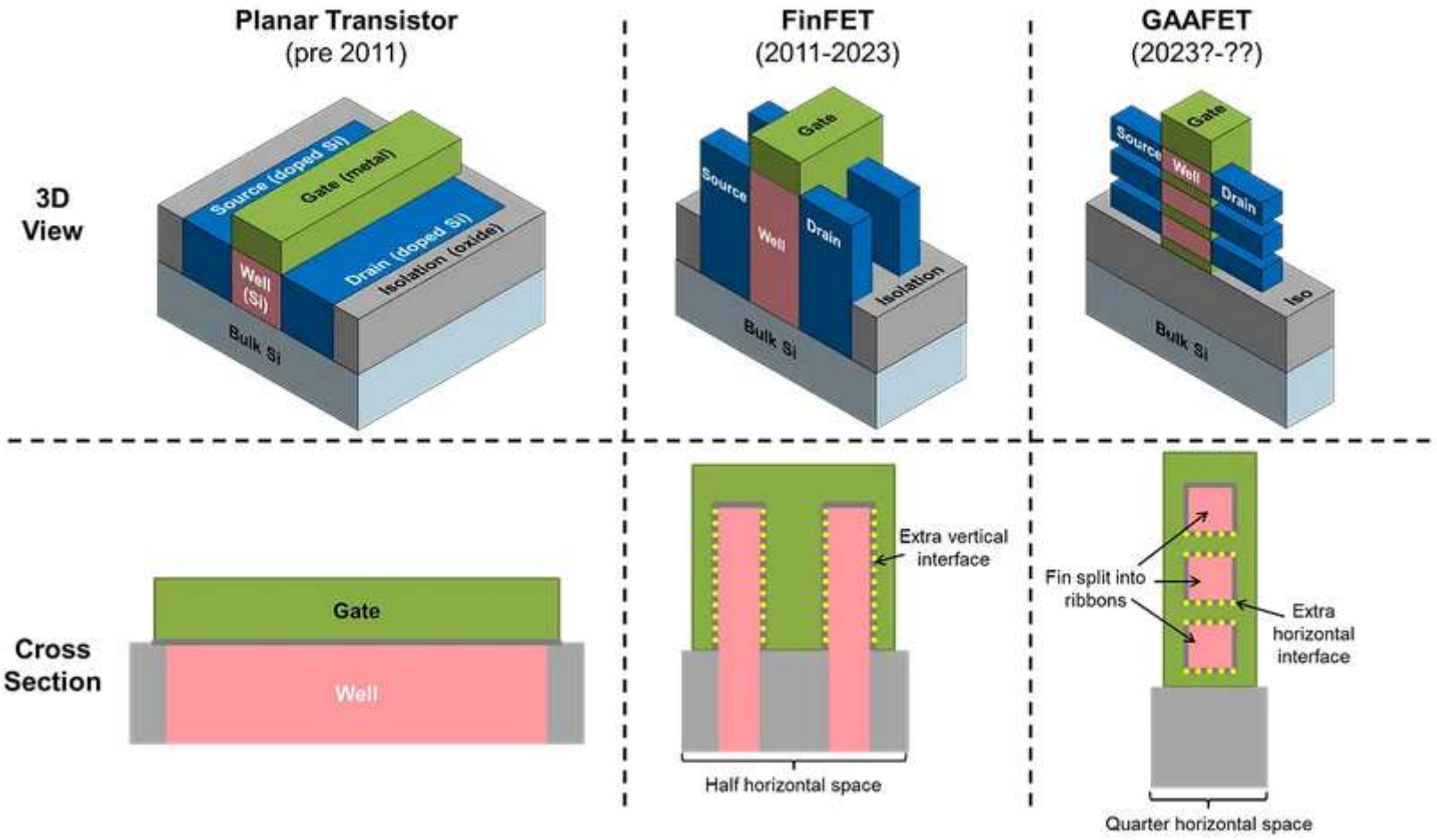
4.5.1 Introduction to the GAAFET transisitors

- The GAAFET transistor is termed as Gate-All-Around transistor or Ribbon FET.
- A GAA MOSFET was first demonstrated in 1988, by a Toshiba research team
- The main goal is to increasing transistor density (Moore law)
- The Gate-All-Around Field-Effect Transistor (GAAFET) represents a significant advancement in integrated circuits technology, offering enhanced functionality compared to its predecessor, the Fin Field-Effect Transistor (FinFET).
- Until now there are developed two generations of GAAFET transistors.



4.6.2 Introduction to the GAAFET transistor

Transistor technologies differences:



4.6.1 Introduction to the GAAFET transistors

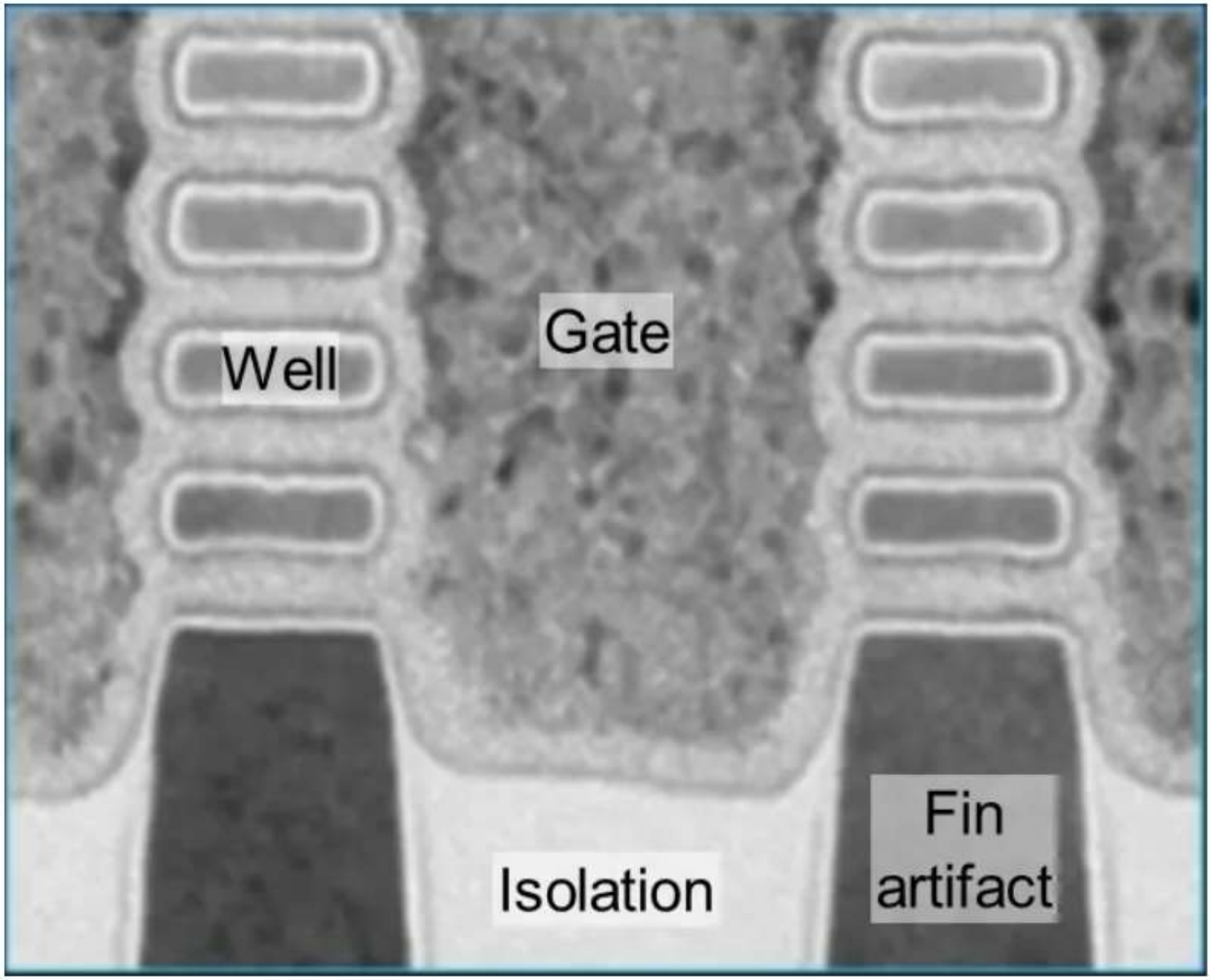
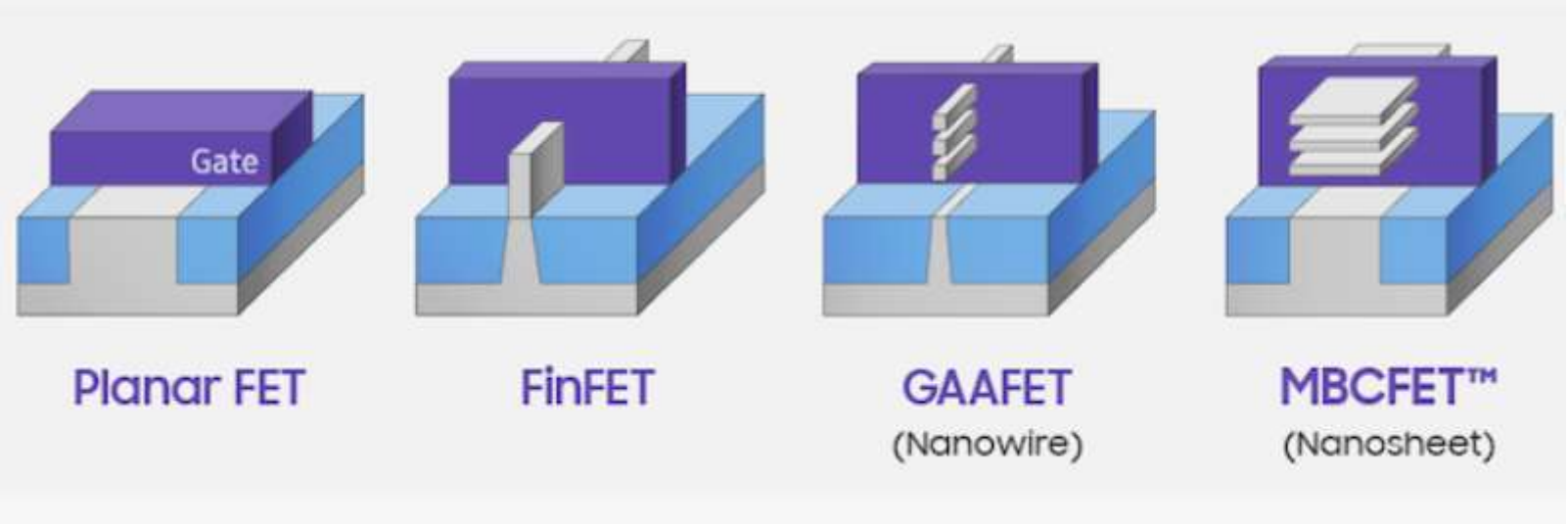


Figure 7. Electron Microscopy of Intel 20A 4-stack RibbonFET https://www.intel.com/content/www/us/en/newsroom/news/intel-accelerated-webcast-livestream-replay.html#gs.vic3x8

4.6.2 Introduction to the MBCFET transistor



MBCFET: Performance & power benefit

Unlike FinFETs, both the width and the number of the sheets can be varied to adjust drive strength or the amount of current the transistor can drive at a given voltage

The width of the nanosheet is a key metric in defining the power and performance characteristics: the higher the width, the higher the performance (at higher power).

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