**Design and implementation of an asynchronous MOD-60 counter**

**Objective**

1. To design an asynchronous MOD-60 counter using only basic logic gates and flip-flops.
2. To simulate the counter circuit to verify its functionality.
3. To analyze the performance of the circuit based on simulation results.

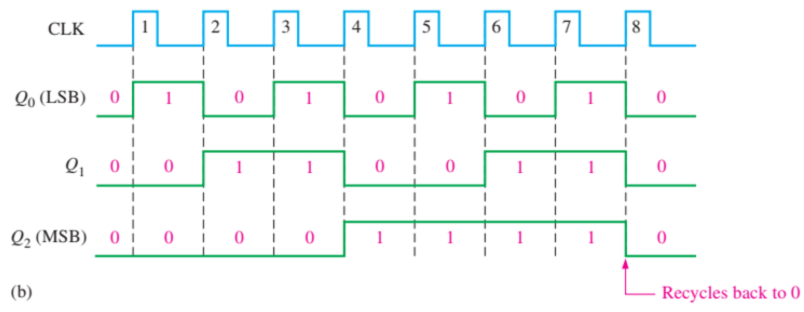
**Theory**

The design of an asynchronous MOD-60 counter involves creating a circuit that can count from 0 to 59 (60 states in total) and then reset to 0. This counter can be realized by cascading two counters: a MOD-10 (decade counter) and a MOD-6 counter. Each counter is constructed using JK flip-flops and logic gates.

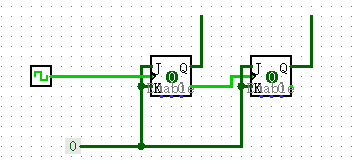
1. **Asynchronous Counter**

In an asynchronous counter, each flip-flop (FF) is triggered by the rising edge of the clock input. The key characteristics of this design are:

* First Flip-Flop: Directly triggered by the rising edge of the external clock pulse, ensuring immediate response to clock changes.
* Subsequent Flip-Flops: Each triggered by the rising edge of the output from the previous flip-flop, resulting in a sequential state change throughout the counter.



**Fig 2-1** The timing diagram for an asynchronous counter



**Fig 2-2** A 2-bit asynchronous counter

1. **Mod-N Counter**

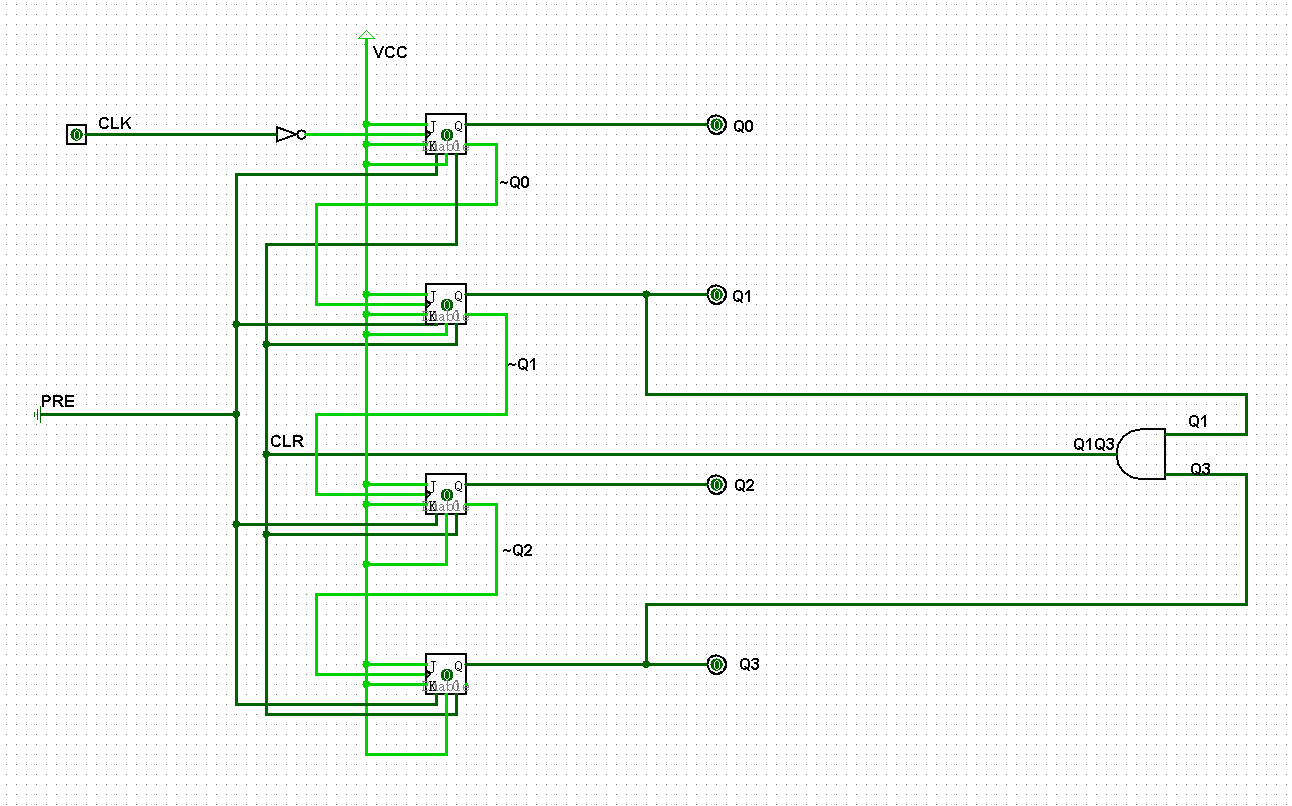
The MOD number in a counter indicates the total unique states it cycles through before resetting. For instance, a MOD-6 counter goes through six states (from 000 to 110 in binary) and then resets to 000. To create a counter with a MOD number less than the maximum count of a standard N-bit binary counter, additional logic is used. This logic monitors the counter's output and triggers a reset when it reaches the specified MOD number.

**In our implementation we use JK flip-flops to design counter**

* **Flip-Flop Configuration**: Set JK flip-flops in toggle mode (both J and K high). Each clock pulse toggles the flip-flop's output, enabling counting.
* **Detection Circuit**: Implement a circuit to monitor flip-flop outputs and detect when the count equals the MOD number.
* **Reset Signal**: Use the detection circuit's output to generate a reset signal. This resets all flip-flops, returning the counter to zero

1. **Mod 10**

The MOD-10 counter, characterized by its ability to count ten distinct states from 0000 (0 in decimal) to 1001 (9 in decimal), is commonly referred to as a decade counter.

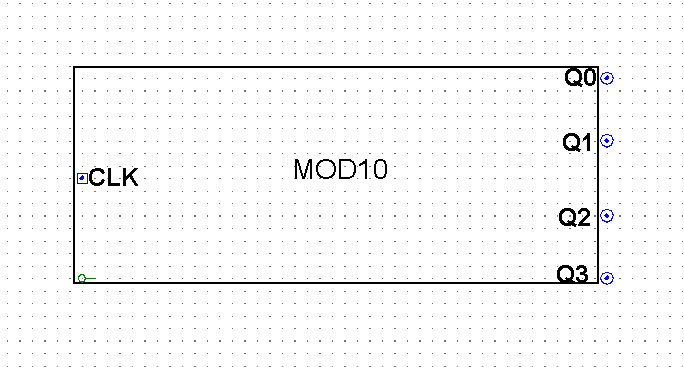


**Fig 2-3** Mod-10 counter Circuit Diagram

The circuit diagram Fig 2-4 illustrates a 4-bit binary counter composed of four flip-flops, each representing a single bit in the binary count sequence. The flip-flops are arranged in a typical ripple counter configuration where the output of each flip-flop serves as the clock input to the next flip-flop in the series.

**Circuit Diagram Description:**

* **Output States (Q0, Q1, Q2, Q3):** The outputs are labeled for each bit, from the least significant bit (Q0) to the most significant bit (Q3). These outputs will change state with each clock pulse, counting up in binary from 0 (0000) to 9 (1100).
* **Reset Input(CLR):** The CLR input responds to an external signal to immediately set the counter's output to zero. An AND gate connected to specific outputs (in this case, Q1 and Q3) is used to detect the reset condition and generate the required clear signal. When the counter reaches the binary count of 1010 (decimal 10), which is a temporary state, the AND gate outputs a high signal that activates the CLR input and resets the counter.

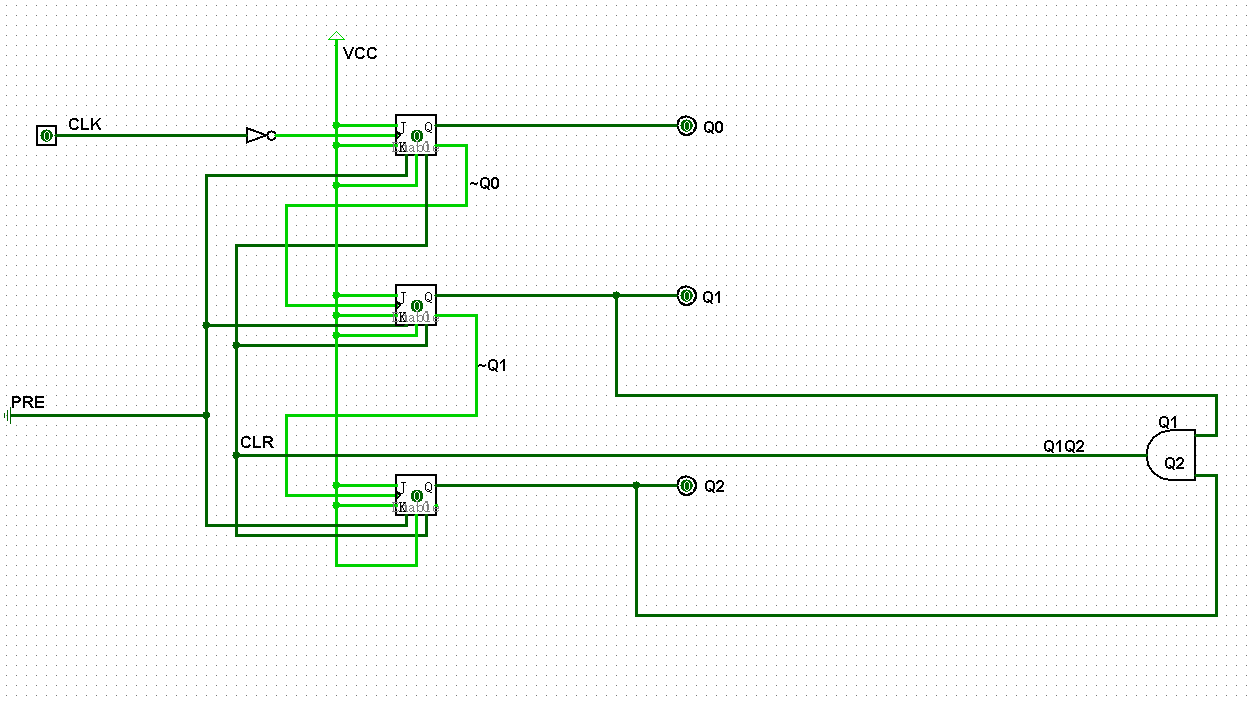


**Fig 2-4** Package diagram of a Mod-10 counter

Fig 2-4 shows the package diagram of a MOD-10 counter, encapsulating the complexity of the internal circuitry within a simple rectangular symbol for ease of use in system-level diagrams.

1. **Mod 6**

The MOD-6 counter is designed to count six distinct states from 000 (0 in decimal) to 101 (5 in decimal) and is an essential component for applications requiring counting in a range less than a full decade. Unlike the MOD-10 counter, the MOD-6 counter must recycle back to zero after reaching the sixth count instead of the tenth.

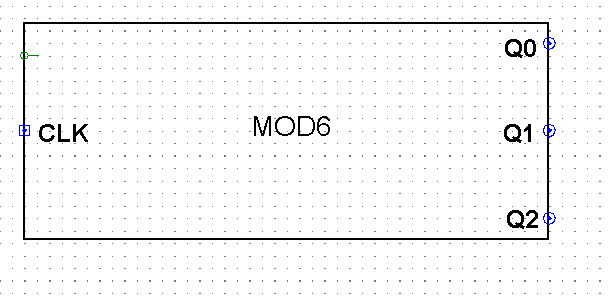


**Fig 2-5** Mod-6 counter Circuit Diagram

The circuit diagram Fig 2-5 illustrates a 3-bit binary counter composed of three flip-flops, each representing a single bit in the binary count sequence. The flip-flops are arranged in a typical ripple counter configuration where the output of each flip-flop serves as the clock input to the next flip-flop in the series.

**Circuit Diagram Description:**

* **Output States (Q0, Q1, Q2):** Outputsfor each bit, with Q0 being the least significant bit and Q2 the most significant bit, would represent the binary count. The counter would increment its binary value from 0 (000) to 5 (101).
* **Reset Logic for MOD-6 Counter**: When both Q1 and Q2 are HIGH, the AND gate would output a HIGH signal, which, when connected to the CLR input of the flip-flops, would reset the counter back to zero.



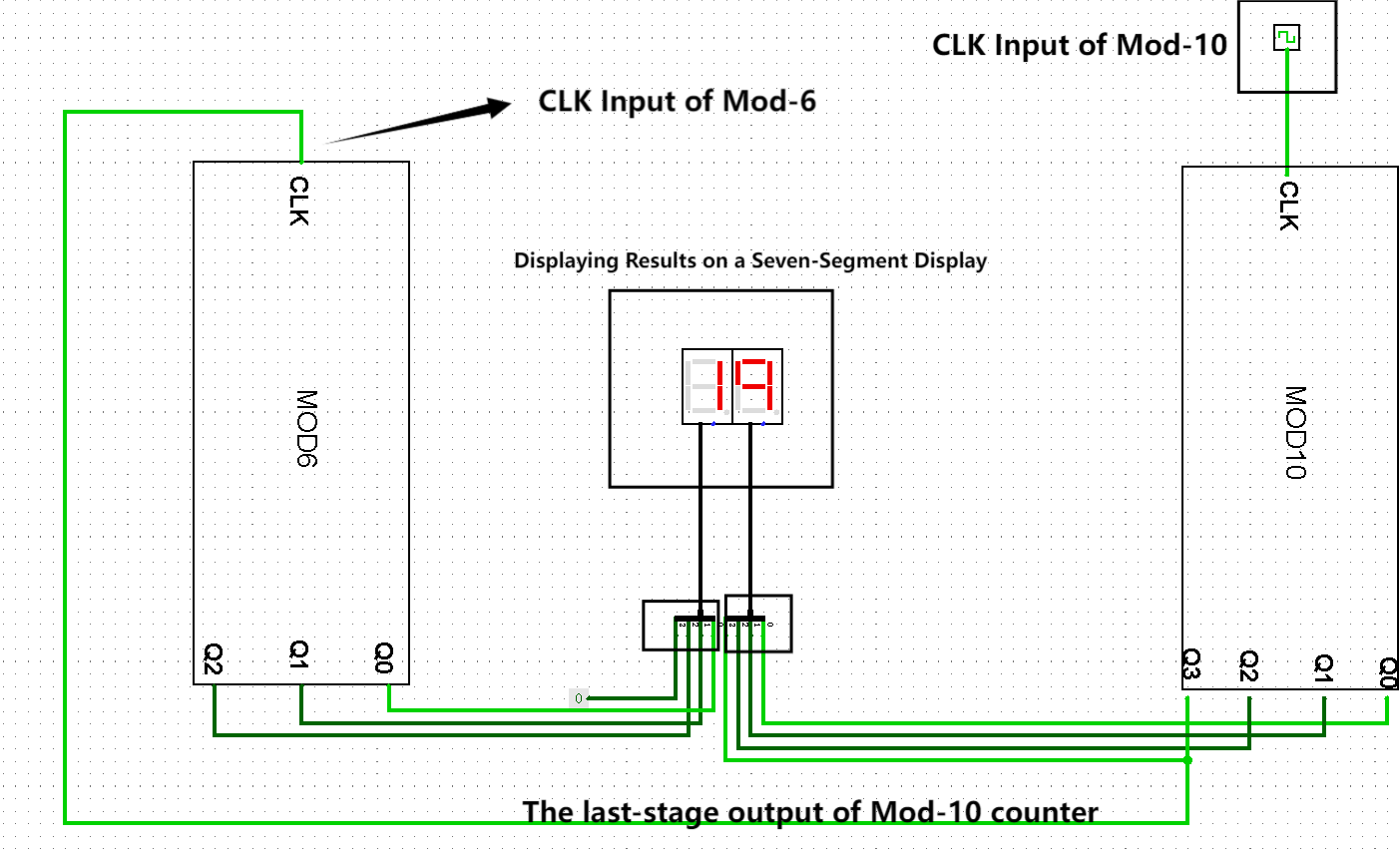
**Fig 2-6** Package diagram of a Mod-6 counter

Fig 2-6 shows the package diagram of a MOD-6 counter, encapsulating the complexity of the internal circuitry within a simple rectangular symbol for ease of use in system-level diagrams. The counter is represented as a single module labelled 'MOD6', which abstracts the internal configuration of flip-flops and logic gates used to create the Mod6 counting functionality.

1. **Cascade Counter**

To construct a MOD-60 counter, a MOD-10 counter and a MOD-6 counter are cascaded. The MOD-10 counter acts as the least significant digit, counting from 0 to 9, while the MOD-6 counter represents the most significant digit, counting from 0 to 5. Upon the MOD-10 counter's transition from 9 back to 0, it triggers the MOD-6 counter to increment, thus creating a combined count that cycles from 00 to 59 before resetting to 00.

The increment trigger from the MOD-10 to the MOD-6 counter is typically implemented by connecting the carry-out or a specific state output (like when all bits are high) of the MOD-10 counter to the clock input of the MOD-6 counter.



**Fig 2-7** A cascaded counter of MOD-6 counter and MOD-10 counter circuit diagram

The circuit diagram Fig 2-7 would illustrate the interconnected MOD-10 and MOD-6 counters, showing the flow of signals between them and the logic involved in their cascading.

**List of apparatus/components**

Below are the lists of the components used in this circuit.

|  |  |
| --- | --- |
| **Gate** | **Quantity** |
| 2-Input AND Gate | 2 |
| Inverter | 2 |
| JK flip-flop | 7 |
| Hex Digit Display | 2 |

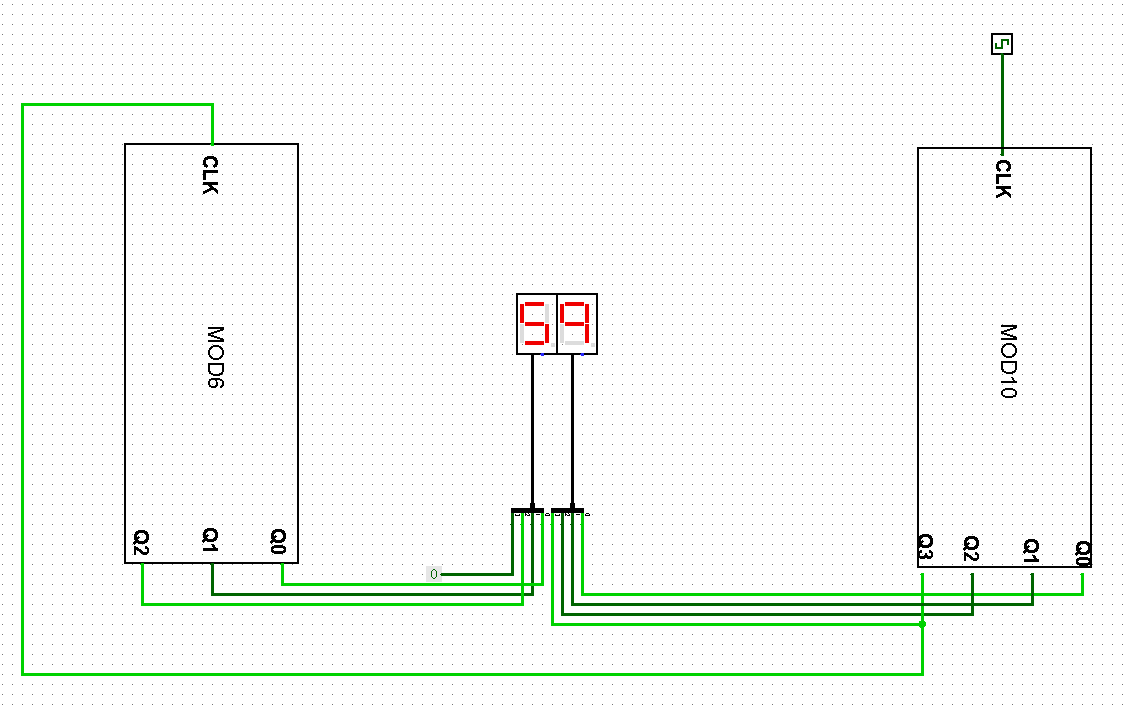
**Table 2-1** Gate List

|  |  |  |
| --- | --- | --- |
| **IC No** | **Description** | **Quantity** |
| CD4081 | Quad 2-Input AND Gate | 2 |
| 74HC112 | Dual JK flip-flop with set and reset; negative-edge trigger | 3 |
| CD4511 | BCD-to-7-Segment LED Latch Decoder | 1 |

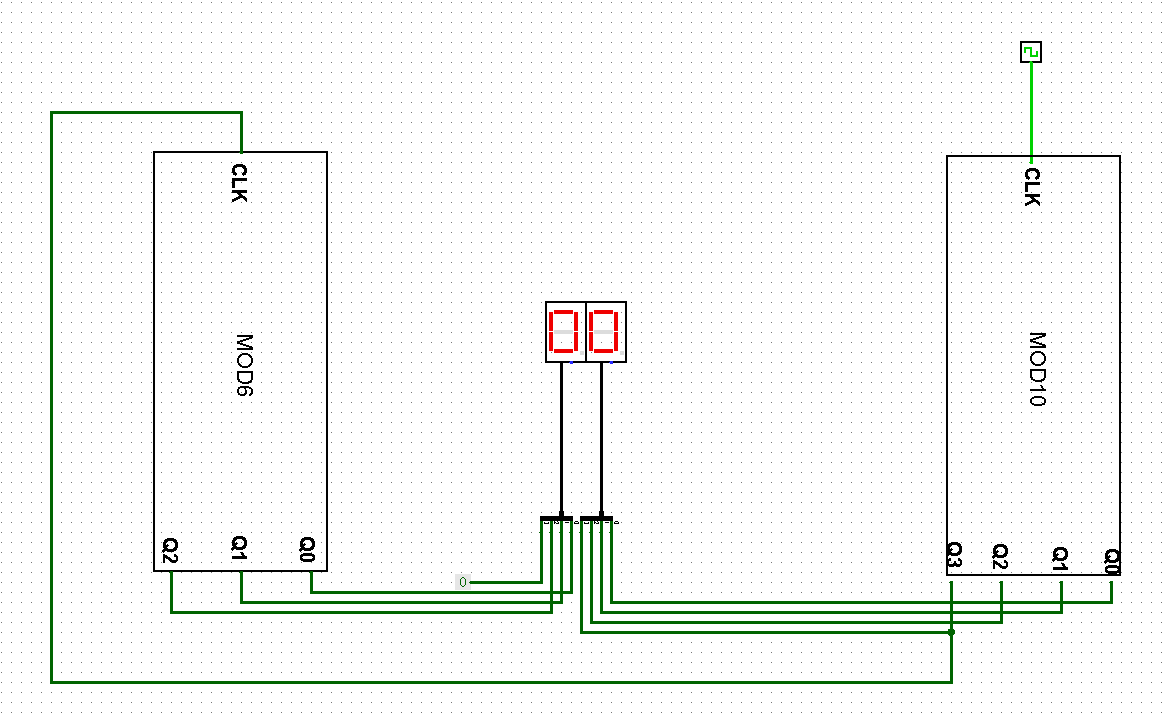
**Table 2-2** IC List

**Result**

**In Figures 2-8 and 2-9,** we observe the counter at the moment following a reset activation. The displays indicate '0', confirming the counter's capability to successfully reset and initiate a new counting sequence. This illustrates the proper functioning of the reset mechanism, which is critical in the transition from the final count state '59' to an overflow condition that would naturally lead to '60'. Instead of proceeding to '60', the reset logic intervenes, causing both the MOD-6 and MOD-10 counters to revert to their initial state. Consequently, the display is reset to show '00', indicating readiness for a new cycle. This successful reset operation is a testament to the effectiveness of the combinational logic implemented to monitor and control the counter states.



**Fig 2-8** Final State Before Reset



**Fig 2-9** Initial State After Reset

The simulation results confirm the functionality of the MOD-60 counter, showcasing its capacity to count up to 59 and then recycle to 0 as expected.

**Discussion and comment**

**Propagation Delay**

In designing the asynchronous MOD-60 counter, propagation delay, setup time, and hold time are critical parameters that define the performance and reliability of the circuit. The propagation delay, , is the time taken for a signal to transition from low to high and high to low, respectively. These delays are crucial in determining the maximum operating frequency of the counter.

During our experimental procedure, we opted for the 74HC112 JK Flip-Flops as the primary components in the MOD-60 counter design. This model was selected due to its balanced propagation delay of 17 ns for both , which is conducive to achieving a responsive yet stable counting mechanism.

To derive the maximum operational clock frequency ,we will assume the worst case the total propagation delay of the counter

Given that our MOD-60 counter utilizes a total of 7 JK flip-flops—representing a combination of a MOD-10 and a MOD-6 counter to encapsulate the full range of 60 states—we set N to 7.

By incorporating this value into the calculation, we determine the upper limit for the clock frequency permissible for the counter's seamless operation without the risk of state-skipping or miscounting due to propagation delay.

**Difference from Asynchronous and Synchronous Counters**

The design choice between asynchronous and synchronous counters is influenced by key operational parameters. Asynchronous counters, characterized by flip-flops triggered sequentially, suffer from cumulative propagation delays that limit their operational speed. However, their simplicity offers a design advantage for less demanding applications.

Conversely, synchronous counters, with flip-flops triggered concurrently by a common clock signal, exhibit uniform propagation delays and higher operational speeds. While they are more complex to design due to additional logic requirements, their synchronised operation enhances reliability and scalability for high-speed applications.

In our MOD-60 counter design, using 74HC112 JK Flip-Flops, the asynchronous configuration was deemed suitable due to its simplicity and the acceptable propagation delay of 17 ns, sufficient for the required counting frequency and precision.