Allwinner Technology

Allwinner A64 Datasheet

Mobile Application Processor

Version 1.1

Jun. 26, 2015

Revision History

Version	Date	Description
V1.0	Mar.30,2015	Initial Release Version.
V1.1	Jun.26,2015	Revise the feature of display output. Add SMHC1/SMHC2 AC electrical characteristics.

Declaration

THIS A64 DATASHEET IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF ALLWINNER TECHNOLOGY ("ALLWINNER"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF ALLWINNER AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE INFORMATION FURNISHED BY ALLWINNER IS BELIEVED TO BE ACCURATE AND RELIABLE. ALLWINNER RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE. ALLWINNER DOES NOT ASSUME ANY RESPONSIBILITY AND LIABILITY FOR ITS USE. NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF ALLWINNER. THIS DATASHEET NEITHER STATES NOR IMPLIES WARRANTY OF ANY KIND, INCLUDING FITNESS FOR ANY PARTICULAR APPLICATION.

THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. ALLWINNER SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. ALLWINNER SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

Table of Contents

1. Overview

Allwinner's A64 is a quad-core,64bit SoC targeted for high performance tablets.A64 integrates a higher energy efficiency ARM Cortex-A53 CPU architecture, and also includes advanced 3D graphics processing unit, high-definition video decoding/encoding, low power audio codec, excellent display controllers and a broad range of interfaces.

The processor has some very exciting features:

- **CPU**   Quad-core ARM Cortex-A53 Processor, a power-efficient ARM v8 architecture, it has 64 and 32bit execution states for scalable high performance ,which includes a NEON multimedia processing engine.
- **Graphics**   ARM Mali400MP2 graphics acceleration provides mobile users with superior experience in web browsing, video playback and gaming effects; OpenGL ES2.0 ,OpenVG1.1 standards are supported.
- **Video**   A64 provides almost full motion playback of up to 4K high-definition video, and supports H.265 decoder by 4K@30fps , H.264 decoder by 1080p@60fps, MPEG1/2/4 decoder by 1080p@60fps, VP8 decoder by 1080p@60fps, AVS/AVS+ decoder by 1080p@60fps,VC1 decoder by 1080p@30fps, H.264 encoder by 1080p@60fps with dedicated hardware.
- **Audio**   An integrated audio subsystem delivers extremely low power audio playback and exceptional high quality sound.
- **Display**   A64 features Allwinner's SmartColor2.0^{TM} technology with an integrated display engine. Content can be displayed on 4-lane MIPI DSI displays up to 1920x1200@60fps, or a RGB panel interface up to 1920x1200@60fps, or LVDS panel up to 1366x768@60fps, or HDMI v1.4 is also supported up to 4K@30fps.
- **External Memory**   Many types of external memory devices are supported, including LPDDR2, LPDDR3, DDR2, DDR3 ,DDR3L, NAND Flash(MLC,SLC,TLC,EF),Nor Flash, SD/SDIO/MMC including eMMC up to rev5.0,and also supports booting from RAW NAND,eMMC,SD/TF Card or Nor Flash.
- **Security**   A64 delivers hardware security features that enable trustzone security system, Digital Rights Management(DRM), information encryption/decryption, secure boot, secure JTAG and secure efuse.
- **Connectivity**   A64 has a broad range of hardware interfaces such as parallel CMOS sensor interface, 10/100/1000Mbps EMAC,USB OTG v2.0 operating at high speed(480Mbps) with PHY, USB Host with PHY and a variety of other popular interfaces(SPI,UART,CIR,TS,TWI,RSB,SCR).

2. Feature

2.1. CPU Architecture

- Quad-core ARM Cortex-A53 Processor
- A power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- 3~10x better software encryption performance
- Support NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Support Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache
- 512KB L2 cache

2.2. GPU Architecture

- ARM Mali400MP2 GPU
- Support OpenGL ES 2.0 and OpenVG 1.1 standard

2.3. Memory Subsystem

Boot ROM
- On-chip memory
- Size:112KB(non secure ROM:48KB,secure ROM:64KB)
- Support secure and non-secure access boot
- Support system boot from the following device:
  - Raw NAND
  - eMMC
  - SD/TF card
  - SPI NOR Flash
- Support system code download through USB OTG

SDRAM
- Compatible with JEDEC standard DDR2 /DDR3 /DDR3L/LPDDR2/LPDDR3 SDRAM
- Support clock frequency up to 667MHz(DDR3-1333)
- Support 2 chip selects
- Up to 3GB address space
- 32-bits bus width
- 16 address signal lines and 3 bank signal lines
- Support Memory Dynamic Frequency Scale(MDFS)

NAND Flash
- Up to 2 chip selects
- 8-bit data bus width
- Up to 64-bit ECC per 1024 bytes
- Support 1024,2048,4096,8192,16K bytes size per page

- Support SLC/MLC/TLC flash and EF-NAND memory
- Support SDR,ONFI DDR and Toggle DDR NAND
- Embedded DMA to do data transfer
- Support data transfer together with normal DMA

SD/MMC
- Up to three SD/MMC controllers
- Comply to eMMC standard specification V5.0, SD physical layer specification V2.0, SDIO card specification V3.0
- 1-bit or 4-bit data bus transfer mode for SD cards
- 1-bit or 4-bit data bus transfer mode for SDIO interface
- 1-bit ,4-bit or 8-bit data bus transfer mode for MMC cards
- Embedded special DMA to do data transfer
- Support hardware CRC generation and error detection

2.4. System Peripheral

Timer
- Two on-chip timers with interrupt-based operation
- One watchdog to resume the controller operation
- Two AVS Counter to synchronize video and audio in the player
- 24MHz or 32KHz clock input

High Speed Timer
- One high speed timer with 56bit counter
- Clock source is synchronized with AHB1 clock, much more accurate than other timers

RTC
- Calendar :Counters second,minutes,hours,day,week,month and year with leap year generator
- Alarm: general alarm and weekly alarm
- One 32768Hz fanout

GIC
- Support 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 125 Shared Peripheral Interrupts(SPIs)

DMA
- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

CCU
- 13 PLLs
- One on-chip RC oscillator
- Support a external 24MHz oscillator and a external32.768KHz oscillator
- Support clock configuration and clock generated for corresponding modules
- Support software-controlled clock gating and software-controlled reset for corresponding modules

KEYADC
- ADC with 6-bit resolution for key
- Support hold key and continuous key

- Support single key, normal key and continuous key

PWM
- Support outputting two kinds of waveform: continuous waveform and pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency

Thermal Sensor
- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Support over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Support 3 sensors:sensor0 for CPU,sensor1/2 for GPU

Crypto Engine(CE)
- Support Symmetrical algorithm: AES,DES,TDES
    - Support AES 128/192/256-bits with ECB,CBC,CTS,CTR mode
    - Support DES/TDES with ECB,CBC,CTR mode
- Support Hash algorithm: MD5,SHA1,SHA224,SHA256,HMAC
- Support Asymmetrical algorithm:RSA512/1024/2048bit
- Support 160-bits hardware PRNG with 175-bits seed
- Support 256-bits hardware TRNG
- Internal Embedded DMA to do data transfer
- Support secure and non-secure interfaces respectively

Security ID
- Support 2K-bits EFUSE for chip ID and security application

CPU Configuration
- Capable of CPU reset, including core reset, debug circuit rest, etc
- Capable of other CPU-related control, including interface control, CP15 control, and power control, etc
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc

2.5. Display Subsystem

DE
- Output size up to 4096x4096
- Support four alpha blending channels for main display, two channels for aux display
- Support four overlay layers in each channel, and has a independent scaler
- Support potter-duff compatible blending operation
- Support input format :YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ RGB565
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-side Half 3D format data
- Support SmartColor^{TM} 2.0 for excellent display experience
    - Adaptive edge sharping
    - Adaptive color enhancement
    - Adaptive contrast enhancement and fresh tone rectify
- Support writeback and rotation for high efficient dual display and miracast

Display Output
- Support LVDS interface with single link, up to 1366x768@60fps
- Support RGB interface with DE/SYNC mode, up to 1920x1200@60fps
- Dither function from RGB666/RGB565 to RGB888

- Support 4-lanes MIPI DSI up to 1920x1200@60fps
- Support HDMI1.4 with HDCP1.2 up to 4K@30fps

2.6. Video Engine

Video Decoding
- Support multi-format video decoder, include:
    - H.265 : 4K@30fps, 1080p@120fps
    - H.264 : 1080p@60fps
    - MPEG1/2/4 : 1080p@60fps
    - VC1 : 1080p@30fps
    - VP8 : 1080p@60fps
    - AVS/AVS+: 1080p@60fps
    - JPEG/MJPEG:1080p@30fps
- Support 1080p blu-ray 3D
- Support frame compatible 3D format,size:3840x1080,1920x2160

Video Encoding
- Support H.264 video encoding up to 1080p@60fps
- JPEG baseline: picture size up to 8192x8192
- Support input formats: YU12/YV12/NV12/NV21/YUYV/YVYU/UYVY/VYUY/ARGB/BGRA/RGBA/ABGR/YU16/YV16/TILE32/TILE128
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Support rotated input

2.7. Image In

CSI
- Support 8bit YUV422 CMOS sensor parallel interface
- Support CCIR656 protocol for NTSC and PAL
- Maximum still capture resolution to 5M
- Maximum video capture resolution to 1080p@30fps

2.8. Audio Subsystem

Audio Codec
- Two audio digital-to-analog(DAC) channels
- Stereo capless headphone drivers:
    - 100dB SNR@A-weight
    - Support DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Differential earpiece driver
- Analog low-power loop from line-in/microphone to headphone/earpiece outputs
- Support Dynamic Range Controller(DRC) adjusting the DAC playback output
- Accessory button press detection
- Four audio inputs:
    - Two differential microphone inputs
    - One differential Phone input
    - Stereo Line-in L/R input

- Four audio outputs:
  - Earpiece amplifier differential output
  - Phone amplifier differential output
  - Headphone amplifier L/R channel output
  - Line-out L/R output
- Two audio analog-to-digital(ADC) channels
  - 96dB SNR@A-weight
  - Supports ADC Sample Rates from 8KHz to 48KHz
- Support Automatic Gain Control(AGC) and Dynamic Range Control(DRC) adjusting the ADC recording output
- Two PCM interface connected with BB and BT
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Support Audio HUB

I2S/PCM
- Up to two I2S/PCM controllers
- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8KHz to 192KHz
- Support 8-bits u-law and 8-bits A-law companded sample
- Support programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)
- Support Audio HUB

One Wire Audio(OWA)
- IEC-60958 transmitter and receiver functionality
- Complies with SPDIF Interface
- Support channel status insertion for the transmitter
- Hardware Parity generation on the transmitter
- One 32x24bits TX FIFO for audio data transfer
- Programmable FIFO thresholds
- Support Audio HUB

2.9. External Peripherals

USB Controller
- One USB 2.0 OTG,with integrated one USB 2.0 analog PHY
  - Complies with USB2.0 Specification
  - Support High-Speed (HS,480Mbps),Full-Speed(FS,12Mbps) and Low-Speed(LS,1.5Mbps) in host mode
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
  - Support 8KB FIFO for EPs(excluding EP0)
  - HCI(EHCI+OHCI) and USB2.0 OTG SIE share USB analog PHY
- One EHCI/OHCI Host, multiplexed with one USB 2.0 analog PHY and one HSIC PHY
  - Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.

EMAC
- Support RMII/RGMII interface
- Support 10/100/1000Mbps data transfer rate

- Support full-duplex and half-duplex operation
- Support linked-list descriptor list structure
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes

UART
- Up to six UART controllers
- Two of six UART controllers support 2-wire while others support 4-wire
- 64-Bytes Transmit and receive data FIFOs for all UART
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association(IrDA) 1.0 SIR
- Support speed up to 3MHz

SPI
- Up to two SPI controllers
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- Support single and dual IO mode

Two Wire Interface(TWI)
- Up to four TWI controllers
- Support Standard mode(up to 100K bps) and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bit addressing transactions
- Perform arbitration and clock synchronization
- Allow operation from a wide range of input clock frequencies

CIR
- A flexible receiver for IR remote
- 64x8bits FIFO for data buffer
- Programmable FIFO threshold

RSB^{TM}
- Up to 20MHz speed with ultra low power
- Support push-pull bus
- Support host mode and multi-devices
- Programmable output delay of CD signal
- Support parity check for address and data transmission

TS
- Compliant with the industry-standard AMBA Host Bus(AHB) Specification, Revision 2.0.Support 32-bit Little Endian bus.
- Support DVB-CSA V1.1 Descrambler
- One external Synchronous Parallel Interface(SPI) or one external Synchronous Serial Interface(SSI)
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting

SCR

- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Support asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
    - Card activation and deactivation
    - Cold/warm reset
    - Answer to Reset (ATR) response reception
    - Data transfers to and from the card

2.10. Package

- FBGA396 balls, 0.65mm ball pitch, 15x15mm

3. Block Diagram

Figure 3-1 shows the block diagram of the A64.

Image	Video Engine		Connectivity
Parallel CSI 5M pixel 8-bit bus	Decoder Multi-format H.265 4K@30fps	Encoder H.264 1080p@60fps	USB2.0 OTG with USB 2.0 PHY

Display
- DE SmatColor 2.0
- LVDS output 1366x768@60fps
- RGB 1920x1200@60fps
- 4-lanes MIPI DSI 1920x1200@60fps
- HDMI 1.4 with HDCP1.2 4K@30fps

Cortex-A53 Quad-core
- 32KB L1 I-cache + 32KB L1 D-cache per core
- 512KB L2 cache

GPU
- Mali400MP2 OpenGL ES 2.0 and OpenVG 1.1

Connectivity
- USB2.0 OTG with USB 2.0 PHY
- USB Host with USB 2.0 PHY and HSIC PHY
- TS Demux x1 SPI/SSI mode with CSA1.1
- SDIO3.0
- SCR
- TWI x4
- CIR Rx
- SPI x2
- UART x6
- RSB
- KEYADC

External Memory
- DDR2/DDR3/DDR3L/ LPDDR2/ LPDDR3 32-bits bus 667MHz(DDR3-1333)
- NDFC 8bits bus 64bits ECC
- SD2.0/eMMC5.0 1/4/8-bits bus

System
- CLOCK 24MHz/32.768KHz
- CCU
- Thermal Sensor
- Timer
- DMA
- PWM
- GPIO

Audio
- I2S/PCM x 2
- OWA output
- Audio Codec

Security System
- Security Boot
- Crypto Engine
- TrustZone
- Efuse

Ethernet
- 10/100/1000M EMAC

Figure 3-1. A64 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of A64 Pins from seven aspects: BALL#, Pin Name, Default Function, Type, Reset State, Default Pull Up/Down, and Buffer Strength.

Table 4-1. Pin Characteristics

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
DRAM						
P5	SA0	DRAM	I/O	Z	-	-
R4	SA1	DRAM	I/O	Z	-	-
N5	SA2	DRAM	I/O	Z	-	-
N6	SA3	DRAM	I/O	Z	-	-
P6	SA4	DRAM	I/O	Z	-	-
G4	SA5	DRAM	I/O	Z	-	-
F3	SA6	DRAM	I/O	Z	-	-
E4	SA7	DRAM	I/O	Z	-	-
D3	SA8	DRAM	I/O	Z	-	-
C4	SA9	DRAM	I/O	Z	-	-
M4	SA10	DRAM	I/O	Z	-	-
U4	SA11	DRAM	I/O	Z	-	-
K5	SA12	DRAM	I/O	Z	-	-
E8	SA13	DRAM	I/O	Z	-	-
K4	SA14	DRAM	I/O	Z	-	-
T4	SA15	DRAM	I/O	Z	-	-
D8	SBA0	DRAM	O	Z	-	-
R3	SBA1	DRAM	O	Z	-	-
C6	SBA2	DRAM	O	Z	-	-
C9	SCAS	DRAM	O	Z	-	-
G3	SCKN	DRAM	O	Z	-	-
G2	SCKP	DRAM	O	Z	-	-
J3	SCKE0	DRAM	O	Z	-	-
H6	SCKE1	DRAM	O	Z	-	-
E5	SCS0	DRAM	O	Z	-	-
H5	SCS1	DRAM	O	Z	-	-
D5	SODT0	DRAM	O	Z	-	-
E7	SODT1	DRAM	O	Z	-	-
L3	SDQ0	DRAM	I/O	Z	-	-
G1	SDQ1	DRAM	I/O	Z	-	-
H3	SDQ2	DRAM	I/O	Z	-	-

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
K1	SDQ3	DRAM	I/O	Z	-	-
H2	SDQ4	DRAM	I/O	Z	-	-
H1	SDQ5	DRAM	I/O	Z	-	-
L1	SDQ6	DRAM	I/O	Z	-	-
L2	SDQ7	DRAM	I/O	Z	-	-
T3	SDQ8	DRAM	I/O	Z	-	-
T2	SDQ9	DRAM	I/O	Z	-	-
T1	SDQ10	DRAM	I/O	Z	-	-
R2	SDQ11	DRAM	I/O	Z	-	-
N3	SDQ12	DRAM	I/O	Z	-	-
N2	SDQ13	DRAM	I/O	Z	-	-
N1	SDQ14	DRAM	I/O	Z	-	-
M2	SDQ15	DRAM	I/O	Z	-	-
E3	SDQ16	DRAM	I/O	Z		
F2	SDQ17	DRAM	I/O	Z		
E2	SDQ18	DRAM	I/O	Z		
E1	SDQ19	DRAM	I/O	Z		
B1	SDQ20	DRAM	I/O	Z		
B2	SDQ21	DRAM	I/O	Z		
A2	SDQ22	DRAM	I/O	Z		
B3	SDQ23	DRAM	I/O	Z		
C5	SDQ24	DRAM	I/O	Z		
B4	SDQ25	DRAM	I/O	Z		
A4	SDQ26	DRAM	I/O	Z		
A5	SDQ27	DRAM	I/O	Z		
A7	SDQ28	DRAM	I/O	Z		
A8	SDQ29	DRAM	I/O	Z		
B8	SDQ30	DRAM	I/O	Z		
B9	SDQ31	DRAM	I/O	Z		
J2	SDQM0	DRAM	O	Z	-	-
P3	SDQM1	DRAM	O	Z	-	-
C2	SDQM2	DRAM	O	Z		
B7	SDQM3	DRAM	O	Z		
K2	SDQS0N	DRAM	I/O	Z	-	-
K3	SDQS0P	DRAM	I/O	Z	-	-
P2	SDQS1N	DRAM	I/O	Z	-	-
P1	SDQS1P	DRAM	I/O	Z	-	-
D1	SDQS2N	DRAM	I/O	Z	-	-
D2	SDQS2P	DRAM	I/O	Z	-	-
B5	SDQS3N	DRAM	I/O	Z	-	-
B6	SDQS3P	DRAM	I/O	Z	-	-

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
F7	SRAS	DRAM	O	Z	-	-
D10	SRST	DRAM	O	Z	-	-
G5	SVREF	DRAM	P	Z	-	-
C8	SWE	DRAM	O	Z	-	-
U1	SZQ	DRAM	A	Z	-	-
G7,G8,G9,J8,K6,K7, L6,L7,L8,N7,N8	VCC-DRAM	POWER	P	-	-	-
GPIO B						
V9	PB0	GPIO	I/O	Z	NO PULL	20
AB7	PB1	GPIO	I/O	Z	NO PULL	20
W10	PB2	GPIO	I/O	Z	NO PULL	20
AA7	PB3	GPIO	I/O	Z	NO PULL	20
W7	PB4	GPIO	I/O	Z	NO PULL	20
AA6	PB5	GPIO	I/O	Z	NO PULL	20
W8	PB6	GPIO	I/O	Z	NO PULL	20
Y6	PB7	GPIO	I/O	Z	NO PULL	20
V10	PB8	GPIO	I/O	Z	NO PULL	20
Y7	PB9	GPIO	I/O	Z	NO PULL	20
GPIO C						
T21	PC0	GPIO	I/O	Z	NO PULL	20
K18	PC1	GPIO	I/O	Z	NO PULL	20
P20	PC2	GPIO	I/O	Z	NO PULL	20
P19	PC3	GPIO	I/O	Z	Pull-up	20
T20	PC4	GPIO	I/O	Z	Pull-up	20
G20	PC5	GPIO	I/O	Z	NO PULL	20
K19	PC6	GPIO	I/O	Z	Pull-up	20
T19	PC7	GPIO	I/O	Z	Pull-up	20
M21	PC8	GPIO	I/O	Z	NO PULL	20
L19	PC9	GPIO	I/O	Z	NO PULL	20
K20	PC10	GPIO	I/O	Z	NO PULL	20
H20	PC11	GPIO	I/O	Z	NO PULL	20
P18	PC12	GPIO	I/O	Z	NO PULL	20
L20	PC13	GPIO	I/O	Z	NO PULL	20
J21	PC14	GPIO	I/O	Z	NO PULL	20
R21	PC15	GPIO	I/O	Z	NO PULL	20
N20	PC16	GPIO	I/O	Z	NO PULL	20
R16	VCC-PC	POWER	P	-	-	-
GPIO D						
AA20	PD0	GPIO	I/O	Z	NO PULL	20
AA17	PD1	GPIO	I/O	Z	NO PULL	20
W19	PD2	GPIO	I/O	Z	NO PULL	20
AA14	PD3	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
V18	PD4	GPIO	I/O	Z	NO PULL	20
AA15	PD5	GPIO	I/O	Z	NO PULL	20
Y11	PD6	GPIO	I/O	Z	NO PULL	20
AA16	PD7	GPIO	I/O	Z	NO PULL	20
V17	PD8	GPIO	I/O	Z	NO PULL	20
AA13	PD9	GPIO	I/O	Z	NO PULL	20
W16	PD10	GPIO	I/O	Z	NO PULL	20
Y16	PD11	GPIO	I/O	Z	NO PULL	20
AC16	PD12	GPIO	I/O	Z	NO PULL	20
AB16	PD13	GPIO	I/O	Z	NO PULL	20
AB15	PD14	GPIO	I/O	Z	NO PULL	20
AB14	PD15	GPIO	I/O	Z	NO PULL	20
AC14	PD16	GPIO	I/O	Z	NO PULL	20
AC13	PD17	GPIO	I/O	Z	NO PULL	20
AB13	PD18	GPIO	I/O	Z	NO PULL	20
AB12	PD19	GPIO	I/O	Z	NO PULL	20
AB11	PD20	GPIO	I/O	Z	NO PULL	20
AC11	PD21	GPIO	I/O	Z	NO PULL	20
Y13	PD22	GPIO	I/O	Z	NO PULL	20
AC10	PD23	GPIO	I/O	Z	NO PULL	20
Y14	PD24	GPIO	I/O	Z	NO PULL	20
U16	VCC-PD	POWER	P	-	-	-
GPIO E						
AA18	PE0	GPIO	I/O	Z	NO PULL	20
AB23	PE1	GPIO	I/O	Z	NO PULL	20
AA22	PE2	GPIO	I/O	Z	NO PULL	20
AA21	PE3	GPIO	I/O	Z	NO PULL	20
AA19	PE4	GPIO	I/O	Z	NO PULL	20
W17	PE5	GPIO	I/O	Z	NO PULL	20
W20	PE6	GPIO	I/O	Z	NO PULL	20
Y19	PE7	GPIO	I/O	Z	NO PULL	20
AC22	PE8	GPIO	I/O	Z	NO PULL	20
Y17	PE9	GPIO	I/O	Z	NO PULL	20
AB22	PE10	GPIO	I/O	Z	NO PULL	20
W21	PE11	GPIO	I/O	Z	NO PULL	20
AB20	PE12	GPIO	I/O	Z	NO PULL	20
Y22	PE13	GPIO	I/O	Z	NO PULL	20
AC20	PE14	GPIO	I/O	Z	NO PULL	20
Y23	PE15	GPIO	I/O	Z	NO PULL	20
AB21	PE16	GPIO	I/O	Z	NO PULL	20
W22	PE17	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name®	Default Function®	Type®	Reset State®	Default Pull Up/Down®	Buffer Strength® (mA)
U18	VCC-PE	POWER	P	-	-	-
GPIO F						
AB10	PF0	GPIO	I/O	JTAG_MS	NO PULL	20
W13	PF1	GPIO	I/O	JTAG_DI	NO PULL	20
AC8	PF2	GPIO	I/O	Z	NO PULL	20
W9	PF3	GPIO	I/O	JTAG_DO	NO PULL	20
AB6	PF4	GPIO	I/O	Z	NO PULL	20
AB9	PF5	GPIO	I/O	JTAG_CK	NO PULL	20
AB8	PF6	GPIO	I/O	Z	NO PULL	20
GPIO G						
V21	PG0	GPIO	I/O	Z	NO PULL	20
U20	PG1	GPIO	I/O	Z	NO PULL	20
U19	PG2	GPIO	I/O	Z	NO PULL	20
V22	PG3	GPIO	I/O	Z	NO PULL	20
Y21	PG4	GPIO	I/O	Z	NO PULL	20
W23	PG5	GPIO	I/O	Z	NO PULL	20
AB17	PG6	GPIO	I/O	Z	NO PULL	20
U23	PG7	GPIO	I/O	Z	NO PULL	20
AC17	PG8	GPIO	I/O	Z	NO PULL	20
U21	PG9	GPIO	I/O	Z	NO PULL	20
AB19	PG10	GPIO	I/O	Z	NO PULL	20
AB18	PG11	GPIO	I/O	Z	NO PULL	20
AC19	PG12	GPIO	I/O	Z	NO PULL	20
U22	PG13	GPIO	I/O	Z	NO PULL	20
T17	VCC-PG	POWER	P	-	-	-
GPIO H						
W11	PH0	GPIO	I/O	Z	NO PULL	20
AA10	PH1	GPIO	I/O	Z	NO PULL	20
AC4	PH2	GPIO	I/O	Z	NO PULL	20
AA9	PH3	GPIO	I/O	Z	NO PULL	20
AB5	PH4	GPIO	I/O	Z	NO PULL	20
AC7	PH5	GPIO	I/O	Z	NO PULL	20
AB4	PH6	GPIO	I/O	Z	NO PULL	20
AC5	PH7	GPIO	I/O	Z	NO PULL	20
Y10	PH8	GPIO	I/O	Z	NO PULL	20
AA8	PH9	GPIO	I/O	Z	NO PULL	20
Y8	PH10	GPIO	I/O	Z	NO PULL	20
AA5	PH11	GPIO	I/O	Z	NO PULL	20
GPIO L						
D17	PL0	GPIO	I/O	Z	NO PULL	20
C17	PL1	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name©	Default Function©	Type©	Reset State©	Default Pull Up/Down©	Buffer Strength© (mA)
A19	PL2	GPIO	I/O	Z	NO PULL	20
E19	PL3	GPIO	I/O	Z	NO PULL	20
A20	PL4	GPIO	I/O	Z	NO PULL	20
D19	PL5	GPIO	I/O	Z	NO PULL	20
B20	PL6	GPIO	I/O	Z	NO PULL	20
C19	PL7	GPIO	I/O	Z	NO PULL	20
B21	PL8	GPIO	I/O	Z	NO PULL	20
D20	PL9	GPIO	I/O	Z	NO PULL	20
D21	PL10	GPIO	I/O	Z	NO PULL	20
C20	PL11	GPIO	I/O	Z	NO PULL	20
D22	PL12	GPIO	I/O	Z	NO PULL	20
J16	VCC-PL	POWER	P	-	-	-
System Control						
G18	NMI	-	I	OD	NO PULL	-
E17	RESET	-	I	-	NO PULL	-
H14	TEST	-	I	-	PULL DOWN	-
F17	FEL	-	I	-	-	-
K22	X24MIN	-	A	-	-	-
K23	X24MOUT	-	A	-	-	-
LRADC						
A16	KEYADC	-	A	-	-	-
DEBUG						
AA11	JTAG-SEL0	-	A	-	-	-
AA12	JTAG-SEL1	-	A	-	-	-
HDMI						
F21	HCEC	-	A	-	-	-
E21	HHPD	-	A	-	-	-
E20	HSDA	-	A	-	-	-
G21	HSCL	-	A	-	-	-
G23	HTX0N	-	A	-	-	-
G22	HTX0P	-	A	-	-	-
F22	HTX1N	-	A	-	-	-
E23	HTX1P	-	A	-	-	-
E22	HTX2N	-	A	-	-	-
D23	HTX2P	-	A	-	-	-
H23	HTXCN	-	A	-	-	-
H22	HTXCP	-	A	-	-	-
M16	HVCC	-	P	-	-	-
MIPI DSI						
P23	MDSI-CKN	-	A	-	-	-
N23	MDSI-CKP	-	A	-	-	-

Ball#	Pin Name®	Default Function®	Type®	Reset State®	Default Pull Up/Down®	Buffer Strength® (mA)
T23	MDSI-D0N	-	A	-	-	-
T22	MDSI-D0P	-	A	-	-	-
R22	MDSI-D1N	-	A	-	-	-
P22	MDSI-D1P	-	A	-	-	-
N22	MDSI-D2N	-	A	-	-	-
M22	MDSI-D2P	-	A	-	-	-
L22	MDSI-D3N	-	A	-	-	-
L23	MDSI-D3P	-	A	-	-	-
N19	VCC-MDSI	-	P	-	-	-
USB						
B22	USB0-DM	-	A	-	-	-
A22	USB0-DP	-	A	-	-	-
C22	USB1-DM	-	A	-	-	-
B23	USB1-DP	-	A	-	-	-
L16	VCC-USB	-	P	-	-	-
HSIC						
G19	HSIC-DAT	-	A	-	-	-
H19	HSIC-STR	-	A	-	-	-
K16	VCC-HSIC	-	P	-	-	-
AUDIO_CODEC						
A11	AGND	-	G	-	-	-
G14	AVCC	-	P	-	-	-
E10	CPN	-	A	-	-	-
E11	CPP	-	A		-	-
E13	CPVDD	-	P	-	-	-
F12	CPVEE	-	P	-	-	-
G13	VEE		P			
A13	EAROUTN	-	A	-	-	-
B13	EAROUTP	-	A	-	-	-
D13	HBIAS	-	A	-	-	-
D11	HP-DET	-	A	-	-	-
C10	HP-FB	-	A	-	-	-
C13	HPOUTL	-	A			
C12	HPOUTR	-	A	-	-	-
B14	LINEINL		A	-	-	-
A14	LINEINR		A	-	-	-
C16	LINEOUTN/R	-	A	-	-	-
D16	LINEOUTP/L	-	A	-	-	-
E14	MBIAS	-	A	-	-	-
B10	MIC-DET	-	A	-	-	-
B16	MICIN1N	-	A	-	-	-

Ball#	Pin Name°	Default Function°	Type°	Reset State°	Default Pull Up/Down°	Buffer Strength° (mA)
B15	MICIN1P	-	A	-	-	-
A17	MICIN2N	-	A	-	-	-
B17	MICIN2P	-	A	-	-	-
C14	PHONEINN	-	A	-	-	-
D14	PHONEINP	-	A	-	-	-
F16	PHONEOUTN	-	A	-	-	-
E16	PHONEOUTP	-	A	-	-	-
B12	VRA1	-	A	-	-	-
B11	VRA2	-	A	-	-	-
C11	VRP	-	A	-	-	-
RTC						
G16	RTC-VIO	-	P	-	-	-
C18	X32KIN	-	A	-	-	-
B19	X32KOUT	-	A	-	-	-
B18	X32KFOUT	-	A	-	-	-
H16	VCC-RTC	-	P	-	-	-
Other						
T6	VDD-CPUXFB	-	O	-	-	-
P16	VDD-EFUSEBP	-	O	-	-	-
Power						
T14,U15	VCC-IO	-	P	-	-	-
N16	VCC-PLL	-	P	-	-	-
N18	VDD-EFUSE	-	P	-	-	-
U6,V2,V3,V4,V5,V6,W1,W3,W4,W5,Y2,Y3,Y4,AA1,AA3,AB2,AC1,AC2	VDD-CPUX	-	P	-	-	-
H15	VDD-CPUS	-	P	-	-	-
J12,J13,K14,L13,L14,M13,M14,N14,P14,R13,R14,T15	VDD-SYS	-	P	-	-	-
AC23,C3,C7,D7,G11,G6,H13,H4,J10,J11,J14,J15,J9,K10,K11,K12,K13,K8,K9,L10,L11,L12,L15,L4,L5,L9,M10,M11,M12,M15,M3,M8,M9,N10,N11,N12,N13,N15,N4,N9,P10,P11,P12,P13,P7,P8,P9,R10,R11,R12,R15,R5,R6,R7,R8,R9,T10,T11,T12,T13,T8,T9,U11,U12,U2,U5,U7,U8,U9,V14,V8	GND	-	G	-	-	-

Notes:

1) **Default Function** defines the default function of each pin, especially for pins with multiplexing functions;

2) **Type** defines the signal direction: I (Input), O (Output), I/O(Input / Output), OD(Open-Drain),A (Analog), AI(Analog Input),AO(Analog Output),A I/O(Analog Input /Output),P (Power), G (Ground);

3) **Reset State** defines the state of the terminal at reset: Z for high-impedance；

4) **Default Pull Up/Down** defines the presence of an internal pull up or pull down resister. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

5) **Buffer Strength** defines drive strength of the associated output buffer.

4.2. GPIO Multiplexing Functions

Table 4-2 provides a description of the A64 GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function 2	Function3	Function 4	Function 5	Function 6
PB0	GPIO	I/O	DIS	Z	UART2_TX	-	JTAG_MS0	-	PB_EINT0
PB1		I/O	DIS	Z	UART2_RX	-	JTAG_CK0	SIM_PWREN	PB_EINT1
PB2		I/O	DIS	Z	UART2_RTS	-	JTAG0_DO0	SIM_VPPEN	PB_EINT2
PB3		I/O	DIS	Z	UART2_CTS	I2S0_MCLK	JTAG_DI0	SIM_VPPPP	PB_EINT3
PB4		I/O	DIS	Z	AIF2_SYNC	PCM0_SYNC	-	SIM_CLK	PB_EINT4
PB5		I/O	DIS	Z	AIF2_BCLK	PCM0_BCLK	-	SIM_DATA	PB_EINT5
PB6		I/O	DIS	Z	AIF2_DOUT	PCM0_DOUT	-	SIM_RST	PB_EINT6
PB7		I/O	DIS	Z	AIF2_DIN	PCM0_DIN	-	SIM_DET	PB_EINT7
PB8		I/O	DIS	Z	-	-	UART0_TX	-	PB_EINT8
PB9		I/O	DIS	Z	-	-	UART0_RX	-	PB_EINT9
PC0	GPIO	I/O	DIS	Z	NAND_WE	-	SPI0_MOSI	-	-
PC1		I/O	DIS	Z	NAND_ALE	SDC2_DS	SPI0_MISO	-	-
PC2		I/O	DIS	Z	NAND_CLE	-	SPI0_CLK	-	-
PC3		I/O	DIS	Pull-Up	NAND_CE1	-	SPI0_CS	-	-
PC4		I/O	DIS	Pull-Up	NAND_CE0	-	-	-	-
PC5		I/O	DIS	Z	NAND_RE	SDC2_CLK	-	-	-
PC6		I/O	DIS	Pull-Up	NAND_RB0	SDC2_CMD	-	-	-
PC7		I/O	DIS	Pull-Up	NAND_RB1	-	-	-	-
PC8		I/O	DIS	Z	NAND_DQ0	SDC2_D0	-	-	-
PC9		I/O	DIS	Z	NAND_DQ1	SDC2_D1	-	-	-
PC10		I/O	DIS	Z	NAND_DQ2	SDC2_D2	-	-	-
PC11		I/O	DIS	Z	NAND_DQ3	SDC2_D3	-	-	-
PC12		I/O	DIS	Z	NAND_DQ4	SDC2_D4	-	-	-
PC13		I/O	DIS	Z	NAND_DQ5	SDC2_D5	-	-	-
PC14		I/O	DIS	Z	NAND_DQ6	SDC2_D6	-	-	-
PC15		I/O	DIS	Z	NAND_DQ7	SDC2_D7	-	-	-
PC16		I/O	DIS	Z	NAND_DQS	SDC2_RST	-	-	-
PD0	GPIO	I/O	DIS	Z	LCD_D2	UART3_TX	SPI1_CS	CCIR_CLK	-
PD1		I/O	DIS	Z	LCD_D3	UART3_RX	SPI1_CLK	CCIR_DE	-
PD2		I/O	DIS	Z	LCD_D4	UART4_TX	SPI1_MOSI	CCIR_HSYNC	-
PD3		I/O	DIS	Z	LCD_D5	UART4_RX	SPI1_MISO	CCIR_VSYNC	-
PD4		I/O	DIS	Z	LCD_D6	UART4_RTS	-	CCIR_D0	-
PD5		I/O	DIS	Z	LCD_D7	UART4_CTS	-	CCIR_D1	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/down	Function 2	Function3	Function 4	Function 5	Function 6
PD6		I/O	DIS	Z	LCD_D10	-	-	CCIR_D2	-
PD7		I/O	DIS	Z	LCD_D11	-	-	CCIR_D3	-
PD8		I/O	DIS	Z	LCD_D12	-	RGMII_RXD3 /RMII_NULL	CCIR_D4	-
PD9		I/O	DIS	Z	LCD_D13	-	RGMII_RXD2 / RMII_NULL	CCIR_D5	-
PD10		I/O	DIS	Z	LCD_D14	-	RGMII_RXD1 / RMII_RXD1	-	-
PD11		I/O	DIS	Z	LCD_D15	-	RGMII_RXD0 / RMII_RXD0	-	-
PD12		I/O	DIS	Z	LCD_D18	LVDS_VP0	RGMII_RXCK /RMII_NULL	-	-
PD13		I/O	DIS	Z	LCD_D19	LVDS_VN0	RGMII_RXCTL/RMII_CRS_DV	-	-
PD14		I/O	DIS	Z	LCD_D20	LVDS_VP1	RGMII_NULL /RMII_RXER	-	-
PD15		I/O	DIS	Z	LCD_D21	LVDS_VN1	RGMII_TXD3 / RMII_NULL	CCIR_D6	-
PD16		I/O	DIS	Z	LCD_D22	LVDS_VP2	RGMII_TXD2 / RMII_NULL	CCIR_D7	-
PD17		I/O	DIS	Z	LCD_D23	LVDS_VN2	RGMII_TXD1 / RMII_TXD1	-	-
PD18		I/O	DIS	Z	LCD_CLK	LVDS_VPC	RGMII_TXD0 / RMII_TXD0	-	-
PD19		I/O	DIS	Z	LCD_DE	LVDS_VNC	RGMII_TXCK /RMII_TXCK	-	-
PD20		I/O	DIS	Z	LCD_HSYNC	LVDS_VP3	RGMII_TXCTL/RMII_TXEN	-	-
PD21		I/O	DIS	Z	LCD_VSYNC	LVDS_VN3	RGMII_CLKIN/RMII_NULL	-	-
PD22		I/O	DIS	Z	PWM0	-	MDC	-	-
PD23		I/O	DIS	Z	-	-	MDIO	-	-
PD24		I/O	DIS	Z	-	-	-	-	-
PE0		I/O	DIS	Z	CSI_PCLK	-	TS_CLK	-	-
PE1		I/O	DIS	Z	CSI_MCLK	-	TS_ERR	-	-
PE2		I/O	DIS	Z	CSI_HSYNC	-	TS_SYNC	-	-
PE3		I/O	DIS	Z	CSI_VSYNC	-	TS_DVLD	-	-
PE4		I/O	DIS	Z	CSI_D0	-	TS_D0	-	-
PE5		I/O	DIS	Z	CSI_D1	-	TS_D1	-	-
PE6		I/O	DIS	Z	CSI_D2	-	TS_D2	-	-
PE7	GPIO	I/O	DIS	Z	CSI_D3	-	TS_D3	-	-
PE8		I/O	DIS	Z	CSI_D4	-	TS_D4	-	-
PE9		I/O	DIS	Z	CSI_D5	-	TS_D5	-	-
PE10		I/O	DIS	Z	CSI_D6	-	TS_D6	-	-
PE11		I/O	DIS	Z	CSI_D7	-	TS_D7	-	-
PE12		I/O	DIS	Z	CSI_SCK	-	-	-	-
PE13		I/O	DIS	Z	CSI_SDA	-	-	-	-
PE14		I/O	DIS	Z	PLL_LOCK_DBG	TWI2_SCK	-	-	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/down	Function 2	Function3	Function 4	Function 5	Function 6
PE15		I/O	DIS	Z	-	TWI2_SDA	-	-	-
PE16		I/O	DIS	Z	-	-	-	-	-
PE17		I/O	DIS	Z	-	-	-	-	-
PF0		I/O	JTAG_MS	Z	SDC0_D1	JTAG_MS1	-	-	-
PF1		I/O	JTAG_DI	Z	SDC0_D0	JTAG_DI1	-	-	-
PF2		I/O	DIS	Z	SDC0_CLK	UART0_TX	-	-	-
PF3	GPIO	I/O	JTAG_DO	Z	SDC0_CMD	JTAG_DO1	-	-	-
PF4		I/O	DIS	Z	SDC0_D3	UART0_RX	-	-	-
PF5		I/O	JTAG_CK	Z	SDC0_D2	JTAG_CK1	-	-	-
PF6		I/O	DIS	Z	-	-	-	-	-
PG0		I/O	DIS	Z	SDC1_CLK	-	-	-	PG_EINT0
PG1		I/O	DIS	Z	SDC1_CMD	-	-	-	PG_EINT1
PG2		I/O	DIS	Z	SDC1_D0	-	-	-	PG_EINT2
PG3		I/O	DIS	Z	SDC1_D1	-	-	-	PG_EINT3
PG4		I/O	DIS	Z	SDC1_D2	-	-	-	PG_EINT4
PG5		I/O	DIS	Z	SDC1_D3	-	-	-	PG_EINT5
PG6	GPIO	I/O	DIS	Z	UART1_TX	-	-	-	PG_EINT6
PG7		I/O	DIS	Z	UART1_RX	-	-	-	PG_EINT7
PG8		I/O	DIS	Z	UART1_RTS	-	-	-	PG_EINT8
PG9		I/O	DIS	Z	UART1_CTS	-	-	-	PG_EINT9
PG10		I/O	DIS	Z	AIF3_SYNC	PCM1_SYNC	-	-	PG_EINT10
PG11		I/O	DIS	Z	AIF3_BCLK	PCM1_BCLK	-	-	PG_EINT11
PG12		I/O	DIS	Z	AIF3_DOUT	PCM1_DOUT	-	-	PG_EINT12
PG13		I/O	DIS	Z	AIF3_DIN	PCM1_DIN	-	-	PG_EINT13
PH0		I/O	DIS	Z	TWI0_SCK	-	-	-	PH_EINT0
PH1		I/O	DIS	Z	TWI0_SDA	-	-	-	PH_EINT1
PH2		I/O	DIS	Z	TWI1_SCK	-	-	-	PH_EINT2
PH3		I/O	DIS	Z	TWI1_SDA	-	-	-	PH_EINT3
PH4		I/O	DIS	Z	UART3_TX	-	-	-	PH_EINT4
PH5		I/O	DIS	Z	UART3_RX	-	-	-	PH_EINT5
PH6	GPIO	I/O	DIS	Z	UART3_RTS	-	-	-	PH_EINT6
PH7		I/O	DIS	Z	UART3_CTS	-	-	-	PH_EINT7
PH8		I/O	DIS	Z	OWA_OUT	-	-	-	PH_EINT8
PH9		I/O	DIS	Z	-	-	-	-	PH_EINT9
PH10		I/O	DIS	Z	MIC_CLK	-	-	-	PH_EINT10
PH11		I/O	DIS	Z	MIC_DATA	-	-	-	PH_EINT11
PL0		I/O	DIS	Pull-Up	S_RSB_SCK	S_TWI_SCK	-	-	S_PL_EINT0
PL1		I/O	DIS	Pull-Up	S_RSB_SDA	S_TWI_SDA	-	-	S_PL_EINT1
PL2	GPIO	I/O	DIS	Z	S_UART_TX	-	-	-	S_PL_EINT2
PL3		I/O	DIS	Z	S_UART_RX	-	-	-	S_PL_EINT3
PL4		I/O	DIS	Z	S_JTAG_MS	-	-	-	S_PL_EINT4

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/ down	Function 2	Function3	Function 4	Function 5	Function 6
PL5		I/O	DIS	Z	S_JTAG_CK	-	-	-	S_PL_EINT5
PL6		I/O	DIS	Z	S_JTAG_DO	-	-	-	S_PL_EINT6
PL7		I/O	DIS	Z	S_JTAG_DI	-	-	-	S_PL_EINT7
PL8		I/O	DIS	Z	S_TWI_CSK	-	-	-	S_PL_EINT8
PL9		I/O	DIS	Z	S_TWI_SDA	-	-	-	S_PL_EINT9
PL10		I/O	DIS	Z	S_PWM	-	-	-	S_PL_EINT10
PL11		I/O	DIS	Z	S_CIR_RX	-	-	-	S_PL_EINT11
PL12		I/O	DIS	Z	-	-	-	-	S_PL_EINT12

4.3. Detailed Pin/Signal Description

Table 4-3 shows the detailed function description of every pin/signal based on the different interface.

Table 4-3. Detailed Pin Description

Pin/Signal Name	Description	Type
DRAM		
DQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
DQS[3:0]	DRAM Active-high Bidirectional Data Strobes to the Memory Device	I/O
DQSB[3:0]	DRAM Active-low Bidirectional Data Strobes to the Memory Device	I/O
DQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
DCK	DRAM Active-high Clock Signal to the Memory Device	O
DCKB	DRAM Active-low Clock Signal to the Memory Device	O
DCKE[1:0]	DRAM Clock Enable Signal to the Memory Device for Two Chip Select	O
DA[15:0]	DRAM Address Signal to the Memory Device	O
DWE	DRAM Write Enable Strobe to the Memory Device	O
DCAS	DRAM Column Address Strobe to the Memory Device	O
DRAS	DRAM Row Address Strobe to the Memory Device	O
DCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
DBA[2:0]	DRAM Bank Address Signal to the Memory Device	O
DODT[1:0]	DRAM On-Die Termination Output Signal for Two Chip Select	O
DRST	DRAM Reset Signal to the Memory Device	O
DZQ	DRAM ZQ Calibration	A
DVREF	DRAM Reference Voltage Input	P
VCC-DRAM	DRAM Power Supply	P
System Control		
FEL	UBOOT	I
TEST	TEST Signal	I
NMI	Non-Maskable Interrupt	I
RESET	RESET Signal	I
JTAG-SEL0	JTAG Mode Select	I
JTAG-SEL1	JTAG Mode Select	I
X24MIN	Clock Input Of 24MHz Crystal	AI

Pin/Signal Name	Description	Type
X24MOUT	Clock Output Of 24MHz Crystal	AO
VCC-PLL	PLL Power Supply	P
RTC&PLL		
RTC-VIO	Internal LDO Output Bypass	P
X32KIN	Clock input of 32768Hz Crystal	AI
X32KOUT	Clock output of 32768Hz Crystal	AO
X32KFOUT	Clock output of LOSC	OD
VCC-RTC	RTC Power Supply	P
USB		
USB0-DM	USB data signal DM	A I/O
USB0-DP	USB data signal DP	A I/O
USB1-DM	USB data signal DM	A I/O
USB1-DP	USB data signal DP	A I/O
VCC-USB	USB Power Supply	P
HSIC		
HSIC-DAT	USB HSIC Data Signal	A I/O
HSIC-STR	USB HSIC Strobe Signal	A I/O
VCC-HSIC	USB HSIC Power Supply	P
ADC		
KEYADC	ADC input for key	AI
AUDIO CODEC		
LINEINL	LINE-IN Left Channel Input	AI
LINEINR	LINE-IN Right Channel Input	AI
LINEOUTP/L	LINE-OUT Left Channel Output	AO
LINEOUTN/R	LINE-OUT Right Channel Output	AO
EAROUTP	Earpiece Amplifier Positive Differential Output	AO
EAROUTN	Earpiece Amplifier Negative Differential Output	AO
MIC_DET	Headphone MIC Detect	AI
HBIAS	Master Analog Headphone Bias Voltage Output	AO
HPOUTL	Headphone Output Left Channel	AO
HPOUTR	Headphone Output Right Channel	AO
HP-DET	Headphone Detect	AI
MBIAS	Master Analog Microphone Bias Voltage Output	AO
MICIN1N	Microphone Negative Input 1	AI
MICIN1P	Microphone Positive Input 1	AI
MICIN2N	Microphone Negative Input2	AI
MICIN2P	Microphone Positive Input 2	AI
PHONEINP	Phone Positive Differential Input	AI
PHONEINN	Phone Negative Differential Input	AI
PHONEOUTN	Phone Positive Differential Output	AO
PHONEOUTP	Phone Negative Differential Output	AO
CPP	Charge Pump Flying-back Capacitor	AO
CPN	Charge Pump Flying-back Capacitor	AO

Pin/Signal Name	Description	Type
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
CPVDD	Analog Power for Headphone Charge Pump	P
CPVEE	Charge Pump Negative Voltage Output	P
VEE	PA Negative Voltage Input	P
HP-FB	Headphone Common Reference Feedback Input	AI
SD /MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O
SDC1_CMD	Command Signal for SDIO WIFI	I/O
SDC1_CLK	Clock for SDIO WIFI	O
SDC1_D[3:0]	Data Input and Output for SDIO WIFI	I/O
SDC2_CMD	Command Signal for SD/eMMC	I/O
SDC2_CLK	Clock for SD/eMMC	O
SDC2_D[7:0]	Data Input and Output for SD/eMMC	I/O
SDC2_RST	Reset Signal for SD/eMMC	O
SDC2_DS	Data Strobe for SD/eMMC	I/O
NAND		
NAND_DQ[7:0]	Nand Flash Data Bit	I/O
NAND_WE	Nand Flash Write Enable	O
NAND_ALE	Nand Flash Address Latch Enable	O
NAND_CLE	Nand Flash Command Latch Enable	O
NAND_CE1	Nand Flash Chip Select	O
NAND_CE0	Nand Flash Chip Select	O
NAND_RE	Nand Flash Read Enable	O
NAND_RB0	Nand Flash Ready/Busy Bit	I
NAND_RB1	Nand Flash Ready/Busy Bit	I
NAND_DQS	Nand Flash Data Strobe	I/O
I2S/PCM		
I2S0_MCLK	I2S Master Clock	O
PCM0_SYNC	I2S/PCM Sample Rate Clock/Sync	I/O
PCM0_BCLK	I2S/PCM Sample Rate Clock	I/O
PCM0_DOUT	I2S/PCM Serial Data Output	O
PCM0_DIN	I2S/PCM Serial Data Input	I
PCM1_SYNC	I2S/PCM Sample Rate Clock/Sync	I/O
PCM1_BCLK	I2S/PCM Sample Rate Clock	I/O
PCM1_DOUT	I2S/PCM Serial Data Output	O
PCM1_DIN	I2S/PCM Serial Data Input	I
OWA		

Pin/Signal Name	Description	Type
OWA_OUT	One Wire Audio Output	O
SIM Card		
SIM_PWREN	SIM Card Power Enable	O
SIM_VPPEN	SIM Card Programming Voltage Enable	O
SIM_VPPPP	SIM Card Power Voltage	P
SIM_CLK	SIM Card Clock	O
SIM_DATA	SIM Card Serial Data Input/Output	I/O
SIM_RST	SIM Card Reset Signal	O
SIM_DET	SIM Card Detect	O
Interrupt		
PB_EINT[9:0]	GPIO B Interrupt	I
PG_EINT[13:0]	GPIO G Interrupt	I
PH_EINT[11:0]	GPIO H Interrupt	I
PWM		
PWM0	Pulse Width Modulation output channel0	O
S_PWM	Pulse Width Modulation output channel for CPUs	O
CIR		
S_CIR_RX	IR Data Receive	I
LCD		
LCD_D2	LCD Data Output	O
LCD_D3	LCD Data Output	O
LCD_D4	LCD Data Output	O
LCD_D5	LCD Data Output	O
LCD_D6	LCD Data Output	O
LCD_D7	LCD Data Output	O
LCD_D10	LCD Data Output	O
LCD_D11	LCD Data Output	O
LCD_D12	LCD Data Output	O
LCD_D13	LCD Data Output	O
LCD_D14	LCD Data Output	O
LCD_D15	LCD Data Output	O
LCD_D18	LCD Data Output	O
LCD_D19	LCD Data Output	O
LCD_D20	LCD Data Output	O
LCD_D21	LCD Data Output	O
LCD_D22	LCD Data Output	O
LCD_D23	LCD Data Output	O
LCD_CLK	LCD Clock Signal	O
LCD_DE	LCD Data Enable	O
LCD_HSYNC	LCD Horizontal SYNC	O
LCD_VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS_VP[3:0]	LVDS Data Positive Signal Output	AO

Pin/Signal Name	Description	Type
LVDS_VN[3:0]	LVDS Data Negative Signal Output	AO
LVDS_VPC	LVDS Clock Positive Signal Output	AO
LVDS_VNC	LVDS Clock Negative Signal Output	AO
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[7:0]	CSI Data Input	I
CSI_SCK	CSI Command Serial Clock Signal	I/O
CSI_SDA	CSI Command Serial Data Signal	I/O
MIPI_DSI		
MDSI-CKN	MIPI DSI Negative Differential Clock Line	AO
MDSI-CKP	MIPI DSI Positive Differential Clock Line	AO
MDSI-D0N	MIPI DSI Negative Differential Data Line0	AIO
MDSI-D0P	MIPI DSI Positive Differential Data Line0	AIO
MDSI-D1N	MIPI DSI Negative Differential Data Line1	AO
MDSI-D1P	MIPI DSI Positive Differential Data Line1	AO
MDSI-D2N	MIPI DSI Negative Differential Data Line2	AO
MDSI-D2P	MIPI DSI Positive Differential Data Line2	AO
MDSI-D3N	MIPI DSI Negative Differential Data Line3	AO
MDSI-D3P	MIPI DSI Positive Differential Data Line3	AO
VCC-MDSI	MIPI DSI Power Supply	P
HDMI		
HTX0P	HDMI Positive Differential Data Line0	AO
HTX0N	HDMI Negative Differential Data Line0	AO
HTX1P	HDMI Positive Differential Data Line1	AO
HTX1N	HDMI Negative Differential Data Line1	AO
HTX2P	HDMI Positive Differential Data Line2	AO
HTX2N	HDMI Negative Differential Data Line2	AO
HTXCP	HDMI Positive Differential Clock Line	AO
HTXCN	HDMI Negative Differential Clock Line	AO
HHPD	HDMI Hot Plug Detection	I/O
HCEC	HDMI CEC	I/O
HSDA	HDMI DDC Data	O
HSCL	HDMI DDC Clock	O
HVCC	HDMI Power Supply	P
EMAC		
RGMII_RXD3 /RMII_NULL	RGMII Receive Data	I
RGMII_RXD2 / RMII_NULL	RGMII Receive Data	I
RGMII_RXD1 / RMII_RXD1	RGMII /RMII Receive Data	I
RGMII_RXD0 / RMII_RXD0	RGMII/RMII Receive Data	I

Pin/Signal Name	Description	Type
RGMII_RXCK / RMII_NULL	RGMII Receive Clock	I
RGMII_RXCTL / RMII_CRS_DV	RGMII Receive Control /RMII Carrier Sense-Receive Data Valid	I
RGMII_NULL / RMII_RXER	RMII Receive Error	I
RGMII_TXD3 / RMII_NULL	RGMII Transmit Data	O
RGMII_TXD2 / RMII_NULL	RGMII Transmit Data	O
RGMII_TXD1 / RMII_TXD1	RGMII /RMII Transmit Data	O
RGMII_TXD0 / RMII_TXD0	RGMII /RMII Transmit Data	O
RGMII_TXCK / RMII_TXCK	RGMII /RMII Transmit Clock: Output Pin for RGMII, Input Pin for RMII	I/O
RGMII_TXCTL / RMII_TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII_CLKIN / RMII_NULL	RGMII Transmit Clock from External	I
MDC	RGMII /RMII Management Data Clock	O
MDIO	RGMII /RMII Management Data Input/Output	I/O
TS		
TS_CLK	Transport Stream Clock	I
TS_ERR	Transport Stream Error Indicate	I
TS_SYNC	Transport Stream SYNC	I
TS_DVLD	Transport Stream Valid Signal	I
TS_D[7:0]	Transport Stream Data Bit	I
SPI		
SPI0_CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI1_CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear to Send	I
UART1_RTS	UART1 Data Request to Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear to Send	I
UART2_RTS	UART2 Data Request to Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear to Send	I
UART3_RTS	UART3 Data Request to Send	O
UART4_TX	UART4 Data Transmit	O

Pin/Signal Name	Description	Type
UART4_RX	UART4 Data Receive	I
UART4_CTS	UART4 Data Clear to Send	I
UART4_RTS	UART4 Data Request to Send	O
S_UART_TX	UART Data Transmit for CPUs	O
S_UART_RX	UART Data Receive for CPUs	I
TWI		
TWI0_SCK	TWI0 Serial Clock Signal	I/O
TWI0_SDA	TWI0 Serial Data Signal	I/O
TWI1_SCK	TWI1 Serial Clock Signal	I/O
TWI1_SDA	TWI1 Serial Data Signal	I/O
TWI2_SCK	TWI2 Serial Clock Signal	I/O
TWI2_SDA	TWI2 Serial Data Signal	I/O
S_TWI_SCK	TWI Serial Clock Signal for CPUs	I/O
S_TWI_SDA	TWI Serial Data Signal for CPUs	I/O
JTAG		
JTAG_MS[1:0]	JTAG Mode Select	I
JTAG_CK[1:0]	JTAG Clock Signal	I
JTAG_DO[1:0]	JTAG Data Output	O
JTAG_DI[1:0]	JTAG Data Input	I
S_JTAG_MS	JTAG Mode Select	I
S_JTAG_CK	JTAG Clock Signal	I
S_JTAG_DO	JTAG Data Output	O
S_JTAG_DI	JTAG Data Input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. **Table 5-1** specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Note: All measurements in the A64 Datasheet are taken at room temperature of 25°C unless other noted.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$I_{I/O}$	In/Out current for input and output	-40	40	mA
AVCC	Power Supply for Analog part	-0.3	3.6	V
VCC-HSIC	Power Supply for HSIC	-0.3	1.4	V
CPVDD	Analog Power Supply for Headphone Charge Pump	-0.3	1.8	V
VCC-IO,VCC-PC, VCC-PD,VCC-PE, VCC-PG,VCC-PL	Power Supply for Port B,F,H Power Supply for Port C Power Supply for Port D Power Supply for Port E Power Supply for Port G Power Supply for Port L	-0.3	3.6	V
HVCC	Power Supply for HDMI	-0.3	3.3	V
VDD-EFUSE	Power Supply for Efuse	-0.3	3.6	V
VCC-PLL	Power Supply for system PLL	-0.3	3.6	V
VCC-MDSI	Power Supply for MIPI DSI	-0.3	3.6	V
VCC-RTC	Power Supply for RTC	-0.3	3.6	V
VCC-USB	Power Supply for USB	-0.3	3.6	V
VCC-DRAM	Power Supply for DRAM	-0.3	1.98	V
VDD-CPUX	Power Supply for CPU0~3	-0.3	1.4	V
VDD-CPUS	Power Supply for CPUs	-0.3	1.4	V
VDD-SYS	Power Supply for System	-0.3	1.4	V
T_{STG}	Storage Temperature	-40	125	°C

5.2. Recommended Operating Conditions

All A64 modules are used under the operating Conditions contained in **Table 5-2**.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
AVCC	Power Supply for Analog part	-	3.0	-	V
VCC-HSIC	Power Supply for HSIC	1.1	1.2	1.3	V

CPVDD	Analog Power Supply for Headphone Charge Pump	1.5	1.8	-	V
VCC-IO,VCC-PC, VCC-PD,VCC-PE, VCC-PG,VCC-PL	Digital GPIO(Port B,F,H,C,D,E,G,L)Power(3.3V/2.5V/1.8V)	3.0 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
HVCC	Power Supply for HDMI	-	3.3	-	V
VDD-EFUSE	Power Supply for Efuse	-	3.0	3.3	V
VCC-PLL	Power Supply for system PLL	2.7	3.0	3.3	V
VCC-MDSI	Power Supply for MIPI DSI	3.0	3.3	3.6	V
VCC-RTC	Power Supply for RTC	-	3.0	3.3	V
VCC-USB	Power Supply for USB	2.7	3.0	3.45	V
VCC-DRAM	Power Supply for DDR2	1.7	1.8	1.9	V
	Power Supply for DDR3	1.425	1.5	1.575	V
	Power Supply for DDR3L	1.283	1.35	1.45	V
	Power Supply for LPDDR2	1.14	1.2	1.3	V
	Power Supply for LPDDR3	1.14	1.2	1.3	V
VDD-CPUX	Power Supply for CPU0~3	1.04	1.1	1.3	V
VDD-CPUS	Power Supply for CPUs	1.0	1.1	1.3	V
VDD-SYS	Power Supply for System	1.0	1.1	1.2	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of A64.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

A64 contains two external input clocks:X24MIN and X32KIN, two output clocks:X24MOUT and X32KOUT.

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks,the clock is provided through X24MIN. **Table 5-4** lists the 24MHz crystal specifications.

Table 5-4. 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	24.000	–	MHz
t_{ST}	Startup Time	–	–	–	ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	300	uW
C_L	Equivalent Load capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	–	25	–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–	–	pF
C_{SHUT}	Shunt capacitance	5	6.5	7.5	pF
R_{BIAS}	Internal bias resistor	0.4	0.5	0.6	MΩ

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN.**Table 5-5** lists the 32768Hz crystal specifications.

Table 5-5. 32768Hz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	32768	–	Hz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
P_{ON}	Drive level	–	–	50	uW
C_L	Equivalent Load capacitance	–	–	–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–	–	–	pF
R_S	Series Resistance(ESR)	–	–	–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional capacitance	–	–	–	pF
C_{SHUT}	Shunt capacitance	–	–	–	pF
R_{BIAS}	Internal bias resistor	–	–	–	MΩ

5.5. Electrical Characteristics for Power Supply

Table 5-6 shows the peak power consumption of A64.

Table 5-6. Peak Power Consumption

Parameter	Sub Parameter	Power	Condition	MIN	TYP	MAX	Unit
Internal Core Power	CPU	VDD-CPUX	@1.1V, 816MHz	-	-	2000	mA
	SYS	VDD-SYS	@1.1V	-	-	TBD	mA
GPIO Power		VCC-IO VCC-PC VCC-PD VCC-PE VCC-PG	@3.3V @2.5V @1.8V	-	-	100	mA

	VCC-PL						
Memory I/O Power	VCC-DRAM	@1.5V	-	-	800	mA
Oscillator	VCC-PLL	@3.0V	-	-	TBD	mA
USB 3.0V Power of PHY	VCC-USB	@3.0V	-	-	80	mA
HSIC Power	VCC-HSIC	@1.2V	-	-	TBD	mA
RTC Power	VCC-RTC	@3.0V	-	-	1	mA
Analog Power for Headphone Charge Pump	CPVDD	@1.8V,0Data, 33ohm	-	-	2.5	mA
MIPI DSI Power	VCC-MDSI	@3.3V, 1Gbps 4lane	-	-	16.57	mA
HDMI Power	HVCC	@3.3V	-	-	40	mA
ADC Analog Power	AVCC	@3.0V	-	-	2.8	mA
DAC Analog Power	AVCC	@3.0V	-	-	1.35	mA
PLL Power	VCC-PLL	@3.0V	-	-	TBD	mA

5.6. Nand AC Electrical Characteristics
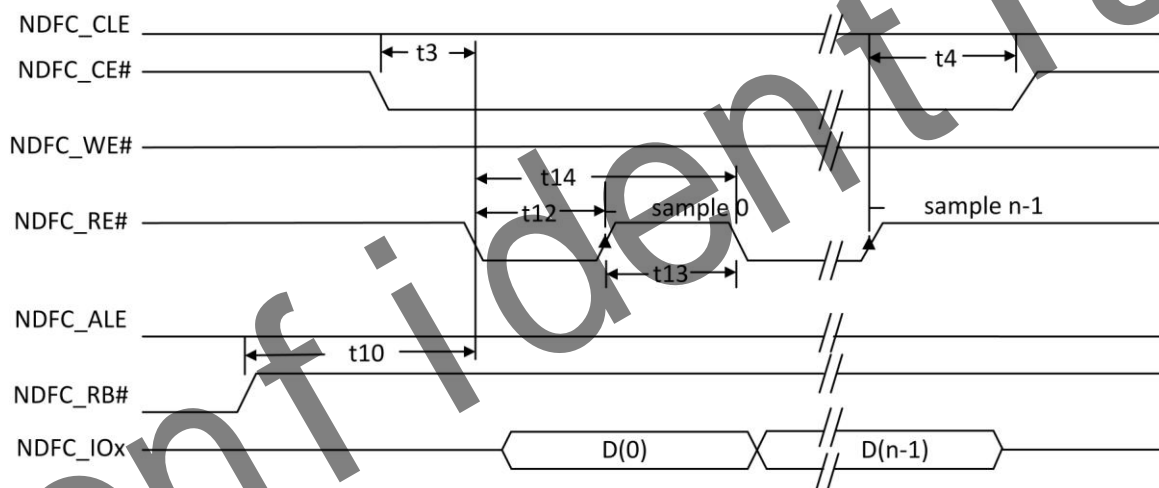
Figure 5-1. Conventional Serial Access Cycle Diagram (SAM0)
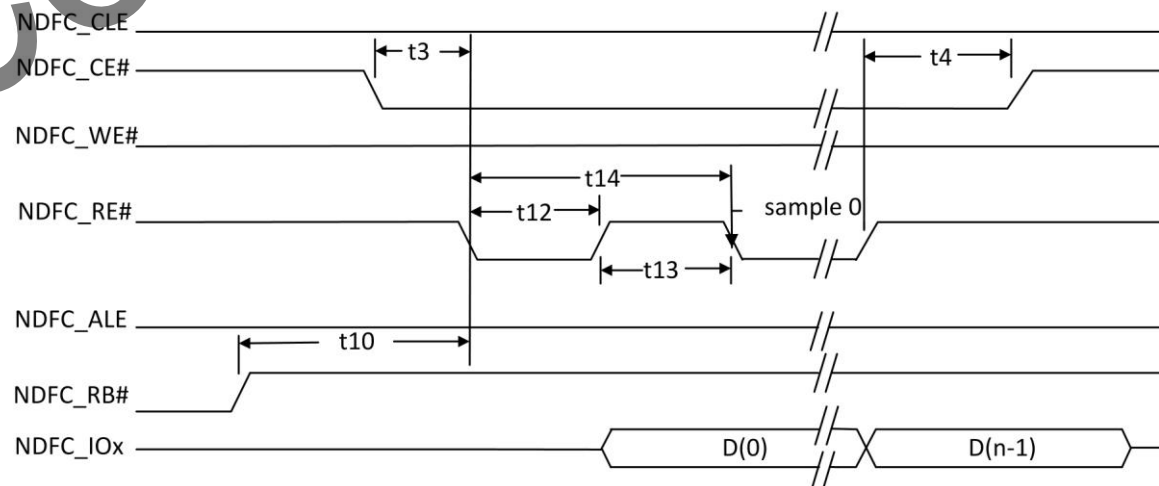
Figure 5-2. EDO type Serial Access after Read Cycle (SAM1)
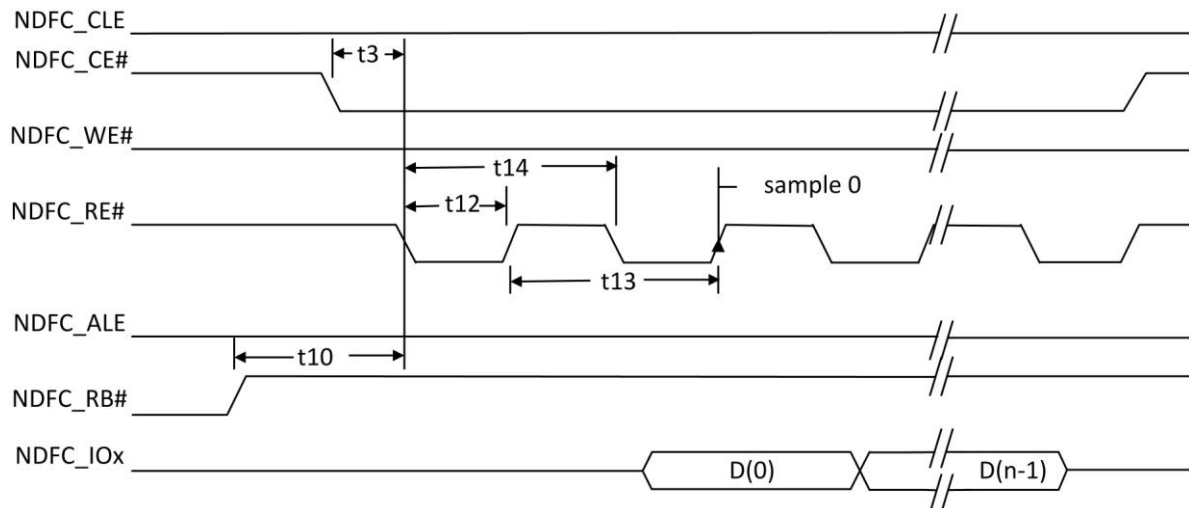
Figure 5-3. Extending EDO type Serial Access Mode (SAM2)
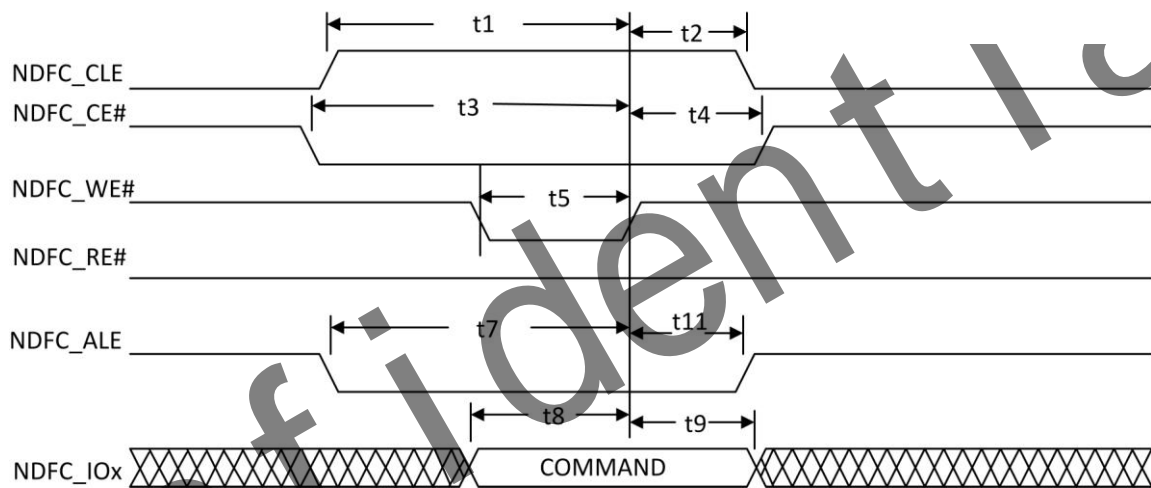
Figure 5-4. Command Latch Cycle
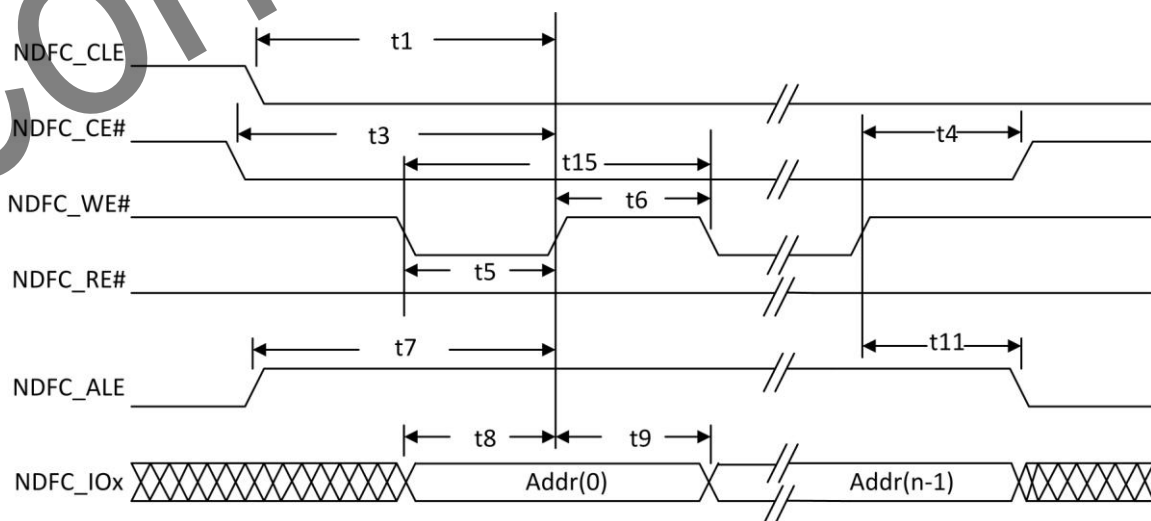
Figure 5-5. Address Latch Cycle
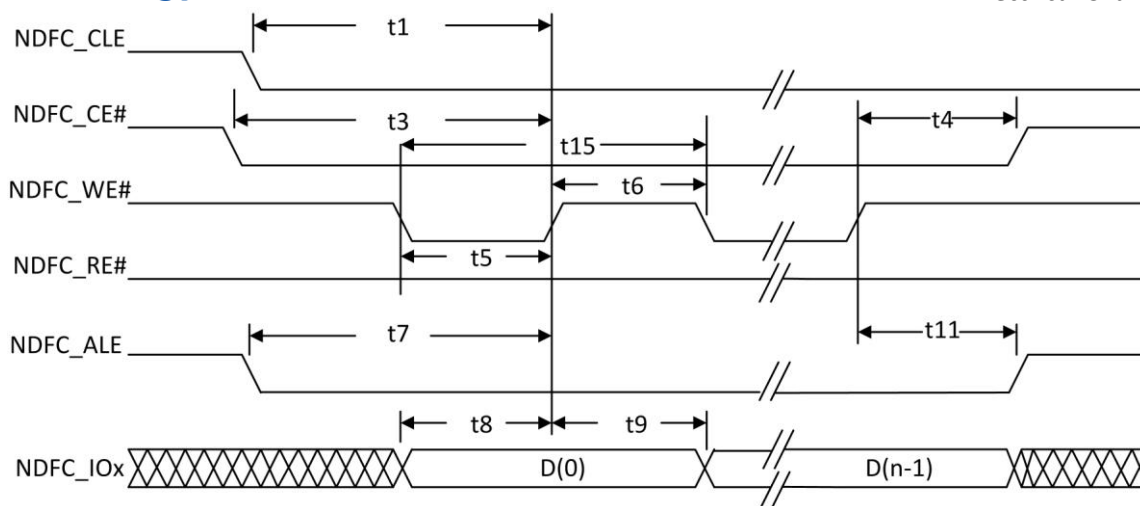
Figure 5-6. Write Data to Flash Cycle
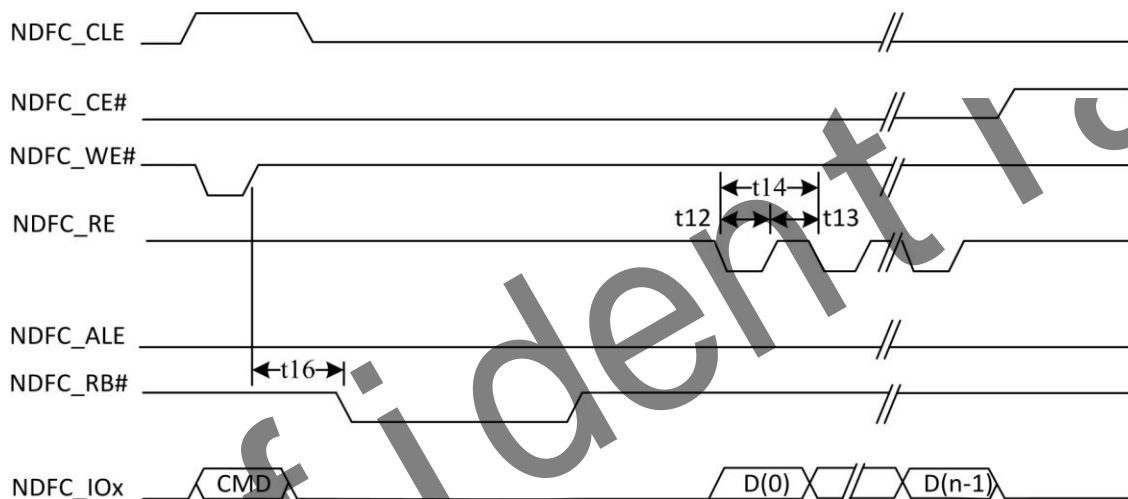
Figure 5-7. Waiting R/B# ready Diagram
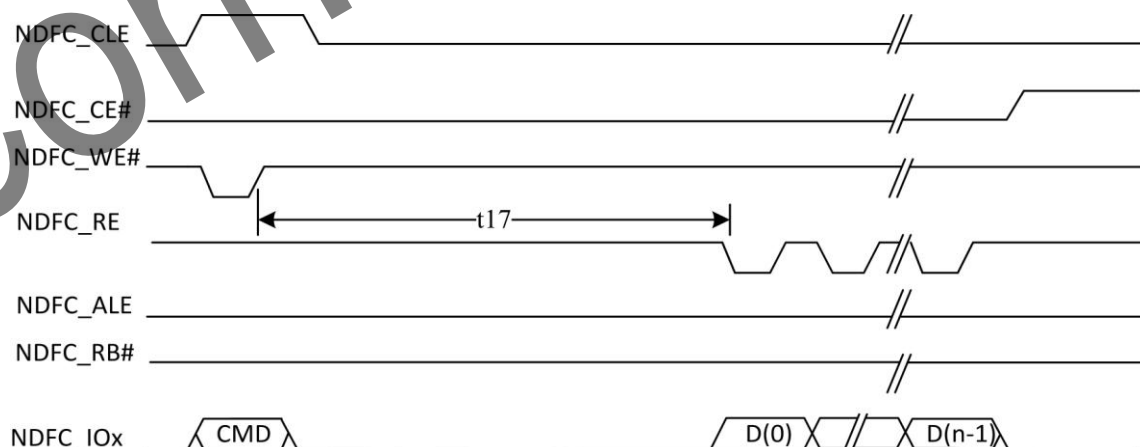
Figure 5-8. WE# high to RE# low Timing Diagram
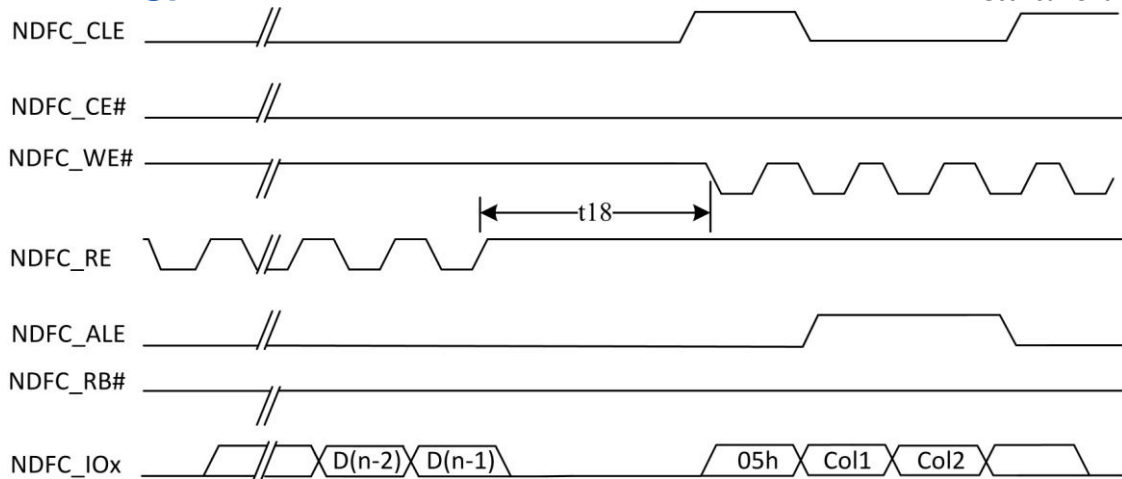
Figure 5-9. RE# high to WE# low Timing Diagram
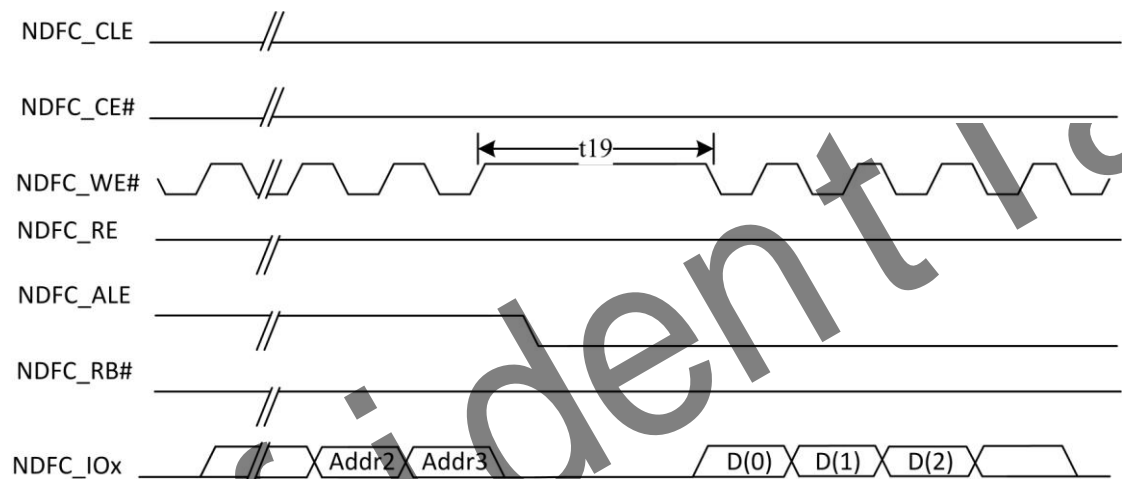
Figure 5-10. Address to Data Loading Timing Diagram

Table 5-7. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T[1]	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB[2]	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR[3]	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW[4]	ns

Address to Data Loading time	t19	T_ADL[5]			ns

NOTE (1):T is the cycle of clock.

NOTE (2),(3),(4),(5): This values is configurable in nand flash controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T.

5.7. SMHC AC Electrical Characteristics

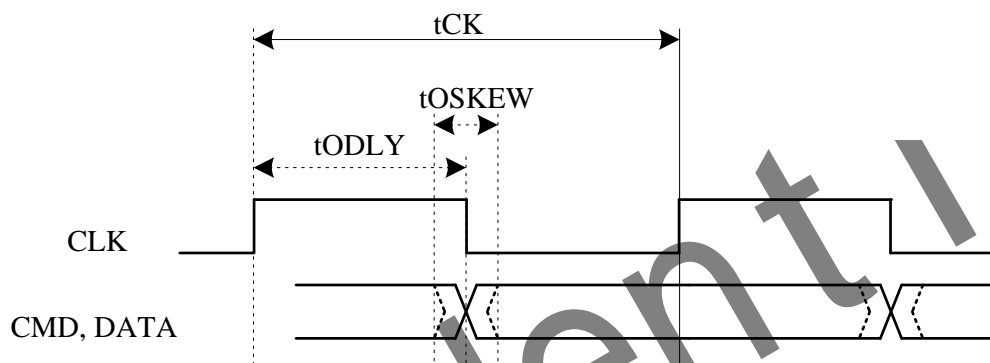### 5.7.1. SMHC0 AC Electrical Characteristics
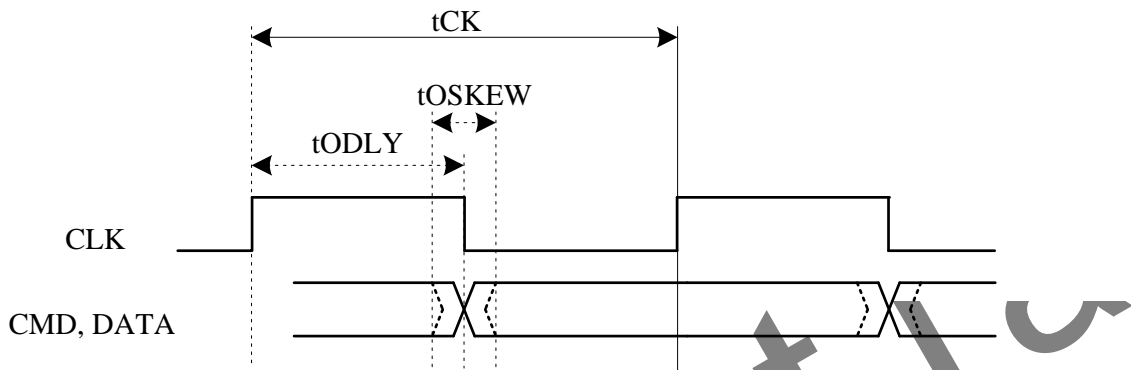
Figure 5-11. SMHC0 Output Timing Diagram in High-Speed Mode

Table 5-8. SMHC0 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.

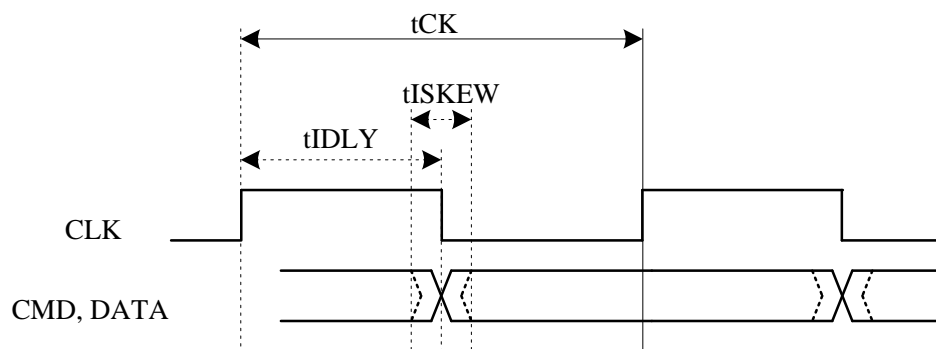(2).The GPIO's driver strength level is 2 for test.

Figure 5-12. SMHC0 Input Timing Diagram in High-Speed Mode

Table 5-9. SMHC0 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz

Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	1	ns

Note:

(1).The GPIO's driver strength level is 2 for test.

5.7.2. SMHC1 AC Electrical Characteristics

SDR Mode

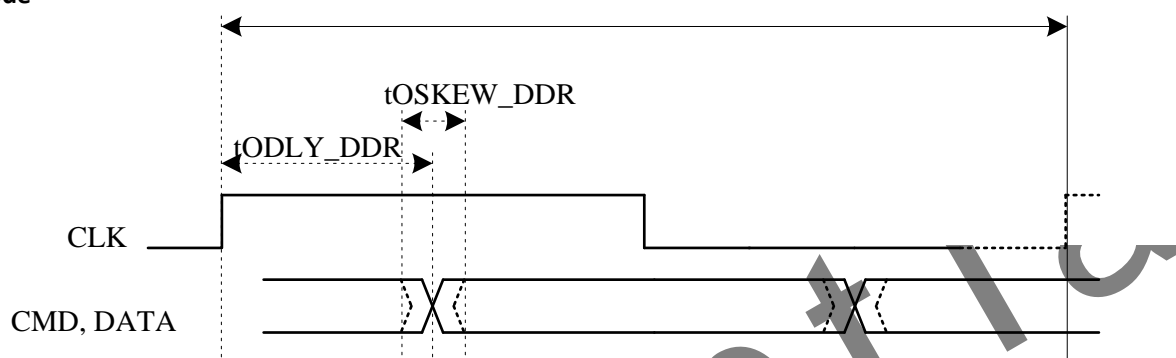It is used for DS,HS,SDR12,SDR25,SDR50,SDR104(<100MHz).

Figure 5-13. SMHC1 Output Timing Diagram in High-Speed Mode

Table 5-10. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.

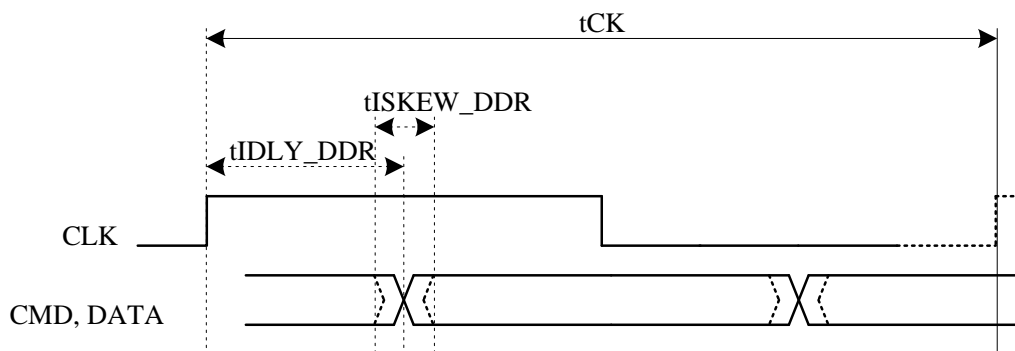(2).The GPIO's driver strength level is 2 for test.

Figure 5-14. SMHC1 Input Timing Diagram in High-Speed Mode

Table 5-11. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					

Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	1	ns

Note:

(1).The GPIO's driver strength level is 2 for test.

DDR50 Mode

Figure 5-15. SMHC1 Output Timing Diagram in HS-DDR Mode

Table 5-12. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.4	ns

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.

(2).The GPIO's driver strength level is 2 for test.

Figure 5-16. SMHC1 Input Timing Diagram in HS-DDR Mode

Table 5-13. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz

Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	7	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.4	ns

Note:

(1).The GPIO's driver strength level is 2 for test.

SDR104 Mode(>100MHz)
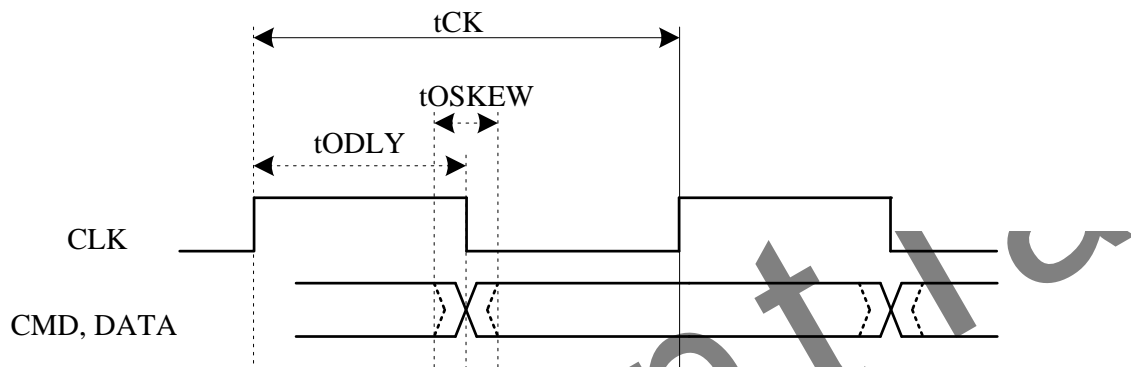
Figure 5-17. SMHC1 Output Timing Diagram in High-Speed Mode

Table 5-14. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.
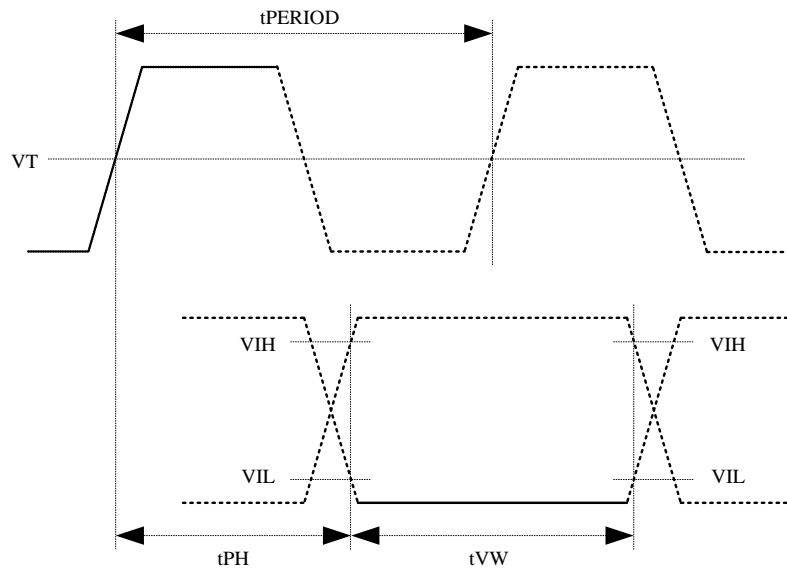(2).The GPIO's driver strength level is 2 for test.

Figure 5-18. SMHC1 Input Timing Diagram in High-Speed Mode

Table 5-15. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

(2).The GPIO's driver strength level is 3 for test.

(3).Temperature variation: -20°C.

(4).Temperature variation: 90°C.

5.7.3. SMHC2 AC Electrical Characteristics

HS-SDR/HS-DDR Mode

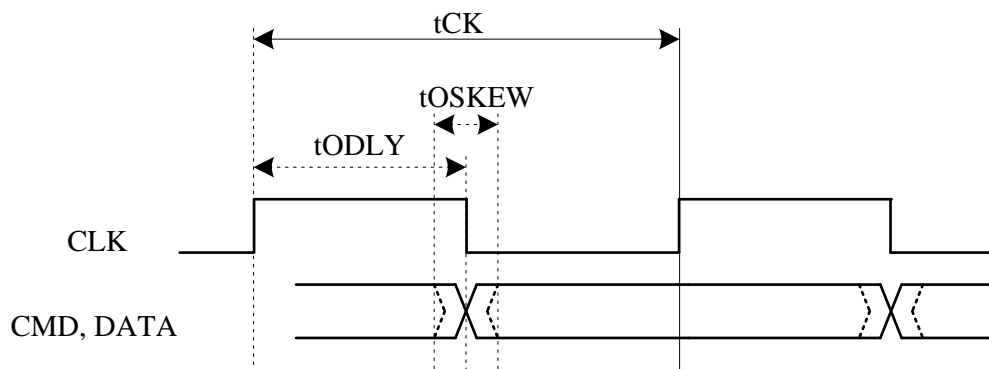The IO voltage is 1.8V or 3.0V.

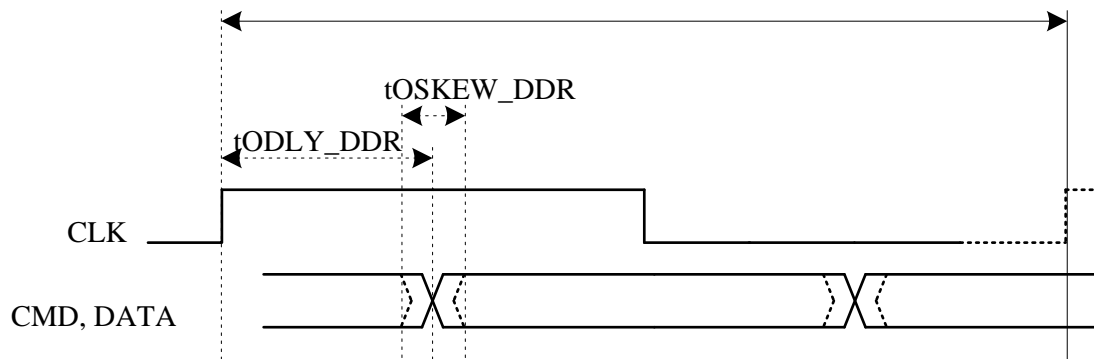Figure 5-19. SMHC2 Output Timing Diagram in HS-SDR Mode

Figure 5-20. SMHC2 Output Timing Diagram in HS-DDR Mode

Table 5-16. SMHC2 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.4	ns	

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz.
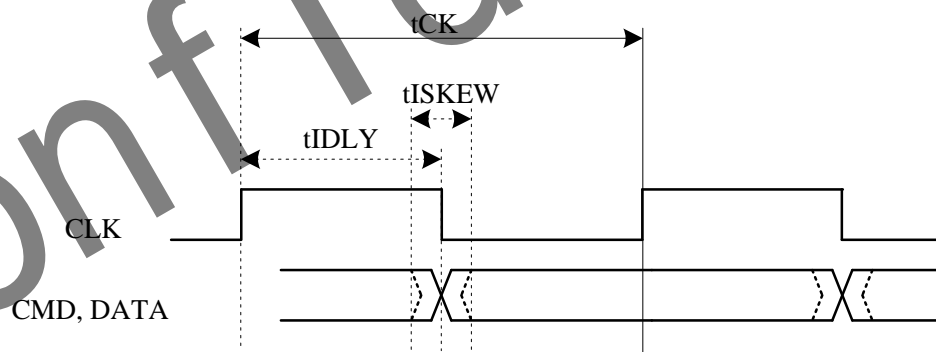
(2).The GPIO's driver strength level is 2 for test.
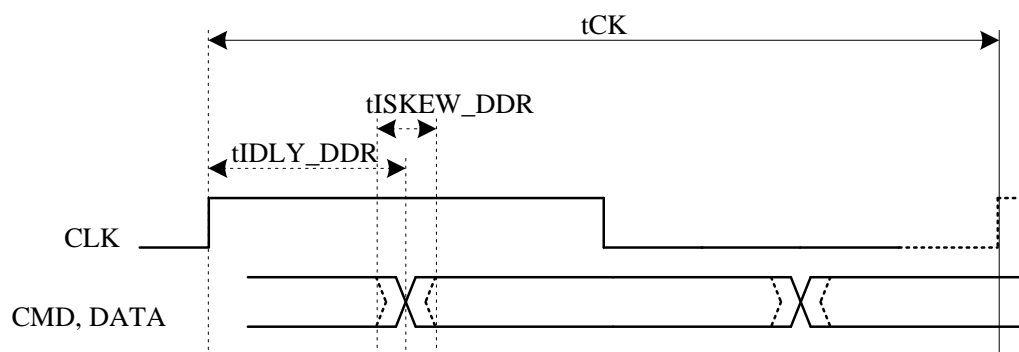

Figure 5-21. SMHC2 Input Timing Diagram in HS-SDR Mode

Figure 5-22.SMHC2 Input Timing Diagram in HS-DDR Mode

Table 5-17. SMHC2 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	21	ns	
Data input delay in DDR mode.It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8	ns	
Data input skew time in SDR mode	tISKEW	-	-	1.7	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.5	ns	

Note:

(1).The GPIO's driver strength level is 2 for test.

HS200 Mode
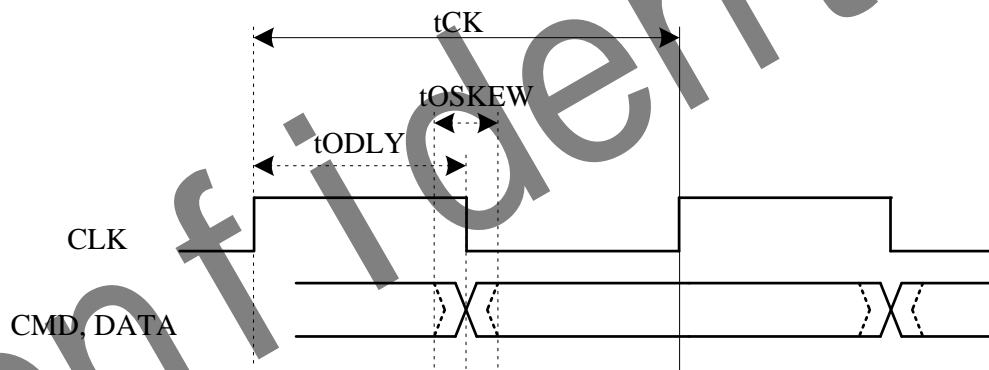
Figure 5-23. SMHC2 HS200 Output Timing Diagram

Table 5-18. SMHC2 HS200 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.4	ns	

Note:

(1).Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

(2).The GPIO's driver strength level is 3 for test.
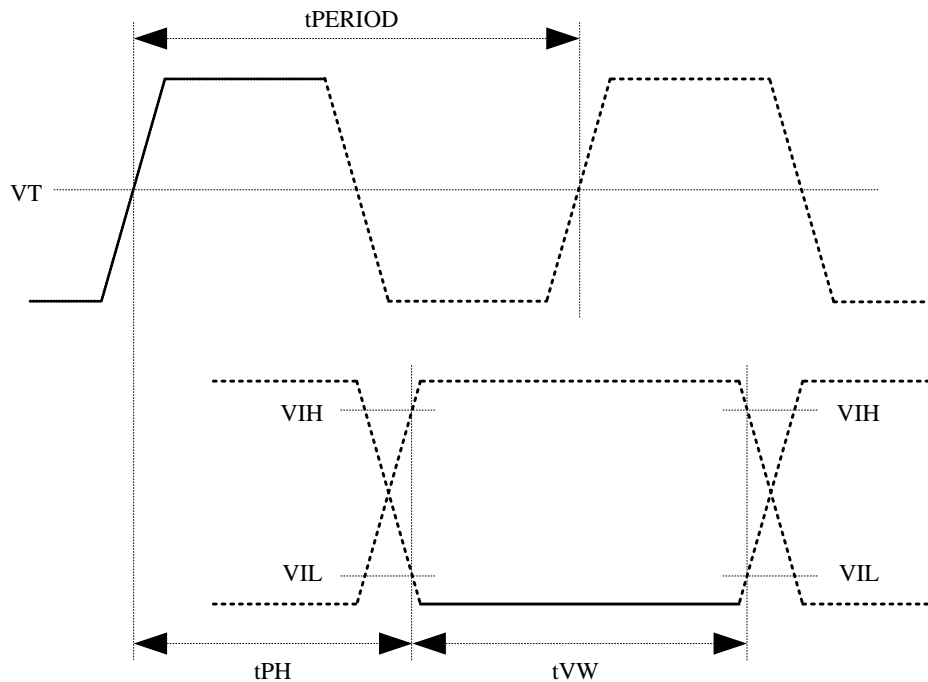
Figure 5-24. SMHC2 HS200 Input Timing Diagram

Table 5-19. SMHC2 HS200 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	

Note:
(1).Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.
(2).The GPIO's driver strength level is 3 for test.
(3).Temperature variation: -20°C.
(4).Temperature variation: 90°C.

HS400 Mode
The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.
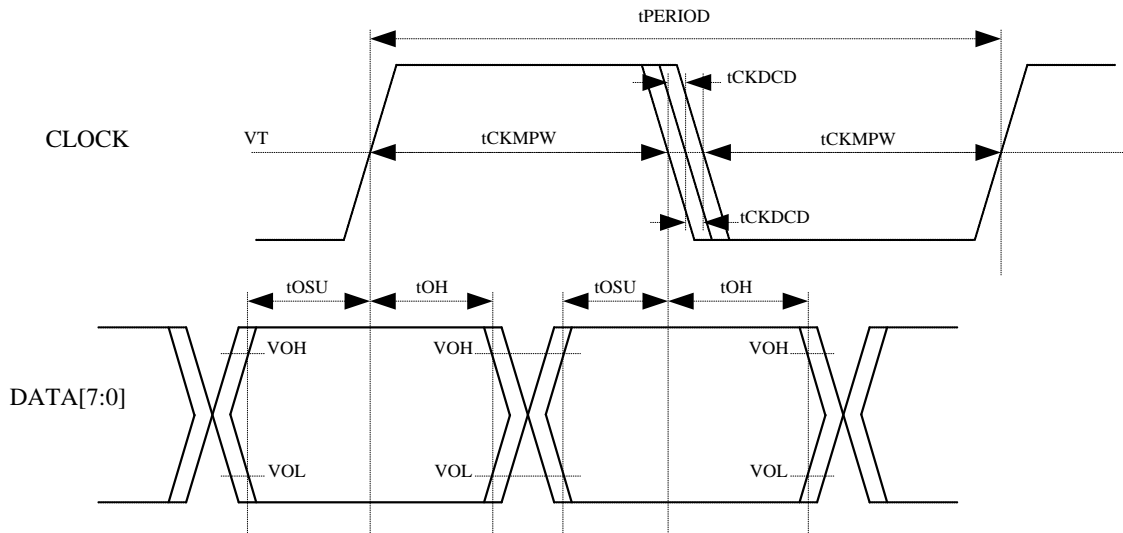
Figure 5-25. SMHC2 HS400 Output Timing Diagram

Table 5-20. SMHC2 HS400 Output Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-		V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output CMD, DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	

Note:

1.Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

2.The GPIO's driver strength level is 3 for test.
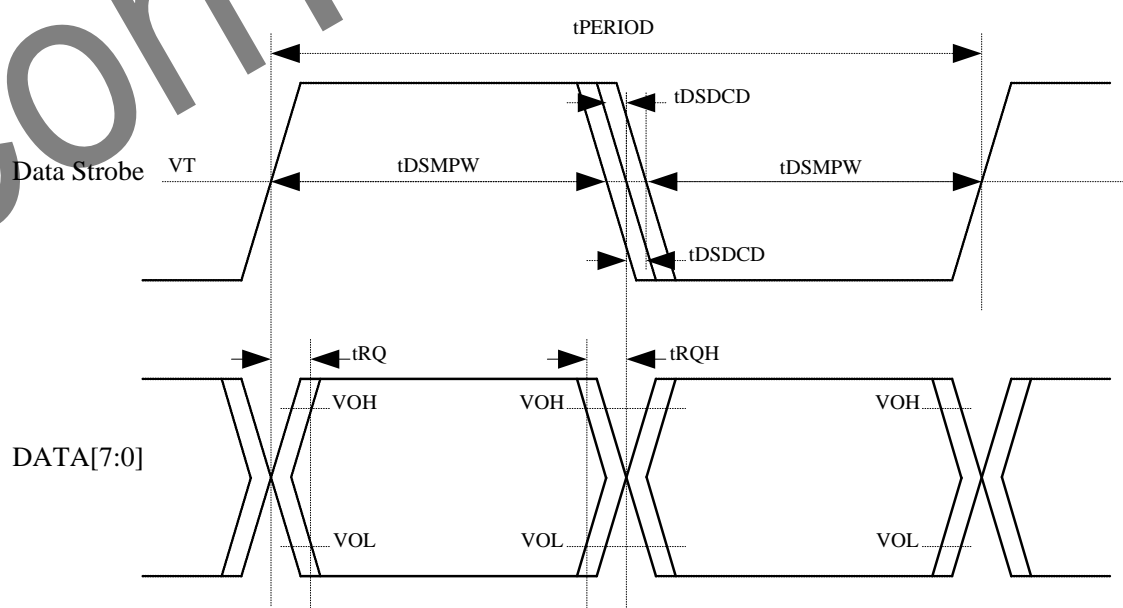
Figure 5-26. SMHC2 HS400 Input Timing Diagram

Table 5-21. SMHC2 HS400 Input Timing Constants

Parameter	Symbol	Min	Type	Max	Unit	Remark

DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Input DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	

Note:

1.Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz.

2.The GPIO's driver strength level is 3 for test.

5.8. LCD AC Electrical Characteristics
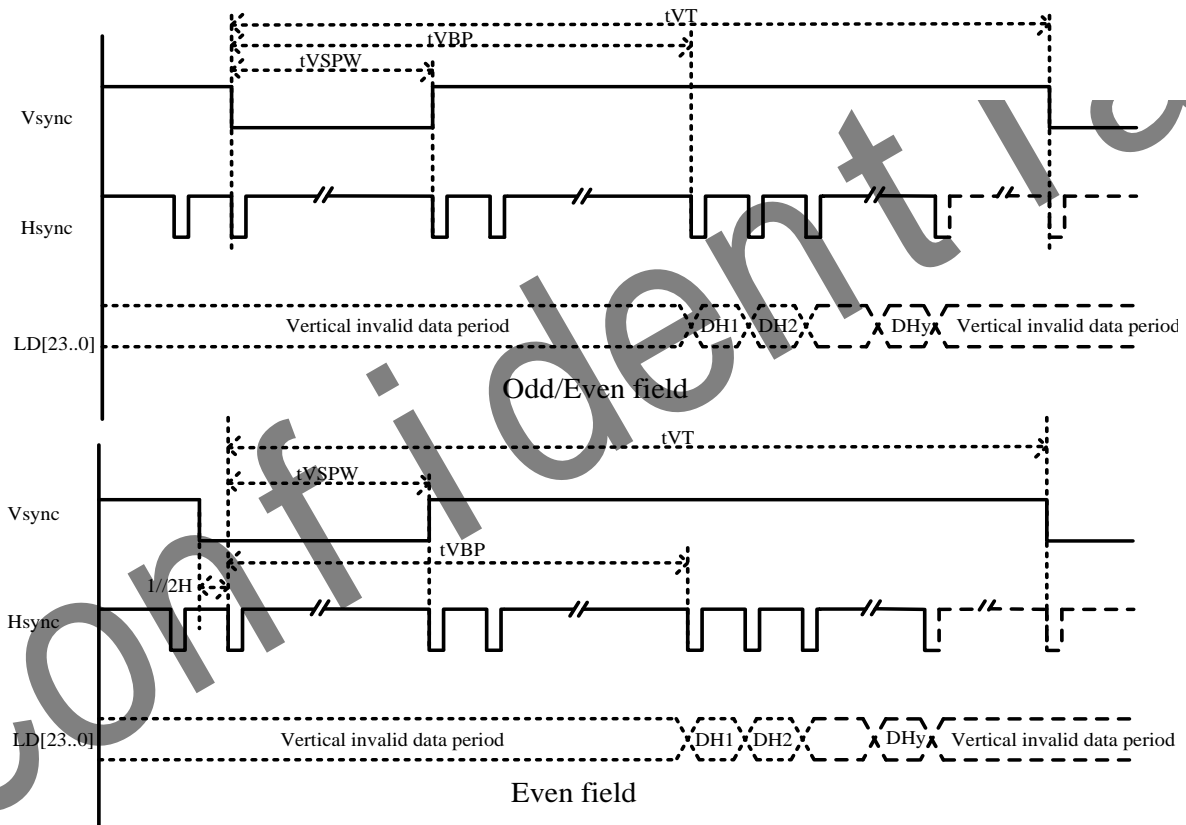
Figure 5-27. HV_IF interface Vertical Timing
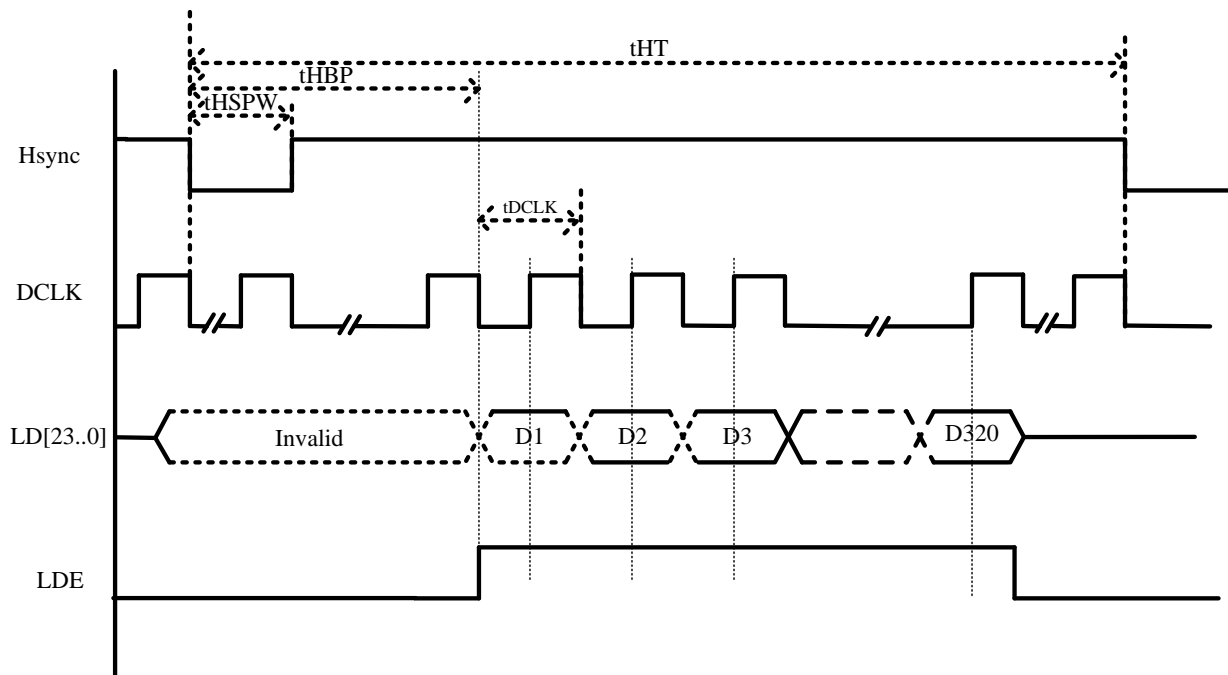
Figure 5-28. HV_IF interface Parallel Mode Horizontal Timing
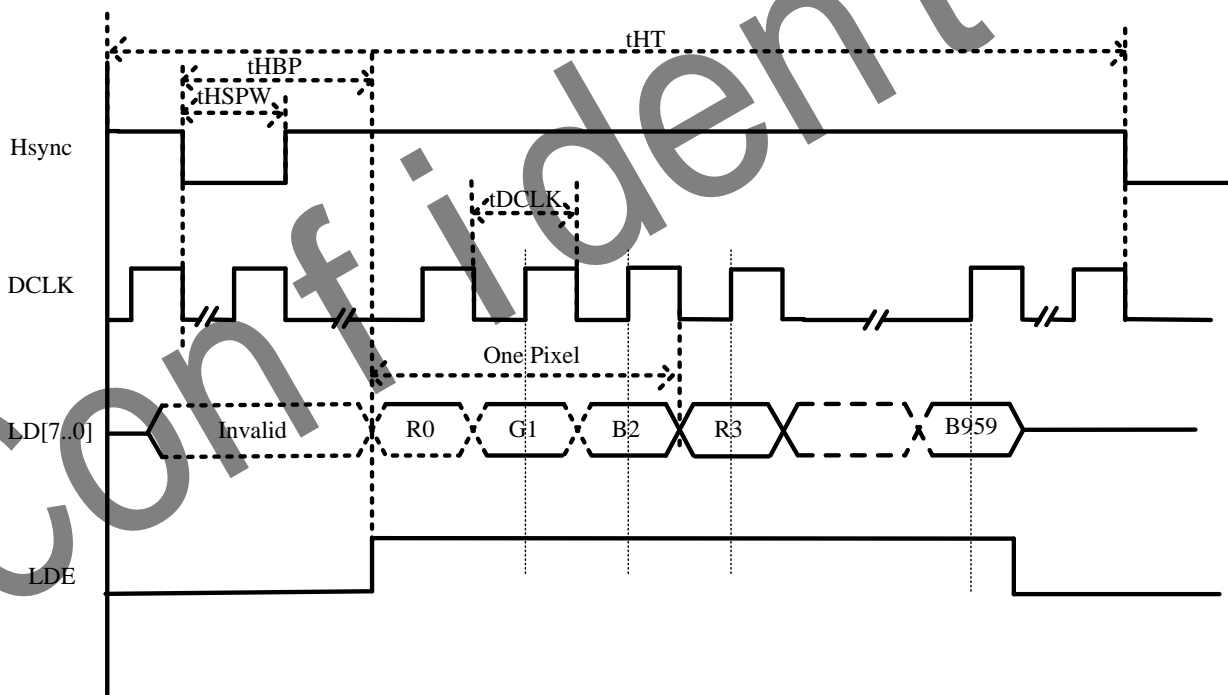
Figure 5-29. HV_IF interface Serial Mode Horizontal Timing

Table 5-22. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

Note:
(1). Vsync: Vertical sync, indicates one new frame
(2). Hsync: Horizontal sync, indicate one new scan line
(3). DCLK: Dot clock, pixel data are sync by this clock
(4). LDE: LCD data enable
(5). LD[23..0]: 18Bit RGB/YUV output from input FIFO for panel

5.9. CSI AC Electrical Characteristics
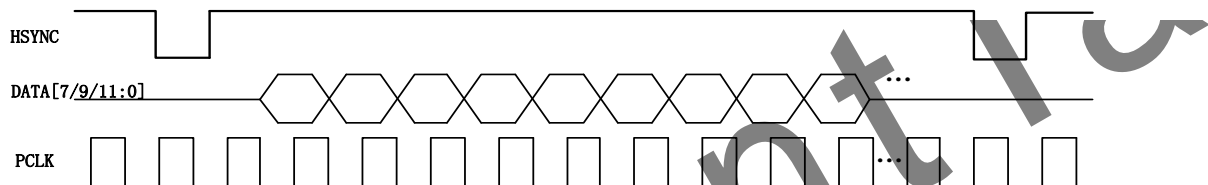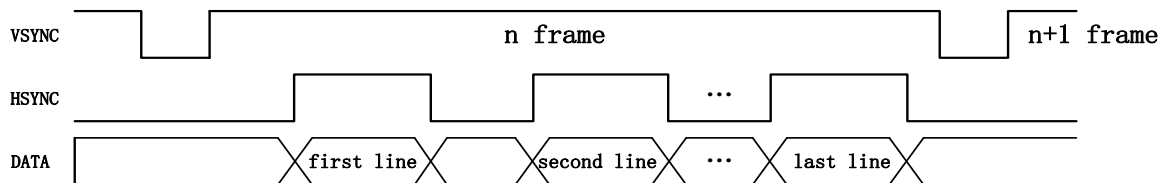
Figure 5-30. 8-bit CMOS Sensor Interface Timing
(clock rising edge sample.vsync valid = positive,hsycn valid = positive)
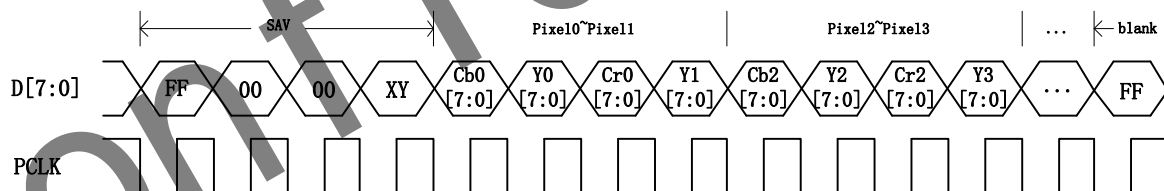
Figure 5-31. 8-bit YCbCr4:2:2 with embedded syncs(BT656) Timing
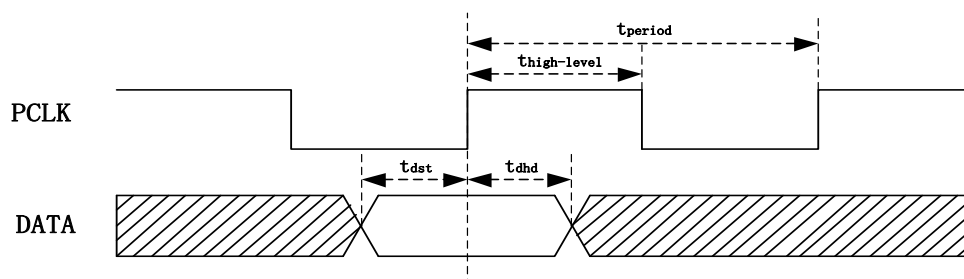
Figure 5-32. Data sample Timing

Table 5-23. CSI Interface Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Pclk Period	t_{period}	5.95	-	-	ns
Pclk Frequency	$1/t_{period}$	-	-	168	MHz
Pclk Duty	$t_{high-level}/t_{period}$	40	50	60	%

Data input Setup time	t_{dst}	0.6	-	-	ns
Data input Hold time	t_{dhd}	0.6	-	-	ns

5.10. EMAC AC Electrical Characteristics

Figure 5-33. EMAC RGMII Interface Transmit Timing

Table 5-24. RGMII Transmit Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Tclk	rgmii_tx_clk clock period	8	-	DC	ns
Tisu	GMII/TBI input set up prior to rgmii_tx_clk	2.8	-	-	ns
Tiph	GMII/TBI input data hold after rgmii_tx_clk	0.1	-	-	ns
Topv	RGMII output data valid after rgmii_tx_clk	-	-	0.85	ns
Toph	RGMII output data hold after rgmii_tx_clk	0	-	-	ns
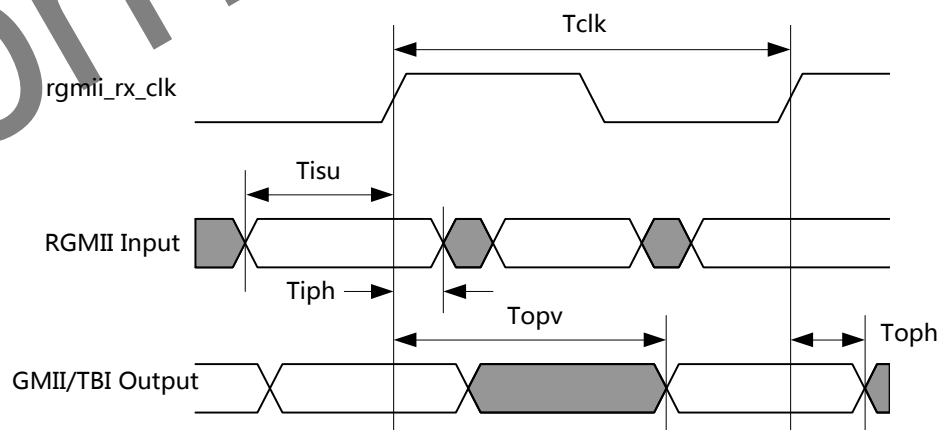
Figure 5-34. EMAC RGMII Interface Receive Timing

Table 5-25. RGMII Receive Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Tclk	rgmii_rx_clk clock period	8	-	DC	ns
Tisu	RGMII input set up prior to rgmii_rx_clk	2.6	-	-	ns
Tiph	RGMII input data hold after rgmii_rx_clk	0.8	-	-	ns

Topv	GMII/TBI iutput data valid after rgmii_rx_clk	-	-	5.2	ns
Toph	GMII output data hold after rgmii_rx_clk	0.1	-	-	ns
	TBI output data hold after rgmii_rx_clk	0.5			
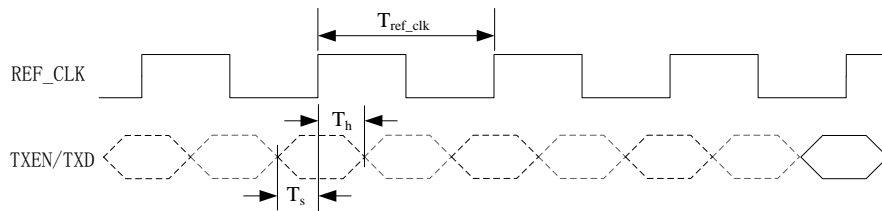
Figure 5-35. EMAC RMII Interface Transmit Timing

Table 5-26. RMII Transmit Timing Constants

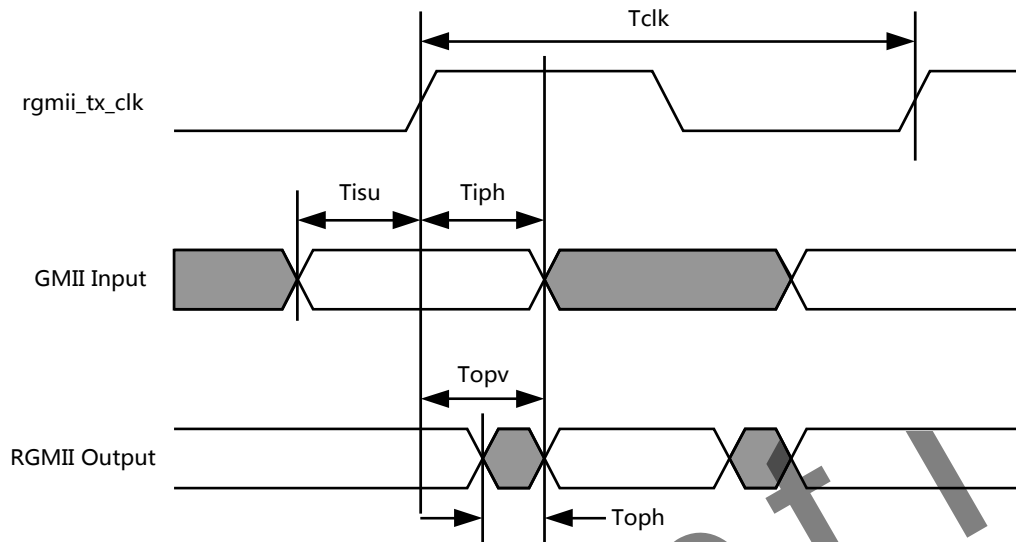| Parameter	Symbol	Min	Type	Max	Unit
T_{ref_clk}	Reference Clock Period	-	20	-	ns
T_s	TXD/TXEN to REF_CLK setup time	4	-	-	ns
T_h	TXD/TXEN to REF_CLK hold time	2	-	-	ns
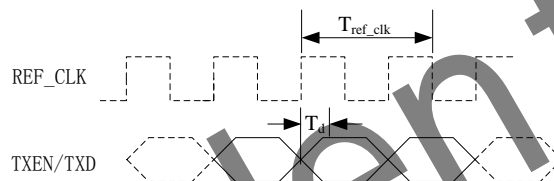
Figure 5-36. EMAC RMII Interface Receive Timing

Table 5-27. RMII Receive Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
T_{ref_clk}	Reference Clock Period	-	20	-	ns
T_d	REF_CLK rising edge to RX_DV/RXD	-	10	12	ns

5.11. CIR AC Electrical Characteristics
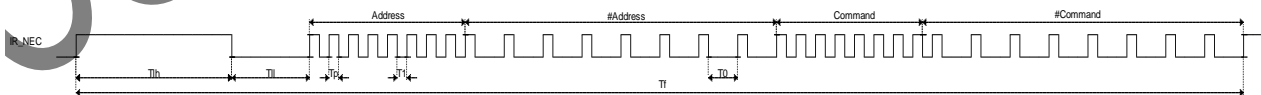
Figure 5-37. CIR-RX Timing

Table 5-28. CIR-RX Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Tf	Frame Period	-	67.5	-	ms
Tlh	Lead Code High Time	-	9	-	ms
Tll	Lead Code Low Time	-	4.5	-	ms
Tp	Pulse Time	-	560	-	us
T1	Logical 1 Low Time	-	1680	-	us
T0	Logical 0 Low Time	-	560	-	us

5.12. SPI AC Electrical Characteristics
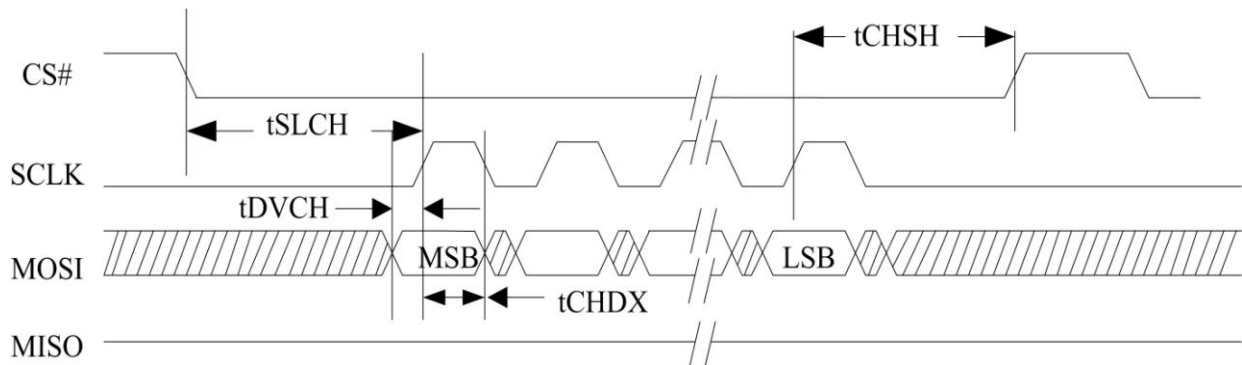
Figure 5-38. SPI MOSI Timing
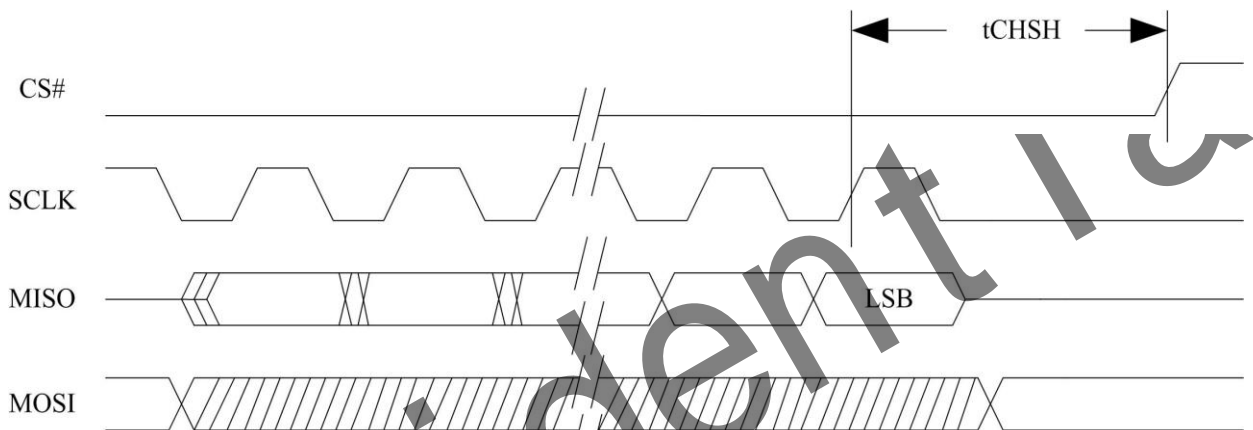
Figure 5-39. SPI MISO Timing

Table 5-29. SPI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T[1]	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns

Note (1):T is the cycle of clock.

5.13. UART AC Electrical Characteristics

Register Setting:

    Data length(DLS in LCR[1:0]) = 3 (8bit)

    Stop bit length(STOP in LCR[2]) = 1 (2bit)

    Parity enable(PEN in LCR[3]) = 1

RX   start   data   parity   stop

RX FIFO DATA   vaild data
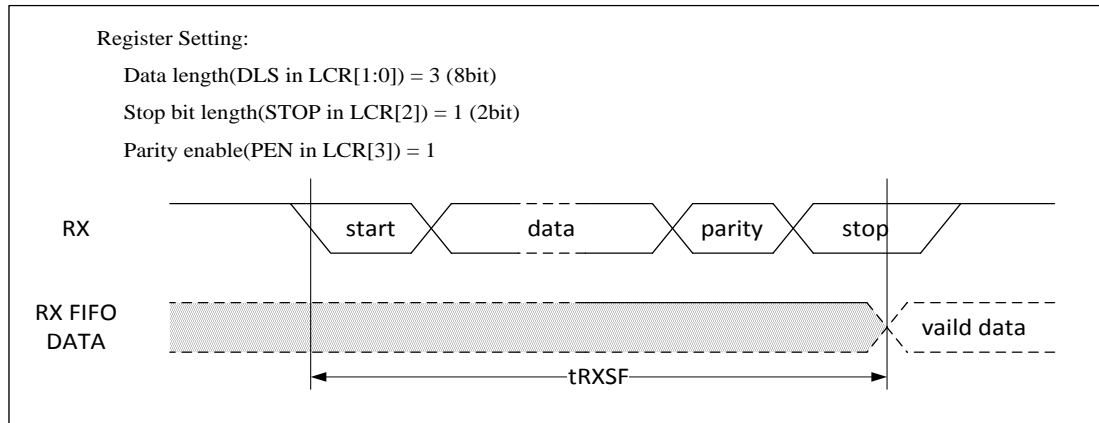
tRXSF

Figure 5-40. UART RX Timing

TX   start   data   parity   stop   start

nCTS

tDCTS   tACTS
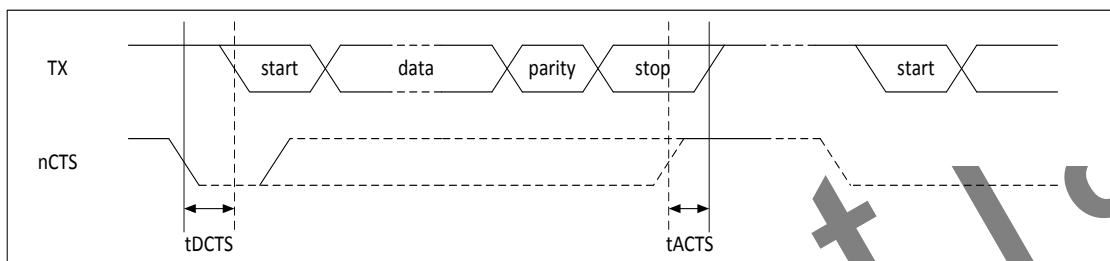
Figure 5-41. UART nCTS Timing

Register Setting:

    RTS Trigger level(RT in FCR[7:6]) = 3 (De-asserted nRTS when FIFO valid data number reach FIFO depth-2)

RX FIFO DATA NUM   FD[1]-3   FD-2   0

nRTS

tDRTS   tARTS

Note (1): FD: FIFO Depth
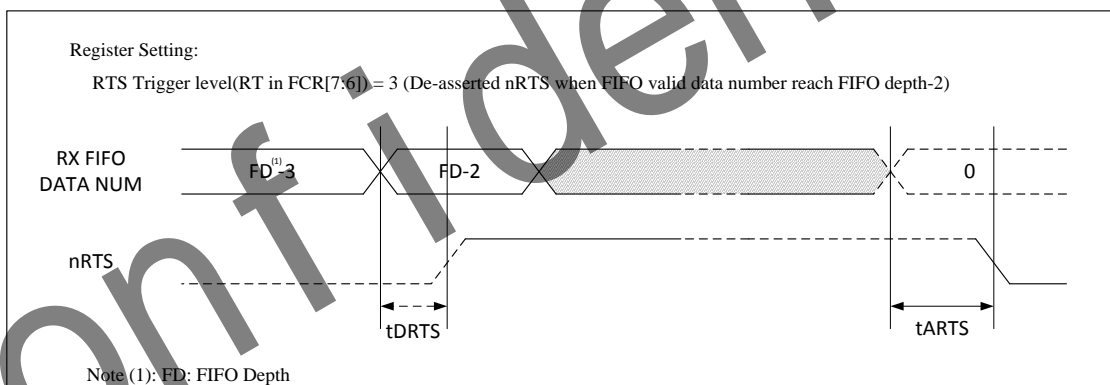
Figure 5-42. UART nRTS Timing

Table 5-30. UART Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
RX start to RX FIFO	tRXSF	$10.5\times$ BRP[1]	-	$11\times$ BRP[1]	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP[1]	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP[1]/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP[1]	ns
Delay time of asserted nRTS	tARTS	-	-	BRP[1]	ns

Note (1): BRP(Baud-Rate Period).

5.14. TWI AC Electrical Characteristics
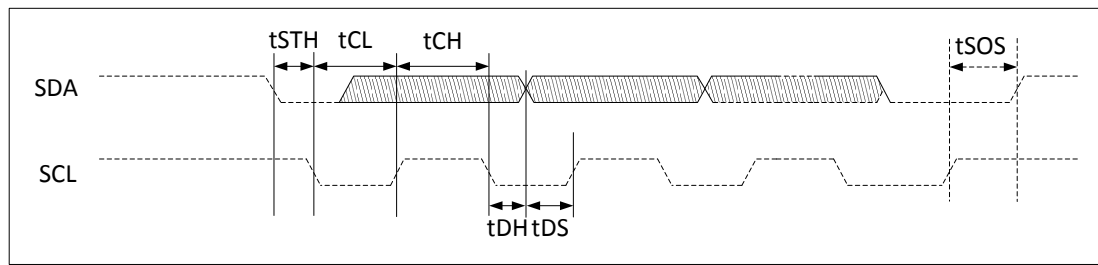
Figure 5-43. TWI Timing

Table 5-31. TWI Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
High period of SCL	tCH	0.96	-	-	µs
Low period of SCL	tCL	1.5	-	-	µs
SCL hold time for START condition	tSTH	1.5	-	-	µs
SCL step time for STOP condition	tSOS	1.6	-	-	µs
SDA hold time	tDH	0.82	-	-	µs
SDA step time	tDS	0.72	-	-	µs

5.15. TS AC Electrical Characteristics
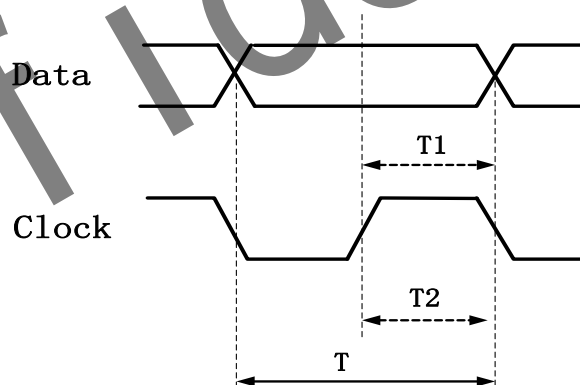
Figure 5-44. TSC Data and Clock Timing

Table 5-32. TSC Timing Constants

Parameter	Symbol	Min	Type	Max	Unit
Data hold time	T1	T/2-T/10	T$^{(1)}$/2	T/2+T/10	us
Clock pulse width	T2	T/2-T/10	T/2	T/2+T/10	us

NOTE (1):T is the cycle of clock.

5.16. SCR AC Electrical Characteristics
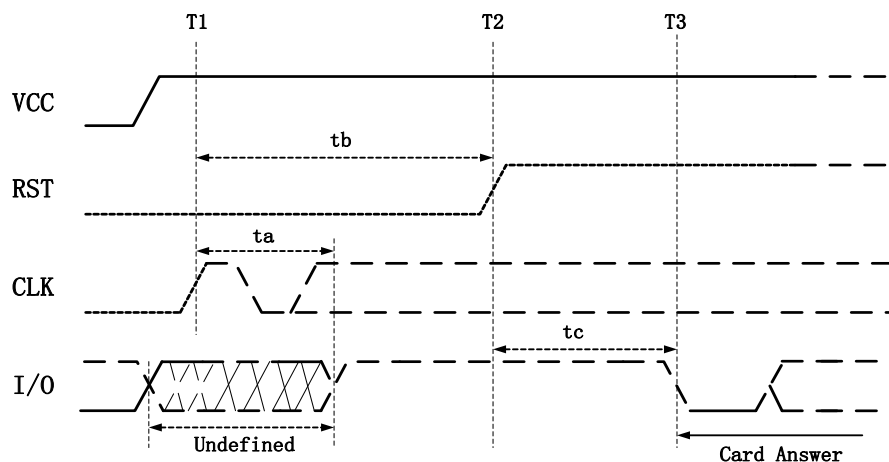
Figure 5-45. SCR Activation and Cold Reset Timing
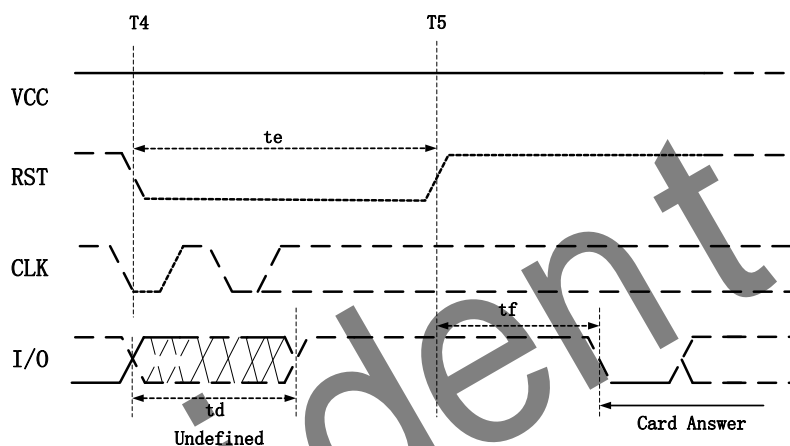
Figure 5-46. SCR Warm Reset Timing

Table 5-33. SCR Timing Constants

Symbol	Min	Type	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us

Note:

(1). Activation: Before time T1

(2). Cold Reset: After time T1

(3). T1: The clock signal is applied to CLK at time T1.

(4). T2: The RST is put to state H.

(5). T3: The card begin answer at time T3

(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1 +ta).

(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).

(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).

(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).

(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled   clock signal.

(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).

(12). f is the frequency of clock.

5.17. Power-up and Power-down Sequence

The section provides information about the A64 power up and power down sequence requirements.

5.17.1. Power-up Sequence

The following steps give an example of power-up sequence supported by the A64 device.

(1).When it is key,VCC-PL,AVCC,VCC-PL,VCC-PC,VCC-PG,CPVDD,VDD-CPUS,VCC-PD,VCC-USB,VDD-CPUX,VCC-DRAM,

 VDD-SYS are powered up simultaneously.

(2).T1 rise time is about 100us.

(3).T2 rise time is about 1000us.

(4).VCC-MDSI,HVCC and VCC-HSIC are default to be powered off. When the some domains of PMIC are enabled , VCC-MDSI,HVCC and VCC-HSIC can be powered up.

Figure 5-47 shows an example of the device power up sequence.
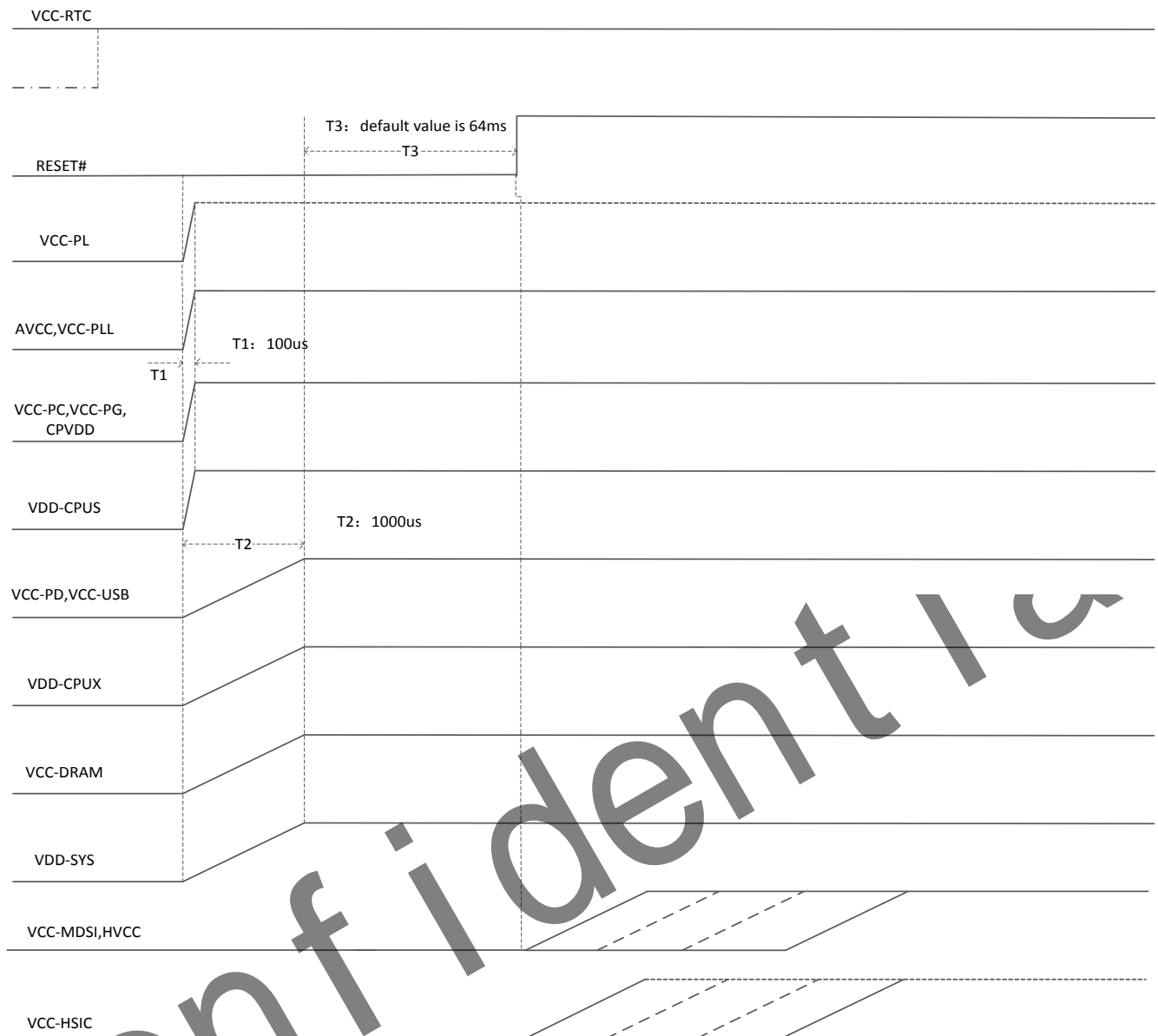
Figure 5-47. Power On Timing

5.17.2. Power-down Sequence

The following steps give an example of the power-down sequence supported by the A64 device.

(1).Reset A64 device.

(2).After PMIC receives the power-down command, pull-down RESET#, then power down all domains after 4ms.

(3).All domains are not powered down simultaneously, following the below sequence:

    (a).Power down MIPI-DSI,HDMI and HSIC domains(VCC-MDSI,HVCC,VCC-HSIC).

    (b).Power down VCC-PL,AVCC,VCC-PL,VCC-PC,VCC-PG,CPVDD,VDD-CPUS,VCC-PD,VCC-USB,VDD-CPUX,VCC-DRAM, VDD-SYS.

Figure 5-48 shows an example of the device power down sequence.
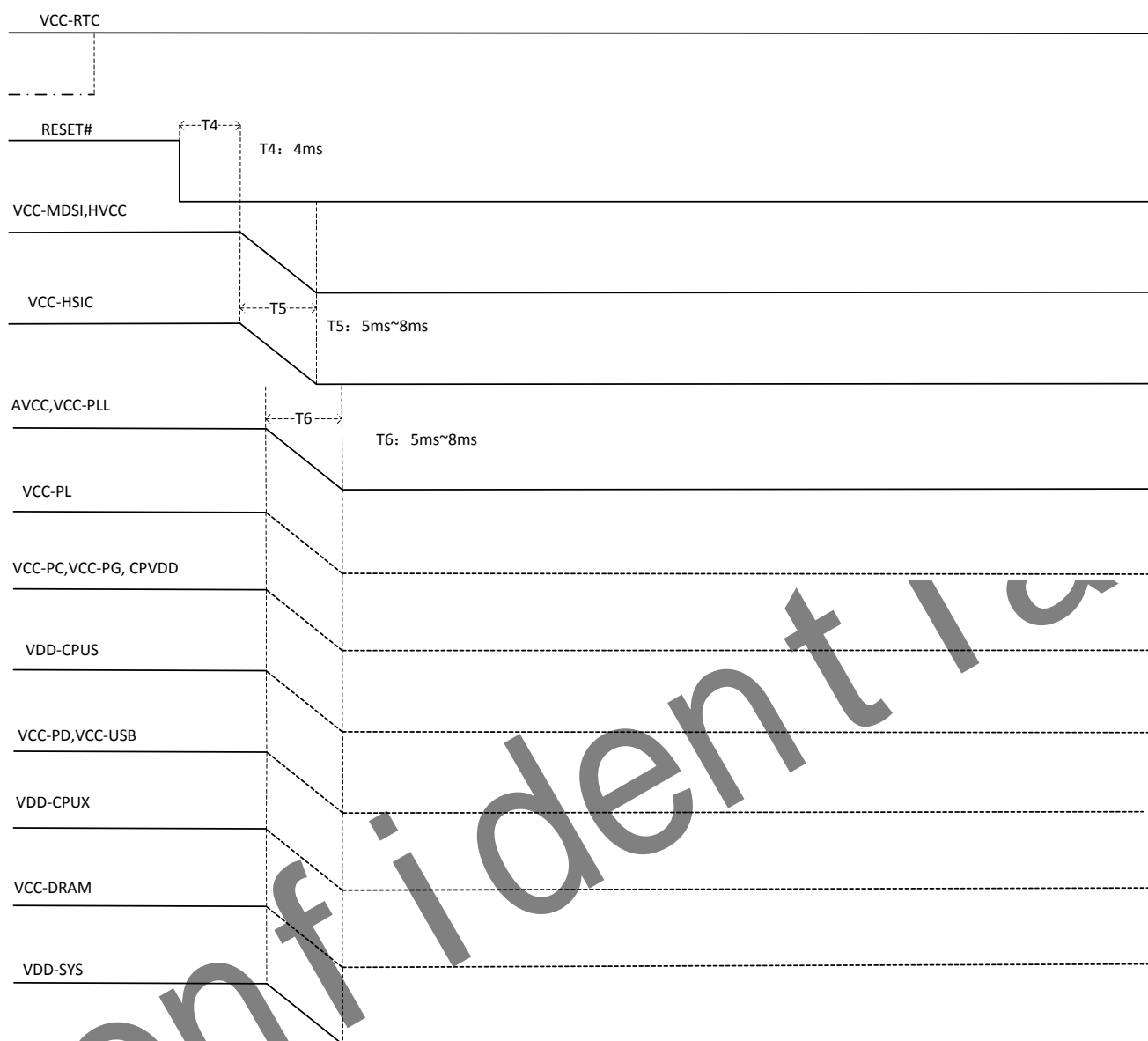
Figure 5-48. Power Down Timing

6. Package Thermal Characteristics

For reliability and operability concerns, the absolute maximum junction temperature of A64 has to be below 125°C.The testing PCB is based on 4 layers. The following thermal resistance characteristics in **Table 6-1** is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51 , the simulating resulting data is a reference only, please prevail in the actual application condition test.

Table 6-1. A64 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
T_J	Junction Temperature	-	-	+125	°C
θ $_{JA}$	Junction-to-ambient thermal resistance	-	21.6	-	°C/W
θ $_{JB}$	Junction-to-board thermal resistance	-	TBD	-	°C/W
θ $_{JC}$	Junction-to-case thermal resistance	-	TBD	-	°C/W
ψ$_{JT}$	Junction-to-top characterization parameter	-	TBD	-	°C/W
ψ$_{JB}$	Junction-to-board characterization parameter	-	TBD	-	°C/W

7. Pin Assignment

7.1. Pin Map

For A64, FBGA 396 balls, 15x15mm,0.65mm pitch package is offered. The pin maps are illustrated in **Figure 7-1** for this package.

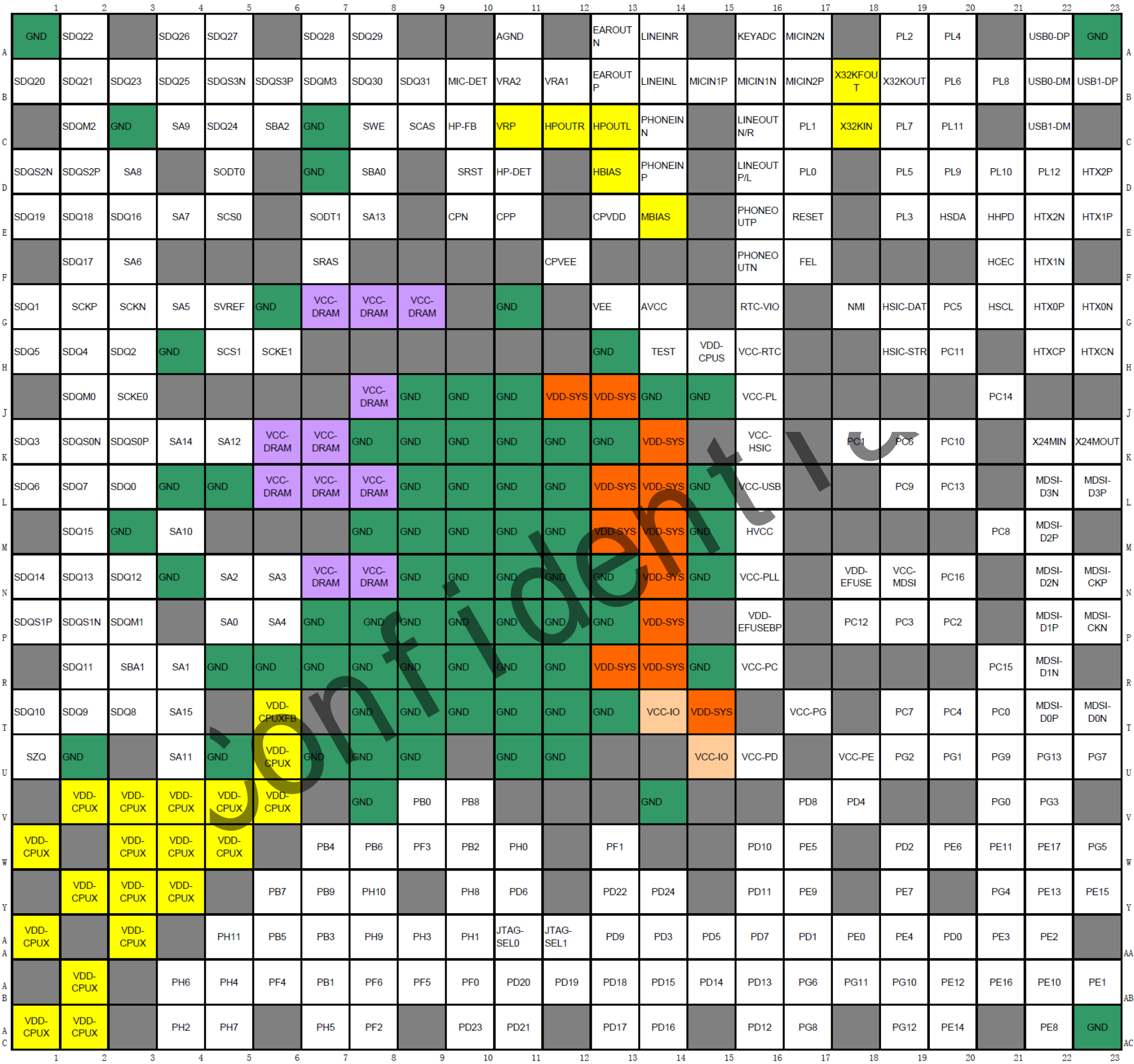|	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	SDQ22		SDQ26	SDQ27		SDQ28	SDQ29			AGND		EAROUTN	LINEINR		KEYADC	MICIN2N		PL2	PL4		USB0-DP	GND	A
B	SDQ20	SDQ21	SDQ23	SDQ25	SDQS3N	SDQS3P	SDQM3	SDQ30	SDQ31	MIC-DET	VRA2	VRA1	EAROUTP	LINEINL	MICIN1P	MICIN1N	MICIN2P	X32KFOUT	X32KOUT	PL6	PL8	USB0-DM	USB1-DP	B
C		SDQM2	GND	SA9	SDQ24	SBA2	GND	SWE	SCAS	HP-FB	VRP	HPOUTR	HPOUTL	PHONEINN		LINEOUTN/R	PL1	X32KIN	PL7	PL11		USB1-DM		C
D	SDQS2N	SDQS2P	SA8		SODT0		GND	SBA0		SRST	HP-DET		HBIAS	PHONEINP		LINEOUTP/L	PL0		PL5	PL9	PL10	PL12	HTX2P	D
E	SDQ19	SDQ18	SDQ16	SA7	SCS0		SODT1	SA13		CPN	CPP		CPVDD	MBIAS		PHONEOUTP	RESET		PL3	HSDA	HHPD	HTX2N	HTX1P	E
F		SDQ17	SA6				SRAS				CPVEE					PHONEOUTN	FEL				HCEC	HTX1N		F
G	SDQ1	SCKP	SCKN	SA5	SVREF		GND	VCC-DRAM	VCC-DRAM	VCC-DRAM			GND	VEE	AVCC	RTC-VIO		NMI	HSIC-DAT	PC5	HSCL	HTX0P	HTX0N	G
H	SDQ5	SDQ4	SDQ2	GND	SCS1	SCKE1							GND	TEST	VDD-CPUS	VCC-RTC		HSIC-STR	PC11			HTXCP	HTXCN	H
J		SDQM0	SCKE0				VCC-DRAM	GND	GND	GND	VDD-SYS	VDD-SYS	GND	GND		VCC-PL					PC14			J
K	SDQ3	SDQS0N	SDQS0P	SA14	SA12	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	GND	VDD-SYS		VCC-HSIC		PC1	PC6	PC10		X24MIN	X24MOUT	K
L	SDQ6	SDQ7	SDQ0	GND	GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	GND	GND	GND	VDD-SYS	VDD-SYS	GND		VCC-USB			PC9	PC13		MDSI-D3N	MDSI-D3P	L
M		SDQ15	GND	SA10			GND	GND	GND	GND		VDD-SYS	VDD-SYS			HVCC					PC8		MDSI-D2P	M
N	SDQ14	SDQ13	SDQ12	GND	SA2	SA3	VCC-DRAM	VCC-DRAM	GND	GND	GND	GND	GND	VDD-SYS	GND	VCC-PLL	VDD-EFUSE	VCC-MDSI	PC16			MDSI-D2N	MDSI-CKP	N
P	SDQS1P	SDQS1N	SDQM1	SA0	SA4	GND	GND	GND	GND	GND	GND	GND	GND	VDD-SYS		VDD-EFUSEBP	PC12	PC3	PC2			MDSI-D1P	MDSI-CKN	P
R		SDQ11	SBA1	SA1	GND	GND	GND	GND	GND	GND	GND	GND	VDD-SYS	VDD-SYS	GND	VCC-PC					PC15		MDSI-D1N	R
T	SDQ10	SDQ9	SDQ8	SA15	VDD-CPUXFB		GND	GND	GND	GND	GND	VCC-IO	VDD-SYS			VCC-PG			PC7	PC4	PC0	MDSI-D0P	MDSI-D0N	T
U	SZQ	GND		SA11	GND	VDD-CPUX	GND		GND		GND	VCC-IO				VCC-PD		VCC-PE	PG2	PG1	PG9	PG13	PG7	U
V		VDD-CPUX	VDD-CPUX	VDD-CPUX	VDD-CPUX	VDD-CPUX	GND	PB0	PB8							GND	PD8	PD4			PG0	PG3		V
W	VDD-CPUX		VDD-CPUX	VDD-CPUX	VDD-CPUX		PB4	PB6	PF3	PB2	PH0		PF1			PD10	PE5		PD2	PE6	PE11	PE17	PG5	W
Y		VDD-CPUX	VDD-CPUX	VDD-CPUX	PB7	PB9	PH10			PH8	PD6		PD22	PD24		PD11	PE9		PE7		PG4	PE13	PE15	Y
AA	VDD-CPUX		VDD-CPUX		PH11	PB5	PB3	PH9	PH3	PH1	JTAG-SEL0	JTAG-SEL1	PD9	PD3	PD5	PD7	PD1	PE0	PE4	PD0	PE3	PE2		AA
AB		VDD-CPUX		PH6	PH4	PF4	PB1	PF6	PF5	PF0	PD20	PD19	PD18	PD15	PD14	PD13	PG6	PG11	PG10	PE12	PE16	PE10	PE1	AB
AC	VDD-CPUX	VDD-CPUX		PH2	PH7		PH5	PF2		PD23	PD21		PD17	PD16		PD12	PG8		PG12	PE14		PE8	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 7-1. A64 Pin Map

7.2. Package Dimension

Figure 7-2 shows the top,bottom,and side views of A64 package dimension.

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.300	—	—	0.051
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.940	0.990	1.040	0.037	0.039	0.041
c	0.250	0.290	0.330	0.010	0.011	0.013
D	14.900	15.000	15.100	0.587	0.591	0.594
E	14.900	15.000	15.100	0.587	0.591	0.594
D1	—	14.300	—	—	0.563	—
E1	—	14.300	—	—	0.563	—
e	—	0.650	—	—	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
N	396			396		
MD/ME	23/23			23/23		

Top View

Bottom View

Side View

TECHNOLOGY SPECIFICATION

1. BALL PAD OPENING: 0.270mm;
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C;
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd;
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
7. ALL UNITS ARE IN MILLIMETER;
8. THE DERECTION OF VIEW :
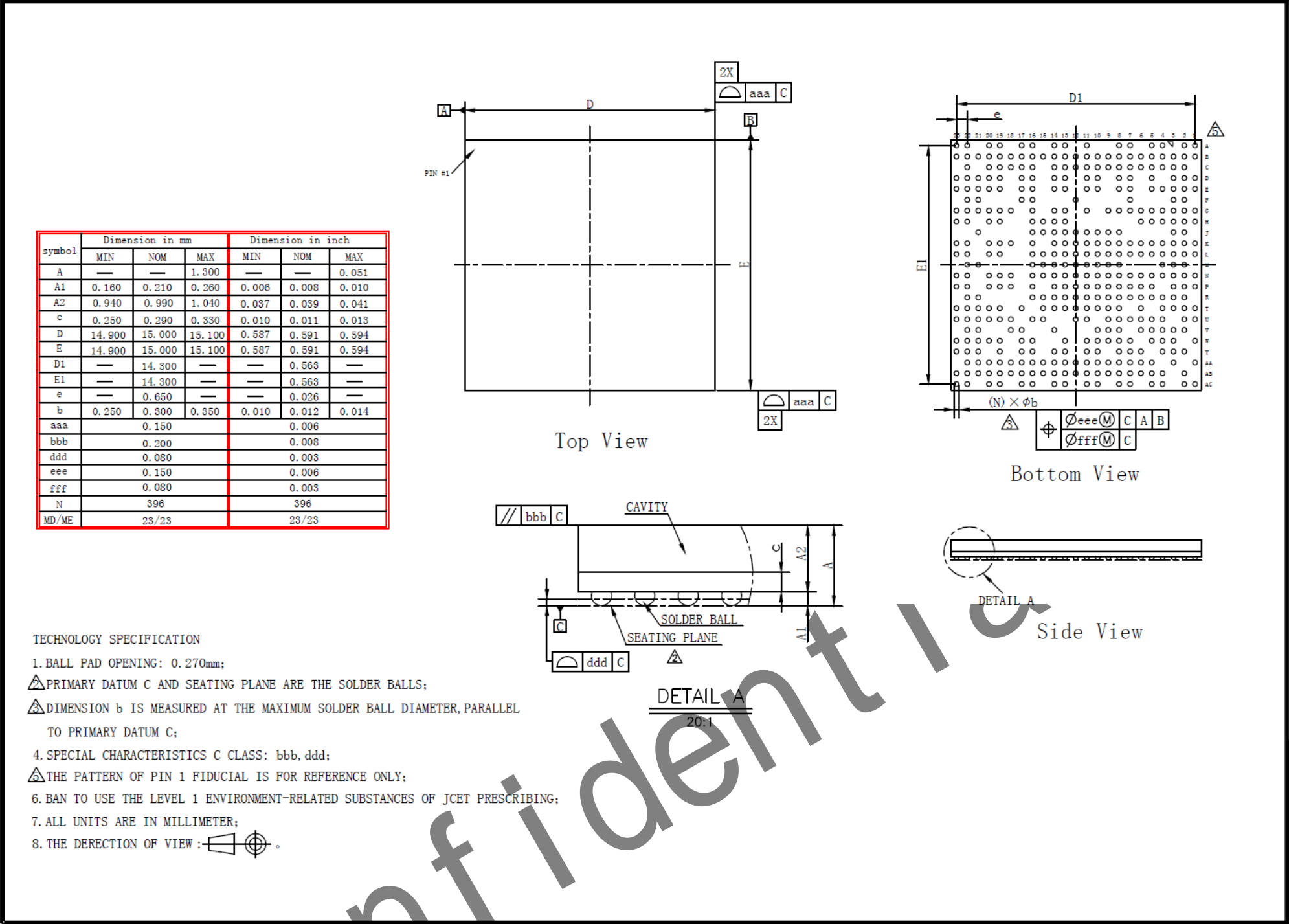
Figure 7-2. A64 Package Dimension

Copyright © 2015 Allwinner Technology Co.,Ltd.All Rights Reserved.

Allwinner Technology Co.,Ltd.

No.9 Technology Road 2,High-Tech Zone,

Zhuhai, Guangdong Province, China

Contact US:

Service@allwinnertech.com

www.allwinnertech.com