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# HARDWARE IMPLEMENTATION OF SPIKING NEURONS USING VO2 OCILLATOR DEVICES

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# Hardware Implementation of Spiking Neurons using $VO_2$ Oscillator Device


## Abstract

In this work, several designs of $VO_2$ based spiking neuron circuits were measured and demonstrated. These circuits could generate a series of voltage spikes (known as action potentials) with refractory periods under constant voltage inputs. This property could potentially be used to implement a frequency coding scheme similar to that in a biological neural network. The leaky integrate-and-fire functionality was also demonstrated, with a simplified circuit design for spike generation. Furthermore, both excitatory and inhibitory inputs were implemented and tested for the spiking neuron circuits. These $VO_2$ based spiking neurons were shown to be capable of interacting with each other in a circuit, providing potentials for various spike based computation schemes. This is conceptually demonstrated through the measurement on a feedback loop, consisting of two such neuron circuits, which is similar to a recurrent inhibition circuitry commonly found in cortical nervous system.



Key words**: spiking neuron; vanadium dioxide; relaxation oscillator; inhibition;**


# 1. Introduction

The human brain is uniquely capable and efficient in various cognitive tasks, such as visual recognition, speech recognition, and language processing[1,2], in which a digital computer running a conventional software doesn't do nearly as well or as efficient[3,52]. Hence, it has long been hypothesized that a brain-inspired computational paradigm, which seeks to harness the computational power of a biological nervous system by drawing resemblances of some form to it, could have the potential to improve the performance of machines in these areas[4,5].

One of such brain-inspired approaches is neuromorphic engineering, originally proposed by Meed[6] in 1989. It refers to the attempt of building hardware electrical devices and circuits that mimic the neurons, synapses and their connections in terms of electrical properties and signaling process[7,8].

**Biological neurons.** The main function of a neuron in a biological nervous system is to generate and transmit action potentials, or spikes, in response of various stimuli. Action potentials are widely believed to be the carriers of information in neural signaling process[9]. Physically, an action potential is an abrupt voltage spike (typically ~100mV in amplitude in humans) of the membrane potential, $V_m$, from its resting value[10]. This generation process has been attributed to the complex dynamics of sodium and potassium ion channels on the membrane of a neuron, which could be modeled with an equivalent electrical circuit[11].

An action potential is typically followed by a post-potential hyperpolarization, which is the phenomena that the membrane potential would drop below its resting value immediately after a spike[10]. This is then followed by a refractory period of up to hundreds of miniseconds, during which the neuron could not generate another action potential under the same stimulus intensity[12]. The presence of a refractory period is especially important for the frequency coding of neuronal signaling[13], where the intensity information of a stimulus is coded in the frequency of firing of action potentials.

Neurons are connected with other neurons through synapses, which, in the central nervous system, are unidirectional structures used to transmit the information of action potentials from the pre-synaptic neuron to the post-synaptic neuron[10]. A neuron integrates the information from its pre-synaptic neurons and would generate an action potential, if the threshold is reached. This threshold integrate-and-fire property is crucial to the signaling of neurons[14,15].

The action potential travels through its axon, which branches into ~$10^3$ synapses[10] on its post-synaptic neurons. One of the important characteristics of the synapses is that they are either excitatory or inhibitory. When an action potential arrives, the excitatory synapses would increase the ability of a post-synaptic neuron to fire an action potential, while the inhibitory synapses would suppress the generation of post-synaptic action potentials[16]. This property of excitation and inhibition has contributed to the functioning of various types of neuronal circuitry in the biological nervous system[17,18], such as recurrent inhibition[19,20], in which a principle neuron adjusts its own firing pattern through the feedback of an inhibitory interneuron.

**Spiking neuron circuits.** The circuits that could reproduce the firing of action potentials and related characteristics are typically referred to as spiking neuron circuits, or simply spiking neurons[7,21]. Many such implementations have been proposed, mostly being analog or mixed signal circuits based on silicon transistors[5,22,23]. These designs either do not generate spikes similar to neuronal action potentials, or suffer from inefficiencies in terms of complexity and area, as the basic building block, the transistor, has very different electrical properties from the biological neurons.

Recently, it has been shown that several emerging materials and devices, such as Mott insulators[25,27], phase transition materials[26], spin-transfer torque[24], could be used in constructing neuromorphic circuits. These devices feature highly non-linear dynamics[28], which could potentially be harnessed to facilitate a more compact design of spiking neuron circuits.

In this paper, several spiking neuron circuits were demonstrated. These designs were based on $VO_2$ relaxation oscillators previously proposed by Nikhil Shukla *et al*[28]. An action potential with a post-potential hyperpolarization and a refractory period[9,12] was demonstrated. The circuit has also been shown to have potentials in frequency coding scheme. This design is referred to as a regular spiking neuron circuit in this paper, as its output could mimic the Regular Spiking (RS) pattern of a biological neuron[29]. A more compact design of the circuit was demonstrated to facilitate the leaky integrate-and-fire functionality. Furthermore, inhibitory synaptic connection was also implemented, and a basic recurrent inhibitory circuit was built and measured to show the interactions of two such spiking neurons through their excitatory and inhibitory synaptic connections.

## 2. Overview

**$VO_2$ material.** As a phase-transition material (PTM), Vanadium Dioxide ($VO_2$) is characterized[37] by sharp Insulator-to-Metal and Metal-to-Insulator Transitions (referred to as IMT and MIT, respectively). This type of materials is commonly known as Mott insulators[25]. Although the exact physical mechanism through which the transitions are facilitated is still open for exploration[30,31], the phase-transition property itself has become increasingly attractive to a wide range of studies and applications[32-36].

The transition between metallic and insulating states in $VO_2$ material could be triggered through various external stimuli, such as temperature, electrical voltage, electrical current, pressure, and even doping[36]. For instance, figure 1-a shows the thermally induced IMT/MIT pair of a $VO_2$ film deposited on a $TiO_2$ substrate. The resistivity of the film undergoes ~2 orders of magnitude transition between the metallic and insulating states.

More importantly for circuit applications, the transitions could also be triggered electrically[37], as shown in the $VO_2$ I-V characteristics in figure 1-b, by applying a voltage across the $VO_2$ device. The IMT occurs at ~5.5 V during the forward sweep, while the MIT occurs at ~ 3.3 V during the reverse sweep, opening up a hysteresis window of ~ 2.2 V.

**$VO_2$ oscillator device.** As demonstrated by Nikhil Shukla *et al*[28], one of the ways to harness the rich dynamics associated with the $VO_2$ resistivity transitions is to connect the $VO_2$ device with a series resistor, as depicted in figure 1-d, where a transistor operates as the series resistor. The series resistor feeds back to the $VO_2$ device through its load line. It has been shown that[28], when the load line is biased in a non-hysteresis regime of the $VO_2$ I-V curve, the state of the $VO_2$ device would undergo sustained transitions, resulting in a voltage oscillation at the internal node (which is also the output node $V_{out}$), as shown in figure 1-c.

$V_{out}$ reflects the state of the $VO_2$ device. When the $VO_2$ device is in a metallic state, $V_{out}$ approaches $V_{ds}$. When it transitions back to the insulating state, the internal node voltage drops to its original value. In the measurement results presented in this work, the typical duration of a single voltage spike (an IMT/MIT pair of the $VO_2$ device) is measured to be 10~50 us, with a spike amplitude of ~6 V.

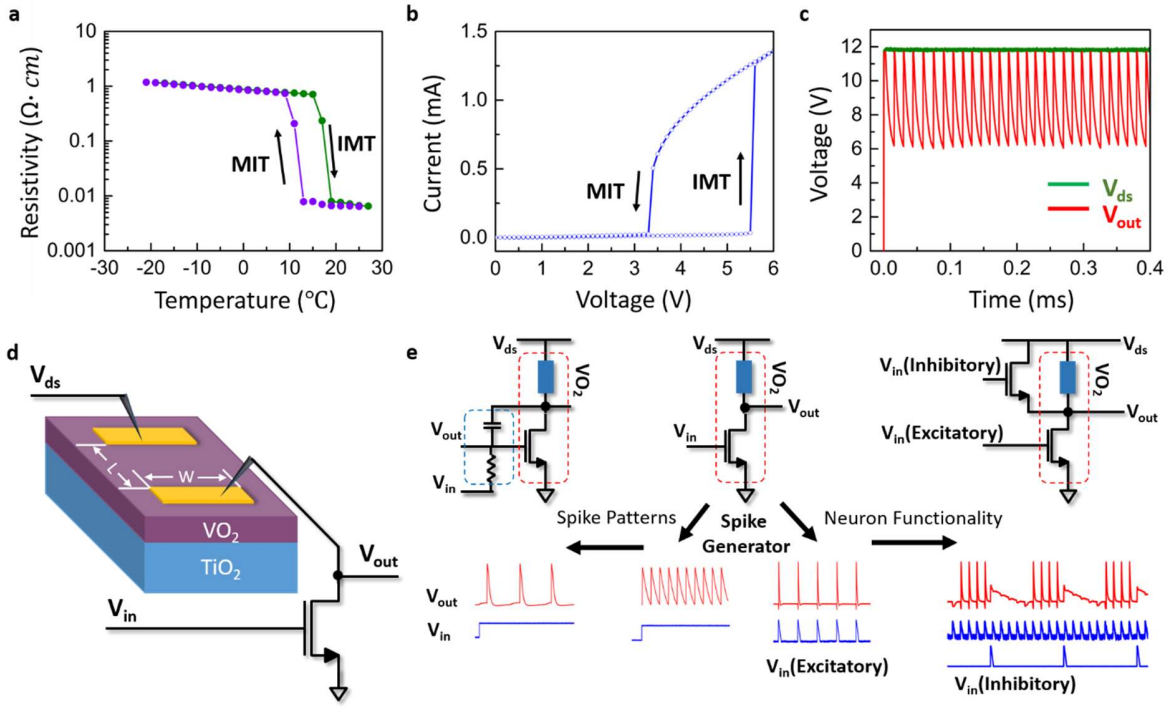


**Figure 1 | $VO_2$ based spiking neuron circuits overview. (a)** Resistivity vs. Temperature curves of the $VO_2$ film. **(b)** I-V characteristics of a $VO_2$ device (W = 6 um, L = 8 um), showing electrically triggered IMT/MIT. **(c)** Measured waveform of a $VO_2$ relaxation oscillator. Device dimension: W = 4 um, L = 6 um. Series resistance = 36 kΩ. Supply voltage $V_{ds}$ = 12 V. **(d)** Schematic of $VO_2$ based spike generator circuit. **(e)** Illustrations of $VO_2$ spiking neuron design concepts. **Middle**: $VO_2$ spike generator circuit. **Left**: $VO_2$ regular spiking neuron circuit. **Right**: $VO_2$ principle neuron circuit with excitatory and inhibitory inputs.

**$VO_2$ spiking neuron circuits.** The $VO_2$ oscillator device provides an opportunity for implementing spiking neuron circuits. With its voltage-dependent resistivity transitions, the $VO_2$ device could be an efficient way to mimic the dynamics of the sodium and potassium ion channels on the membrane of a biological neuron. Although it has not been shown in a $VO_2$ device, but it was suggested that, in $NiO_2$, a material very similar to $VO_2$ in terms of phase transition properties, the dynamics of MIT/IMT pair show similarity[25] with the Hodgkin-Huxley action potential model[11] mathematically.

In this work, the proposed spiking neuron circuits are based on the $VO_2$ oscillator, which consists of a $VO_2$ device and a transistor in series, and is henceforth referred to as a $VO_2$ spike generator in the rest of the

paper. This circuit is depicted in figure 1-e middle panel. The main function of a $VO_2$ spike generator is to fire a spike at the output node under the correct input conditions. The transistor could be biased into two different initial conditions, either completely off, of at a subthreshold gate voltage, facilitating two different spiking neuron circuit designs, as depicted in figure 1-e. More detailed discussion of the working of these circuits are provided in the next section.

As long as the load line of the series resistor is biased in the oscillating regime, the voltage oscillation of a $VO_2$ oscillator is sustained during the period of operation. To introduce a refractory period, it is necessary then to adjust the load line through a feedback mechanism. In this design, the generation of a single spike is fed back to the gate terminal of the series transistor through a low-pass filter. The resulting circuit, as illustrated in the left inset of figure 1-e, is referred to as a regular spiking neuron circuit. It is capable of generating action potentials with post-potential hyperpolarization and a refractory period. When biased under sustained input stimulus, as is often done in biological neuronal recordings[9,15], it demonstrated potentials for frequency coding schemes.

Another important function implemented based on the $VO_2$ spike generator is the addition of an inhibitory input node. This is realized by connecting a second transistor in parallel with the $VO_2$ device to serve as the second input, as illustrated in figure 1-e right panel. When an input signal arrives at the gate of the inhibitory transistor, it pulls up the voltage at the internal node (which is also the output node), $V_{out}$, suppressing the ability for the $VO_2$ device to transition to a metallic state. This design is referred to as a $VO_2$ principle neuron circuit, following the convention of its biological counterpart[17].

The leaky integrate-and-fire functionality[38,39] could be implemented by adding a leaky integrator circuit, consisting of a capacitor and a resistor in parallel, to the gate of the series transistor. This design is referred to as an interneuron circuit. Its measured performance is demonstrated in the next section.

**Method.** The $VO_2$ device was fabricated by depositing a $VO_2$ film (15 nm thickness) on $TiO_2$ substrate. Pt/Au electrodes were patterned in pairs on the surface of the $VO_2$ film to form two-terminal devices with various channel widths and lengths. The $TiO_2$ substrate induces strain to the $VO_2$ lattice, thus reducing its thermal transition temperature to ~18 C, as compared to ~68 C in unstrained $VO_2$ film. Hence, in order to obtain stable oscillation waveforms, all transient measurements are done in ~-6 C temperature.

The $VO_2$ device is connected to a circuit bread board through a probe station. The circuits measured here consisted of discrete components. A two-channel function generator was used to provide supply voltage and various input signals to the circuits. Two types of input signals were used in the measurements: square waves for the regular spiking neuron circuit; DC-biased AC pulses for the principle neuron and the leaky integrate-and-fire neuron circuits. The waveforms were measured and recorded through an oscilloscope.

# 3. Results

**Action potential.** The generation of biologically feasible action potentials is implemented in the regular spiking neuron circuit, as depicted in figure 2-a. $VO_2$ device dimensions of W = 6 um and L = 6 um was used in all measurements in figure 2. The circuit is based on a $VO_2$ spike generator. An additional series resistor $R_s$ is added to the spike generator. It serves to protect the $VO_2$ device from large transient currents during MIT/IMT transitions. The circuit feeds back the output of the $VO_2$ spike generator to its input, through a high-pass filter, comprised of a feedback capacitor and an input resistor. The feedback capacitor is connected between the drain and gate of the transistor. Output signal ($V_{out}$) is taken from the gate of the transistor and is separated by an input resistor from the input node.

The measurements were taken under a constant input voltage. This stimulus condition is similar to what is commonly used in the recording of action potentials generated by biological neurons[9,15]. Under such conditions, this circuit generates a train of action potentials with biologically feasible details, including post-potential hyperpolarization and refractory periods, as shown in figure 2-b. The measurement was taken with the following circuit conditions: series resistor $R_s$ = 9.8 kΩ; feedback capacitor C = 330 pF; input resistor $R_{in}$ = 36 kΩ.

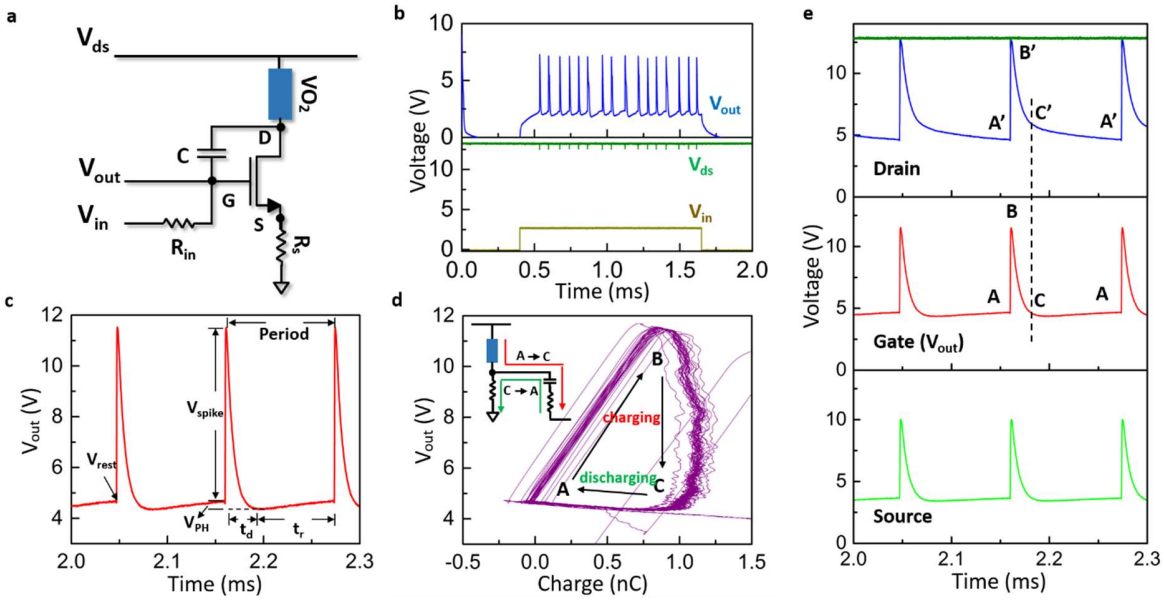


**Figure 2 | Generation of action potentials (spike trains) under constant input voltage. (a)** Diagram of the $VO_2$ regular spiking neuron circuit. The circuit consists of a $VO_2$ spike generator and a high-pass filter. **(b)** Measured waveform showing a train of spikes. Square waves are used as the input signal. $V_{in}$ = 2.8 V; supply voltage $V_{ds}$ = 13 V. **(c)** A more detailed waveform of the spike train. Input signal $V_{in}$ = 5.4 V; supply voltage $V_{ds}$ = 13 V. **(d)** Q -V phase diagram showing the states of the circuit. Charge is calculated by $Q = C \cdot \Delta V$ ($\Delta V$: voltage across the capacitor, defined as $V_{drain}$ - $V_{gate}$). **Inset**: illustration of charging and discharging paths in the equivalent circuit. **(e)** Traces of the voltage waveforms at the drain, gate ($V_{gate}$ = $V_{out}$) and source of the transistor. The corresponding points of states A, B, C in (d) are marked on the voltage traces. The dashed C-C' line marks the onset of the refractory period.

Figure 2-c illustrates mores details of the spike train. Several characteristics are defined here to describe the individual spikes, similar to the conventions used for biological action potentials[10]: $V_{rest}$ (resting voltage) = the gate voltage at which a spike could be triggered, which is also the "resting voltage" for the neuron circuit; $V_{spike}$ (amplitude of the spike) = the voltage difference between the peak of the spike and its $V_{rest}$; $V_{PH}$ (Post-potential Hyperpolarization voltage) = The voltage drop from $V_{rest}$ that occurs immediately after a spike; $t_d$ = duration of the spike; $t_r$ (duration of the refractory period) = the time interval between the ending of the previous spike and the initiation of the next spike. The time period between the initiation of two consecutive spikes is considered to be ($t_d$ + $t_r$). The frequency or the rate of the spike train (number of spikes per unit time window) is expressed as the reciprocal of the period. The waveforms in figure 2 c-e were measured with the following circuit conditions: $R_s$ = 27.7 kΩ; $R_{in}$ = 42.8 kΩ; C = 770 pF.

The capacitor C introduces asymmetry to the system states before and after an individual spike. It functions as a feedback control as well as a charge storage unit for the circuit. During a single spike, the $VO_2$ device

undergoes an IMT/MIT transition pair. Electrical charges are accumulated on the capacitor, creating a voltage difference, $\Delta V$, between the drain and gate of the transistor. Hence an asymmetry could be obtained in the system between pre-spike and post-spike states in the form of the charge stored on the capacitor.

This asymmetry between pre-spike and post-spike system states is evident in the phase diagram in figure 2-d. The system state could be expressed in terms of Q – V pair, i.e., the charges stored on the feedback capacitor vs. the corresponding output voltage value. Asymmetry in system pre-spike state (A) and post-spike state (C) is clearly observed as ~$10^{-9}$C residual charges are stored during the spike. This asymmetry prevents the $VO_2$ device from immediately transitioning back to metallic state, thus halting the generation of sustained oscillations. Charging (A->B) and discharging (C->A) processes have distinct paths, facilitating a prolonged refractory period (C-> A), typically ~100 us. It also leads to a notable post-potential hyperpolarization typically 200~500 mV. The system state undergoes periodic evolution (A -> B -> C-> A) that accompanies the IMT/MIT transitions of the VO2 device, hence producing a spike train as observed in figure 2-b and 2-c.

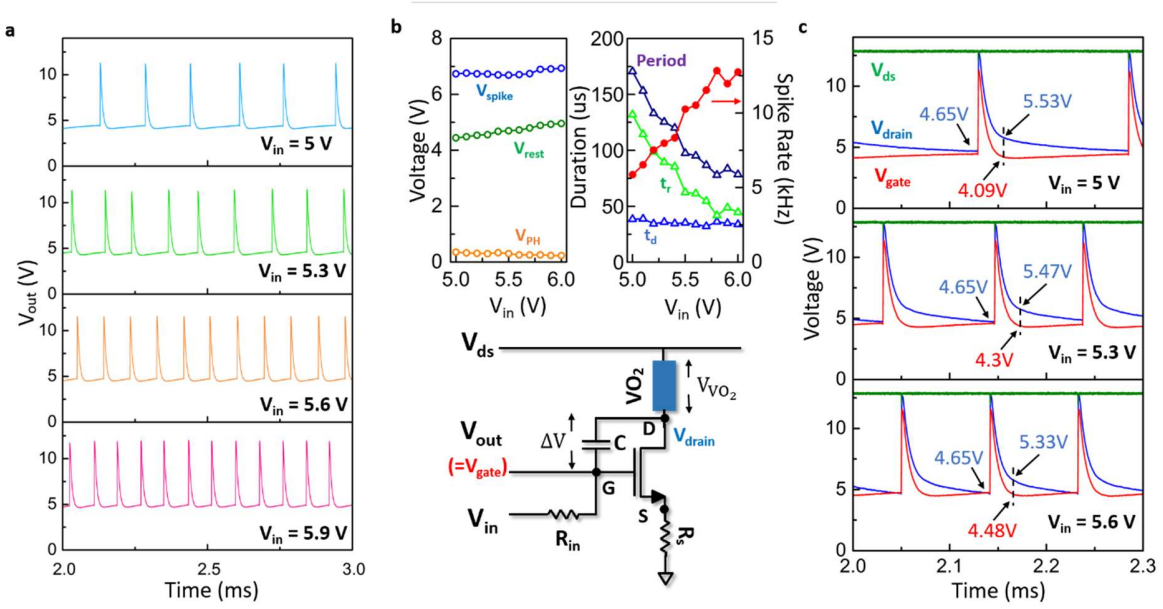


**Figure 3 | Spike trains measured under different input voltages. (a)** Traces of spike trains measured under different input voltage levels ($V_{in}$ = 5 V, 5.3 V, 5.6 V, 5.9 V from top to down, respectively). Supply voltage $V_{ds}$ = 13 V. **(b)** Variation of spike characteristics under different input voltage levels. **Left**: voltage characteristics ($V_{spike}$, $V_{PH}$, $V_{rest}$) vs $V_{in}$. **Right**: duration characteristics ($t_d$, $t_r$, period, spike rate) vs $V_{in}$. **(c)** Traces of measured $V_{drain}$ and $V_{gate}$ (also $V_{out}$) under different $V_{in}$ values. The dashed line marks the voltage across the feedback capacitor, $\Delta V$. $V_{in}$ = 5 V, 5.3 V, 5.6 V from top to down, respectively.

**Frequency coding.** It is of interest to measure the change of the generated spike trains in response to different input voltage levels. This could potentially function as a frequency coding scheme, which is widely considered to be one of the main information coding strategies employed by the biological neural networks[13,40]. Figure 3-a demonstrates several spike trains under different input voltage levels. The waveforms in figure 3 were measured with the following circuit conditions: $R_s$ = 27.7 kΩ; $R_{in}$ = 42.8 kΩ; C = 770 pF; $VO_2$ device dimensions are W = 6 um and L = 6 um.

Figure 3-b shows the measured relationship between several spike characteristics and input voltage value. The shape of the spike, as determined by $V_{spike}$, $V_{PH}$ and $t_d$, is fairly constant under different input voltages. The refractory period shrinks with higher input voltage, which is consistent with the recordings in biological neurons[10,41], allowing for the information of input stimulus intensity (as represented by the input voltage value) to be coded in terms of the frequency or rate of the spike trains.

To understand the mechanism through which the frequency modulation takes place, it is useful to take a closer look at the waveforms of the drain voltage of the transistor, $V_{drain}$, as provided in figure 3-c. This information is important in the sense that $V_{drain}$ reflects the state of the $VO_2$ spike generator. As the supply voltage $V_{ds}$ is constant, $V_{drain}$ determines the voltage across the $VO_2$ device itself, which could be calculated as $V_{VO_2} = V_{ds} - V_{drain}$. It could also be used to measure the voltage across the feedback capacitor, defined as $\Delta V = V_{drain} - V_{gate}$. Note that $V_{gate}$ is also the output voltage, $V_{out}$. These voltages are illustrated on the inset circuit diagram in figure 3.

As mentioned in section 2, $V_{VO_2}$ determines the triggering of an IMT/MIT pair. Naturally, at the initiation point of a spike (a triggered IMT), this voltage is measured to be invariant w.r.t. $V_{in}$ ($V_{ds}$ = 13 V, $V_{drain}$ = 4.65 V, thus $V_{VO_2}$ = 8.35 V for all traces shown), as shown in figure 3-c. On the other hand, $\Delta V$ reflects the charges being stored on the capacitor. This charge could be calculated as $Q = C \cdot \Delta V$. Interestingly, for higher input voltage, it is observed that less amount of charge is stored on the capacitor, as $\Delta V$ is shown to be decreasing in figure 3-c.

This observation is important, because the stored charge is the only measure of the degree of asymmetry between the pre-spike and post-spike states of the circuit. When there is less amount of charge stored on the capacitor, it takes less time to discharge it to the pre-spike state. The length of the refractory period is determined by the time needed to discharge the capacitor to its original pre-spike state, in which a new spike would be triggered. Hence, with higher input voltages, the length of the refractory period would reduce, resulting in the increase of frequency or spike rate.

This mechanism closely resembles its biological counterparts in principle. The refractory period in the spike trains of biological neurons is believed to be the result of decreased voltage responsiveness of the ion channels on the membrane of the neuron[10]. Aside from a short duration of an absolute refractory period[12], when it's absolutely impossible for the neuron to fire another action potential, the majority of the duration of a refractory period is a relative refractory period. During this period, the threshold of firing is raised above the resting value and decays non-linearly with time[12]. Hence, an increased intensity of stimulus would shorten the relative refractory period, thus increasing the firing rate.

**Simplified spike generator circuit**. The action potentials carry information within a biological neural network. The regular spiking neuron circuit described in previous sections could reproduce biological action potentials to a certain degree, and it's potentially useful for translating input stimulus into spike trains during the first stage of processing.

However, there are two reasons to utilize spikes in a simpler fashion. Firstly, for the neurons to function in an electronic circuit, the spike trains don't necessarily have to carry all the details resembling a biological spike train. Secondly, in any neuromorphic circuit employing such spiking neuron devices, both the input and output signals of any neuron would be spikes, instead of the constant voltage levels used previously.

Therefore, in the designs described in the following sections, where the target is to perform computation based on spikes, the spike generation has been simplified to be performed by the basic $VO_2$ spike generator circuit, which has been described in section 2. This allows for a more compact design, thus leaving space

for more functionality. A $VO_2$ device (dimensions: L = 6 um, W = 4 um) is connected to the drain of a series transistor. This circuit is again presented in figure 4-a.

Another modification is that the input signals are configured to be a DC bias plus an AC spike train of small amplitudes. The AC signals are intended as the real inputs. The bias is added for its potential usefulness in configuring different neuron circuits with different circuit parameters. In real applications, this bias could be replaced by adding another transistor in parallel with the series transistor shown in figure 4-a. For the simplicity of experiment, in all the measurements presented in this paper, a DC bias plus an AC signal is added to the gate of a single series transistor.

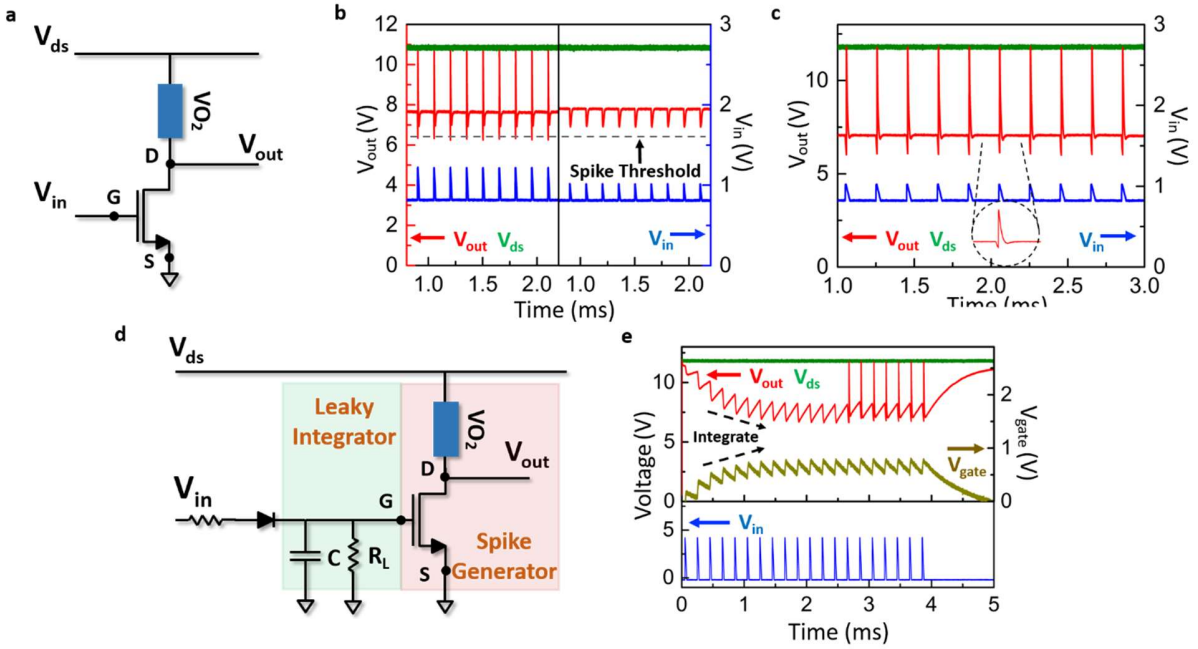


**Figure 4 |Measurements of the simplified $VO_2$ spike generator and the leaky integrate-and-fire functionality. (a)** Circuit diagram of $VO_2$ spike generator. **(b)** Input signal sufficient (**Left**) or insufficient (**Right**) to trigger output spikes. **(c)** Waveform measured at output node under input voltage spikes. $V_{in}$ is an AC pulse signal added to a DC level (DC = 0.9 V, AC = 0.2 V). **Inset**: shape of an individual output spike. **(d)** Circuit diagram to implement leaky integrate-and-fire functionality. **(e)** The measured waveform.

The DC bias settles the voltage at the output node, $V_{out}$, to a resting value. When the input spike in the form of the AC signal arrives at the gate of the transistor, the transistor is further turned on, hence $V_{out}$ dips in response. The voltage across the $VO_2$ device is determined by $V_{out}$. As illustrated in figure 4-b, under any DC bias, there is always a threshold for which the $V_{out}$ dip has to cross in order to fire a spike. If the dip is sufficient to trigger the $VO_2$ device to undergo IMT/MIT transitions, an output spike with ~5 V amplitude would be generated, as depicted in figure 4-c.

This simplified design of a spike generator circuit is by itself a mere translation of input spike trains into output spike trains. However, it provides the possibilities for the implementation of other useful functions on top of it.

**Leaky integrate-and-fire.** A biological neuron generates and transmits an action potential in response to the action potentials received from other neurons. Although a biological neuron is fairly slow (typically in ~miniseconds) compared to the speed of electronic devices, they are very powerful in terms of computation. One of the reasons for this is that any individual neuron is able to perform weighted integration of both

spatial and temporal information from thousands of its presynaptic neurons[3]. This has inspired various artificial neural network models[14,15], dating back to McCulloch & Pitt's perceptron network[42] in 1943.

One of the simplest spiking neuron models inspired by this biological property is known as a leaky integrate-and-fire neuron model[39]. This neuron performs temporal integration. The concept is that, the post-synaptic neuron only fires an action potential once the firing threshold is crossed. The neuron integrates temporally the pre-synaptic spikes, while simultaneously checking whether or not the threshold has been crossed. Being "leaky" means that the integration of any input spike is weighted by its time of arrival, i.e., the earlier the spike arrives, the less impact it has on the post-synaptic neuron.

Figure 4-d presents a possible implementation of such leaky integrate-and-fire functionality. A leaky integrator consists of a capacitor C and a leaky resistor $R_L$. It is connected to the gate terminal of the series transistor in the $VO_2$ spike generator circuit. As this design is targeted to be the post-synaptic neuron of other pre-synaptic neurons, additional components were added to simulate the inputs from other neurons. Namely, the input voltage signal is converted to current spikes through an input resistor and a diode. This seeks to represent the commonly accepted concept[43] that a synapse in a spiking neural network functions as a resistance. It is unclear whether the diode serves any importance computationally, but functionally, it provides isolation between pre-synaptic and post-synaptic neurons, while making the information flow unidirectionally, as in a biological neural network.

When a train of input spikes arrives, charges are accumulated on the capacitor and leaked through the resistor. This is reflected in the level of gate voltage. $V_{gate}$ is hence the temporal integration of input voltage spikes, weighted by the arrival time of individual spikes. Output spikes are generated when the gate voltage reaches the threshold to fire. This behavior is shown in figure 4-e, where the circuit parameters are as follows: C = 4.7nF; $R_L$ = 168 kΩ; $R_{in}$ = 30 kΩ. It should be pointed out that the demonstration presented here is still very primitive in terms of real functionality.

**Inhibition.** The simplified spike generator circuit also facilitates a way to implement the inhibitory function. Most spiking neural network models consider the inhibitory synapses to be implemented as some form of negative synaptic weights connecting two neurons. This is relatively easy to accomplish if the underlying physical circuit transmits digital spikes and stores synaptic weights in digital bits, such as in the TrueNorth chip developed by IBM[4,44]. However, it is still useful to look at the potential of implementing the inhibitory function directly on the neuron circuit, while maintaining all the synaptic weights to be positive.

One possible design is illustrated in figure 5-a. In addition to the simplified spike generator circuit introduced in previous sections, an inhibitory input was added through the gate of a second transistor connected in parallel with the $VO_2$ device. This neuron circuit, with both the excitatory and inhibitory inputs, is hence referred to as a principle neuron circuit, as per the convention used in neuroscience[16].

Both M1 and M2 are n-channel transistors. The leaky integrator component as well as the diode for the excitatory input was omitted from this circuit, as this measurement is intended to demonstrate the inhibitory functionality only. But they could be added in real circuits, nonetheless, without affecting the inhibitory input. The output signal is read from the common node of the two transistors. In the following measurements in figure 5, the $VO_2$ device has dimensions of W = 6 um and L = 6 um.

The input signals are a combination of a DC bias and an AC signal. The amplitude of the excitatory AC signal is referred to as $V_{exc}$, while the amplitude of the inhibitory AC signal is referred to as $V_{inh}$. The excitatory input signal is kept the same as in previous sections, for simplicity of demonstration. Therefore, the main difference between these two signals is that the excitatory signal is very small in DC and AC amplitudes, hence it could not be directly connected as the output of another neuron circuit. Several ways could be exploited to circumvent this problem. One of them is to add a leaky integrator. Another possible

solution is to add a voltage adapting component between the output of a pre-synaptic neuron circuit and the excitatory input of a post-synaptic neuron. This approach is demonstrated in the next section.

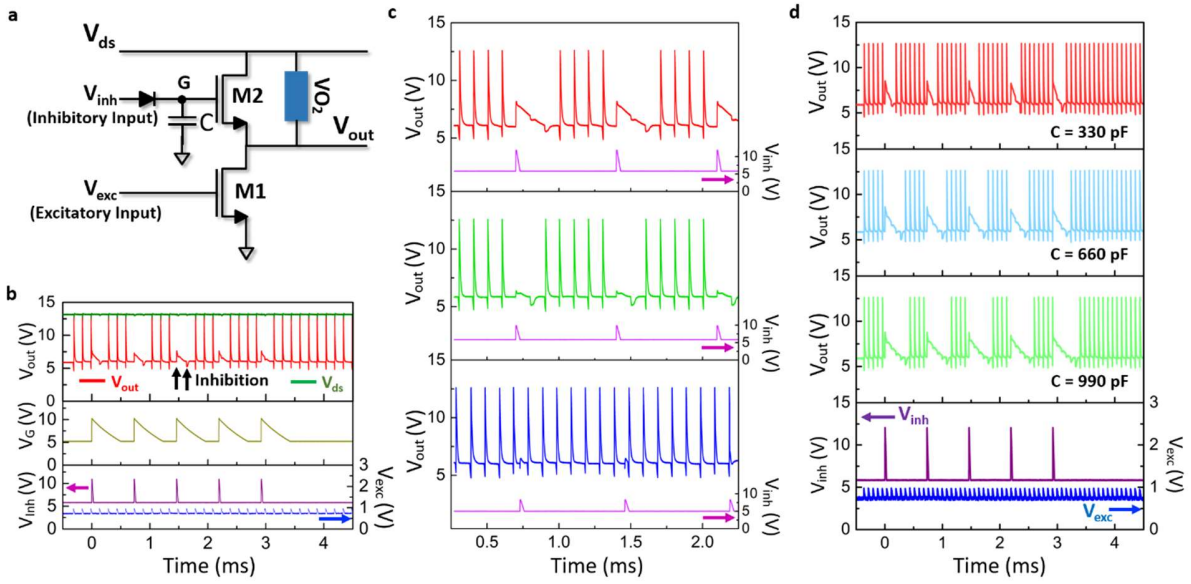


**Figure 5 | Experimental demonstration of Inhibition. (a)** Circuit diagram of a $VO_2$ spiking neuron with excitatory and inhibitory inputs. **(b)** Measured waveform showing inhibitory function. Excitatory and inhibitory signals are both voltage spikes ($V_{exc}$ = 0.2 V, DC bias = 1 V, spike interval = 150 us; $V_{inh}$ = 5 V, DC bias = 8.5 V, spike interval = 730 us). **(c)** Inhibitory function depends on the amplitude of the inhibitory input signal. From top to down, $V_{inh}$ = 6V (DC = 6 V), 4 V (DC = 6 V), 3.3 V (DC = 5.7 V), respectively (spike interval = 700 us). **(d)** Inhibitory functionality measured under same input signal ($V_{exc}$ = 0.2 V, DC bias = 1 V, spike interval = 150 us; $V_{inh}$ = 6.2 V, DC bias = 9 V, spike interval = 730 us) with different capacitance values. Supply voltage $V_{ds}$ = 13.5 V.

The inhibitory signal should be expected to maintain a certain effective period. This is realized by connecting a capacitor to the gate of the transistor M2. A leaky resistor could also be added in parallel to the capacitor to facilitate discharging. In measurements for figure 5, the discharging path is through the reversely biased diode itself, while discharging through a large leaky resistor is demonstrated in figure 6 in the next section.

The inhibitory function is demonstrated in figure 5-b. The inhibitory signal charges the capacitor, raising the voltage at gate terminal, $V_G$. This reduces the channel resistance of transistor M2, thus raising the resting voltage level at the output node, as shown by the increased value of $V_{out}$ immediately following an inhibitory spike. During the effective period of an inhibitory input spike, the neuron is inhibited from generating output spikes. This is manifested by the voltage dips of $V_{out}$, induced by excitatory input spikes, which are insufficient to reach the threshold for the neuron circuit to fire an output spike, similar to the situation in figure 4-b in the previous section. As $V_G$ discharges, the resting level of $V_{out}$ drops to its normal value, where an excitatory spike could then initiate an output spike.

Conceptually, the effect of an inhibitory signal is surely related to the amplitude of the inhibitory signal itself, as evident in the waveforms shown in figure 5-c, where the inhibitory effects induced by different inhibitory input signals are measured. The excitatory input signal is $V_{exc}$ = 0.2V with a DC bias = 0.93V,

and a spike interval = 100 us, for all waveforms. Larger signal amplitude leads to prolonged effective periods of inhibition, as expected. Figure 5-d further confirms the impact of the capacitor. Under the same input signals, it was observed that larger capacitance value leads to longer periods of inhibition.

These results provided some insights into designing the conditions for the inhibitory input to function properly in a real spiking neuron circuit. It should be noted that the inhibitory function would be most useful when a neuron takes the inhibitory input signal from other neurons' outputs. With this consideration, the inhibitory input signal should be designed to match the actual output signal of a spiking neuron circuit in terms of the amplitude and duration of the spike.

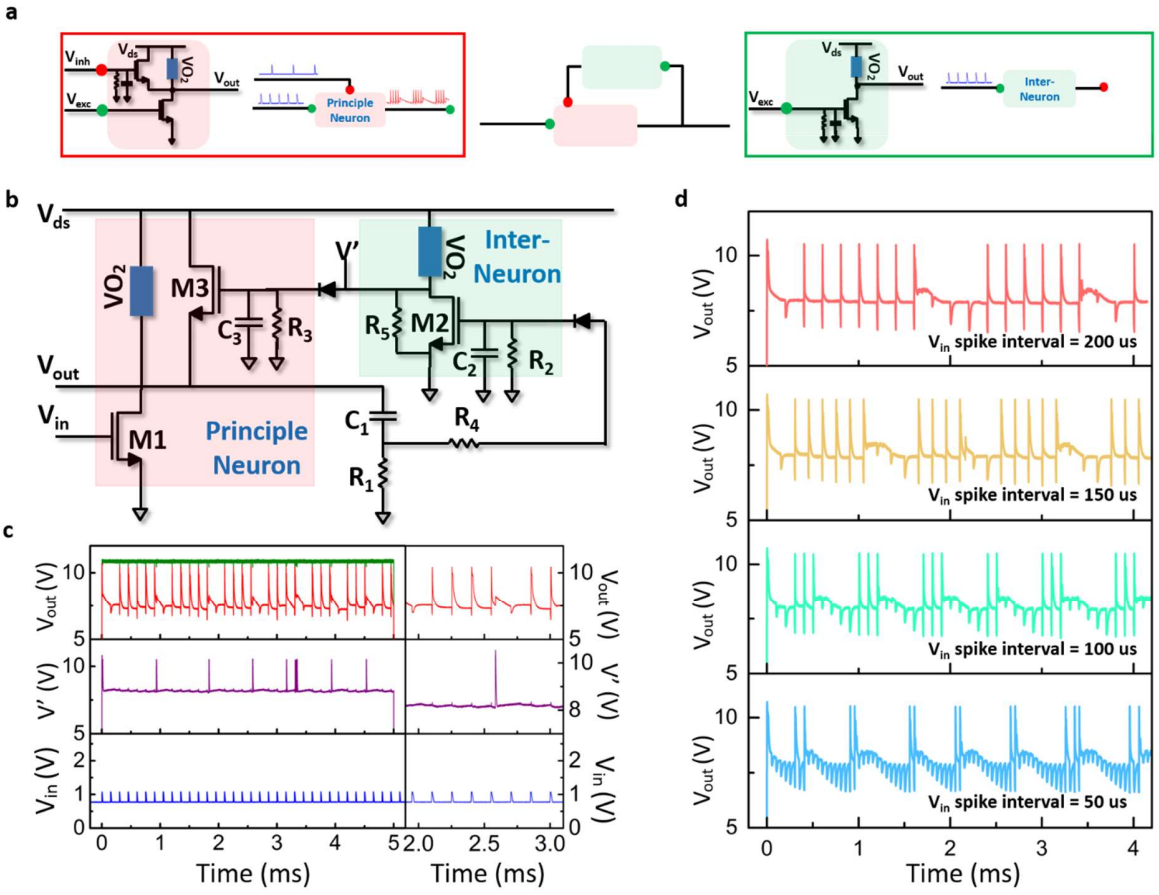


**Figure 6 | Experimental demonstration two $VO_2$ based spiking neurons interacting. (a)** Illustration of the recurrent inhibition circuitry. **(b)** Physical circuit diagram of recurrent inhibition implementation. **(c)** Measured waveform showing recurrent inhibition. Input signal to the principle neuron are excitatory voltage spikes ($V_{in}$ = 0.3 V, DC bias = 0.85 V, spike interval = 150 us). Supply voltage $V_{ds}$ = 11 V. **Right**: waveform between time window 2 to 3 ms to show the details of recurrent inhibition. **(d)** Traces output waveforms ($V_{out}$) under different input spike rates ($V_{in}$ = 0.4 V, DC bias = 0.88 V; spike intervals = 200 us, 150 us, 100 us, 50 us from top to down, respectively). Supply voltage $V_{ds}$ = 11 V. The circuit under test has the same parameters as in **c**, with the exception of $R_2$ = 333 kΩ.

**Neuron-neuron interaction.** A simple way to test the functionality of the VO2 based spiking neurons is to measure the interaction of two such neuron circuits in a configuration as illustrated in figure 6-a.

Known as the recurrent inhibition circuitry in neuroscience, this configuration is commonly found in biological nervous systems[16,17,19,45]. It comprises of two neurons. One is a principle neuron circuit, which, as mentioned in the previous section, is implemented to have both the excitatory and inhibitory inputs. The

other neuron is referred to as an interneuron circuit, which is a leaky integrate-and-fire neuron circuit with only the excitatory input node. The interneuron takes excitatory inputs from the output of the principal neuron and inhibits the principal neuron through feedback.

Figure 6-b depicts the physical components of the recurrent inhibition circuitry. The detailed circuitry of both the principle and inter neurons have been discussed in previous sections. As mentioned previously, a leaky resistor, $R_3$, is added to the inhibitory input of the principle neuron. The interneuron is further biased with a parallel resistor $R_5$ to provide initialization of the measurements (otherwise the output of the interneuron would be fixed at $V_{ds}$). This would not pose additional problems for real applications, as both the principle and inter neurons would be biased using extra biasing signals.

As the excitatory input signal to the interneuron has smaller amplitudes compared to the output of the principle neurons, a voltage adaption component is connected between the two neurons to circumvent this problem. Here, the voltage adaptation component is simply a high-pass filter, comprising of $C_1$, $R_1$ and $R_4$. This problem arises mainly from insufficient optimization of the parameters of the circuitry, but in principle, should not limit the feasibility of the demonstration.

In these measurements, the circuit under test consisted two $VO_2$ devices, both of which have dimensions of W = 4 um and L = 6 um. The circuit components are discrete, and have the following values: $C_1$ = 330 pF; $C_2$ = 4.7 nF; $C_3$ = 990 pF; $R_1$ = 9.8 kΩ; $R_2$ = 236 kΩ; $R_3$ = 0.95 MΩ; $R_4$ = 1.7 kΩ; $R_5$ = 65 kΩ.

The recurrent inhibition functionality is demonstrated in the waveforms in figure 6-c. The voltage V' refers the output of the interneuron, which is connected to the inhibitory input of the principle neuron. It is observed that, under a train of excitatory spikes, the output of the principle neuron showed a pattern of bursting, where groups of spikes were interrupted by relatively constant intervals of resting. This observation is very similar to that found in the recurrent inhibition circuitry in biological nervous system[46]. It could be concluded that the reason for this bursting pattern is that principle neuron is periodically inhibited by the interneuron.

Figure 6-d illustrates the potential to use such inhibitory functions as a way to count the rate of input excitatory spikes. As shown in the figure, when the input spike rate is increased, the output bursts have fewer spikes in each of the bursting groups before an inhibitory interval interrupts the spike train. Although the demonstrations showed in figure 6 were quite primitive and have no practical usefulness, it does show implications that the idea of several such $VO_2$ based spiking neuron circuits interacting with each other is feasible.

In a real circuit, several principle neurons could take the input spike trains with different spike rates, as translated from the intensity of the actual input stimulus, such as the pixel values in a 2-D image. If these principle neurons inhibit each other laterally through various interneurons[47], such a network could potentially be used to pick the maximal input spike rate, as the principle neuron receiving the maximal spike rate would naturally inhibit all other principle neurons

# 4. Discussions

**This work.** The results presented in this work were limited to functional demonstrations. The circuit design, parameters as well as input conditions were not carefully optimized. The idea of using spikes to perform computation was, in part, conceptually demonstrated through various measurements of $VO_2$ based discrete circuits. However, the feasibility, usefulness as well as efficiency for building larger, more meaningful circuits with these $VO_2$ based spiking neuron circuits for real scale applications, remained unanswered. This

was partly a result of the difficulty encountered in the measurements, when trying to demonstrate more than two neurons interacting in a circuit.

**The idea of brain-inspired computation.** This work also calls into question the very idea of neuromorphic engineering, as many other works have previously pointed out. The neuromorphic engineering approach seeks to mimic the way a biological neural network does computation by implementing real spikes and synapses in electronic circuits. However efficient the physical implementation might become in the future, it is far from clear whether or not such an attempt is practical in light of scaling up the complexity of such spiking neuron networks.

On the other hand, the concept of a brain performing computation is in itself still ambiguous. It has been shown in neuroscience research, that biological neural networks indeed perform complex computations. These operations could be accomplished by either a single neuron[48], a group of neurons[49], or a network of neurons[50]. Marr & Poggio[51] proposed a tri-level analysis to understand how does a biological neural network compute. It is therefore questionable to restrict the computations performed by a biological neural network as being only feasible if implemented with a physical substrate, or hardware, that has similar properties and structures as its biological counterparts.

For instance, recent years, deep neural networks running on conventional digital computers (optimized for parallel data processing) have been proven to be highly effective in performing tasks that were previously considered to be the expertise of biological nervous systems only[52-54].The physical hardware of such approach bears also no resemblance with the biological nervous system, although the structure of the mathematical model of deep neural networks does draw some of its insights from the hierarchical organization of visual cortex in primates[50,52].

# 5. Conclusion

In this paper, measurement results of several $VO_2$ based spiking neuron circuits were presented. These circuits could be seen as extensions from the $VO_2$ oscillator device originally conceived by Nikhil Shukla et al. The circuits could generate biologically similar action potentials with potential usefulness in implementing frequency coding scheme. Other designs aimed at implementing leaky integrate-and-fire as well as inhibition functionalities using as little circuit components as possible. Area efficiency was a major concern in these designs. Functional demonstrations of such designs were illustrated and discussed. This was followed by the endeavor to show that multiple such neuron circuits could interact with each other in a circuit, done in the form of presenting the measurements on a simple two-neuron recurrent inhibition circuitry. In summary, although functionally confirming, the results in this work were, in large sense, exploratory, providing only insights but not feasibility of or justification to the concept of using $VO_2$ based spiking neuron circuits for real applications.

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## References & Bibliography


1. O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, S. Ma, Z. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, "ImageNet Large Scale Visual Recognition Challenge," *Int. J. Comput. Vis.*, vol. 115, no. 3, pp. 211–252, 2015.
2. W. Xiong, J. Droppo, X. Huang, F. Seide, M. Seltzer, A. Stolcke, D. Yu, and G. Zweig, "Achieving Human Parity in Conversational Speech Recognition," *arXiv*, no. February, 2016.
3. D. Debanne, A. Bialowas, and S. Rama, "What are the mechanisms for analogue and digital signaling in the brain?" *Nat. Rev. Neurosci.*, vol. 14, no. 1, pp. 63–9, 2013.
4. P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science (80-. ).*, vol. 345, no. 6197, pp. 668–673, Aug. 2014.
5. E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic electronic circuits for building autonomous cognitive systems," *Proc. IEEE*, vol. 102, no. 9, pp. 1367–1388, 2014.
6. C. Mead, "Neuromorphic Electronic Systems," *Proc. IEEE*, vol. 78, no. 10, pp. 1629–1636, 1990.
7. G. Indiveri and T. K. Horiuchi, "Frontiers in neuromorphic engineering," *Front. Neurosci.*, vol. 5, no. OCT, pp. 1–2, 2011.
8. A. S. Cassidy, P. Merolla, J. V. Arthur, S. K. Esser, B. Jackson, R. Alvarez-Icaza, P. Datta, J. Sawada, T. M. Wong, V. Feldman, A. Amir, D. B. D. Rubin, F. Akopyan, E. McQuinn, W. P. Risk, and D. S. Modha, "Cognitive computing building block: A versatile and efficient digital neuron model for neurosynaptic cores," *Proc. Int. Jt. Conf. Neural Networks*, 2013.
9. B. P. Bean, "The action potential in mammalian central neurons," *Nat. Rev. Neurosci.*, vol. 8, no. 6, pp. 451–465, Jun. 2007.
10. Eric R. Kandel, James H. Schwartz, Thomas M. Jessell, Steven A. Siegelbaum, A. J. Hudspeth, Sarah Mack, *Principles of Neural Science, Fifth Editon*.
11. A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *Bull. Math. Biol.*, vol. 52, no. 1–2, pp. 25–71, 1990.
12. J. S. Yeomans, "The absolute refractory periods of self-stimulation neurons," *Physiol. Behav.*, vol. 22, no. 5, pp. 911–919, 1979.
13. R. VanRullen and S. J. Thorpe, "Rate coding versus temporal order coding: what the retinal ganglion cells tell the visual cortex.," *Neural Comput.*, vol. 13, no. 6, pp. 1255–83, 2001.
14. Wulfram Gerstner, Werner M. Kistler, Spiking *Neuron Models: Single Neurons, Populations, Plasticity*
15. E. M. Izhikevich, "Which model to use for cortical spiking neurons?" *IEEE Trans. Neural Networks*, vol. 15, no. 5, pp. 1063–1070, 2004.
16. J. J. Couey, A. Witoelar, S.-J. Zhang, K. Zheng, J. Ye, B. Dunn, R. Czajkowski, M.-B. Moser, E. I. Moser, Y. Roudi, and M. P. Witter, "Recurrent inhibitory circuitry as a mechanism for grid formation.," *Nat. Neurosci.*, vol. 16, no. 3, pp. 318–24, 2013.
17. H. Hu, J. Gan, and P. Jonas, "Interneurons. Fast-spiking, parvalbumin$^{+}$ GABAergic interneurons: from cellular design to microcircuit function.," *Science*, vol. 345, no. 6196, p. 1255263, 2014.
18. J. Simonnet, M. Nassar, F. Stella, I. Cohen, B. Mathon, N. Boccara, R. Miles, and D. Fricker, "How activity dependent feedback inhibition may maintain head direction signals in mouse presubiculum," 2017.
19. G. S. Bhumbra, B. A. Bannatyne, M. Watanabe, A. J. Todd, D. J. Maxwell, and M. Beato, "The recurrent case for the Renshaw cell.," *J. Neurosci.*, vol. 34, no. 38, pp. 12919–12932, 2014.
20. J. Zhu, M. Jiang, M. Yang, H. Hou, and Y. Shu, "Membrane potential-dependent modulation of recurrent inhibition in rat neocortex," *PLoS Biol.*, vol. 9, no. 3, 2011.
21. L. F. Abbott, B. DePasquale, and R. Memmesheimer, "Building functional networks of spiking model neurons," *Nat. Neurosci.*, vol. 19, no. 3, pp. 350–355, Feb. 2016.

22. G. Indiveri, B. Linares-Barranco, T. J. Hamilton, A. van Schaik, R. Etienne-Cummings, T. Delbruck, S. C. Liu, P. Dudek, P. Hafliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Folowosele, S. Saighi, T. Serrano-Gotarredona, J. Wijekoon, Y. Wang, and K. Boahen, "Neuromorphic silicon neuron circuits," *Front. Neurosci.*, vol. 5, no. MAY, pp. 1–23, 2011.
23. I. Sourikopoulos, S. Hedayat, C. Loyez, F. Danneville, V. Hoel, E. Mercier, and A. Cappy, "A 4-fJ/Spike Artificial Neuron in 65 nm CMOS Technology," *Front. Neurosci.*, vol. 11, no. March, pp. 1–14, 2017.
24. Sengupta, A., & Roy, K. (2015). Spin-Transfer Torque Magnetic neuron for low power neuromorphic computing. In *International Joint Conference on Neural Networks (IJCNN)* (pp. 1–7). IEEE.
25. M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with Mott memristors.," *Nat. Mater.*, vol. 12, no. 2, pp. 114–7, 2013.
26. T. Tuma, A. Pantazi, M. Le Gallo, A. Sebastian, and E. Eleftheriou, "Stochastic phase-change neurons," *Nat. Nanotechnol.*, vol. 11, no. 8, pp. 693–699, May 2016.
27. P. Stoliar, J. Tranchant, B. Corraze, E. Janod, M.-P. Besland, F. Tesler, M. Rozenberg, and L. Cario, "A Leaky-Integrate-and-Fire Neuron Analog Realized with a Mott Insulator," *Adv. Funct. Mater.*, 2017.
28. N. Shukla, A. Parihar, E. Freeman, H. Paik, G. Stone, V. Narayanan, H. Wen, Z. Cai, V. Gopalan, R. Engel-Herbert, D. G. Schlom, A. Raychowdhury, and S. Datta, "Synchronized charge oscillations in correlated electron systems.," *Sci. Rep.*, vol. 4, p. 4964, 2014.
29. E. M. Izhikevich, "Simple model of spiking neurons," *IEEE Trans. Neural Networks*, vol. 14, no. 6, pp. 1569–1572, 2003.
30. O. Nájera, M. Civelli, V. Dobrosavljević, and M. J. Rozenberg, "Resolving the $VO_2$ controversy: Mott mechanism dominates the insulator-to-metal transition," *Phys. Rev. B*, vol. 95, no. 3, p. 35113, Jan. 2017.
31. M. M. Qazilbash, M. Brehm, B.-G. Chae, P.-C. Ho, G. O. Andreev, B.-J. Kim, S. J. Yun, A. V Balatsky, M. B. Maple, F. Keilmann, H.-T. Kim, and D. N. Basov, "= 4 ns, we obtain a readout energy efficiency of 25%, defined as the energy of the released pulse divided by the energy of the incident data pulse. For T," *Science.*, vol. 318, no. December, pp. 1750–1753, 2007.
32. W.-Y. Tsai, X. Li, M. Jerry, B. Xie, N. Shukla, H. Liu, N. Chandramoorthy, M. Cotter, A. Raychowdhury, D. M. Chiarulli, S. P. Levitan, S. Datta, J. Sampson, N. Ranganathan, and V. Narayanan, "Enabling New Computation Paradigms with HyperFET - An Emerging Device," *IEEE Trans. Multi-Scale Comput. Syst.*, vol. 2, no. 1, pp. 30–48, Jan. 2016.
33. N. Shukla, A. V Thathachary, A. Agrawal, H. Paik, A. Aziz, D. G. Schlom, S. K. Gupta, R. Engel-Herbert, and S. Datta, "A steep-slope transistor based on abrupt electronic phase transition.," *Nat. Comm.*, vol. 6, p. 7812, 2015.
34. A. Pergament, A. Crunteanu, A. Beaumont, G. Stefanovich, and A. Velichko, "Vanadium Dioxide: Metal-Insulator Transition, Electrical Switching and Oscillations. A Review of State of the Art and Recent Progress," pp. 9–12, 2016.
35. A. Aziz, N. Shukla, S. Datta, and S. K. Gupta, "COAST: Correlated material assisted STT MRAMs for optimized read operation," *Proc. Int. Symp. Low Power Electron. Des.*, vol. 2015–Septe, no. Cm, pp. 1–6, 2015.
36. You Zhou, S. Ramanathan, "Mott Memory and Neuromorphic Devices," *Proc. IEEE*, vol. 103, no. 8, pp. 1289–1310, Aug. 2015.
37. H. T. Kim, B. J. Kim, S. Choi, B. G. Chae, Y. W. Lee, T. Driscoll, M. M. Qazilbash, and D. N. Basov, "Electrical oscillations induced by the metal-insulator transition in VO2," *J. Appl. Phys.*, vol. 107, no. 2, 2010.
38. J. C. Magee, "Dendritic integration of excitatory synaptic input," *Nat. Rev. Neurosci.*, vol. 1, no. 3, pp. 181–190, Dec. 2000.
39. M. A. Nahmias, B. J. Shastri, A. N. Tait, and P. R. Prucnal, "A leaky integrate-and-fire laser neuron for ultrafast cognitive computing," *IEEE J. Sel. Top. Quantum Electron.*, vol. 19, no. 5, 2013.
40. P. Reinagel and R. C. Reid, "Temporal coding of visual information in the thalamus.," *J. Neurosci.*, vol. 20, no. 14, pp. 5392–400, 2000.
41. M. J. Berry and M. Meister, "Refractoriness and neural precision.," *J. Neurosci.*, vol. 18, no. 6, pp. 2200–11, 1998.
42. W. S. McCulloch and W. Pitts, "A logical calculus of the ideas immanent in nervous activity," *Bull. Math. Biophys.*, vol. 5, no. 4, pp. 115–133, 1943.
43. D. Kuzum, S. Yu, and H.-S. Philip Wong, "Synaptic electronics: materials, devices and applications," *Nanotechnology*, vol. 24, no. 38, p. 382001, 2013.

44. J. Sawada, F. Akopyan, A. S. Cassidy, D. S. Modha et al, "TrueNorth Ecosystem for Brain-Inspired Computing: Scalable Systems, Software, and Applications," in *SC16: International Conference for High Performance Computing, Networking, Storage and Analysis*, 2016, pp. 130–141.
45. C. Buetfering, K. Allen, and H. Monyer, "Parvalbumin interneurons provide grid cell-driven recurrent inhibition in the medial entorhinal cortex," *Nat. Neurosci.*, vol. 17, no. 5, pp. 710–8, 2014.
46. R. J. Douglas, C. Koch, M. Mahowald, K. a Martin, and H. H. Suarez, "Recurrent excitation in neocortical circuits." *Science.*, vol. 269, no. 5226, pp. 1–5, 1995.
47. L. de Almeida, M. Idiart, and J. E. Lisman, "A second function of gamma frequency oscillations: an E%-max winner-take-all mechanism selects which cells fire.," *J. Neurosci.*, vol. 29, no. 23, pp. 7497–503, 2009.
48. H. Fotowat and F. Gabbiani, "Collision Detection as a Model for Sensory-Motor Integration," *Annu. Rev. Neurosci.*, vol. 34, no. 1, pp. 1–19, Jul. 2011.
49. D. H. Hubel and T. N. Wiesel, "Receptive fields, binocular interaction and functional architecture in the cat's visual cortex," *J. Physiol.*, vol. 160, no. 1, pp. 106–154, Jan. 1962.
50. D. J. Felleman and D. C. Van Essen, "Distributed hierachical processing in the primate cerebral cortex," *Cereb. Cortex*, vol. 1, pp. 1–47, 1991.
51. David Marr, *Vision. A Computational Investigation into the Human Representation and Processing of Visual Information*, 1982
52. Y. LeCun, Y. Bengio, and G. Hinton, "Deep learning," *Nature*, vol. 521, no. 7553, pp. 436–444, May 2015.
53. J. S. Chung, A. Senior, O. Vinyals, A. Zisserman, "Lip Reading Sentences in the Wild," *arXiv1611.05358 [cs]*, 2016.
54. Q. Liu, G. Pineda-García, E. Stromatias, T. Serrano-Gotarredona, and S. B. Furber, "Benchmarking Spike-Based Visual Recognition: A Dataset and Evaluation," *Front. Neurosci.*, vol. 10, no. November, p. 496, 2016.