



1. Description

1.1. Project

Project Name	Weed_F104_Time
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	10/24/2021

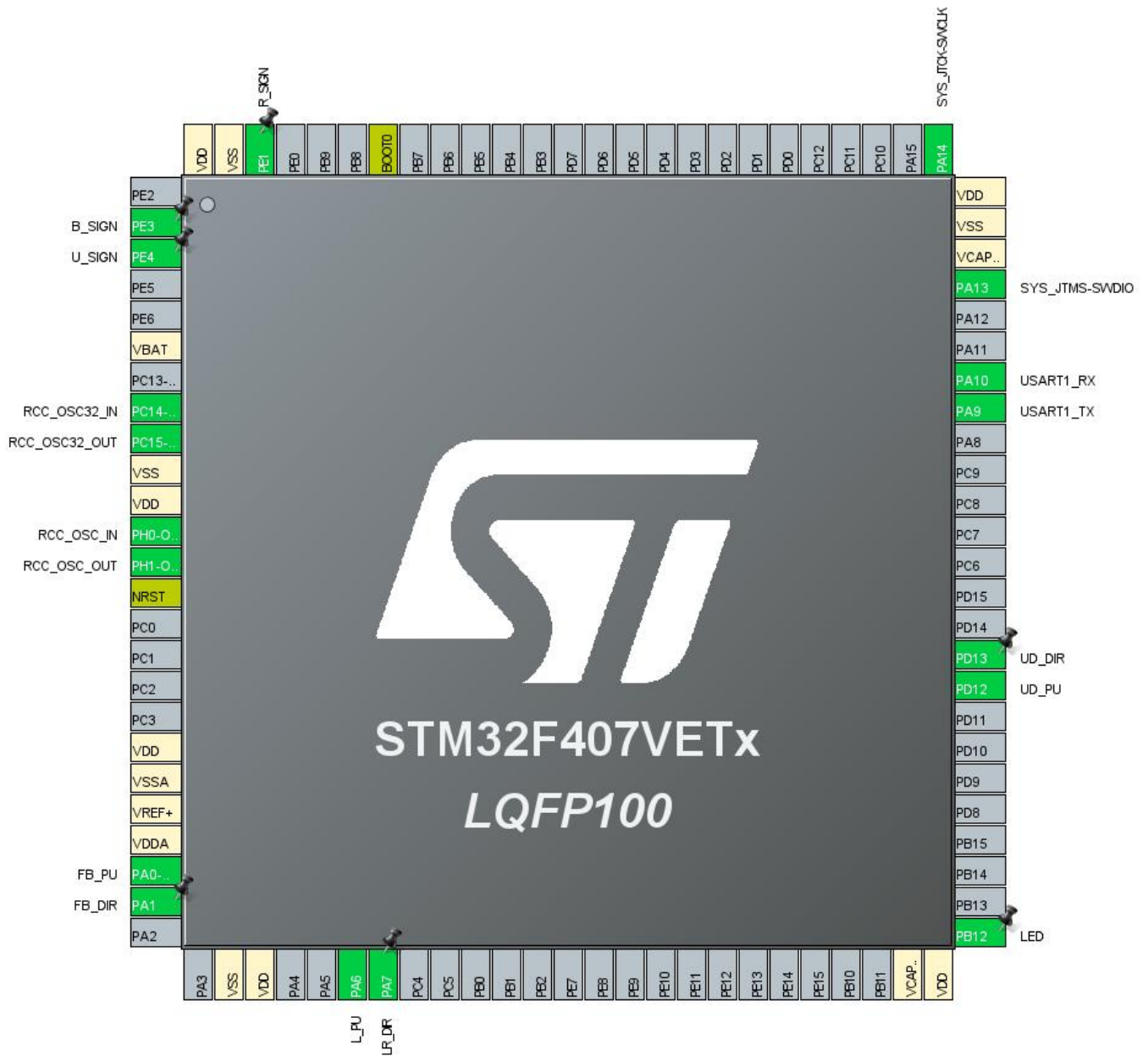
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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2. Pinout Configuration

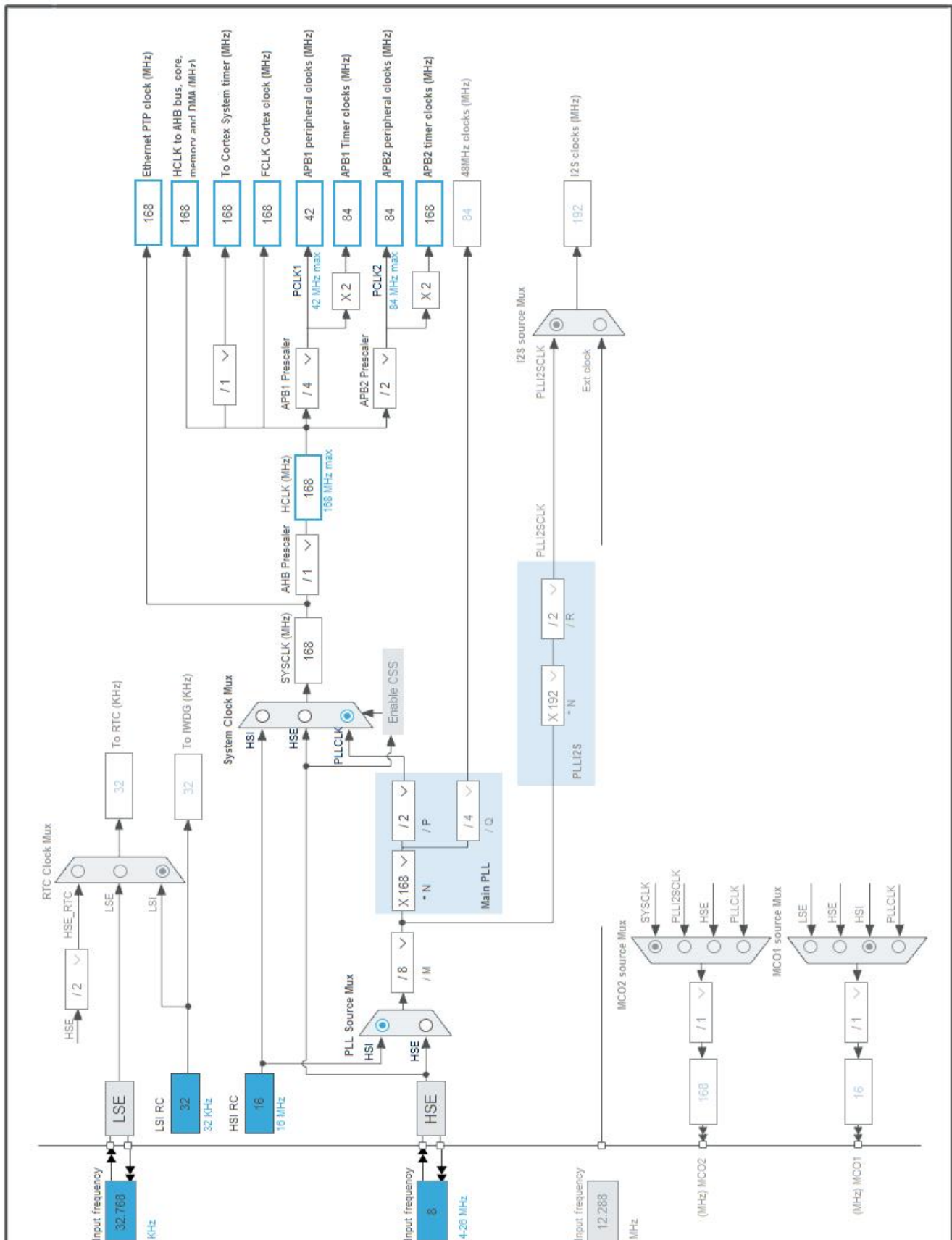


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3	I/O	GPIO_EXTI3	B_SIGN
3	PE4	I/O	GPIO_EXTI4	U_SIGN
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	FB_PU
24	PA1 *	I/O	GPIO_Output	FB_DIR
27	VSS	Power		
28	VDD	Power		
31	PA6	I/O	TIM3_CH1	L_PU
32	PA7 *	I/O	GPIO_Output	LR_DIR
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	LED
59	PD12	I/O	TIM4_CH1	UD_PU
60	PD13 *	I/O	GPIO_Output	UD_DIR
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
94	BOOT0	Boot		
98	PE1	I/O	GPIO_EXTI1	R_SIGN
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Weed_F104_Time
Project Folder	F:\STM32\Project\Weed_F104_Time
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_TIM3_Init	TIM3
4	MX_TIM4_Init	TIM4
5	MX_TIM5_Init	TIM5
6	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

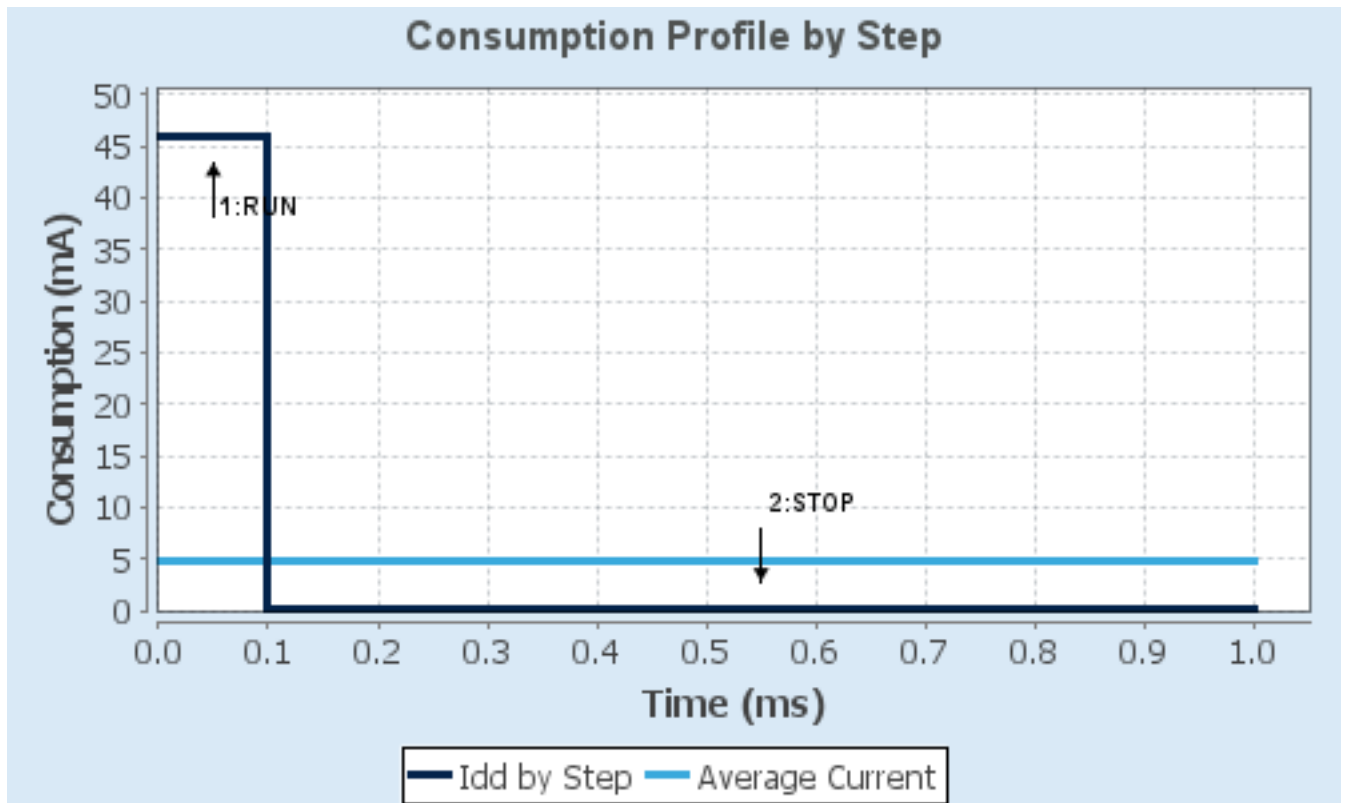
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μ A
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.47	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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7.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.3. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	41 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	100 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
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Trigger Event Selection

Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode

PWM mode 1

Pulse (16 bits value)

50 *

Output compare preload

Enable

Fast Mode

Disable

CH Polarity

High

7.4. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

41 *

Counter Mode

Up

Counter Period (AutoReload Register - 16 bits value)

100 *

Internal Clock Division (CKD)

No Division

auto-reload preload

Enable *

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode

PWM mode 1

Pulse (16 bits value)

50 *

Output compare preload

Enable

Fast Mode

Disable

CH Polarity

High

7.5. TIM5

mode: Clock Source

Channel1: PWM Generation CH1

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

41 *

Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	100 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *
Trigger Output (TRGO) Parameters:	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)
PWM Generation Channel 1:	
Mode	PWM mode 1
Pulse (32 bits value)	50 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:	
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1
Advanced Parameters:	
Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	L_PU
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	UD_PU
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	FB_PU
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PE3	GPIO_EXTI3	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	B_SIGN
	PE4	GPIO_EXTI4	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	U_SIGN
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	FB_DIR
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	LR_DIR
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	High *	UD_DIR
	PE1	GPIO_EXTI1	External Interrupt Mode with Falling	Pull-up *	n/a	R_SIGN

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			edge trigger detection			

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line1 interrupt	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
TIM3 global interrupt	true	2	0
TIM4 global interrupt	true	2	0
USART1 global interrupt	true	1	0
TIM5 global interrupt	true	2	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line1 interrupt	false	true	true
EXTI line3 interrupt	false	true	true
EXTI line4 interrupt	false	true	true
TIM3 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
TIM4 global interrupt	false	true	true
USART1 global interrupt	false	true	true
TIM5 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Security

Computing

DMA

TIM3



USART1



GPIO



TIM4



NVIC



TIM5



RCC



SYS



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00037051.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00031020.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00037591.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00025071.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00050879.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00123028.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

Application note http://www.st.com/resource/en/application_note/DM00154959.pdf

Application note http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00263732.pdf

Application note http://www.st.com/resource/en/application_note/DM00281138.pdf

Application note http://www.st.com/resource/en/application_note/DM00296349.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00373474.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

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Application note http://www.st.com/resource/en/application_note/DM00536349.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf