4 switches connection:

1st switch connects 6 xena ports: 0-0-0 to 0-0-5

2nd switch connects 4 xena ports: 0-2-0 to 0-2-3

3rd switch connects 4 xena ports: 0-2-4 to 0-2-5, 0-4-1 to 0-4-1

4th switch connects 4 xena ports: 0-4-2 to 0-4-5

Result for 2889 with 1 switch and 4 switches.

1. ***Address Caching Capacity Results:***

1 switch: 1504.

4 switches: 1504.

Each switch has 18 ports. So 1504 /18=83 switches. Within aging time, the address cache of one WR switch could only save 1504 items of MAC address and its port, 83 WR switches. More switches are used for FAIR, it could introduce much traffic by packet flooding for the address learning.

2. ***Congestion control***

1 switch: 64 bytes -> 256 bytes frame, no packet loss in uncongested port

4 switches: all length frames, packet loss in uncongested port. (no matter congested port and uncongested port are in the same switch or not)

3. ***Broadcast traffic (1->N or N->N)***

1 switch: 64 bytes -> 512 bytes frame, the throughput and forwarding could reach 900Mbps.

4 switches: 64 bytes -> 512 bytes frame, the throughput and forwarding could reach 900Mbps.

4. ***Unicast (1->N)***

1 switch: 64 bytes -> 1518 bytes frame, the throughput and forwarding could reach 900Mbps

4 switches: 64 bytes -> 1518 bytes frame, the throughput and forwarding < 100Mbps

5. Unicast (N->N, N<->N))

1 switch: 64 bytes -> 128 bytes frame, the throughput and forwarding < 100Mbps

256 bytes -> 1518 bytes frame, the throughput and forwarding could reach 900Mbps

4 switches: 64 bytes -> 1518 bytes frame, the throughput and forwarding < 100Mbps

6. ***Forward Pressure***

1 switch: no forward pressure

4 switches: no forward pressure

7. ***Error frame filter***

1 switch: WR switch could not filter oversize and undersize frames.

4 switches: WR switch could not filter oversize, undersize and FCS frames. WR switch causes FCS error.