EGCP-3210 **Computer Architecture** **Spring 2026**
Homework 2 **Brandon Aikman**

1. What is the difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? (5 pts)

   Direct address instructions contain the address of the operand, while indirect address instructions contain a 'pointer' to another location, which has the operand instruction. For direct address instructions, only one reference to memory is needed, but for indirect address instructions, at least two references to memory are necessary to bring an operand into a processor register.

2. Use the MANO machine data path diagram presented in the lecture notes to answer the following questions:

   (a) Explain why each of the following operations cannot be executed during a single clock pulse in the system shown in slide 8. (5pts)

      i. **To move the contents of what is located at the address of the program counter, the contents of the program counter must be loaded into the address register, then into the memory unit, and finally the memory unit can output the data on the bus which the instruction register can receive.**

      ii. **To update the accumulator by adding the temporary register to it, the data from the temporary register must be moved into the data register. Then, on the next clock cycle, it can go into the accumulator and be added.**

      iii. **First, the contents of the data register must be added to the accumulator. Then, the result can be put back onto the main bus and the data register can receive the summation.**

   (b) Specify a sequence of micro-operations that will perform the operation. (15pts, 5 each)

      i. IR←M[PC]

      AR←PC
      IR←M[AR](, PC←PC + 1)

      ii. AC←AC+TR

      DR←TR
      AC←AC + DR

iii. DR←DR+AC

AC←AC + DR
DR←AC

3. Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. (5 pts)

   (a) How many bits are needed for the program counter?
   24 bits.

   (b) What is the maximum directly addressable memory capacity?
   2^{32-8} **bits** = 2097152 **bytes.**

4. The content of PC in the MANO machine is 3AF. The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. (15 pts, 5 each)

   (a) What is the instruction that will be fetched and executed next?
   ADD (0x9xxx).

   (b) Show the binary operation that will be performed in the AC when the instruction is executed.
   1000101110011111 + 0111111011000011.

   (c) Give the contents of registers PC, AR, DR, AC, and IR in hexadecimal and the value of E, I, and the sequence counter in binary at the end of the instruction cycle.
   PC: 3B0
   AR: 9AC
   DR: 8B9F
   AC: 0A62
   IR: 932E
   E: 1
   I: 1
   SC: 0

5. Provide your insights on the article *It's Time for Clockless Chips*. (5 pts)

   The October 2001 article, *It's Time for Clockless Chips*, provides interesting insight into the state of the microprocessor design industry in the early 2000s. Looking back on strong claims about past technological developments that seemed to be on the brink of real, long-term success, we see that these products that are hyped up to the public seldom reach success and seldom provide lasting value to the public. Relating to this article, the author makes bold claims about the inevitability of the clockless microprocessor takeover, which, 25 years later, we can see never happened to scale.

Still, the article provides a good, high-level overview of the capabilities of clockless microprocessors, especially their applications. I think that the biggest takeaway from the article is that clockless chips are difficult to develop, but they can have certain niche applications that validate the costs associated with their development and fabrication.