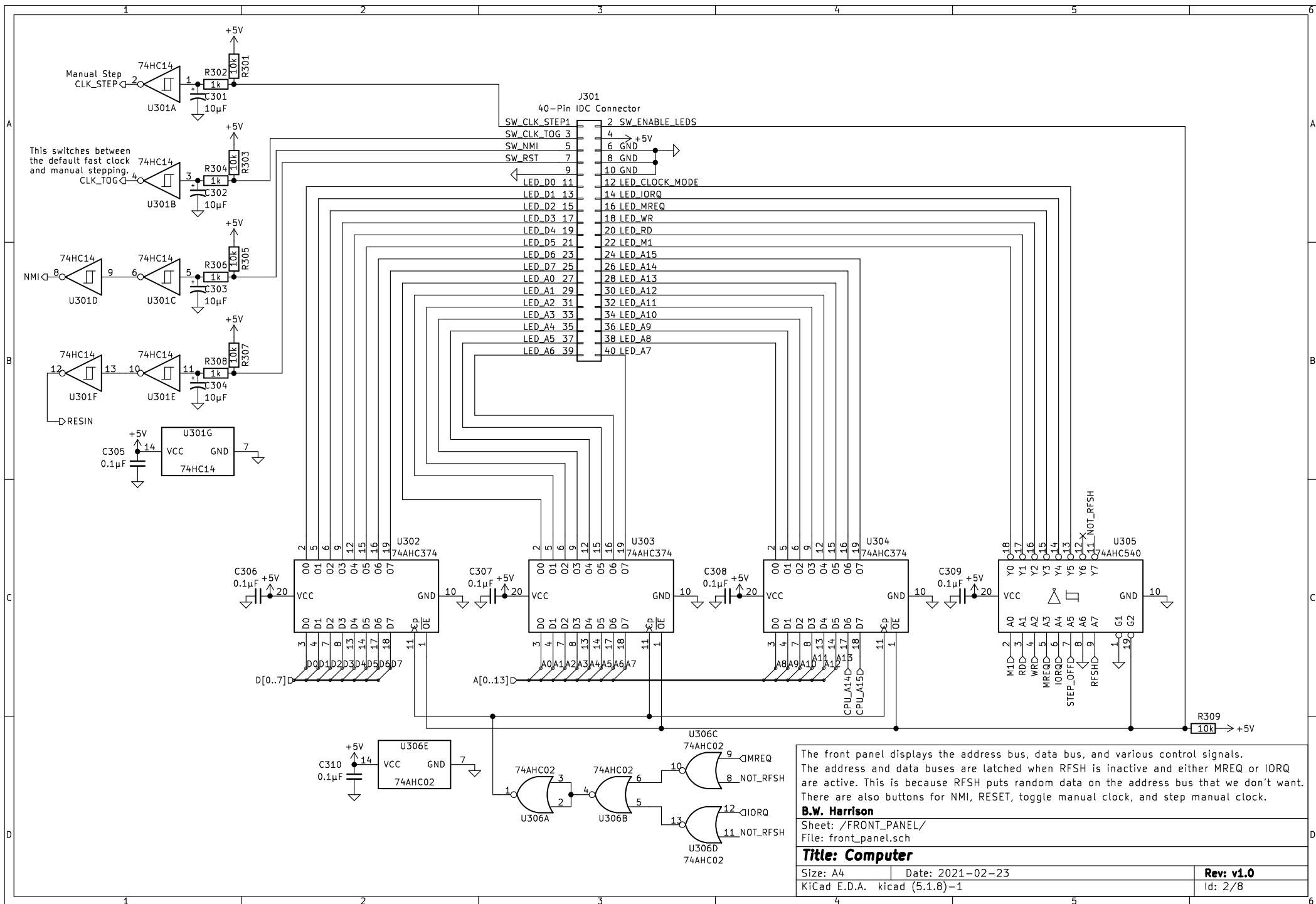


8-Bit Z80 computer motherboard 4 MB of pageable address space and 6 expansion slots 32 KB ROM and 512 KB RAM included The 40-pin IDC connector hooks up to the front panel switches and LEDs Bailey Harrison		
Sheet: / File: computer.sch		
Title: Computer		
Size: A4	Date: 2021-02-23	Rev: v1.0
KiCad E.D.A. kicad (5.1.8)-1		Id: 1/8



The front panel displays the address bus, data bus, and various control signals. The address and data buses are latched when RFSH is inactive and either MREQ or IORQ are active. This is because RFSH puts random data on the address bus that we don't want. There are also buttons for NMI, RESET, toggle manual clock, and step manual clock.

B.W. Harrison

Sheet: /FRONT_PANEL/

File: front_panel.sch

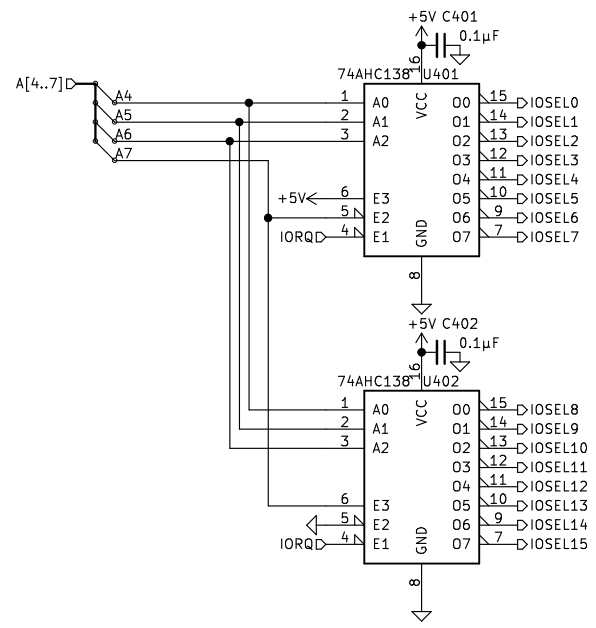
Title: Computer

Size: A4 Date: 2021-02-23

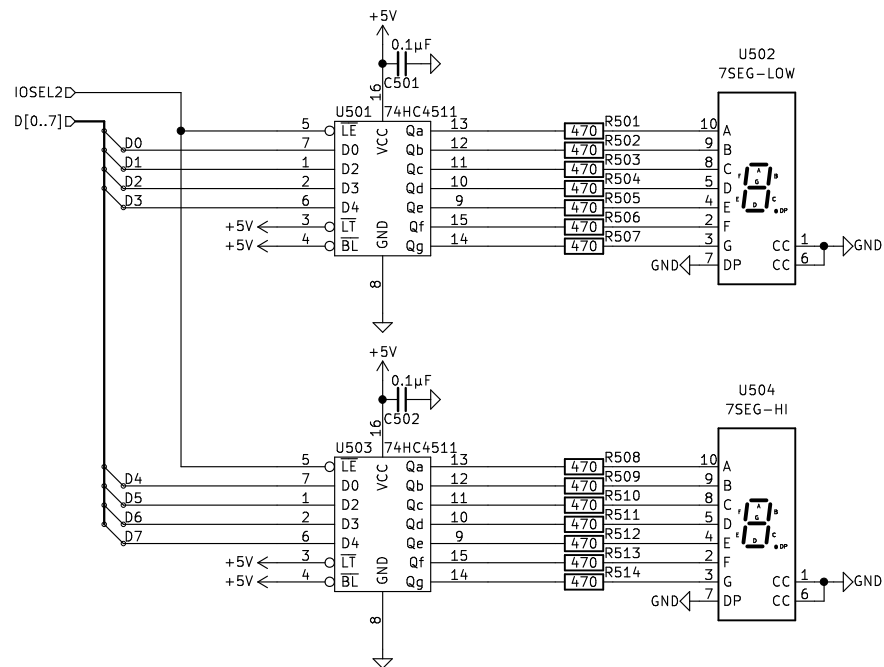
KiCad E.D.A. kicad (5.1.8)-1

Rev: v1.0

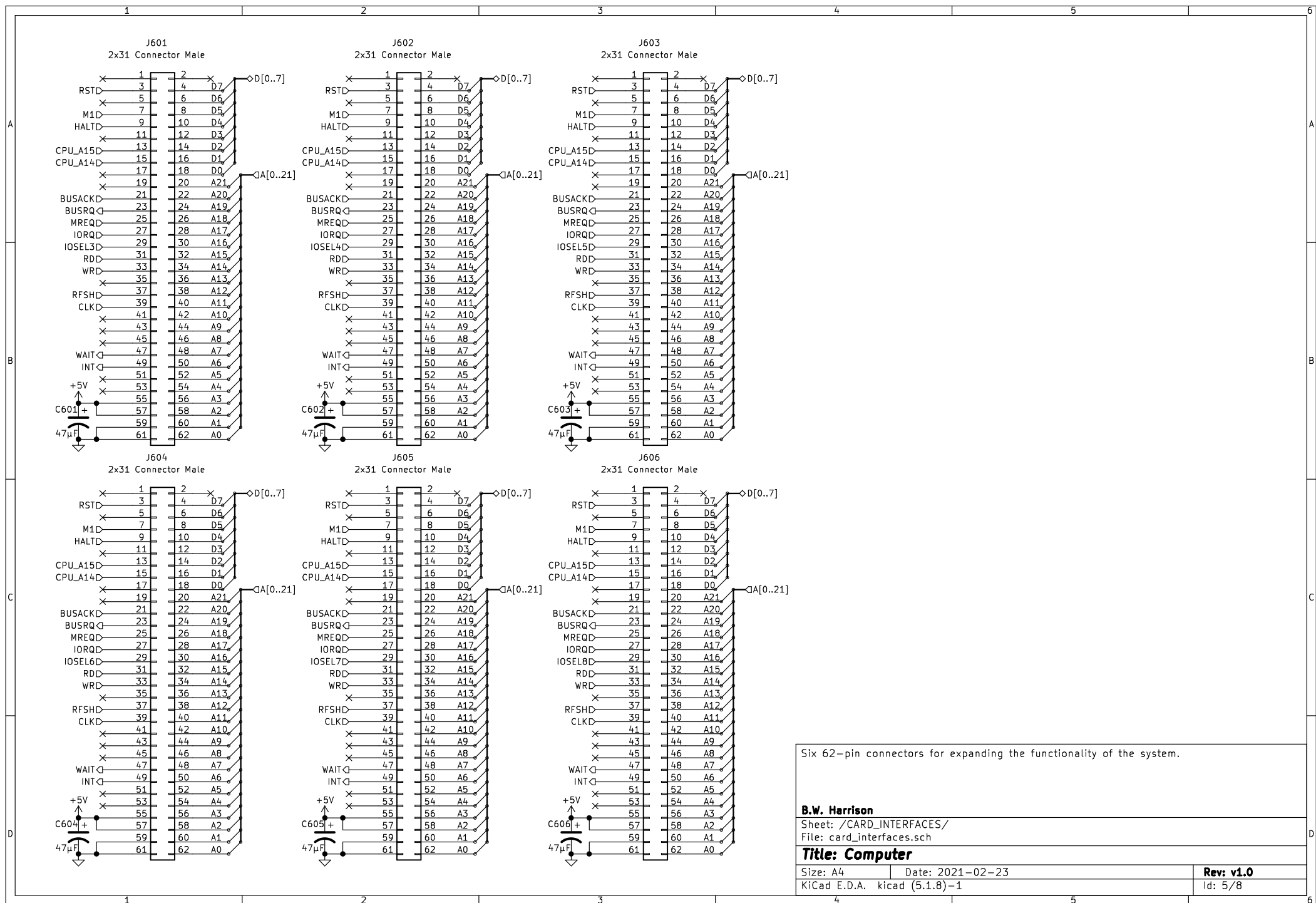
Id: 2/8



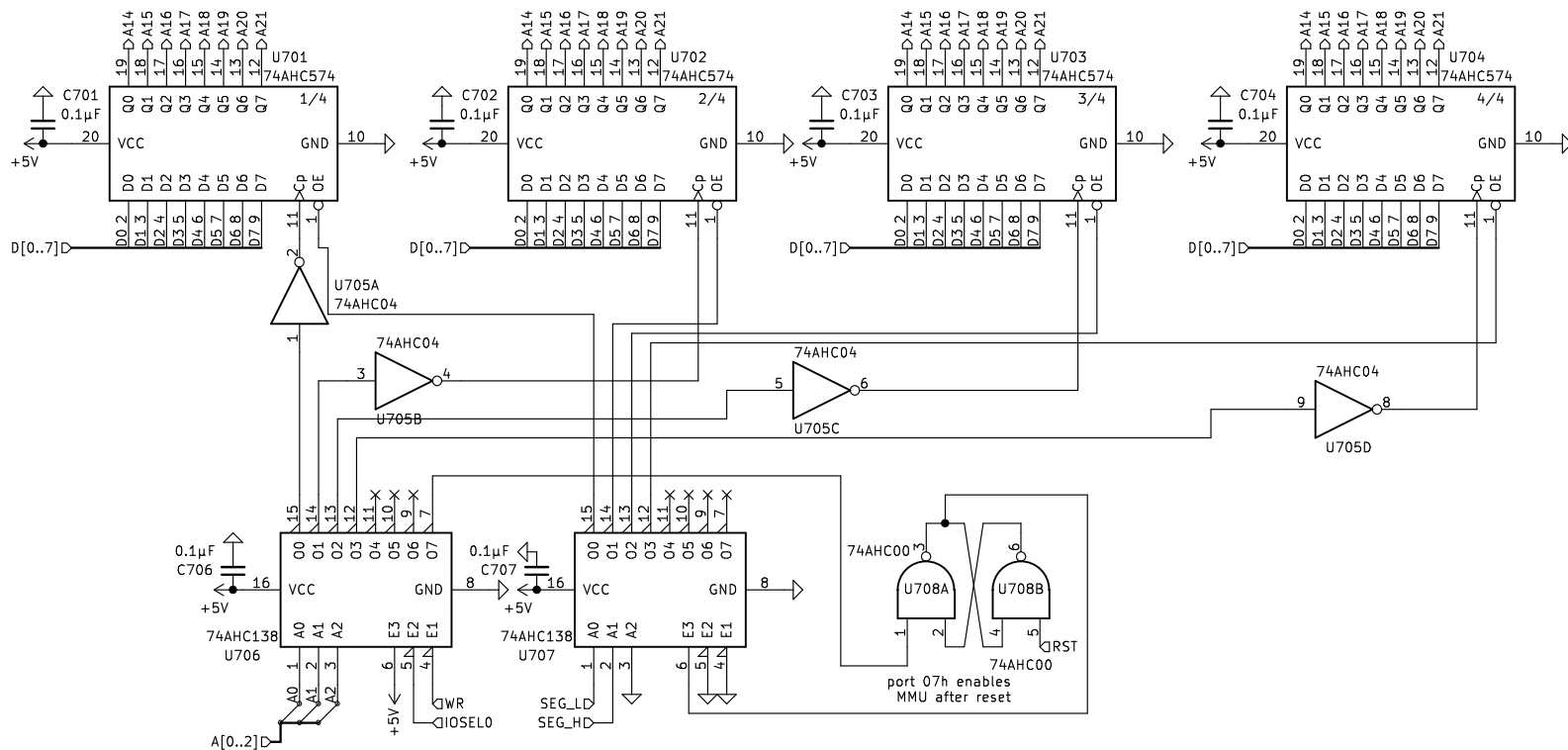
Decodes A4–A7 for IO device selection. This leaves 4 bits free per device, so each device can have 16 ports. Format: DDDPPPP D = device to select, P = port to select B.W. Harrison		
Sheet: /IO_DECODER/ File: io_decoder.sch		
Title: Computer		
Size: A4	Date: 2021-02-23	Rev: v1.0
KiCad E.D.A. kicad (5.1.8)–1		Id: 3/8



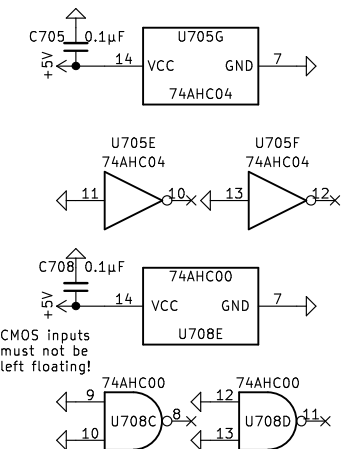
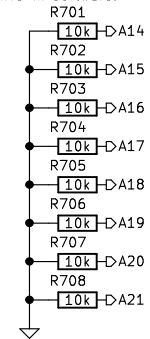
Two seven-segment displays with BCD inputs. D[0..3] is the low-order digit, D[4..7] is the high-order digit. To reduce the number of ICs, the WR line is not checked. Trying to read the IO port will result in unpredictable data being stored in the latches.		
B.W. Harrison		
Sheet: /SEVEN_SEGMENT/ File: seven_segment.sch		
Title: Computer		
Size: A4	Date: 2021-02-23	Rev: v1.0
KiCad E.D.A. kicad (5.1.8)-1		Id: 4/8



Six 62-pin connectors for expanding the functionality of the system.		
B.W. Harrison		
Sheet: /CARD_INTERFACES/		
File: card_interfaces.sch		
Title: Computer		
Size: A4	Date: 2021-02-23	Rev: v1.0
KiCad E.D.A. kicad (5.1.8)-1		Id: 5/8



We pull-down the high address lines so that when the MMU is high-Z (reset), the ROM is active. This lets us initialise the MMU in software.



The MMU splits the 64 KB address space into four 16 KB segments. This is achieved by routing A14 and A15 through a decoder which selects one of four registers. Each register can be loaded with an IO write to \$00-\$03. The registers output A14-A21 which extends the address space to 4 MB.

B.W. Harrison

Sheet: /MMU/

File: mmu.sch

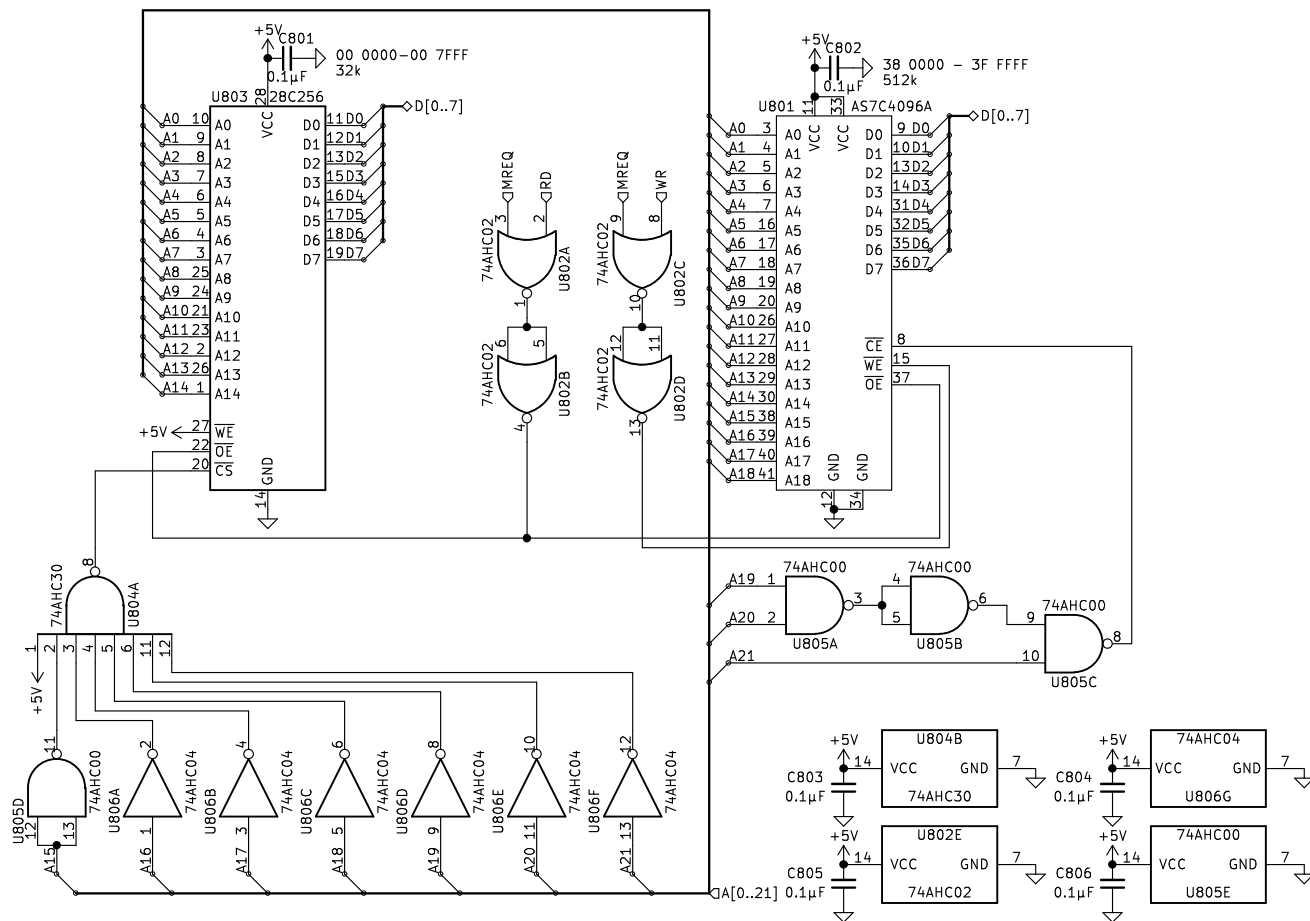
Title: Computer

Size: A4 Date: 2021-02-23

KiCad E.D.A. kicad (5.1.8)-1

Rev: v1.0

Id: 6/8



32 KB ROM pages \$00-\$01, 512 KB RAM pages \$E0-\$FF
 Because of the ROM's slow access time (150ns), the clock speed is initially set to 2.5MHz.
 The clock speed should only be changed to 20MHz when the ROM is no longer being accessed by the CPU.

B.W. Harrison

Sheet: /RAM_AND_ROM/

File: ram_and_rom.sch

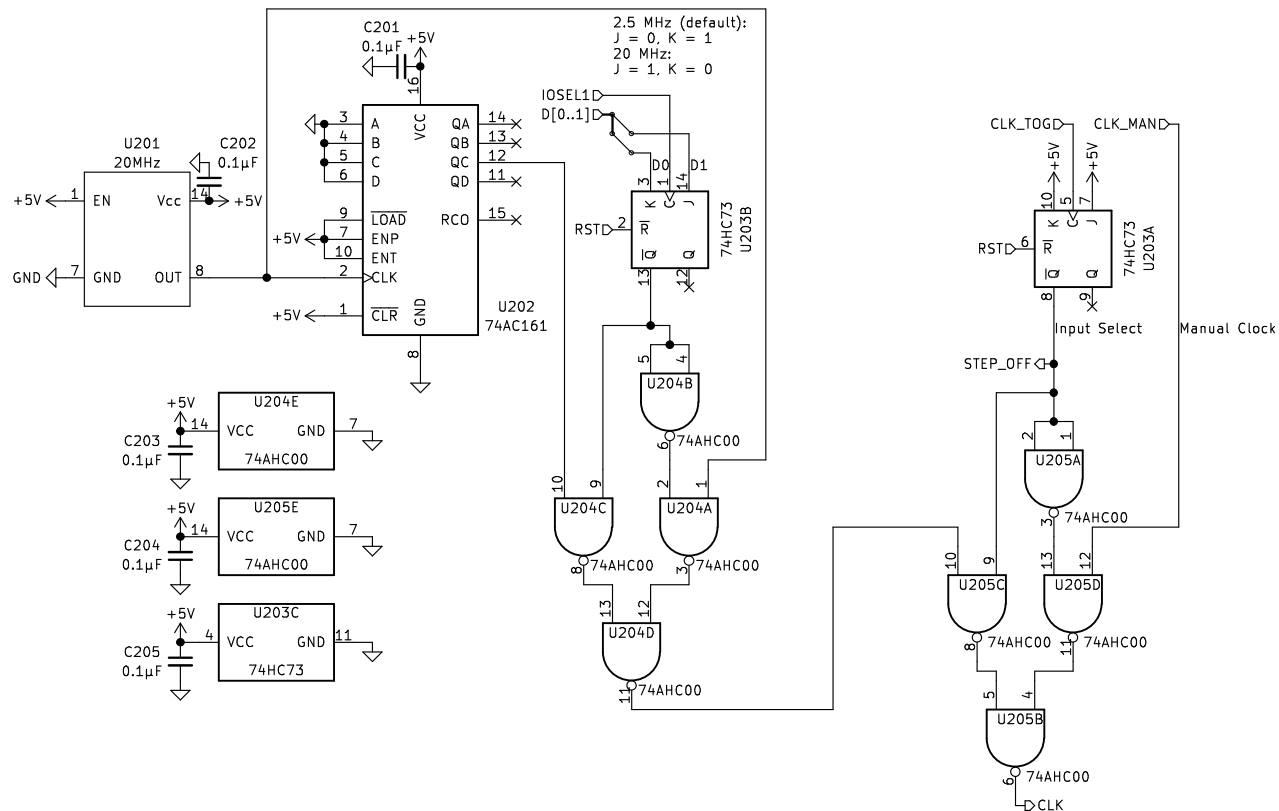
Title: Computer

Size: A4 Date: 2021-02-23

KiCad E.D.A. kicad (5.1.8)-1

Rev: v1.0

Id: 7/8



This circuit generates the appropriate system-wide clock signal depending on which mode is selected. There are 3 clock modes: 2.5MHz, 20MHz, and manual step. 2.5MHz is selected automatically on reset to allow the ROM to be read. 2.5MHz/20MHz can be toggled with an IO write. Manual step is toggled by the front panel.

B.W. Harrison

Sheet: /CLOCK/

File: clock.sch

Title: Computer

Size: A4 Date: 2021-02-23

KiCad E.D.A. kicad (5.1.8)-1

Rev: v1.0

Id: 8/8