S.D. Roll No.....

DIGITAL ELECTRONICS

3RD Exam/ECE/ETV/ECEII/Comp/CSc/EEE/0620/May'17

Duration: 3Hrs **M.Marks:75**

SECTION- A

Q1. Do as directed: **15x1=15**

a. The numbers of levels in a digital system are _____.
b. 1011 is a valid BCD number. (T/F)
c. Binary code of gray code 1011_{gray} is_____.
d. The expression A.B represents _____gate.
e. The clear signal is same as reset signal.(T/F)
f. The fastest ADC is _____.
g. The maximum count in a 4-bit ripple counter is _____.
h. To convert a JK flip-flop into T flip-flop, the inputs J=K=_____.
i. The condition S=R=1 is called as _____condition.
j. The complement of Boolean algebra AB. (BC+AC) is _____.
k. The radix of octal number is _____.
l. The parity is used for error detection and correction. (T/F)
m. _____logic family has maximum fan-out.
n. ASCII is a _____code.
o. A universal shift register can shift register left or right. (T/F)

SECTION- B

Q2: Attempt any six questions. **6x5=30**

i. Draw symbol and truth table of NOT, NAND and OR gate.
ii. Convert the following: **A)** 62_{16} X 36_{16} **B)** $341_8 = (?)_{10}$
iii. Define noise margin, propagation delay and fan-out.
iv. Compare all logic families and their characteristics.
v. Explain the operation of JK flip-flop using NAND gate.
vi. Explain dual slope A/D converter.
vii. Why universal shift registers are called universal? Explain.
viii. Draw and implement half adder.
ix. What are the applications of digital signal?

SECTION-C

Attempt any three questions **(3x10=30)**

Q3. Simplify the given K-map and draw logic circuit using gates. $F(A,B,C,D) = \sum(0,3,6,7,9,13,14,15)$

Q4. Explain the working of 3-bit asynchronous counter.

Q5. Draw and explain BCD to decimal decoder. Give its applications also.

Q6. Write Short note on any two:

(a) 4-bit adder
(b) D/A converter
(c) Buffer register
(d) Latch and flip-flop