

S. B. Roll. No.....

**DIGITAL ELECTRONICS**  
**3<sup>rd</sup> Exam/ECE/CSE/IT/0195/Jun'2021**  
**(For 2018 Batch onwards)**

**Duration: 1.15Hrs.**

**M.Marks:25**

**SECTION-A**

**Q1. Attempt any three questions.**

**3x5=15**

- i.  $(CDA)_{16} = ( )_2 = ( )_{10}$
- ii. Reduce the expression using karnaugh map  $\sum m(1,2,4,5,6,12,13,14)$
- iii. With the help of neat diagram explain the working of JK flip flop.
- iv. Explain briefly the following characteristics in relation to digital logic families
  - a) Propagation delay
  - b) Fan in
  - c) Fan out
  - d) Noise immunity.
- v. What is a full adder circuit? Explain with help of a diagram and truth table.
- vi. Explain the working of weighted register D/A converter.

**SECTION-B**

**Q2. Attempt any one question.**

**1x10=10**

- a. With the help of a diagram explain the working of successive approximation type A/D converter.
- b. With the help of a neat diagram explain the working of three bit asynchronous counter.
- c. Draw the diagram and explain the working of 3 to 8 line decoder circuit.
- d. Write short notes on the following.
  - i) IC 7495
  - ii) TTL logic family.