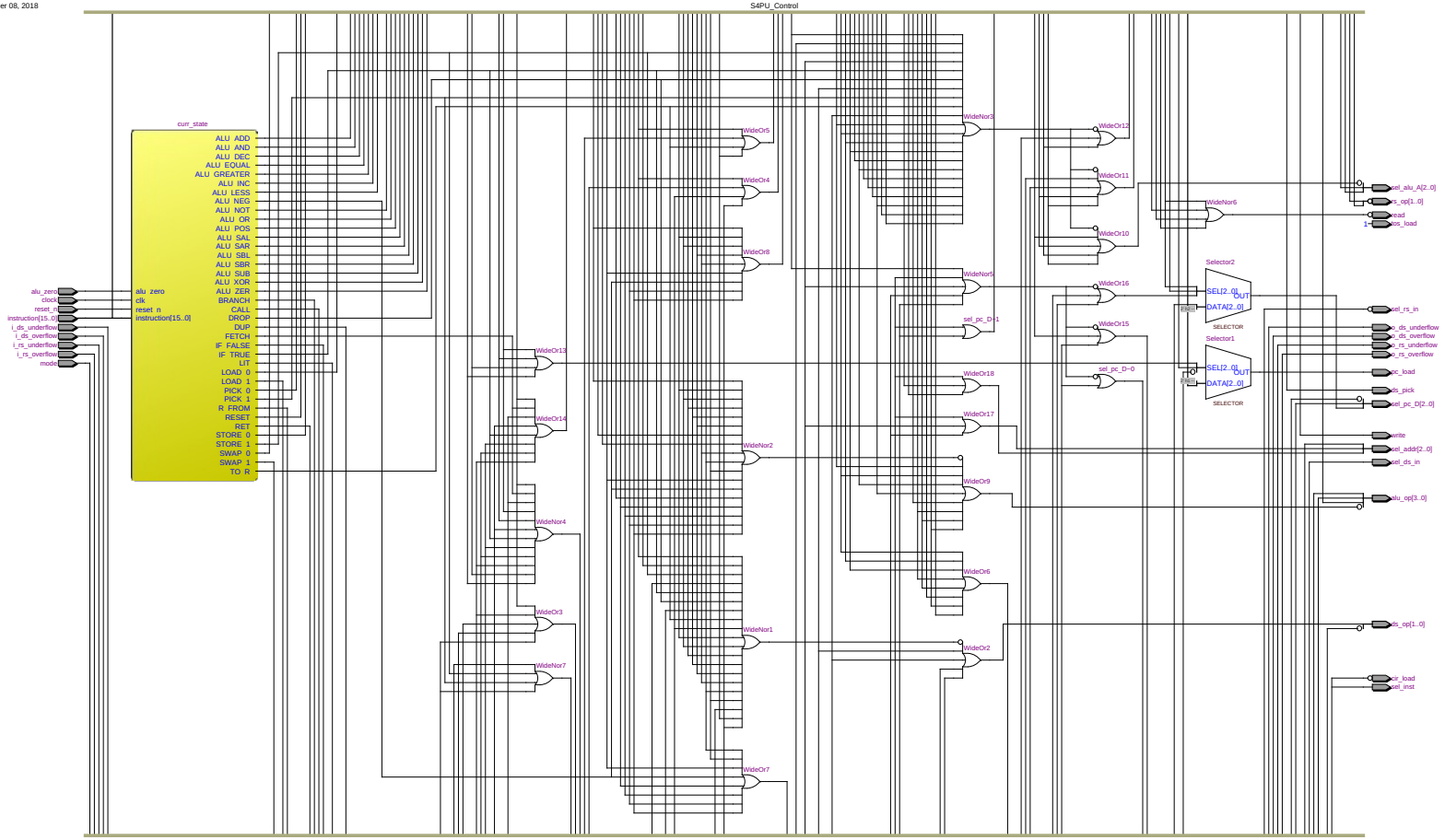
curr_state
ALU_ADD
ALU_AND
ALU_DEC
ALU_EQUAL
ALU_GREATER
ALU_INC
ALU_LESS
ALU_NEG
ALU_NOT
ALU_OR
ALU_POS
ALU_SAL
ALU_SAR
ALU_SBL
ALU_SBR
ALU_SUB
ALU_XOR
ALU_ZER
BRANCH
CALL
DROP
DUP
FETCH
IF_FALSE
IF_TRUE
LIT
LOAD_0
LOAD_1
PICK_0
PICK_1
R_FROM
RESET
RET
STORE_0
STORE_1
SWAP_0
SWAP_1
TO_R
alu_zero
clk
reset_n
instruction[15..0]
alu_zero
clock
reset_n
instruction[15..0]
i_ds_underflow
i_ds_overflow
i_rs_underflow
i_rs_overflow
mode
WideOr5
WideOr4
WideOr8
WideOr13
WideOr14
WideNor4
WideOr3
WideNor7
WideNor2
WideNor1
WideOr7
WideNor3
WideNor5
sel_pc_D=1
WideOr18
WideOr17
WideOr9
WideOr6
WideOr2
WideOr12
WideOr11
WideOr10
WideOr16
WideOr15
sel_pc_D=0
WideNor6
Selector2
SEL[2..0]
DATA[2..0]
OUT
SELECTOR
Selector1
SEL[2..0]
DATA[2..0]
OUT
SELECTOR
sel_alu_A[2..0]
rs_op[1..0]
read
1
ds_load
sel_rs_in
o_ds_underflow
o_ds_overflow
o_rs_underflow
o_rs_overflow
pc_load
ds_pick
sel_pc_D[2..0]
write
sel_addr[2..0]
sel_ds_in
alu_op[3..0]
ds_op[1..0]
ir_load
sel_inst