Baishen Huang

baishen.huang@gmail.com | baishen.github.io| F-1 Visa on STEM OPT Ext. (eligible to work in the U.S.)

Objective

Seeking a challenging software engineer position, where I can apply my knowledge in software and computer engineering to contribute to the company

Language: Proficient in C/C++ 11 and Python

Work Experience

Modem SW Performance and Architecture Engineer at Qualcomm July 2017 to Present

- Lead performance profiling, optimization and latency reduction on 5G modem chipset
  - Deliver up to 20% CPU load reduction on silicon
  - Identify performance bottlenecks and timeline violations to directors and provide optimized prototypes
- Drive task level performance profile tooling innovation, from initial proposal to commercialization
  - Work with kernel, automation and tech teams to produce an end-to-end profiling workflow

Education

Georgia Institute of Technology Atlanta, GA

M.S. in Computer Engineering August 2016 to May 2017

B.S. in Computer Engineering (Highest Honor, Overall GPA: 3.91/4.0) Fall 2013 to May 2016

Academic Research

Distributed FPGA Accelerator for Machine Learning with Prof. Hadi Esmaeilzedeh Oct 2016 to July 2017

- Implement a multi-threaded template dataflow architecture on FPGA
- Implement the multi-stage pipeline and interconnect as microarchitectural components
- Result in an efficient, scalable, and programmable ML accelerator on FPGA

Memory Compression for Bandwidth Reduction with Prof. Moin Qureshi Jan 2017 to May 2017

- Design and implement a memory compression scheme for bandwidth reduction
- Design for minimal microarchitectural changes without additional OS support

Academic Projects

Computer Architecture Simulation (C++) Spring 2015 to Present

- Implement a runtime utility-based cache partitioning mechanism to partition shared caches
- Implement various key components in an out of order superscalar pipeline simulator and a multi-level cache simulator with support for multi cores

Operating System (C++) Summer 2014 to Present

- MapReduce: implement a simplified version of MapReduce infrastructure with gRPC and protobuf
- Virtualization: implement a resource manager for vCPU and memory to dynamically balance resources for guest OS
- DFS: design and implement a dynamic replica management system for HDFS
- Spark: build a movie recommendation system with SVD and collaborative filtering on Spark MLlib

FPGA Programming (Verilog) Spring 2017

- Implement a real-time image edge detection algorithm on FPGA

Assembly Programming (MIPS) Fall 2014

- Implement robot localization and navigation with over 1000 lines of MIPS assembly code

Internship

Enterprise Middleware Intern at UPS Information Service Global Integration Center Summer 2015

- Develop JMS message reprocess functionality and enhance message searching and selection functionality
- Use Java, SQL, AJAX, and HTML

DevOps Intern at Liaison Technologies Summer 2016

- Create end-to-end automation workflow for Cisco VPN setup, statistics retrieval, maintenance and IP planner
- Use Python and Rundeck