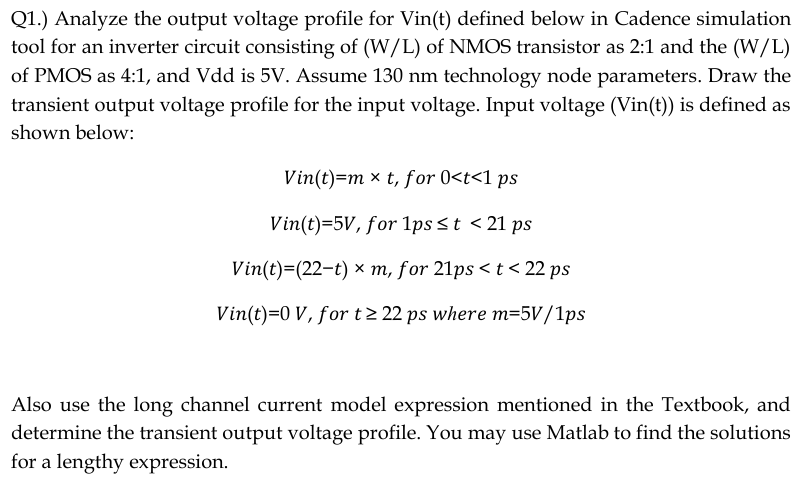
DCMOS ASSIGNMENT-2

Name: Vaibhav Bajoriya

Roll No: IMT2022574

Email-Id: [Vaibhav.Bajoriya@iiitb.ac.in](mailto:Vaibhav.Bajoriya@iiitb.ac.in)

Q1.

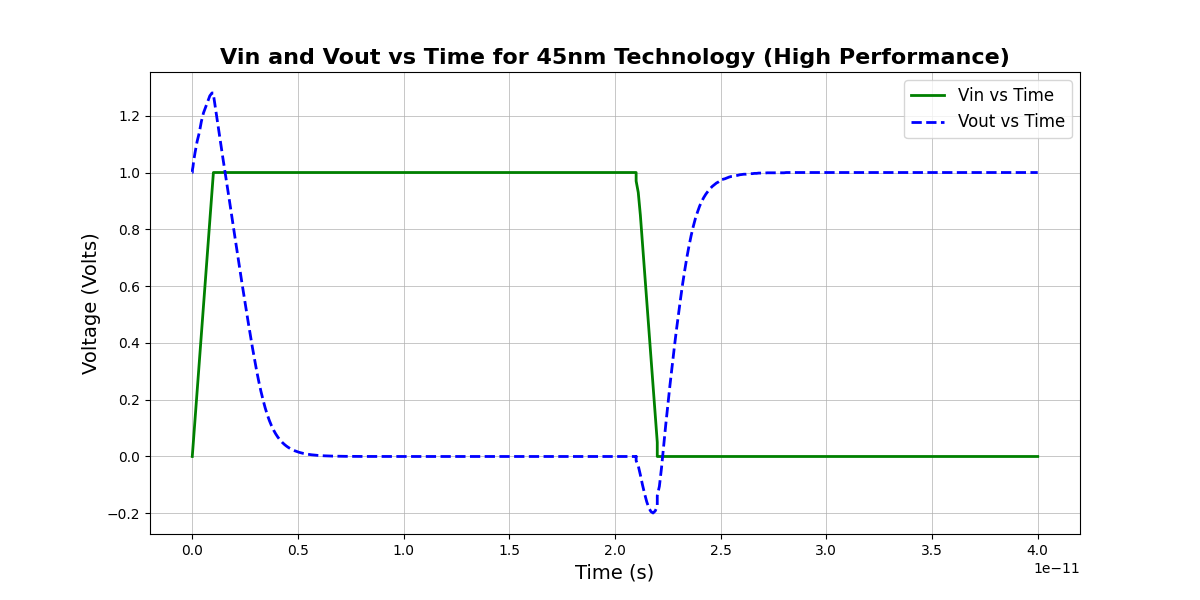


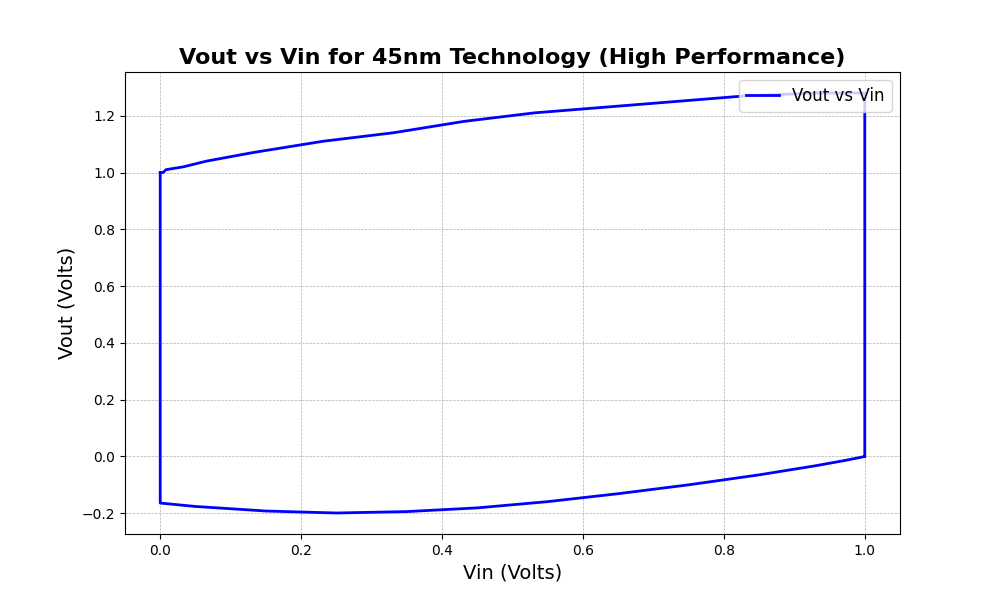
=>

**Schematics:**

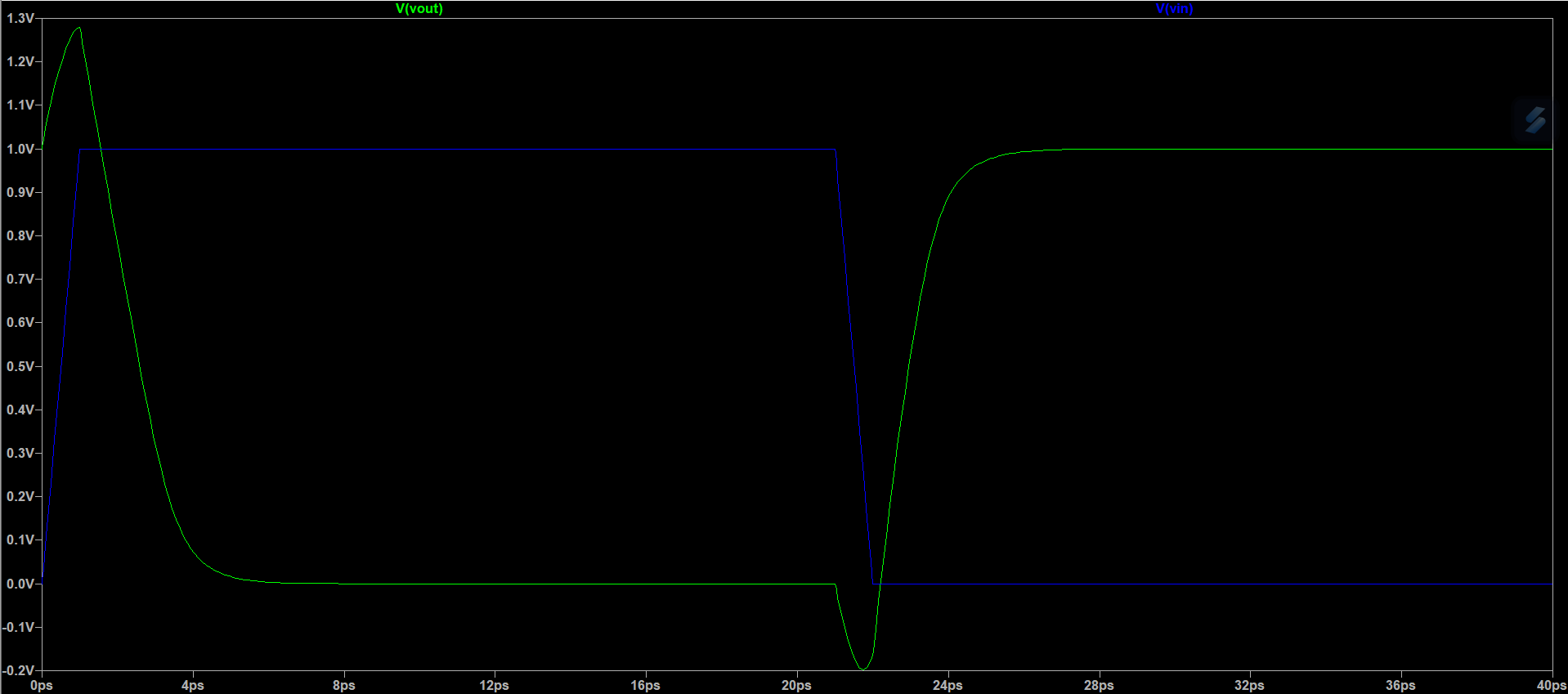


Graphs:

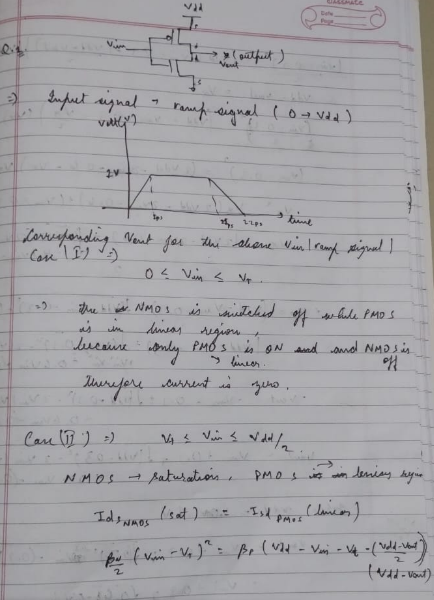


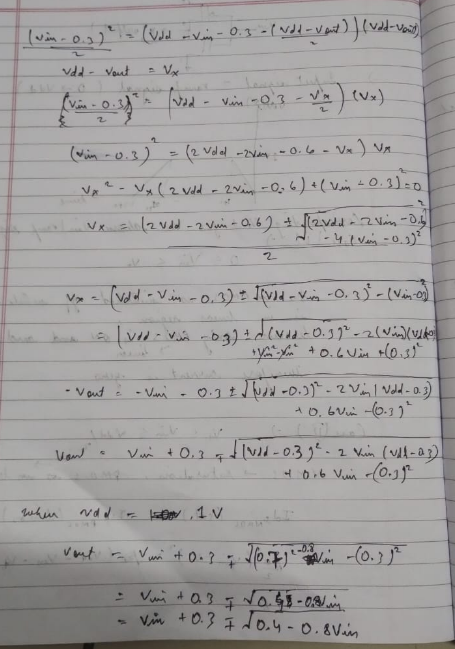


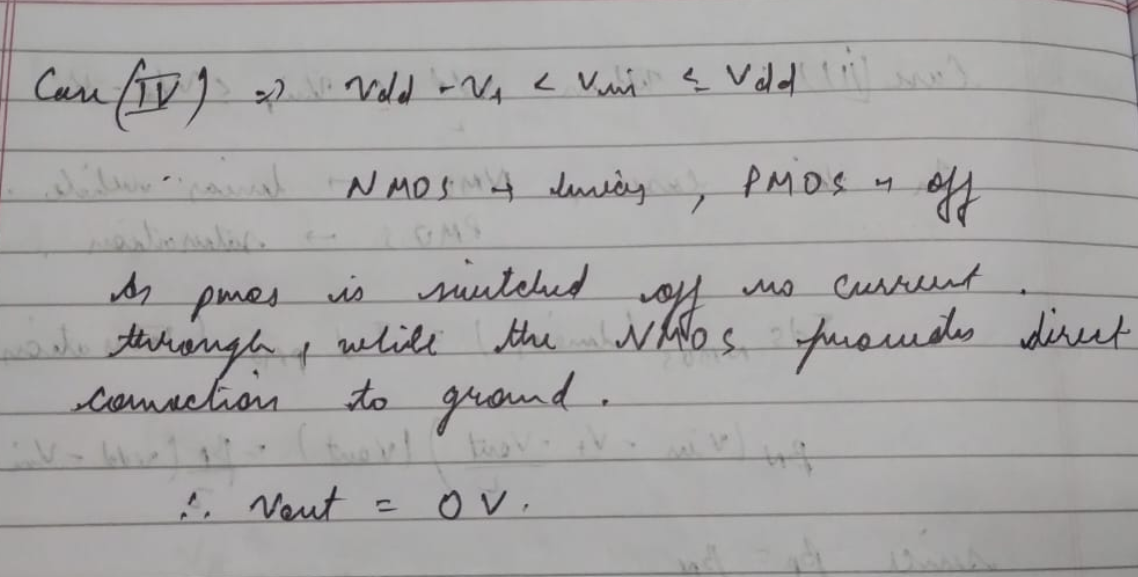
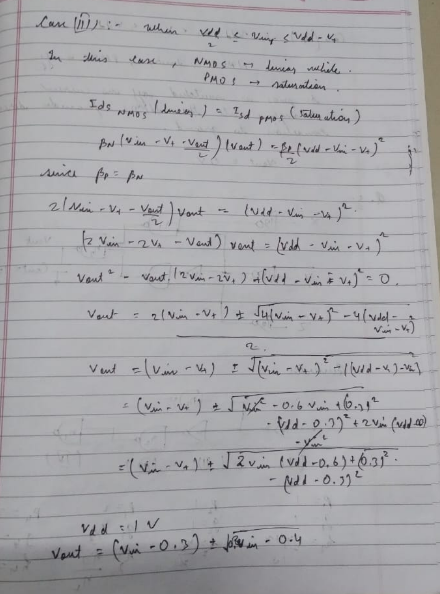
(LTspice)



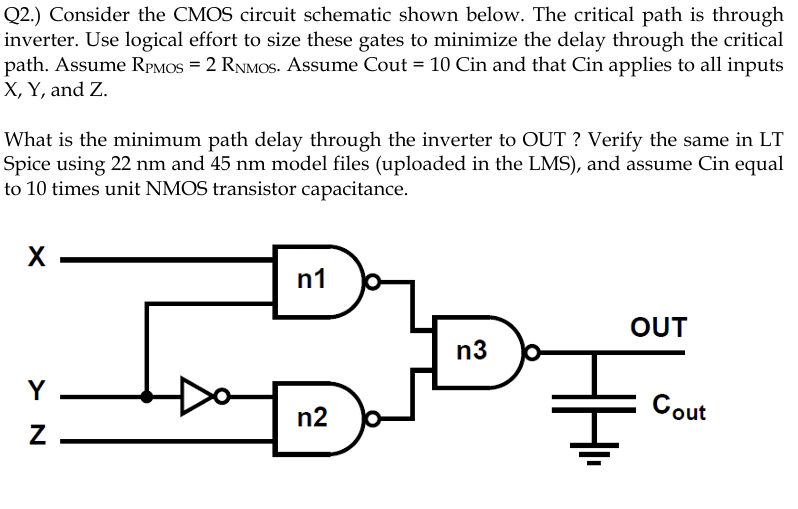
Theory:





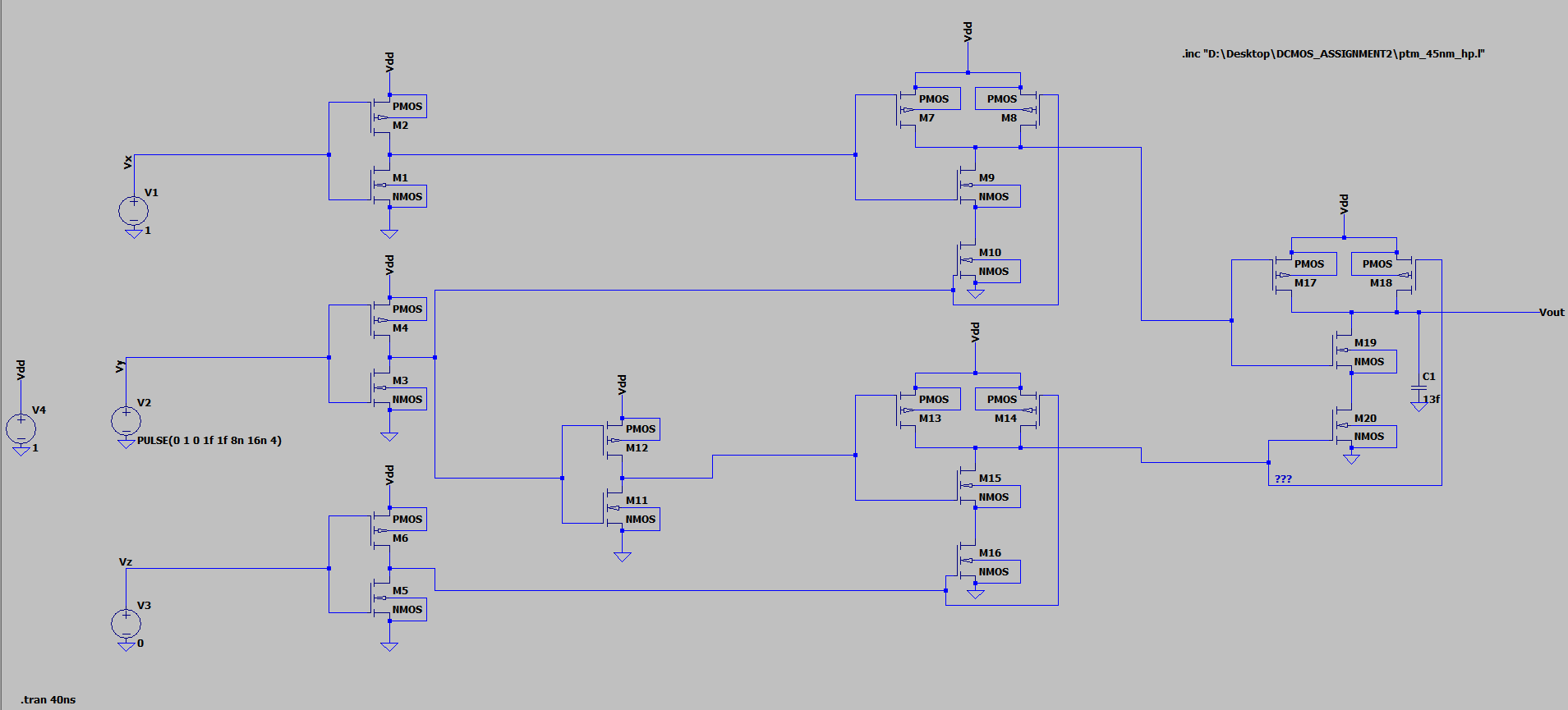


Q2.



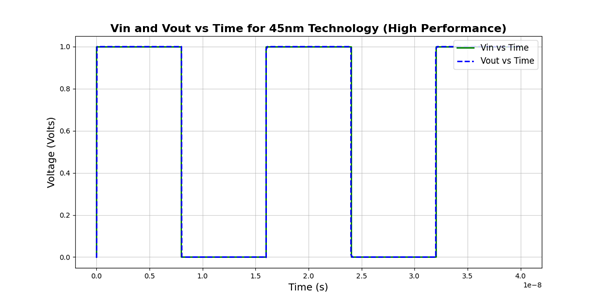
=>

**Schematics:**



Graphs:

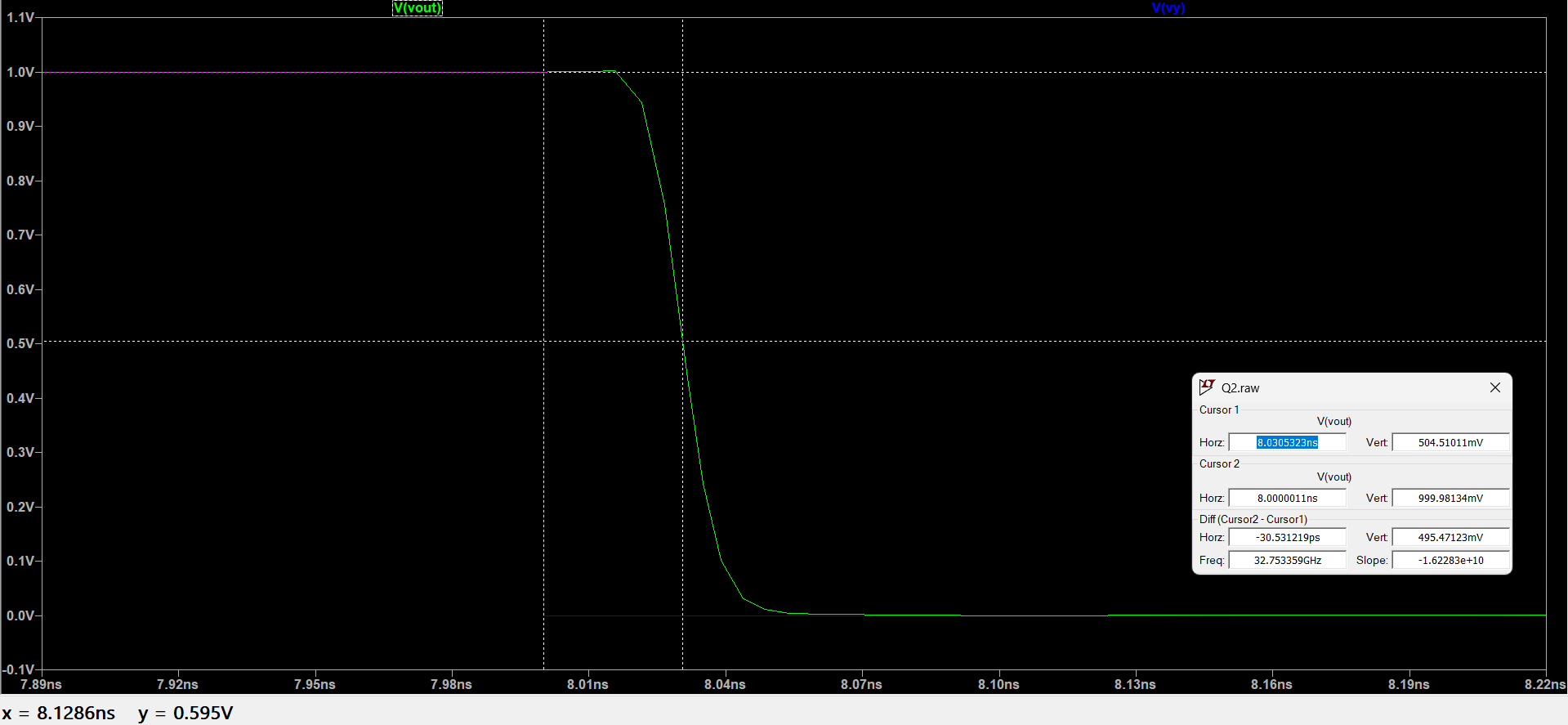
(Taking y as the input voltage,ie. Vin = Vy(PULSE input) , Vx = 1 and Vz = 0)



(Zoomed out)

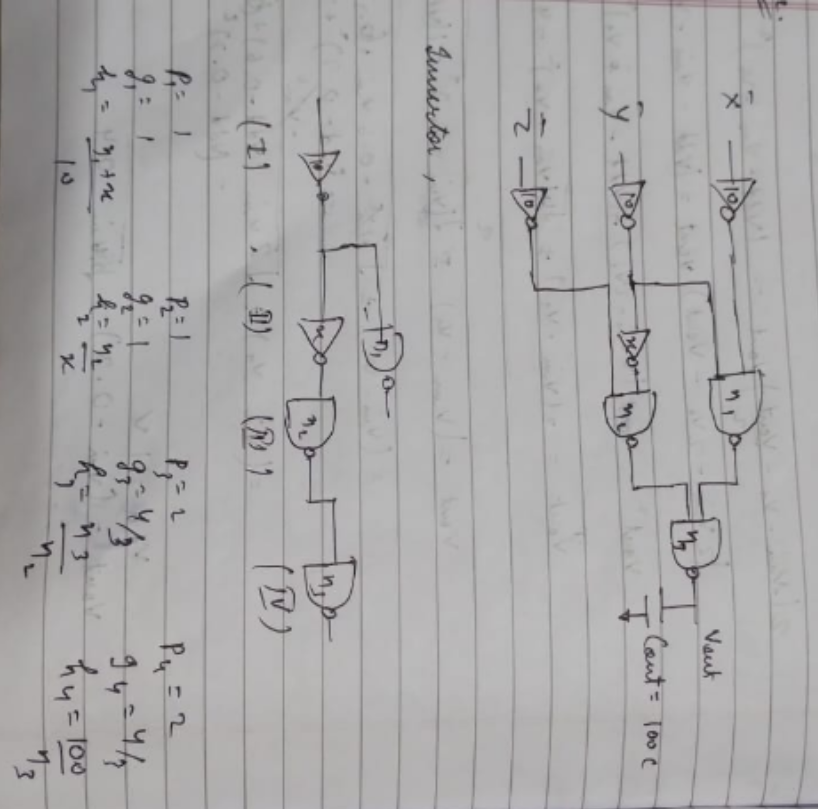


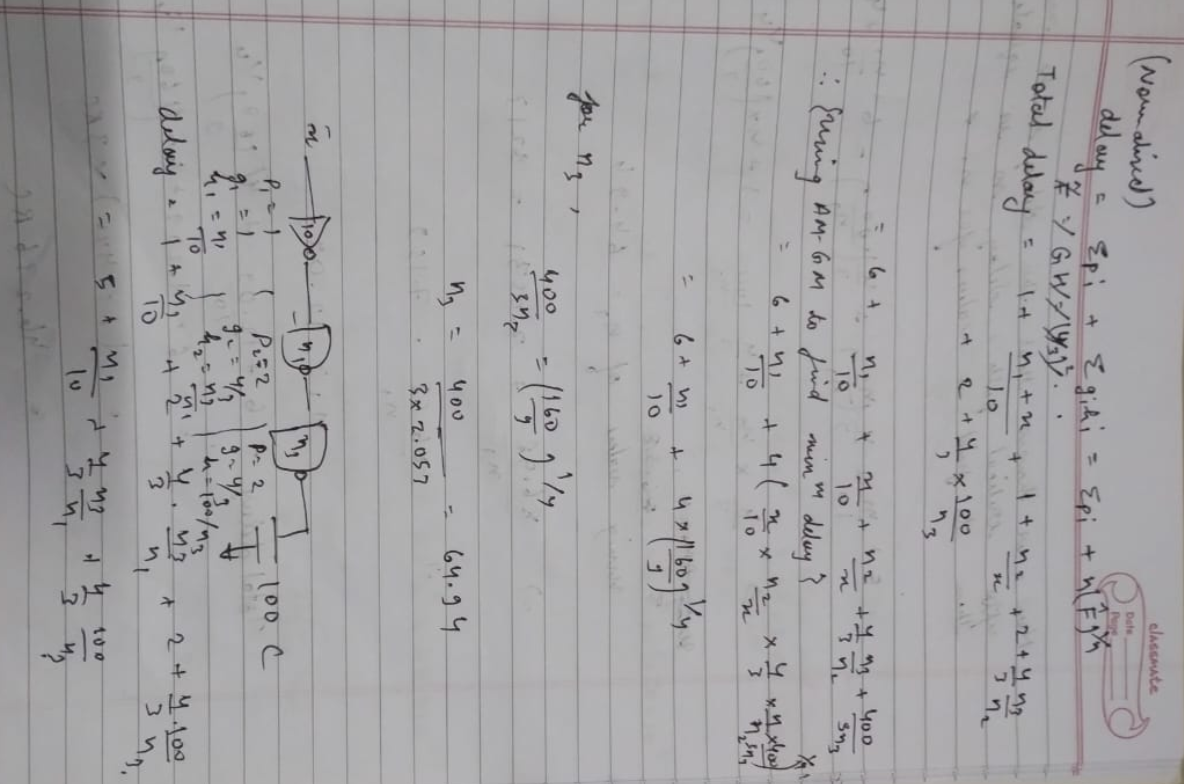
(LTspice for better propagation delay)



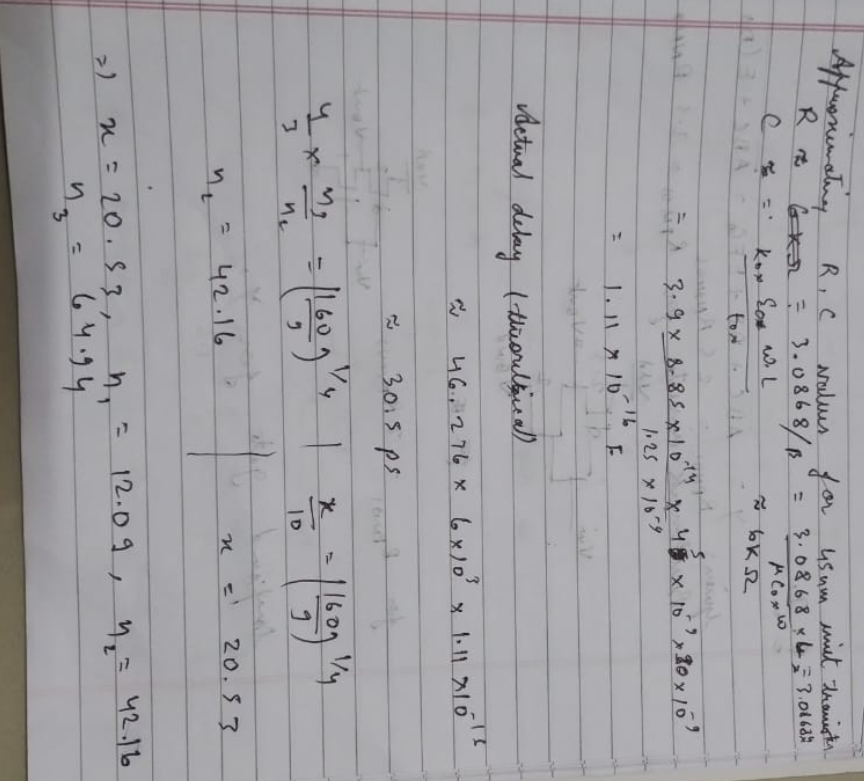
Delay from above LTspice stimulation = (8.0305-8.0000)ps = 30.5ps(approx.)

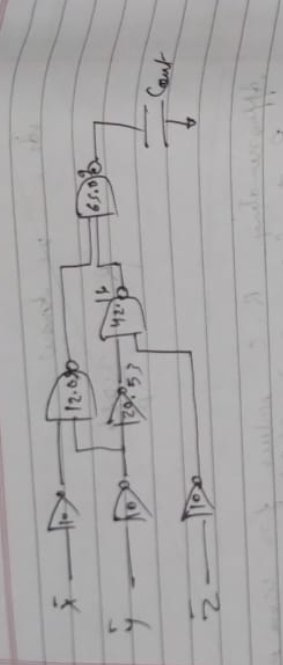
Theory:



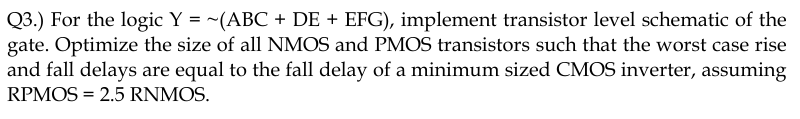








Q3.



=>

