DCMOS ASSIGNMENT-2

Name: Vaibhav Bajoriya

Roll No: IMT2022574

Email-Id: Vaibhav.Bajoriya@iiitb.ac.in

Q1.

Q1.) Analyze the output voltage profile for Vin(t) defined below in Cadence simulation tool for an inverter circuit consisting of (W/L) of NMOS transistor as 2:1 and the (W/L) of PMOS as 4:1, and Vdd is 5V. Assume 130 nm technology node parameters. Draw the transient output voltage profile for the input voltage. Input voltage (Vin(t)) is defined as shown below:

$$Vin(t)=m \times t, \; for \; 0<t<1 \; ps$$

$$Vin(t)=5V, \; for \; 1ps \leq t \; < 21 \; ps$$

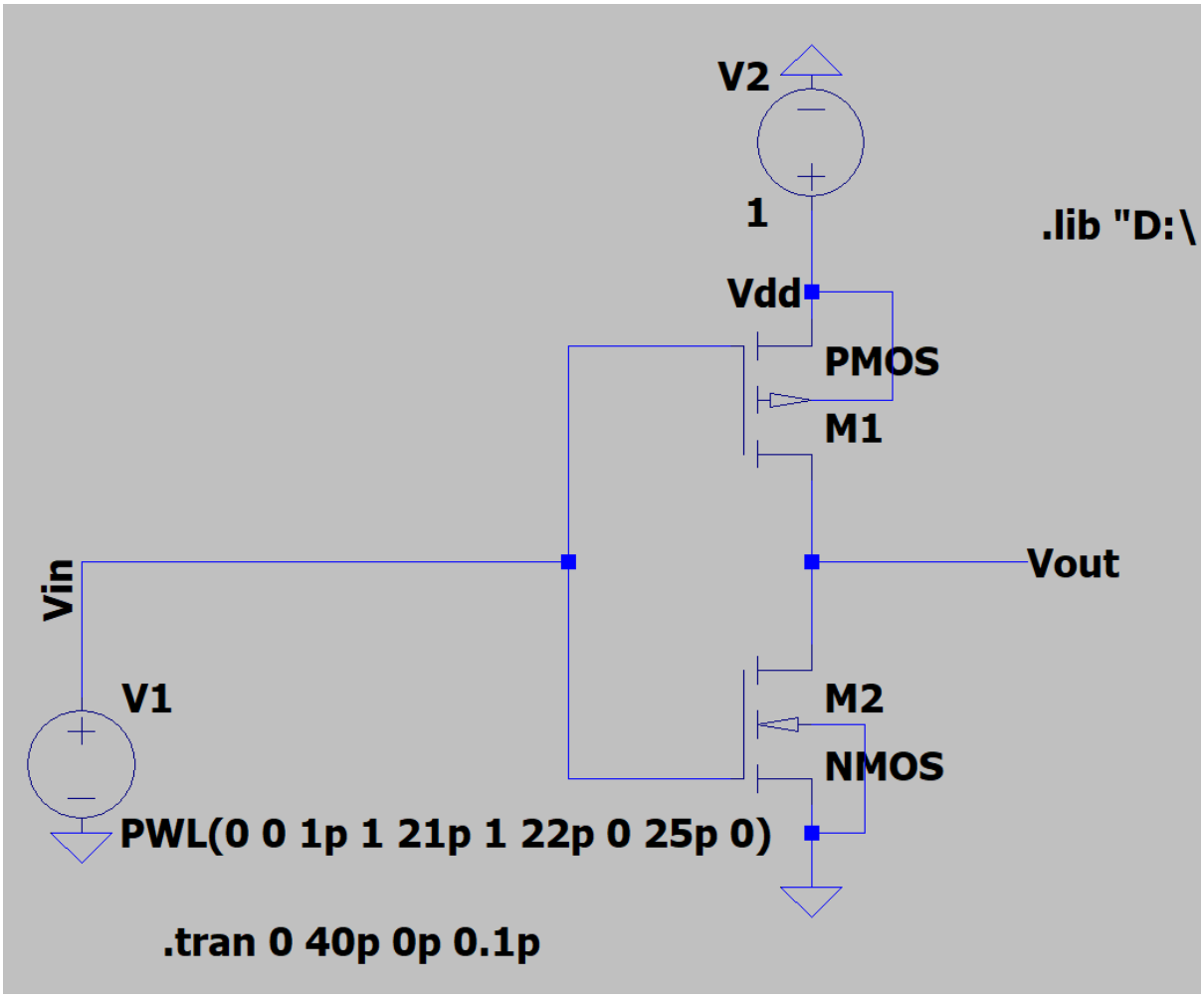
$$Vin(t)=(22-t) \times m, \; for \; 21ps < t < 22 \; ps$$

$$Vin(t)=0 \; V, \; for \; t \geq 22 \; ps \; where \; m=5V/1ps$$

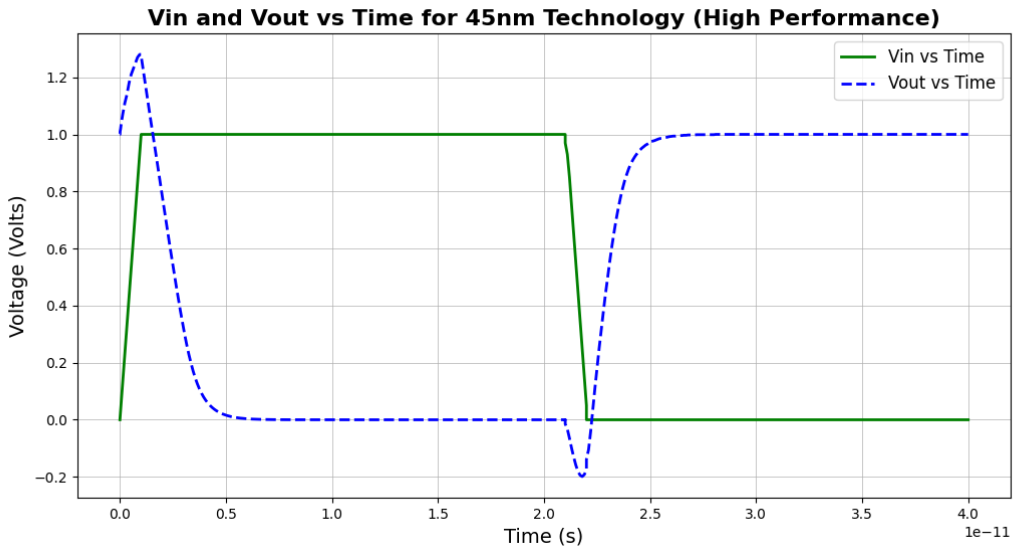
Also use the long channel current model expression mentioned in the Textbook, and determine the transient output voltage profile. You may use Matlab to find the solutions for a lengthy expression.

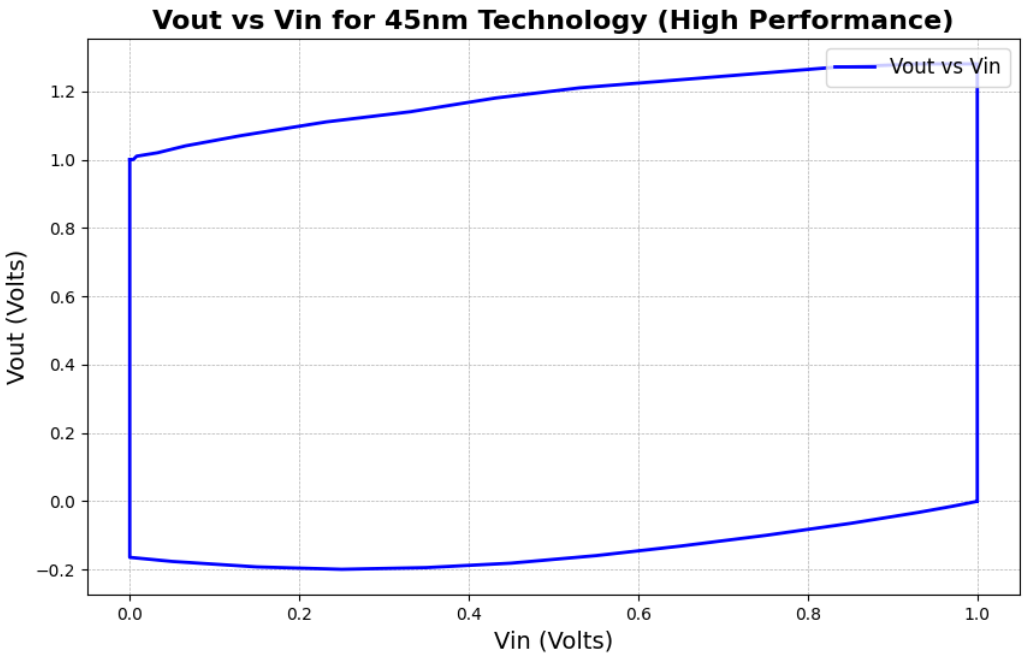
=>

Schematics:

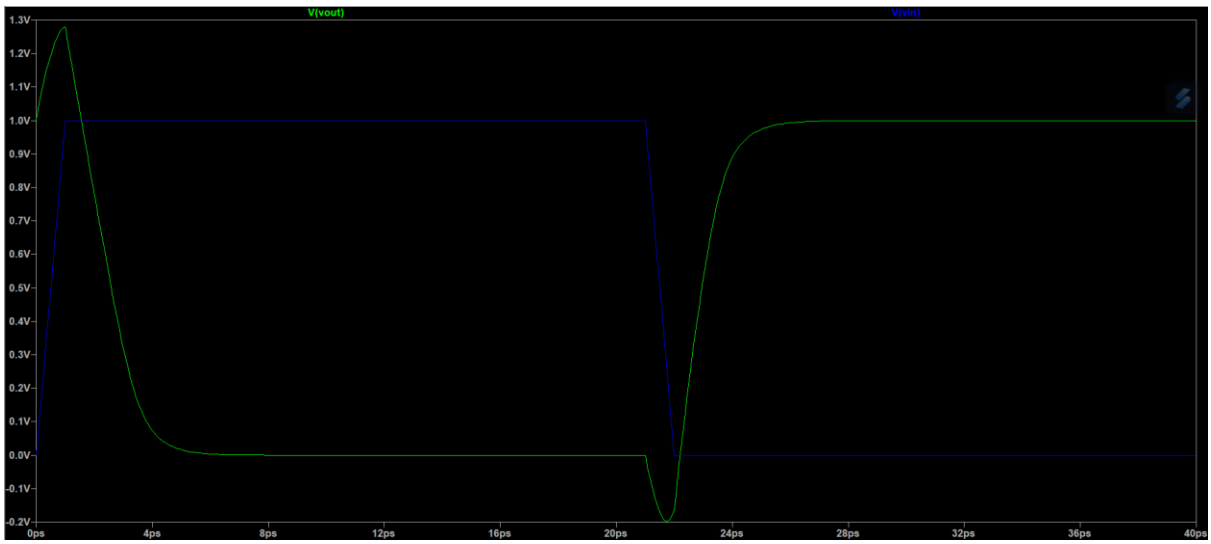

V2
1
.lib "D:\
Vdd
PMOS
M1
Vout
Vin
V1
M2
NMOS
PWL(0 0 1p 1 21p 1 22p 0 25p 0)
.tran 0 40p 0p 0.1p

Graphs:


Vin and Vout vs Time for 45nm Technology (High Performance)
Vin vs Time
Vout vs Time
Voltage (Volts)
Time (s)
1e−11
1.2
1.0
0.8
0.6
0.4
0.2
0.0
−0.2
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0

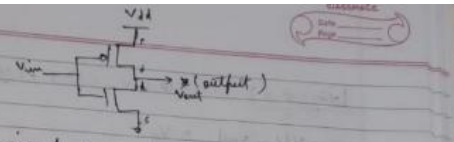


(LTspice)

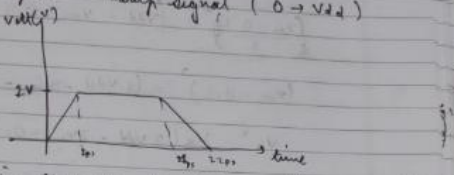


Theory:

Q.3.



=) Input signal → ramp signal (0 → Vdd)



Corresponding Vout for the above Vin (ramp signal)

Case (I) =)

$0 \le V_{in} \le V_t$.

=) the NMOS is switched off while PMOS is in linear region,
because only PMOS is ON and and NMOS is off
→ linear.

Therefore current is zero.

Case (II) =) $V_t \le V_{in} \le V_{dd}/2$.

NMOS → saturation, PMOS is in linear region

$$Id_{s_{NMOS}}(sat) = Id_{s_{PMOS}}(linear)$$

$$\frac{\beta_n}{2}(V_{in} - V_t)^2 = \beta_p\left(V_{dd} - V_{in} - V_t - \left(\frac{V_{dd} - V_{out}}{2}\right)\right)(V_{dd} - V_{out})$$

$$\frac{(V_{in} - 0.3)^2}{2} = \left(V_{dd} - V_{in} - 0.3 - \left(\frac{V_{dd} - V_{out}}{2}\right)\right)(V_{dd} - V_{out})$$

$V_{dd} - V_{out} = V_x$

$$\left(\frac{V_{in} - 0.3}{2}\right)^2 = \left(V_{dd} - V_{in} - 0.3 - \frac{V_x}{2}\right)(V_x)$$

$$(V_{in} - 0.3)^2 = (2V_{dd} - 2V_{in} - 0.6 - V_x)V_x$$

$$V_x^2 - V_x(2V_{dd} - 2V_{in} - 0.6) + (V_{in} - 0.3)^2 = 0$$

$$V_x = \frac{(2V_{dd} - 2V_{in} - 0.6) \pm \sqrt{(2V_{dd} - 2V_{in} - 0.6)^2 - 4(V_{in} - 0.3)^2}}{2}$$

$$V_x = (V_{dd} - V_{in} - 0.3) \pm \sqrt{(V_{dd} - V_{in} - 0.3)^2 - (V_{in} - 0.3)^2}$$

$$= (V_{dd} - V_{in} - 0.3) \pm \sqrt{(V_{dd} - 0.3)^2 - 2(V_{in})(V_{dd} - 0.3) + V_{in}^2 - V_{in}^2 + 0.6V_{in} + (0.3)^2}$$

$$-V_{out} = -V_{in} - 0.3 \pm \sqrt{(V_{dd} - 0.3)^2 - 2V_{in}(V_{dd} - 0.3) + 0.6V_{in} - (0.3)^2}$$

$$V_{out} = V_{in} + 0.3 \mp \sqrt{(V_{dd} - 0.3)^2 - 2V_{in}(V_{dd} - 0.3) + 0.6V_{in} - (0.3)^2}$$

when $V_{dd} = 1V$

$$V_{out} = V_{in} + 0.3 \mp \sqrt{(0.7)^2 - 0.8V_{in} - (0.3)^2}$$

$$= V_{in} + 0.3 \mp \sqrt{0.58 - 0.8V_{in}}$$

$$= V_{in} + 0.3 \mp \sqrt{0.4 - 0.8V_{in}}$$

Case (III) :- when $\frac{V_{dd}}{2} \leq V_{in} \leq V_{dd} - V_t$

In this case, NMOS → linear region.
PMOS → saturation.

$I_{ds\,NMOS}$ (linear) = $I_{sd\,PMOS}$ (saturation)

$$\beta_N \left(V_{in} - V_t - \frac{V_{out}}{2}\right) V_{out} = \frac{\beta_P}{2} (V_{dd} - V_{in} - V_t)^2$$

since $\beta_P = \beta_N$

$$2\left(V_{in} - V_t - \frac{V_{out}}{2}\right) V_{out} = (V_{dd} - V_{in} - V_t)^2$$

$$(2V_{in} - 2V_t - V_{out})\, V_{out} = (V_{dd} - V_{in} - V_t)^2$$

$$V_{out}^2 - V_{out}(2V_{in} - 2V_t) + (V_{dd} - V_{in} + V_t)^2 = 0$$

$$V_{out} = \frac{2(V_{in} - V_t) \pm \sqrt{4(V_{in} - V_t)^2 - 4(V_{dd} - V_{in} - V_t)^2}}{2}$$

$$V_{out} = (V_{in} - V_t) \mp \sqrt{(V_{in} - V_t)^2 - (V_{dd} - V_{in} - V_t)^2}$$

$$= (V_{in} - V_t) \pm \sqrt{V_{in}^2 - 0.6 V_{in} + 0.3^2 - (V_{dd} - 0.3)^2 + 2V_{in}(V_{dd} - 0.3) - V_{in}^2}$$

$$= (V_{in} - V_t) \pm \sqrt{2V_{in}(V_{dd} - 0.6) + 0.3^2 - (V_{dd} - 0.3)^2}$$

$V_{dd} = 1\ V$

$V_{out} = (V_{in} - 0.3) \pm \sqrt{2V_{in} - 0.4}$

Case (IV) $\Rightarrow V_{dd} - V_t < V_{in} \leq V_{dd}$

NMOS → linear, PMOS → off

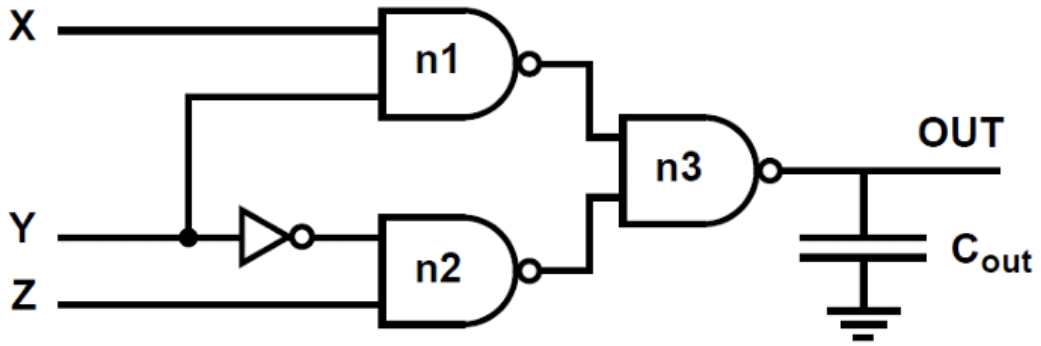
As pmos is switched off no current strength, while the NMOS provides direct connection to ground.

$\therefore V_{out} = 0\ V.$

Q2.

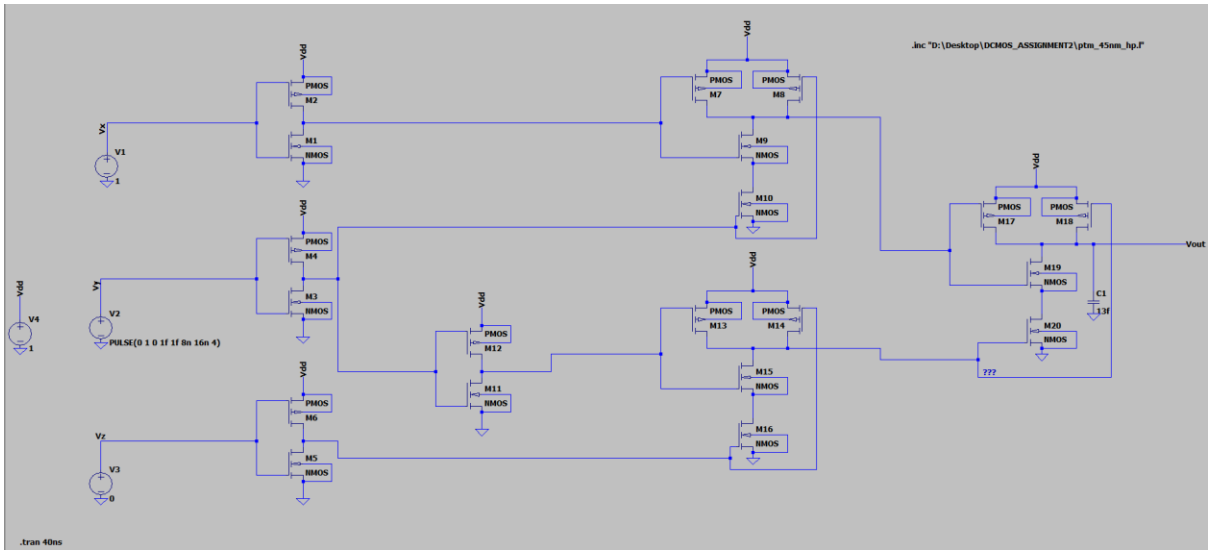
Q2.) Consider the CMOS circuit schematic shown below. The critical path is through inverter. Use logical effort to size these gates to minimize the delay through the critical path. Assume $R_{PMOS} = 2\ R_{NMOS}$. Assume Cout = 10 Cin and that Cin applies to all inputs X, Y, and Z.

What is the minimum path delay through the inverter to OUT ? Verify the same in LT Spice using 22 nm and 45 nm model files (uploaded in the LMS), and assume Cin equal to 10 times unit NMOS transistor capacitance.



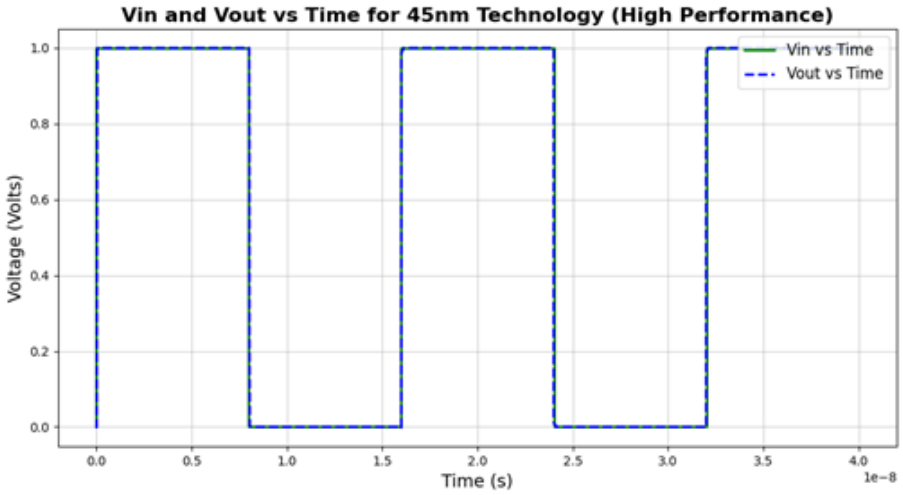
=>

Schematics:

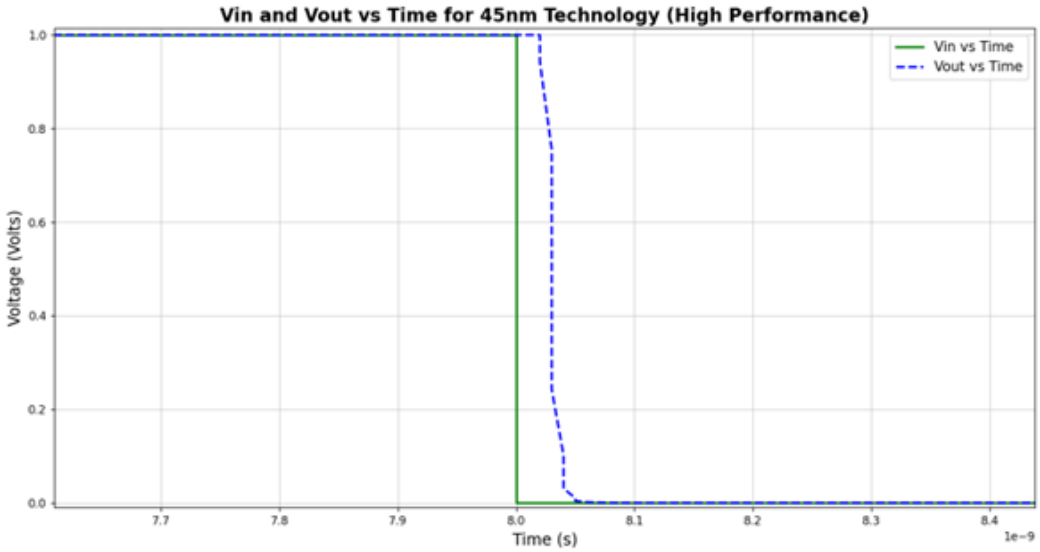


Graphs:

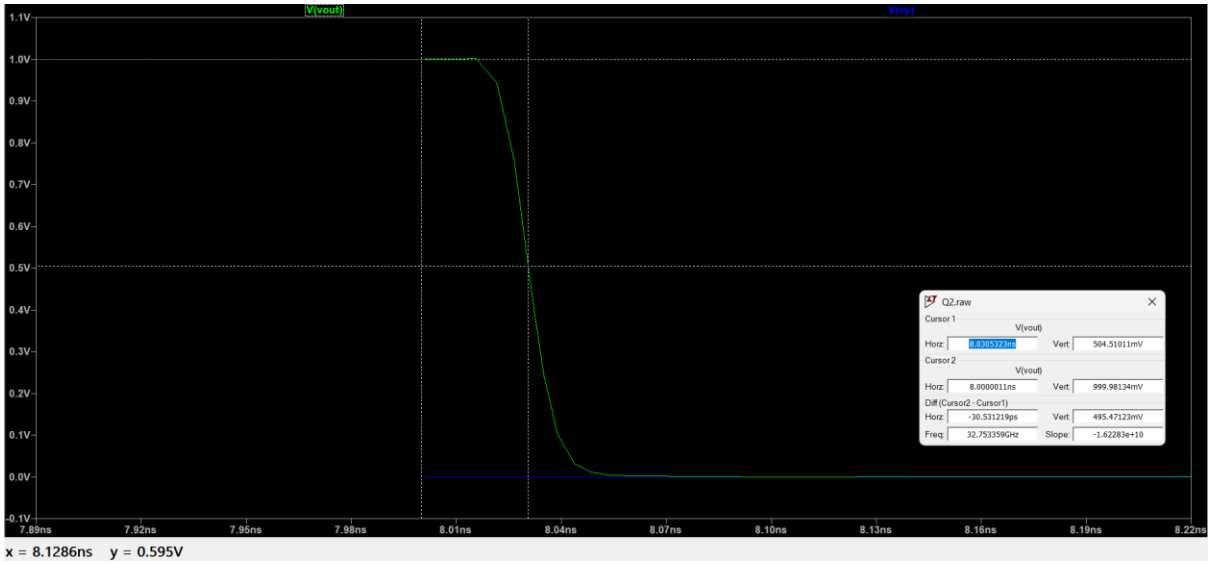
(Taking y as the input voltage,ie. Vin = Vy(PULSE input) , Vx = 1 and Vz = 0)



(Zoomed out)

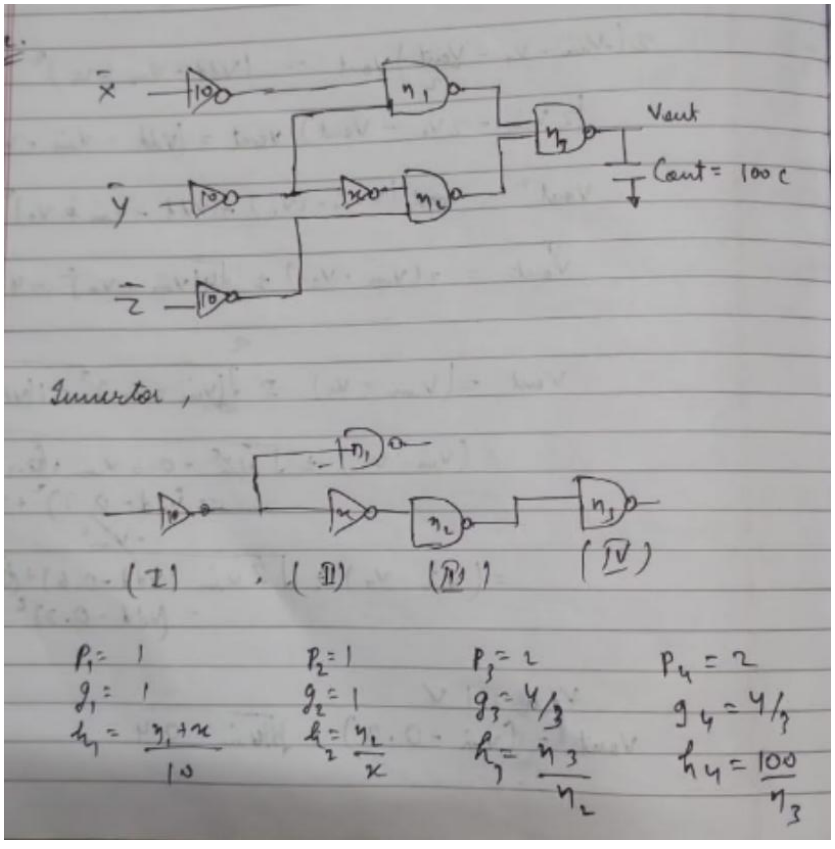


(LTspice for better propagation delay)



Delay from above LTspice stimulation = (8.0305-8.0000)ps = 30.5ps(approx.)

Theory:



(Normalized)

delay = $\Sigma p_i + \Sigma g_i h_i = \Sigma p_i + n(F)^{1/n}$

$\tilde{F} = GH = (4/3)^2$.

Total delay = $1 + \frac{n_1 + n}{10} + 1 + \frac{n_2}{n} + 2 + \frac{4}{3}\frac{n_3}{n_2}$

$+ 2 + \frac{4}{3} \times \frac{100}{n_3}$

$= 6 + \frac{n_1}{10} + \frac{n}{10} + \frac{n_2}{n} + \frac{4}{3}\frac{n_3}{n_2} + \frac{400}{3n_3}$

∴ {using AM-GM to find min^m delay}

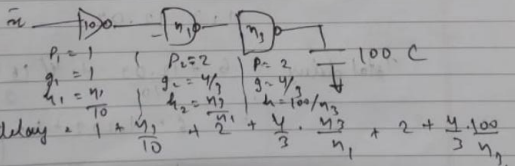
$= 6 + \frac{n_1}{10} + 4\left(\frac{n}{10} \times \frac{n_2}{n} \times \frac{4}{3} \times \frac{n_3}{n_2} \times \frac{400}{3n_3}\right)^{1/4}$

$= 6 + \frac{n_1}{10} + 4 \times \left(\frac{160}{9}\right)^{1/4}$

for n_3,

$\frac{400}{3n_3} = \left(\frac{160}{9}\right)^{1/4}$

$n_3 = \frac{400}{3 \times 2.057} = 64.94$



delay = $1 + \frac{n_1}{10} + 2 + \frac{4}{3} \cdot \frac{n_3}{n_1} + 2 + \frac{4}{3} \cdot \frac{100}{n_3}$

$= 5 + \frac{n_1}{10} + \frac{4}{3}\frac{n_3}{n_1} + \frac{4}{3}\frac{100}{n_3}$

Now, we know that this delay can't be maximum after critical path's delay, so we equate them to find n values for n_1.

$5 + \frac{n_1}{10} + \frac{4}{3}\left(\frac{n_3}{n_1}\right) + \frac{4}{3}\left(\frac{100}{n_3}\right) = 6 + \frac{n_1}{10} + 4\left(\frac{160}{9}\right)^{1/4}$

$\Rightarrow \frac{4}{3} \times \frac{n_3}{n_1} + \frac{4}{3}\frac{100}{n_3} = 1 + 4 \times \left(\frac{160}{9}\right)^{1/4}$

~~So, 86.58~~

using value of $n_3 = 64.94$

$\Rightarrow \frac{86.58}{n_1} + 2.0573 = 9213$

$\Rightarrow \frac{86.58}{n_1} = 7.157$

$n_1 = 12.09$

Total delay = $6 + \frac{12.09}{10} + 4\left(\frac{160}{9}\right)^{1/4}$

$= 6 + 1.209 + 4 \times \left(\frac{160}{9}\right)^{1/4}$

$= (15.422) \times 3RC$

$= 46.236\ RC$

Approximating R, C values for 45nm unit transistor

$R \approx 6K\Omega \div 3.0868/\beta = \frac{3.0868 \times 6}{\mu C_{ox} \omega} = 3.0868\Omega$

$\approx 6K\Omega$

$C = \frac{k_{ox} \varepsilon_{ox} w.L}{t_{ox}}$

$= \frac{3.9 \times 8.85 \times 10^{-14} \times 45 \times 10^{-9} \times 80 \times 10^{-9}}{1.25 \times 10^{-9}}$

$= 1.11 \times 10^{-16} F$

Actual delay (theoritical)

$\approx 46.276 \times 6 \times 10^{3} \times 1.11 \times 10^{-15}$

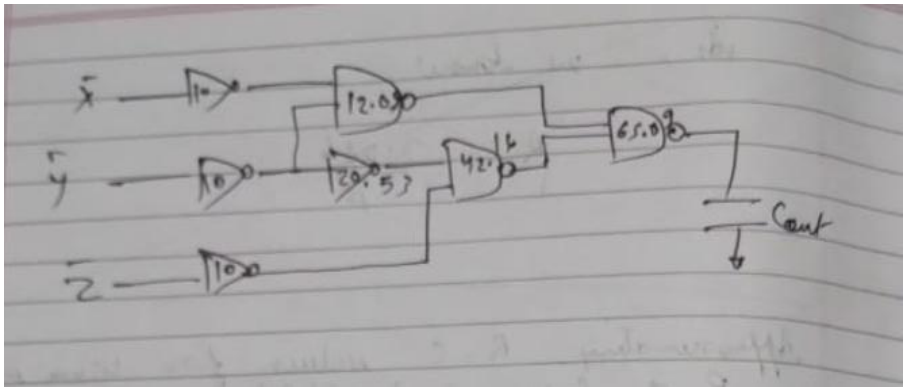
$\approx 30.5 ps$

$\frac{4}{3} \times \frac{n_3}{n_2} = \left(\frac{160}{9}\right)^{1/4} \quad | \quad \frac{x}{10} = \left(\frac{160}{9}\right)^{1/4}$

$n_2 = 42.16 \quad | \quad x = 20.53$

$\Rightarrow x = 20.53, \; n_1 = 12.09, \; n_2 = 42.16$

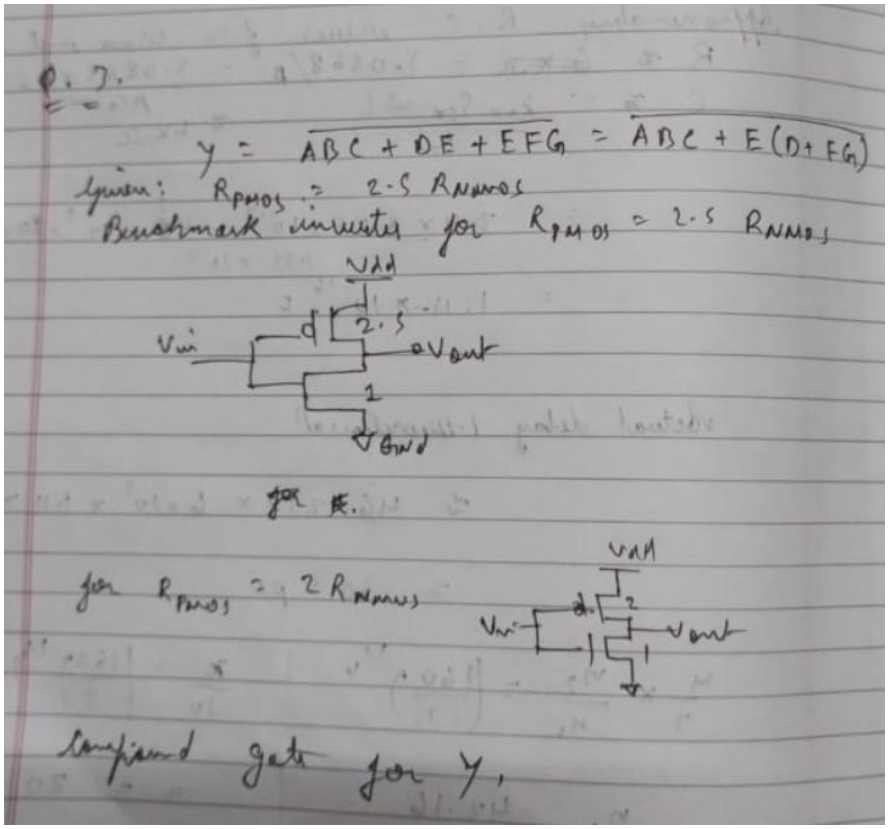
$n_3 = 64.94$

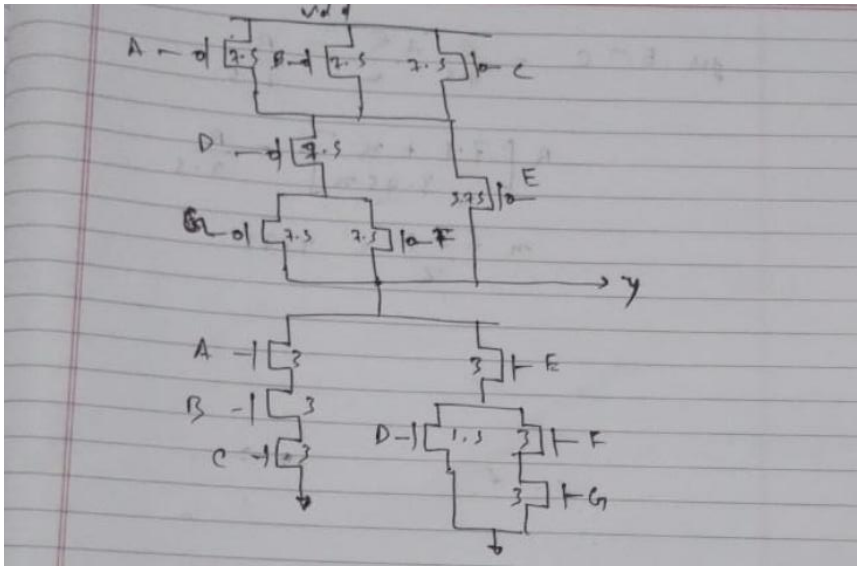


Q3.

Q3.) For the logic Y = ~(ABC + DE + EFG), implement transistor level schematic of the gate. Optimize the size of all NMOS and PMOS transistors such that the worst case rise and fall delays are equal to the fall delay of a minimum sized CMOS inverter, assuming RPMOS = 2.5 RNMOS.

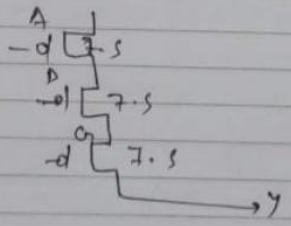
=>





Pull up circuit :

G → D → A



$$\frac{R}{7.5} + \frac{R}{7.5} + \frac{R}{7.5} = \frac{3R}{7.5} = \frac{R}{2.5}$$

for $F \rightarrow D \rightarrow A = \frac{R}{7.5} + \frac{R}{7.5} + \frac{R}{7.5} = \frac{3R}{7.5} = \frac{R}{2.5}$

for $E \rightarrow C = \frac{R}{7.5} + \frac{R}{x} = \frac{R}{2.5}$

$$R\left[\frac{7.5 + x}{3.75x}\right] = \frac{R}{2.5}$$

$$x = \frac{7.5}{2} = 3.75$$