Assignment#2

Q1.) Analyze the output voltage profile for Vin(t) defined below in Cadence simulation tool for an inverter circuit consisting of (W/L) of NMOS transistor as 2:1 and the (W/L) of PMOS as 4:1, and Vdd is 5V. Assume 130 nm technology node parameters. Draw the transient output voltage profile for the input voltage. Input voltage (Vin(t)) is defined as shown below:

$$Vin(t)=m \times t, for\ 0<t<1\ ps$$

$$Vin(t)=5V, for\ 1ps \leq t\ < 21\ ps$$

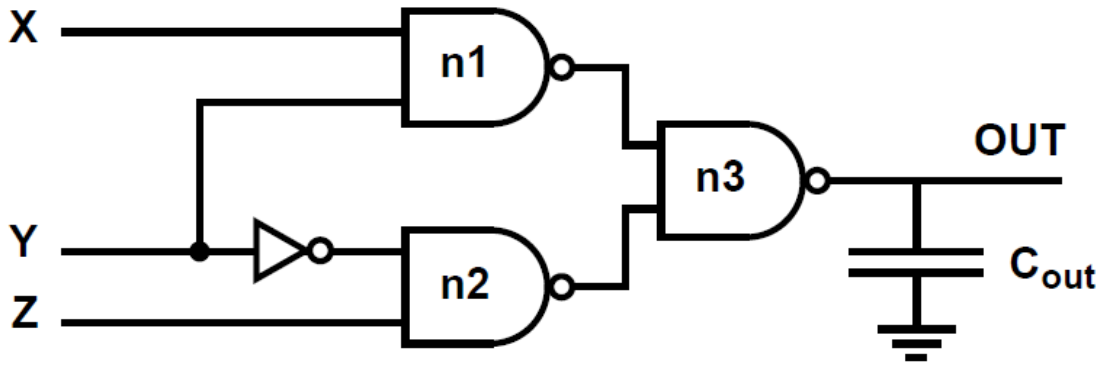
$$Vin(t)=(22-t) \times m, for\ 21ps < t < 22\ ps$$

$$Vin(t)=0\ V, for\ t \geq 22\ ps\ where\ m=5V/1ps$$

Also use the long channel current model expression mentioned in the Textbook, and determine the transient output voltage profile. You may use Matlab to find the solutions for a lengthy expression.

Q2.) Consider the CMOS circuit schematic shown below. The critical path is through inverter. Use logical effort to size these gates to minimize the delay through the critical path. Assume R_{PMOS} = 2 R_{NMOS}. Assume Cout = 10 Cin and that Cin applies to all inputs X, Y, and Z.

What is the minimum path delay through the inverter to OUT ? Verify the same in LT Spice using 22 nm and 45 nm model files (uploaded in the LMS), and assume Cin equal to 10 times unit NMOS transistor capacitance.



Q3.) For the logic Y = ~(ABC + DE + EFG), implement transistor level schematic of the gate. Optimize the size of all NMOS and PMOS transistors such that the worst case rise and fall delays are equal to the fall delay of a minimum sized CMOS inverter, assuming RPMOS = 2.5 RNMOS.