Open-Source ASIC Tool Flow: RTL Synthesis and Analysis

1. Area and Gate Count Estimation with Yosys

Yosys is the de-facto open-source synthesis tool that supports gate-level mapping and area estimation.

```
# Read all RTL files
read_verilog rtl/*.v

# Define top module (replace with your top)
hierarchy -check -top top_module

# Run synthesis passes
proc; opt; fsm; opt; memory; opt;

# Map to generic cells or a specific standard cell library
# (For generic gate count, use the built-in "techmap" and "abc" for logic optimization)
techmap; opt; abc -liberty your_lib.lib; opt;

# Print statistics (includes gate count, LUT count, etc)
stat

# Write synthesized netlist for backend or inspection
write_verilog synth_out.v
```

2. Detect Combinational Loops

Yosys warns about combinational loops during optimization (`opt`), e.g.,

Warning: Combinational loop detected!

You can also run:

yosys -p "read_verilog rtl/*.v; hierarchy -top top_module; proc; opt; stat"

and check warnings in the log.

3. Detect Gated Clocks

Open-source tools don't have a built-in command like Synopsys' `report_gated_clocks`, but you can:

- Search RTL for clock enables or gating logic (e.g., signals named `clk_en`, `clk_gate`).

- Use linting tools like Verilator or Yosys's lint command:

```
yosys -p "read_verilog rtl/*.v; hierarchy -top top_module; lint"
```

Look for clock gating related warnings manually.

4. Additional Open-Source Tools

- Verilator: Great for linting and detecting bad coding styles or potential loops.

- Icarus Verilog: For simulation to check behavior.

Example Workflow Script (run_synth.sh)

```
#!/bin/bash

# Synthesize with yosys
yosys synth.ys > synth.log

# Check synth.log for warnings/errors
grep -i warning synth.log
grep -i error synth.log

# Optional: lint RTL
yosys -p "read_verilog rtl/*.v; hierarchy -top top_module; lint" > lint.log

# Review lint.log manually or parse for gated clock signals

echo "Synthesis and linting done. Check synth.log and lint.log for details."
```

Summary

Feature	Open Source Tool(s)	Notes
Area & Gate Count	Yosys	Use `stat` after synthesis
Combinational Loops	Yosys	Detected during `opt` passes

| Gated Clocks | Manual + Yosys Linting | No direct report, manual check |

| Simulation | Icarus Verilog, Verilator | To verify behavior |

If you want, I can help write a complete Yosys synthesis script tailored to your RTL hierarchy or a Python parser for the Yosys output. Interested?