USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Change Registers Type in Chapter 13
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:
Changes the Register types in Chapter 13 to match definitions.

Benefits as a result of the changes:
A more clear definition of register behavior in Chapter 13.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
None

An analysis of the hardware implications:
None

An analysis of the software implications:
None

An analysis of the compliance testing implications:
None

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Actual Change

(a). Table 13-14, Vendor Specific 1 Capability Fields, Page 546

To Text:

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
3	VSC_CS_3	0	**Link Errors – Adapter A*** A Router shall set this field to 1b when the *Link Errors Enable – Adapter A* bit is 1b and one of the bits in the *Logical Layer Errors of Adapter A* is set to 1b. This bit is not valid if the *Link Errors Enable – Adapter A* bit is 0b. * Adapter A is the lowest-numbered Lane Adapter.	~~R/~~W/ Clr	0b
		1	**HEC Error – Adapter A** A Router shall set this field to 1b when the *Link Errors Enable – Adapter A* bit is 1b and a Transport Layer Packet is received on Adapter A with an uncorrectable HEC error in the header. This bit is not valid if the *HEC Error Enable – Adapter A* bit is 0b.	~~R/~~W/ Clr	0b
		2	**Flow Control Error – Adapter A** A Router shall set this field to 1b when the *Link Errors Enable – Adapter A* bit is 1b and a Transport Layer Packet is received on Adapter A for a flow controlled Path where the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the *Flow Control Error Enable – Adapter A* bit is 0b.	~~R/~~W/ Clr	0b
		3	**Reserved**	Rsvd	0b
		4	**Link Errors – Adapter B*** A Router shall set this field to 1b when the *Link Errors Enable – Adapter B* bit is 1b and one of the bits in the *Logical Layer Errors of Adapter B* is set to 1b. This bit is not valid if the *Link Errors Enable – Adapter B* bit is 0b. * Adapter B is the second lowest-numbered Lane Adapter	~~R/~~W/ Clr	0b
		5	**HEC Error – Adapter B** A Router shall set this field to 1b when the *Link Errors Enable – Adapter B* bit is 1b and a Transport Layer Packet is received on Adapter B with an uncorrectable HEC error in the header. This bit is not valid if the *HEC Error Enable – Adapter B* bit is 0b.	~~R/~~W/ Clr	0b
3	VSC_CS_3	6	**Flow Control Error – Adapter B** A Router shall set this field to 1b when the *Link Errors Enable – Adapter B* bit is 1b and a Transport Layer Packet is received on Adapter B on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the *Flow Control Error Enable – Adapter B* bit is 0b.	~~R/~~W/ Clr	0b
		7	**Reserved**	Rsvd	0b

DW	Register Name	Bit(s)	Field Name and Description	Type	Default Value
		8	**Link Errors – Adapter C*** A Router shall set this field to 1b when the *Link Errors Enable – Adapter C* bit is 1b and one of the bits in the *Logical Layer Errors of Adapter C* is set to 1b. This bit is not valid if the *Link Errors Enable – Adapter C* bit is 0b. * Adapter C is the third lowest-numbered Lane Adapter	~~R/~~W/ Clr	0b
		9	**HEC Error – Adapter C** A Router shall set this field to 1b when the *Link Errors Enable – Adapter C* bit is 1b and a Transport Layer Packet is received on Adapter C with an uncorrectable HEC error in the header. This bit is not valid if the *HEC Error Enable – Adapter C* bit is 0b.	~~R/~~W/ Clr	0b
		10	**Flow Control Error – Adapter C** A Router shall set this field to 1b when the *Link Errors Enable – Adapter C* bit is 1b and a Transport Layer Packet is received on Adapter C on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the *Flow Control Error Enable – Adapter C* bit is 0b.	~~R/~~W/ Clr	0b
		11	**Reserved**	Rsvd	0b
		12	**Link Errors – Adapter D*** A Router shall set this field to 1b when the *Link Errors Enable – Adapter D* bit is 1b and one of the bits in the *Logical Layer Errors of Adapter D* is set to 1b. This bit is not valid if the *Link Errors Enable – Adapter D* bit is 0b. * Adapter D is the fourth lowest-numbered Lane Adapter	~~R/~~W/ Clr	0b
		13	**HEC Error – Adapter D** A Router shall set this field to 1b when the *Link Errors Enable – Adapter D* bit is 1b and a Transport Layer Packet is received on Adapter D with an uncorrectable HEC error in the header. This bit is not valid if the *HEC Error Enable – Adapter D* bit is 0b.	~~R/~~W/ Clr	0b
		14	**Flow Control Error – Adapter D** A Router shall set this field to 1b when the *Link Errors Enable – Adapter D* bit is 1b and a Transport Layer Packet is received on Adapter D on a flow controlled Path and the appropriate buffer (dedicated or shared) has no space for the Packet or is not enabled. This bit is not valid if the *Flow Control Error Enable – Adapter D* bit is 0b.	~~R/~~W/ Clr	0b
		15	**Reserved**	Rsvd	0b