USB4 2.0 ENGINEERING CHANGE NOTICE FORM

Title: PCIe Revision Support
Applied to: USB4 Specification Version 2.0

Brief description of the functional changes:

1. Allow Internal PCIe Ports to support PCIe Revision 5.0
2. Change INTx from mandatory support to optional

Benefits as a result of the changes:

- PCI Express® Base Specification Revision 5.0 Version 1.0 was published on 5/22/2019
- The specification contains some enhancements relevant to USB4 tunneling
    - E.g., hot plug and unplug via DPC
- The USB4 specification should track releases of relevant specifications

Proposal: support PCIe 5.0 ports that interface a USB4 Domain

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

None

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

None

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Actual Change

(a). Section 1.5 Related Documents

PCI Express® Base Specification, Revision 4, Version 1, September 27, 2017 (PCIe Specification)

PCI Express® Base Specification, Revision 5.0, Version 1.0, 22 May 2019 (PCIe Specification)

(b). Section 11 PCI Express Tunneling

Editor Note: Insert at the end of Section 11, before Section 11.1

Note: A reference to the PCIe Specification in this chapter refers to either Revision 4 or Revision 5.0 depending on the revision supported by the Port.

(c). Section 11.2 Internal PCIe Ports

This section defines the functionality of an Internal PCIe Port that interfaces to a PCIe Adapter. An Internal PCIe Port shall be compatible with the PCI Express® Base Specification, Revision 4. An Internal PCIe Port may be compatible with the PCI Express® Base Specification, Revision 5.0. Each Internal PCIe Port that interfaces to a PCIe Adapter shall implement a Physical Layer Logical sub-block, a Data Link Layer, and a Transaction Layer as defined in the PCIe Specification with the modifications, configurations, and parameters described in this section.

(d). Section 12.5 Interrupts

A PCIe Host Router shall support Message Signaled Interrupt (either MSI or MSI-X or both). Supporting PCI Compatible INTx interrupt emulation is optional.~~INTx Interrupt Signaling and Message Signaled Interrupt (MSI and MSI-X).~~