USB4 1.0 ENGINEERING CHANGE NOTICE FORM

Title: Change in CL0s to CL1 Flow
Applied to: USB4 Specification Version 1.0

Brief description of the functional changes:

When a Port is in CL0s TX and it receives a CL1/2_REQ it shall respond according to the rules for a responding Port in the entry flow or with CL_NACK.

Benefits as a result of the changes:

Reducing the exit time from CL0s to CL0 and allow a flow to bring the Link to active state

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

None

An analysis of the hardware implications:

None

An analysis of the software implications:

None

An analysis of the compliance testing implications:

Need to verify Port can detect and behave accordingly when receiving CL1_ACK, CL0s_ACK and CL_NACK.

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Actual Change

(a). Section 4.2.1.6.5, Exit from State, Page 160
To Text:

1. Transition to CL0 state.
   - If the USB4 Port operated as a Dual-Lane Link prior to entry to CL0s state, the USB4 Port shall resume operation as a Dual-Lane Link independent of the setting of the TS2 Ordered Sets. A de-skew Ordered Set shall be sent as defined in Section 4.4.4. The scrambler shall load a new seed as defined in Section 4.3.5.
   - If the Router initiated exit from CL0s state due to receiving CL1_REQ or CL2_REQ Ordered Sets, then the Router shall not send any Transport Layer Packets before responding to the request Ordered Sets according to the rules in section 4.2.1.6.2 or with CL_NACK. The Router shall resume regular CL0 operation once it stops sending the CL_NACK Ordered Sets. ~~The Router shall not send any Transport Layer Packets before completing the CLx entry flow~~