

# USB4 2.0 ENGINEERING CHANGE NOTICE FORM

**Title: DPCD 0200Fh Handle**

**Applied to: USB4 Specification Version 2.0**

<b>Brief description of the functional changes:</b>
As defined by the DP Spec, DPCD 0200Fh should be treated the same as 00205h.

<b>Benefits as a result of the changes:</b>
Adds missing information to the specification.

<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
None

<b>An analysis of the hardware implications:</b>
None

<b>An analysis of the software implications:</b>
None

<b>An analysis of the compliance testing implications:</b>
None

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## Actual Change

### (a). Table 10-10. DPCD Internal Addresses

**Table 10-10. DPCD Internal Addresses**

Functionality	Address	Name
Link Training Control	00100h	LINK_BW_SET
	00101h	LANE_COUNT_SET
	00102h <sup>1</sup>	TRAINING_PATTERN_SET
	00103-6h <sup>1</sup>	TRAINING_LANE <sub>x</sub> _SET
Link Status <sup>1</sup>	00202h	LANE0_1_STATUS
	00203h	LANE2_3_STATUS
	00204h	LANE_ALIGN_STATUS_UPDATED
	00205h <sup>2</sup>	SINK_STATUS
	00206h	ADJUST_REQUEST_LANE0_1
	00207h	ADJUST_REQUEST_LANE2_3
	0200Ch	LANE0_1_STATUS_ESI
	0200Dh	LANE2_3_STATUS_ESI
	0200Eh	LANE_ALIGN_STATUS_UPDATED_ESI
	0200Fh <sup>2</sup>	SINK_STATUS_ESI
Link Quality Control	0010Bh	LINK_QUAL_LANE0_SET
	0010Ch	LINK_QUAL_LANE1_SET
	0010Dh	LINK_QUAL_LANE2_SET
	0010Eh	LINK_QUAL_LANE3_SET
	0010Fh	LINK_SQUARE_PATTERN_num+_1
DP Tunneling over USB4	E0000h – E00FFh	DP Tunneling over USB4 field DPCDs
Notes: 1. Link Status DPCD registers, TRAINING_PATTERN_SET, and TRAINING_LANE <sub>x</sub> _SET are Internal only during Link Training phase. Link Training phase starts when DPTX writes TRAINING_PATTERN_SELECT to a non-zero value and ends when it writes zero to TRAINING_PATTERN_SELECT. 2. When a DPTX reads addresses 00205h & 0200Fh during link training, a DP IN Adapter shall respond with value of 0h.		