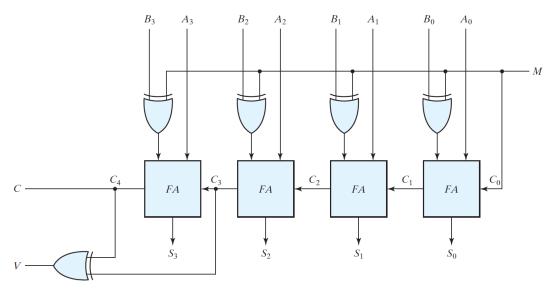


Name: Number: Quiz 2:

Experiment 2 – Implementation of Combinational Circuits with VHDL

Q)



The adder–subtractor circuit in the figure above has the following values for mode input M and data inputs A and B. In each case, determine the values of the four *SUM* outputs, the carry *C*, and overflow *V*.

М	A	В	SUM	С	V
0	0111	0110			
0	1000	1001			
1	1100	1000			
1	0101	1010			
1	0000	0001			