TSPC-Based **Serial Adder** and **Ripple Carry Adder** Using Microwind

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1. Introduction

The design of high-performance arithmetic circuits is a cornerstone of VLSI design. This project focuses on efficient sequential and parallel arithmetic units using True Single-Phase Clock (TSPC) logic, known for high speed and area efficiency. Our designs use two core building blocks: a TSPC D-Flip-Flop (D-FF) and a TSPC Full Adder. The D-FF acts as a one-bit memory element, capturing and storing data between clock cycles. It holds the carry-out in sequential operations and registers the final sum in the accumulator. The Full Adder performs binary addition of two input bits and a carry-in, producing sum and carry-out outputs. A Serial Adder was built using one Full Adder and a D-FF for area efficiency. A parallel Accumulator was also designed using a Ripple Carry Adder and D-FFs to compute a running total.

2. Tools and Technology Used

Microwind 3.0 – For CMOS layout design, transient simulation, and parameter extraction.
ClockType: Single-phase (TSPC).
Design Style: Dynamic logic using precharge and evaluation networks.

3. Theory of Operation

TSPC (True Single Phase Clock) logic operates using only one clock phase for both precharge and evaluation. This simplifies clock routing, improves switching speed, and reduces area overhead.

Operating Phases:

- Precharge Phase (CLK = 0): The PMOS precharge transistor is turned ON, charging dynamic nodes to logic ‘1’.
- Evaluation Phase (CLK = 1): The NMOS evaluation network discharges the dynamic nodes depending on input combinations.

Key Advantages:

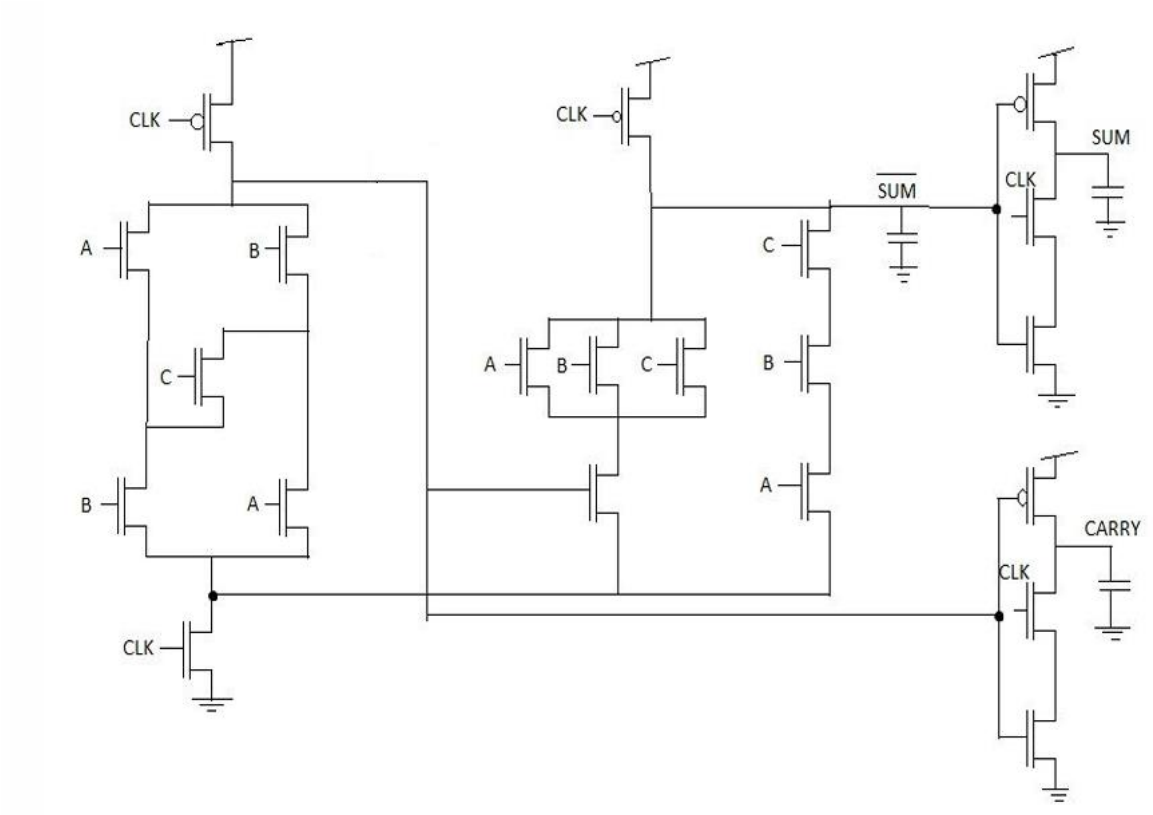
- High-speed operation with minimal clock skew.
- Reduced power dissipation compared to static CMOS.
- No need for complementary clocks (only one clock signal).

Weak keeper transistors are used to hold dynamic nodes during evaluation to prevent charge leakage.

4. Circuit Design

The fundamental building blocks for creating more complex arithmetic circuits are the **TSPC Full-Adder**, the **TSPC D Flip-Flop**, and by extension, the **Shift Register**. These components are all that is needed to construct both a serial adder and a ripple-carry adder. For the **serial adder**, a single Full-Adder performs the bit-wise calculation, while a D Flip-Flop is used to store and feed back the carry-out from one bit position to the next in the following clock cycle. For the **ripple-carry adder**, the design simply requires an array of Full-Adders connected in a chain, where the carry-out of one is the carry-in to the next. The D flip-flops are then used to form registers that hold the input operands and store the final output of the parallel addition.

1. TSPC Full Adder



Unlike a standard adder that provides an output continuously, the TSPC adder operates in two distinct phases controlled by a single clock signal (CLK). This dynamic approach is the key to its efficiency.

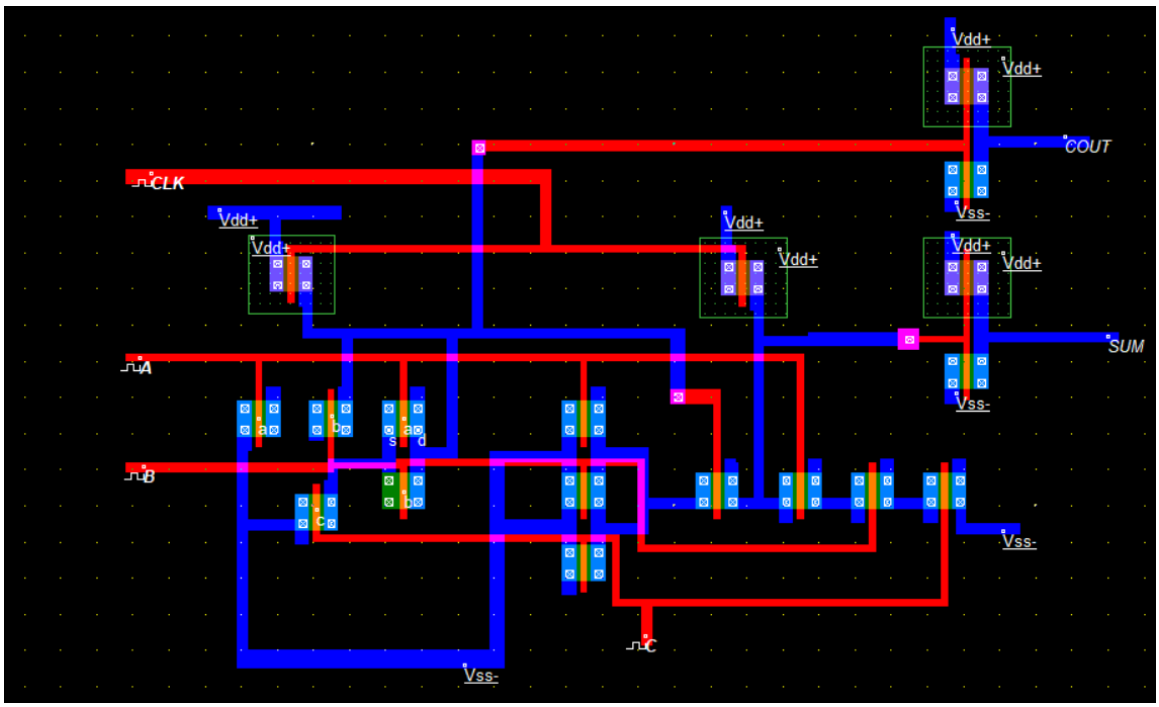
1. **Precharge Phase (when CLK is LOW):**
    - The PMOS transistors at the top (connected to CLK) turn **ON**.
    - This charges the internal nodes for both the SUM and CARRY logic to a HIGH voltage level. The circuit is essentially "reset" in preparation for the calculation.
2. **Evaluation Phase (when CLK is HIGH):**
    - The PMOS precharge transistors turn **OFF**, and the NMOS transistors at the bottom turn **ON**.
    - The logic is now "evaluated." Depending on the inputs (A, B, C), the pull-down networks of NMOS transistors will either create a path to ground or not.
    - If a path is created, the precharged HIGH node is discharged to LOW. If no path exists, it remains HIGH.
    - The final output latches capture these results to produce the final SUM and CARRY outputs.

This precharge-evaluate cycle allows the circuit to perform complex logic with a very simple and fast structure.

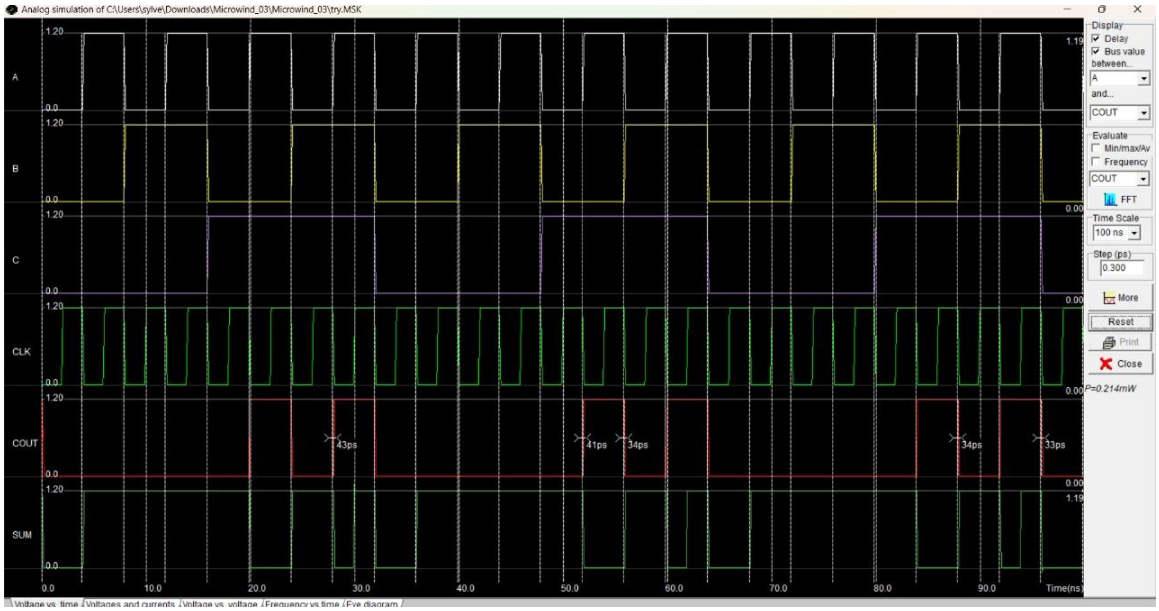
Truth Table of a Full Adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Layout Design of TSPC Full Adder



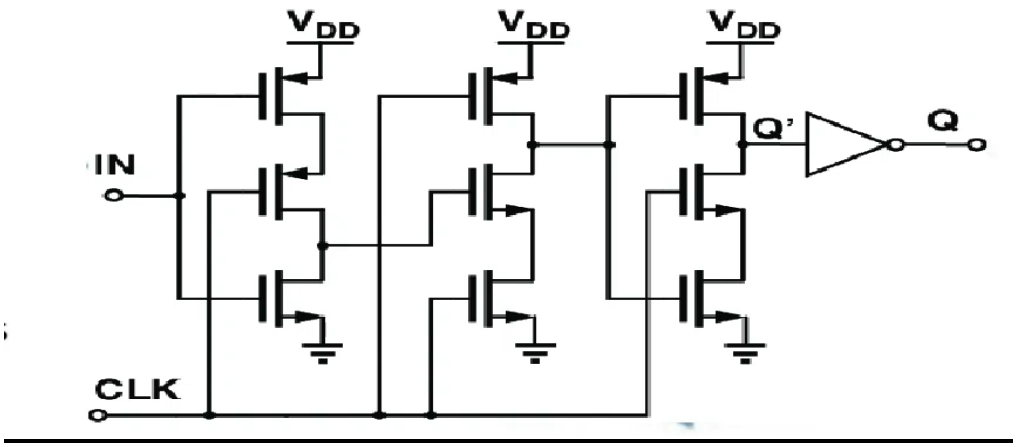
Simulation Of TSPC Full Adder



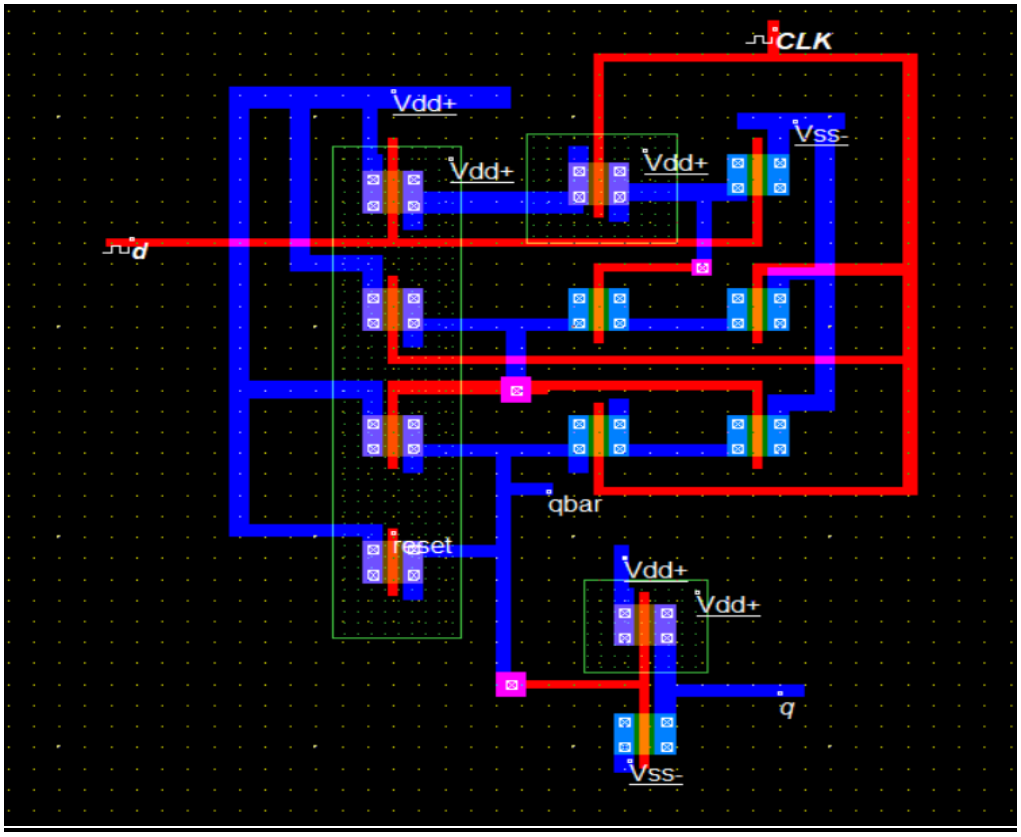
2. TSPC D Flip-Flop

A **TSPC D flip-flop** is a type of dynamic flip-flop that uses a single clock signal to control its operation. Unlike a normal static flip-flop, it works in two phases: a **precharge** phase (when the clock is low) and an **evaluate** phase (when the clock is high). During precharge, internal nodes are set to a known state, and during the evaluate phase, the input is sampled, and the output is determined, TSPC flip-flops are generally faster because they have a lower transistor count and simpler logic, which reduces parasitic capacitance and allows for quicker switching.

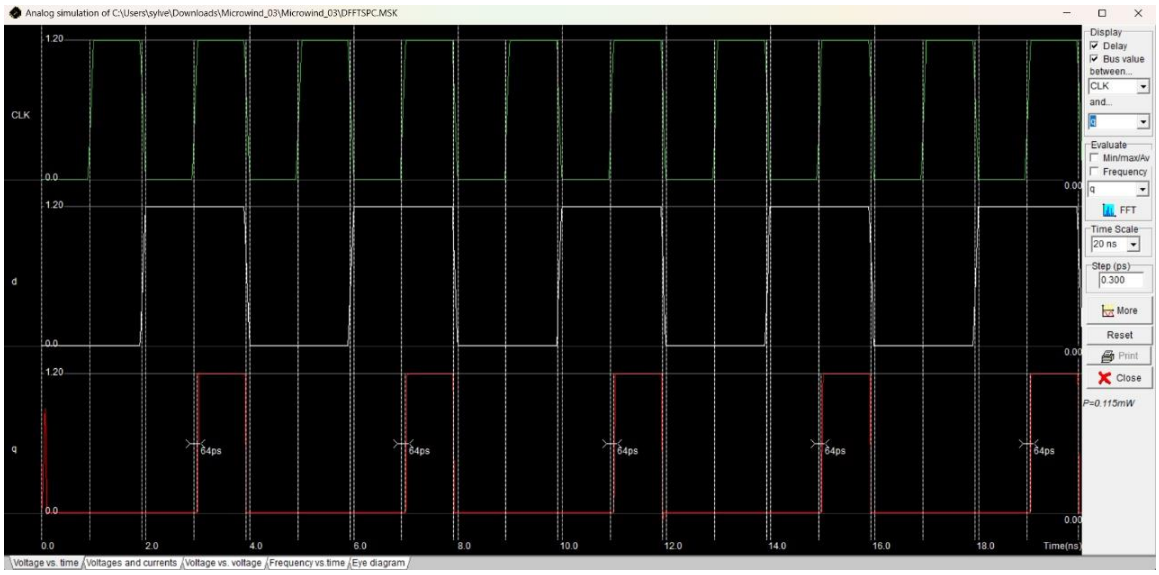
Circuit Diagram of TSPC D Flip Flop



Layout Design of TSPC D Flip Flop



Simulation Of TSPC D Flip Flop

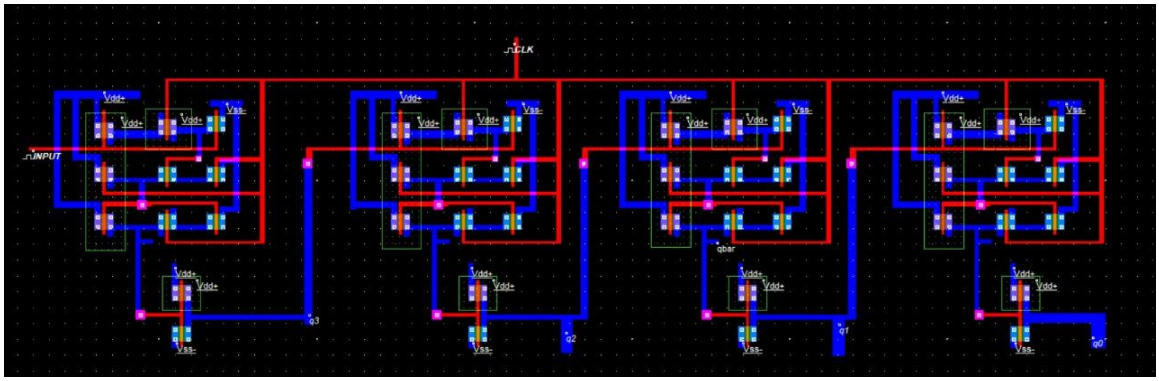


3. 4 Bit TSPC Shift Register

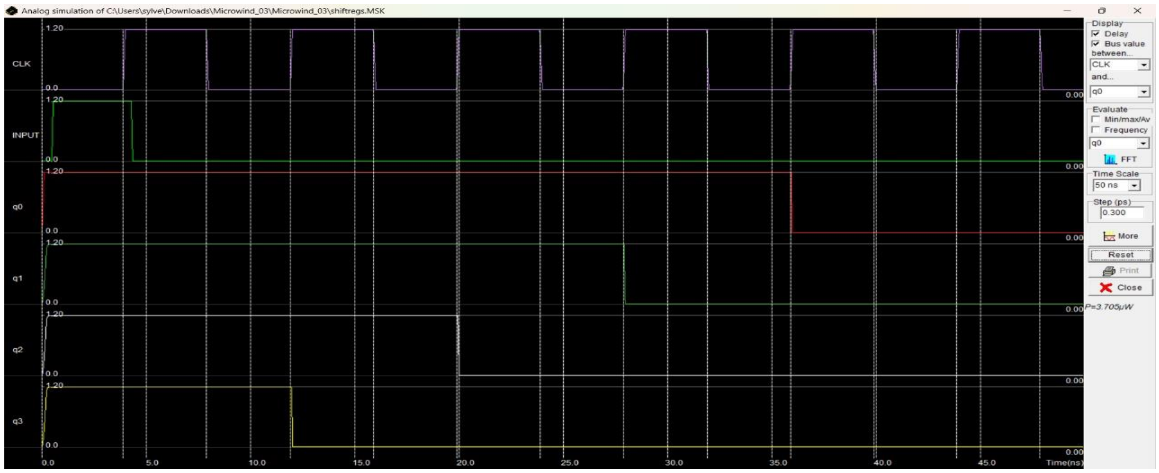
A shift register is a sequential logic circuit used to store and move binary data through a series of flip-flops under the control of a clock signal. A 4-bit shift register consists of four flip-flops connected in sequence, where the output of one flip-flop becomes the input of the next.

When implemented using True Single Phase Clock (TSPC) logic, the circuit achieves high-speed operation, reduced area, and simpler clock routing compared to conventional static CMOS shift registers.

Layout Design of TSPC Shift Register



Simulation Of TSPC Shift Register



TSPC Serial Adder

The TSPC Serial Adder consists of the following main blocks:

TSPC Full Adder (FA) – performs one-bit binary addition.

TSPC D Flip-Flop (Carry Storage) – holds the carry-out from one addition cycle and feeds it back as the next carry-in.

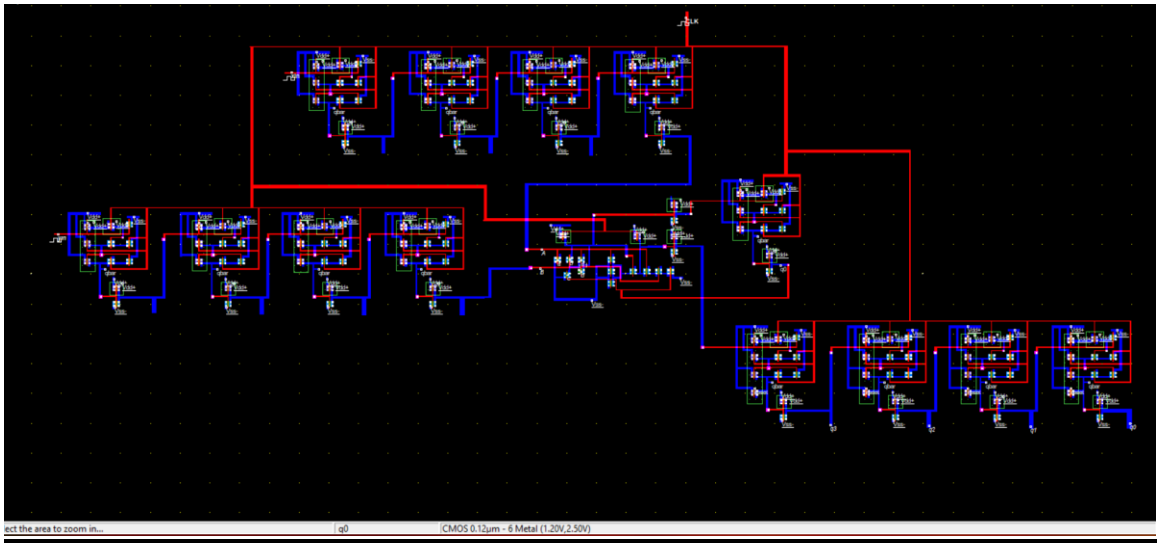
Shift Register A – stores the first operand (A) and shifts bits serially toward the adder.

Shift Register B – stores the second operand (B) and shifts bits serially toward the adder.

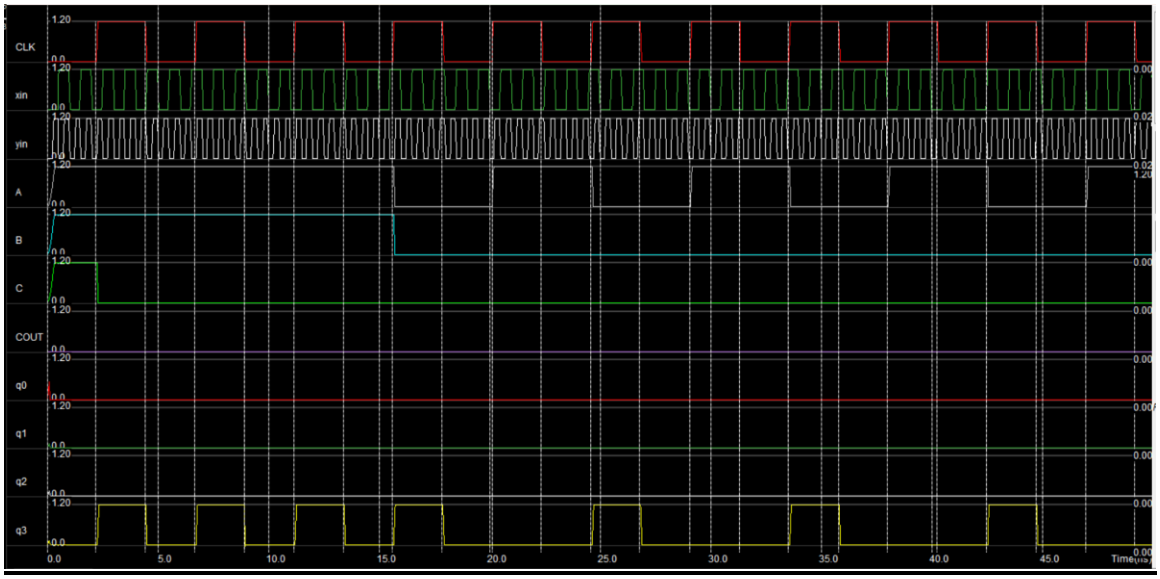
Shift Register Sum – stores the sum and shifts bits serially.

Clock Signal (CLK) – single-phase clock that controls all dynamic operations simultaneously.

Layout Design of TSPC Serial Adder



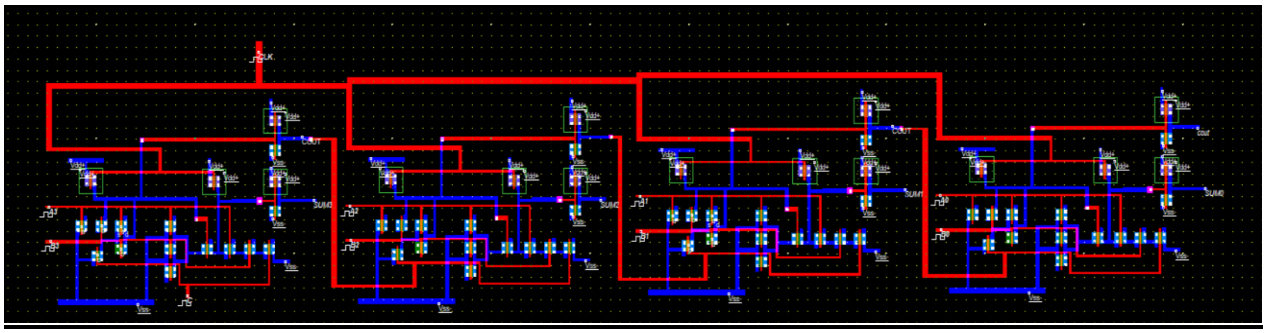
Simulation Of TSPC Serial Adder



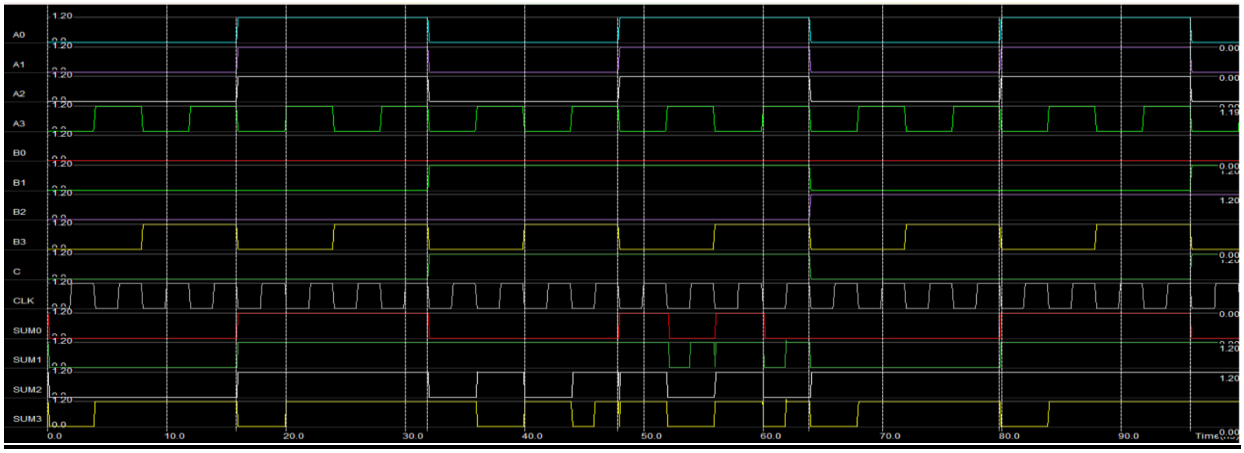
TSPC 4-Bit Ripple Carry Adder

A 4-bit Ripple Carry Adder (RCA) is built by cascading four TSPC Full Adders to perform multi-bit binary addition. Each TSPC Full Adder computes the sum and carry for its bit, while the carry-out ripples to the next higher bit. The array of four adders forms the core of the parallel accumulator, enabling 4-bit additions each clock cycle. A bank of TSPC D-Flip-Flops (D-FFs) is used to register the 4-bit sum, providing synchronized storage of the running total. The D-FFs also capture the final carry when required for extended arithmetic or chaining. Using TSPC cells ensures high-speed operation and area efficiency for the 4-bit RCA. The design retains the same precharge/evaluate timing characteristics of single-bit TSPC blocks, scaled across four bits. This 4-bit RCA plus register implements a compact, fast parallel accumulator suitable for VLSI arithmetic units.

Layout Design of TSPC Ripple Carry Adder



Simulation Of TSPC Ripple Carry Adder



5.Conclusion

In the TSPC Serial Adder, integration of shift registers, a full adder, and a D flip-flop enabled sequential bit-by-bit addition with significantly reduced hardware. The TSPC D Flip-Flop ensured proper carry storage and propagation between cycles while maintaining dynamic stability through weak keeper transistors.

The 4-bit TSPC Ripple Carry Adder demonstrated parallel addition capability with fast carry propagation and high operating speed.

The 4-bit TSPC Register and Shift Register further highlighted the versatility of single-phase clocked dynamic circuits in designing compact and high-speed sequential systems. These designs show reduced transistor count, smaller layout area, and improved timing performance compared to conventional static CMOS counterparts.