**STEP 3: Open loop Control of a Fan’s Speed**

**Pulse Width modulation PWM:**

A common digital-to-analog conversion technique is to pulse-width modulate (PWM) a digital output pin. The pin is switched between low and high. Controlling the duty cycle adjusts the average value of the waveform.

T

PW

A common application of PWM is in motor control

**PWM Generator:   
SE3:** The FPGA board clk is 50MHz (20nS). For a PWM of 10KHz and 8-bit resolution: T=0.1mS≈100,000nS. Thus the PC counter (8-bit binary counter) must be incremented ever 100000/256 = 391 nS ( about 19 clk cycles). To time the incrimination of PC the counter IC is used. IC is loaded with 18 and decremented with every clk pulse until it reaches 0 when PC is incremented.  
**Nexys4:** The FPGA board clk is 100MHz (10nS). For a PWM of 10KHz and 8-bit resolution: T=0.1mS≈100,000nS. Thus the PC counter (8-bit binary counter) must be incremented ever 100000/256 = 391 nS (about 39 clk cycles). To time the incrimination of PC the counter IC is used. IC is loaded with 38 and decremented with every clk pulse until it reaches 0 when PC is incremented.

IC==0

Yes

Yes

No

No

No

Yes

PC < PW

PW ==0

Yes

PW ==255

No

**Measuring the speed:**To measure the frequency a counter can be used. After resetting the counter it is enabled for a period MP. The counter is then incremented at the positive edge of each input signal’s pulse (s). The count at the end of the period MP divided by the period MP is the frequency.

s

reset

MPW

count

0

1

2

3

4

5

counter

reset

enable

clk

16

count

The division step can be avoided by choosing MP to be 1/(unit of measurement). For example if we want to measure in units of kHz, then T=1/1000=1ms. So when the count is 10:

Let the maximum frequency of the signal s be fsmax. To map fsmax to a value of 255 an 8-bit counter is used to measure the speed. Thus the measuring period (MP) in clk cycles will be:

The size of the measuring counter (MPC) can be computed from:

**Speed Meter:**

MPC==0

pe

yes

yes

no

no

LV

TV

T

8

clk

clk

PWM

PWM  
Generator

8

ADC

pw

L

**filter**

W

T

8

Binary to BCD  
Converter

8

pe

DPW

DL

DT

12

12

L

8

12

S

12

8

Speed  
Meter

DI

W

DI  
Controller

Df

WADD

clk

DIN

**Filter:**

D

Q

SS

DSS

clk

pe

8-bit shift register

SISHR

W

clk

Q[7:0]

8

S1

S0

1

0

I0

I1

I2

I3

PWM

Half-  
Bridge

Vmotor

300Ω

74HC14

decoder

w

**Hardware:**

For the purpose of this step you will feed T into PWM generator.

**PreLab:**

1. Write the Verilog code for the PWM generator and the speed meter
2. Write the necessary Test Fixture code to simulate theses subsystems

**Lab:**

1. Complete the system Verilog code.
2. Implement your design
3. Test your system.
4. Measure the motor’s speed as a function of PW . In addition to temperature and light, both the fan’s speed and PW are displayed.. Then graph the fan’s speed as a function of PW.
5. Measure the step response of the motor.
6. Demonstrate your system