



SC13 Emerging Technologies Power Efficient, Scalable Hybrid DSP+ARM+FPGA Platform

for Computer Vision Tasks

Object Detection and Tracking with TI C66x Digital Signal Processor

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Objective: real-time object detection and tracking for arbitrarily high resolution imaging on a mobile platform

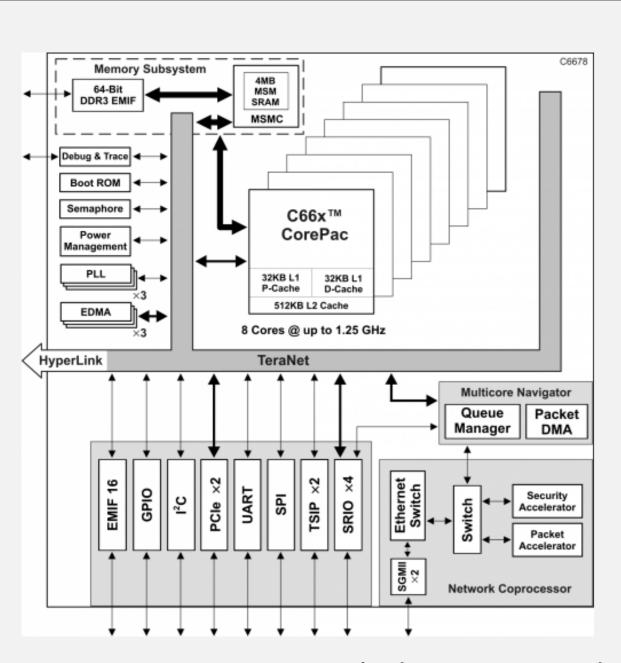


Algorithm: (1) dense optical flow, (2) cluster flow field pixels using BFS

Challenge:

- Optical flow requires, per 1920x1080 frame:
 - > 180M floating-point operations,
 - > 5.4 Gflops sustained for 30 fps (in addition to video, communication, and post processing overheads)
 - Need to scale for higher resolutions
- Embedded processors generally can't achieve this performance
- Embedded processor + GPU is power inefficient
- GPUs cannot run independently (no O/S)

Texas Instruments C6678 Keystone DSP:



- Keystone SoC includes integrated peripherals/offchip interfaces:
 - Gb ethernet, Serial RapidIO, PCIe, Hyperlink, DMA engine

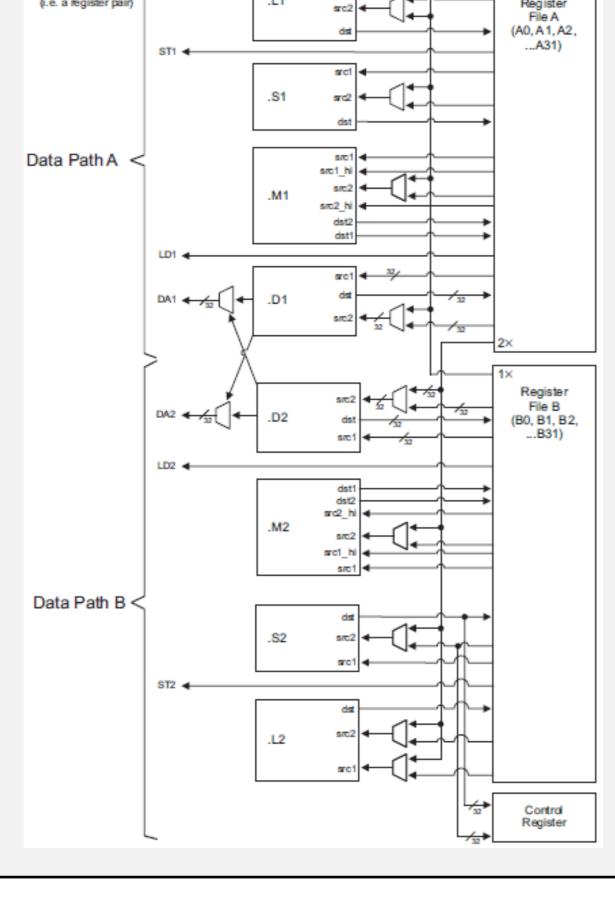
Default bus width

- Eight DSP cores on chip
- Each core: eightway VLIW µarch
- Cores are logically decoupled
- 128 peak
- theoretical Gflops 128 GB/s
- scratchpad b/w 12.8 peak GB/s
- DDR3 b/w

DSP core design:

- Two 32x32 register files
- Eight functional units
- 1. S unit: general arithmetic operations (2 flops/cycle) 2. L unit: general arithmetic
- operations (2 flops/cycle)
- 3. M unit: multiply (4 flops/cycle)
- 4. D unit: 8-byte load/store

ILP exploited through programmer- and compiler-scheduled software pipelining for VLIW and SIMD



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Optical Flow:

Assume brightness of pixels are subject to constraint:

$$I(x, y, t) = I(x + \Delta x, y + \Delta y, t + \Delta t)$$

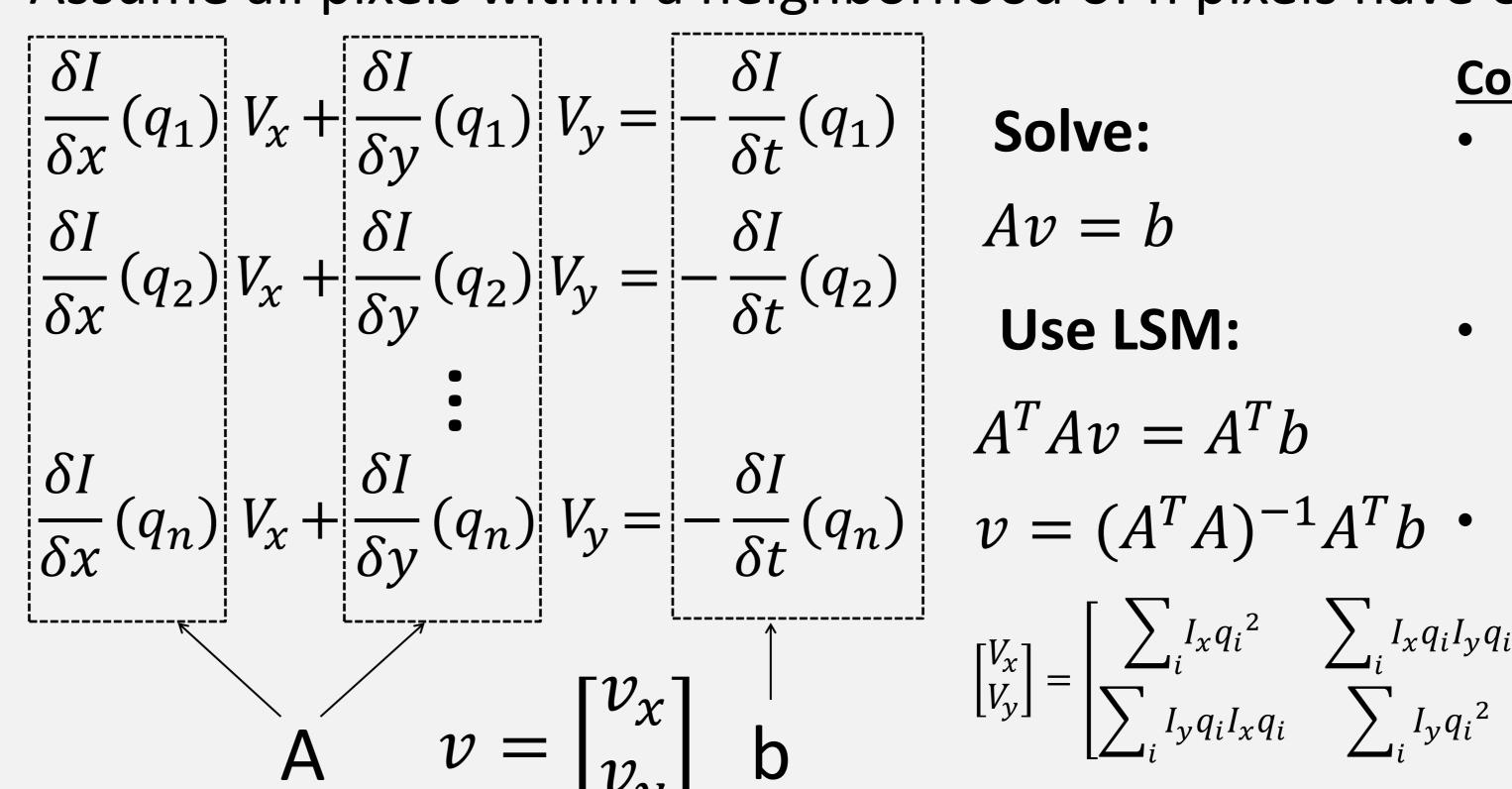
Apply first-order Taylor expansion:

$$I(x + \Delta x, y + \Delta y, t + \Delta t) = I(x, y, t) + \frac{\delta I}{\delta x} \Delta x + \frac{\delta I}{\delta y} \Delta y + \frac{\delta I}{\delta t} \Delta t$$
 ...implies:

$$\frac{\delta I}{\delta x} \Delta x + \frac{\delta I}{\delta y} \Delta y + \frac{\delta I}{\delta t} \Delta t = 0 \qquad \frac{\delta I}{\delta x} \frac{\Delta x}{\Delta t} + \frac{\delta I}{\delta y} \frac{\Delta y}{\Delta t} + \frac{\delta I}{\delta t} = 0 \qquad \frac{\delta I}{\delta x} \frac{\delta y}{\delta x} + \frac{\delta I}{\delta y} \frac{\delta y}{\delta y} = -\frac{\delta I}{\delta t}$$

Lucas Kanade Method:

Assume all pixels within a neighborhood of n pixels have equal V_x and V_y :



Use LSM:

Computational steps:

- Compute A (x and y part. derivatives)
- Compute b (t derivative part. derivative) Compute v

$$\begin{bmatrix} V_{x} \\ V_{y} \end{bmatrix} = \begin{bmatrix} \sum_{i}^{l} I_{x} q_{i}^{2} & \sum_{i}^{l} I_{x} q_{i} I_{y} q_{i} \\ \sum_{i}^{l} I_{y} q_{i} I_{x} q_{i} & \sum_{i}^{l} I_{y} q_{i}^{2} \end{bmatrix}^{-1} \begin{bmatrix} -\sum_{i}^{l} I_{x} q_{i} I_{t} q_{i} \\ -\sum_{i}^{l} I_{y} q_{i} I_{t} q_{i} \end{bmatrix}$$



frame *n*+1 frame *n*

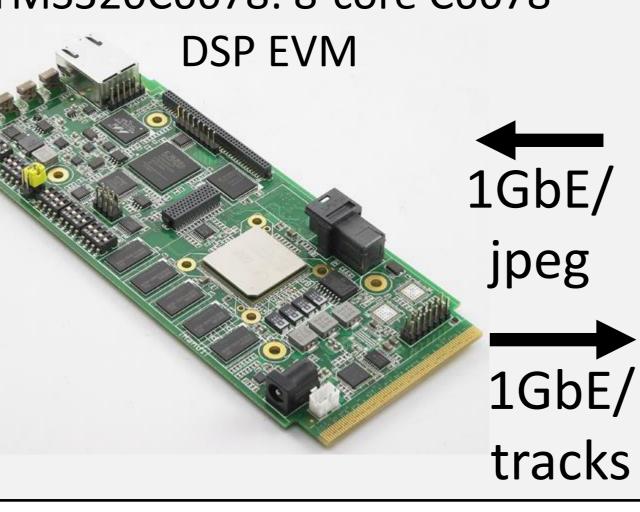
derivatives green=dI/dx, red=dI/dy,

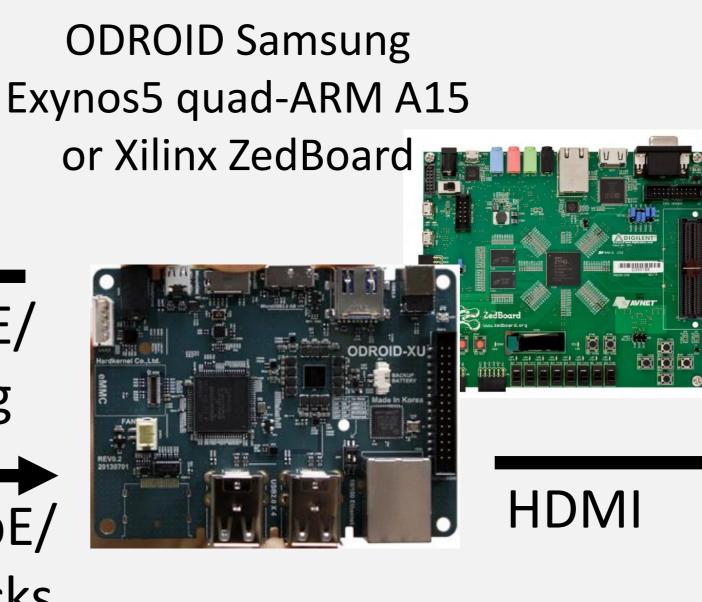
blue=dI/dt

optical flow red = |V|

Custom Platform:

TMS320C6678: 8-core C6678 DSP EVM







Code Optimizations:

- Hand-scheduled loops to increase VLIW/SIMD utilization
- DMA to scratchpad memory
- Parallelize over seven DSP cores (one core used for network interface)

Power Consumption:

~16 Watts peak (+5 W with onboard emulator)

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Performance Results:						
Kernel	Flops per byte	% total frame time	C66 eff. IPC per DSP core	C66 eff. Gflops (7 cores)	C66 Scratchpad eff. b/w	C66 DRAM eff. b/w
Jpeg decode		33%				
Copy blocks on chip		5%				5.6 GB/s
Gaussian blur	0.41	16%	3.9 / 8	16.8	42 GB/s	
Derivative	0.59	7%	4.2 / 8	20.3	35 GB/s	
Least square method	0.33	23%	2.5 / 8	10.5	29 GB/s	
Copy blocks off chip		13%				5.6 GB/s
Clustering		2%				