Lab Report - Lab1
CS391
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For me personally, most of this lab comprised of becoming familiar with the syntax of SystemVerilog and how to properly use the language. After each step of adding different test cases for functions and refactoring code, I got much more used to how how the language was structured. When approaching the problems in the exercises, I referenced back my knowledge from CS210 and the CS391 lecture slides to know how to format my files and logic especially when it was to time to create my test benches. Additionally, at certain times, I had to make sure that the bit constraint for certain registers aligned with what I placed in my test bench and initial ALU module. This step showed me how precise SystemVerilog is in coding hardware. Overall, the major challenge to this lab was learning and implementing the syntax of SystemVerilog, but after I was able to place all Gate functions and comparators requested through repetition and slowly understanding the code.