

Bakshree Mishra

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EDUCATION

PhD in Computer Science **2021-Present**
University of Illinois, Urbana-Champaign **GPA: 3.9/4**

ADVISOR: Prof. Sarita Adve

AREAS OF INTEREST: Computer Architecture, Hardware-Software Codesign, Machine Learning & Systems

M.Tech in Computer Science **2015-2017**
National Institute Of Technology, Rourkela **GPA: 9.69/10**

ADVISORS: Prof. Bansidhar Majhi (NIT Rourkela), Mr. Tarjinder Singh (Intel)

B.Tech in Computer Science and Engineering **2010-2014**
College Of Engineering and Technology, Bhubaneswar **GPA: 8.85/10**

PUBLICATIONS

(Under Review:) Suresh, V. and Mishra, B. and Zhu, Z. and Jing, Y. and Jin, N. and Block, C. and Mantovani, P. and Giri, D. and Zuckerman, J. and Carloni, L. and Adve, S. *Taming the Acceleration Tax: Enabling New Opportunities for Accelerator-Level Parallelism*

Mishra, B. and Chakraborty, D. and Makkadayil, S. and Patil, S. D. and Nallani, B. *Hardware Acceleration of Computer Vision and Deep Learning Algorithms on the Edge using OpenCL*, Proceedings of EAI Endorsed Transactions on Cloud Systems, 2019 [\[Paper\]](#)

WORK EXPERIENCE

Graduate (PhD) Intern May 2024 – Aug 2024
Analytical modelling of data movement optimizations. *AMD, Bellevue*

Graduate Research Assistant May 2022 – Present
Heterogeneous disaggregated accelerator systems *University of Illinois, Urbana Champaign*

Graduate Teaching Assistant August 2021 – May 2022
CS 233 Computer Architecture, CS 225 Data Structures *University of Illinois, Urbana Champaign*

ML and IP Design Engineer June 2017 – August 2021
Analysis and acceleration of machine learning algorithms *Intel Corporation, Bangalore*

Graduate Technical Intern May 2016 – May 2017
Acceleration of pedestrian detection and other ADAS algorithms *Intel Corporation, Bangalore*

Assistant System Engineer June 2014 – July 2015
Development of E-Municipality portal *Tata Consultancy Services, Bhubaneswar*

Summer Intern June 2013 – August 2013
Prototype modules for E-Municipality portal *Tata Consultancy Services, Bhubaneswar*

PROJECTS

With Prof. Sarita Adve (2021 - Present)

Hardware acceleration with heterogeneous disaggregated accelerator systems June 2022 – Present

- Designed and implemented light-weight accelerator synchronization interface (ASI) in System-C, compatible with the accelerator suite from Columbia's heterogeneous SoC **ESP framework**, synthesizable to FPGA bitfile
- Created a synthetic accelerator benchmark suite to evaluate trade-offs of monolithic and disaggregated accelerator systems for workloads with different compute patterns and intensities
- Analyzed impact of ASI and disaggregated accelerator systems in accelerating complex workloads such as spatial audio, Mini-ERA and FCNNs
- Conducted all the evaluations on Linux booted over a heterogeneous SoC instantiated on FPGA

Evaluation of Spandex Coherence Protocol August 2021 – June 2022

- Converted the collaborative autonomous vehicle workload, Mini-ERA, to baremetal for evaluation on FPGA
- Benchmarked the impact of data movement and coherence on accelerating baremetal Mini-ERA on a heterogeneous SoC (instantiated on FPGA using ESP framework)
- Simulated on-vehicle sensor behavior to evaluate data movement overheads for the end-to-end workload

- Evaluated the overheads for different coherence protocols including MESI, Coherent DMA and Spandex-FCS on FPGA, and characterized their behavior using simulation waveforms.

Select Projects at Intel India (2016 - 2021)

Real-Time Barcode Localization and Detection on Edge Devices

- Created custom accelerator for the algorithm bottleneck, Barcode localization, using OpenCL HLS
- Highly pipelined architecture leveraging data redundancy in algorithm
- Improved performance from **19 FPS** to **104 FPS** on 2MP video to satisfy industrial constraints
- **Internal paper** accepted at Intel Design and Test Technology Conference (DTTC), 2019

Real-Time Optical Character Recognition on Edge Devices

- Created OpenCL based FPGA accelerator having parallel convolution engines and buffered partial results
- Accelerator improved performance from detected 250 characters at **10 FPS** to **50 FPS** from 2MP video
- Presented **live demo** at Intel DTTC, Portland, OR, 2019
- **Paper** presented at IEEE WinTechCon, Bangalore, India, 2019

Hardware Design for Functional Safety IP

- Designed hardware for Fault Detector module for Functional Safety (FuSa).
- Analyzed High Level Architecture Specification (HAS) and created Micro Architecture Specifications (MAS)
- The IP achieved ISO26262 certification for Functional Safety
- **Internal paper** on our work was accepted at Intel DTTC 2019, **patent application filed**.

Real-Time Pedestrian Detection System Using OpenCL-Based FPGA Acceleration

- Created a custom architecture for computer vision based Pedestrian Detection system for Master's research
- Deep-dived into FPGA OpenCL compiler optimization issues and reported to the compiler team
- Independently improved initial design to give **3x** performance while reducing area by **10x**

SELECT AWARDS AND HONORS

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| • Among Teachers Ranked as Excellent for CS225 in Spring 2022 | 2022 |
| • Best Paper in Track Award, Intel HSPE TechCon 2021 | 2021 |
| • Two Departmental Recognition Awards for customer and leadership demos | 2020 |
| • Co-authored 2 accepted internal papers and presented a demo at Intel DTTC, Portland, OR | 2019 |
| • Two Intel Division Recognition Awards for critical contributions | 2019 |
| • Intel Division Recognition Award for Masters' Project | 2017 |
| • 2 nd Runners' Up in Intel India WIN Hackathon | 2017 |
| • Ranked 2 nd among all Masters (~110) students in CS Department at NIT Rourkela | 2017 |
| • CET Merit Scholarship (Undergrad scholarship 2010-2014) | 2010 |
| • Won the prestigious National Talent Search Examination Scholarship | 2008 |
| • Rajiv Gandhi Chhatra Prativa Award for ranking 8 th in Odisha State, in the X th Grade National Boards | 2008 |

TECHNICAL SKILLS

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|--------------------|---|
| • Languages | C/C++, Python, MATLAB, OpenCL, System-C, System Verilog |
| • Tools | Quartus, Design Compiler, Vivado, Stratus, V-Tune, NSight |

VOLUNTEERING AND SERVICE

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|---|----------------|
| • Co-chair of the Systems and Architecture session for the 19 th CSL Student Conference | 2024 |
| • Co-started and run weekly coffee meet-ups for women in comp. arch in CS and ECE | 2022 - present |
| • Named one of Top 50 Volunteers in Intel India, for service at Cancer Hospice Karunashraya | 2020 |
| • Won an Intel Seed Grant and oversaw renovation of nurses' dining hall at Karunashraya | 2019 |
| • During undergrad, co-founded the student e-zine CET Rising , and served as Chief Editor | 2013 - 2014 |