EE 705: VLSI DESIGN LAB 2025

PROJECT- FULL INTEGRATION - ASIC

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. Keep the port names and module names as mentioned in the question.
3. Code must be in **Verilog**
4. **Submit all your Verilog codes and TBs.**
5. **Submission and Evaluation Deadline: 15/04/2025**

TASK-1:

1) After the integration and testing is done on FPGA, you are expected to use the integrated modules to generate the RTL-GDS Flow on OpenLane.
2) Instantiate icache_tag_ram.v (Instruction memory) and icache_data_ram.v (Data memory) with the OpenRAM generated memories. Kindly note that you will be including the .lib, .lef and .gds files of these memories in your synthesis and pnr scripts along with the sky130 files.
   Note: No need to perform Post-synthesis or Post-pnr simulation.
3) Need to include the following in your report:
   a) Go to reports/signoff and paste the screenshot of .lvs.rpt file.

   b) Config.json and placement.cfg file screenshot

   c) Layout of the design on Magic (screenshot). Also, mark the (X,Y) dimension on the layout.

   d) Report the number of cells used.

   e) Go to the logs/routing folder, open the design_sta.log and fill up the table below:

Clock Frequency (MHz)	
Worst case setup slack (ns)	
Worst case hold slack (ns)	
Design area (μm^2)	
Total Power Consumption (µW)	

TASK-2:

1) Run the Openlane RTL-GDS flow on the modules that you were assigned in PART-A of the project and generate the GDS and other files.
2) (Only for TASK-2) On the Openlane, you will be performing Post-synthesis simulation on the netlist by writing appropriate test bench for your modules.
3) Now as two groups are merged into one, so there will be two different modules that needs to be worked on for TASK-2 separately (but the evaluation will happen together).

For example: Say group1 had their PART-A project as CSR and group2 had their PART-A project as EXEC. Say, group1 and group2 were combined for the final integration, then in TASK-2 you will create GDS for CSR and EXEC separately. Also, perform Post-synthesis simulation on those two modules separately.

4) Need to include the following in your report:
   a) Include everything that was mentioned in TASK-1.
   b) Include the Post-synthesis simulation results and waveforms.