Friday	EE 705: VLSI DESIGN LAB 2025	Due On
JAN 17, 2025	ASSIGNMENT-2	JAN 24, 2025

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. You can use VIO, ILA, BRAM, CLK WIZARD IP for this assignment.
3. Code must be in **Verilog- Structural Modelling**.

Q1.) Design a 16-bit Dadda Multiplier. For testing the multiplier, you will be using BRAM, VIO, ILA and Control unit (which can read the data from BRAM and send it to your multiplier module).

Task-1 - Design a **16-bit unsigned Dadda Multiplier using half adders and full adders, i.e. it takes two unsigned 16-bit numbers as input and the output should be unsigned 32-bit**. Write a testbench and simulate the circuit.

You will design a multiplier module using 2 methods:

(a) Using Dadda Multiplier

(b) Using * operator only.

Also report the Resource Utilization for the above cases.

Note: You need to generate the partial products properly. Use half-adders and full-adders wherever required. The Last stage of Dadda multiplier will utilize the 32-bit Brent-Kung adder from Assignment-1.

Task-2 -As done in Assignment-1, design a controller which takes 1 signal from the VIO: A start/stop signal which can continuously read the data from BRAM and send it to the Multiplier.
For TASK2, you will be generating a bit stream file which will be tested on PYNQ board (keep the bitstream ready before your evaluation).

Task-3 – Upload a .zip file containing: Report (should contain all the results) and Xilinx project folder. (Kindly do not save waveform while running the simulation). If your file size exceeds 10 MB, upload three separate files- report, zip folder with .srcs and the .bit file.

Q2.) Design a 8-bit Logarithmic Barrel shifter, for performing Right and Left Shift (Logical) operation.
(Structural style modelling of Verilog for Mux)

Note: *Bit i of the shift amount represents no shift (if it is 0) and a constant shift by 2^i places (if it is 1). Two way multiplexer's will be utilized, which will be controlled by bit i of the shift amount.*
(Read the Theory document uploaded on Moodle for more details.)

Task-1 - Design a **8-bit Logical Left and Right Shifter using Logarithmic Barrel Shifter.** Write a testbench and simulate the circuit.

You will design a Shifter module using 2 methods:

(a) Using Logarithmic Barrel shifter

(b) Using >> and << operator.

Also report the Resource Utilization for the above cases.

Task-2 – For testing the module, you will be using BRAM, VIO, ILA and Control unit (which can read the data as well as the shift/rotate amount from the BRAM and send it to your Barrel shifter module).
For TASK2, you will be generating a bit stream file which will be tested on PYNQ board.

Task-3 – Upload a .zip file containing: Report (should contain all the results) and Xilinx project folder. (Kindly do not save waveform while running the simulation). If your file size exceeds 10 MB, upload three separate files- report, zip folder with .srcs and the .bit file