Friday JAN 10, 2025	EE 705: VLSI DESIGN LAB 2025 ASSIGNMENT-1	Due On JAN 17, 2025

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. You can use VIO, ILA, BRAM, CLK WIZARD IP for this assignment.

Q1.) Design a 32-bit Brent-Kung adder. For testing the adder, you will be using BRAM, VIO, ILA and Control unit (which can read the data from BRAM and send it to your ADDER module).

Task-1 - Design a 32-bit Adder/Subtractor and write a testbench and simulate the circuit.

You will design Adder/Subtractor module using 2 methods:

(a) Using Brent-Kung adder

(b) Using + operator only.

Also report the Resource Utilization for the above cases.

Task-2 - Design a controller which takes 2 signals from VIO: (a) A start/stop signal which can continuously read the data from BRAM and send it to the Adder (b) A signal to select addition or subtraction operation to be performed. BRAM will provide the inputs to your Adder as shown in the figure given below.

Create a testbench to test the controller with BRAM.

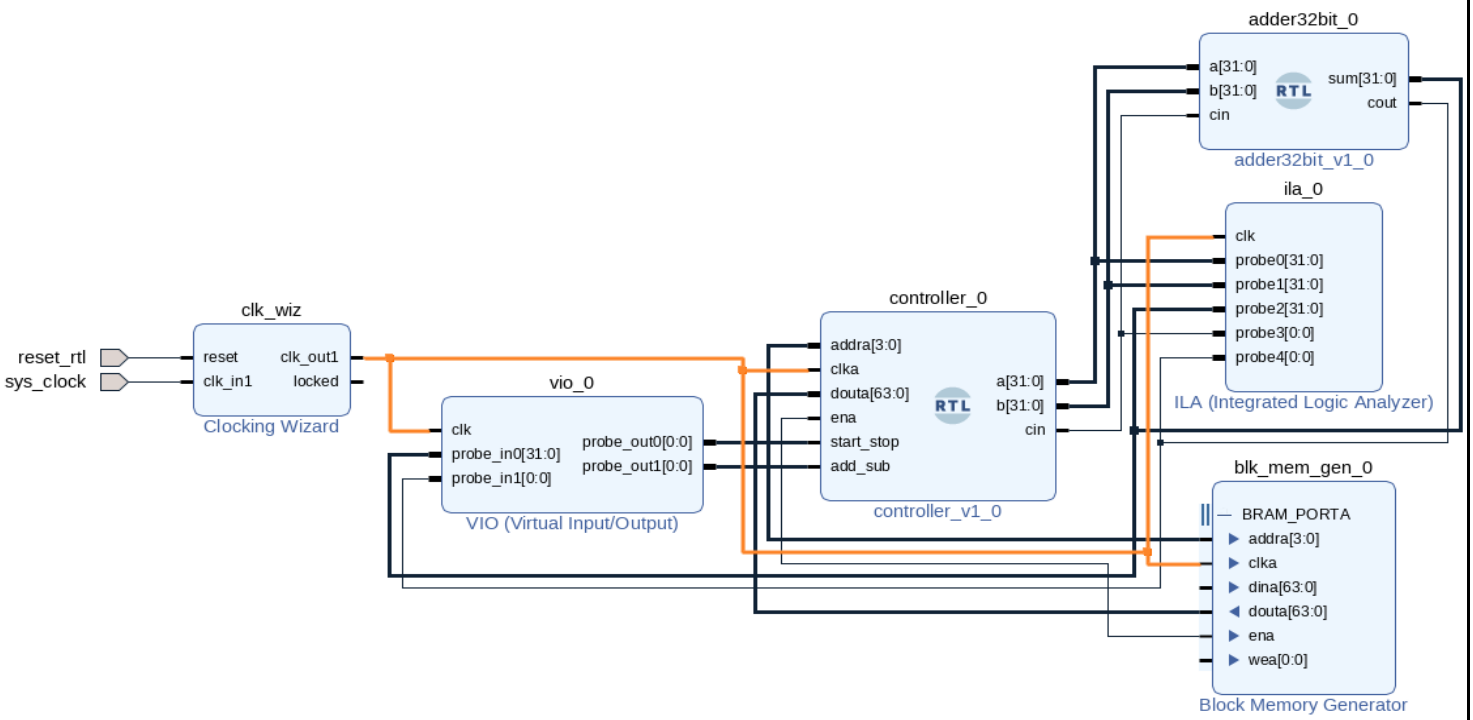

Figure 1

NOTE: You will have to generate BRAM using block memory generator. You have to select **Mode – Stand Alone** under basic tab. Write and Read width- 64-bit input (32 bits for **a** and 32 bits for **b**) and write and read depth is 16. You have to initialize the memory using .coe file.

addra-> address
clka-> clock
douta -> data out
ena -> enable

For TASK2, you will be generating a bit stream file which will be tested on PYNQ board.

Task-3 – Upload a .zip file containing: Report (should contain all the results) and Xilinx project folder. (Kindly do not save waveform while running the simulation)