Tuesday
JAN 28, 2025

EE 705: VLSI DESIGN LAB 2025
ASSIGNMENT-3

Report Due On
FEB 7, 2025

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. Code must be in **Verilog**
3. Deadline: **PART A will be evaluated on 4th Feb 2025 and PART B will be evaluated on 7th Feb 2025**
4. Report must contain verilog codes and test benches along with the necessary waveforms (outputs and state diagrams)

PART-A

Q1) In this question, we will interface a BRAM with a *Xilinx* AXI BRAM Controller IP to create an AXI-BRAM. Create a testbench (Master) that mimics an AXI-4 lite interface to perform a single transaction on the AXI-BRAM (Slave). The testbench (Master) should generate suitable AXI-4 lite signals to perform following operations:
(a) Write to the memory (single address)
(b) Read back from the same address

[Hint: Mode-BRAM Controller]
You need to show the test bench simulation results to the TA
NOTE: DO NOT USE ANY .COE FILE FOR Q1

Q2) The same AXI-BRAM from Q1 will be initialized with a .coe file in this question. You will create a new module/design that will interface with the AXI-BRAM to read all data from the initialized BRAM (all AXI compatible signals will be generated by this module). The testbench should only consist of a Clock, Reset and a data out port (which will display the read data). **[Hint: BRAM Standalone]**

PART-B

Q3) In this question, you will interface the BRAM with the Dadda Multiplier using AXI-4 Lite. To do this,
(a) Use the AXI-BRAM from Q1. This BRAM will be divided into two halves. The first half will store 32 bits of data that represent concatenation of two numbers 'A' and 'B' (16-bits each) for the Dadda Multiplier. The second half of the BRAM will be used to store the output of multiplication. Initialize the BRAM with a .coe file (initialize the results section of the BRAM with all zeros).
(b) Use the module in Q2 and incorporate the Dadda Multiplier within this module to get data from the AXI-BRAM (and pass it as input to the multiplier) and store the output of the multiplier back in the AXI-BRAM. The result of the multiplication and all the write AXI signals will also be shown using ILA. Generate the bit file for demonstration on FPGA.
NOTE: DO NOT USE ANY Testbench FOR Q3.
[Hint: BRAM Standalone]