Table 1: Mixer Performance Summary Table

	Design Metric	Performance	Specification
Conversion Gain	Minimum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	20.81dB	>$15dB$
	Maximum Peak Gain in the specified band [$f_{RF} = f_{LO}$]	21.61dB	>$15dB$
	Peak Gain flatness in specified band [Max-Min Peak Gain]	0.8dB	
	$3dB$ RF Bandwidth [From the plot of $f_{RF} = f_{LO}$]	400meg	
	Minimum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	18.64dB	>$15dB$
	Maximum Band-Edge Gain in the specified band [$f_{RF} = f_{LO} + 10MHz$]	19.39dB	>$15dB$
Noise Figure	Avg. SSB Noise Figure for $f_{LO} = 1.9GHz$	8.4dB	<$13dB$
	Avg SSB Noise Figure for $f_{LO} = 2.0GHz$	7.01dB	<$13dB$
	Avg. SSB Noise Figure for $f_{LO} = 2.1GHz$	9.08dB	<$13dB$
Linearity – IIP_2	Input power used for extrapolation	-49.11dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-46.83dBm	-
	Power of IM_2 Tone at output (at chosen input power)	-118.359dBm	-
	Extrapolated IIP_2	22.53dBm	$> 40dBm$
Linearity – IIP_3	Input power used for extrapolation	-35.108dBm	-
	Power of Fundamental Tone at output (at chosen input power)	-27.69dBm	-
	Power of IM_3 Tone at output (at chosen input power)	-102.986dBm	-
	Extrapolated IIP_3	2.5dBm	$> -10dBm$
Power	Mixer DC power consumption [Excluding Bias]	2.84mW(only I-phase)	
	Bias circuit power consumption	2.30mW(onl -y I phase)	Minimize
Other	Sum of all resistances [excluding bias]	0	-
	Sum of biasing resistances	621.05K (I-phase)	-
	Sum of all capacitances [Including AC coupling]	3uF (I-phase)	-
	Sum of all inductances	14nH(I-phase)	
	Load chosen	0.3pF diff. (only I-phase)	-
	Differential Mixer Input Capacitance	0.11pF	-
	Simulator Used	Eldo	-

Table 2: LNA + Mixer Performance Summary Table

	Design Metric	LNA	Mixer	Cascade	
				Expected	Simulated
Conversion Gain	$f_{IN} = f_{LO}, f_{LO} = 1.9GHz$	30.21dB	21.6dB	44.7dB	42.37dB
	$f_{IN} = f_{LO} + 10MHz, f_{LO} = 2.0GHz$	32.04dB	19.02dB	43.96dB	40.059dB
	$f_{IN} = f_{LO}, f_{LO} = 2.1GHz$	29.11dB	20.81dB	42.82dB	40.5dB
	$f_{IN} = f_{LO} + 10MHz, f_{LO} = 1.9GHz$	30.4dB	19.39dB	42.69dB	40.46dB
	$f_{IN} = f_{LO}, f_{LO} = 2.0GHz$	32.34dB	21.2dB	46.44dB	41.95dB
	$f_{IN} = f_{LO} + 10MHz, f_{LO} = 2.1GHz$	28.8dB	18.64dB	40.34dB	38.58dB
Noise Figure (avg)	$f_{LO} = 1.9GHz$	1.173dB	8.4dB	1.35dB	4dB
	$f_{LO} = 2.0GHz$	1.17dB	7.01dB	1.31dB	3.2dB
	$f_{LO} = 2.1GHz$	1.174dB	9.08dB	1.33dB	4.2dB
Linearity – IIP3	Input power used for extrapolation				-50.1727dBm
	Power of Fundamental Tone at output (at chosen input power)				-40.048dBm
	Power of IM_3 Tone at output (at chosen input power)				-100.97dBm
	Extrapolated IIP_3				-19.719dBm
Power	Total power consumption [Excluding Bias]				9.77mW
	Bias circuit power consumption				4.61mW

MIXER Project

Roll No. : EE18B155
Name : Balasubramaniam M C

April 18th 2021

Introduction

This project is about designing a Gilbert cell doubly balanced direct down-conversion mixer close to given parameters of conversion gain, IIP2, IIP3 and noise figure as much as possible. A differential input to differential output mixer with In-phase and quadrature components is designed.

CIRCUIT SCHEMATIC:

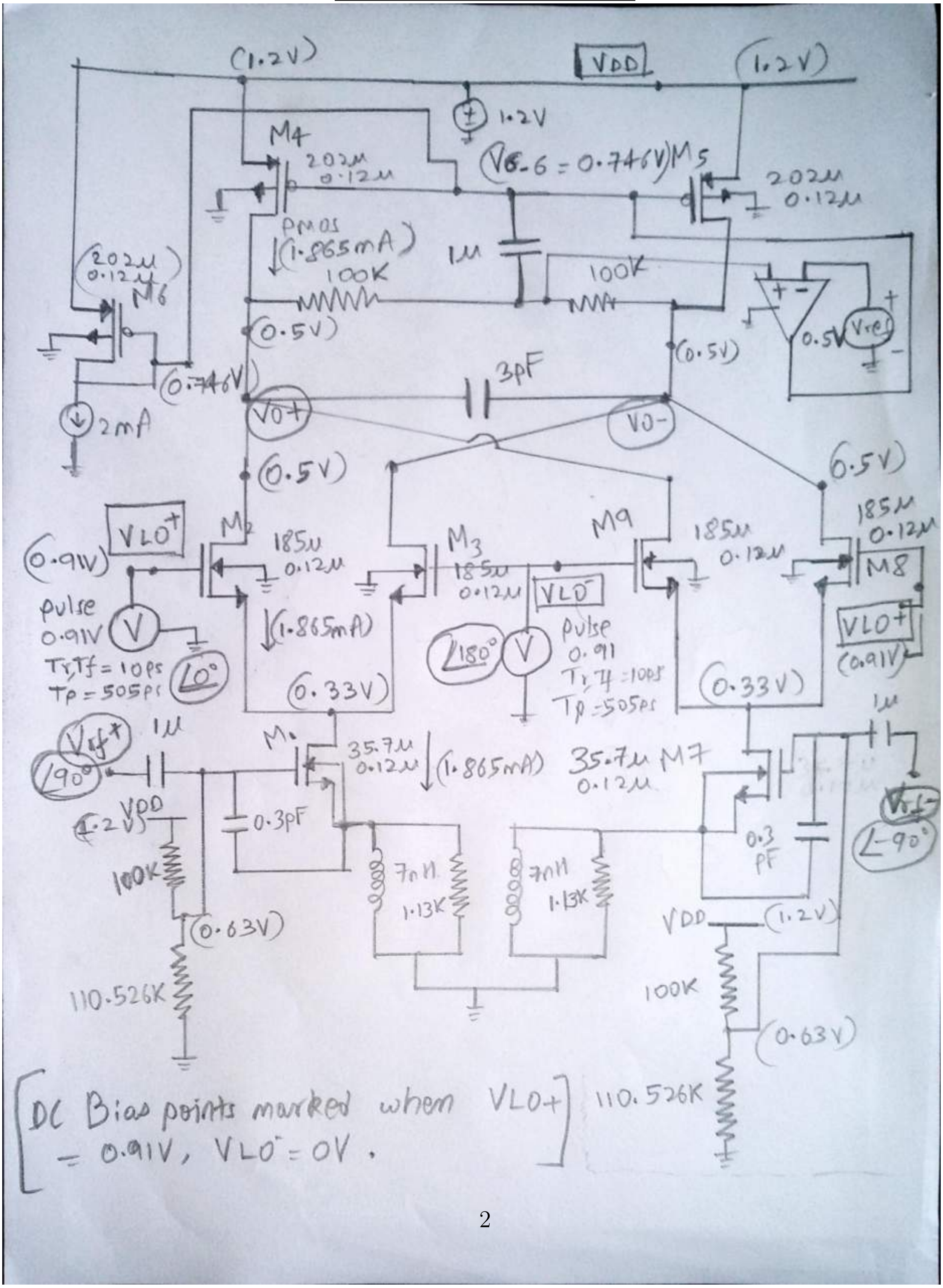


Figure 1: Circuit schematic of the fully differential direct downconversion mixer (In-phase part). The quadrature component will be exactly the same except that the phases of VLO+, VLO- will now be +90 and -90 degrees.

Mixer Performance:

Conversion Gain:

Starting with the first parameter on conversion gain with a minimum required gain of 15dB, we use an active load here based on a rough calculation that given this minimum conversion gain, if we were to use a resistor for typical values of gm1 (transconductor's gm usually in mS), the resistor value required would be close to kohms, hence giving a headroom issue. The common mode drain voltage of the PMOS active load, its currents and the gate voltage was tuned in such a way as to support the same current I-tail(in M1) as well as to get a gds of around 326uS. Another challenge faced was to tune the M1 width in such a way as to pass low enough current for good IIP2 as well as get a high conversion gain. We make sure the width of M1 is small enough with a low gate bias of 0.63V so that we get a gm of just 19.4mS which is good to go along with the rds of around 3Kohms. Since IIP2 mainly is very sensitive to any change in the circuit, any upgrade in the IIP2 simulation part was step by step verified to give a good conversion gain as well. The conversion gain and bandwidth calculations are in the appendix accounting for the inductively degenerated transconductor.
The peak Conversion gain is about 21.3dB as shown in fig.2 .
Conversion gain graphs for flo from 1.9G to 2.1G along with peak value, 10meg value and 3dB BW can be seen from figs. 13-17.

Linearity:

Linearity was the hardest spec to achieve of all mainly for IIP2. In order to get high IIP3, we use an inductively degenerated transconductor whose calculations based on input impedance and transfer function are shown in the appendix. It was observed that increasing the inductor value keeps reducing the pole frequency of the transfer function and hence, it cuts off more 3x harmonics or in other words giving better IIP3 which is why we use an inductor of 7nH. In order to maintain max cap requirement we use a low transconductor cap as well. We also used a fairly just high enough Vgs-VT of the transconductor. This mostly kept the IIP3 high enough throughout.
For IIP2, we did a couple of things. Firstly, we ensured that the VLO swing (0.91V on one side) was high enough (higher than $\sqrt{2}(Vgs-VT)$ (in common mode)) to give good fast switching and also increased the cascode widths so that the common mode overdrive voltage is low keeping in mind that the parasitics dont increase a lot. A higher VLO would have caused the slope of the LO waveform to increase and for the same reason we keep a 10ps Trise

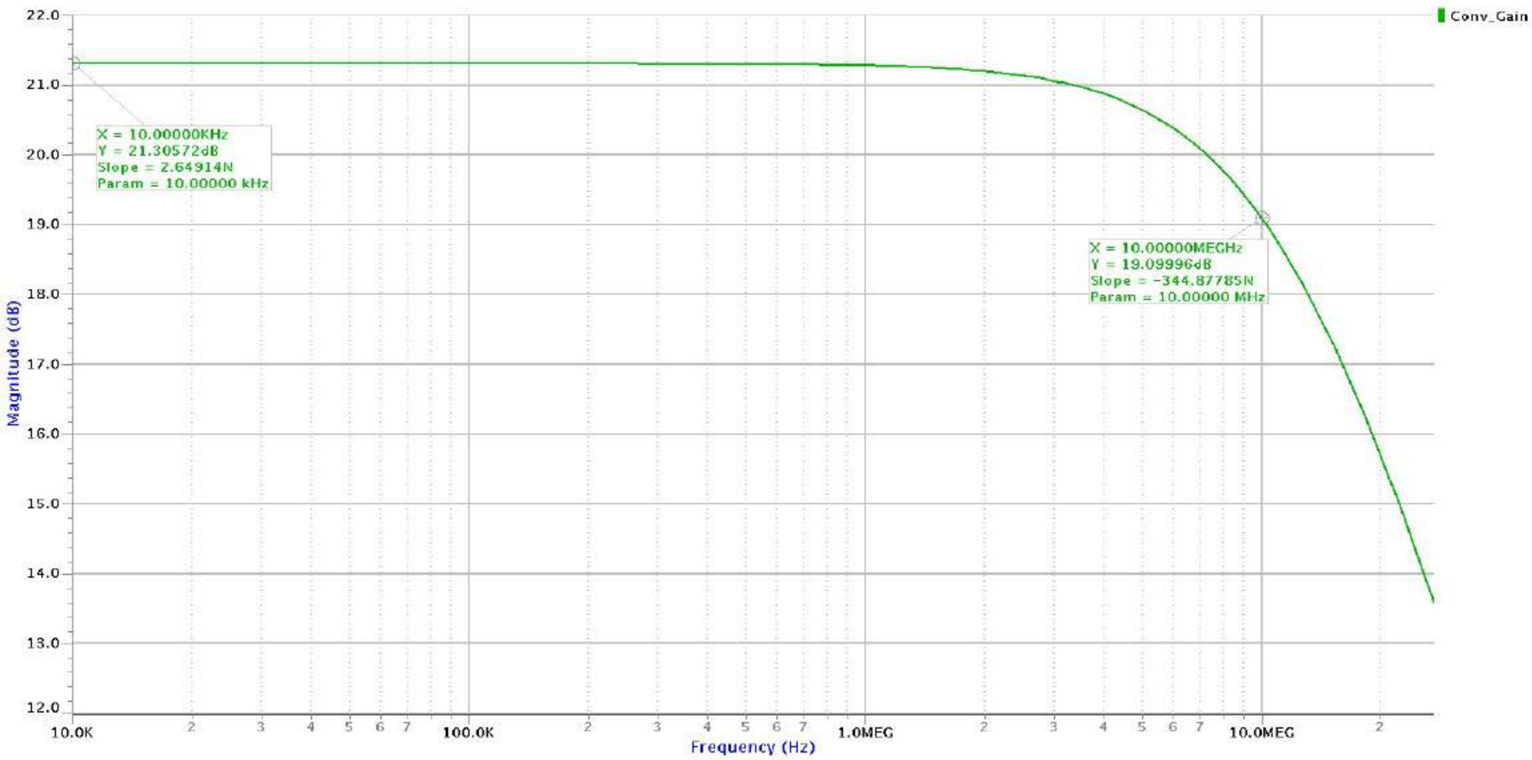


Figure 2: Differential Conversion gain for the I-phase component of the mixer flo = 1.98G.

and Tfall in order to keep the parasitics at drain of M1 low, we used a low width M1 as well. High VLO also means that the voltage at drain of M1 (at 2x frequencies) would increase.
We also keep the current to a low 1.8mA (= I-Tail) so that the current escaping into the parasitics of the drain node of M1 was low as well and even with low current due to active load we get a high IF output power.
The issue faced with IIP2 was that, since the parasitics also were functions of the voltage biases and changing the drain voltages of the cascode or transconductor totally changes the curve, we had to make sure they dont dominate by keeping small enough widths and change any parameter both ways, ie, increase or decrease and see the effect. Once it slowly started climbing, based on these changed parameters, we had to tune again and repeat the process until it went up to the given value. Additionally, we had to ensure the conversion gain didn't change, so at every step the conversion gain, the DC picture

was checked.
The hand calculations for overdrive voltage of cascode are also shown in the appendix.
50 harmonics for the square pulse (calculated from given Trise, Tfall = 10ps) at flo frequency, with 4-5 harmonics of the RF frequency were used to simulate for IIP2, IIP3.
The obtained IIP2 is about 22.5dB as shown in fig.3 with proof in fig.4.
The obtained IIP3 is about 2.5dB as shown in fig.5 with proof in fig.6.

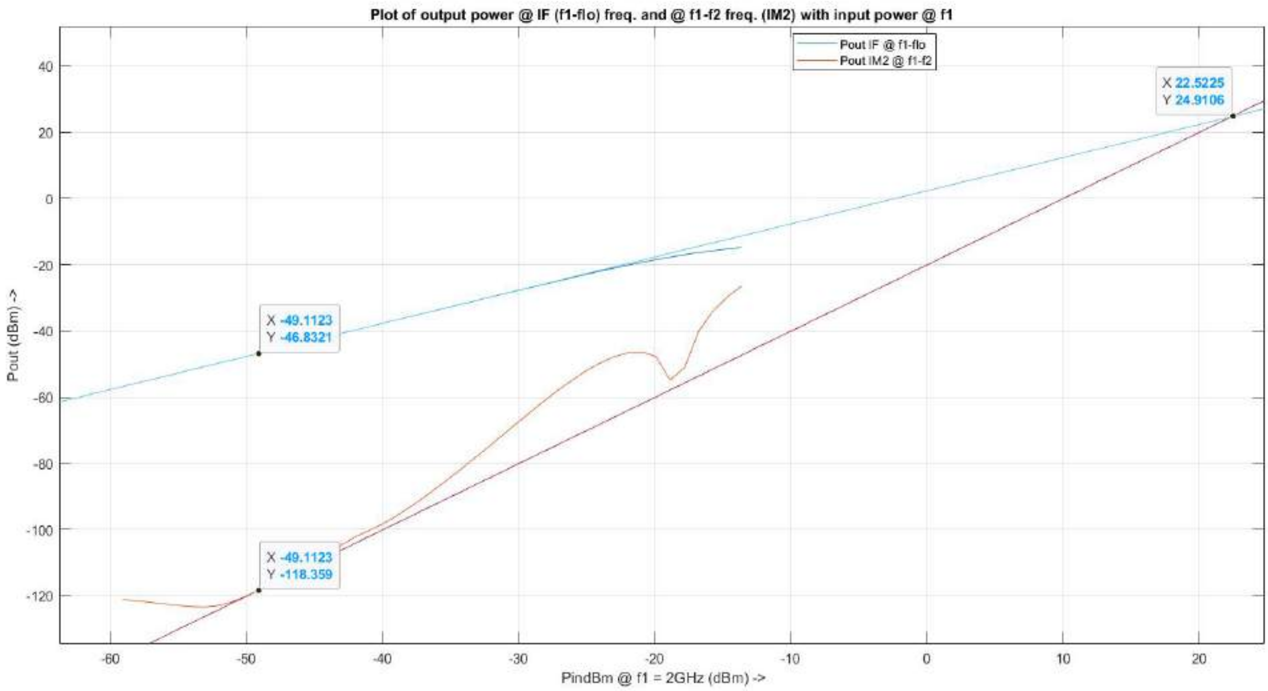


Figure 3: IIP2 Extrapolaion for mixer.

Noise Figure:

Finally, we didn't have much of a choice in tuning for noise figure once the parameters for IIP2, IIP3 and conversion gain were set, but we did use a low tail current for IIP2 which turned out to be helpful in reducing the total output noise. The VLO and (VGS-VT) (of transconductor) were high enough ensuring a noise figure lower than the given spec even with the high width,

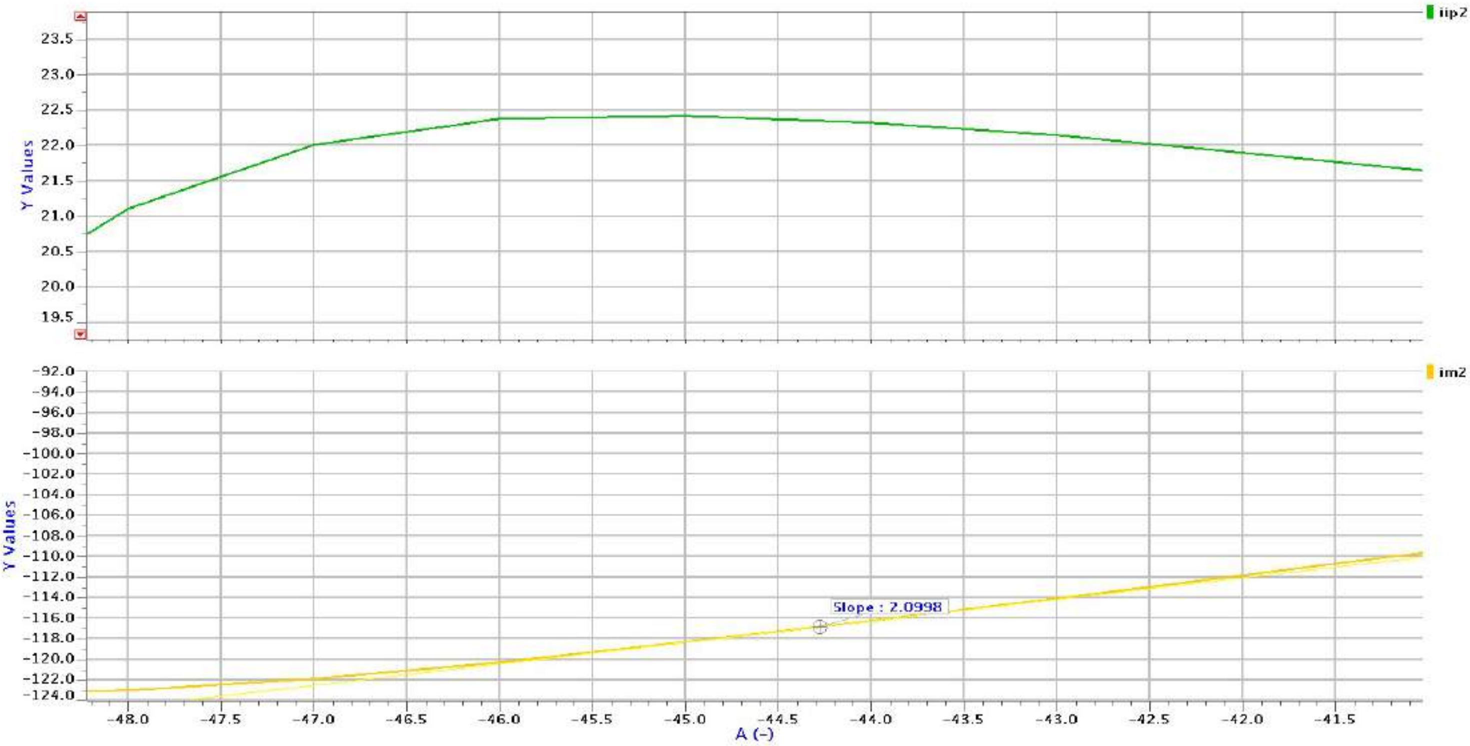


Figure 4: Plot of calculated IIP2 values and IM2 curve with 'A' (Pin in fourier source).We can see the slope of 2dB/dB and a fairly flat calculated IIP2 curve over the region of 'A' values.

gm PMOS active load.
The Single Side Band spot noise figure curve and the resulting integrated curve is as shown in fig. 7 resulting in a NF of 8.7 dB after averaging.

```
(Integrated NF)/10MHz = Avg NF
Hence avg. NF = 87.1855 Meg (dBHz)/10Meg (Hz) = 8.7
```

DC bias and power consumption:

The main issue with the DC picture in case of mixers was with headroom. Using a resistor we weren't getting enough gain and it was consuming headroom. So, with a PMOS active load we could get gain and headroom. We also used an ideal opamp under negative feedback (we can see the 180 deg

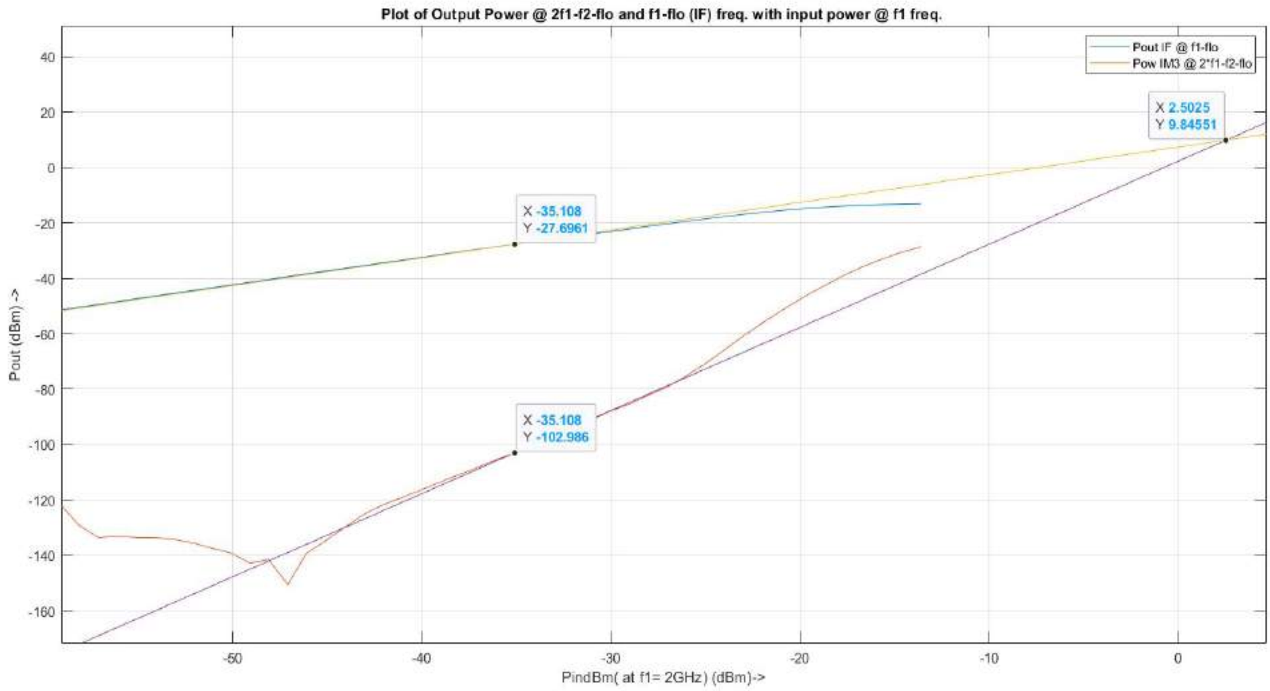


Figure 5: IIP3 Extrapolaion for mixer

phase shift offered by the PMOS which is why the node next to the 100K resistor is connected to +) to set the voltage there to be 0.5V giving sufficient headroom for swing at output , making sure the PMOS is in saturation and keeping the cascode just at the edge of saturation yielding an ideal situation. Another use of the opamp is that it sets the voltage to be exact 0.5V while with normal drain gate feedback with PMOS it was hard to set this voltage. Its an ideal opamp so technically we don't need miller compensation but we connect the cap to make sure of small signal common mode ground and for completing the loop in the incremental analysis picture with the opamp. To get enough gm we use both a low width as well as low VGS for the M1 mosfet. One issue faced was that often some mosfet or the other would go into triode or cutoff when tuning for other specifications. So, the only solution that was possible here was to tune to a fairly small range using educated guessing of what the voltages might be if its tuned in the given way and recheck the DC picture often to ensure everything is in saturation. Sometimes, we might have to change the widths by 100s of microns in which case to maintain the same current the ratio of widths of mosfets M2 and M1 were kept constant

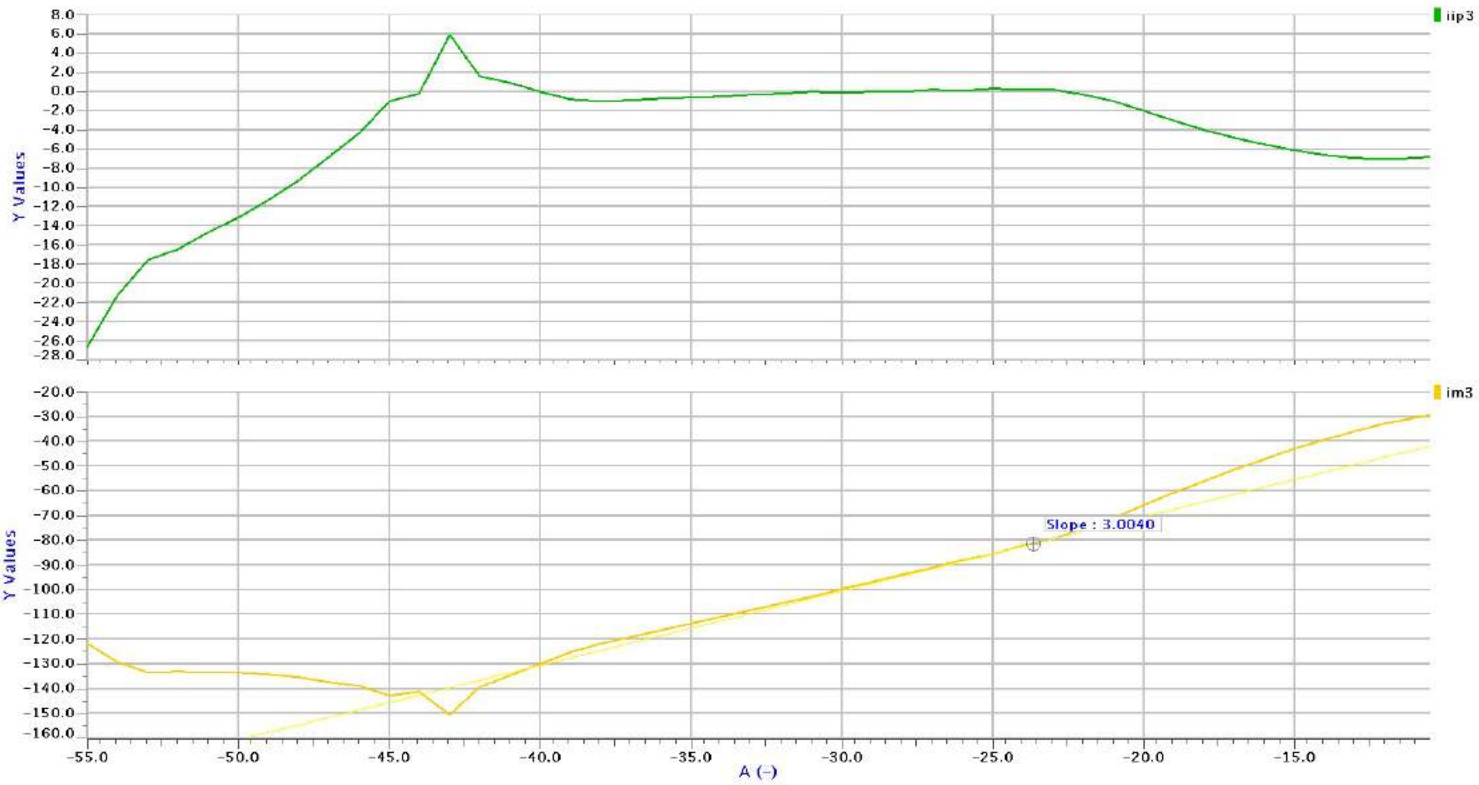


Figure 6: Plot of calculated IIP3 values and IM3 curve with 'A' (Pin in fourier source).We can see the slope of 3dB/dB and a fairly flat calculated IIP3 curve over the region of 'A' values.

and many other such calculative changes were done. The current through Current mirror and PMOS (or even M1) was kept close so that we avoid any current due to channel length modulation.
Regarding power consumption, We tried to keep a low enough current through M1 which is probably the only thing we can do. The power consumption is as shown in fig.8 The net power consumed was taken for one cycle(meaning only one half of the mixer is on) and ofcourse the same avg. power holds through all time.

```
Tot. Pow. for In-phase component of mixer:5.14mW
Tot. Pow. by biasing components for In-phase component of mixer:2.30mW
```

Bias calculations are in appendix.

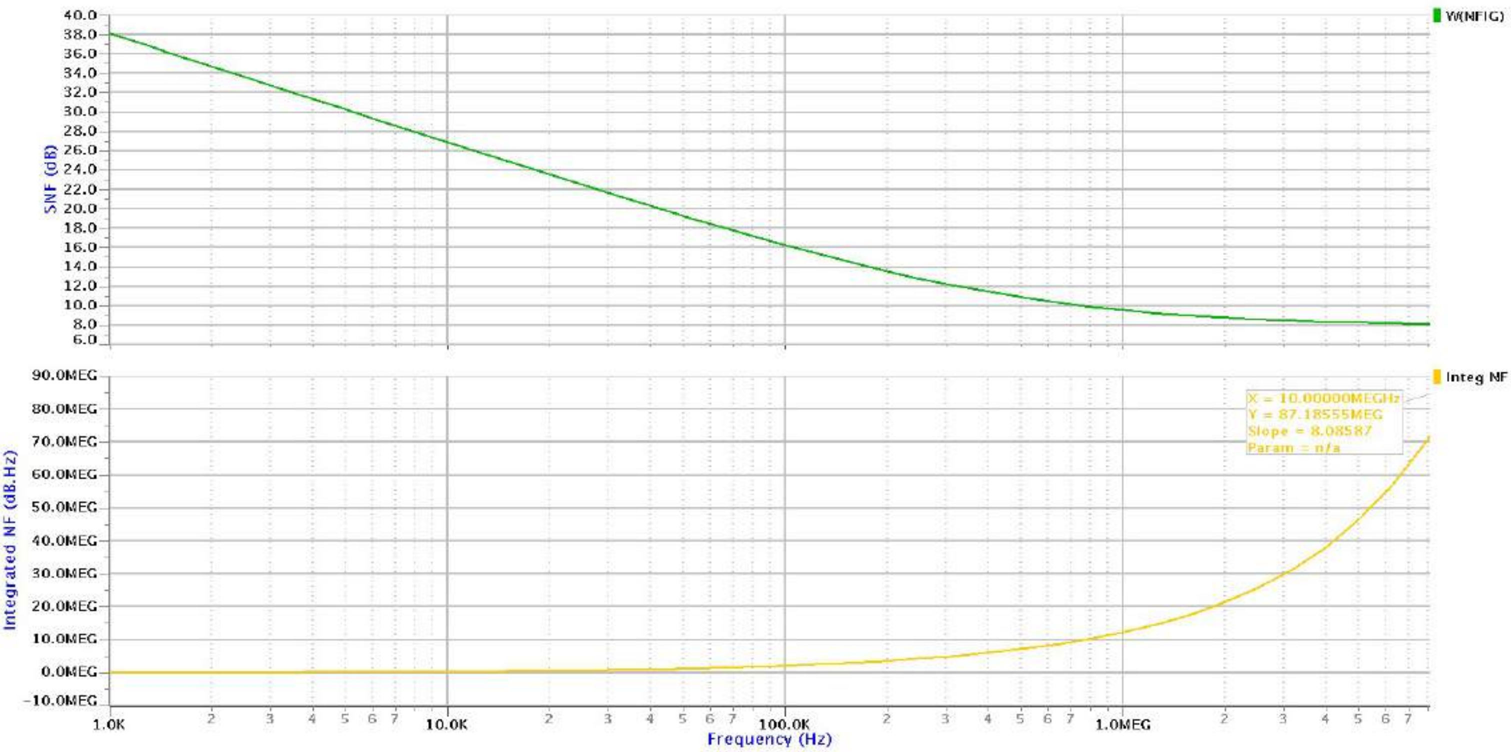


Figure 7: Spot noise figure over baseband and integrated Noise figure.

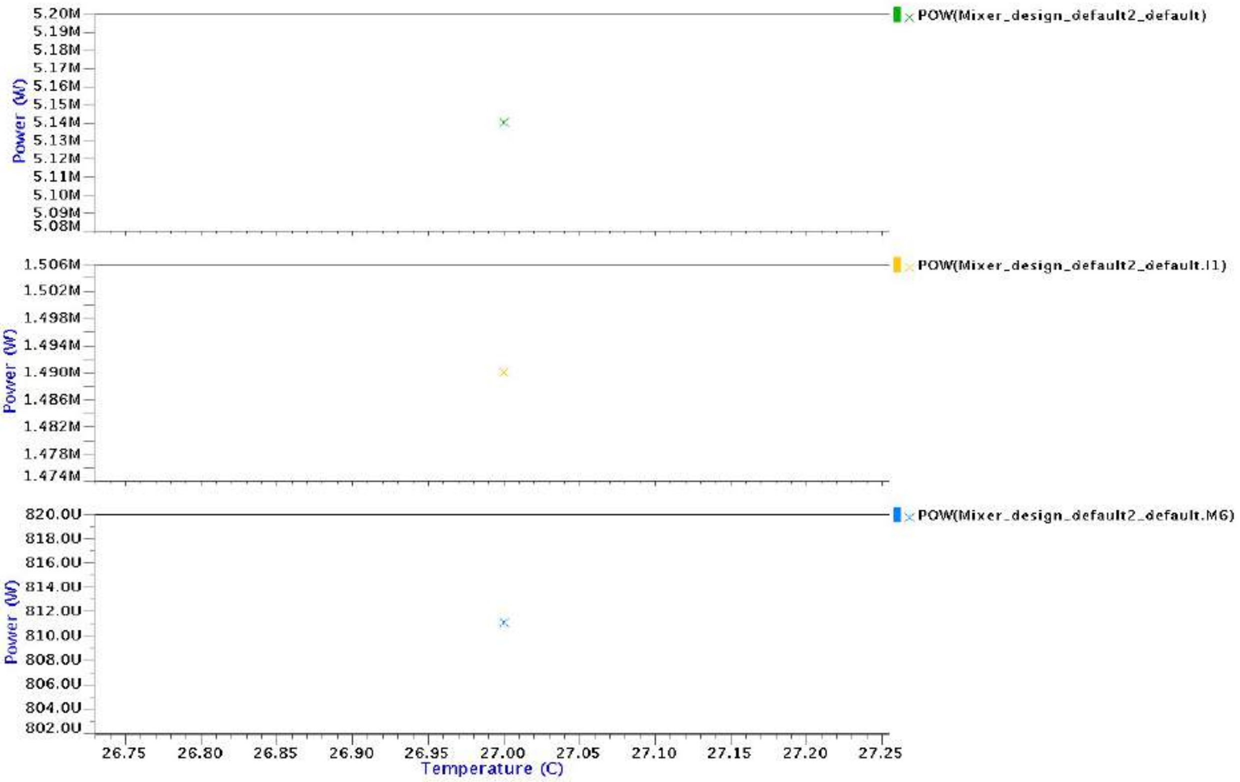


Figure 8: Total power consumption and power consumed by current source and mosfet of the current mirror (Other biasing components have negligible power consumption).

Mixer + LNA Performance:

Gain:

The overall gain of cascaded system is as shown in fig.9. We see that LNA effective gain drops due to the resistive part of the input impedance of the mixer. This can be verified in fig. 10.

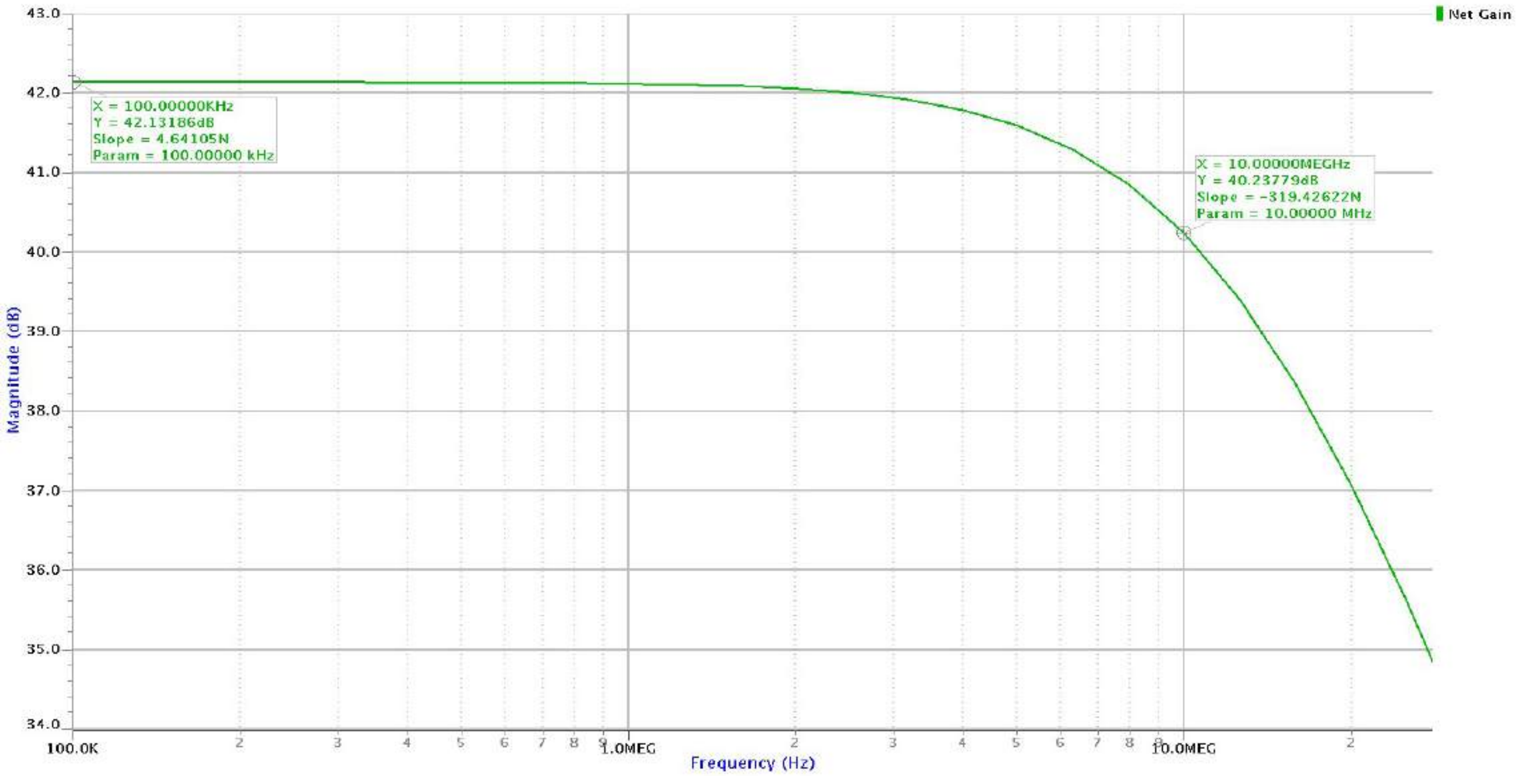


Figure 9: Net gain of the whole LNA + Mixer system.

The gain hand calculations are in the appendix. We see that this is greater than the total minimum spec of 35dB.

Noise Figure:

As seen in the handcalculations, we observe that the noise figure is actually more than what is estimated. This probably is probably because we have effectively reduced the Rout of the LNA causing a lower resistance and higher

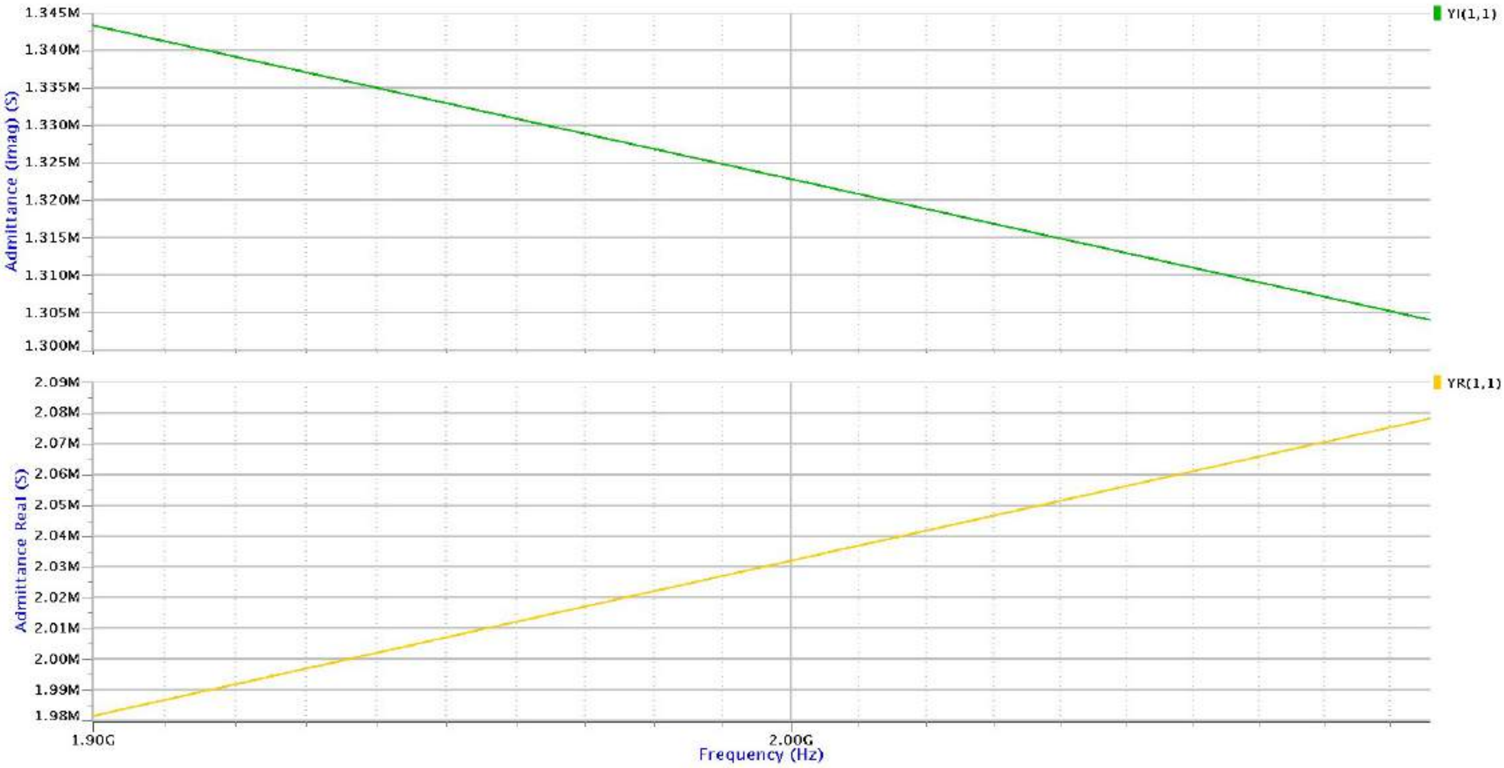


Figure 10: Input admittance as seen in one (+) port of the I-phase mixer. This turns out to give a differential cap of 0.11pF and a resistance of 490.2 ohms.

noise sent in to the mixer. The estimate calculated was using the noise figure of a standalone LNA. The net spot noise figure is as shown in fig. 11.

```
(Integrated NF)/10MHz = Avg NF
Hence avg. NF = 40.34387 Meg (dBHz)/10Meg (Hz) =  4.034
```

Net power consumption:

Net power consumption turned out to be: 9.77mW without bias. Net power consumption for biasing: 4.61mW

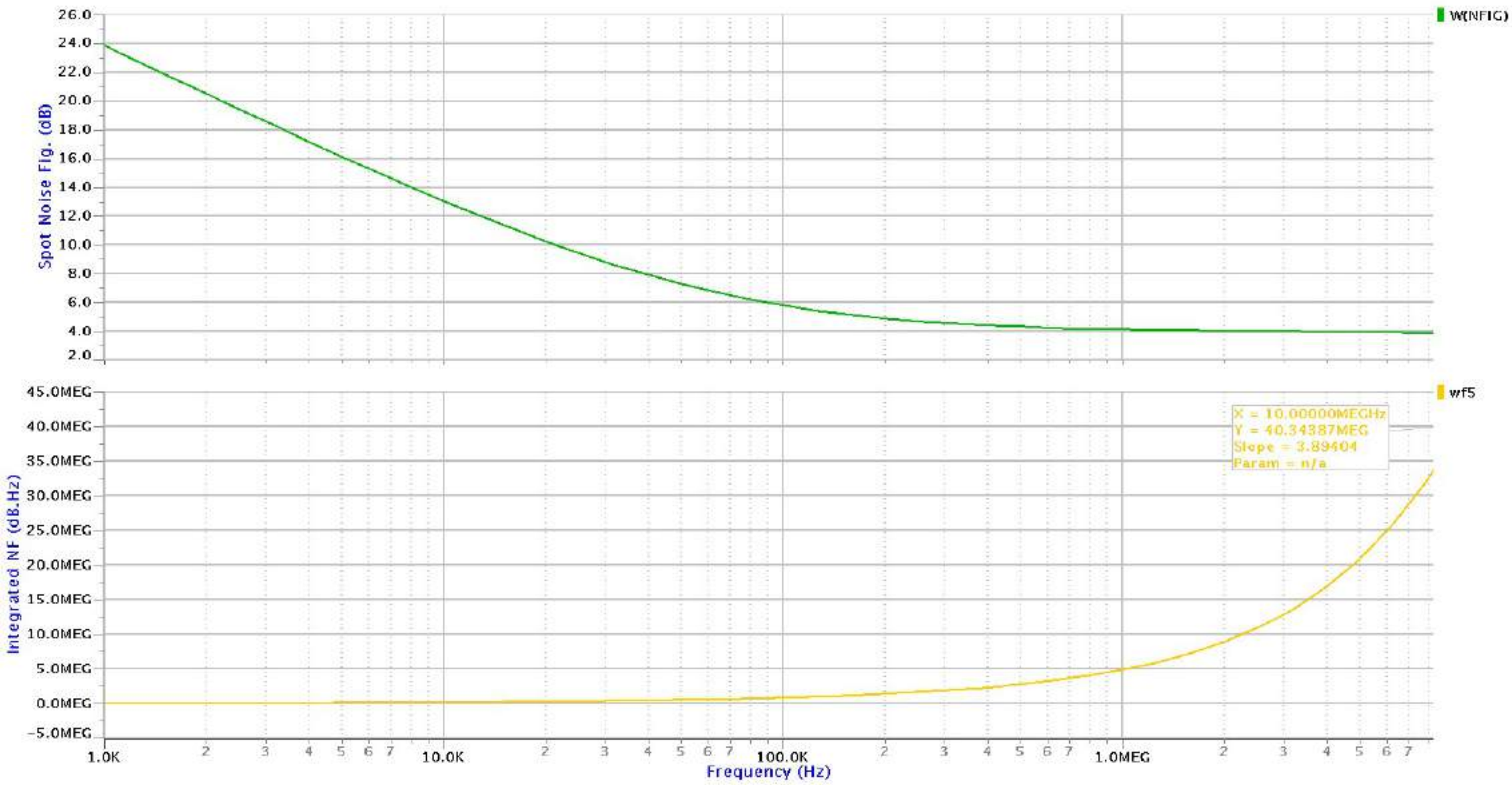


Figure 11: Net spot noise figure (dB) over the band and integrated noise figure(dBHz).

Linearity:

The total linearity however holds good with the net estimate as shown in the hand calculations. As shown in fig. 12 we see a net IIP3 of around -19.7197dBm.

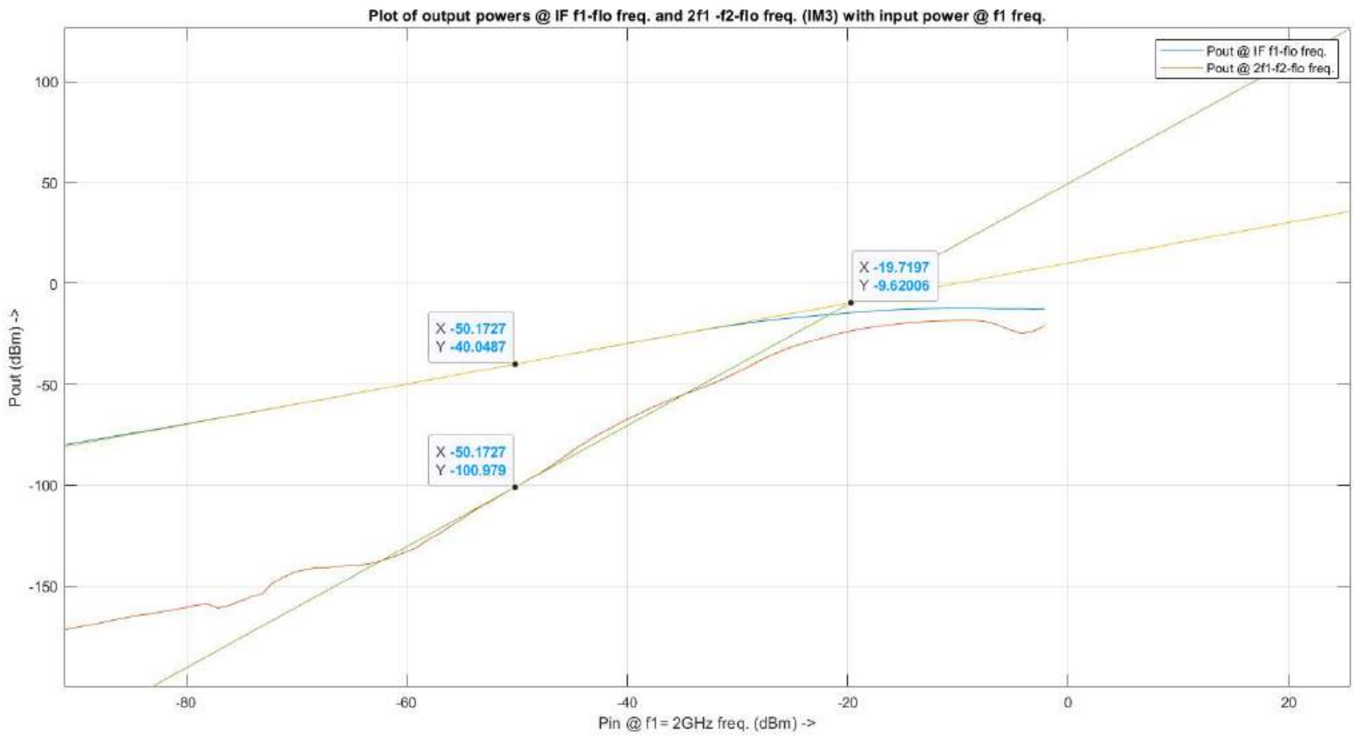


Figure 12: IIP3 Extrapolation for Mixer+LNA system

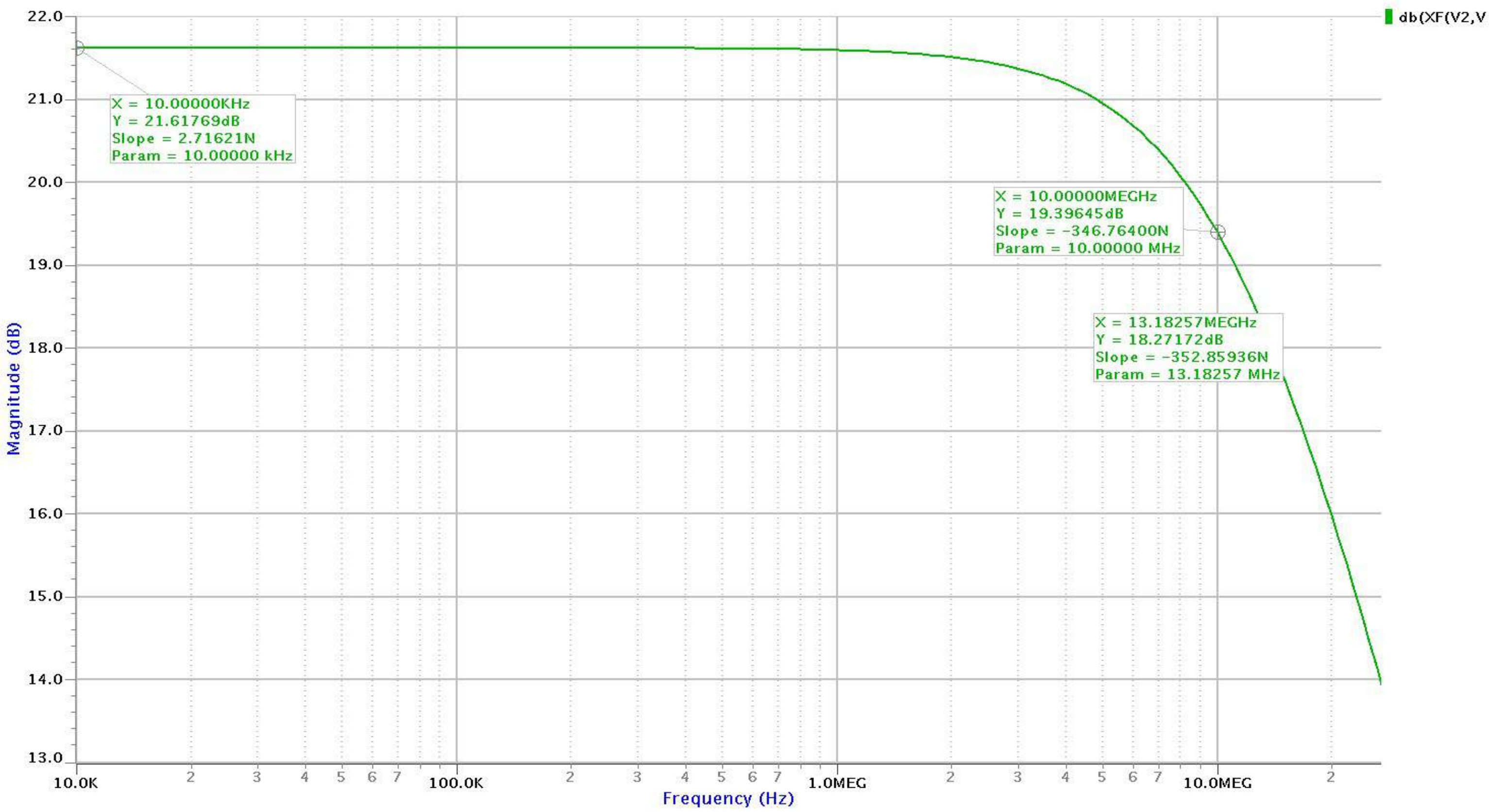


Figure 13: Differential Conversion gain for the I-phase component of the mixer flo = 1.9G.

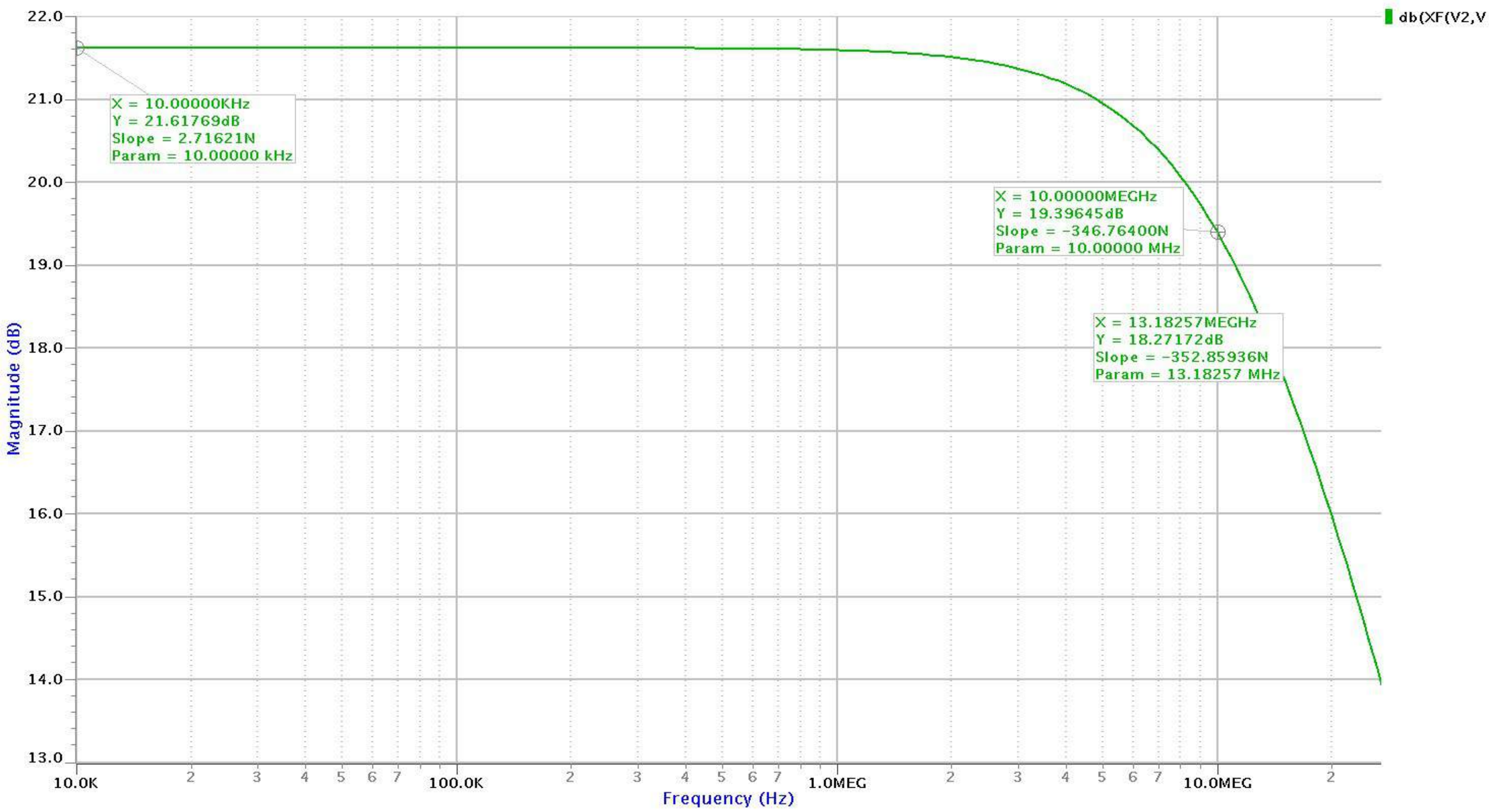


Figure 14: Differential Conversion gain for the I-phase component of the mixer flo = 1.9G.

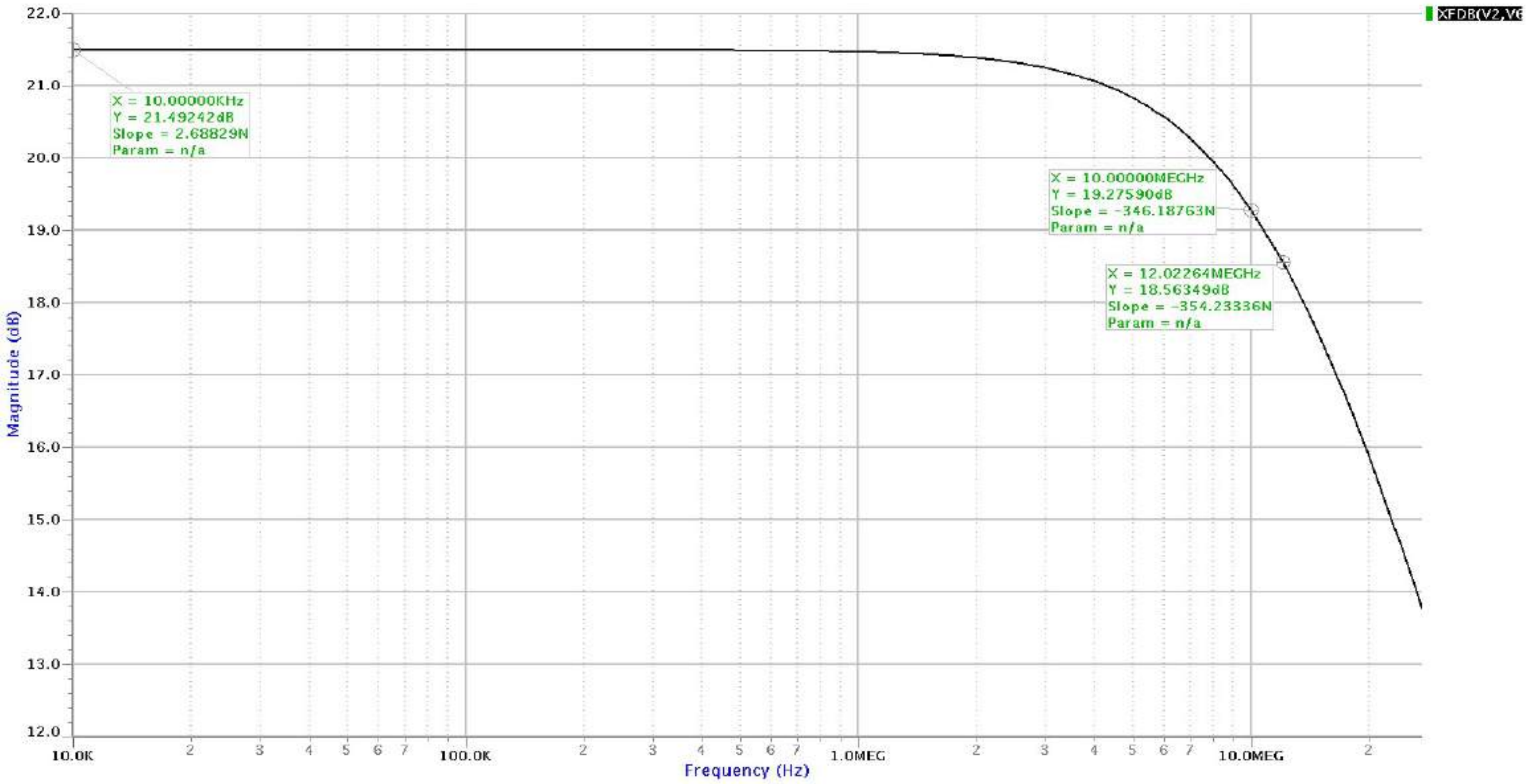


Figure 15: Differential Conversion gain for the I-phase component of the mixer flo = 1.933G.

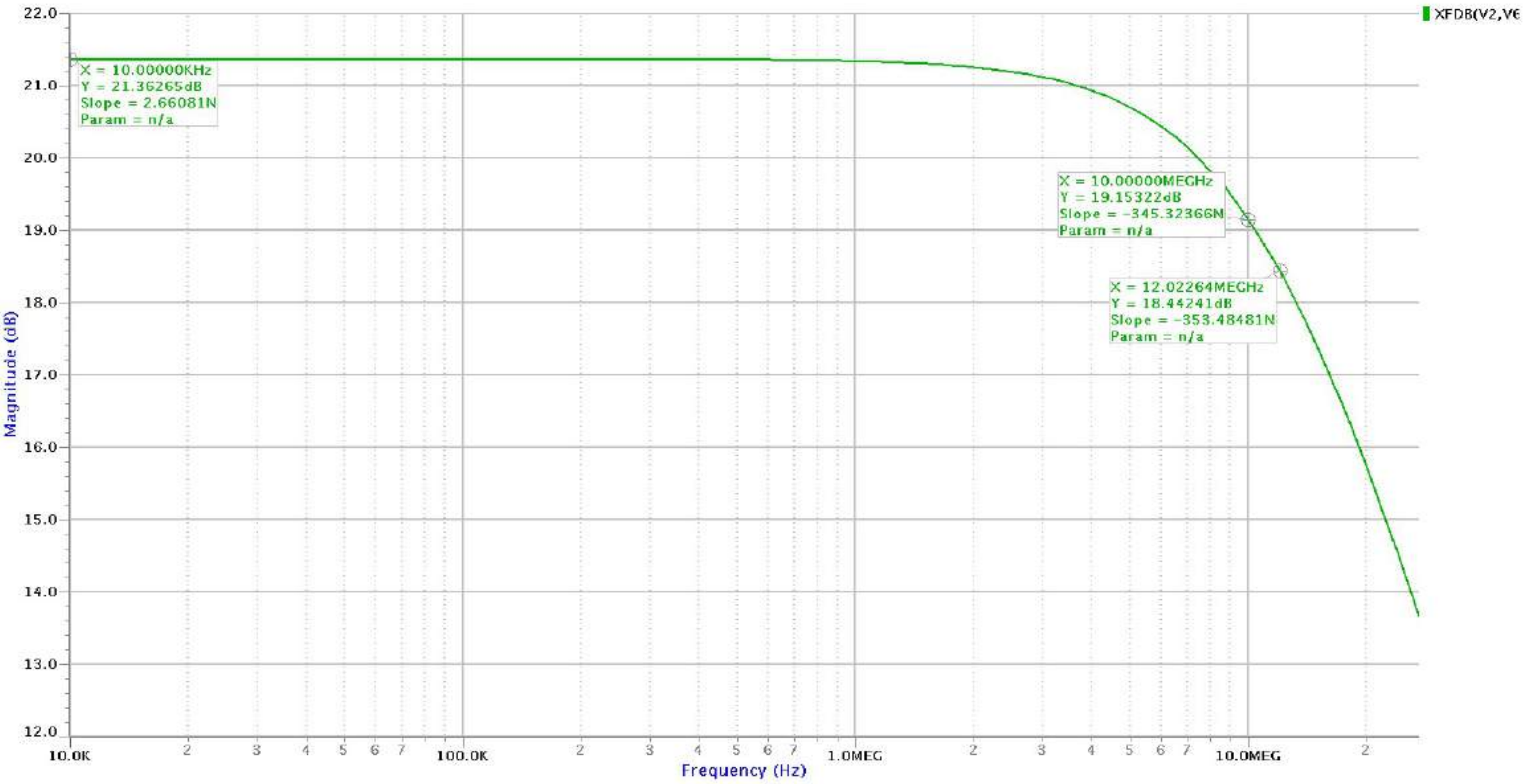


Figure 16: Differential Conversion gain for the I-phase component of the mixer flo = 1.966G.

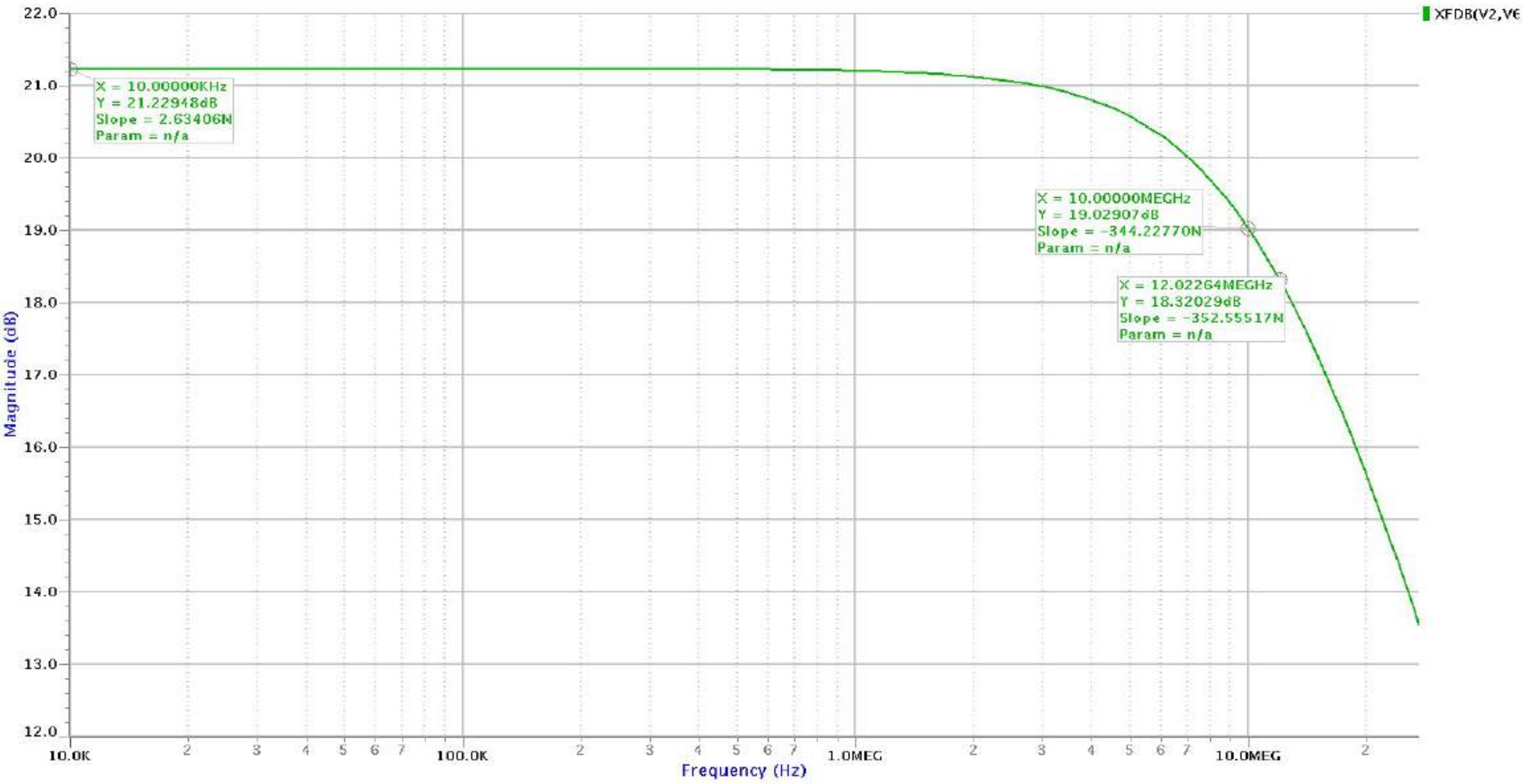


Figure 17: Differential Conversion gain for the I-phase component of the mixer flo = 1.999G.

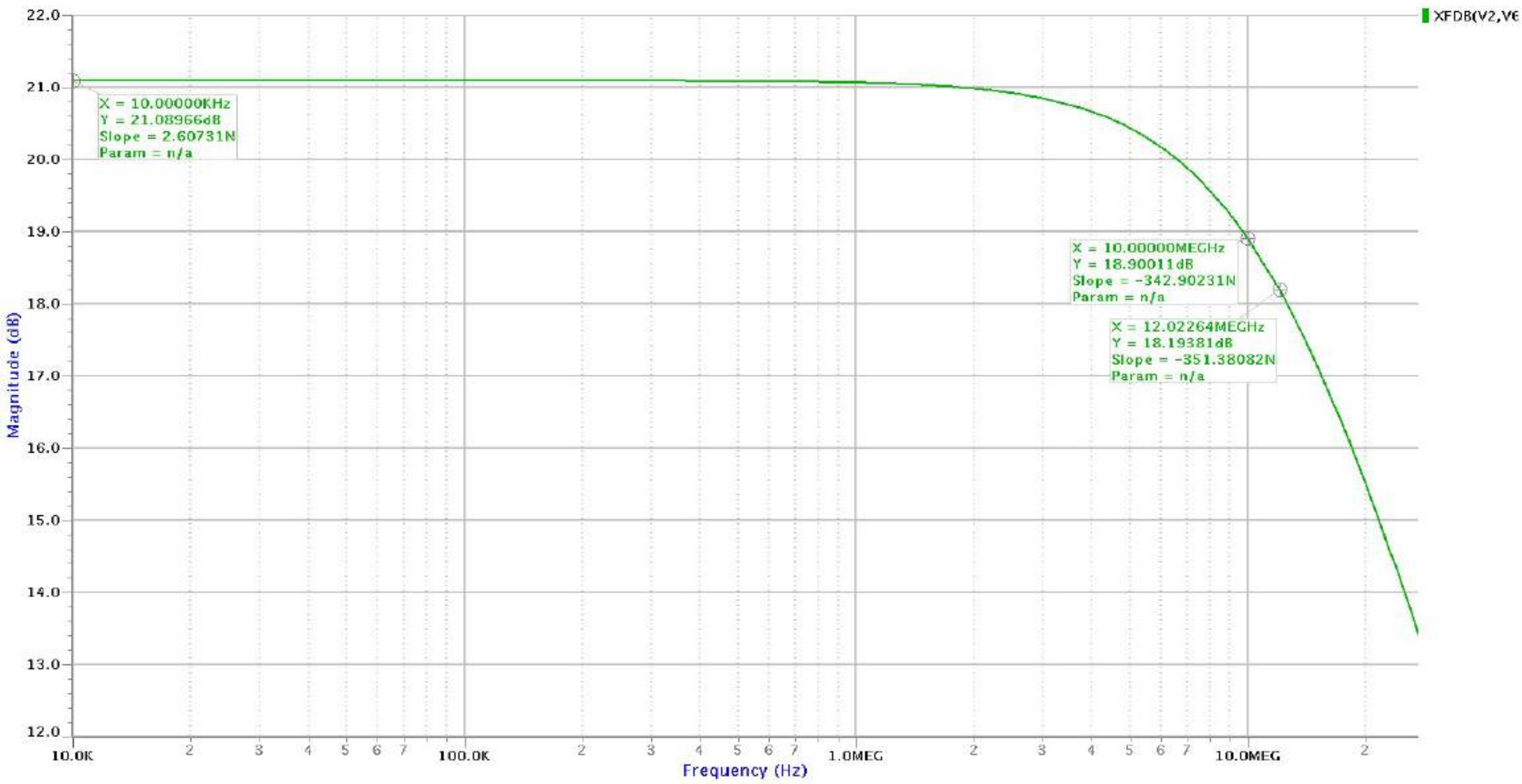


Figure 18: Differential Conversion gain for the I-phase component of the mixer flo = 2.033G.

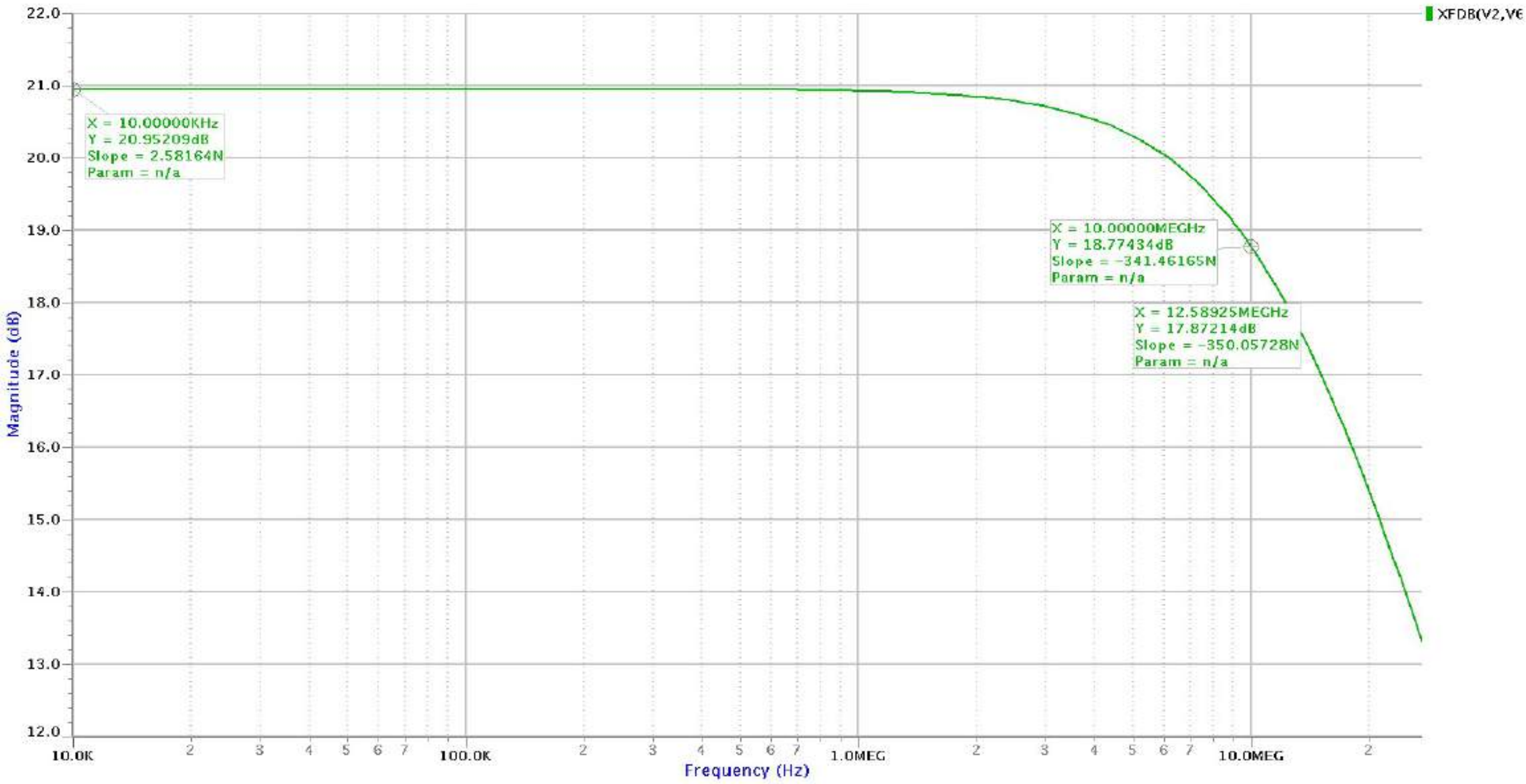


Figure 19: Differential Conversion gain for the I-phase component of the mixer flo = 2.066G.

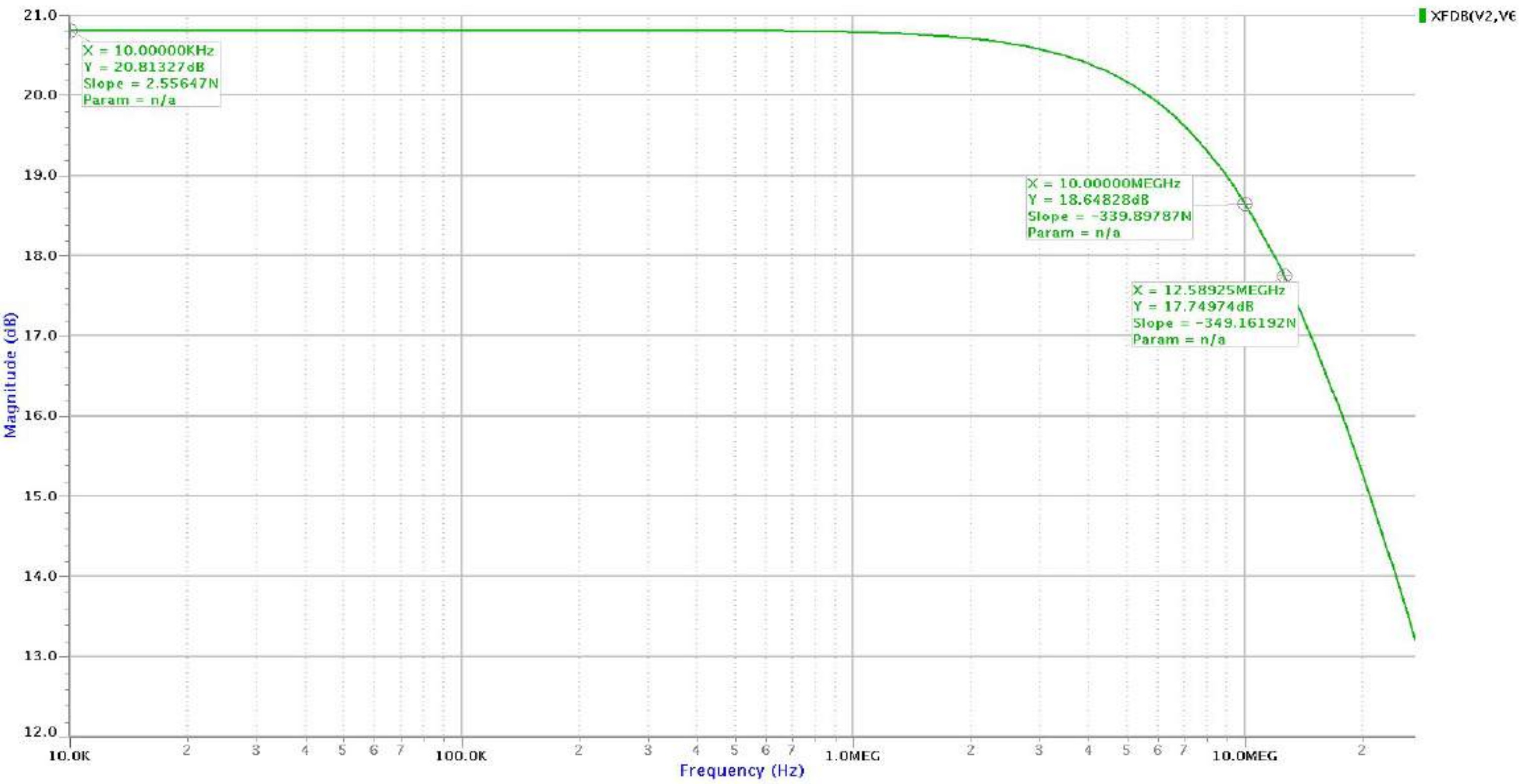


Figure 20: Differential Conversion gain for the I-phase component of the mixer flo = 2.099G.

Appendix

Hand Calculations

▷ Conversion gain.

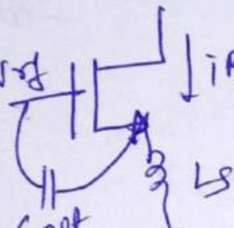
Conversion gain is given by (Diff - Diff i/p o/p) $= \frac{2}{\pi} g_{m1} R_L$

Here g_{m1} = gm of transconductor @ RF or approx 2GHz

R_L = r_{ds} active load.

gm of transconductor is given by

$$V_{RF}\, g_{meff} = \frac{g_m V_{RF}}{\left[s^2 L_s C_{gs} + 2 g_m L_s s + 1 \right]}$$



' C_{gs} ' here is actually Cnet

Cnet = 0.3pF

gm → gm of Mosfet M_1 = 19.372 mS

L_s = 7nH

$s = j 2\pi \times 2\times10^9$ rad/s

Plugging in values

$$|g_{meff}| = \frac{|(19.372\,mS)|}{|3.47 \angle 1.38\,rad|} = 5.583\,mS$$

As we can see gmeff is reduced, but this is done for good IIP2, IIP3 with high inductor. We have a high resistance active load anyway.

Active load

g_{ds} measured = 326.532 µS.

$\Rightarrow r_{ds} = 3062.49\ \Omega$

Assuming ideal cascode (cascode $g_m = 36.46\text{mS}$ fairly high)

$\therefore \frac{2}{\pi} g_{m\,eff}\, r_{ds}$ = Conv-gain (one side)

= Conv-gain (diff.) as well

$\therefore \frac{2}{\pi} \times 5.583\times10^{-3}\,S \times 3.06249\,K\Omega$

$= \underline{\underline{10.88}}$

$\therefore$ In dB $\rightarrow$ $20\log(10.885) = \boxed{20.74\,dB}$

voltage conv-gain

Assuming RF = 2GHz $\rightarrow$ Agrees with simul-ation

Bandwidth

R_{load} on one side = 3.062K

C_{load} (diff) = 3pF $\Rightarrow$ 6pF single side C_{load}

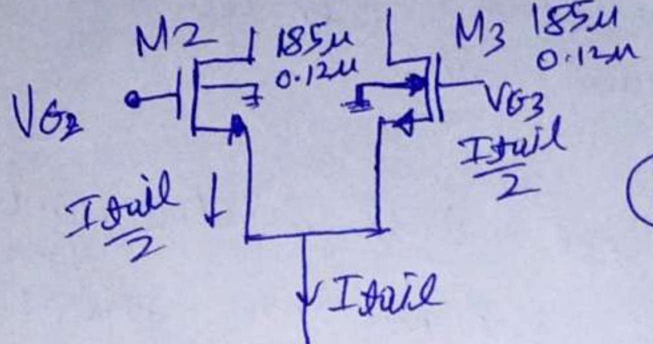
$\therefore RC = 3.062K \times 6pF = \frac{1}{\omega_{3dB\,out}}$

$f_{3dB} = \frac{1}{2\pi \times 3.06249K \times 6pF} = \boxed{8.66\,MHz}$

Close to simulation value

IIP2 - Voverdrive calc.

I_{Tail} measured = 1.865 mA.



In common mode

$$\frac{1}{2}(K_n)\frac{W}{L}\left(V_{GS_{2,3}}-V_T\right)^2 = \frac{I_{tail}}{2}$$

Eqn 1

$\underline{K_n \text{ estimation}}$, In our DC picture, only M_2 on M_3 off

gm_2 meas. = 36.4629 mS, V_{GS_2} meas = 0.577 mV.

$V_{TM2} = 0.471$ V.

$$\therefore K_n\left(\frac{W}{L}\right)\cdot\left(V_{GS_2}-V_T\right) = gm$$

$$K_{n_2} = 2.23\times10^{-4}.$$

From (1)

$$\frac{1}{2}\,2.23\times10^{-4}\left(\frac{185}{0.12}\right)\left(V_{GS}-V_T\right) = \frac{1.865\,\text{mA}}{2}$$

$$\therefore \sqrt{2}\left(V_{GS}-V_T\right)_{CM} = 104.116\,\text{mV}$$

$$\therefore V_{LO} >> \sqrt{2}\left(V_{GS}-V_T\right)_{CM}$$

$$0.91\text{V} > 0.1\text{V} \quad \text{satisfied.}$$

IIP3, IIP2 - Transconductor calc.

Transconductor transfer function is $\dfrac{gm}{\left(s^2 L_s C_{net} + 2gm L_s s + 1\right)}$

We want pole freq. $\dfrac{1}{\sqrt{L_s C_{net}}}$

to be very high so as to give constt. gm over all RF freq.

, but also not too high that it includes other harmonics.

So, ideally it shd. be $g_{meff} = g_m$ over the RF band. So, $(\omega^2 L_s C_{net})$, $(2 g_m L_s \omega) <<< 1$ is the ideal condⁿ.

Given chosen L_s, C_{net},

$\omega^2 L_s C_{net} = 0.33$ which is fairly lower than 1.

$2 g_m L_s \omega = 3.41$ however

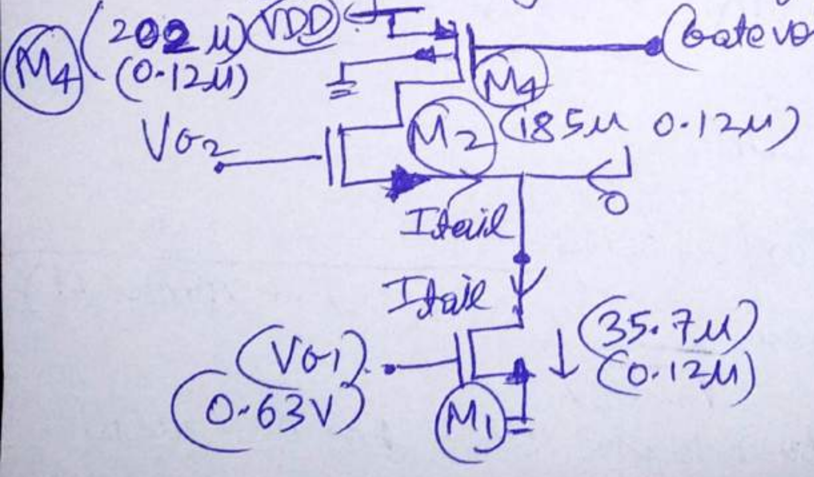
As we can see it obviously didn't give the same g_m across band, but this is done to remove extra harmonics

pole freq. $= \dfrac{1}{2\pi\sqrt{L_s C_{net}}} = 3.47\text{ GHz} > 2\text{ GHz}$

but still fairly low to cutoff higher ~~freq~~.

DC bias point calculations

During one cycle one half is on, other off



M4 PMOS active load

M2 - cascode

M1 - transconductor

$\underline{M_1}$:- I_{tail} measured = $\underline{1.865mA}$.

$V_{T1} = 0.422V$ V_{D_1} measured $= 0.33V > V_{G1} - \underline{V_{Tn}}$

$V_{G1} = 0.63V$

$$I = \frac{1}{2} K_n\left(\frac{W}{L}\right)(V_{GS_1} - V_{T1})^2$$

$\underline{K_n \text{ estimation}}$ - $\frac{g_{m_1}}{W/L(V_{GS_1} - V_T)} = \frac{19.372mS}{\frac{(35.7\mu)}{0.12\mu}(0.63-0.42)}$

$$K_n = 262.56\times10^{-6}$$

$$\therefore I = \frac{1}{2} 262.56\times10^{-6} \times \frac{35.7\mu}{0.12\mu}(0.63-0.422)^2$$

$= \underline{1.7mA}$ → close $\underline{\text{enough}}$.

$\underline{M_2}$:- $K_{n2} = 2.23\times10^{-4}$.

$V_{GS_2} = 0.577V$ $0.47V = \underline{\text{thresh}}$

$$I = \frac{1}{2}\times2.23\times10^{-4}\times\frac{185\mu}{0.12\mu}(0.577-0.47V)^2$$

$V_{D2} = 0.5V$ $\underline{= 1.9mA \to \text{agrees}}$

(set by common mode ~~fb~~ ~~negfb~~ bias)

~~$\#$~~ $\Rightarrow V_{D_2} = 0.5V > 0.91V - 0.47 = \underline{0.44V}$

$\underline{M4}$:- V_{Tp} measured $= 324.8mV$.

V_{Gate} from current mirror $= 0.74V$

$V_{D4} = V_{O+} = 0.5V < 0.746V + \underline{0.324V} \therefore \underline{\text{in sat}}$

$$I = \frac{1}{2} k_p \frac{W}{L} (V_{SG4} - V_T)^2.$$

$g_m = 25.5mS$

$$K_p\,ext = \frac{g_m}{W/L (V_{SG} - V_T)} = 115.29 \times 10^{-6}.$$

$$\therefore I = \frac{1}{2} \times 115.29 \times 10^{-6} \times \frac{202}{0.12} (V_{SG} - V_T)^2$$

$\approx 1.7mA$ agrees

Current mirror → Voltage is generated after tuning (I source of 2mA) to give 0.746V

LNA + mixer Calculations :-

→ Net gain = (Gain of LNA)$_{modified}$ × (Conv. gain)

The gain of LNA is slightly modified by Rin of mixer.

Rin of mixer is now 492.61Ω @ 2GHz.
(This translates to some Rindiff. as well)

Rout (LNA) (diff.) = 620.96Ω

So, gain of LNA is reduced by a factor

$$\frac{(R_{parallel})}{(620.96)} = \underline{0.44},$$ but it's

compensated by high conv. gain of mixer

$\therefore$ Gain net = $(\text{Gain LNA})_{\text{standalone}} \times 0.44 \times (\text{Gain mixer})$

Gain of LNA alone $\approx 30\,dB \Rightarrow 31.62$ volt gain

Gain mixer $\approx 21\,dB = 11.22$ volt gain

$\therefore$ Net gain = $11.22 \times 0.44 \times 31.62$
$= \underline{\underline{156.10}}$

$\boxed{\approx 44\,dB}$ ~~greater than~~

greater than ~~close to~~ min spec of $\underbrace{15\,dB}_{\text{mixer}} + \underbrace{20\,dB}_{\text{LNA}} = 35\,dB$

and agrees with $\underline{\text{simulations}}$.

→ <u>Net noise figure</u> $F_1 + \dfrac{(F_2 - 1)}{G_1}$

G_1 is modified gain (power) = 193.60 after the $(0.44)^2$ factor

$F_2 \approx 10^{(8.7/10)} = 7.44$

for standalone LNA (1.17dB) F_1 = SNF magnitude was actually ~ $\underline{1.31}$

$\therefore F_{net} = 1.31 + \dfrac{(7.44 - 1)}{193.60}$

$= 1.343 \approx 1.3\,dB$

But actual NF ~ 4dB probably because we effectively reduced Rout of LNA by 0.44 and F_1 is standalone Noise factor

Net IIP3 =

$$\frac{1}{IIP_3} = \frac{1}{I_1} + \frac{G}{I_2}$$

$I_1 = \simeq -3.82\,dBm = 0.41495\,mW$

$I_2 \approx 2.5\,dBm = 1.77828\,mW$

$G \approx 200$ (modified)

$$\frac{1}{IIP_3} = \frac{1}{(8.70 \times 10^{-3})} \Rightarrow IIP_3 \approx \underline{-20.6\,dBm}$$

verified