

Table 1: VCO Performance Summary Table

	Design Metric	Performance	Specification
Output Amplitude	$f_o = 3.8\text{GHz}$	0.976V	$\geq 1\text{V}$
	$f_o = 4.0\text{GHz}$	0.98V	$\geq 1\text{V}$
	$f_o = 4.2\text{GHz}$	0.99V	$\geq 1\text{V}$
Phase Noise [1MHz offset]	$f_o = 3.8\text{GHz}$	-116.855dBc/Hz	$\leq -115\text{dBc/Hz}$
	$f_o = 4.0\text{GHz}$	-116.52dBc/Hz	$\leq -115\text{dBc/Hz}$
	$f_o = 4.2\text{GHz}$	-115.66dBc/Hz	$\leq -115\text{dBc/Hz}$
Phase Noise [20MHz offset]	$f_o = 3.8\text{GHz}$	-144.84dBc/Hz	$\leq -140\text{dBc/Hz}$
	$f_o = 4.0\text{GHz}$	-144.56dBc/Hz	$\leq -140\text{dBc/Hz}$
	$f_o = 4.2\text{GHz}$	-143.86dBc/Hz	$\leq -140\text{dBc/Hz}$
Tuning Range	Total Tuning Range [Specify Range]	[3.798G, 4.218G] 420MHz	$\geq 400\text{MHz}$
	Number of bits in coarse-tuning	2	
	Voltage range in fine-tuning	[0.095V, 1.2V] 1.11V	
	Average K_{VCO}	155MHz/V	$\approx 100\text{MHz/V}$
	% variation in K_{VCO}	74%	Minimal
Power [4.2GHz]	VCO average power consumption [Excluding Bias]	1.61mW	
	Bias circuit power consumption	4.93mW	
Other	Sum of all capacitances [in capacitor bank]	0.15pF in one bank	
	Inductance used	Total : 3.56nH	
	Simulator Used	Eldo	
Overlap	Between 4G, 3.9G curves	65.9%	>33%
	Between 4.1G, 4G curves	47.8%	>33%
	Between 4.2G, 4.1G curves	64.6%	>33%

VCO Project

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Introduction

This project deals with making an only NMOS cross coupled differential output VCO (voltage controlled oscillator) using a digitally tuned capacitor bank with a MOSFET based varactor for fine tuning.

CIRCUIT SCHEMATIC:

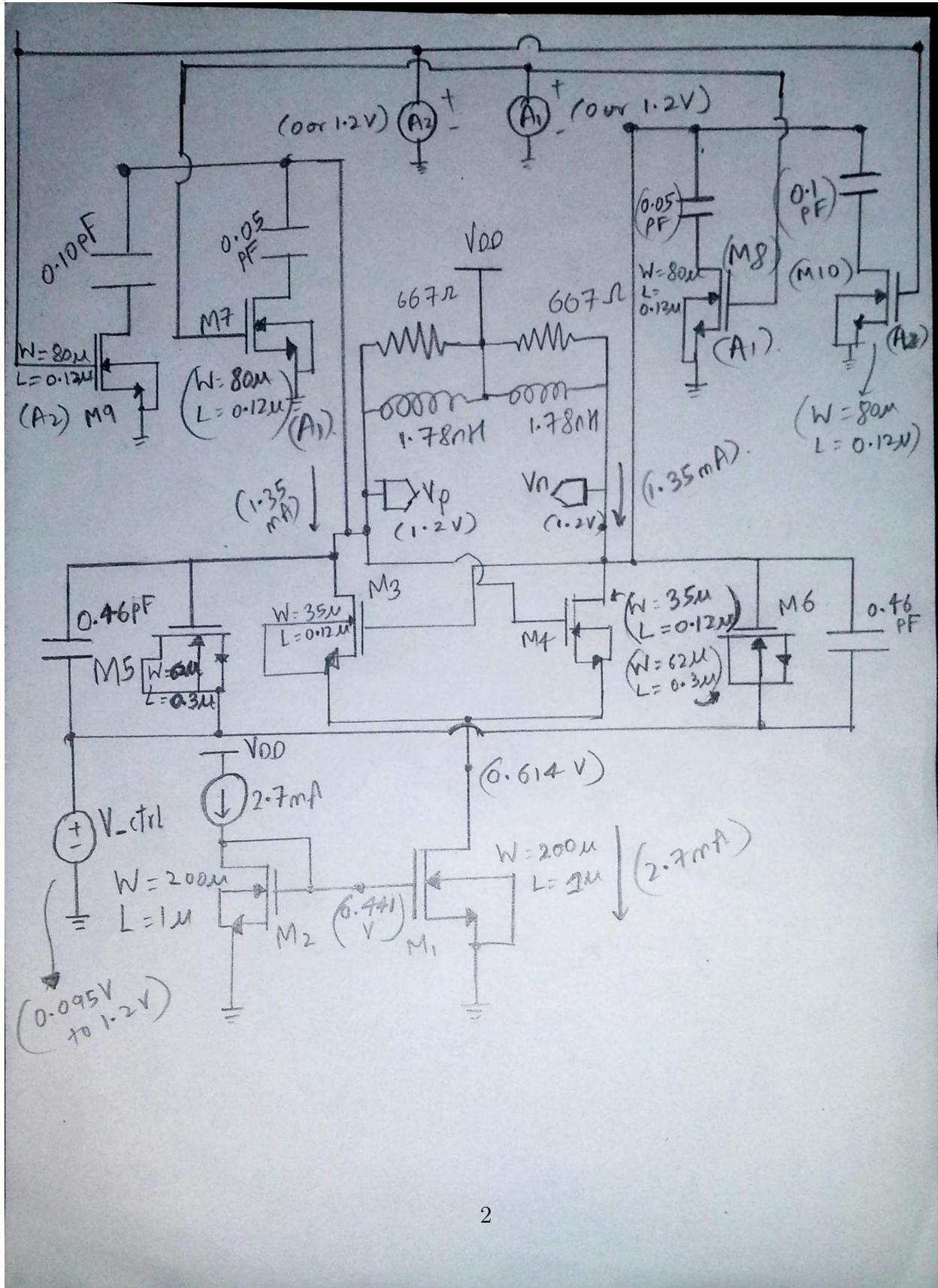


Figure 1: Circuit schematic for the only NMOS cross coupled differential output VCO. Op points at DC steady state.

VCO Performance:

Single ended Output Amplitude:

Before we start, the reason for choosing an NMOS only CC pair instead of a complimentary pair with a current source is that there would be headroom issues in the latter and it's observed that symmetry in the output waveforms is good enough for the former. Hence, we proceed with the NMOS only CC pair VCO.

First, in order to design for maximum amplitude, we first set the current according to what could be giving minimal power consumption. So, we choose a tail current of 2.7mA (initially was 2mA, changed to increase amplitude). We use same widths and lengths for M1 and M2 to ensure good current control throughout the design. Once, this current through MOSFET M1 is set, we set the output single ended amplitude to 1V at the saturation point of the v_{out} vs I_{tail} graph. So, we ensured amplitude didn't change upon increasing current further. To do this, we analysed the condition of M1 under the lowest drain voltage it can take. A modest value would be about 0.25V considering that the VT is reduced due to higher M1 length (M1 length, width is increased for good flicker noise performance). The width, length is changed such that 0.25V is above the threshold voltage of M1. We also ensure low enough gm so that the thermal noise from M1 isn't high, hence we don't increase the width a lot. Also, if I had to reduce the M1 overdrive voltage in order to decrease drain voltage supported, I could decrease current, but the output voltage may reduce and any changes in R_L (hence, the inductor value) is seen to affect noise performance a lot. The calculations are shown in the appendix.

Now that we know the net tail current, we can calculate widths of M3, M4 based on current passing through them in the dc steady state under saturation, keeping L to be $L_{min} = 0.12\mu$ to ensure lower parasitics. We can ideally keep any width in saturation (because of CLM the V_{ds} can change), but we keep a high enough width so as to just ensure the overdrive voltage is low enough (hence keeping high source voltage) ensuring the current source isn't in triode at all times. We don't increase width any further to keep parasitics and the gm low (lower thermal noise) . The calculations are in the appendix.

Now that we first decided the current, this automatically gives us the output resistance value to be used for a single ended amplitude of 1V. The theoretical value calculated differs slightly from the value of R_L chosen due to tuning of

the inductor value for noise performance and frequency tuning. So, with RL , we also obtain the inductor value needed. Now, upon adding an appropriate capacitor, this would give us the amplitude we want. The calculations are in the appendix.

The graph for output voltage amplitude at a $V_{ctrl} = 0.65V$ (mid value of the tuning range) and at different operating frequencies are shown in fig. 2,3 and 4. It's seen that we get a close enough single ended output amplitude of 0.98V to 0.99V (calculated from halving differential output voltage). Since, we had already maxed out the current that can be applied, in order to increase it further we would have to change the width of M1 or M3 and even RL . This might disturb the performance of other specs and hence, we went ahead with this amplitude performance keeping in mind a fairly low power consumption.

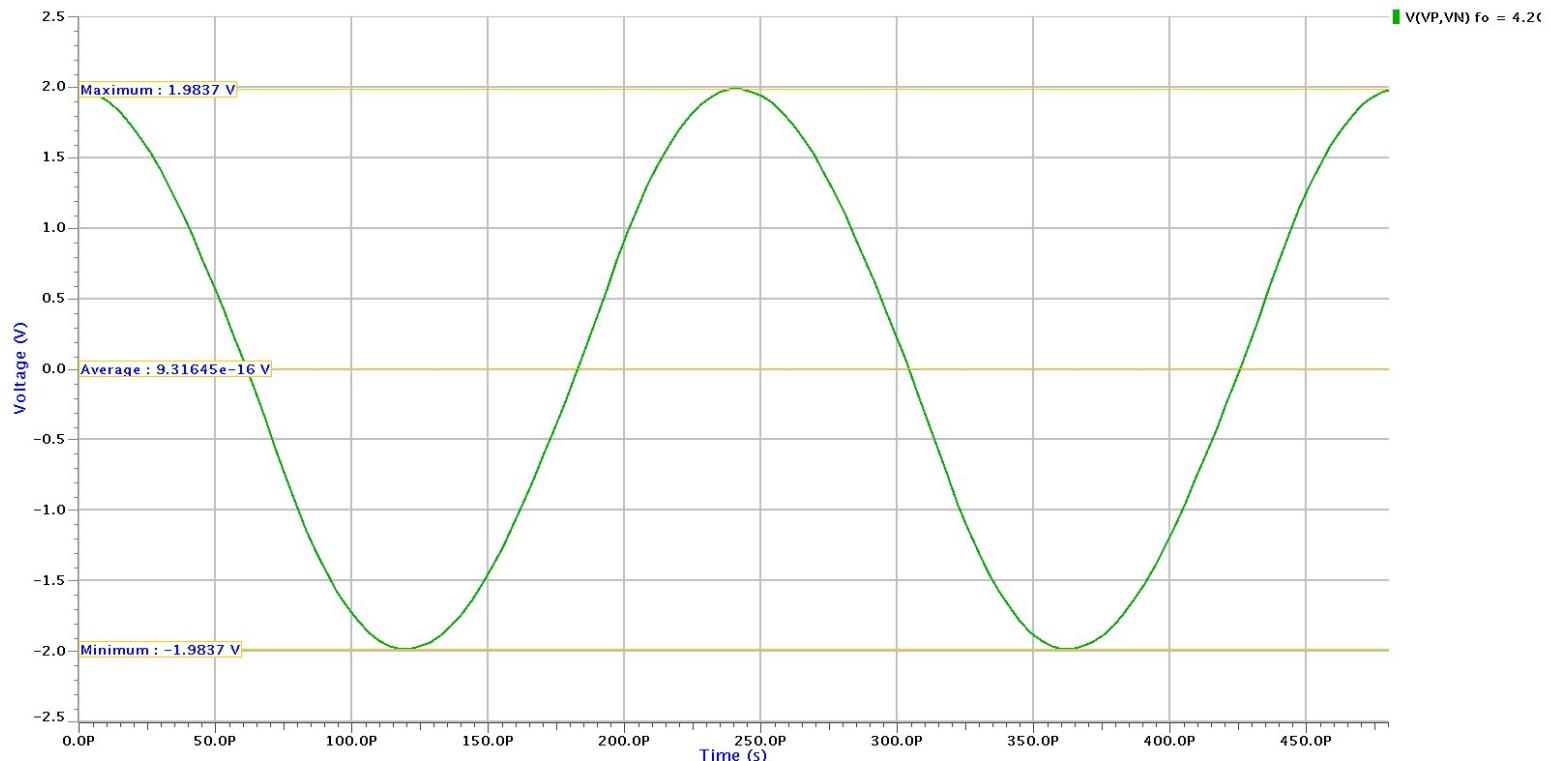


Figure 2: Plot of output differential amplitude for $fo = 4.2G$, with $V_{ctrl} = 0.65V$. Single ended amplitude turns out to be: 0.99V

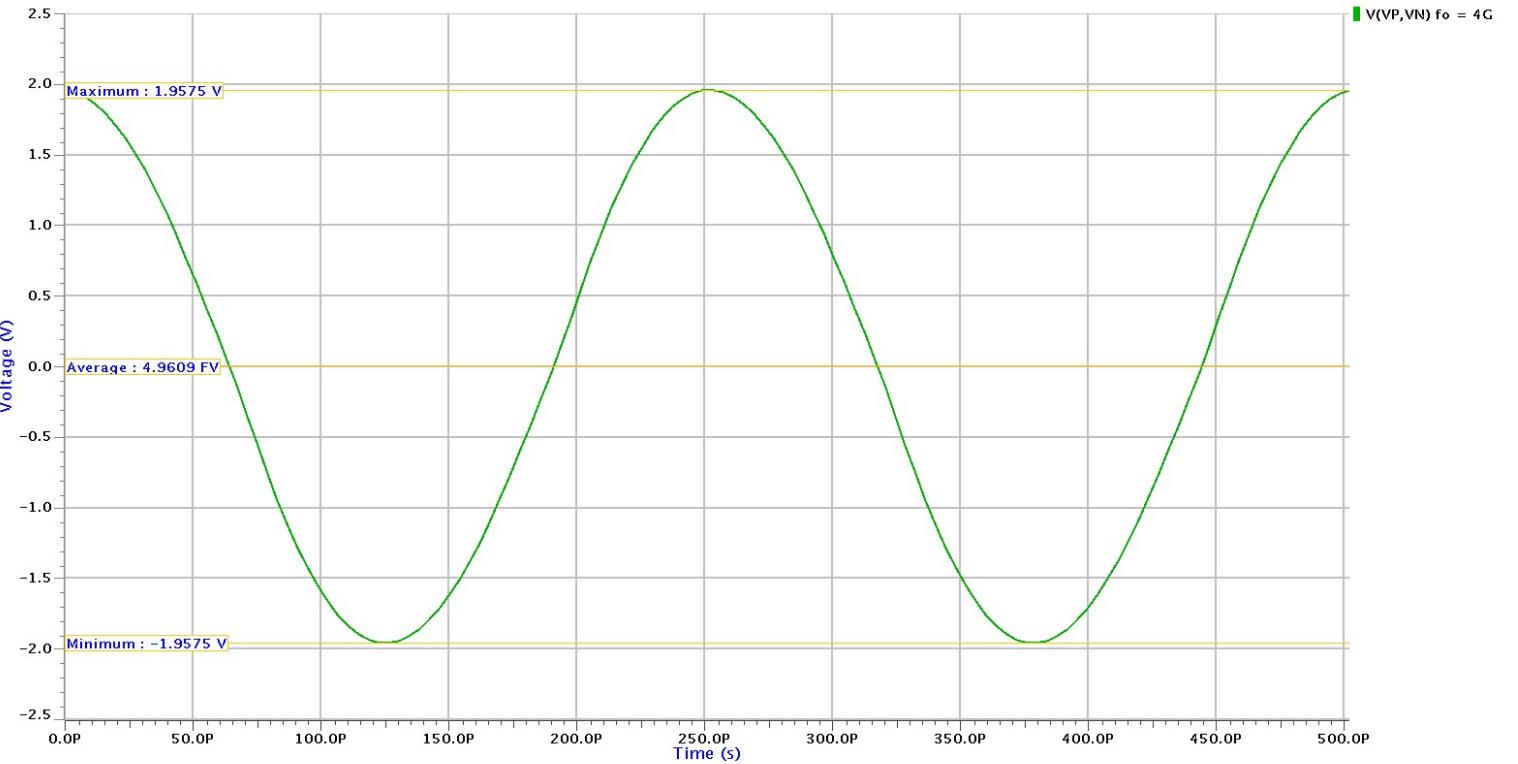


Figure 3: Plot of output differential amplitude for $f_o = 4G$, with $V_{ctrl} = 0.65V$. Single ended amplitude turns out to be: 0.98V

Phase Noise Performance:

The two parameters to change the noise performance in the VCO is the width, length of M1 and also the output amplitude. We ensured a close enough output amplitude already and the width , length of M1 were chosen to be around 200u, 1u to keep the flicker noise low. We also maintained low enough gm from M1 (around 24mS) and M3,M4 to lower thermal noise. One way of tuning that was adopted here was to keep the ratio of width and length of M1 constant and change the product so that the gm doesn't change, hence improving flicker noise and keeping thermal noise as it is.

One of the design challenges faced when tuning for noise was that, the noise was not only a function of the output amplitude and W,L of M1, it was changing with the inductor value chosen (which changes RL). It was observed that noise was better at a lower inductor value compared to a higher

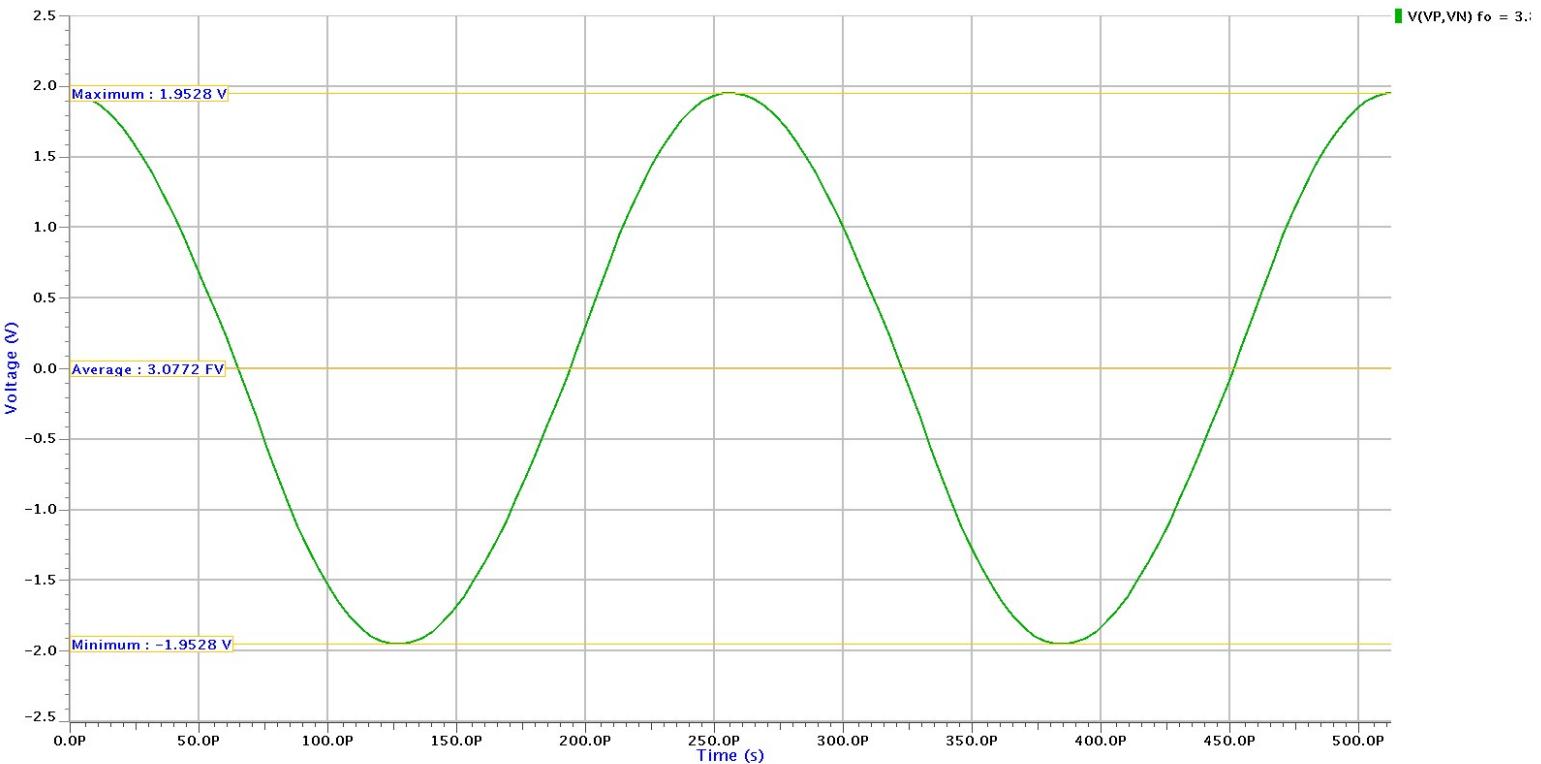


Figure 4: Plot of output differential amplitude for $f_o = 3.8G$, with $V_{ctrl} = 0.65V$. Single ended amplitude turns out to be: 0.976V

one (keeping L^*C constant ofcourse). A possible reason is that, since we define noise as a ratio involving voltage amplitudes here, the voltage noise from a resistor decreases as it's resistance decreases. So, finally we had to tune the 'L' (decreasing L) and 'C' such that noise was also good and even ensuring a good single ended voltage amplitude after choosing all the parameters discussed in the previous section. This is also probably why the current had to be increased from 2mA to 2.7mA as specified in the beginning.

The phase noise performance for a 1MHz offset and 20MHz offset at three operating frequencies is as shown in fig. 5, 6 and 7. We again use the middle value for $V_{ctrl} = 0.65V$. We see that all the noise specifications are satisfied and especially see a good thermal noise performance.

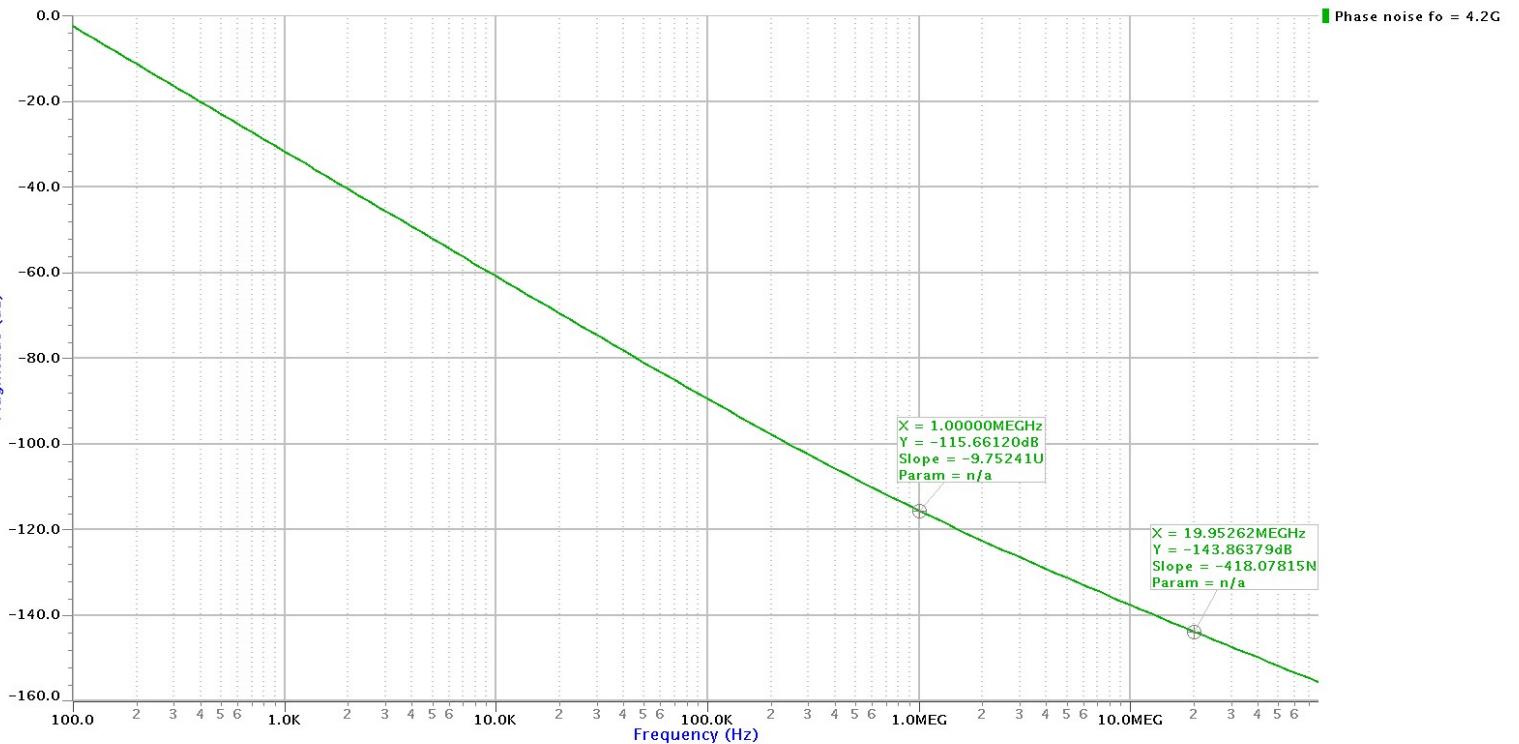


Figure 5: Plot of phase noise and values at 1MHz, 20MHz offset for $f_0 = 4.2\text{G}$, with $V_{ctrl} = 0.65\text{V}$

Tuning Range:

Since the specification on KVCO is around 100MHz/V (minimum), a rough calculation would yield that given the 400MHz tuning range, we'll need four coarse tunes. Ofcourse there's overlap because KVCO would be greater than 100MHz/V . So, we use a 2 bit digital switch controlled capacitor bank with a varactor.

Capacitor Bank:

For the design of switches, we ensure minimum parasitics by choosing low W,L ($= L_{min}$). We also need a low 'Ron' (on resistance). The on-resistance calculated when the mosfet is in triode, is inversely proportional to overdrive voltage, W/L as well. So, we use 1.2V for 'on' and 0V for 'off'. The 'W' chosen is pretty high maintaining $L = L_{min}$. To ensure proper cutoff, the 'off' voltage for the switch is chosen as 0V .

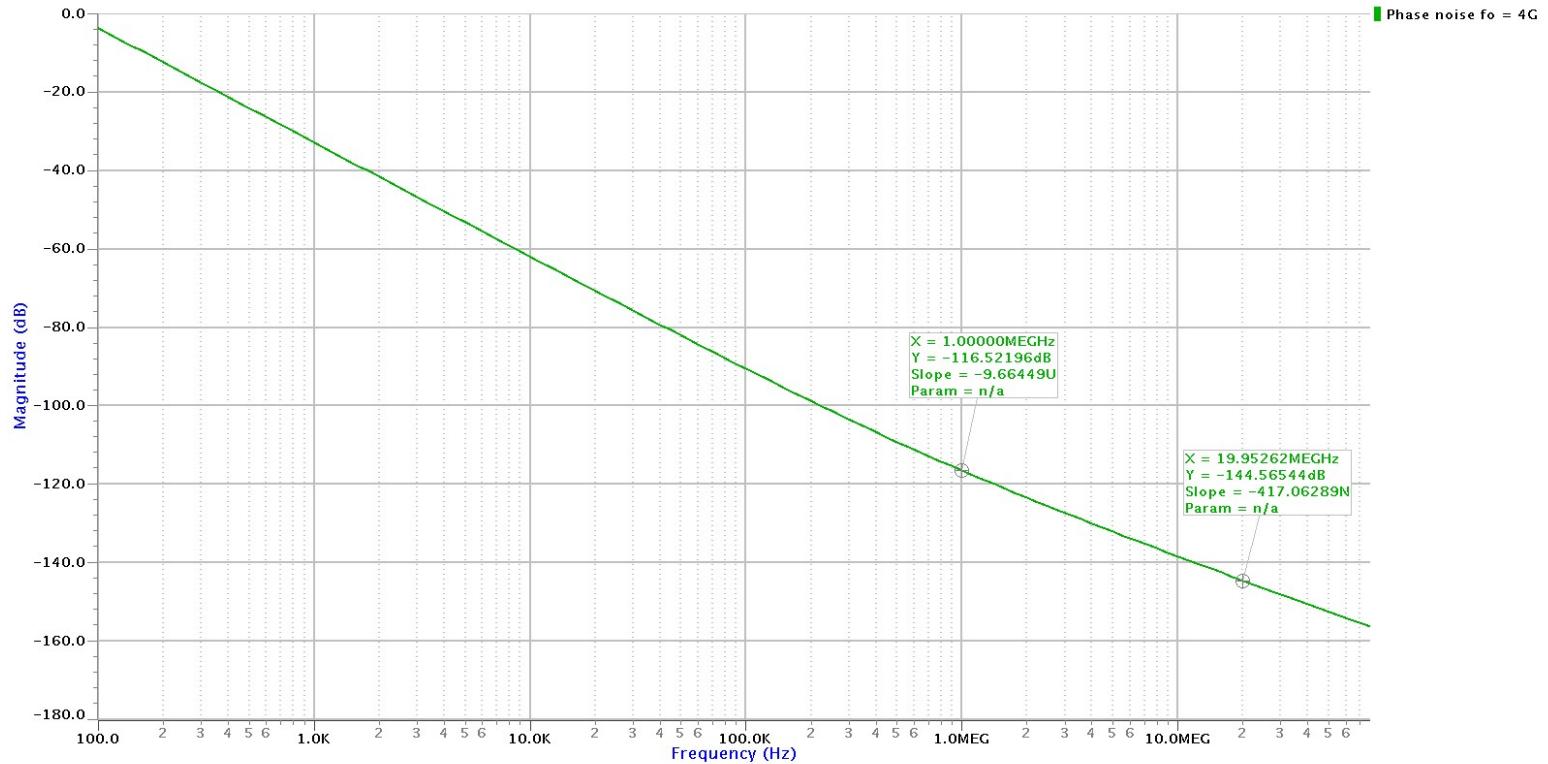


Figure 6: Plot of phase noise and values at 1MHz, 20MHz offset for $f_0 = 4G$, with $V_{ctrl} = 0.65V$

The incremental capacitors were just chosen by using capacitors of 1 order less in magnitude (0.05pF). They were tuned to set a good overlap between the frequency curves in the desired operating range of frequency, voltage.

Varactor:

The varactor is chosen to give the minimal KVCO needed of 100 MHz/V with a max variation upto 200MHz/V. We use a MOSFET based varactor with drain and source shorted and source voltage controlled by another voltage source V_{ctrl} (0.095V to 1.2V). AS the product of width and length of the varactor increases, it's capacitance, KVCO also increases.

Initially, to set the oscillation frequency, varactor width, we set the incremental cap at 0.05pF and set both switches to '11', ie total cap added is $2*C + C = 3C$ (0.15pF). Next, the width of varactor and the fixed capaci-

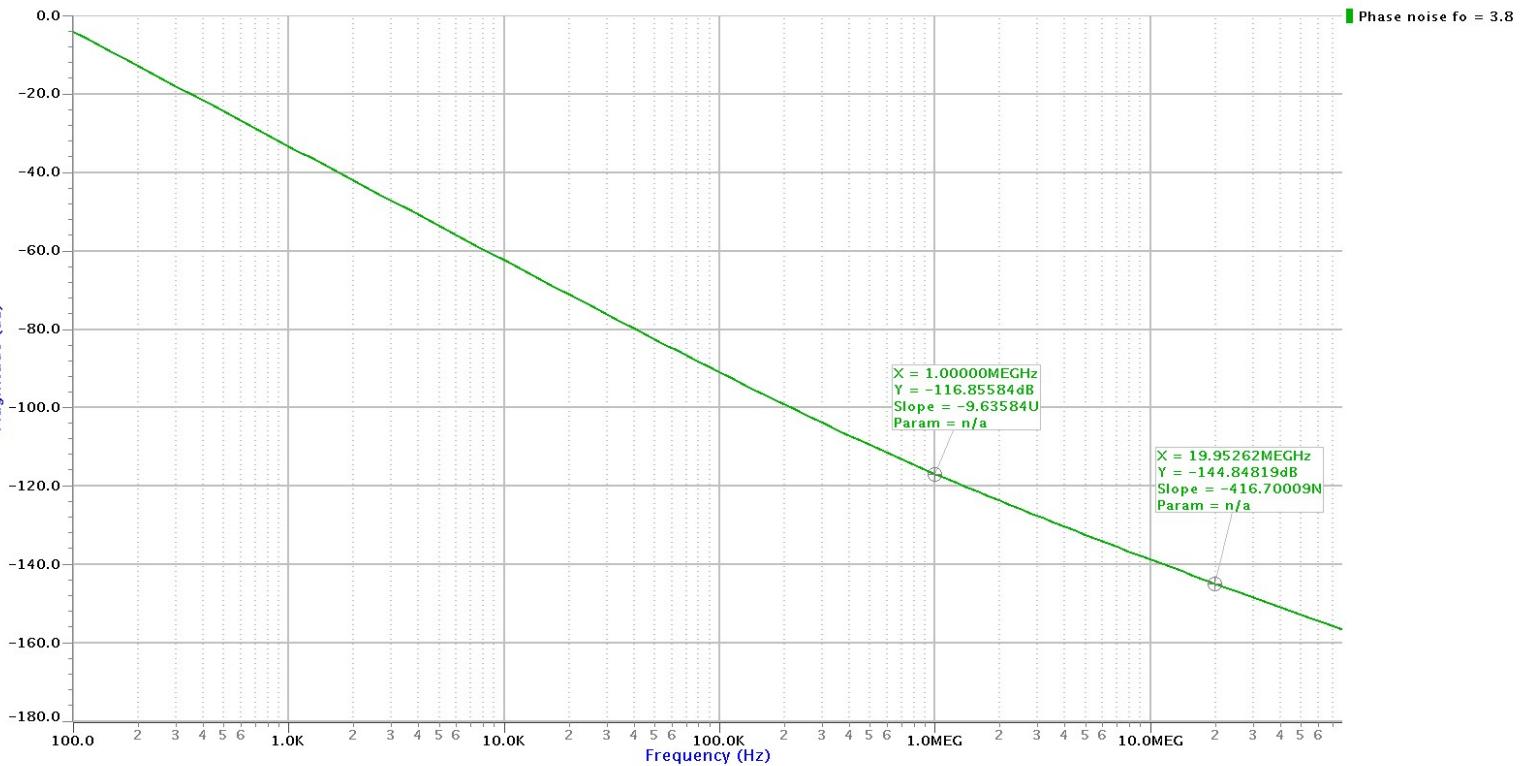


Figure 7: Plot of phase noise and values at 1MHz, 20MHz offset for $f_0 = 3.8\text{GHz}$, with $V_{ctrl} = 0.65\text{V}$

tance value is tuned such that we get the range of frequencies of 3.8GHz to 3.9GHz and also giving a KCVO of around atleast 100MHz/V, but also ensuring a low peak in KVCO (around 180MHz/V). This ensures that the KVCO in subsequent combinations of switches, should be greater than 100MHz/V, because at '11' the varactor has minimal contribution to capacitance and hence minimal tuning ability (which increases as we go from '11' to '00'). The high enough KVCO provides a good overlap in curves as shown in fig. 8,9 and 10. We can see the different curves and the marked frequency levels. There are four curves corresponding to 4.2G, 4.1G, 4G, 3.9G. The overlap percentage is calculated as shown below:

Between 4.2G and 4.1G: $121.96\text{Meg} / 190.02\text{Meg} = 64.6\%$

Between 4.1G and 4G curves: $86\text{Meg} / 179.9\text{Meg} = 47.8\%$

Between 4G and 3.9G curves: $112\text{Meg} / 171.50\text{Meg} = 65.9\%$

In fig. 11, we can see the KVCO values for different values of A1,A2. The KVCO is always above 100MHz/V in the tuning control voltage range of around 0.1V to 0.12V. The average KVCO calculated and percent variation is:

$f_0 = 4.2G$
 Avg. KVCO: 180.29Meg
 Max variation: 78%

$f_0 = 4.1G$
 Avg. KVCO: 172Meg
 Max variation: 78%

$f_0 = 4G$
 Avg. KVCO: 162.46Meg
 Max variation: 73.5%

$f_0 = 3.9G$
 Avg. KVCO: 155Meg
 Max variation: 74.5%

With a MOS varactor this variation is expected. Best case avg KVCO is 155MHz/V with a 74 percent variation. The net tuning range in frequency, voltage is:

$f_{min} = 3.798GHz$
 $f_{max} = 4.218GHz$
 Tuning range: 420MHz
 $V_{ctrl\ min} = 0.095V$
 $V_{ctrl\ max} = 1.2V$

Hence, we get a 420MHz of tuning range.

Startup Nature:

In fig. 12, we see the startup nature of the VCO. We also saw in the hand-calculations that the gmR in startup is around 11. This ensures really fast startup and hence fast settling at around 3-4ns as shown in the figure.

Power Consumption:

The total DC steady state Power Consumption turns out to be:

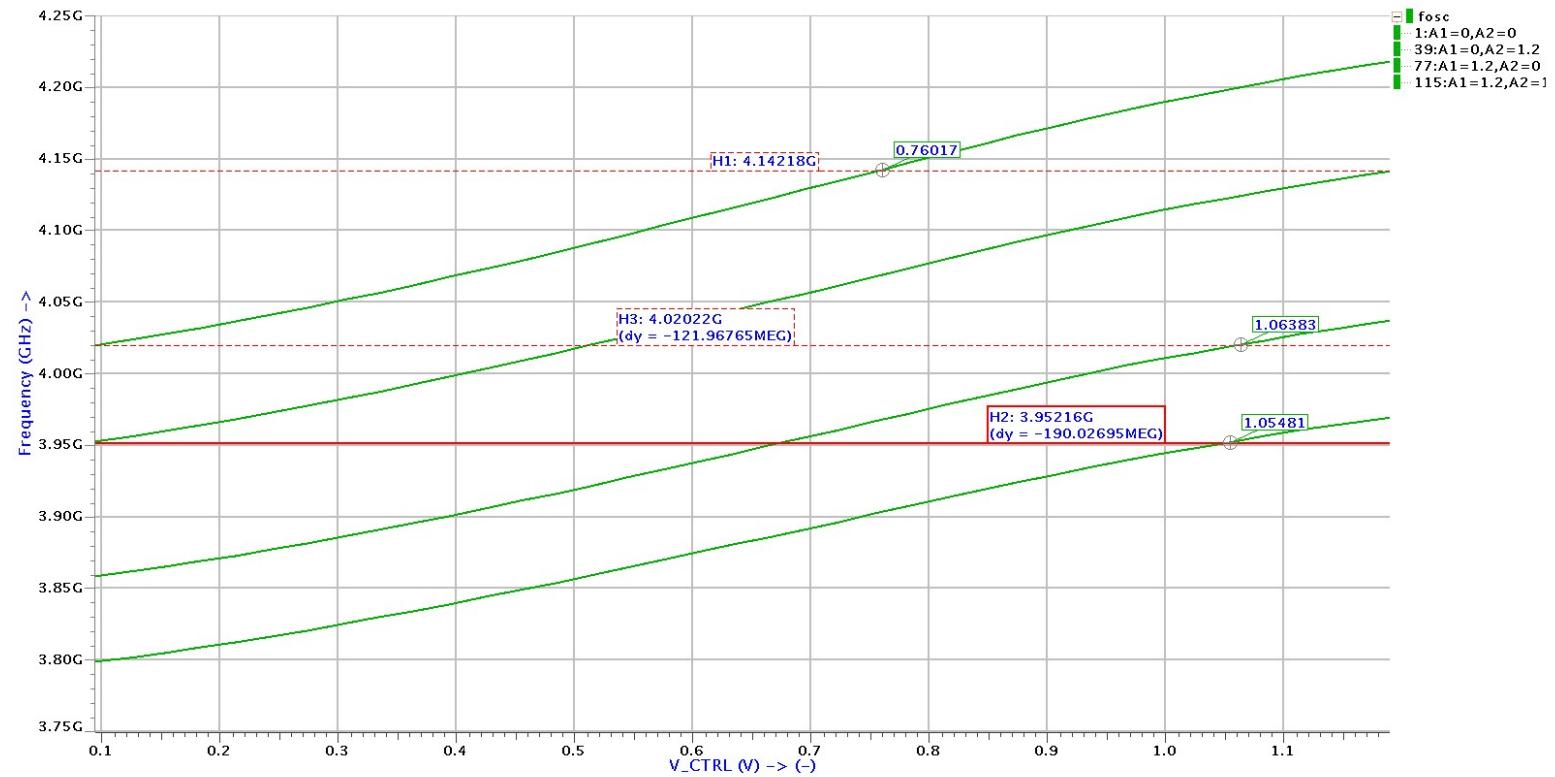


Figure 8: Overlap between $f_0 = 4.2\text{G}$, $f_0 = 4.1\text{G}$ tuning curves.

Total Power: 6.54mW

Total Power (excluding bias): 1.61mW

Total Power (only bias): 4.93mW

The proof of power consumption for M3, M4, M1 and total power is as shown in fig. 13.

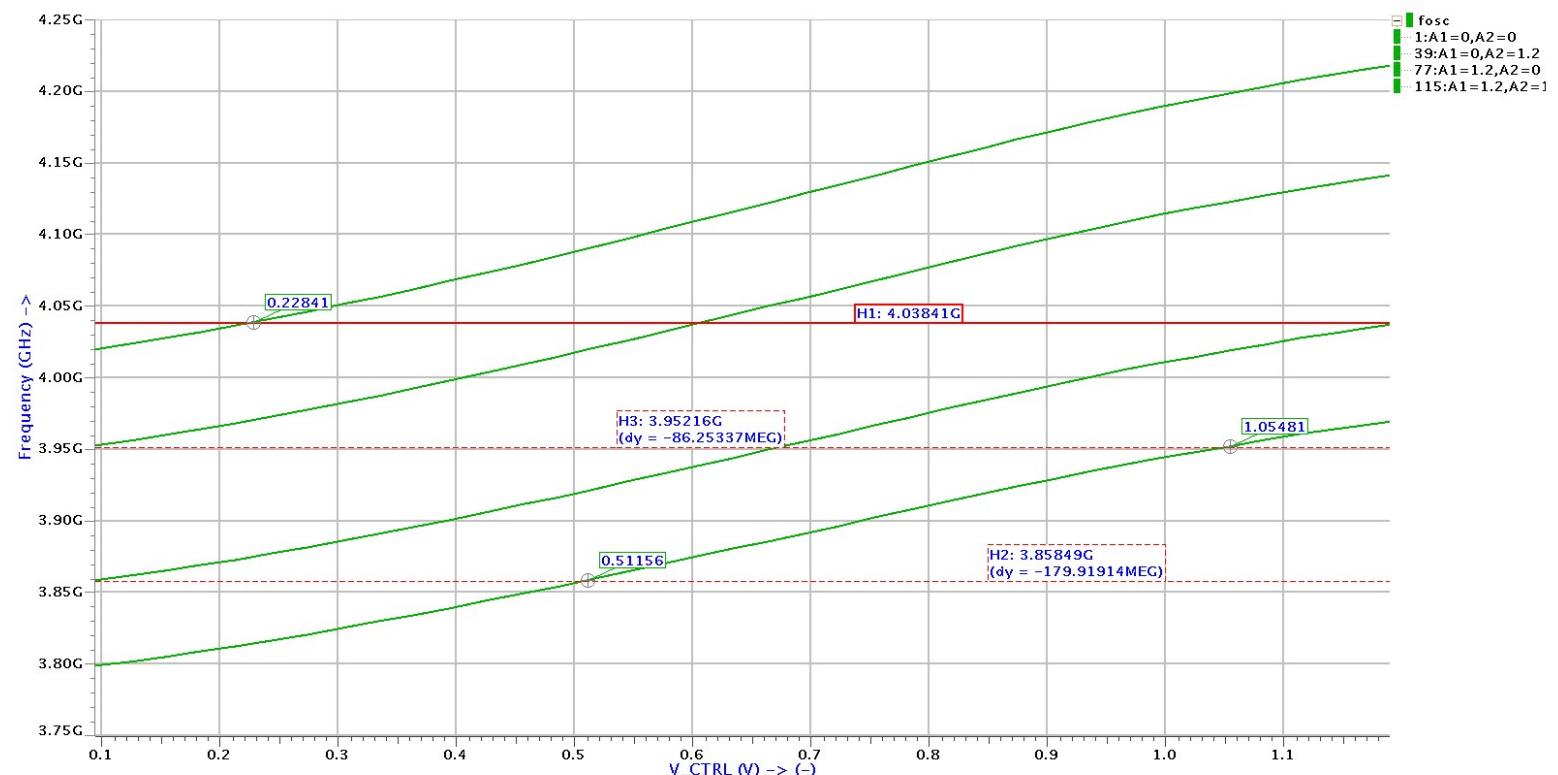


Figure 9: Overlap between $f_0 = 4.1\text{G}$, $f_0 = 4.0\text{G}$ tuning curves.

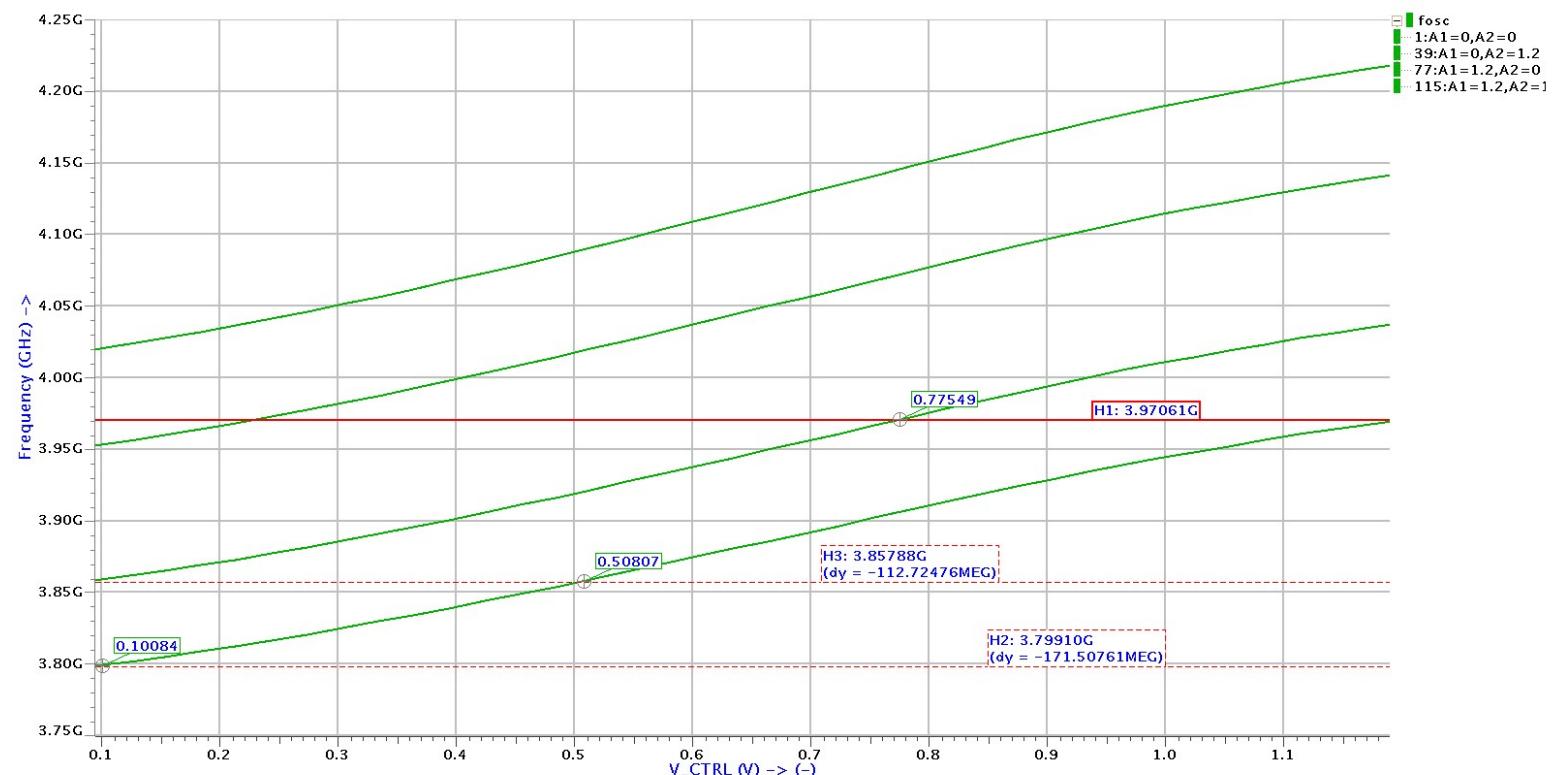


Figure 10: Overlap between $f_0 = 4\text{G}$, $f_0 = 3.9\text{G}$ tuning curves.

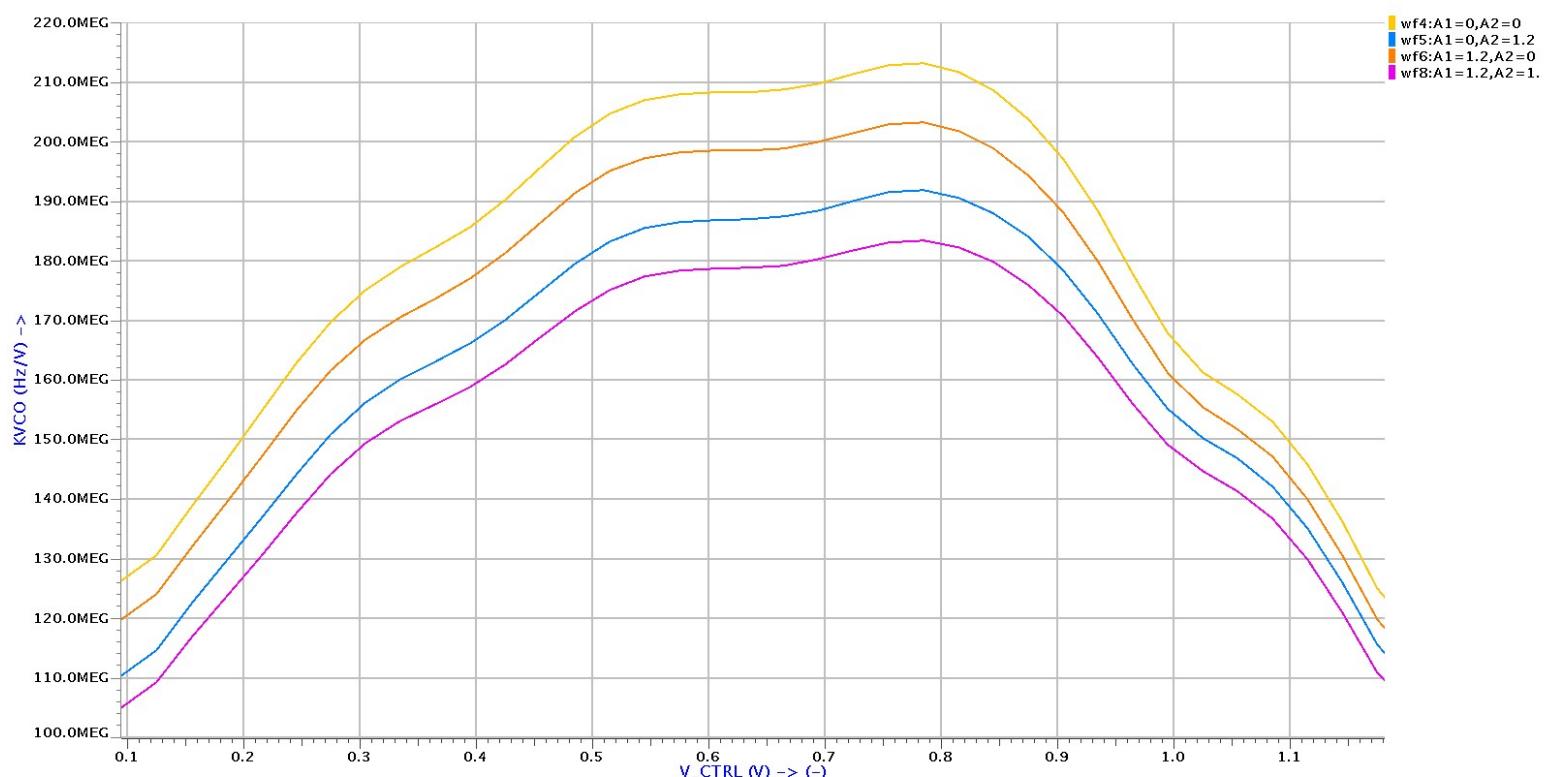


Figure 11: Plot of KVCO for different f0 and over given Vctrl of 0.1V to 1.2V and for different values of A1,A2: 0,0 ; 0,1.2 ; 1.2,0 ; 1.2,1.2 .

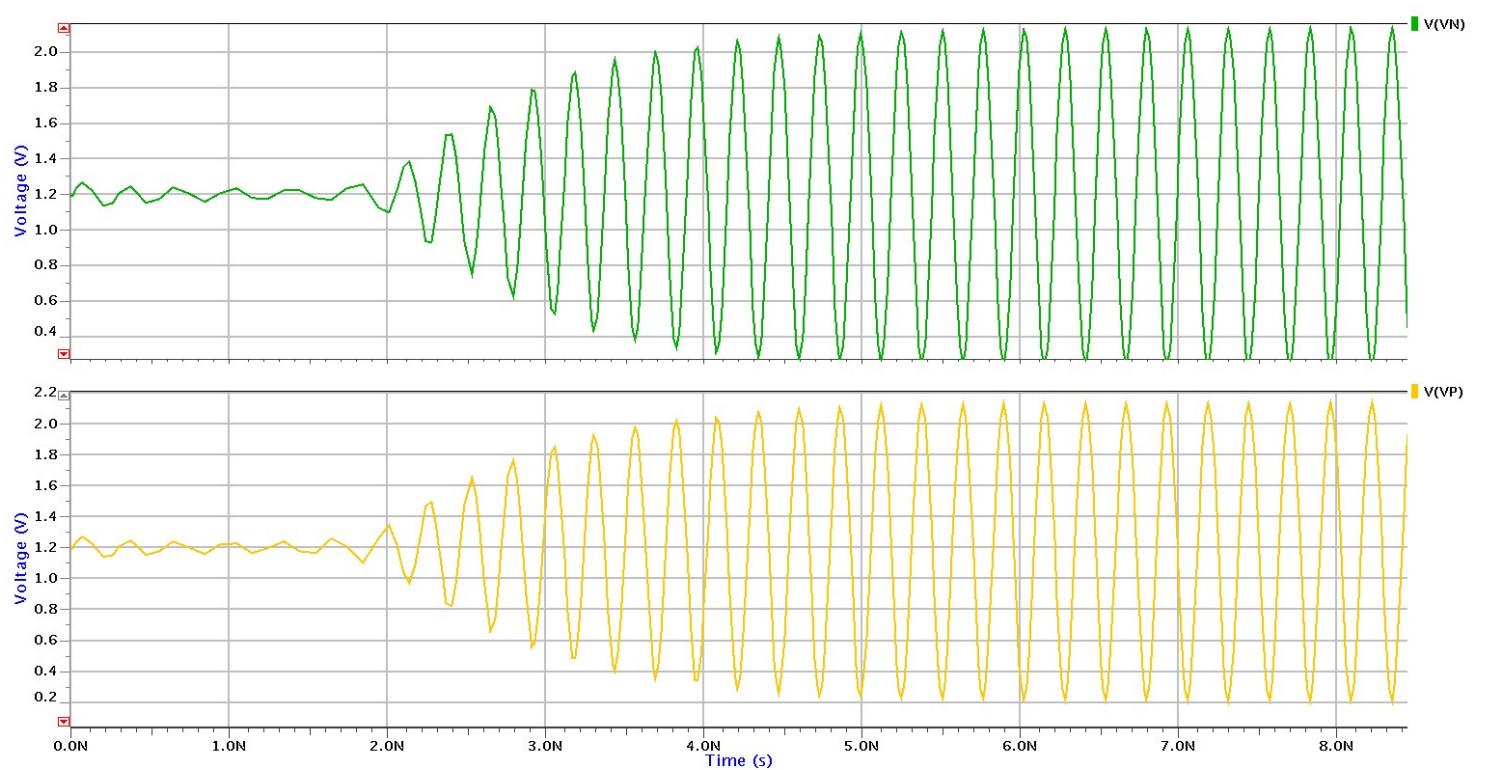


Figure 12: Startup nature of V_{out} (+ and -) shown for $f_0 = 4\text{GHz}$, $V_{ctrl} = 0.65\text{V}$ and after introducing a 1mV initial voltage offset in one of the fixed capacitors .

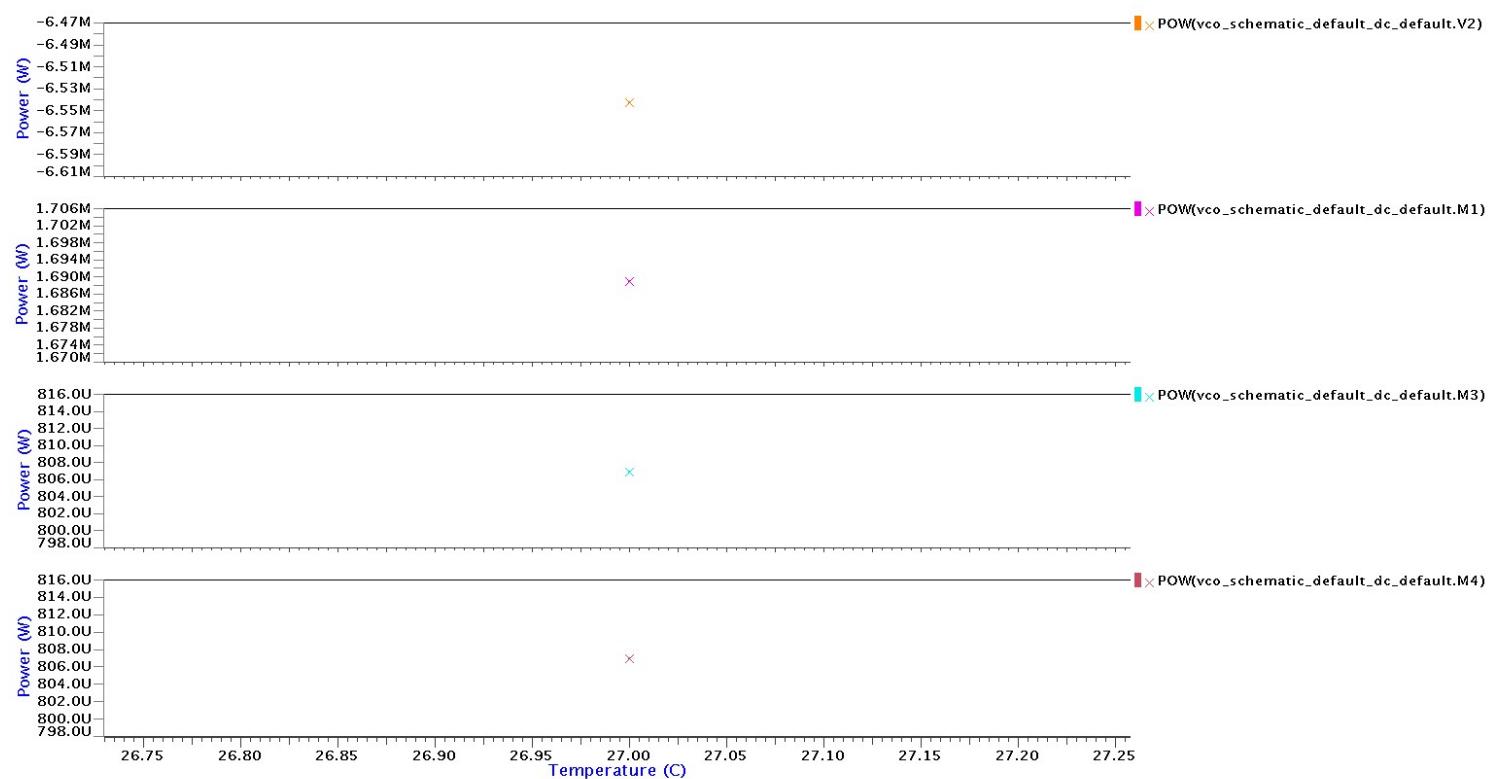


Figure 13: DC Power consumption in M3, M4, M1 and total power (V2-supply).

Appendix

Hand calculations :-

Analysis @ extremes of D/I/volt

→ Calculation for width, length of M₁, :-

The way it's actually done on the simulator is to attach a voltage source @ Drain of M₁, tune width, length for given current, worst case drain voltage.

Since it's designed for V_D = 0.25V, we attach a 0.25V volt-source @ the Drain and change (W/L)(M₁).

Finally, we arrive @ this :- W = 200μm, L = 1μm.

This can be verified as:-

$$M_1: \frac{V_{T1} \text{ measured} = 168 \text{ mV}}{g_m \text{ measured } \approx 20 \text{ mS.}} \rightarrow \frac{1}{L} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) = 20 \text{ mS.}$$
$$V_{GS} = 0.44 \text{ V.}$$

$$I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (\text{In saturation})$$

To show it's in saturation $I = 0.5(V_{GS} - V_T)g_m$ only if it's in saturation.

[(DR). To involve the W/L as well, we first find $(\mu_n C_{ox})_{\text{estimated}}$ from the given W, L range using gm. So, for W in the 200μ range or L near 1μ,

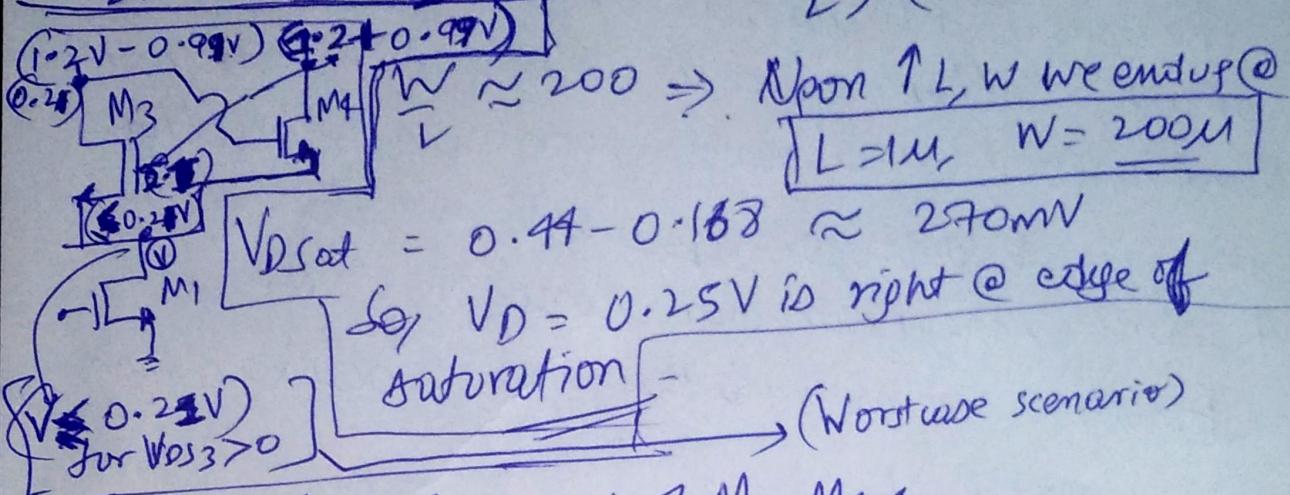
$$\frac{1}{L} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) = g_m$$

$$(\mu_n C_{ox}) \frac{(200)\mu}{1\mu} (0.44 - 0.168) = 20 \text{ mS.}$$

$$(\mu_n C_{ox} = 3.676 \times 10^{-4})$$

\therefore (These widths, lengths, used needn't be exactly 200μ, 1μ)

$$2.7mA = I = \frac{1}{2} (3.678 \times 10^{-4}) \left(\frac{W}{L} \right) (0.44 - 0.168)^2$$



DC point, calc. of W, L of M_3, M_4 :

M_3 : $\mu m M_3 = 16.6mS$ (measured) (for widths, lengths of the pmosfet M_3)

$$\Rightarrow 16.6mS = \text{Unlon} \frac{W}{L} (V_{GS} - V_T) \text{ close to chosen } (\mu m \text{ value})$$

Note DC operating point for $M_3 \Rightarrow$ DC stable

state where $I_{M3} = I_{M4} \approx 1.35mA$ (No oscillations)

$$\text{so } I = \frac{I_T}{2} = 1.35mA = \frac{1}{2} (\mu \text{lon}) \frac{W}{L} (V_{GS} - V_T)^2$$

$$V_{G3} = 1.2V \text{ (DC)}; V_{GS3} \text{ measured} = 0.586V$$

$$V_{T3} = 0.421V \quad V_{S3} = 0.61V$$

$$\therefore \frac{W}{L} \approx 290 \Rightarrow \boxed{\begin{aligned} L &= 0.12\mu \\ W &= 35\mu \end{aligned}}$$

For M_1 : If turns out, V_o measured is $\approx 0.44V$,
 $V_{D_T} = V_{S3} = 0.61V > V_{O1} - V_T$.

$$V_T = \frac{1}{2} (3.676 \times 10^{-4}) (0.44 - 0.168V) \times \frac{200}{1} \approx 2.7mA$$

In saturation, verified.

DC picture is also done. (This is the DC s-s. picture)

Tuning range, Output amplitude:-

D/P amplitude :-
 Now we have the current, we find R_L so that
 single ended D/P amplitude is 1V.

$I_T = 2.7mA$, We saw earlier that
 @ the extremes, the current source can handle
 $\sim 0.25V$ @ the Drain being @ edge of
 saturation. Exact current turns out to be
 around $2.56mA$ (measured)

(after applying $0.25V$ @ Drain)

$$V_{o\text{ max}} = 2 \frac{1}{T_1} \cdot I_T \cdot R_L = 2 \frac{1}{T_1} \times (2.56mA) \times (666) \approx 1.09V$$

(666 Ω is chosen) close to $0.99V$ measured

(Note - $2.56mA$ measured is in M_1)

(After applying $0.25V$ @ Drain) ~~for gate (I tail)~~

So, After using I_T , $V_o = 1V$ to get $R_L \approx 666\Omega$ we choose the inductor.

Inductor, cap value:

$$(w_0 L) Q = R_L = 667 \Omega$$

$$Q = 15 @ 46\text{Hz} \quad L \approx 1.77 \text{nH}$$

$$w_0 = 2\pi \times 46 \text{Hz}$$

Verified

\therefore Cap value @ 46Hz = 0.90 pF
(net).

Tuning range: 400MHz needed, 100MHz/V

minimum K_{VCO}. Hence, for about 1V V_{ctrl} range, we need 4 coarse tunes. \therefore 2 bit Digital cap bank is used.

In the cap. bank, $R_{on} \propto \frac{1}{W(V_{DS} - VT)}$

so, V_{DS} ; W/L is maximized,

$$V_D = 1.2V, \quad W = 80\mu\text{m}, \quad L = 0.12\mu\text{m}$$

(To ensure low parasitics)

Incremental cap = 0.05 pF.

is used.

Varactor width = 62 μm , $L = 0.3\mu\text{m}$ } Based on given K_{VCO}, setting the freq range b/w 3.8 GHz to 4.2 GHz

fixed cap = 0.46 pF

Note: For cap. bank each switch is tested for Z_{out} ensuring low (out, R_{out}) given the incremental cap.

Power consumption :-

(DC steady state)

Measured Power @ $M_3, M_4 = 0.806 \text{ mW}$

Power @ $M_1 = 1.69 \text{ mW}$

$P_{M_3 + M_4 + M_1} = 3.30 \text{ mW}$

Rest is current mirror bias + curr source
 $= 1.2V \times 2.7 \text{ mA}$
 $= 3.24 \text{ mW}$.

\therefore Total = $6.54 \text{ mW} \rightarrow$ same as measured

Startup behaviour :-

$$g_m(M_3) = 17.932 \text{ mS.}$$

$$R = 666 \Omega.$$

$$g_m R \geq 1 \quad g_m R = \underline{\underline{11.92}} \gg 1$$

Hence it satisfied startup cond^{it}.

So We made sure $g_m R > 1$ with given
"R" value chosen