Table 1: Power Amplifier Performance Summary Table

	Design Metric	Performance	Specification
Output P1dB	f_o = 1.9 GHz	10.66dBm	≥ 10 dBm
	f_o = 2.0 GHz	10.69dBm	≥ 10 dBm
	f_o = 2.1 GHz	10.57dBm	≥ 10 dBm
AM-PM deviation at P1dB	f_o = 1.9 GHz	0.81 deg	≤ 5 degrees
	f_o = 2.0 GHz	0.6 deg	≤ 5 degrees
	f_o = 2.1 GHz	0.3 deg	≤ 5 degrees
Voltage-gain from gate to drain	f_o = 1.9 GHz	18.81	≥ 2
	f_o = 2.0 GHz	18.805	≥ 2
	f_o = 2.1 GHz	18.71	≥ 2
Power	PA average power consumption [Excluding Bias]	27.84mW	-
	Bias circuit power consumption	1.2mW	Minimize
Other	Sum of all capacitances [Including AC coupling]	2uF	-
	Inductance used	5.2nH	-
	Simulator Used	Eldo	-

Power Amplifier Project

Roll No. : EE18B155
Name : Balasubramaniam M C

May 16th 2021

Introduction

This project deals with making a power amplifier of given specs with no input or output match.

CIRCUIT SCHEMATIC:

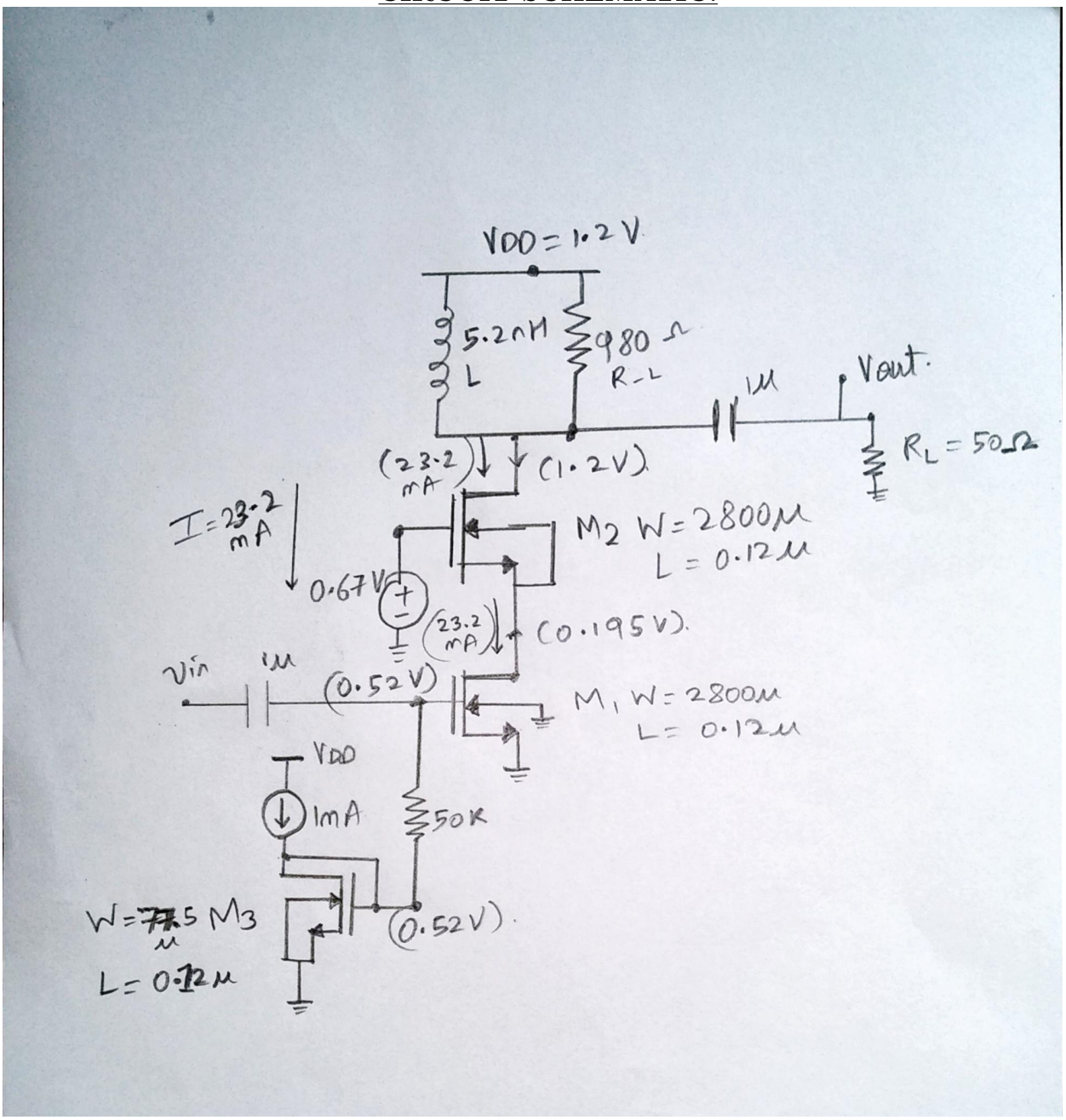


Figure 1: Circuit schematic for the Power amplifier including DC bias points.

PA Performance:

Output P1dB:

We first start from designing for the output power, from which usually, voltage gain and AM-PM deviation are also satisfied. A cascoded structure is used for better stability and easier calculation of parasitics at the drain of cascode. Design for output power using the triode limit and cutoff limit could be used. A stronger limit is the cutoff limit determining maximum signal current, while the VDSat limit isn't very exact. So, based on this a minimum bias current of 20mA needed was calculated. However, we need a very high width which is why we use 2800u. Bias voltage of M1 turned out to be 0.52V to give 20mA for a 2800u width. A ballpark value of 2500u width was chosen initially and then tuned instead of directly calculating because we don't exactly know the electron mobility or Cox at those widths. The drain of M1 is set to be biased at edge of triode (around 100mV - from VGS-VT) initially to increase swing. It was later increased to set M1 and M2's gm to be the same and to slightly move M1 out of triode during the swing. This was done by increasing gate bias voltage of M2 to 0.67V. Finally, the current bias has increased to 23mA increasing output saturation power as well. The challenge with using the VDSAT limit or equating it to the cutoff limit would be that there's significant Channel length Modulation. Hence, we can't exactly say the output power swing. Even the VDSAT measured and VGS-VT's applied were different due to this. So, we made sure the VDSAT measured was low enough anyway for high swing and use the cutoff limit mainly to control the current. We don't increase it too much above 20mA to minimize power.
Finally, the output fundamental power plots are shown in figs. 2,3 and 4. We see that at all these frequencies we satisfy the power requirement.

```
P1dB @ 1.9GHz: 10.66dBm
P1dB @ 2GHz: 10.69dBm
P1dB @ 2.1GHz: 10.57dBm
```

Voltage gain:

Designing for voltage gain is easy now because we have achieved a high enough power using high MOSFET widths. This should give us a very high gm for M1,M2 (around 460-480mS). As shown in the hand calculations the gain measured and calculated is around 18.7. Fig. 5 shows voltage gain at 1.9, 2 and 2.1 GHz and the maximum voltage gain as well.

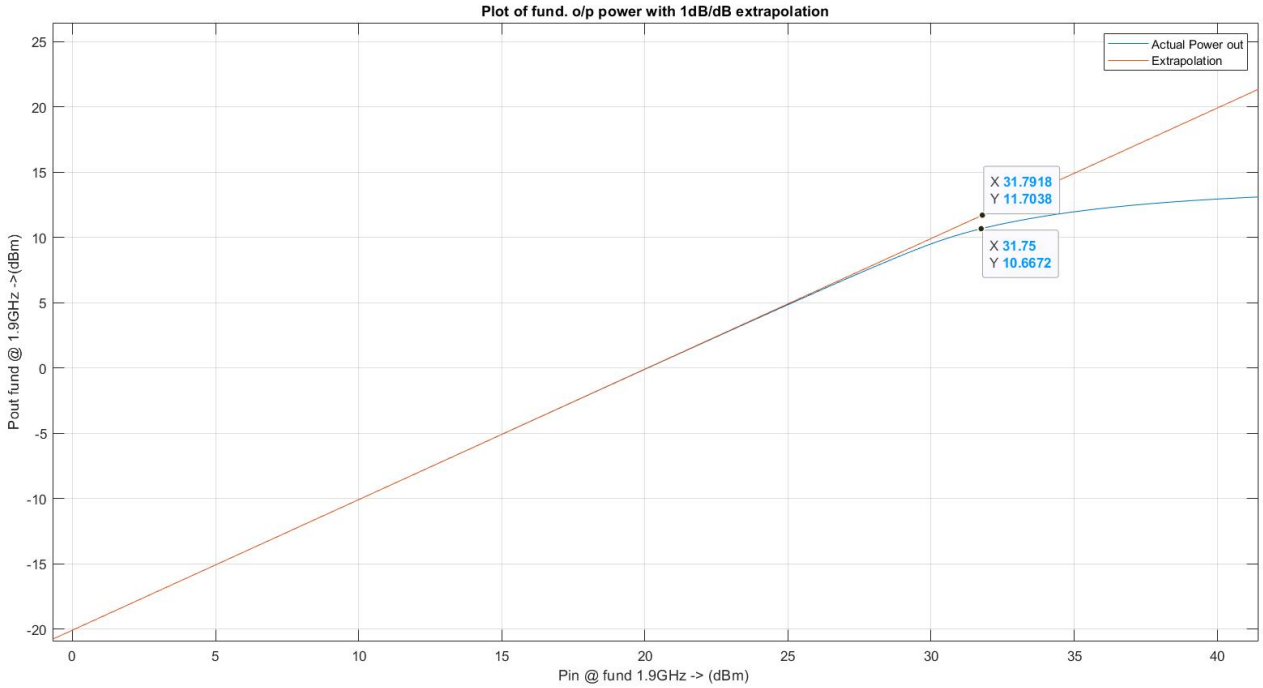


Figure 2: Plot of output power fundamental (1.9GHz) vs input power and 1dB point.

```
Gain in ratio form:
Voltage gain @ 1.9GHz: 18.81
Voltage gain @ 2GHz: 18.805
Voltage gain @ 2.1GHz: 18.71
```

The voltage gain is well above the specification over all specified frequencies 1.9GHz to 2.1GHz. As shown in the hand calculations, using the parasitic capacitance at M2 drain, the inductor value is calculated and we can also see the center frequency is also close to 2GHz. Parasitics may be varying with drain voltage and hence the frequency offset. This is fine since theres no gain flatness specification.

AM-PM deviation:

As for AM-PM deviation, the slightly increased current helps, but it's already met the specification with deviation less than 5 degrees at the specific

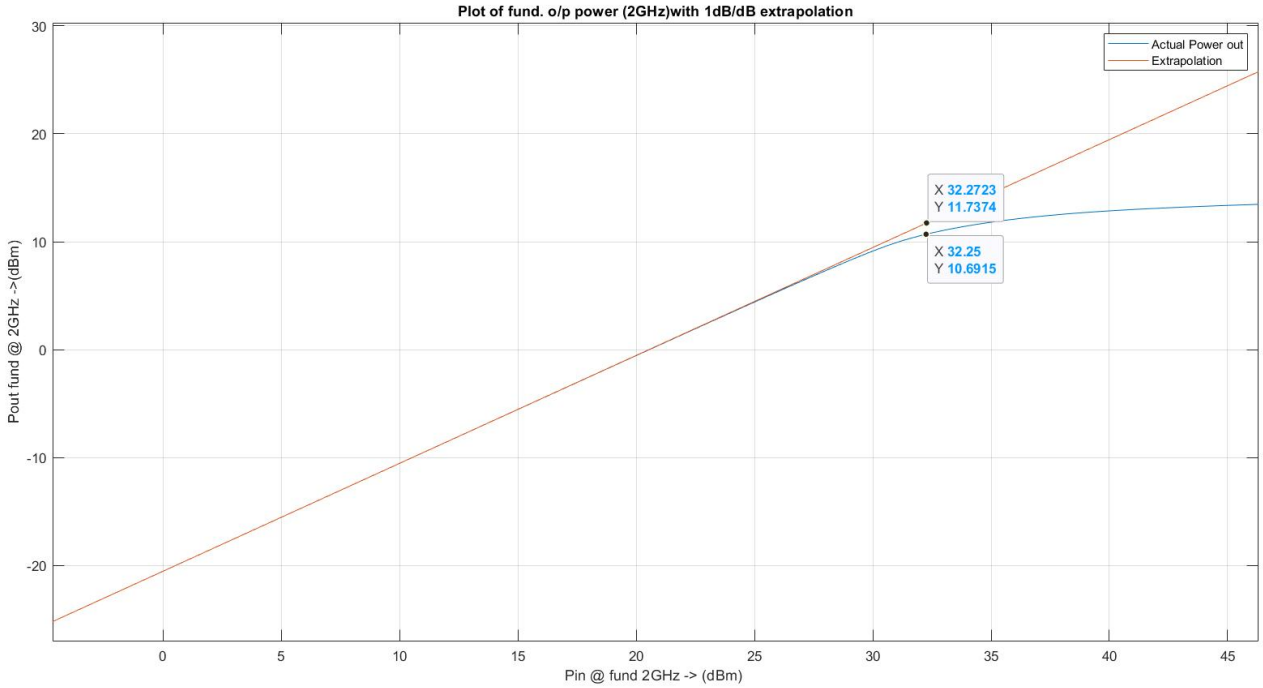


Figure 3: Plot of output power fundamental (2GHz) vs input power and 1dB point.

measured (via eldo commands) input P1dB power. Figs. 6,7 and 8 show the deviation at different operating frequencies.

```
Deviation @ f0 = 1.9GHz: 0.81 deg.
Deviation @ f0 = 2GHz: 0.6 deg.
Deviation @ f0 = 2.1GHz: 0.3 deg.
```

Power Consumption and current mirror bias:

As we have already discussed, the current bias is maintained close to 20mA to have low power. As for the current mirror bias, we use only 1mA to bias M3 and as shown in the hand calculations the width of M3 turns out to be 77.5um.

```
The total power consumption: 29.04mW
Power consumption without bias: 27.84mW
Power consumption by bias: 1.2mW
```

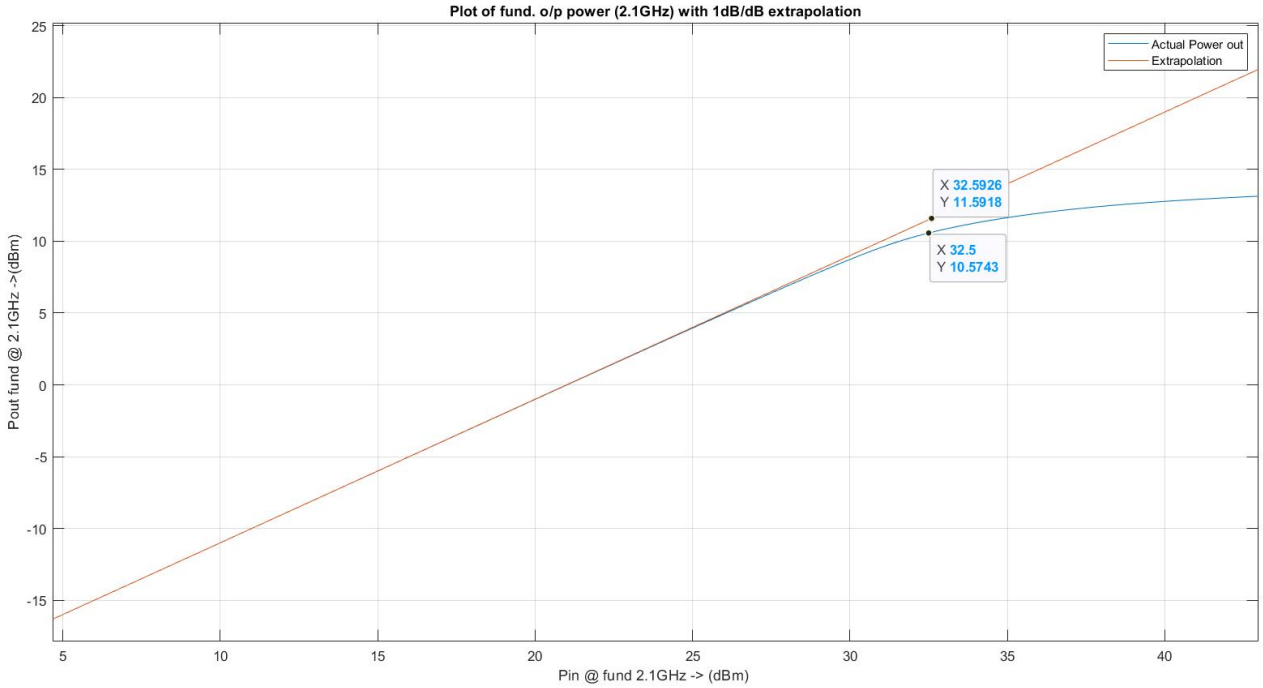


Figure 4: Plot of output power fundamental (2.1GHz) vs input power and 1dB point.

The proof of power consumption is as shown in fig. 9. The hand calculations verify what's measured for current mirror bias and the rest of the power amplifier circuit.

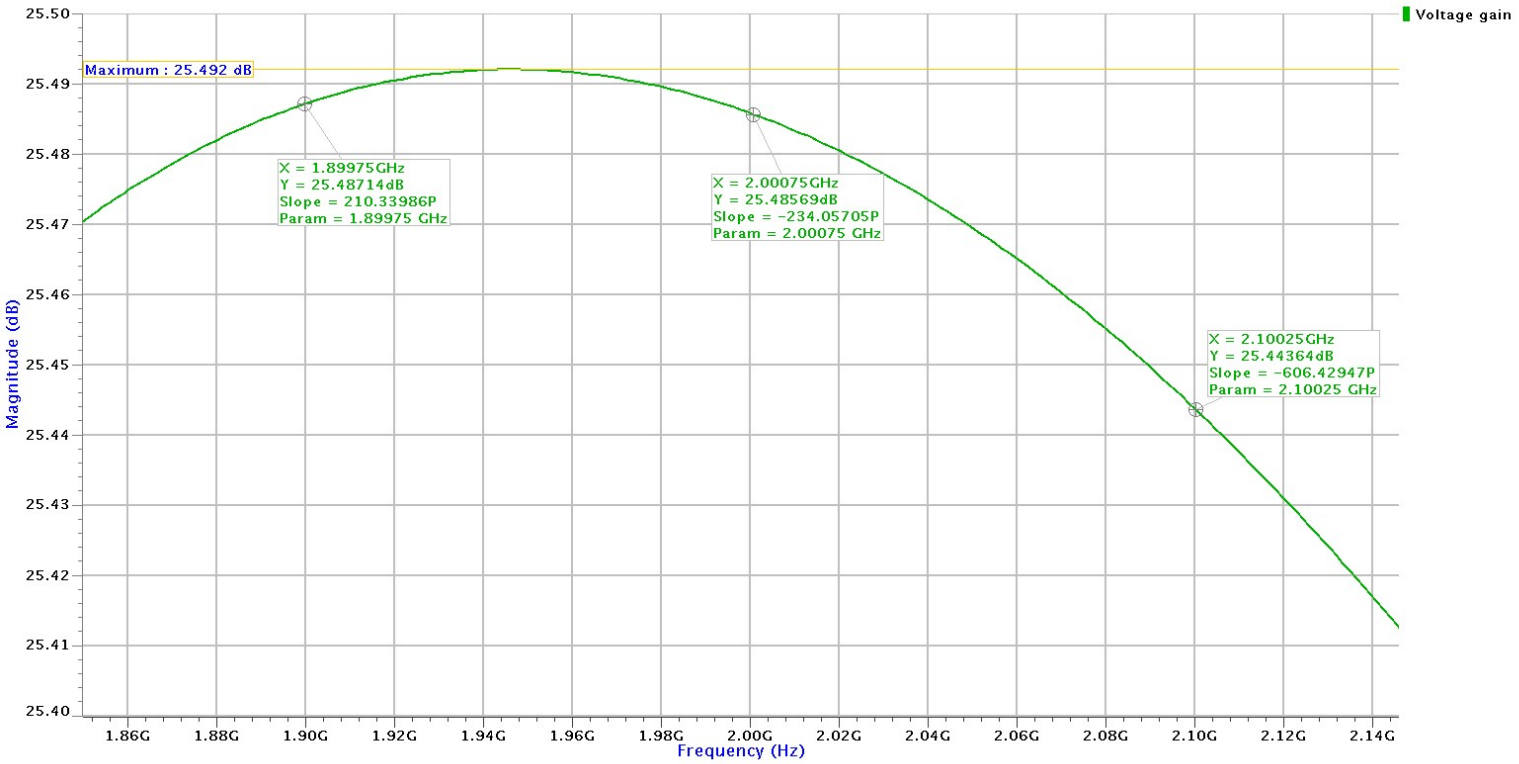


Figure 5: Plot of Voltage gain (in dB) from gate to drain at three frequencies including the maximum voltage gain.

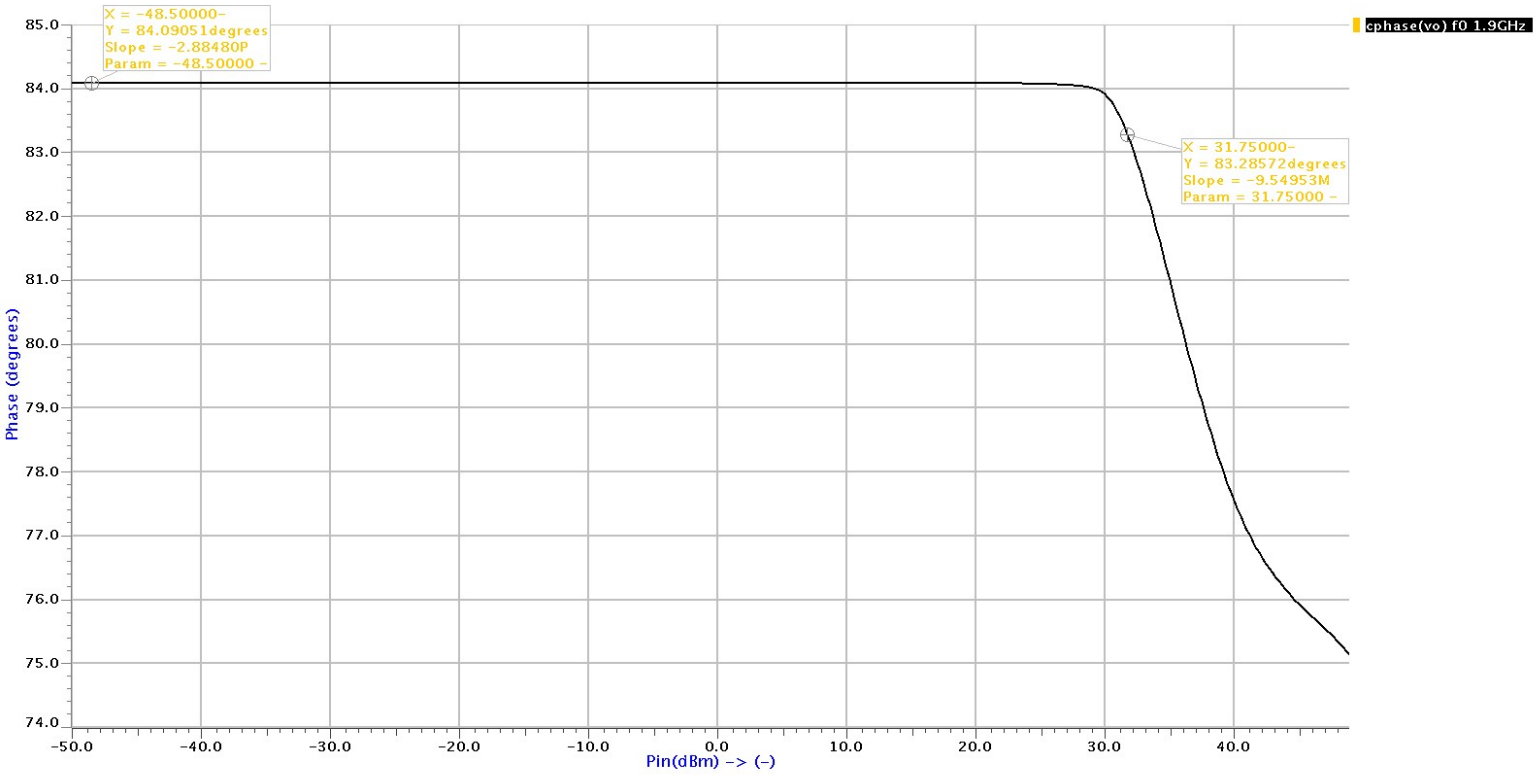


Figure 6: Plot of phase of output voltage vs input power at f0 = 1.9GHz. Power input 1dB = 31.75dBm

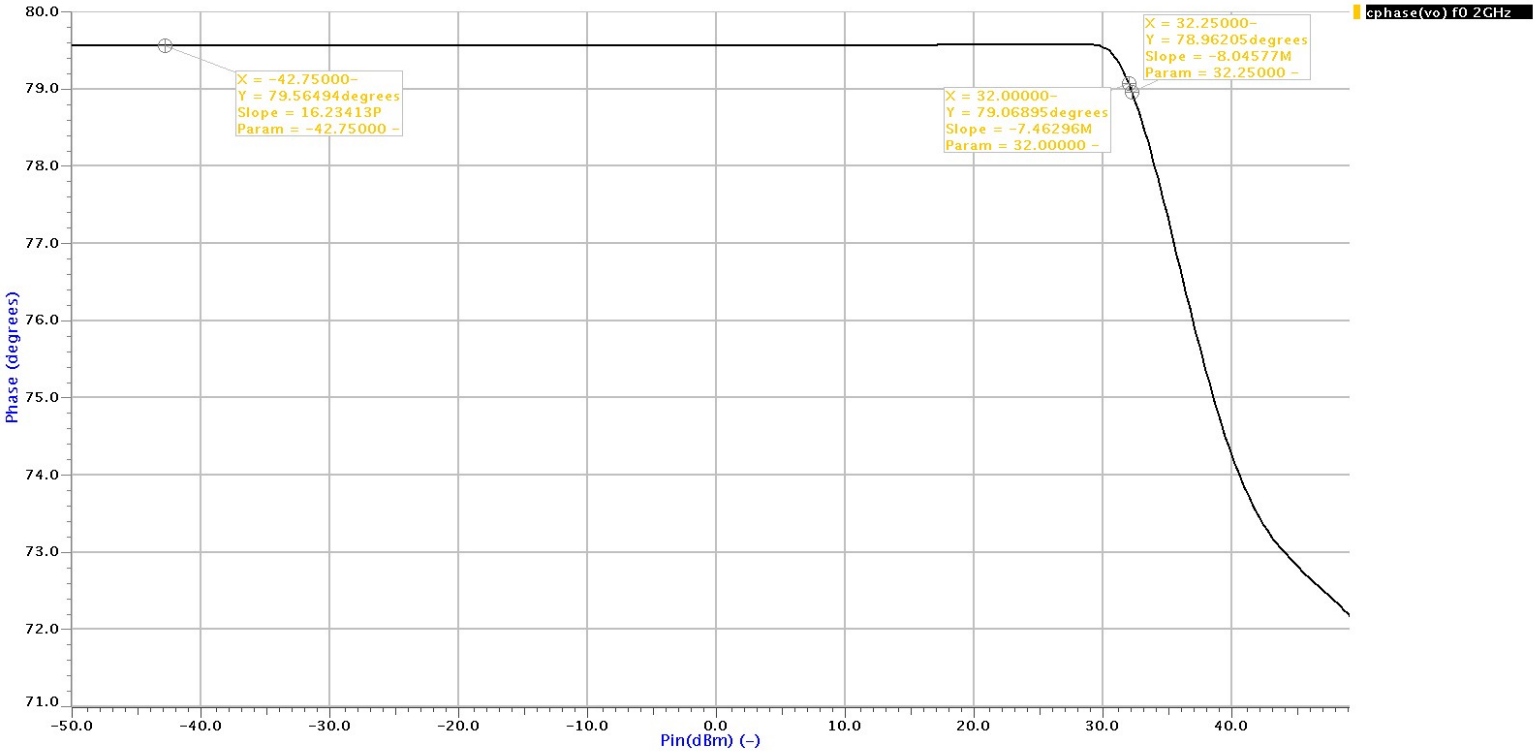


Figure 7: Plot of phase of output voltage vs input power at f0 = 2GHz. Power input 1dB = 32.25dBm

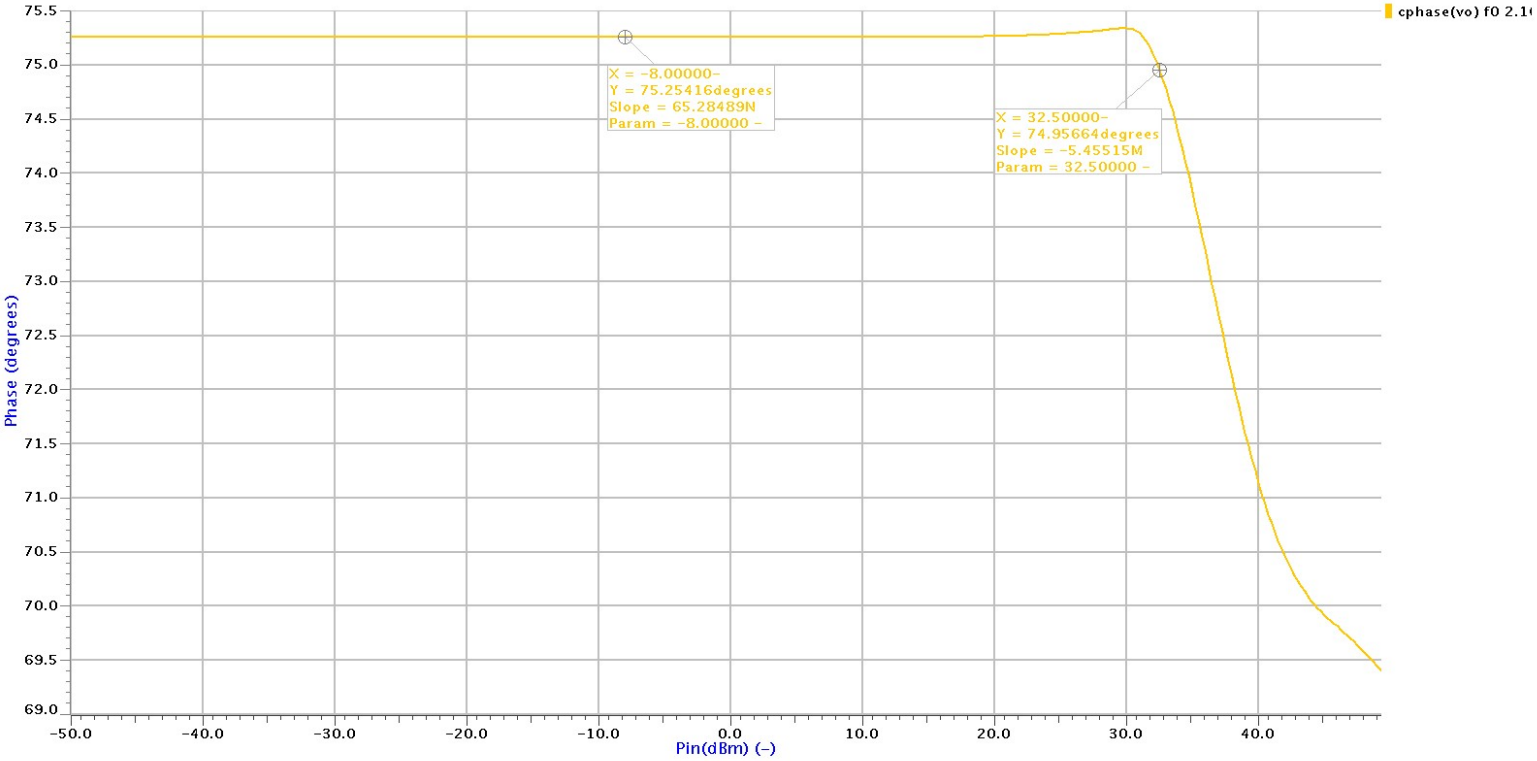


Figure 8: Plot of phase of output voltage vs input power at f0 = 2.1GHz. Power input 1dB = 32.5dBm

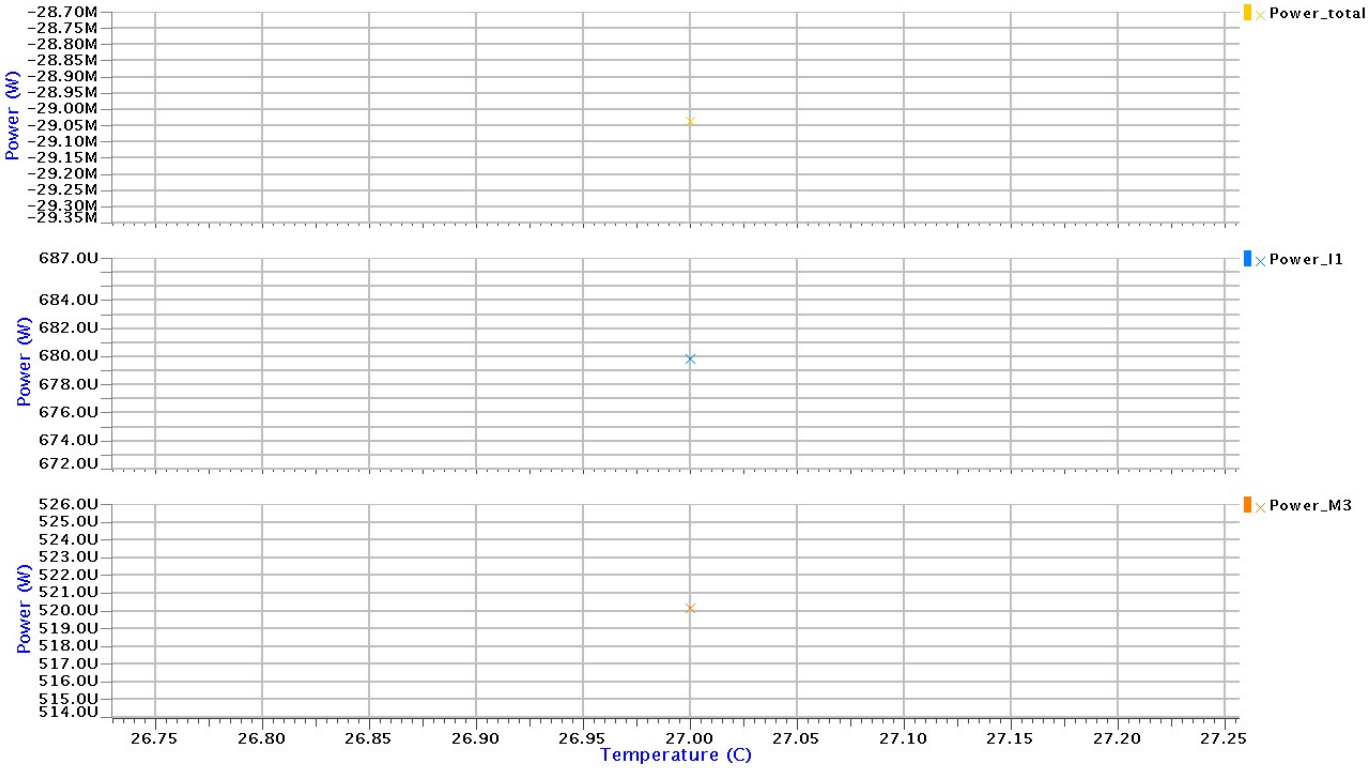
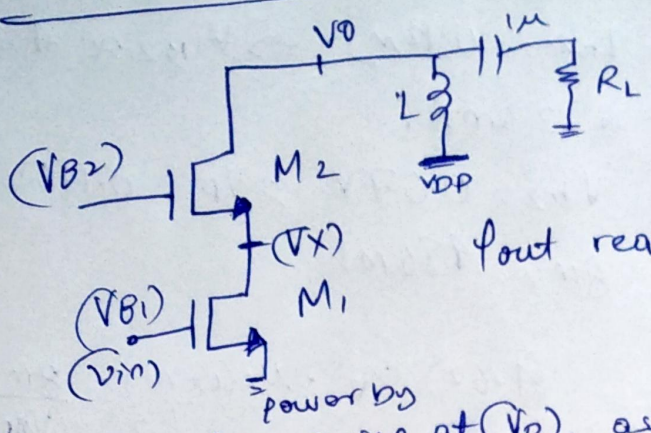


Figure 9: Total power consumed from VDD, power from current source and MOSFET M3 in current mirror.

Hand calculations - Power Amplifier

→ DC points, P1dB :-



→ Max swing at (V_o). assuming v_{in} is much smaller than V_o, $V_{Dsat\,1,2}$ is. $\frac{(V_{DD} - 2V_{Dsat})^2}{2R_L}$

P_{out} requirement (min) = +10dBm = 10mW

→ Because :- Assume M_1 is biased in edge of triode for max swing. $\therefore V_X \geq V_{Dsat\,1}$.

- Good design implies $V_{Dsat\,1} = V_{Dsat\,2}$.
- V_{B2}, V_{B1} - high enough for cutoff condn.
- $\therefore V_{o\,total} \geq 2V_{DS(sat)\,1,2}$. (neglecting small signal @ V_x assuming small v_{in})

So $V_{o\,swing\,max} = (V_{DD} - 2V_{Dsat})$

↳ From triode limit (1, 2) (M_1, M_2).

$\therefore \frac{(V_{DD} - 2V_{Dsat})^2}{2R_L} \geq P_{out\,min} = 10mW$

$R_L = 50\Omega$.

$\therefore$ **$V_{Dsat\,1,2} \leq 100mV$**

Cutoff condn : At this $P_{out\,(min)}$ $\left(\frac{i_d^2}{2} R_L\right) = 10mW$.

($i_d \leq I_{bias}$) for cutoff condn M_1, 2

From power req:,

$i_{d,swing\ ampl} = 20mA$

$\therefore$ **$I_{bias} \geq 20mA$**

Now, we choose a high enough width of 2800μ and start from there. $L = L_{min} = 0.12\mu$ $\Rightarrow V_{T,1,2} \approx 420mV$

→ Found out to be biased @ 23mA.

$V_{b1} = 0.52V$, $V_{b2} = 0.67V$. $\therefore V_{D1} = 0.195V$.

$g_{m1} = 462.45mS$ $g_{m2} = 486mS$.

$$\left(\mu_n C_{ox}\frac{W}{L}\right)_1 = \frac{(g_{m1})}{(V_{b1} - V_{T1})} = (4.62)(S/V); \left(\mu_n C_{ox}\frac{W}{L}\right)_2 = \frac{g_{m2}}{(V_{GS_2} - V_T)} = 8.82 S/V$$

$$I_{D1} = (g_{m1}) \times (0.5)(V_{OS1} - V_T)$$

$$= 0.5 \times (462.45) \times 10^{-3} (0.52 - 0.42)$$

$I_{D1} = 23.12mA$

(M)(1) verified

$I_{D2} = g_{m2} \times 0.5 (V_{OS_2} - V_T) \times (1 + \lambda V_{DS})$

Estimating 'λ'.

$(g_{os} = I_{bias} \cdot \lambda)$

$g_{os} = 18.5mS$

$I_{bias} = 23mA$

$\lambda = 0.78 (S/A)$

Now, $I_{D2} = g_{m2} \times 0.5 (V_{OS_2} - V_{T_2}) \times (1 + \lambda V_{DS_2})$

$= (486) \times 10^{-3} \times 0.5 (0.67 - 0.195 - 0.42)(1 + 0.78 \times (1.2 - 0.195))$

$I_{D2} = 23.84mA$ verified

So, both are in saturation in DC picture

$V_{Dsat1} = 64mV$ measured

$V_{Dsat2} = 52mV$

V_{Dsat1} calc $= (V_{OS} - V_{T_0}) \approx 0.100V$.

V_{Dsat2} calc $\approx .55mV$

Pidb :- We want $I_{bias} \geq 20mA$ → done, verified

$V_{Dsat1,2} < 100mV$ → done.

So, now we have required biasing to get good power.

$P_{out} = \left(\frac{I_{D2}^2 R_L}{2}\right)_{max}$ or $\frac{(V_{DD} - 2V_{Dsat})^2}{2R_L}$ → $[V_{Dsat1} + V_{Dsat2} \approx 155mV \text{ (calc)}]$

$= 13.46mW$ $= 10.92mW$

So by triode $(10.92mW = P_{out\,max})$ ✓

$P_{out\,max\,(linear)}$ from hand calc $= 10.38dBm$ ✓

and simulated is $\approx 10.6dBm = P_{1dB}$

Verified.

Voltage gain :-

Inductor calculations :- $= (g_{m1} R_L)_{at}$ $= (g_{m1})(R_{ind} \| R_L)$

$(L \in_{dbM2})\omega^2 = 1$ $= (g_{m1})(980\Omega \| 50\Omega)$

$(2\pi \times 2\times10^9)^2 \times L \times 1.2pF = 1$ $= (462mS) \times \left(\frac{1}{980} + \frac{1}{50}\right)^{-1}$

$= 5.28nH$ ✓ $= 21.98$

around 5.2nH (measured) ✓ $= 26.84dB$ ✓

The frequency (center) is also around 1.9GHz → 2GHz as in voltage gain graphs ✓

(Voltage gain hand calc) ✓

Measured = 25.49dB Verified

Current bias calc. & Total power :-

M_3 : $g_{m3} = 18.778mS$ $V_{T3} = 421mV$

$I_{D3} = 1mA$ $V_G = ?$

In saturation $(g_{m3}) \times (0.5)(V_{OS3} - V_{T3}) = I_{D3}$

For a width 77.5um $L = L_{min} = 0.12um$

$$V_{G3} = \frac{I_{D3}}{(g_{m3}\,0.5)} + V_{T3} = 0.528V$$

∴ Verified close to 0.52V @ V_{G1}.

Total power:- $(I_{bias} \times V_{DD}) + (V_{DD}) \times (1mA)$ (current mirror)

$\approx 29.04mW$

Measured total = 29.04mW

Measured I_1, M_3 current mirror = 0.680mW + 0.520mW

= 1.20mW

$= V_{DD} \times 1mA$

Hence, verified