
# EEE – 273, spring 2016

## Hierarchical Digital Design Methodology

## Term Project

Instructor: Dr. Behnam Arad

SUBMITTED BY:
Srinivas Srivasthava Balagowni(sbalagowni@gmail.com)
Bharghav Malla (mallabharghav@gmail.com)

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# Table of Content

*CSc/EEE 273*
*Term Project Status Report*
*Team #3*
*Date 05/04/2016*

| *Names* | *Signatures* | *Overall Grade* |
|---|---|---|
| *1)Srinivas srivasthava Balagowni* | | |
| *2)Bharghav Malla* | | |

Provide the required information as accurately as possible based on the status of your Floating Point ALU (FPALU) submitted on the due date. The completed form must appear after Table of Contents (TOC) in your report.

## I. Project Report / Demo / 200 points

**Table 1: (*To be filled by the instructor*)**

| Item in the report | Issues | points |
|---|---|---|
| Cover sheet | | |
| TOC | | |
| Project Status Report | | |
| Block diagrams for the DUT and Testbench | | |
| Source code | | |
| Test bench<br>• DUT instant<br>• FPALU Model<br>• Automated validation<br>• Simulation results (submitted as part of the softcopy only) | | |
| Synthesis<br>1. Script<br>2. Synthesis report<br>3. check_design report | | |
| | | |

| | | |
|---|---|---|
| Tabulated area and timing results | | |
| Synthesis reports | | |
| Code Coverage results | | |
| VALIDITY OF RESULTS IN THE REPORT | | |

## II.Design and Modeling Phase: /500 points

**Table 2. Source code**: Comment on the functionality of the source code you developed for each component of the FPALU as accurately as possible. The comments you provide here must be based on your simulation results. Add more rows as needed. (300 points)

| Component | Name of the person who modeled and validated the component | Is this component fully functional | If not, state any functional issue |
|---|---|---|---|
| Sequential multiplier | Srinivas & Bharghav | YES | |
| Normalization & Round Off | Srinivas | YES | |
| Input's FSM | Bharghav | YES | |
| Output FSM | Srinivas | YES | |
| Top_multiplication | Srinivas & Bharghav | YES | |
| Addition | Srinivas & Bharghav | YES | |
| FPALU_top | Bharghav & Srinivas | YES | |
| Automated_tb | Bharghav & Srinivas | YES | |
| Vector Generation | Bharghav | YES | |

**Table 3 Top-level Design.** Comment on the functionality of the FPALU you developed (The functionality of the top-level design). 200 points

| | |
|---|---|
| State functional issues in DUT | NONE |
| State functional issues in the testbench | NONE |

**Table 4. Code Coverage:** Fill the following table based on the coverage reports vcs generated for your FPALU design for applicable options.

| Coverage Type | Percentage | Comments if any |
|---|---|---|
| Line | 88.03 | |
| Toggle | 76.74 | |
| Conditional | 58.10 | |
| FSM | 50.53 | |

## III. Synthesis: 25 % ...../ 250 points

**Table 5.** Fill out the following table based on your best synthesis trials: timing & area. In each case, state the sign of the timing and area parameters as provided by the Design Compiler tool.

| Clock Period in ns | Area slack from area report | Timing slack from timing report | data required time for max path from timing report | data arrival time for the max path from timing report path |
|---|---|---|---|---|
| 5 | 382089.34 | 0.00 | 4.91 | 4.91 |
| | | | | |
| | | | | |

List any RTL changes you made to improve performance for each trial. Be very BRIEF!!
Trial 1:
Initially we used multiplication operator for multiplying two operands, but we faced timing issues. So we used sequential multiplier.

Trial 2:
Initially we used two's compliment for adding negative numbers but we though that it is the addition of only magnitudes. So we have considered addition and subtraction operators to perform signed addition.

Trial 3

## IV FPALU performance …….../50 points

1. How many clock cycles does your FPALU require for addition and multiplication?
   Addition:1 clock cycle
   Multiplication:pipelined-26 cycles to fill the pipeline and after that one output at each clock cycle.

2. What's the maximum clock rate your complete design can operate at?
   200MHz

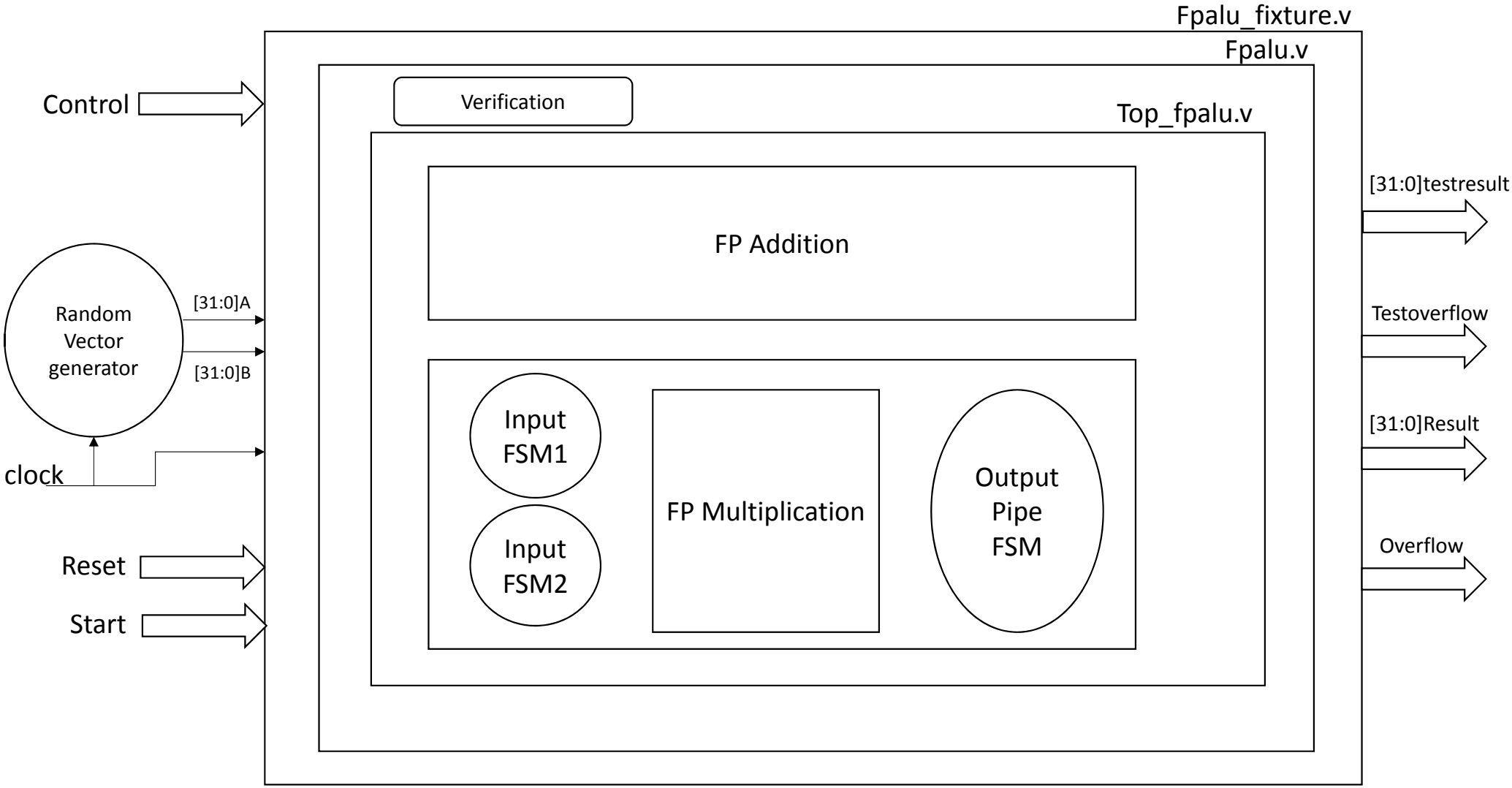
3. What is the maximum operation rate your design can sustain? (for example x multiplications per cycle)

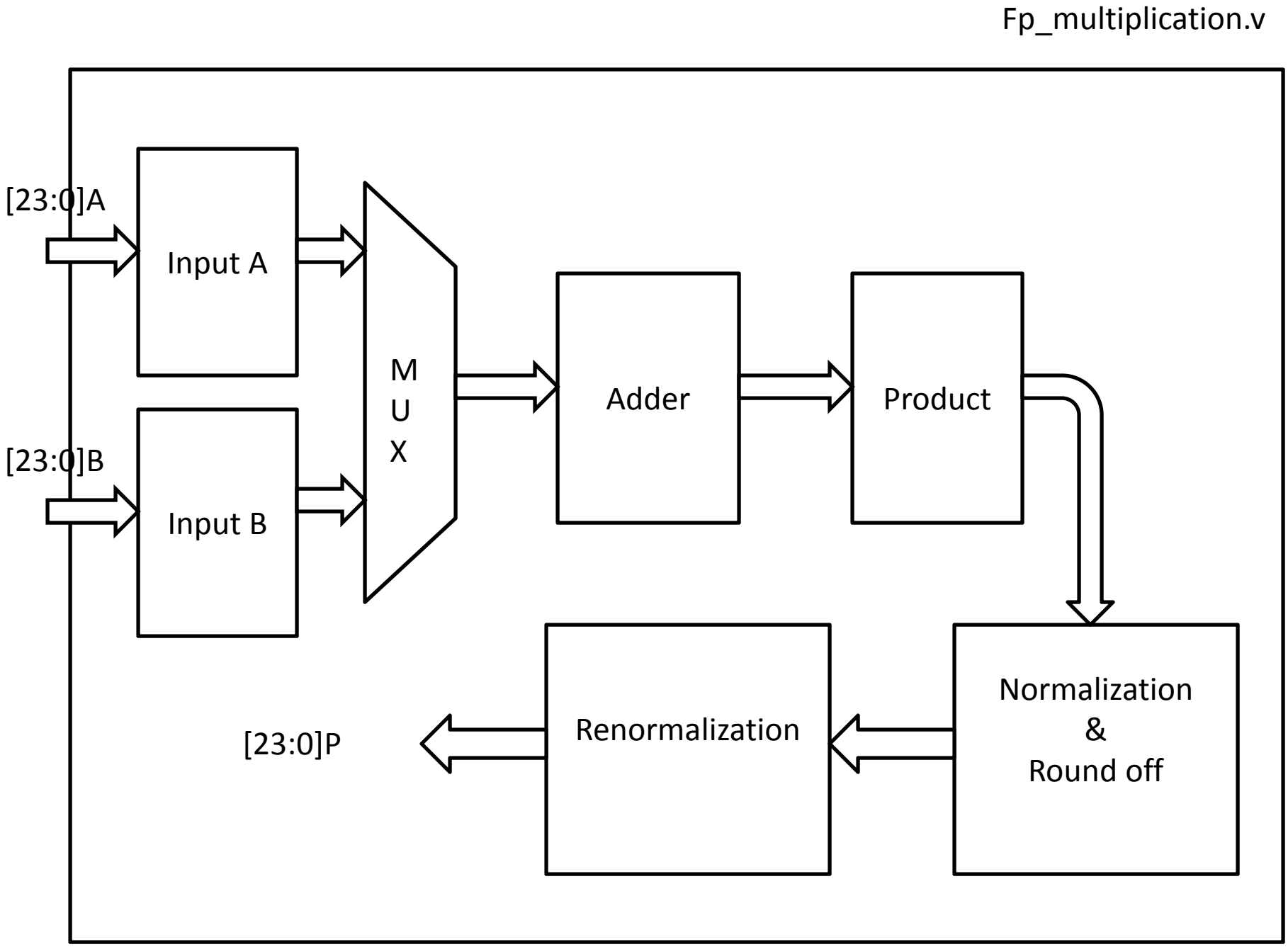
   26 cycles to fill the pipeline and after that one output at each clock cycle.(FSM based design which mimics pipelined)

**Tables 6**: For each partner, state the contribution percentage for each task listed below: Please only provide a percentage.

| Name | Design | Simulation | Synthesis | Project report |
|---|---|---|---|---|
| Srinivas Srivasthava Balagowni | 50% | 50% | 50% | 50% |
| Bharghav Malla | 50% | 50% | 50% | 50% |
| | | | | |

Feedback from the Instructor:


Fpalu_fixture.v
Fpalu.v
Control
Verification
Top_fpalu.v
FP Addition
[31:0]testresult
Random
Vector
generator
[31:0]A
[31:0]B
Testoverflow
Input
FSM1
FP Multiplication
Output
Pipe
FSM
[31:0]Result
clock
Input
FSM2
Overflow
Reset
Start


Fp_multiplication.v
[23:0]A
Input A
[23:0]B
Input B
M
U
X
Adder
Product
Normalization
&
Round off
Renormalization
[23:0]P

# SOURCE CODES

```
module vector_gn();

integer A,B;

integer i,j;

initial
begin

A=$fopen("filea.txt","w");

for (i=0;i<400;i=i+1)

begin

$fdisplay(A,"%h",$random());

end
$fclose (A);
end


initial
begin

B=$fopen("fileb.txt","w");

for (i=0;i<400;i=i+1)

begin

$fdisplay(B,"%h",$random());

end
$fclose (B);
end

endmodule
```

```
`include "fpalu.v"
module fpalu_fixture;

reg [31:0] A,B;
reg reset,start,control,clk;
wire [31:0]result,testresult;
wire overflow,testoverflow;
reg [31:0]mema[399:0];
reg [31:0]memb[399:0];
reg [32:0]result_mem[399:0];
reg [32:0]verify_mem[399:0];
integer i=0;
integer j=0,q=0,q1=1,k=0,f=0;
reg [10:0]l,z;
reg pass,fail;


integer c,d;


initial
$vcdpluson ;
initial
$monitor($time , "clk=%b A=%h B=%h control=%b result=%h overflow=%b testresult=%h
testoverflow=%b  pass=%b fail=%b",clk,
A,B,control,result,overflow,testresult,testoverflow,pass,fail);



fpalu uut(A,B,start,clk,reset,control,result,overflow,testresult,testoverflow);

initial clk=0;
always #10 clk=~clk;



initial
begin
$readmemh("filea.txt",mema);
$readmemh("fileb.txt",memb);
end


initial
begin
        z=0; l=0;pass=1'b0;fail=1'b0;reset=0; start=1'b0; control=1'b1;
#40     reset=1; start=1; control=1;
#1000   reset=1; start=1; control=0;
#1000;

end

always @ (negedge clk)
begin
  A=mema[i];
 i=i+1;
  B=memb[j];
 j=j+1;
end

always @ (posedge clk)
begin
f=f+1;
```

```
end

always @ (posedge clk)
begin
if (f < 29)
begin
pass=1'b0;
fail=1'b0;
end
else if((result_mem[k+27]==verify_mem[k+1]) && (control==1'b1))
begin
pass=1'b1;
fail=1'b0;
k=k+1;
end
else if((result_mem[k]==verify_mem[k]) && (control==1'b0))
begin
pass=1'b0;
fail=1'b1;
k=k+1;
end
end


always @ (posedge clk)
begin
result_mem[l]={result,overflow};
l=l+1;
end


always @ (negedge clk)
begin
verify_mem[z]={testresult,testoverflow};
z=z+1;
end


always @ (*)
begin
if(l==150 )
begin
c=$fopen("filer.txt","w");
for (q=0;q<=150;q=q+1)
begin
$fdisplay(c,"%h",result_mem[q]);
end
end
$fclose (c);
end


always @ (*)
begin
if(z==150)
begin
d=$fopen("filev.txt","w");
for (q1=0;q1<=150;q1=q1+1)
begin
$fdisplay(d,"%h",verify_mem[q1]);
end
end
$fclose (d);
```

```
end


initial
  #3500 $finish;


endmodule
```

```
`include "fpalu_verification.v"
`include "top_fpalu.v"

module fpalu(A,B,start,clk,reset,control,result,overflow,testresult,testoverflow);
input [31:0]A,B;
input start,clk,reset,control;
output [31:0]result,testresult;
output overflow,testoverflow;

top_fpalu u1(A,B,start,clk,reset,control,result,overflow);
fpalu_verification u2(A,B,start,clk,reset,control,testresult,testoverflow);

endmodule
```

```
`include "fp_addition.v"
`include "fp_multiplication.v"

module top_fpalu(A,B,start,clk,reset,control,result,overflow);
input [31:0]A,B;
input start,control,reset,clk;
output [31:0]result;
output overflow;
reg [31:0]result;
reg overflow;
reg start1,start2;
wire [31:0]result1,result2;
wire overflow1,overflow2;
reg [1:0]cs,ns;
parameter s0=2'b00, s1=2'b01, s2=2'b10;

always @ (posedge clk or negedge reset)
begin
 if (~reset)
  begin
   cs<=s0;
  end
 else if(start==1)
  cs<=ns;
end

always @ (*)
begin
 case (cs)
  s0: begin
       if( control==1'b1)
        ns=s1;
       else if(control==1'b0)
        ns=s2;
       else
        ns=s0;
      end

  s1:begin
      if(control==1'b0)
       ns=s2;
      else
       ns=s1;
     end
  s2:begin
      if(control==1'b1)
       ns=s1;
      else
       ns=s2;
     end
 endcase
end


always @ (*)
begin
 case(cs)
  s0:begin
      if (reset==0)
       begin
        start1=1'b0;
        start2=1'b0;
        result=32'b0;
```

```
      overflow=1'b0;
     end
    else if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
    else
     begin
      start1=1'b0;
      start2=1'b0;
      result=32'b0;
      overflow=1'b0;
     end
   end
s1:begin
    if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
    else
     begin
      start1=1'b0;
      start2=1'b0;
      result=32'b0;
      overflow=1'b0;
     end
   end

s2:begin
    if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
```

```
      else
       begin
        start1=1'b0;
        start2=1'b0;
        result=32'b0;
        overflow=1'b0;
       end
     end
 endcase
end

fp_multiplication uut1(A,B,start1,reset,clk,result1,overflow1);
fp_addition uut(A,B, reset,start2, result2, overflow2);

endmodule
```

# FLOATING POINT MULTIPLICATION

```
module
fp_multiplication_input_pipe1(A,B,clk,start,reset,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,
p11,p12,p13,q0,q1,q2,q3,q4,q5,q6,q7,q8,q9,q10,q11,q12,q13,start0,start1,start2,start
3,start4,start5,start6,start7,start8,start9,start10,start11,start12,start13);
input [31:0]A,B;
input clk,reset,start;
output
[31:0]p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,q0,q1,q2,q3,q4,q5,q6,q7,q8,q9,q1
0,q11,q12,q13;
output
start0,start1,start2,start3,start4,start5,start6,start7,start8,start9,start10,start1
1,start12,start13;
reg
start0,start1,start2,start3,start4,start5,start6,start7,start8,start9,start10,start1
1,start12,start13;
reg
[31:0]p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,q0,q1,q2,q3,q4,q5,q6,q7,q8,q9,q1
0,q11,q12,q13;
reg [5:0]cs,ns;

parameter
st0=6'b000000,st1=6'b000001,st2=6'b000010,st3=6'b000011,st4=6'b000100,st5=6'b000101,
st6=6'b000111,st7=6'b001000,st8=6'b001001,st9=6'b001010,st10=6'b001011,st11=6'b00110
0,st12=6'b001101,st13=6'b001110,sidle=6'b001111,st14=6'b010000,st15=6'b010001,
st16=6'b010010,
st17=6'b010011,
st18=6'b010100,
st19=6'b010101,
st20=6'b010110,
st21=6'b010111,
st22=6'b011000,
st23=6'b011001,
st24=6'b011010,
st25=6'b011011,
st26=6'b011100;


always @ (posedge clk or negedge reset)
begin
 if(reset==0)
  begin
   cs<=sidle;
  end
 else if(start==1)
   cs<=ns;
end

always @ (cs)
begin
 case(cs)
  sidle:ns=st0;
  st0: ns=st1;
  st1: ns=st2;
  st2: ns=st3;
  st3: ns=st4;
  st4: ns=st5;
  st5: ns=st6;
  st6: ns=st7;
  st7: ns=st8;
  st8: ns=st9;
  st9: ns=st10;
  st10: ns=st11;
  st11: ns=st12;
```

```
  st12: ns=st13;
  st13: ns=st14;
  st14: ns=st15;
  st15: ns=st16;
  st16: ns=st17;
  st17: ns=st18;
  st18: ns=st19;
  st19: ns=st20;
  st20: ns=st21;
  st21: ns=st22;
  st22: ns=st23;
  st23: ns=st24;
  st24: ns=st25;
  st25: ns=st26;
  st26: ns=sidle;
 endcase
end

always @ (*)
begin
 case(cs)
  sidle: begin
          if(~reset)
           begin
            p0=32'b0;
            p1=32'b0;
            p2=32'b0;
            p3=32'b0;
            p4=32'b0;
            p5=32'b0;
            p6=32'b0;
            p7=32'b0;
            p8=32'b0;
            p9=32'b0;
           p10=32'b0;
           p11=32'b0;
           p12=32'b0;
           p13=32'b0;
            q0=32'b0;
            q1=32'b0;
            q2=32'b0;
            q3=32'b0;
            q4=32'b0;
            q5=32'b0;
            q6=32'b0;
            q7=32'b0;
            q8=32'b0;
            q9=32'b0;
           q10=32'b0;
           q11=32'b0;
           q12=32'b0;
           q13=32'b0;
          end
         else if(start==1)
          begin
           start0=start0;
           p0=p0;
           q0=q0;
          end
         end

  st13:begin
        if(start==1)
```

```
       begin
        start0=1;
        p0=A;
        q0=B;
       end
     end
st14:begin
      if(start==1)
       begin
        start1=1;
        p1=A;
        q1=B;
       end
     end
st15:begin
      if(start==1)
       begin
        start2=1;
        p2=A;
        q2=B;
       end
     end
st16:begin
      if(start==1)
       begin
        start3=1;
        p3=A;
        q3=B;
       end
     end
st17:begin
      if(start==1)
       begin
        start4=1;
        p4=A;
        q4=B;
       end
     end
st18:begin
      if(start==1)
       begin
        start5=1;
        p5=A;
        q5=B;
       end
     end
st19:begin
      if(start==1)
       begin
        start6=1;
        p6=A;
        q6=B;
       end
     end
st20:begin
      if(start==1)
       begin
        start7=1;
        p7=A;
        q7=B;
       end
     end
st21:begin
```

```
      if(start==1)
       begin
        start8=1;
        p8=A;
        q8=B;
       end
     end
st22:begin
      if(start==1)
       begin
        start9=1;
        p9=A;
        q9=B;
       end
     end
st23:begin
      if(start==1)
       begin
        start10=1;
        p10=A;
        q10=B;
       end
     end
st24:begin
      if(start==1)
       begin
        start11=1;
        p11=A;
        q11=B;
       end
     end
st25:begin
      if(start==1)
       begin
        start12=1;
        p12=A;
        q12=B;
       end
     end
st26:begin
      if(start==1)
       begin
        start13=1;
        p13=A;
        q13=B;
       end
     end
default:begin
         p0=p0;
         p1=p1;
         p2=p2;
         p3=p3;
         p4=p4;
         p5=p5;
         p6=p6;
         p7=p7;
         p8=p8;
         p9=p9;
         p10=p10;
         p11=p11;
         p12=p12;
         p13=p13;
         q0=q0;
```

```
            q1=q1;
            q2=q2;
            q3=q3;
            q4=q4;
            q5=q5;
            q6=q6;
            q7=q7;
            q8=q8;
            q9=q9;
            q10=q10;
            q11=q11;
            q12=q12;
            q13=q13;
           end
 endcase
end
endmodule
```

```
module
fp_multiplication_input_pipe2(A,B,clk,start,reset,m0,m1,m2,m3,m4,m5,m6,m7,m8,m9,m10,
m11,m12,m13,n0,n1,n2,n3,n4,n5,n6,n7,n8,n9,n10,n11,n12,n13,s0,s1,s2,s3,s4,s5,s6,s7,s8
,s9,s10,s11,s12,s13);
input [31:0]A,B;
input clk,reset,start;
output
[31:0]m0,m1,m2,m3,m4,m5,m6,m7,m8,m9,m10,m11,m12,m13,n0,n1,n2,n3,n4,n5,n6,n7,n8,n9,n1
0,n11,n12,n13;
output s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s12,s13,s11;
reg s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s12,s13,s11;
reg
[31:0]m0,m1,m2,m3,m4,m5,m6,m7,m8,m9,m10,m11,m12,m13,n0,n1,n2,n3,n4,n5,n6,n7,n8,n9,n1
0,n11,n12,n13;
reg [5:0]cs,ns;

parameter
st0=6'b000000,st1=6'b000001,st2=6'b000010,st3=6'b000011,st4=6'b000100,st5=6'b000101,
st6=6'b000111,st7=6'b001000,st8=6'b001001,st9=6'b001010,st10=6'b001011,st11=6'b00110
0,st12=6'b001101,st13=6'b001110,sidle=6'b001111,st14=6'b010000,st15=6'b010001,
st16=6'b010010,
st17=6'b010011,
st18=6'b010100,
st19=6'b010101,
st20=6'b010110,
st21=6'b010111,
st22=6'b011000,
st23=6'b011001,
st24=6'b011010,
st25=6'b011011,
st26=6'b011100;


always @ (posedge clk or negedge reset)
begin
 if(reset==0)
  begin
   cs<=sidle;
  end
 else if(start==1)
   cs<=ns;
end

always @ (cs)
begin
 case(cs)
  sidle:ns=st0;
  st0: ns=st1;
  st1: ns=st2;
  st2: ns=st3;
  st3: ns=st4;
  st4: ns=st5;
  st5: ns=st6;
  st6: ns=st7;
  st7: ns=st8;
  st8: ns=st9;
  st9: ns=st10;
  st10: ns=st11;
  st11: ns=st12;
  st12: ns=st13;
  st13: ns=st14;
  st14: ns=st15;
  st15: ns=st16;
```

```
  st16: ns=st17;
  st17: ns=st18;
  st18: ns=st19;
  st19: ns=st20;
  st20: ns=st21;
  st21: ns=st22;
  st22: ns=st23;
  st23: ns=st24;
  st24: ns=st25;
  st25: ns=st26;
  st26: ns=sidle;
 endcase
end

always @ (*)
begin
 case(cs)
  sidle: begin
          if(~reset)
           begin
            m0=32'b0;
            m1=32'b0;
            m2=32'b0;
            m3=32'b0;
            m4=32'b0;
            m5=32'b0;
            m6=32'b0;
            m7=32'b0;
            m8=32'b0;
            m9=32'b0;
           m10=32'b0;
           m11=32'b0;
           m12=32'b0;
           m13=32'b0;
            n0=32'b0;
            n1=32'b0;
            n2=32'b0;
            n3=32'b0;
            n4=32'b0;
            n5=32'b0;
            n6=32'b0;
            n7=32'b0;
            n8=32'b0;
            n9=32'b0;
           n10=32'b0;
           n11=32'b0;
           n12=32'b0;
           n13=32'b0;
          end
         else if(start==1)
          begin
           s0=1;
           m0=A;
           n0=B;
          end
        end
  st0:begin
       if(start==1)
        begin
         s1=1;
         m1=A;
         n1=B;
        end
```

```
    end
st1:begin
     if(start==1)
      begin
       s2=1;
       m2=A;
       n2=B;
      end
    end
st2:begin
     if(start==1)
      begin
       s3=1;
       m3=A;
       n3=B;
      end
    end
st3:begin
     if(start==1)
      begin
       s4=1;
       m4=A;
       n4=B;
      end
    end
st4:begin
     if(start==1)
      begin
       s5=1;
       m5=A;
       n5=B;
      end
    end
st5:begin
     if(start==1)
      begin
       s6=1;
       m6=A;
       n6=B;
      end
    end
st6:begin
     if(start==1)
      begin
       s7=1;
       m7=A;
       n7=B;
      end
    end
st7:begin
     if(start==1)
      begin
       s8=1;
       m8=A;
       n8=B;
      end
    end
st8:begin
     if(start==1)
      begin
       s9=1;
       m9=A;
       n9=B;
```

```
      end
    end
st9:begin
     if(start==1)
      begin
       s10=1;
       m10=A;
       n10=B;
      end
    end
st10:begin
      if(start==1)
       begin
        s11=1;
        m11=A;
        n11=B;
       end
     end
st11:begin
      if(start==1)
       begin
        s12=1;
        m12=A;
        n12=B;
       end
     end
st12:begin
      if(start==1)
       begin
        s13=1;
        m13=A;
        n13=B;
       end
     end
default:
       begin
          m0=m0;
          m1=m1;
          m2=m2;
          m3=m3;
          m4=m4;
          m5=m5;
          m6=m6;
          m7=m7;
          m8=m8;
          m9=m9;
        m10=m10;
        m11=m11;
        m12=m12;
        m13=m13;
          n0=n0;
          n1=n1;
          n2=n2;
          n3=n3;
          n4=n4;
          n5=n5;
          n6=n6;
          n7=n7;
          n8=n8;
          n9=n9;
        n10=n10;
        n11=n11;
        n12=n12;
```

```
          n13=n13;
        end
 endcase
end
endmodule
```

```
module dffa(clk,reset,load,da,qa);
input clk,reset,load;
input [23:0] da;
output [23:0] qa;
reg [23:0] qa;

always@(posedge clk or negedge reset)
begin
 if(~reset)
  qa <=24'b0;
 else if (load)
  qa<=da;
 else
  qa<=qa;
end
endmodule
```

```
module dffb(clk,reset,load,shift,db,qb,s);
input clk,reset,load,shift;
input [23:0] db;
output [23:0] qb;
reg [23:0] qb;
output s;
reg s;

always@(posedge clk or negedge reset)
begin
 if (reset == 0)
  begin
   s<=1'b0;
   qb <=24'b0;
  end
 else if (load==1)
   qb<=db;
 else if(shift==1)
  begin
   qb<={1'b0,qb[23:1]};
   s<=qb[0];
  end
 else
  begin
   qb<=qb;
   s<=s;
  end
end
endmodule
```

```
module mux(da,s,y);
input [23:0]da;
input s;
output [23:0] y;
reg [23:0]y;
wire [23:0]d0;
assign d0=24'b0;
always@(da or d0 or s)
begin
 if(s)
  y=da;
 else
  y=d0;
end
endmodule
```

```
module adder(a,b,cout,sum);
        input [23:0]a;
        input [23:0]b;
        output cout;
        output [23:0]sum;
assign {cout,sum}=a+b;
endmodule
```

```
module finalshift(sum,shiftp,cout,shiftph,shift,load,clock,reset);
input [23:0]sum;
input reset,clock,shift,load,cout;
output [23:0]shiftph;
output [23:0]shiftp;
reg [23:0]shiftph;
reg [23:0]shiftp;

always @(posedge clock or negedge reset)
begin
 if(reset==0)
  begin
   shiftp<=24'b0;
   shiftph<=24'b0;
  end
 else if(shift==1)
  begin
   shiftp<={cout,sum[23:1]};
   shiftph[23]<=sum[0];
   shiftph[22:0]<=shiftph[23:1];
  end
 else
  begin
   shiftp<=shiftp;
   shiftph<=shiftph;
  end
end
endmodule
```

```
`include "dffa.v"
`include "dffb.v"
`include "mux.v"
`include "finalshift.v"
`include "adder.v"


module multiplication(a,b,reset,shift,clk,p,load);
input [23:0]a,b;
input reset,shift,clk,load;
output [47:0]p;
reg [47:0]p;
wire [23:0]shiftp,shiftph;
wire s,cout;
wire [23:0]qa,adderinput,sum,qb;

dffa a1(clk,reset,load,a,qa);

dffb b1(clk,reset,load,shift,b,qb,s);

mux m1(qa,s,adderinput);

finalshift f1(sum,shiftp,cout,shiftph,shift,load,clk,reset);

adder a2(shiftp[23:0],adderinput,cout,sum);

always @ (*)
begin
 p={shiftp[23:0],shiftph[23:0]};
end
endmodule
```

```
module fsm_multiplication(clk,reset,load,shift,start);
input clk, reset,start;
output load,shift;
reg load,shift;
reg [4:0]cs,ns;
parameter
idle=5'b00000,s1=5'b00001,s2=5'b00010,s3=5'b00011,s4=5'b00100,s5=5'b00101,s6=5'b0011
0,s7=5'b00111,s8=5'b01000,s9=5'b01001,s10=5'b01010,s11=5'b01011,s12=5'b01100,s13=5'b
01101,s14=5'b01110,s15=5'b01111,s16=5'b10000,
s17=5'b10001,s18=5'b10010,s19=5'b10011,s20=5'b10100,s21=5'b10101,s22=5'b10110,s23=5'
b10111,s24=5'b11000,s25=5'b11001,s26=5'b11010,s27=5'b11011;

always@(posedge clk or negedge reset)
begin
 if(reset==0)
  cs<=idle;
 else
  cs<=ns;
end

always@ (*)
begin
 case(cs)
  idle:  ns=s1;
  s1  : if (start==1)
          ns=s2;
        else
          ns=idle;
  s2   :  ns=s3;
  s3   :  ns=s4;
  s4   :  ns=s5;
  s5   :  ns=s6;
  s6   :  ns=s8;
  s8   :  ns=s9;
  s9   :  ns=s10;
  s10  :  ns=s11;
  s11  :  ns=s12;
  s12  :  ns=s13;
  s13  :  ns=s14;
  s14  :  ns=s15;
  s15  :  ns=s16;
  s16  :  ns=s17;
  s17  :  ns=s18;
  s18  :  ns=s19;
  s19  :  ns=s20;
  s20  :  ns=s21;
  s21  :  ns=s22;
  s22  :  ns=s23;
  s23  :  ns=s24;
  s24  :  ns=s25;
  s25  :  ns=s26;
  s26  :  ns=s27;
  s27  :  ns=s7;
  s7   :  ns=s7;
  default  :  ns=idle;
 endcase
end

always @ (cs)
begin
 case(cs)
  idle :
         begin
```

```
        load=0; shift=0;
       end
s1   :
       begin
        if(start==1)
         begin
          load=1; shift=0;
         end
        else
         begin
          load=0;shift=0;
         end
       end
s2   :
        begin
         load=0; shift=1;
        end
s3   :
        begin
         load=0; shift=1;
        end
s4   :
        begin
         load=0; shift=1;
        end
s5   :
        begin
         load=0; shift=1;
        end
s6:
        begin
         load=0; shift=1;
        end
s8:
        begin
         load=0; shift=1;
        end
s9:
        begin
         load=0; shift=1;
        end
s10:
        begin
        load=0; shift=1;
        end
s11:
        begin
         load=0; shift=1;
        end
s12:
        begin
         load=0; shift=1;
        end
s13:
        begin
         load=0; shift=1;
        end
s14:
        begin
         load=0; shift=1;
        end
s15:
        begin
```

```
          load=0; shift=1;
         end
  s16:
         begin
          load=0; shift=1;
         end
  s17:
         begin
          load=0; shift=1;
         end
  s18:
         begin
          load=0; shift=1;
         end
  s19:
         begin
          load=0; shift=1;
         end
  s20:
         begin
          load=0; shift=1;
         end
  s21:
         begin
          load=0; shift=1;
         end
  s22:
         begin
          load=0; shift=1;
         end
  s23:
         begin
          load=0; shift=1;
         end
  s24:
         begin
          load=0; shift=1;
         end
  s25:
         begin
          load=0; shift=1;
         end
  s26:
         begin
          load=0; shift=1;
         end
  s27:
         begin
          load=0; shift=1;
         end
  s7:
         begin
          load=0; shift=0;
         end
  default:begin
          load=0;shift=0;
         end
 endcase
end
endmodule
```

```
`include "fsm_multiplication.v"
`include "multiplication.v"


module fp_multiplication_prenormalization(a,b,reset,clk,p,start,out,expo);
input [23:0]a,b;
input reset,clk,start;
output [47:0]p;
output [24:0]out;
output expo;
reg [24:0]out;
reg expo;
wire load,shift;

fsm_multiplication t1(clk,reset,load,shift,start);
multiplication t2(a,b,reset,shift,clk,p,load);

always @ (*)
begin
 if(p[47]==0 && p[22]==1)
  begin
   {out[24],out[23:0]}={1'b1,p[45:23]}+1'b1;
   expo=1'b0;
  end
 else if(p[47]==0 && p[22]==0)
  begin
   {out[24],out[23:0]}={1'b1,p[45:23]}+1'b0;
   expo=1'b0;
  end
 else if(p[47]==1 && p[22]==0)
  begin
   {out[24],out[23:0]}={1'b1,p[46:24]}+1'b0;
   expo=1'b1;
  end
 else if(p[47]==1 && p[22]==1)
  begin
   {out[24],out[23:0]}={1'b1,p[46:24]}+1'b1;
   expo=1'b1;
  end
end
endmodule
```

```
`include "fp_multiplication_prenormalization.v"
module fp_multiplication_round_normalized(a,b,clk,reset,start,product,overflow);
input [31:0]a,b;
input clk,reset,start;
output [31:0]product;
output overflow;
reg overflow;
wire [7:0]biasedexpo;
reg [31:0]product;
reg [23:0]m,n;
wire [47:0]p;
wire expo,carry;
reg carry1;
wire [24:0]out;

assign {carry,biasedexpo}=(a[30:23]+b[30:23]-8'b01111111);

always @ (*)
begin
  if(reset==0)
   begin
    m=24'h0;
    n=24'h0;
   end
  else
   begin
    m={1'b1,a[22:0]};
    n={1'b1,b[22:0]};
   end
end

fp_multiplication_prenormalization t1(m,n,reset,clk,p,start,out,expo);

always @ (*)
begin
 if(reset==0)
  begin
   overflow=1'b0;
   product=32'b0;
  end
 else if((a[30:23]==8'b0000000 | b[30:23]==8'b0) && (a[22:0]==23'b0 |
b[22:0]==23'b0))
  begin
   product={(a[31]^b[31]),31'b0};
   overflow=1'b0;
  end
 else if((a[30:23]==8'b0000000 || b[30:23]==8'b0) && (a[22:0]!=23'b0 ||
b[22:0]!=23'b0))
  begin
   overflow=1'b1;
   product=32'h0;
  end
 else if (a[30:23]==8'b11111111 | b[30:23]==8'b11111111 |
{carry,biasedexpo}>=8'd255)
  begin
   overflow=1'b1;
   product=32'b0;
  end
 else if( expo == 1'b1 && out[24]==1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+2'b10;
   product[31]=a[31]^b[31];
```

```
   product[22:0]=out[23:1];
  end
 else if( expo == 1'b1  && out[24]!=1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b1;
   product[31]=a[31]^b[31];
   product[22:0]=out[22:0];
  end
 else if(expo==1'b0 && out[24]==1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b1;
   product[31]=a[31]^b[31];
   product[22:0]=out[23:1];
  end
 else
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b0;
   product[31]=a[31]^b[31];
   product[22:0]=out[22:0];
  end
end
endmodule
```

```
`include "fp_multiplication_input_pipe1.v"
`include "fp_multiplication_round_normalized.v"
`include "fp_multiplication_input_pipe2.v"

module fp_multiplication_outputpipe(a,b,clk,reset,start,product1,overflow1);
input [31:0]a,b;
input clk,start,reset;
reg [31:0]aa,bb;
wire
[31:0]pr0,pr1,pr2,pr3,pr4,pr5,pr6,pr7,pr8,pr9,pr10,pr11,pr12,pr13,pr14,pr15,pr16,pr1
7,pr18,pr19,pr20,pr21,pr22,pr23,pr24,pr25,pr26,pr27;
wire
o0,o1,o2,o3,o4,o5,o6,o7,o8,o9,o10,o11,o12,o13,o14,o15,o16,o17,o18,o19,o20,o21,o22,o2
3,o24,o25,o26,o27;
wire
[31:0]m0,m1,m2,m3,m7,m4,m5,m6,m8,m9,m10,m11,m12,m13,n0,n1,n2,n3,n4,n5,n6,n7,n8,n9,n1
0,n11,n12,n13,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,q0,q1,q2,q3,q4,q5,q6,q7,
q8,q9,q10,q11,q12,q13;
wire
start0,start1,start2,start3,start4,start5,start6,start7,start8,start9,start10,start1
1,start12,start13;
wire s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,s12,s13;
output [31:0]product1;
reg [31:0]product1;
output overflow1;
reg [31:0]product;
reg overflow1;
reg overflow;
wire [7:0]biasedexpo;
wire carry;

always @ (*)
begin
 aa=a;
 bb=b;
end

fp_multiplication_input_pipe1
f1(a,b,clk,start,reset,p0,p1,p2,p3,p4,p5,p6,p7,p8,p9,p10,p11,p12,p13,q0,q1,q2,q3,q4,
q5,q6,q7,q8,q9,q10,q11,q12,q13,start0,start1,start2,start3,start4,start5,start6,star
t7,start8,start9,start10,start11,start12,start13);
fp_multiplication_input_pipe2
f2(aa,bb,clk,start,reset,m0,m1,m2,m3,m4,m5,m6,m7,m8,m9,m10,m11,m12,m13,n0,n1,n2,n3,n
4,n5,n6,n7,n8,n9,n10,n11,n12,n13,s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11,s12,s13);
reg [5:0]cs,ns;

parameter
st0=6'b000000,st1=6'b000001,st2=6'b000010,st3=6'b000011,st4=6'b000100,st5=6'b000101,
st6=6'b000111,st7=6'b001000,st8=6'b001001,st9=6'b001010,st10=6'b001011,st11=6'b00110
0,st12=6'b001101,st13=6'b001110,sidle=6'b001111,st14=6'b010000,st15=6'b010001,
st16=6'b010010,
st17=6'b010011,
st18=6'b010100,
st19=6'b010101,
st20=6'b010110,
st21=6'b010111,
st22=6'b011000,
st23=6'b011001,
st24=6'b011010,
st25=6'b011011,
st26=6'b011100,
st27=6'b011101,
st28=6'b011110,
```

```
st29=6'b011111,
st30=6'b100000,
st31=6'b100001,
st32=6'b100010,
st33=6'b100011,
st34=6'b100100,
st35=6'b100101,
st36=6'b100111,
st37=6'b101000,
st38=6'b101001,
st39=6'b101010,
st40=6'b101011,
st41=6'b101100,
st42=6'b101101,
st43=6'b101110,
st44=6'b101111,
st45=6'b110000,
st46=6'b110001,
st47=6'b110010,
st48=6'b110011,
st49=6'b110100,
st50=6'b110101,
st51=6'b110110,
st52=6'b110111,
st53=6'b111000,
st54=6'b111001;




always @ (posedge clk or negedge reset)
begin
 if(reset==0)
  begin
   cs<=sidle;
  end
 else
   cs<=ns;
end

always @ (cs)
begin
 case(cs)
  sidle:ns=st0;
  st0: ns=st1;
  st1: ns=st2;
  st2: ns=st3;
  st3: ns=st4;
  st4: ns=st5;
  st5: ns=st6;
  st6: ns=st7;
  st7: ns=st8;
  st8: ns=st9;
  st9: ns=st10;
  st10: ns=st11;
  st11: ns=st12;
  st12: ns=st13;
  st13: ns=st14;
  st14: ns=st15;
  st15: ns=st16;
  st16: ns=st17;
```

```
  st17: ns=st18;
  st18: ns=st19;
  st19: ns=st20;
  st20: ns=st21;
  st21: ns=st22;
  st22: ns=st23;
  st23: ns=st24;
  st24: ns=st25;
  st25: ns=st26;
  st26: ns=st27;
  st27: ns=st28;
  st28: ns=st29;
  st29: ns=st30;
  st30: ns=st31;
  st31: ns=st32;
  st32: ns=st33;
  st33: ns=st34;
  st34: ns=st35;
  st35: ns=st36;
  st36: ns=st37;
  st37: ns=st38;
  st38: ns=st39;
  st39: ns=st40;
  st40: ns=st41;
  st41: ns=st42;
  st42: ns=st43;
  st43: ns=st44;
  st44: ns=st45;
  st45: ns=st46;
  st46: ns=st47;
  st47: ns=st48;
  st48: ns=st49;
  st49: ns=st50;
  st50: ns=st51;
  st51: ns=st52;
  st52: ns=st53;
  st53: ns=st27;
 endcase
end

assign {carry,biasedexpo}=(a[30:23]+b[30:23]-8'b01111111);

always @ (*)
begin
 if(~reset)
  begin
   product1=32'h0;
   overflow1=1'b0;
  end
 else if(product[30:23]==8'b0 && product[22:0]==23'b0)
  begin
   product1={product[31],31'h0};
   overflow1=overflow;
  end
 else if(product[30:23]==8'b0 && product[22:0]!=23'b0)
  begin
   product1=32'h0;
   overflow1=overflow;
  end
 else if(product[30:23]==8'b11111111)
  begin
   product1=32'h0;
   overflow1=overflow;
```

```
  end
 else
  begin
   product1=product;
   overflow1=overflow;
  end
end

always @ (*)
begin
 case(cs)
  sidle: begin
          product=32'b0;
          overflow=1'b0;
         end
  st0:begin
       product=32'b0;
       overflow=1'b0;
      end
  st1:begin
       product=32'b0;
       overflow=1'b0;
      end
  st2:begin
       product=32'b0;
       overflow=1'b0;
      end
  st3:begin
       product=32'b0;
       overflow=1'b0;
      end
  st4:begin
       product=32'b0;
       overflow=1'b0;
      end
  st5:begin
       product=32'b0;
       overflow=1'b0;
      end
  st6:begin
       product=32'b0;
       overflow=1'b0;
      end
  st7:begin
       product=32'b0;
       overflow=1'b0;
      end
  st8:begin
       product=32'b0;
       overflow=1'b0;
      end
  st9:begin
       product=32'b0;
       overflow=1'b0;
      end
  st10:begin
        product=32'b0;
        overflow=1'b0;
       end
  st11:begin
        product=32'b0;
        overflow=1'b0;
       end
```

```
st12:begin
      product=32'b0;
      overflow=1'b0;
     end
st13:begin
      product=32'b0;
      overflow=1'b0;
     end
st14:begin
      product=32'b0;
      overflow=1'b0;
     end
st15:begin
      product=32'b0;
      overflow=1'b0;
     end
st16:begin
      product=32'b0;
      overflow=1'b0;
     end
st17:begin
      product=32'b0;
      overflow=1'b0;
     end
st18:begin
      product=32'b0;
      overflow=1'b0;
     end
st19:begin
      product=32'b0;
      overflow=1'b0;
     end
st20:begin
      product=32'b0;
      overflow=1'b0;
     end
st21:begin
      product=32'b0;
      overflow=1'b0;
     end
st22:begin
      product=32'b0;
      overflow=1'b0;
     end
st23:begin
      product=32'b0;
      overflow=1'b0;
     end
st24:begin
      product=32'b0;
      overflow=1'b0;
     end
st25:begin
      product=32'b0;
      overflow=1'b0;
     end
st26:begin
      product=pr0;
      overflow=o0;
     end
st27:begin
      product=pr1;
      overflow=o1;
```

```
     end
st28:begin
      product=pr2;
      overflow=o2;
     end
st29:begin
      product=pr3;
      overflow=o3;
     end
st30:begin
      product=pr4;
      overflow=o4;
     end
st31:begin
      product=pr5;
      overflow=o5;
     end
st32:begin
      product=pr6;
      overflow=o6;
     end
st33:begin
      product=pr7;
      overflow=o7;
     end
st34:begin
      product=pr8;
      overflow=o8;
     end
st35:begin
      product=pr9;
      overflow=o9;
     end
st36:begin
      product=pr10;
      overflow=o10;
     end
st37:begin
      product=pr11;
      overflow=o11;
     end
st38:begin
      product=pr12;
      overflow=o12;
     end
st39:begin
      product=pr13;
      overflow=o13;
     end
st40:begin
      product=pr14;
      overflow=o14;
     end
st41:begin
      product=pr15;
      overflow=o15;
     end
st42:begin
      product=pr16;
      overflow=o16;
     end
st43:begin
      product=pr17;
```

```
        overflow=o17;
       end
  st44:begin
        product=pr18;
        overflow=o18;
       end
  st45:begin
        product=pr19;
        overflow=o19;
       end
  st46:begin
        product=pr20;
        overflow=o20;
       end
  st47:begin
        product=pr21;
        overflow=o21;
       end
  st48:begin
        product=pr22;
        overflow=o22;
       end
  st49:begin
        product=pr23;
        overflow=o23;
       end
  st50:begin
        product=pr24;
        overflow=o24;
       end
  st51:begin
        product=pr25;
        overflow=o25;
       end
  st52:begin
        product=pr26;
        overflow=o26;
       end
  st53:begin
        product=pr27;
        overflow=o27;
       end
 endcase
end


fp_multiplication_round_normalized t1(m0,n0,clk,reset,s0,pr0,o0);

fp_multiplication_round_normalized t2(m1,n1,clk,reset,s1,pr1,o1);

fp_multiplication_round_normalized t3(m2,n2,clk,reset,s2,pr2,o2);

fp_multiplication_round_normalized t4(m3,n3,clk,reset,s3,pr3,o3);

fp_multiplication_round_normalized t5(m4,n4,clk,reset,s4,pr4,o4);

fp_multiplication_round_normalized t6(m5,n5,clk,reset,s5,pr5,o5);

fp_multiplication_round_normalized t7(m6,n6,clk,reset,s6,pr6,o6);

fp_multiplication_round_normalized t8(m7,n7,clk,reset,s7,pr7,o7);

fp_multiplication_round_normalized t9(m8,n8,clk,reset,s8,pr8,o8);
```

```
fp_multiplication_round_normalized t10(m9,n9,clk,reset,s9,pr9,o9);
fp_multiplication_round_normalized t11(m10,n10,clk,reset,s10,pr10,o10);
fp_multiplication_round_normalized t12(m11,n11,clk,reset,s11,pr11,o11);
fp_multiplication_round_normalized t13(m12,n12,clk,reset,s12,pr12,o12);
fp_multiplication_round_normalized t14(m13,n13,clk,reset,s13,pr13,o13);
fp_multiplication_round_normalized t15(p0,q0,clk,reset,start0,pr14,o14);
fp_multiplication_round_normalized t16(p1,q1,clk,reset,start1,pr15,o15);
fp_multiplication_round_normalized t17(p2,q2,clk,reset,start2,pr16,o16);
fp_multiplication_round_normalized t18(p3,q3,clk,reset,start3,pr17,o17);
fp_multiplication_round_normalized t19(p4,q4,clk,reset,start4,pr18,o18);
fp_multiplication_round_normalized t20(p5,q5,clk,reset,start5,pr19,o19);
fp_multiplication_round_normalized t21(p6,q6,clk,reset,start6,pr20,o20);
fp_multiplication_round_normalized t22(p7,q7,clk,reset,start7,pr21,o21);
fp_multiplication_round_normalized t23(p8,q8,clk,reset,start8,pr22,o22);
fp_multiplication_round_normalized t24(p9,q9,clk,reset,start9,pr23,o23);
fp_multiplication_round_normalized t25(p10,q10,clk,reset,start10,pr24,o24);
fp_multiplication_round_normalized t26(p11,q11,clk,reset,start11,pr25,o25);
fp_multiplication_round_normalized t27(p12,q12,clk,reset,start12,pr26,o26);
fp_multiplication_round_normalized t28(p13,q13,clk,reset,start13,pr27,o27);
endmodule
```

```
`include "fp_multiplication_outputpipe.v"
module fp_multiplication(a,b,start,reset,clk,product1,overflow1);
input [31:0]a,b;
input clk,reset,start;
output [31:0]product1;
output overflow1;
fp_multiplication_outputpipe ff1(a,b,clk,reset,start,product1,overflow1);
endmodule
```

# FLOATING POINT ADDITION

```
module fp_addition(input [31:0]A_in,B_in, input reset,start, output reg [31:0]sum,
output reg overflow1);
reg [23:0]A,B,A1,B1;
reg overflow;
reg [7:0]expa,expb;
reg [7:0]d_exp,a_exp,b_exp;
reg [8:0]expo;
reg [24:0]out;
reg [24:0]fout;
reg [22:0]sum1;
reg round;
reg [7:0]exxp;
reg [8:0]exponent;


always@(*)
begin
 if(~reset)
  begin
   A[23:0]=23'b0;
   B[23:0]=23'b0;
   a_exp[7:0]=8'b0;
   b_exp[7:0]=8'b0;
  end
 else if(start==1)
  begin
   A[23:0]={1'b1,A_in[22:0]};
   B[23:0]={1'b1,B_in[22:0]};
   a_exp[7:0]=A_in[30:23];
   b_exp[7:0]=B_in[30:23];
  end
end

always@(*)
begin
d_exp=(a_exp>b_exp)?a_exp-b_exp:b_exp-a_exp;
end

always@(*)
begin
 if (~reset)
  begin
   B1=24'b0;
   A1=24'b0;
   round=1'b0;
  end
 else if(a_exp>b_exp)
  begin
   A1 = A;
   B1 = B >> d_exp;
   round=B>>d_exp;
  end
 else if(a_exp<b_exp)
  begin
   A1 = A >> d_exp;
   B1 = B;
   round=A>>d_exp;
  end
 else
  begin
   A1=A;
   B1=B;
   round=1'b0;
```

```
  end
end



always @ (*)
begin
 if(~reset)
  begin
   out=25'b0;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) | (A_in[31]==1'b1 & B_in[31]==1'b1))
  begin
   out=A1+B1;
  end
 else if(((A_in[31]==1'b1 & B_in[31]==1'b0) | (A_in[31]==1'b0 & B_in[31]==1'b1)) &
(A1<B1))
  begin
   out=B1-A1;
  end
 else
  begin
   out=A1-B1;
  end
end


always @ (*)
begin
 if(~reset)
  begin
   sum=32'b0;
   overflow1=1'b0;
   exxp=8'b0;
  end
 else if(start==1'b0)
  begin
   sum=32'b0;
   overflow1=1'b0;
  end
 else if(exponent>=255)
  begin
   sum=32'b0;
   overflow1=1'b1;
  end
 else if((A_in[30:23]==8'b0000000 | B_in[30:23]==8'b0) && (A_in[22:0]==23'b0 |
B_in[22:0]==23'b0))
  begin
   sum=32'b0;
   overflow1=1'b1;
  end
 else if((A_in[30:23]==8'b0000000 || B_in[30:23]==8'b0) && (A_in[22:0]!=23'b0 ||
B_in[22:0]!=23'b0))
  begin
   overflow1=1'b1;
   sum=32'h0;
  end
 else if (A_in[30:23]==8'b11111111 | B_in[30:23]==8'b11111111)
  begin
   overflow1=1'b1;
   sum=32'b0;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b1) && ((A_in[30:23]>B_in[30:23]) |
```

```
(A_in[30:23]==B_in[30:23])))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b1) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) && ((A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23])))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]==B_in[30:23]) &&
(A_in[22:0]==B_in[22:0]))
  begin
   sum=32'b0;
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   overflow1=overflow;
```

```
   exxp=A_in[30:23];
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]==B_in[30:23]) &&
(A_in[22:0]==B_in[22:0]))
  begin
   sum=32'b0;
   overflow1=overflow;
  end
end

always @ (*)
begin
 if(~reset)
  begin
   fout=25'b0;
   expo=9'b0;
  end
 else if(out[24]==1'b1 && out[0]==1'b1)
  begin
   fout={1'b1,out[23:1]}+1'b1;
   expo=exxp+1'b1;
  end
 else if(out[24]==1'b1 && out[0]==1'b0)
  begin
   fout={1'b1,out[23:1]}+1'b0;
   expo=exxp+1'b1;
  end
 else if(out[23]==1'b1 && round==1'b1)
  begin
   fout={1'b1,out[22:0]}+1'b1;
   expo=exxp+1'b0;
  end
 else if(out[23]==1'b1 && round==1'b0)
  begin
   fout={1'b1,out[22:0]}+1'b0;
   expo=exxp+1'b0;
  end
 else if(out[22]== 1'b1)
  begin
   fout={1'b1,out[21:0],1'b0}+1'b0;
   expo=exxp-1'b1;
  end
 else if(out[21]== 1'b1)
  begin
   fout={1'b1,out[20:0],2'b0}+1'b0;
   expo=exxp-2'b10;
  end
 else if(out[20]== 1'b1)
  begin
   fout={1'b1,out[19:0],3'b0}+1'b0;
   expo=exxp-3;
  end
 else if(out[19]== 1'b1)
  begin
   fout={1'b1,out[18:0],4'b0}+1'b0;
```

```
  expo=exxp-4;
 end
else if(out[18]== 1'b1)
 begin
  fout={1'b1,out[17:0],5'b0}+1'b0;
  expo=exxp-5;
 end
else if(out[17]== 1'b1)
 begin
  fout={1'b1,out[16:0],6'b0}+1'b0;
  expo=exxp-6;
 end
else if(out[16]== 1'b1)
 begin
  fout={1'b1,out[15:0],7'b0}+1'b0;
  expo=exxp-7;
 end
else if(out[15]== 1'b1)
 begin
  fout={1'b1,out[14:0],8'b0}+1'b0;
  expo=exxp-8;
 end
else if(out[14]== 1'b1)
 begin
  fout={1'b1,out[13:0],9'b0}+1'b0;
  expo=exxp-9;
 end
else if(out[13]== 1'b1)
 begin
  fout={1'b1,out[12:0],10'b0}+1'b0;
  expo=exxp-10;
 end
else if(out[12]== 1'b1)
 begin
  fout={1'b1,out[11:0],11'b0}+1'b0;
  expo=exxp-11;
 end
else if(out[1]== 1'b1)
 begin
  fout={1'b1,out[10:0],12'b0}+1'b0;
  expo=exxp-12;
 end
else if(out[10]== 1'b1)
 begin
  fout={1'b1,out[9:0],13'b0}+1'b0;
  expo=exxp-13;
 end
else if(out[9]== 1'b1)
 begin
  fout={1'b1,out[8:0],14'b0}+1'b0;
  expo=exxp-14;
 end
else if(out[8]== 1'b1)
 begin
  fout={1'b1,out[7:0],15'b0}+1'b0;
  expo=exxp-15;
 end
else if(out[7]== 1'b1)
 begin
  fout={1'b1,out[6:0],16'b0}+1'b0;
  expo=exxp-16;
 end
else if(out[6]== 1'b1)
```

```
   begin
    fout={1'b1,out[5:0],17'b0}+1'b0;
    expo=exxp-17;
   end
  else if(out[5]== 1'b1)
   begin
    fout={1'b1,out[4:0],18'b0}+1'b0;
    expo=exxp-18;
   end
  else if(out[4]== 1'b1)
   begin
    fout={1'b1,out[3:0],19'b0}+1'b0;
    expo=exxp-19;
   end
  else if(out[3]== 1'b1)
   begin
    fout={1'b1,out[2:0],20'b0}+1'b0;
    expo=exxp-20;
   end
  else if(out[2]== 1'b1)
   begin
    fout={1'b1,out[1:0],21'b0}+1'b0;
    expo=exxp-21;
   end
  else if(out[1]== 1'b1)
   begin
    fout={1'b1,out[0],22'b0}+1'b0;
    expo=exxp-22;
   end
  else if(out[0]==1'b1)
   begin
    fout=25'b0;
    expo=exxp-23;
   end
 end

 always @ (*)
 begin
  if(~reset)
   begin
    sum1=23'b0;
    overflow=1'b0;
   end
  else if(expo>=255)
   begin
    overflow=1'b1;
    sum1=23'b0;
   end
  else if(fout[24]==1)
   begin
    sum1=fout[23:1];
    exponent=expo+1'b1;
    overflow=1'b0;
   end
  else if(fout[23]==1)
   begin
    sum1=fout[22:0];
    exponent=expo[7:0];
    overflow=1'b0;
   end
  else
   begin
    sum1=fout[22:0];
```

```
   exponent=expo[7:0];
   overflow=1'b0;
  end
end

endmodule
```

# FPALU VERIFICATION

```
`include "multiplication_rounding_verification.v"
`include "addition_verification.v"

module fpalu_verification(A,B,start,clk,reset,control,result,overflow);
input [31:0]A,B;
input start,control,reset,clk;
output [31:0]result;
output overflow;
reg [31:0]result;
reg overflow;
reg start1,start2;
wire [31:0]result1,result2;
wire overflow1,overflow2;
reg [1:0]cs,ns;
parameter s0=2'b00, s1=2'b01, s2=2'b10;

always @ (posedge clk or negedge reset)
begin
 if (~reset)
  begin
   cs<=s0;
  end
 else if(start==1)
  cs<=ns;
end

always @ (*)
begin
 case (cs)
  s0: begin
       if( control==1'b1)
        ns=s1;
       else if(control==1'b0)
        ns=s2;
       else
        ns=s0;
      end

  s1:begin
      if(control==1'b0)
       ns=s2;
      else
       ns=s1;
     end
  s2:begin
      if(control==1'b1)
       ns=s1;
      else
       ns=s2;
     end
 endcase
end


always @ (*)
begin
 case(cs)
  s0:begin
      if (reset==0)
       begin
        start1=1'b0;
        start2=1'b0;
        result=32'b0;
```

```
      overflow=1'b0;
     end
    else if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
    else
     begin
      start1=1'b0;
      start2=1'b0;
      result=32'b0;
      overflow=1'b0;
     end
   end
s1:begin
    if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
    else
     begin
      start1=1'b0;
      start2=1'b0;
      result=32'b0;
      overflow=1'b0;
     end
   end

s2:begin
    if(start==1'b1 && control==1'b1)
     begin
      start1=1'b1;
      start2=1'b0;
      result=result1;
      overflow=overflow1;
     end
    else if(start==1'b1 && control==1'b0)
     begin
      start2=1'b1;
      start1=1'b0;
      result=result2;
      overflow=overflow2;
     end
```

```
      else
       begin
        start1=1'b0;
        start2=1'b0;
        result=32'b0;
        overflow=1'b0;
       end
     end
 endcase
end

multiplication_rounding_verification uut1(A,B,clk,reset,start1,result1,overflow1);
addition_verification uut(A,B, reset,start2, result2, overflow2);

endmodule
```

```
`include "multiplication_verification.v"
module multiplication_rounding_verification(a,b,clk,reset,start,product,overflow);
input [31:0]a,b;
input clk,reset,start;
output [31:0]product;
output overflow;
reg overflow;
wire [7:0]biasedexpo;
reg [31:0]product;
reg [23:0]m,n;
wire [47:0]p;
wire expo,carry;
reg carry1;
wire [24:0]out;

assign {carry,biasedexpo}=(a[30:23]+b[30:23]-8'b01111111);

always @ (*)
begin
 if(reset==0)
  begin
   m=24'h0;
   n=24'h0;
  end
 else
  begin
   m={1'b1,a[22:0]};
   n={1'b1,b[22:0]};
  end
end

multiplication_verification t1(m,n,reset,clk,p,start,out,expo);

always @ (*)
begin
 if(reset==0)
  begin
   overflow=1'b0;
   product=32'b0;
  end
 else if((a[30:23]==8'b0000000 | b[30:23]==8'b0) && (a[22:0]==23'b0 |
b[22:0]==23'b0))
  begin
   product={(a[31]^b[31]),31'b0};
   overflow=1'b0;
  end
 else if((a[30:23]==8'b0000000 || b[30:23]==8'b0) && (a[22:0]!=23'b0 ||
b[22:0]!=23'b0))
  begin
   overflow=1'b1;
   product=32'h0;
  end
 else if (a[30:23]==8'b11111111 | b[30:23]==8'b11111111 |
{carry,biasedexpo}>=8'd255)
  begin
   overflow=1'b1;
   product=32'b0;
  end
 else if( expo == 1'b1 && out[24]==1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+2'b10;
   product[31]=a[31]^b[31];
```

```
   product[22:0]=out[23:1];
  end
 else if( expo == 1'b1  && out[24]!=1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b1;
   product[31]=a[31]^b[31];
   product[22:0]=out[22:0];
  end
 else if(expo==1'b0 && out[24]==1'b1)
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b1;
   product[31]=a[31]^b[31];
   product[22:0]=out[23:1];
  end
 else
  begin
   overflow=1'b0;
   {carry1,product[30:23]}=(a[30:23]+b[30:23]-8'b01111111)+1'b0;
   product[31]=a[31]^b[31];
   product[22:0]=out[22:0];
  end
end
endmodule
```

```
module multiplication_verification(a,b,reset,clk,p,start,out,expo);
input [23:0]a,b;
input reset,clk,start;
output [47:0]p;
reg [47:0]p;
output [24:0]out;
output expo;
reg [24:0]out;
reg expo;
wire load,shift;

always @ (posedge clk or negedge reset)
begin
 if(~reset)
  begin
   p<=48'b0;
  end
 else
  begin
   p <= a * b;
  end
end


always @ (*)
begin
 if(~reset)
begin
out=25'b0;
expo=1'b0;
end
else if(p[47]==0 && p[22]==1)
  begin
   {out[24],out[23:0]}={1'b1,p[45:23]}+1'b1;
   expo=1'b0;
  end
 else if(p[47]==0 && p[22]==0)
  begin
   {out[24],out[23:0]}={1'b1,p[45:23]}+1'b0;
   expo=1'b0;
  end
 else if(p[47]==1 && p[22]==0)
  begin
   {out[24],out[23:0]}={1'b1,p[46:24]}+1'b0;
   expo=1'b1;
  end
 else if(p[47]==1 && p[22]==1)
  begin
   {out[24],out[23:0]}={1'b1,p[46:24]}+1'b1;
   expo=1'b1;
  end
end
endmodule
```

# FLOATING POINT
# ALU ADDITION
# VERIFICATION

```
module addition_verification(input [31:0]A_in,B_in, input reset,start, output reg
[31:0]sum, output reg overflow1);
reg [23:0]A,B,A1,B1;
reg overflow;
reg [7:0]expa,expb;
reg [7:0]d_exp,a_exp,b_exp;
reg [8:0]expo;
reg [24:0]out;
reg [24:0]fout;
reg [22:0]sum1;
reg round;
reg [7:0]exxp;
reg [8:0]exponent;
integer i,q,m,n;

always@(*)
begin
 if(~reset)
  begin
   A[23:0]=23'b0;
   B[23:0]=23'b0;
   a_exp[7:0]=8'b0;
   b_exp[7:0]=8'b0;
  end
 else if(start==1)
  begin
   A[23:0]={1'b1,A_in[22:0]};
   B[23:0]={1'b1,B_in[22:0]};
   a_exp[7:0]=A_in[30:23];
   b_exp[7:0]=B_in[30:23];
  end
end

always@(*)
begin
 d_exp=(a_exp>b_exp)?a_exp-b_exp:b_exp-a_exp;
end

always@(*)
begin
 if (~reset)
  begin
   B1=24'b0;
   A1=24'b0;
   round=1'b0;
  end
 else if(a_exp>b_exp)
  begin
   A1 = A;
   B1 = B >> d_exp;
   round=B>>d_exp;
  end
 else if(a_exp<b_exp)
  begin
   A1 = A >> d_exp;
   B1 = B;
   round=A>>d_exp;
  end
 else
  begin
   A1=A;
   B1=B;
   round=1'b0;
```

```
  end
end


always @ (*)
begin
 if(~reset)
  begin
   out=25'b0;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) | (A_in[31]==1'b1 & B_in[31]==1'b1))
  begin
   out=A1+B1;
  end
 else if(((A_in[31]==1'b1 & B_in[31]==1'b0) | (A_in[31]==1'b0 & B_in[31]==1'b1)) &
(A1<B1))
  begin
   out=B1-A1;
  end
 else
  begin
   out=A1-B1;
  end
end



always @ (*)
begin
 if(~reset | start==0)
  begin
   sum=32'b0;
   overflow1=1'b0;
  end
 else if((A_in[30:23]==8'b0000000 | B_in[30:23]==8'b0) && (A_in[22:0]==23'b0 |
B_in[22:0]==23'b0) || (A_in[30:23]==8'b0000000 || B_in[30:23]==8'b0) &&
(A_in[22:0]!=23'b0 || B_in[22:0]!=23'b0) || (exponent>=255) ||
(A_in[30:23]==8'b11111111 | B_in[30:23]==8'b11111111))
  begin
   overflow1=1'b1;
   sum=32'b0;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b1) && ((A_in[30:23]>B_in[30:23]) |
(A_in[30:23]==B_in[30:23])))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b1) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) && ((A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23])))
  begin
   sum[31]=1'b0;
```

```
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b0) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=A_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b1 & B_in[31]==1'b0) && (A_in[30:23]==B_in[30:23]) &&
(A_in[22:0]==B_in[22:0]))
  begin
   sum=32'b0;
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]>B_in[30:23])||
(A_in[30:23]==B_in[30:23]))
  begin
   sum[31]=1'b0;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   overflow1=overflow;
   exxp=A_in[30:23];
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]<B_in[30:23]))
  begin
   sum[31]=1'b1;
   sum[30:23] =exponent[7:0];
   sum[22:0]=sum1;
   exxp=B_in[30:23];
   overflow1=overflow;
  end
 else if((A_in[31]==1'b0 & B_in[31]==1'b1) && (A_in[30:23]==B_in[30:23]) &&
(A_in[22:0]==B_in[22:0]))
  begin
   sum=32'b0;
   overflow1=overflow;
  end
end

always @ (*)
begin
```

```
 for(i=22; i>=0 ; i=i-1)
  if (out[i]==1)
   begin
    q=1;
    m=q;
   end
  else
   n=1;
end

always @ (*)
begin
 if(~reset)
  begin
   fout=25'b0;
   expo=9'b0;
  end
 else if(out[24]==1'b1 && out[0]==1'b1)
  begin
   fout={1'b1,out[23:1]}+1'b1;
   expo=exxp+1'b1;
  end
 else if(out[24]==1'b1 && out[0]==1'b0)
  begin
   fout={1'b1,out[23:1]}+1'b0;
   expo=exxp+1'b1;
  end
 else if(out[23]==1'b1 && round==1'b1)
  begin
   fout={1'b1,out[22:0]}+1'b1;
   expo=exxp+1'b0;
  end
 else if(out[23]==1'b1 && round==1'b0)
  begin
   fout={1'b1,out[22:0]}+1'b0;
   expo=exxp+1'b0;
  end
 else if(n==1)
  begin
   fout=25'b0;
   expo=exxp-23;
  end
 else
  begin
   fout = {1'b1,out >> m};
   expo=exxp+1'b0;
  end
end

always @ (*)
begin
 if(~reset)
  begin
   sum1=23'b0;
   overflow=1'b0;
  end
 else if(expo>=255)
  begin
   overflow=1'b1;
   sum1=23'b0;
  end
 else if(fout[24]==1)
  begin
```

```
    sum1=fout[23:1];
    exponent=expo+1'b1;
    overflow=1'b0;
   end
  else if(fout[23]==1)
   begin
    sum1=fout[22:0];
    exponent=expo[7:0];
    overflow=1'b0;
   end
  else
   begin
    sum1=fout[22:0];
    exponent=expo[7:0];
    overflow=1'b0;
   end
end

endmodule
```

# SIMULATION RESULTS

# NOTE:

My DUT output for first input comes after 27 cycles but for the code I used in the automated test bench generates output in one cycle. So while checking the output results , we should compare the outputs of DUT and verification accordingly for the multiplication.

```
Chronologic VCS simulator copyright 1991-2014
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Compiler version I-2014.03-2; Runtime version I-2014.03-2;  May  4 14:27 2016
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Warning-[STASKW_RMIEAFL] Illegal entry
fpalu_fixture.v, 37
  Illegal entry found at file filea.txt line 401 while executing $readmem.
  Please ensure that the file has proper entries.


Warning-[STASKW_RMIEAFL] Illegal entry
fpalu_fixture.v, 38
  Illegal entry found at file fileb.txt line 401 while executing $readmem.
  Please ensure that the file has proper entries.

                   0clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  10clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  20clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  30clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  40clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  50clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  60clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  70clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  80clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                  90clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                 100clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                 110clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                 120clk=0 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                 130clk=1 A=00000000 B=00000000 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=0  pass=0 fail=0
                 140clk=0 A=12153524 B=c0895e81 control=1 result=00000000 overflow=0
testresult=93000000 testoverflow=0  pass=0 fail=0
                 150clk=1 A=12153524 B=c0895e81 control=1 result=00000000 overflow=0
testresult=9320210a testoverflow=0  pass=0 fail=0
                 160clk=0 A=0484d609 B=31f05663 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                 170clk=1 A=0484d609 B=31f05663 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                 180clk=0 A=06b97b0d B=46df998d control=1 result=00000000 overflow=0
testresult=0df96af7 testoverflow=0  pass=0 fail=0
                 190clk=1 A=06b97b0d B=46df998d control=1 result=00000000 overflow=0
testresult=0e220171 testoverflow=0  pass=0 fail=0
                 200clk=0 A=32c28465 B=8ff0cd1f control=1 result=00000000 overflow=0
testresult=83220171 testoverflow=0  pass=0 fail=0
                 210clk=1 A=32c28465 B=8ff0cd1f control=1 result=00000000 overflow=0
testresult=8336f7fb testoverflow=0  pass=0 fail=0
                 220clk=0 A=10e4b020 B=86d7cd0d control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                 230clk=1 A=10e4b020 B=86d7cd0d control=1 result=00000000 overflow=0
```

testresult=00000000 testoverflow=1  pass=0 fail=0
                240clk=0 A=bb23f176 B=2f727d5d control=1 result=00000000 overflow=0
testresult=ab40c717 testoverflow=0  pass=0 fail=0
                250clk=1 A=bb23f176 B=2f727d5d control=1 result=00000000 overflow=0
testresult=ab1b4a8a testoverflow=0  pass=0 fail=0
                260clk=0 A=a646d54a B=462df78c control=1 result=00000000 overflow=0
testresult=ad1b4a8a testoverflow=0  pass=0 fail=0
                270clk=1 A=a646d54a B=462df78c control=1 result=00000000 overflow=0
testresult=ad071e67 testoverflow=0  pass=0 fail=0
                280clk=0 A=007de9f9 B=e33724c6 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                290clk=1 A=007de9f9 B=e33724c6 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                300clk=0 A=807784c5 B=d513d2aa control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                310clk=1 A=807784c5 B=d513d2aa control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                320clk=0 A=72aff7e5 B=bbd27277 control=1 result=00000000 overflow=0
testresult=ef0eeced testoverflow=0  pass=0 fail=0
                330clk=1 A=72aff7e5 B=bbd27277 control=1 result=00000000 overflow=0
testresult=ef10a808 testoverflow=0  pass=0 fail=0
                340clk=0 A=ffb2d612 B=47ecdb8f control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                350clk=1 A=ffb2d612 B=47ecdb8f control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                360clk=0 A=7f3069f2 B=e77696ce control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                370clk=1 A=7f3069f2 B=e77696ce control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                380clk=0 A=e33724c6 B=e2ca4ec5 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                390clk=1 A=e33724c6 B=e2ca4ec5 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                400clk=0 A=e2ca4ec5 B=76295bec control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                410clk=1 A=e2ca4ec5 B=76295bec control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                420clk=0 A=d513d2aa B=11fe0523 control=1 result=00000000 overflow=0
testresult=a785d6a4 testoverflow=0  pass=0 fail=0
                430clk=1 A=d513d2aa B=11fe0523 control=1 result=00000000 overflow=0
testresult=a792adfc testoverflow=0  pass=0 fail=0
                440clk=0 A=72aff7e5 B=520eefa4 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                450clk=1 A=72aff7e5 B=520eefa4 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                460clk=0 A=bbd27277 B=64e165c9 control=1 result=00000000 overflow=0
testresult=e0c48074 testoverflow=0  pass=0 fail=0
                470clk=1 A=bbd27277 B=64e165c9 control=1 result=00000000 overflow=0
testresult=e1394a47 testoverflow=0  pass=0 fail=0
                480clk=0 A=8932d612 B=9ca70439 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                490clk=1 A=8932d612 B=9ca70439 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                500clk=0 A=47ecdb8f B=ef8372df control=1 result=00000000 overflow=0
testresult=f7e95932 testoverflow=0  pass=0 fail=0
                510clk=1 A=47ecdb8f B=ef8372df control=1 result=00000000 overflow=0
testresult=f7f33d45 testoverflow=0  pass=0 fail=0
                520clk=0 A=793069f2 B=ea5814d4 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                530clk=1 A=793069f2 B=ea5814d4 control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
                540clk=0 A=e77696ce B=33836567 control=1 result=00000000 overflow=0
testresult=db94e7be testoverflow=0  pass=0 fail=0

550clk=1 A=e77696ce B=33836567 control=1 result=00000000 overflow=0
testresult=db7d21b0 testoverflow=0  pass=0 fail=0
560clk=0 A=f4007ae8 B=4ea0419d control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=0 fail=0
570clk=1 A=f4007ae8 B=4ea0419d control=1 result=00000000 overflow=0
testresult=00000000 testoverflow=1  pass=1 fail=0
580clk=0 A=e2ca4ec5 B=583125b0 control=1 result=00000000 overflow=0
testresult=fb20db7e testoverflow=0  pass=1 fail=0
590clk=1 A=e2ca4ec5 B=583125b0 control=1 result=00000000 overflow=0
testresult=fb8bfe3e testoverflow=0  pass=1 fail=0
600clk=0 A=2e58495c B=41103982 control=1 result=00000000 overflow=0
testresult=300bfe3e testoverflow=0  pass=1 fail=0
610clk=1 A=2e58495c B=41103982 control=1 result=00000000 overflow=0
testresult=2ff3b3b4 testoverflow=0  pass=1 fail=0
620clk=0 A=de8e28bd B=24d2bf49 control=1 result=00000000 overflow=0
testresult=c3f3b3b4 testoverflow=0  pass=1 fail=0
630clk=1 A=de8e28bd B=24d2bf49 control=1 result=00000000 overflow=0
testresult=c3ea0f48 testoverflow=0  pass=1 fail=0
640clk=0 A=96ab582d B=ecb91ad9 control=1 result=00000000 overflow=0
testresult=43ea0f48 testoverflow=0  pass=1 fail=0
650clk=1 A=96ab582d B=ecb91ad9 control=1 result=00000000 overflow=0
testresult=43f7c961 testoverflow=0  pass=1 fail=0
660clk=0 A=b2a72665 B=1000b720 control=1 result=00000000 overflow=0
testresult=8377c961 testoverflow=0  pass=1 fail=0
670clk=1 A=b2a72665 B=1000b720 control=1 result=9320210a overflow=0
testresult=83281588 testoverflow=0  pass=1 fail=0
680clk=0 A=b1ef6263 B=8e054c1c control=1 result=9320210a overflow=0
testresult=00281588 testoverflow=0  pass=1 fail=0
690clk=1 A=b1ef6263 B=8e054c1c control=1 result=00000000 overflow=1
testresult=00794a92 testoverflow=0  pass=1 fail=0
700clk=0 A=0573870a B=49b16f93 control=1 result=00000000 overflow=1
testresult=0f794a92 testoverflow=0  pass=1 fail=0
710clk=1 A=0573870a B=49b16f93 control=1 result=0e220171 overflow=0
testresult=0fa8ca82 testoverflow=0  pass=1 fail=0
720clk=0 A=c03b2280 B=71b461e3 control=1 result=0e220171 overflow=0
testresult=f2a8ca82 testoverflow=0  pass=1 fail=0
730clk=1 A=c03b2280 B=71b461e3 control=1 result=8336f7fb overflow=0
testresult=f283dbd0 testoverflow=0  pass=1 fail=0
740clk=0 A=10642120 B=954b822a control=1 result=8336f7fb overflow=0
testresult=00000000 testoverflow=1  pass=1 fail=0
750clk=1 A=10642120 B=954b822a control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
760clk=0 A=557845aa B=e471f8c8 control=1 result=00000000 overflow=1
testresult=fa355a42 testoverflow=0  pass=1 fail=0
770clk=1 A=557845aa B=e471f8c8 control=1 result=ab1b4a8a overflow=0
testresult=fa6aaadb testoverflow=0  pass=1 fail=0
780clk=0 A=bb23f176 B=aed72e5d control=1 result=ab1b4a8a overflow=0
testresult=2aeaaadb testoverflow=0  pass=1 fail=0
790clk=1 A=bb23f176 B=aed72e5d control=1 result=ad071e67 overflow=0
testresult=2a89cd7b testoverflow=0  pass=1 fail=0
800clk=0 A=a646d54a B=1d3f9d3a control=1 result=ad071e67 overflow=0
testresult=8409cd7b testoverflow=0  pass=1 fail=0
810clk=1 A=a646d54a B=1d3f9d3a control=1 result=00000000 overflow=1
testresult=8414d340 testoverflow=0  pass=1 fail=0
820clk=0 A=cb203e96 B=4226a984 control=1 result=00000000 overflow=1
testresult=ce14d340 testoverflow=0  pass=1 fail=0
830clk=1 A=cb203e96 B=4226a984 control=1 result=00000000 overflow=1
testresult=cdd0a562 testoverflow=0  pass=1 fail=0
840clk=0 A=8983b813 B=95a9a82b control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
850clk=1 A=8983b813 B=95a9a82b control=1 result=ef10a808 overflow=0
testresult=00000000 testoverflow=1  pass=1 fail=0
860clk=0 A=86bc380d B=1c8d7f39 control=1 result=ef10a808 overflow=0

testresult=00000000 testoverflow=1  pass=1 fail=0
 870clk=1 A=86bc380d B=1c8d7f39 control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
 880clk=0 A=a9a7d653 B=897f1c12 control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
 890clk=1 A=a9a7d653 B=897f1c12 control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
 900clk=0 A=359fdd6b B=a97f0052 control=1 result=00000000 overflow=1
testresult=9fa740e4 testoverflow=0  pass=1 fail=0
 910clk=1 A=359fdd6b B=a97f0052 control=1 result=00000000 overflow=1
testresult=9f9f3dc1 testoverflow=0  pass=1 fail=0
 920clk=0 A=eaa62ad5 B=2c848959 control=1 result=00000000 overflow=1
testresult=d81f3dc1 testoverflow=0  pass=1 fail=0
 930clk=1 A=eaa62ad5 B=2c848959 control=1 result=00000000 overflow=1
testresult=d7ac0e79 testoverflow=0  pass=1 fail=0
 940clk=0 A=81174a02 B=e82b96d0 control=1 result=00000000 overflow=1
testresult=29ac0e79 testoverflow=0  pass=1 fail=0
 950clk=1 A=81174a02 B=e82b96d0 control=1 result=a792adfc overflow=0
testresult=29cacf1f testoverflow=0  pass=1 fail=0
 960clk=0 A=d7563eae B=b759ea6e control=1 result=a792adfc overflow=0
testresult=4ecacf1f testoverflow=0  pass=1 fail=0
 970clk=1 A=d7563eae B=b759ea6e control=1 result=00000000 overflow=1
testresult=4f365f53 testoverflow=0  pass=1 fail=0
 980clk=0 A=0effe91d B=4bf52997 control=1 result=00000000 overflow=1
testresult=1b365f53 testoverflow=0  pass=1 fail=0
 990clk=1 A=0effe91d B=4bf52997 control=1 result=e1394a47 overflow=0
testresult=1b7513ac testoverflow=0  pass=1 fail=0
1000clk=0 A=e7c572cf B=6d8b87db control=1 result=e1394a47 overflow=0
testresult=00000000 testoverflow=1  pass=1 fail=0
1010clk=1 A=e7c572cf B=6d8b87db control=1 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1020clk=0 A=11844923 B=535277a6 control=1 result=00000000 overflow=1
testresult=25573c3e testoverflow=0  pass=1 fail=0
1030clk=1 A=11844923 B=535277a6 control=1 result=f7f33d45 overflow=0
testresult=255983a5 testoverflow=0  pass=1 fail=0
1040clk=0 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1050clk=1 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1060clk=0 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1070clk=1 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1080clk=0 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1090clk=1 A=00000000 B=00000000 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1100clk=0 A=00000000 B=c0895e81 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1110clk=1 A=00000000 B=c0895e81 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
1120clk=0 A=12153524 B=31f05663 control=0 result=31f05663 overflow=0
testresult=31f05663 testoverflow=0  pass=1 fail=0
1130clk=1 A=12153524 B=31f05663 control=0 result=31f05663 overflow=0
testresult=31f05663 testoverflow=0  pass=1 fail=0
1140clk=0 A=0484d609 B=46df998d control=0 result=46df998d overflow=0
testresult=46df998d testoverflow=0  pass=1 fail=0
1150clk=1 A=0484d609 B=46df998d control=0 result=46df998d overflow=0
testresult=46df998d testoverflow=0  pass=1 fail=0
1160clk=0 A=06b97b0d B=8ff0cd1f control=0 result=8ff0ccf1 overflow=0
testresult=8ff0ccf1 testoverflow=0  pass=1 fail=0
1170clk=1 A=06b97b0d B=8ff0cd1f control=0 result=8ff0ccf1 overflow=0
testresult=8ff0ccf1 testoverflow=0  pass=1 fail=0

1180clk=0 A=32c28465 B=86d7cd0d control=0 result=32c28465 overflow=0 testresult=32c28465 testoverflow=0  pass=1 fail=0
1190clk=1 A=32c28465 B=86d7cd0d control=0 result=32c28465 overflow=0 testresult=32c28465 testoverflow=0  pass=1 fail=0
1200clk=0 A=10e4b020 B=2f727d5d control=0 result=2f727d5d overflow=0 testresult=2f727d5d testoverflow=0  pass=1 fail=0
1210clk=1 A=10e4b020 B=2f727d5d control=0 result=2f727d5d overflow=0 testresult=2f727d5d testoverflow=0  pass=1 fail=0
1220clk=0 A=bb23f176 B=462df78c control=0 result=462df78a overflow=0 testresult=462df78a testoverflow=0  pass=1 fail=0
1230clk=1 A=bb23f176 B=462df78c control=0 result=462df78a overflow=0 testresult=462df78a testoverflow=0  pass=1 fail=0
1240clk=0 A=a646d54a B=e33724c6 control=0 result=e33724c6 overflow=0 testresult=e33724c6 testoverflow=0  pass=1 fail=0
1250clk=1 A=a646d54a B=e33724c6 control=0 result=e33724c6 overflow=0 testresult=e33724c6 testoverflow=0  pass=1 fail=0
1260clk=0 A=007de9f9 B=d513d2aa control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1270clk=1 A=007de9f9 B=d513d2aa control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1280clk=0 A=807784c5 B=bbd27277 control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1290clk=1 A=807784c5 B=bbd27277 control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1300clk=0 A=72aff7e5 B=47ecdb8f control=0 result=72aff7e5 overflow=0 testresult=72aff7e5 testoverflow=0  pass=1 fail=0
1310clk=1 A=72aff7e5 B=47ecdb8f control=0 result=72aff7e5 overflow=0 testresult=72aff7e5 testoverflow=0  pass=1 fail=0
1320clk=0 A=ffb2d612 B=e77696ce control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1330clk=1 A=ffb2d612 B=e77696ce control=0 result=00000000 overflow=1 testresult=00000000 testoverflow=1  pass=1 fail=0
1340clk=0 A=7f3069f2 B=e2ca4ec5 control=0 result=7f3069f2 overflow=0 testresult=7f3069f2 testoverflow=0  pass=1 fail=0
1350clk=1 A=7f3069f2 B=e2ca4ec5 control=0 result=7f3069f2 overflow=0 testresult=7f3069f2 testoverflow=0  pass=1 fail=0
1360clk=0 A=e33724c6 B=76295bec control=0 result=76295bec overflow=0 testresult=76295bec testoverflow=0  pass=1 fail=0
1370clk=1 A=e33724c6 B=76295bec control=0 result=76295bec overflow=0 testresult=76295bec testoverflow=0  pass=1 fail=0
1380clk=0 A=e2ca4ec5 B=11fe0523 control=0 result=e2ca4ec5 overflow=0 testresult=e2ca4ec5 testoverflow=0  pass=1 fail=0
1390clk=1 A=e2ca4ec5 B=11fe0523 control=0 result=e2ca4ec5 overflow=0 testresult=e2ca4ec5 testoverflow=0  pass=1 fail=0
1400clk=0 A=d513d2aa B=520eefa4 control=0 result=d51196ec overflow=0 testresult=d51196ec testoverflow=0  pass=1 fail=0
1410clk=1 A=d513d2aa B=520eefa4 control=0 result=d51196ec overflow=0 testresult=d51196ec testoverflow=0  pass=1 fail=0
1420clk=0 A=72aff7e5 B=64e165c9 control=0 result=72aff7e5 overflow=0 testresult=72aff7e5 testoverflow=0  pass=1 fail=0
1430clk=1 A=72aff7e5 B=64e165c9 control=0 result=72aff7e5 overflow=0 testresult=72aff7e5 testoverflow=0  pass=1 fail=0
1440clk=0 A=0509650a B=9ca70439 control=0 result=9ca70439 overflow=0 testresult=9ca70439 testoverflow=0  pass=1 fail=0
1450clk=1 A=0509650a B=9ca70439 control=0 result=9ca70439 overflow=0 testresult=9ca70439 testoverflow=0  pass=1 fail=0
1460clk=0 A=e5730aca B=ef8372df control=0 result=ef8372e7 overflow=0 testresult=ef8372e7 testoverflow=0  pass=1 fail=0
1470clk=1 A=e5730aca B=ef8372df control=0 result=ef8372e7 overflow=0 testresult=ef8372e7 testoverflow=0  pass=1 fail=0
1480clk=0 A=9e314c3c B=ea5814d4 control=0 result=ea5814d4 overflow=0 testresult=ea5814d4 testoverflow=0  pass=1 fail=0
1490clk=1 A=9e314c3c B=ea5814d4 control=0 result=ea5814d4 overflow=0

testresult=ea5814d4 testoverflow=0  pass=1 fail=0
                1500clk=0 A=7968bdf2 B=33836567 control=0 result=7968bdf2 overflow=0
testresult=7968bdf2 testoverflow=0  pass=1 fail=0
                1510clk=1 A=7968bdf2 B=33836567 control=0 result=7968bdf2 overflow=0
testresult=7968bdf2 testoverflow=0  pass=1 fail=0
                1520clk=0 A=452e618a B=4ea0419d control=0 result=4ea041b3 overflow=0
testresult=4ea041b3 testoverflow=0  pass=1 fail=0
                1530clk=1 A=452e618a B=4ea0419d control=0 result=4ea041b3 overflow=0
testresult=4ea041b3 testoverflow=0  pass=1 fail=0
                1540clk=0 A=20c4b341 B=583125b0 control=0 result=583125b0 overflow=0
testresult=583125b0 testoverflow=0  pass=1 fail=0
                1550clk=1 A=20c4b341 B=583125b0 control=0 result=583125b0 overflow=0
testresult=583125b0 testoverflow=0  pass=1 fail=0
                1560clk=0 A=ec4b34d8 B=5d85d3bb control=0 result=ec4b34d8 overflow=0
testresult=ec4b34d8 testoverflow=0  pass=1 fail=0
                1570clk=1 A=ec4b34d8 B=5d85d3bb control=0 result=ec4b34d8 overflow=0
testresult=ec4b34d8 testoverflow=0  pass=1 fail=0
                1580clk=0 A=3c20f378 B=80797c00 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
                1590clk=1 A=3c20f378 B=80797c00 control=0 result=00000000 overflow=1
testresult=00000000 testoverflow=1  pass=1 fail=0
                1600clk=0 A=c48a1289 B=87e44c0f control=0 result=c48a1289 overflow=0
testresult=c48a1289 testoverflow=0  pass=1 fail=0
                1610clk=1 A=c48a1289 B=87e44c0f control=0 result=c48a1289 overflow=0
testresult=c48a1289 testoverflow=0  pass=1 fail=0
                1620clk=0 A=75c50deb B=b4e8d669 control=0 result=75c50deb overflow=0
testresult=75c50deb testoverflow=0  pass=1 fail=0
                1630clk=1 A=75c50deb B=b4e8d669 control=0 result=75c50deb overflow=0
testresult=75c50deb testoverflow=0  pass=1 fail=0
                1640clk=0 A=5b0265b6 B=8653620c control=0 result=5b0265b6 overflow=0
testresult=5b0265b6 testoverflow=0  pass=1 fail=0
                1650clk=1 A=5b0265b6 B=8653620c control=0 result=5b0265b6 overflow=0
testresult=5b0265b6 testoverflow=0  pass=1 fail=0
                1660clk=0 A=634bf9c6 B=2ca81959 control=0 result=634bf9c6 overflow=0
testresult=634bf9c6 testoverflow=0  pass=1 fail=0
                1670clk=1 A=634bf9c6 B=2ca81959 control=0 result=634bf9c6 overflow=0
testresult=634bf9c6 testoverflow=0  pass=1 fail=0
                1680clk=0 A=571513ae B=62fd49c5 control=0 result=62fd49c7 overflow=0
testresult=62fd49c7 testoverflow=0  pass=1 fail=0
                1690clk=1 A=571513ae B=62fd49c5 control=0 result=62fd49c7 overflow=0
testresult=62fd49c7 testoverflow=0  pass=1 fail=0
                1700clk=0 A=de7502bc B=67d735cf control=0 result=67d735b1 overflow=0
testresult=67d735b1 testoverflow=0  pass=1 fail=0
                1710clk=1 A=de7502bc B=67d735cf control=0 result=67d735b1 overflow=0
testresult=67d735b1 testoverflow=0  pass=1 fail=0
                1720clk=0 A=150fdd2a B=4839e590 control=0 result=4839e590 overflow=0
testresult=4839e590 testoverflow=0  pass=1 fail=0
                1730clk=1 A=150fdd2a B=4839e590 control=0 result=4839e590 overflow=0
testresult=4839e590 testoverflow=0  pass=1 fail=0
                1740clk=0 A=85d79a0b B=a8e4d851 control=0 result=a8e4d851 overflow=0
testresult=a8e4d851 testoverflow=0  pass=1 fail=0
                1750clk=1 A=85d79a0b B=a8e4d851 control=0 result=a8e4d851 overflow=0
testresult=a8e4d851 testoverflow=0  pass=1 fail=0
                1760clk=0 A=b897be71 B=b4f9a469 control=0 result=b898b815 overflow=0
testresult=b898b815 testoverflow=0  pass=1 fail=0
                1770clk=1 A=b897be71 B=b4f9a469 control=0 result=b898b815 overflow=0
testresult=b898b815 testoverflow=0  pass=1 fail=0
                1780clk=0 A=42f24185 B=3b83cd77 control=0 result=42f24395 overflow=0
testresult=42f24395 testoverflow=0  pass=1 fail=0
                1790clk=1 A=42f24185 B=3b83cd77 control=0 result=42f24395 overflow=0
testresult=42f24395 testoverflow=0  pass=1 fail=0
                1800clk=0 A=27f2554f B=2523654a control=0 result=27f77079 overflow=0
testresult=27f77079 testoverflow=0  pass=1 fail=0

1810clk=1 A=27f2554f B=2523654a control=0 result=27f77079 overflow=0 testresult=27f77079 testoverflow=0  pass=1 fail=0
1820clk=0 A=9dcc603b B=ec3758d8 control=0 result=ec3758d8 overflow=0 testresult=ec3758d8 testoverflow=0  pass=1 fail=0
1830clk=1 A=9dcc603b B=ec3758d8 control=0 result=ec3758d8 overflow=0 testresult=ec3758d8 testoverflow=0  pass=1 fail=0
1840clk=0 A=1d06333a B=4ddd4d9b control=0 result=4ddd4d9b overflow=0 testresult=4ddd4d9b testoverflow=0  pass=1 fail=0
1850clk=1 A=1d06333a B=4ddd4d9b control=0 result=4ddd4d9b overflow=0 testresult=4ddd4d9b testoverflow=0  pass=1 fail=0
1860clk=0 A=bf23327e B=e20e9ac4 control=0 result=e20e9ac4 overflow=0 testresult=e20e9ac4 testoverflow=0  pass=1 fail=0
1870clk=1 A=bf23327e B=e20e9ac4 control=0 result=e20e9ac4 overflow=0 testresult=e20e9ac4 testoverflow=0  pass=1 fail=0
1880clk=0 A=0aaa4b15 B=5c78b1b8 control=0 result=5c78b1b8 overflow=0 testresult=5c78b1b8 testoverflow=0  pass=1 fail=0
1890clk=1 A=0aaa4b15 B=5c78b1b8 control=0 result=5c78b1b8 overflow=0 testresult=5c78b1b8 testoverflow=0  pass=1 fail=0
1900clk=0 A=78d99bf1 B=dbe6f2b7 control=0 result=78d99bf1 overflow=0 testresult=78d99bf1 testoverflow=0  pass=1 fail=0
1910clk=1 A=78d99bf1 B=dbe6f2b7 control=0 result=78d99bf1 overflow=0 testresult=78d99bf1 testoverflow=0  pass=1 fail=0
1920clk=0 A=6c9c4bd9 B=c378ee86 control=0 result=6c9c4bd9 overflow=0 testresult=6c9c4bd9 testoverflow=0  pass=1 fail=0
1930clk=1 A=6c9c4bd9 B=c378ee86 control=0 result=6c9c4bd9 overflow=0 testresult=6c9c4bd9 testoverflow=0  pass=1 fail=0
1940clk=0 A=31230762 B=984d5a30 control=0 result=31230762 overflow=0 testresult=31230762 testoverflow=0  pass=1 fail=0
1950clk=1 A=31230762 B=984d5a30 control=0 result=31230762 overflow=0 testresult=31230762 testoverflow=0  pass=1 fail=0
1960clk=0 A=2635fb4c B=3bed5377 control=0 result=3bed5377 overflow=0 testresult=3bed5377 testoverflow=0  pass=1 fail=0
1970clk=1 A=2635fb4c B=3bed5377 control=0 result=3bed5377 overflow=0 testresult=3bed5377 testoverflow=0  pass=1 fail=0
1980clk=0 A=4fa1559f B=5ad6c7b5 control=0 result=5ad6c7b7 overflow=0 testresult=5ad6c7b7 testoverflow=0  pass=1 fail=0
1990clk=1 A=4fa1559f B=5ad6c7b5 control=0 result=5ad6c7b7 overflow=0 testresult=5ad6c7b7 testoverflow=0  pass=1 fail=0
2000clk=0 A=47b9a18f B=6a15f5d4 control=0 result=6a15f5d4 overflow=0 testresult=6a15f5d4 testoverflow=0  pass=1 fail=0
2010clk=1 A=47b9a18f B=6a15f5d4 control=0 result=6a15f5d4 overflow=0 testresult=6a15f5d4 testoverflow=0  pass=1 fail=0
2020clk=0 A=7c6da9f8 B=03878707 control=0 result=7c6da9f8 overflow=0 testresult=7c6da9f8 testoverflow=0  pass=1 fail=0
2030clk=1 A=7c6da9f8 B=03878707 control=0 result=7c6da9f8 overflow=0 testresult=7c6da9f8 testoverflow=0  pass=1 fail=0
2040clk=0 A=dbcd60b7 B=3b0b9776 control=0 result=dbcd60b7 overflow=0 testresult=dbcd60b7 testoverflow=0  pass=1 fail=0
2050clk=1 A=dbcd60b7 B=3b0b9776 control=0 result=dbcd60b7 overflow=0 testresult=dbcd60b7 testoverflow=0  pass=1 fail=0
2060clk=0 A=cfc4569f B=74a1ade9 control=0 result=74a1ade9 overflow=0 testresult=74a1ade9 testoverflow=0  pass=1 fail=0
2070clk=1 A=cfc4569f B=74a1ade9 control=0 result=74a1ade9 overflow=0 testresult=74a1ade9 testoverflow=0  pass=1 fail=0
2080clk=0 A=ae7d945c B=45e28b8b control=0 result=45e28b8b overflow=0 testresult=45e28b8b testoverflow=0  pass=1 fail=0
2090clk=1 A=ae7d945c B=45e28b8b control=0 result=45e28b8b overflow=0 testresult=45e28b8b testoverflow=0  pass=1 fail=0
2100clk=0 A=adcbc05b B=00f25f01 control=0 result=adcbc05b overflow=0 testresult=adcbc05b testoverflow=0  pass=1 fail=0
2110clk=1 A=adcbc05b B=00f25f01 control=0 result=adcbc05b overflow=0 testresult=adcbc05b testoverflow=0  pass=1 fail=0
2120clk=0 A=44de3789 B=6d808bdb control=0 result=6d808bdb overflow=0

testresult=6d808bdb testoverflow=0  pass=1 fail=0
2130clk=1 A=44de3789 B=6d808bdb control=0 result=6d808bdb overflow=0
testresult=6d808bdb testoverflow=0  pass=1 fail=0
2140clk=0 A=a4ae3249 B=c0764280 control=0 result=c0764280 overflow=0
testresult=c0764280 testoverflow=0  pass=1 fail=0
2150clk=1 A=a4ae3249 B=c0764280 control=0 result=c0764280 overflow=0
testresult=c0764280 testoverflow=0  pass=1 fail=0
2160clk=0 A=e8233ed0 B=611d9fc2 control=0 result=e8233c5a overflow=0
testresult=e8233c5a testoverflow=0  pass=1 fail=0
2170clk=1 A=e8233ed0 B=611d9fc2 control=0 result=e8233c5a overflow=0
testresult=e8233c5a testoverflow=0  pass=1 fail=0
2180clk=0 A=ebfec0d7 B=e2ecdac5 control=0 result=ebfec113 overflow=0
testresult=ebfec113 testoverflow=0  pass=1 fail=0
2190clk=1 A=ebfec0d7 B=e2ecdac5 control=0 result=ebfec113 overflow=0
testresult=ebfec113 testoverflow=0  pass=1 fail=0
2200clk=0 A=a8c7fc51 B=9827fa30 control=0 result=a8c7fc51 overflow=0
testresult=a8c7fc51 testoverflow=0  pass=1 fail=0
2210clk=1 A=a8c7fc51 B=9827fa30 control=0 result=a8c7fc51 overflow=0
testresult=a8c7fc51 testoverflow=0  pass=1 fail=0
2220clk=0 A=4b212f96 B=d7b2e4af control=0 result=d7b2e4af overflow=0
testresult=d7b2e4af testoverflow=0  pass=1 fail=0
2230clk=1 A=4b212f96 B=d7b2e4af control=0 result=d7b2e4af overflow=0
testresult=d7b2e4af testoverflow=0  pass=1 fail=0
2240clk=0 A=061d7f0c B=b302da66 control=0 result=b302da66 overflow=0
testresult=b302da66 testoverflow=0  pass=1 fail=0
2250clk=1 A=061d7f0c B=b302da66 control=0 result=b302da66 overflow=0
testresult=b302da66 testoverflow=0  pass=1 fail=0
2260clk=0 A=e12ccec2 B=57fbb9af control=0 result=e12ccea4 overflow=0
testresult=e12ccea4 testoverflow=0  pass=1 fail=0
2270clk=1 A=e12ccec2 B=57fbb9af control=0 result=e12ccea4 overflow=0
testresult=e12ccea4 testoverflow=0  pass=1 fail=0
2280clk=0 A=6457edc8 B=f4d86ee9 control=0 result=f4d86ee9 overflow=0
testresult=f4d86ee9 testoverflow=0  pass=1 fail=0
2290clk=1 A=6457edc8 B=f4d86ee9 control=0 result=f4d86ee9 overflow=0
testresult=f4d86ee9 testoverflow=0  pass=1 fail=0
2300clk=0 A=bb825a77 B=7c41aff8 control=0 result=7c41aff8 overflow=0
testresult=7c41aff8 testoverflow=0  pass=1 fail=0
2310clk=1 A=bb825a77 B=7c41aff8 control=0 result=7c41aff8 overflow=0
testresult=7c41aff8 testoverflow=0  pass=1 fail=0
2320clk=0 A=1ef2ed3d B=8376ac06 control=0 result=1ef2ed3d overflow=0
testresult=1ef2ed3d testoverflow=0  pass=1 fail=0
2330clk=1 A=1ef2ed3d B=8376ac06 control=0 result=1ef2ed3d overflow=0
testresult=1ef2ed3d testoverflow=0  pass=1 fail=0
2340clk=0 A=090cdb12 B=f78576ef control=0 result=f78576ef overflow=0
testresult=f78576ef testoverflow=0  pass=1 fail=0
2350clk=1 A=090cdb12 B=f78576ef control=0 result=f78576ef overflow=0
testresult=f78576ef testoverflow=0  pass=1 fail=0
2360clk=0 A=bf05007e B=70ef37e1 control=0 result=70ef37e1 overflow=0
testresult=70ef37e1 testoverflow=0  pass=1 fail=0
2370clk=1 A=bf05007e B=70ef37e1 control=0 result=70ef37e1 overflow=0
testresult=70ef37e1 testoverflow=0  pass=1 fail=0
2380clk=0 A=36e5816d B=cab47c95 control=0 result=cab47c95 overflow=0
testresult=cab47c95 testoverflow=0  pass=1 fail=0
2390clk=1 A=36e5816d B=cab47c95 control=0 result=cab47c95 overflow=0
testresult=cab47c95 testoverflow=0  pass=1 fail=0
2400clk=0 A=1cd9e739 B=f7723eee control=0 result=f7723eee overflow=0
testresult=f7723eee testoverflow=0  pass=1 fail=0
2410clk=1 A=1cd9e739 B=f7723eee control=0 result=f7723eee overflow=0
testresult=f7723eee testoverflow=0  pass=1 fail=0
2420clk=0 A=0fd28f1f B=304e4d60 control=0 result=304e4d60 overflow=0
testresult=304e4d60 testoverflow=0  pass=1 fail=0
2430clk=1 A=0fd28f1f B=304e4d60 control=0 result=304e4d60 overflow=0
testresult=304e4d60 testoverflow=0  pass=1 fail=0

2440clk=0 A=e9ebf6d3 B=f29c5ee5 control=0 result=f29c5f1f overflow=0 testresult=f29c5f1f testoverflow=0  pass=1 fail=0
2450clk=1 A=e9ebf6d3 B=f29c5ee5 control=0 result=f29c5f1f overflow=0 testresult=f29c5f1f testoverflow=0  pass=1 fail=0
2460clk=0 A=42d92f85 B=9420ea28 control=0 result=42d92f85 overflow=0 testresult=42d92f85 testoverflow=0  pass=1 fail=0
2470clk=1 A=42d92f85 B=9420ea28 control=0 result=42d92f85 overflow=0 testresult=42d92f85 testoverflow=0  pass=1 fail=0
2480clk=0 A=bc148878 B=322f7d64 control=0 result=bc14886e overflow=0 testresult=bc14886e testoverflow=0  pass=1 fail=0
2490clk=1 A=bc148878 B=322f7d64 control=0 result=bc14886e overflow=0 testresult=bc14886e testoverflow=0  pass=1 fail=0
2500clk=0 A=2dda595b B=14b43729 control=0 result=2dda595b overflow=0 testresult=2dda595b testoverflow=0  pass=1 fail=0
2510clk=1 A=2dda595b B=14b43729 control=0 result=2dda595b overflow=0 testresult=2dda595b testoverflow=0  pass=1 fail=0
2520clk=0 A=248b4b49 B=f0eeaee1 control=0 result=f0eeaee1 overflow=0 testresult=f0eeaee1 testoverflow=0  pass=1 fail=0
2530clk=1 A=248b4b49 B=f0eeaee1 control=0 result=f0eeaee1 overflow=0 testresult=f0eeaee1 testoverflow=0  pass=1 fail=0
2540clk=0 A=9ff2ae3f B=bbbc5277 control=0 result=bbbc5277 overflow=0 testresult=bbbc5277 testoverflow=0  pass=1 fail=0
2550clk=1 A=9ff2ae3f B=bbbc5277 control=0 result=bbbc5277 overflow=0 testresult=bbbc5277 testoverflow=0  pass=1 fail=0
2560clk=0 A=150caf2a B=3715156e control=0 result=3715156e overflow=0 testresult=3715156e testoverflow=0  pass=1 fail=0
2570clk=1 A=150caf2a B=3715156e control=0 result=3715156e overflow=0 testresult=3715156e testoverflow=0  pass=1 fail=0
2580clk=0 A=2c156358 B=40aaf581 control=0 result=40aaf581 overflow=0 testresult=40aaf581 testoverflow=0  pass=1 fail=0
2590clk=1 A=2c156358 B=40aaf581 control=0 result=40aaf581 overflow=0 testresult=40aaf581 testoverflow=0  pass=1 fail=0
2600clk=0 A=c33f3886 B=6a9fb9d5 control=0 result=6a9fb9d5 overflow=0 testresult=6a9fb9d5 testoverflow=0  pass=1 fail=0
2610clk=1 A=c33f3886 B=6a9fb9d5 control=0 result=6a9fb9d5 overflow=0 testresult=6a9fb9d5 testoverflow=0  pass=1 fail=0
2620clk=0 A=c71a0c8e B=3437d568 control=0 result=c71a0c8e overflow=0 testresult=c71a0c8e testoverflow=0  pass=1 fail=0
2630clk=1 A=c71a0c8e B=3437d568 control=0 result=c71a0c8e overflow=0 testresult=c71a0c8e testoverflow=0  pass=1 fail=0
2640clk=0 A=ce2ff29c B=786271f0 control=0 result=786271f0 overflow=0 testresult=786271f0 testoverflow=0  pass=1 fail=0
2650clk=1 A=ce2ff29c B=786271f0 control=0 result=786271f0 overflow=0 testresult=786271f0 testoverflow=0  pass=1 fail=0
2660clk=0 A=7d3599fa B=d57800aa control=0 result=7d3599fa overflow=0 testresult=7d3599fa testoverflow=0  pass=1 fail=0
2670clk=1 A=7d3599fa B=d57800aa control=0 result=7d3599fa overflow=0 testresult=7d3599fa testoverflow=0  pass=1 fail=0
2680clk=0 A=937dbc26 B=079fc30f control=0 result=937dbc26 overflow=0 testresult=937dbc26 testoverflow=0  pass=1 fail=0
2690clk=1 A=937dbc26 B=079fc30f control=0 result=937dbc26 overflow=0 testresult=937dbc26 testoverflow=0  pass=1 fail=0
2700clk=0 A=39961773 B=f8dc48f1 control=0 result=f8dc48f1 overflow=0 testresult=f8dc48f1 testoverflow=0  pass=1 fail=0
2710clk=1 A=39961773 B=f8dc48f1 control=0 result=f8dc48f1 overflow=0 testresult=f8dc48f1 testoverflow=0  pass=1 fail=0
2720clk=0 A=d18bb4a3 B=be9bbc7d control=0 result=d18bb4a3 overflow=0 testresult=d18bb4a3 testoverflow=0  pass=1 fail=0
2730clk=1 A=d18bb4a3 B=be9bbc7d control=0 result=d18bb4a3 overflow=0 testresult=d18bb4a3 testoverflow=0  pass=1 fail=0
2740clk=0 A=9799a82f B=472e958e control=0 result=472e958e overflow=0 testresult=472e958e testoverflow=0  pass=1 fail=0
2750clk=1 A=9799a82f B=472e958e control=0 result=472e958e overflow=0

testresult=472e958e testoverflow=0  pass=1 fail=0
                2760clk=0 A=d9d292b3 B=f161dce2 control=0 result=f161dce2 overflow=0
testresult=f161dce2 testoverflow=0  pass=1 fail=0
                2770clk=1 A=d9d292b3 B=f161dce2 control=0 result=f161dce2 overflow=0
testresult=f161dce2 testoverflow=0  pass=1 fail=0
                2780clk=0 A=afd8565f B=1e664d3c control=0 result=afd8565f overflow=0
testresult=afd8565f testoverflow=0  pass=1 fail=0
                2790clk=1 A=afd8565f B=1e664d3c control=0 result=afd8565f overflow=0
testresult=afd8565f testoverflow=0  pass=1 fail=0
                2800clk=0 A=22290d44 B=d4b5e6a9 control=0 result=d4b5e6a9 overflow=0
testresult=d4b5e6a9 testoverflow=0  pass=1 fail=0
                2810clk=1 A=22290d44 B=d4b5e6a9 control=0 result=d4b5e6a9 overflow=0
testresult=d4b5e6a9 testoverflow=0  pass=1 fail=0
                2820clk=0 A=7bf8fdf7 B=77ebb1ef control=0 result=7bf9e9a9 overflow=0
testresult=7bf9e9a9 testoverflow=0  pass=1 fail=0
                2830clk=1 A=7bf8fdf7 B=77ebb1ef control=0 result=7bf9e9a9 overflow=0
testresult=7bf9e9a9 testoverflow=0  pass=1 fail=0
                2840clk=0 A=e59b36cb B=ade7d05b control=0 result=e59b36cb overflow=0
testresult=e59b36cb testoverflow=0  pass=1 fail=0
                2850clk=1 A=e59b36cb B=ade7d05b control=0 result=e59b36cb overflow=0
testresult=e59b36cb testoverflow=0  pass=1 fail=0
                2860clk=0 A=f3091ae6 B=d7a23caf control=0 result=f3091ae6 overflow=0
testresult=f3091ae6 testoverflow=0  pass=1 fail=0
                2870clk=1 A=f3091ae6 B=d7a23caf control=0 result=f3091ae6 overflow=0
testresult=f3091ae6 testoverflow=0  pass=1 fail=0
                2880clk=0 A=2d28db5a B=25029b4a control=0 result=2d28dbdc overflow=0
testresult=2d28dbdc testoverflow=0  pass=1 fail=0
                2890clk=1 A=2d28db5a B=25029b4a control=0 result=2d28dbdc overflow=0
testresult=2d28dbdc testoverflow=0  pass=1 fail=0
                2900clk=0 A=14cfc129 B=5cd20db9 control=0 result=5cd20db9 overflow=0
testresult=5cd20db9 testoverflow=0  pass=1 fail=0
                2910clk=1 A=14cfc129 B=5cd20db9 control=0 result=5cd20db9 overflow=0
testresult=5cd20db9 testoverflow=0  pass=1 fail=0
                2920clk=0 A=f682e2ed B=098e2d13 control=0 result=f682e2ed overflow=0
testresult=f682e2ed testoverflow=0  pass=1 fail=0
                2930clk=1 A=f682e2ed B=098e2d13 control=0 result=f682e2ed overflow=0
testresult=f682e2ed testoverflow=0  pass=1 fail=0
                2940clk=0 A=ed536cda B=09c83513 control=0 result=ed536cda overflow=0
testresult=ed536cda testoverflow=0  pass=1 fail=0
                2950clk=1 A=ed536cda B=09c83513 control=0 result=ed536cda overflow=0
testresult=ed536cda testoverflow=0  pass=1 fail=0
                2960clk=0 A=b29fb665 B=32dc4165 control=0 result=b1f22c00 overflow=0
testresult=a7000000 testoverflow=0  pass=1 fail=0
                2970clk=1 A=b29fb665 B=32dc4165 control=0 result=b1f22c00 overflow=0
testresult=a7000000 testoverflow=0  pass=1 fail=0
                2980clk=0 A=da8ae2b5 B=28c62751 control=0 result=da8ae2b5 overflow=0
testresult=da8ae2b5 testoverflow=0  pass=1 fail=0
                2990clk=1 A=da8ae2b5 B=28c62751 control=0 result=da8ae2b5 overflow=0
testresult=da8ae2b5 testoverflow=0  pass=1 fail=0
                3000clk=0 A=efbe94df B=db983ab7 control=0 result=efbe94df overflow=0
testresult=efbe94df testoverflow=0  pass=1 fail=0
                3010clk=1 A=efbe94df B=db983ab7 control=0 result=efbe94df overflow=0
testresult=efbe94df testoverflow=0  pass=1 fail=0
                3020clk=0 A=3cf11979 B=cc981099 control=0 result=cc981099 overflow=0
testresult=cc981099 testoverflow=0  pass=1 fail=0
                3030clk=1 A=3cf11979 B=cc981099 control=0 result=cc981099 overflow=0
testresult=cc981099 testoverflow=0  pass=1 fail=0
                3040clk=0 A=2231ff44 B=9d12083a control=0 result=2231dac2 overflow=0
testresult=2231dac2 testoverflow=0  pass=1 fail=0
                3050clk=1 A=2231ff44 B=9d12083a control=0 result=2231dac2 overflow=0
testresult=2231dac2 testoverflow=0  pass=1 fail=0
                3060clk=0 A=e8740cd0 B=b8ea3a71 control=0 result=e8740cd0 overflow=0
testresult=e8740cd0 testoverflow=0  pass=1 fail=0

3070clk=1 A=e8740cd0 B=b8ea3a71 control=0 result=e8740cd0 overflow=0 testresult=e8740cd0 testoverflow=0  pass=1 fail=0
3080clk=0 A=15090b2a B=317c0762 control=0 result=317c0762 overflow=0 testresult=317c0762 testoverflow=0  pass=1 fail=0
3090clk=1 A=15090b2a B=317c0762 control=0 result=317c0762 overflow=0 testresult=317c0762 testoverflow=0  pass=1 fail=0
3100clk=0 A=55f6adab B=f2356ae4 control=0 result=f2356ae4 overflow=0 testresult=f2356ae4 testoverflow=0  pass=1 fail=0
3110clk=1 A=55f6adab B=f2356ae4 control=0 result=f2356ae4 overflow=0 testresult=f2356ae4 testoverflow=0  pass=1 fail=0
3120clk=0 A=076fcf0e B=1513dd2a control=0 result=1513dd2a overflow=0 testresult=1513dd2a testoverflow=0  pass=1 fail=0
3130clk=1 A=076fcf0e B=1513dd2a control=0 result=1513dd2a overflow=0 testresult=1513dd2a testoverflow=0  pass=1 fail=0
3140clk=0 A=6e5daddc B=beda447d control=0 result=6e5daddc overflow=0 testresult=6e5daddc testoverflow=0  pass=1 fail=0
3150clk=1 A=6e5daddc B=beda447d control=0 result=6e5daddc overflow=0 testresult=6e5daddc testoverflow=0  pass=1 fail=0
3160clk=0 A=cd5ebc9a B=2cee5f59 control=0 result=cd5ebc9a overflow=0 testresult=cd5ebc9a testoverflow=0  pass=1 fail=0
3170clk=1 A=cd5ebc9a B=2cee5f59 control=0 result=cd5ebc9a overflow=0 testresult=cd5ebc9a testoverflow=0  pass=1 fail=0
3180clk=0 A=fedf72fd B=72c3a3e5 control=0 result=fedf72fd overflow=0 testresult=fedf72fd testoverflow=0  pass=1 fail=0
3190clk=1 A=fedf72fd B=72c3a3e5 control=0 result=fedf72fd overflow=0 testresult=fedf72fd testoverflow=0  pass=1 fail=0
3200clk=0 A=e1f102c3 B=76de6bed control=0 result=76de6bed overflow=0 testresult=76de6bed testoverflow=0  pass=1 fail=0
3210clk=1 A=e1f102c3 B=76de6bed control=0 result=76de6bed overflow=0 testresult=76de6bed testoverflow=0  pass=1 fail=0
3220clk=0 A=2b0eed56 B=e4a800c9 control=0 result=e4a800c9 overflow=0 testresult=e4a800c9 testoverflow=0  pass=1 fail=0
3230clk=1 A=2b0eed56 B=e4a800c9 control=0 result=e4a800c9 overflow=0 testresult=e4a800c9 testoverflow=0  pass=1 fail=0
3240clk=0 A=2779e94e B=a0aecc41 control=0 result=2779e3d8 overflow=0 testresult=2779e3d8 testoverflow=0  pass=1 fail=0
3250clk=1 A=2779e94e B=a0aecc41 control=0 result=2779e3d8 overflow=0 testresult=2779e3d8 testoverflow=0  pass=1 fail=0
3260clk=0 A=b3d97667 B=57c1d1af control=0 result=57c1d1af overflow=0 testresult=57c1d1af testoverflow=0  pass=1 fail=0
3270clk=1 A=b3d97667 B=57c1d1af control=0 result=57c1d1af overflow=0 testresult=57c1d1af testoverflow=0  pass=1 fail=0
3280clk=0 A=8531340a B=eda71cdb control=0 result=eda71cdb overflow=0 testresult=eda71cdb testoverflow=0  pass=1 fail=0
3290clk=1 A=8531340a B=eda71cdb control=0 result=eda71cdb overflow=0 testresult=eda71cdb testoverflow=0  pass=1 fail=0
3300clk=0 A=5b6fb9b6 B=e696e8cd control=0 result=e696e8cd overflow=0 testresult=e696e8cd testoverflow=0  pass=1 fail=0
3310clk=1 A=5b6fb9b6 B=e696e8cd control=0 result=e696e8cd overflow=0 testresult=e696e8cd testoverflow=0  pass=1 fail=0
3320clk=0 A=9c0e8a38 B=38139f70 control=0 result=38139f70 overflow=0 testresult=38139f70 testoverflow=0  pass=1 fail=0
3330clk=1 A=9c0e8a38 B=38139f70 control=0 result=38139f70 overflow=0 testresult=38139f70 testoverflow=0  pass=1 fail=0
3340clk=0 A=3cd18779 B=8326d406 control=0 result=3cd18779 overflow=0 testresult=3cd18779 testoverflow=0  pass=1 fail=0
3350clk=1 A=3cd18779 B=8326d406 control=0 result=3cd18779 overflow=0 testresult=3cd18779 testoverflow=0  pass=1 fail=0
3360clk=0 A=dc2bc4b8 B=d14820a2 control=0 result=dc2bc4bc overflow=0 testresult=dc2bc4bc testoverflow=0  pass=1 fail=0
3370clk=1 A=dc2bc4b8 B=d14820a2 control=0 result=dc2bc4bc overflow=0 testresult=dc2bc4bc testoverflow=0  pass=1 fail=0
3380clk=0 A=4a74bf94 B=5e983dbd control=0 result=5e983dbd overflow=0

```
testresult=5e983dbd testoverflow=0  pass=1 fail=0
                3390clk=1 A=4a74bf94 B=5e983dbd control=0 result=5e983dbd overflow=0
testresult=5e983dbd testoverflow=0  pass=1 fail=0
                3400clk=0 A=49c65d93 B=b555de6a control=0 result=49c65d93 overflow=0
testresult=49c65d93 testoverflow=0  pass=1 fail=0
                3410clk=1 A=49c65d93 B=b555de6a control=0 result=49c65d93 overflow=0
testresult=49c65d93 testoverflow=0  pass=1 fail=0
                3420clk=0 A=823f2c04 B=6e3d47dc control=0 result=6e3d47dc overflow=0
testresult=6e3d47dc testoverflow=0  pass=1 fail=0
                3430clk=1 A=823f2c04 B=6e3d47dc control=0 result=6e3d47dc overflow=0
testresult=6e3d47dc testoverflow=0  pass=1 fail=0
                3440clk=0 A=acb7ca59 B=a86c5e50 control=0 result=acb84089 overflow=0
testresult=acb84089 testoverflow=0  pass=1 fail=0
                3450clk=1 A=acb7ca59 B=a86c5e50 control=0 result=acb84089 overflow=0
testresult=acb84089 testoverflow=0  pass=1 fail=0
                3460clk=0 A=6dcb69db B=bd86f47b control=0 result=6dcb69db overflow=0
testresult=6dcb69db testoverflow=0  pass=1 fail=0
                3470clk=1 A=6dcb69db B=bd86f47b control=0 result=6dcb69db overflow=0
testresult=6dcb69db testoverflow=0  pass=1 fail=0
                3480clk=0 A=a6fcde4d B=929d5825 control=0 result=a6fcde4d overflow=0
testresult=a6fcde4d testoverflow=0  pass=1 fail=0
                3490clk=1 A=a6fcde4d B=929d5825 control=0 result=a6fcde4d overflow=0
testresult=a6fcde4d testoverflow=0  pass=1 fail=0
$finish called from file "fpalu_fixture.v", line 130.
$finish at simulation time                 3500
           V C S   S i m u l a t i o n   R e p o r t
Time: 3500
CPU Time:      0.500 seconds;       Data structure size:   0.1Mb
Wed May  4 14:27:44 2016
```

# Script File

```
#Read the design in
read_file -format verilog {"top_fpalu.v"}

#set the current design
set current_design top_fpalu
#Link the design
link

#create clockand constrain the design
create_clock "clk" -period 5      -name  "clk"
set_input_delay -clock clk  -max -rise 0.35 "A"
set_input_delay -clock clk  -min -rise 0.1  "A"
set_input_delay -clock clk  -max -rise 0.35 "B"
set_input_delay -clock clk  -min -rise 0.1  "B"
set_input_delay -clock clk  -max -rise 0.35 "start"
set_input_delay -clock clk  -min -rise 0.1  "start"
set_input_delay -clock clk  -max -rise 0.35 "control"
set_input_delay -clock clk  -min -rise 0.1  "control"


set_output_delay -clock clk  -max -rise 0.8 "result"
set_output_delay -clock clk  -min -rise 0.2 "result"
set_output_delay -clock clk  -max -rise 0.8 "overflow"
set_output_delay -clock clk  -min -rise 0.2 "overflow"

set_max_fanout 3 "clk"
set_ideal_network "clk"
set_dont_touch_network  "clk"
set_max_area 0

#Set operating conditions
set_operating_conditions -library "saed90nm_typ" "TYPICAL"
#Synthesize and generate report
compile  -map_effort high -boundary_optimization
report_attribute >  report1
report_area >  report2
report_constraints -all_violators > report3
report_timing -path full -delay max -max_paths 1 -nworst 1  > report4
report_net_fanout -high_fanout > report5
report_app_var > report6
```

# REPORT: 3

****************************************

Report : constraint

-all_violators

Design : top_fpalu

Version: I-2013.12-SP5-4

Date : Wed May 4 13:49:08 2016

****************************************

max_area

| Design | Required Area | Actual Area | Slack |
|---|---|---|---|
| top_fpalu | 0.00 | 382089.34 | -382089.34 (VIOLATED) |

# REPORT: 4

**********

Report : timing

-path full

-delay max

-max_paths 1

Design : top_fpalu

Version: I-2013.12-SP5-4

Date : Wed May 4 13:49:09 2016

**********

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: TYPICAL Library: saed90nm_typ

Wire Load Model Mode: enclosed

Startpoint: uut1/ff1/t1/t1/t2/b1/s_reg

(rising edge-triggered flip-flop clocked by clk)

Endpoint: uut1/ff1/t1/t1/t2/f1/shiftp_reg[22]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

| Des/Clust/Port | Wire Load Model | Library |
|---|---|---|
| top_fpalu | 540000 | saed90nm_typ |
| multiplication_0 | 8000 | saed90nm_typ |
| adder_0_DW01_add_0 | 8000 | saed90nm_typ |

finalshift_0 8000 saed90nm_typ

Point Incr Path

---

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

uut1/ff1/t1/t1/t2/b1/s_reg/CLK (DFFARX1) 0.00 # 0.00 r

uut1/ff1/t1/t1/t2/b1/s_reg/Q (DFFARX1) 0.18 0.18 r

uut1/ff1/t1/t1/t2/b1/s (dffb_0) 0.00 0.18 r

uut1/ff1/t1/t1/t2/m1/s (mux_0) 0.00 0.18 r

uut1/ff1/t1/t1/t2/m1/U24/Q (AND2X1) 0.12 0.30 r

uut1/ff1/t1/t1/t2/m1/y[1] (mux_0) 0.00 0.30 r

uut1/ff1/t1/t1/t2/a2/b[1] (adder_0) 0.00 0.30 r

uut1/ff1/t1/t1/t2/a2/add_6/B[1] (adder_0_DW01_add_0)

0.00 0.30 r

uut1/ff1/t1/t1/t2/a2/add_6/U124/QN (NAND2X0) 0.07 0.37 f

uut1/ff1/t1/t1/t2/a2/add_6/U129/QN (NAND2X0) 0.07 0.44 r

uut1/ff1/t1/t1/t2/a2/add_6/U131/Q (AND2X1) 0.10 0.55 r

uut1/ff1/t1/t1/t2/a2/add_6/U63/QN (NAND2X0) 0.08 0.62 f

uut1/ff1/t1/t1/t2/a2/add_6/U65/QN (NAND3X0) 0.10 0.73 r

uut1/ff1/t1/t1/t2/a2/add_6/U66/QN (NAND2X0) 0.08 0.81 f

uut1/ff1/t1/t1/t2/a2/add_6/U69/QN (NAND3X0) 0.10 0.91 r

uut1/ff1/t1/t1/t2/a2/add_6/U74/QN (NAND2X0) 0.08 0.99 f

uut1/ff1/t1/t1/t2/a2/add_6/U77/QN (NAND3X0) 0.10 1.09 r

uut1/ff1/t1/t1/t2/a2/add_6/U83/QN (NAND2X0) 0.08 1.17 f

uut1/ff1/t1/t1/t2/a2/add_6/U86/QN (NAND3X0) 0.10 1.28 r

uut1/ff1/t1/t1/t2/a2/add_6/U108/QN (NAND2X0) 0.08 1.36 f

uut1/ff1/t1/t1/t2/a2/add_6/U109/QN (NAND3X0) 0.10 1.46 r

uut1/ff1/t1/t1/t2/a2/add_6/U111/QN (NAND2X0) 0.08 1.54 f

| | | |
|---|---|---|
| uut1/ff1/t1/t1/t2/a2/add_6/U113/QN (NAND3X0) | 0.11 | 1.65 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U45/QN (NAND2X0) | 0.08 | 1.73 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U46/QN (NAND3X0) | 0.10 | 1.83 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U48/QN (NAND2X0) | 0.08 | 1.91 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U50/QN (NAND3X0) | 0.11 | 2.02 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U1_10/CO (FADDX1) | 0.28 | 2.30 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U1_11/CO (FADDX1) | 0.27 | 2.57 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U40/QN (NAND2X0) | 0.08 | 2.64 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U42/QN (NAND3X0) | 0.10 | 2.75 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U53/QN (NAND2X0) | 0.08 | 2.83 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U54/QN (NAND3X0) | 0.10 | 2.93 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U58/QN (NAND2X0) | 0.08 | 3.01 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U60/QN (NAND3X0) | 0.11 | 3.12 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U116/QN (NAND2X0) | 0.08 | 3.20 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U117/QN (NAND3X0) | 0.10 | 3.30 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U121/QN (NAND2X0) | 0.08 | 3.38 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U123/QN (NAND3X0) | 0.10 | 3.48 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U35/QN (NAND2X0) | 0.08 | 3.57 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U37/QN (NAND3X0) | 0.10 | 3.67 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U79/QN (NAND2X0) | 0.08 | 3.75 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U82/QN (NAND3X0) | 0.10 | 3.86 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U99/QN (NAND2X0) | 0.08 | 3.94 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U100/QN (NAND3X0) | 0.11 | 4.04 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U104/QN (NAND2X0) | 0.08 | 4.12 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U105/QN (NAND3X0) | 0.10 | 4.23 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U70/QN (NAND2X0) | 0.08 | 4.31 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U73/QN (NAND3X0) | 0.10 | 4.41 r |
| uut1/ff1/t1/t1/t2/a2/add_6/U89/QN (NAND2X0) | 0.08 | 4.49 f |
| uut1/ff1/t1/t1/t2/a2/add_6/U90/QN (NAND3X0) | 0.11 | 4.60 r |

uut1/ff1/t1/t1/t2/a2/add_6/U92/Q (XOR2X1) 0.17 4.77 r

uut1/ff1/t1/t1/t2/a2/add_6/SUM[23] (adder_0_DW01_add_0)

0.00 4.77 r

uut1/ff1/t1/t1/t2/a2/sum[23] (adder_0) 0.00 4.77 r

uut1/ff1/t1/t1/t2/f1/sum[23] (finalshift_0) 0.00 4.77 r

uut1/ff1/t1/t1/t2/f1/U24/Q (AO22X1) 0.11 4.88 r

uut1/ff1/t1/t1/t2/f1/shiftp_reg[22]/D (DFFARX1) 0.03 4.91 r

data arrival time 4.91

clock clk (rise edge) 5.00 5.00

clock network delay (ideal) 0.00 5.00

uut1/ff1/t1/t1/t2/f1/shiftp_reg[22]/CLK (DFFARX1) 0.00 5.00 r

library setup time -0.09 4.91

data required time 4.91

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data required time 4.91

data arrival time -4.91

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slack (MET) 0.00

# REPORT: 5

**********

Report : net fanout

-high_fanout

Design : top_fpalu

Version: I-2013.12-SP5-4

Date : Wed May 4 13:49:09 2016

**********

Operating Conditions: TYPICAL Library: saed90nm_typ

Wire Load Model Mode: enclosed

| Design | Wire Load Model | Library |
|---|---|---|
| top_fpalu | 540000 | saed90nm_typ |
| fp_multiplication | 540000 | saed90nm_typ |
| fp_addition | 35000 | saed90nm_typ |
| fp_multiplication_outputpipe | 540000 | saed90nm_typ |
| fp_multiplication_input_pipe1 | 35000 | saed90nm_typ |
| fp_multiplication_input_pipe2 | 35000 | saed90nm_typ |
| fp_multiplication_round_normalized_0 | 16000 | saed90nm_typ |
| fp_multiplication_prenormalization_0 | 8000 | saed90nm_typ |

fsm_multiplication_0 8000 saed90nm_typ

multiplication_0 8000 saed90nm_typ

dffa_0 8000 saed90nm_typ

dffb_0 8000 saed90nm_typ

mux_0 8000 saed90nm_typ

finalshift_0 8000 saed90nm_typ

adder_0 8000 saed90nm_typ

fp_multiplication_round_normalized_1

16000 saed90nm_typ

fp_multiplication_round_normalized_2

16000 saed90nm_typ

fp_multiplication_round_normalized_3

16000 saed90nm_typ

fp_multiplication_round_normalized_4

16000 saed90nm_typ

fp_multiplication_round_normalized_5

16000 saed90nm_typ

fp_multiplication_round_normalized_6

16000 saed90nm_typ

fp_multiplication_round_normalized_7

16000 saed90nm_typ

fp_multiplication_round_normalized_8

16000 saed90nm_typ

fp_multiplication_round_normalized_9

16000 saed90nm_typ

fp_multiplication_round_normalized_10

16000 saed90nm_typ

fp_multiplication_round_normalized_11

16000 saed90nm_typ

fp_multiplication_round_normalized_12

16000 saed90nm_typ

fp_multiplication_round_normalized_13

16000 saed90nm_typ

fp_multiplication_round_normalized_14

16000 saed90nm_typ

fp_multiplication_round_normalized_15

16000 saed90nm_typ

fp_multiplication_round_normalized_16

16000 saed90nm_typ

fp_multiplication_round_normalized_17

16000 saed90nm_typ

fp_multiplication_round_normalized_18

16000 saed90nm_typ

fp_multiplication_round_normalized_19

16000 saed90nm_typ

fp_multiplication_round_normalized_20

16000 saed90nm_typ

fp_multiplication_round_normalized_21

16000 saed90nm_typ

fp_multiplication_round_normalized_22

16000 saed90nm_typ

fp_multiplication_round_normalized_23

16000 saed90nm_typ

fp_multiplication_round_normalized_24

16000 saed90nm_typ

fp_multiplication_round_normalized_25

16000 saed90nm_typ

fp_multiplication_round_normalized_26

16000 saed90nm_typ

fp_multiplication_round_normalized_27

16000 saed90nm_typ

fp_multiplication_prenormalization_1

8000 saed90nm_typ

fp_multiplication_prenormalization_2

8000 saed90nm_typ

fp_multiplication_prenormalization_3

8000 saed90nm_typ

fp_multiplication_prenormalization_4

8000 saed90nm_typ

fp_multiplication_prenormalization_5

8000 saed90nm_typ

fp_multiplication_prenormalization_6

8000 saed90nm_typ

fp_multiplication_prenormalization_7

8000 saed90nm_typ

fp_multiplication_prenormalization_8

8000 saed90nm_typ

fp_multiplication_prenormalization_9

8000 saed90nm_typ

fp_multiplication_prenormalization_10

8000 saed90nm_typ

fp_multiplication_prenormalization_11

8000 saed90nm_typ

fp_multiplication_prenormalization_12

8000 saed90nm_typ

fp_multiplication_prenormalization_13

8000 saed90nm_typ

fp_multiplication_prenormalization_14

8000 saed90nm_typ

fp_multiplication_prenormalization_15

8000 saed90nm_typ

fp_multiplication_prenormalization_16

8000 saed90nm_typ

fp_multiplication_prenormalization_17

8000 saed90nm_typ

fp_multiplication_prenormalization_18

8000 saed90nm_typ

fp_multiplication_prenormalization_19

8000 saed90nm_typ

fp_multiplication_prenormalization_20

8000 saed90nm_typ

fp_multiplication_prenormalization_21

8000 saed90nm_typ

fp_multiplication_prenormalization_22

8000 saed90nm_typ

fp_multiplication_prenormalization_23

8000 saed90nm_typ

fp_multiplication_prenormalization_24

8000 saed90nm_typ

fp_multiplication_prenormalization_25

8000 saed90nm_typ

fp_multiplication_prenormalization_26

8000 saed90nm_typ

fp_multiplication_prenormalization_27

8000 saed90nm_typ

fsm_multiplication_1 8000 saed90nm_typ

| | | |
|---|---|---|
| fsm_multiplication_2 | 8000 | saed90nm_typ |
| fsm_multiplication_3 | 8000 | saed90nm_typ |
| fsm_multiplication_4 | 8000 | saed90nm_typ |
| fsm_multiplication_5 | 8000 | saed90nm_typ |
| fsm_multiplication_6 | 8000 | saed90nm_typ |
| fsm_multiplication_7 | 8000 | saed90nm_typ |
| fsm_multiplication_8 | 8000 | saed90nm_typ |
| fsm_multiplication_9 | 8000 | saed90nm_typ |
| fsm_multiplication_10 | 8000 | saed90nm_typ |
| fsm_multiplication_11 | 8000 | saed90nm_typ |
| fsm_multiplication_12 | 8000 | saed90nm_typ |
| fsm_multiplication_13 | 8000 | saed90nm_typ |
| fsm_multiplication_14 | 8000 | saed90nm_typ |
| fsm_multiplication_15 | 8000 | saed90nm_typ |
| fsm_multiplication_16 | 8000 | saed90nm_typ |
| fsm_multiplication_17 | 8000 | saed90nm_typ |
| fsm_multiplication_18 | 8000 | saed90nm_typ |
| fsm_multiplication_19 | 8000 | saed90nm_typ |
| fsm_multiplication_20 | 8000 | saed90nm_typ |
| fsm_multiplication_21 | 8000 | saed90nm_typ |
| fsm_multiplication_22 | 8000 | saed90nm_typ |
| fsm_multiplication_23 | 8000 | saed90nm_typ |
| fsm_multiplication_24 | 8000 | saed90nm_typ |
| fsm_multiplication_25 | 8000 | saed90nm_typ |
| fsm_multiplication_26 | 8000 | saed90nm_typ |
| fsm_multiplication_27 | 8000 | saed90nm_typ |
| multiplication_1 | 8000 | saed90nm_typ |
| multiplication_2 | 8000 | saed90nm_typ |
| multiplication_3 | 8000 | saed90nm_typ |

multiplication_4 8000 saed90nm_typ

multiplication_5 8000 saed90nm_typ

multiplication_6 8000 saed90nm_typ

multiplication_7 8000 saed90nm_typ

multiplication_8 8000 saed90nm_typ

multiplication_9 8000 saed90nm_typ

multiplication_10 8000 saed90nm_typ

multiplication_11 8000 saed90nm_typ

multiplication_12 8000 saed90nm_typ

multiplication_13 8000 saed90nm_typ

multiplication_14 8000 saed90nm_typ

multiplication_15 8000 saed90nm_typ

multiplication_16 8000 saed90nm_typ

multiplication_17 8000 saed90nm_typ

multiplication_18 8000 saed90nm_typ

multiplication_19 8000 saed90nm_typ

multiplication_20 8000 saed90nm_typ

multiplication_21 8000 saed90nm_typ

multiplication_22 8000 saed90nm_typ

multiplication_23 8000 saed90nm_typ

multiplication_24 8000 saed90nm_typ

multiplication_25 8000 saed90nm_typ

multiplication_26 8000 saed90nm_typ

multiplication_27 8000 saed90nm_typ

dffa_1 8000 saed90nm_typ

dffa_2 8000 saed90nm_typ

dffa_3 8000 saed90nm_typ

dffa_4 8000 saed90nm_typ

dffa_5 8000 saed90nm_typ

| | | |
|---|---|---|
| dffa_6 | 8000 | saed90nm_typ |
| dffa_7 | 8000 | saed90nm_typ |
| dffa_8 | 8000 | saed90nm_typ |
| dffa_9 | 8000 | saed90nm_typ |
| dffa_10 | 8000 | saed90nm_typ |
| dffa_11 | 8000 | saed90nm_typ |
| dffa_12 | 8000 | saed90nm_typ |
| dffa_13 | 8000 | saed90nm_typ |
| dffa_14 | 8000 | saed90nm_typ |
| dffa_15 | 8000 | saed90nm_typ |
| dffa_16 | 8000 | saed90nm_typ |
| dffa_17 | 8000 | saed90nm_typ |
| dffa_18 | 8000 | saed90nm_typ |
| dffa_19 | 8000 | saed90nm_typ |
| dffa_20 | 8000 | saed90nm_typ |
| dffa_21 | 8000 | saed90nm_typ |
| dffa_22 | 8000 | saed90nm_typ |
| dffa_23 | 8000 | saed90nm_typ |
| dffa_24 | 8000 | saed90nm_typ |
| dffa_25 | 8000 | saed90nm_typ |
| dffa_26 | 8000 | saed90nm_typ |
| dffa_27 | 8000 | saed90nm_typ |
| dffb_1 | 8000 | saed90nm_typ |
| dffb_2 | 8000 | saed90nm_typ |
| dffb_3 | 8000 | saed90nm_typ |
| dffb_4 | 8000 | saed90nm_typ |
| dffb_5 | 8000 | saed90nm_typ |
| dffb_6 | 8000 | saed90nm_typ |
| dffb_7 | 8000 | saed90nm_typ |

| | | |
|---|---|---|
| dffb_8 | 8000 | saed90nm_typ |
| dffb_9 | 8000 | saed90nm_typ |
| dffb_10 | 8000 | saed90nm_typ |
| dffb_11 | 8000 | saed90nm_typ |
| dffb_12 | 8000 | saed90nm_typ |
| dffb_13 | 8000 | saed90nm_typ |
| dffb_14 | 8000 | saed90nm_typ |
| dffb_15 | 8000 | saed90nm_typ |
| dffb_16 | 8000 | saed90nm_typ |
| dffb_17 | 8000 | saed90nm_typ |
| dffb_18 | 8000 | saed90nm_typ |
| dffb_19 | 8000 | saed90nm_typ |
| dffb_20 | 8000 | saed90nm_typ |
| dffb_21 | 8000 | saed90nm_typ |
| dffb_22 | 8000 | saed90nm_typ |
| dffb_23 | 8000 | saed90nm_typ |
| dffb_24 | 8000 | saed90nm_typ |
| dffb_25 | 8000 | saed90nm_typ |
| dffb_26 | 8000 | saed90nm_typ |
| dffb_27 | 8000 | saed90nm_typ |
| mux_1 | ForQA | saed90nm_typ |
| mux_2 | 8000 | saed90nm_typ |
| mux_3 | ForQA | saed90nm_typ |
| mux_4 | ForQA | saed90nm_typ |
| mux_5 | ForQA | saed90nm_typ |
| mux_6 | ForQA | saed90nm_typ |
| mux_7 | ForQA | saed90nm_typ |
| mux_8 | ForQA | saed90nm_typ |
| mux_9 | ForQA | saed90nm_typ |

| | | |
|---|---|---|
| mux_10 | ForQA | saed90nm_typ |
| mux_11 | ForQA | saed90nm_typ |
| mux_12 | ForQA | saed90nm_typ |
| mux_13 | ForQA | saed90nm_typ |
| mux_14 | ForQA | saed90nm_typ |
| mux_15 | ForQA | saed90nm_typ |
| mux_16 | ForQA | saed90nm_typ |
| mux_17 | ForQA | saed90nm_typ |
| mux_18 | ForQA | saed90nm_typ |
| mux_19 | ForQA | saed90nm_typ |
| mux_20 | ForQA | saed90nm_typ |
| mux_21 | ForQA | saed90nm_typ |
| mux_22 | ForQA | saed90nm_typ |
| mux_23 | ForQA | saed90nm_typ |
| mux_24 | ForQA | saed90nm_typ |
| mux_25 | 8000 | saed90nm_typ |
| mux_26 | 8000 | saed90nm_typ |
| mux_27 | ForQA | saed90nm_typ |
| finalshift_1 | 8000 | saed90nm_typ |
| finalshift_2 | 8000 | saed90nm_typ |
| finalshift_3 | 8000 | saed90nm_typ |
| finalshift_4 | 8000 | saed90nm_typ |
| finalshift_5 | 8000 | saed90nm_typ |
| finalshift_6 | 8000 | saed90nm_typ |
| finalshift_7 | 8000 | saed90nm_typ |
| finalshift_8 | 8000 | saed90nm_typ |
| finalshift_9 | 8000 | saed90nm_typ |
| finalshift_10 | 8000 | saed90nm_typ |
| finalshift_11 | 8000 | saed90nm_typ |

| | | |
|---|---|---|
| finalshift_12 | 8000 | saed90nm_typ |
| finalshift_13 | 8000 | saed90nm_typ |
| finalshift_14 | 8000 | saed90nm_typ |
| finalshift_15 | 8000 | saed90nm_typ |
| finalshift_16 | 8000 | saed90nm_typ |
| finalshift_17 | 8000 | saed90nm_typ |
| finalshift_18 | 8000 | saed90nm_typ |
| finalshift_19 | 8000 | saed90nm_typ |
| finalshift_20 | 8000 | saed90nm_typ |
| finalshift_21 | 8000 | saed90nm_typ |
| finalshift_22 | 8000 | saed90nm_typ |
| finalshift_23 | 8000 | saed90nm_typ |
| finalshift_24 | 8000 | saed90nm_typ |
| finalshift_25 | 8000 | saed90nm_typ |
| finalshift_26 | 8000 | saed90nm_typ |
| finalshift_27 | 8000 | saed90nm_typ |
| adder_1 | 8000 | saed90nm_typ |
| adder_2 | 8000 | saed90nm_typ |
| adder_3 | 8000 | saed90nm_typ |
| adder_4 | 8000 | saed90nm_typ |
| adder_5 | 8000 | saed90nm_typ |
| adder_6 | 8000 | saed90nm_typ |
| adder_7 | 8000 | saed90nm_typ |
| adder_8 | 8000 | saed90nm_typ |
| adder_9 | 8000 | saed90nm_typ |
| adder_10 | 8000 | saed90nm_typ |
| adder_11 | 8000 | saed90nm_typ |
| adder_12 | 8000 | saed90nm_typ |
| adder_13 | 8000 | saed90nm_typ |

adder_14 8000 saed90nm_typ

adder_15 8000 saed90nm_typ

adder_16 8000 saed90nm_typ

adder_17 8000 saed90nm_typ

adder_18 8000 saed90nm_typ

adder_19 8000 saed90nm_typ

adder_20 8000 saed90nm_typ

adder_21 8000 saed90nm_typ

adder_22 8000 saed90nm_typ

adder_23 8000 saed90nm_typ

adder_24 8000 saed90nm_typ

adder_25 8000 saed90nm_typ

adder_26 8000 saed90nm_typ

adder_27 8000 saed90nm_typ

fp_addition_DW01_inc_0 ForQA saed90nm_typ

fp_addition_DW01_inc_1 8000 saed90nm_typ

fp_addition_DW01_inc_2 8000 saed90nm_typ

fp_addition_DW01_inc_3 ForQA saed90nm_typ

fp_addition_DW01_sub_21

8000 saed90nm_typ

fp_addition_DW01_sub_22

8000 saed90nm_typ

fp_addition_DW01_add_0 8000 saed90nm_typ

fp_addition_DW_rash_0 8000 saed90nm_typ

fp_addition_DW_rash_1 8000 saed90nm_typ

fp_addition_DW01_sub_23

8000 saed90nm_typ

fp_addition_DW01_sub_24

8000 saed90nm_typ

fp_multiplication_round_normalized_1_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_1_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_1_DW01_inc_1

8000 saed90nm_typ

adder_1_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_2_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_2_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_2_DW01_inc_1

8000 saed90nm_typ

adder_2_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_3_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_3_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_3_DW01_inc_1

8000 saed90nm_typ

adder_3_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_4_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_4_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_4_DW01_inc_1

8000 saed90nm_typ

adder_4_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_5_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_5_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_5_DW01_inc_1

8000 saed90nm_typ

adder_5_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_6_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_6_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_6_DW01_inc_1

8000 saed90nm_typ

adder_6_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_7_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_7_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_7_DW01_inc_1

8000 saed90nm_typ

adder_7_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_8_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_8_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_8_DW01_inc_1

8000 saed90nm_typ

adder_8_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_9_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_9_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_9_DW01_inc_1

8000 saed90nm_typ

adder_9_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_10_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_10_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_10_DW01_inc_1

8000 saed90nm_typ

adder_10_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_11_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_11_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_11_DW01_inc_1

8000 saed90nm_typ

adder_11_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_12_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_12_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_12_DW01_inc_1

8000 saed90nm_typ

adder_12_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_13_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_13_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_13_DW01_inc_1

8000 saed90nm_typ

adder_13_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_14_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_14_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_14_DW01_inc_1

8000 saed90nm_typ

adder_14_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_15_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_15_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_15_DW01_inc_1

8000 saed90nm_typ

adder_15_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_16_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_16_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_16_DW01_inc_1

8000 saed90nm_typ

adder_16_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_17_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_17_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_17_DW01_inc_1

8000 saed90nm_typ

adder_17_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_18_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_18_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_18_DW01_inc_1

8000 saed90nm_typ

adder_18_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_19_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_19_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_19_DW01_inc_1

8000 saed90nm_typ

adder_19_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_20_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_20_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_20_DW01_inc_1

8000 saed90nm_typ

adder_20_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_21_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_21_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_21_DW01_inc_1

8000 saed90nm_typ

adder_21_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_22_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_22_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_22_DW01_inc_1

8000 saed90nm_typ

adder_22_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_23_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_23_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_23_DW01_inc_1

8000 saed90nm_typ

adder_23_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_24_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_24_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_24_DW01_inc_1

8000 saed90nm_typ

adder_24_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_25_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_25_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_25_DW01_inc_1

8000 saed90nm_typ

adder_25_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_26_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_26_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_26_DW01_inc_1

8000 saed90nm_typ

adder_26_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_27_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_27_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_27_DW01_inc_1

8000 saed90nm_typ

adder_27_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_0_DW01_add_0

8000 saed90nm_typ

fp_multiplication_prenormalization_0_DW01_inc_0

8000 saed90nm_typ

fp_multiplication_prenormalization_0_DW01_inc_1

8000 saed90nm_typ

adder_0_DW01_add_0 8000 saed90nm_typ

fp_multiplication_round_normalized_0_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_27_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_26_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_24_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_23_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_22_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_21_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_20_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_19_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_18_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_17_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_16_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_15_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_25_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_14_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_13_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_12_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_10_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_9_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_8_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_7_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_6_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_5_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_4_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_3_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_2_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_1_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_11_DW01_add_1

8000 saed90nm_typ

fp_multiplication_round_normalized_0_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_0_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_27_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_27_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_26_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_26_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_24_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_24_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_23_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_23_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_22_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_22_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_21_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_21_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_20_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_20_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_19_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_19_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_18_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_18_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_17_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_17_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_16_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_16_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_15_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_15_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_25_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_25_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_14_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_14_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_13_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_13_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_12_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_12_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_10_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_10_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_9_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_9_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_8_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_8_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_7_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_7_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_6_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_6_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_5_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_5_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_4_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_4_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_3_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_3_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_2_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_2_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_1_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_1_DW01_inc_1

ForQA saed90nm_typ

fp_multiplication_round_normalized_11_DW01_inc_0

ForQA saed90nm_typ

fp_multiplication_round_normalized_11_DW01_inc_1

ForQA saed90nm_typ

Attributes:

dr - drc disabled

c - annotated capacitance

d - dont_touch

i - ideal_net

I - ideal_network

p - includes pin load

r - annotated resistance

h - high fanout

Net Fanout Attributes Capacitance Driver

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clk 2258 dr, d, I, h 0.00 clk

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# Design Module List



**Total Module Definition Coverage Summary**

| SCORE | LINE | COND | TOGGLE | FSM |
|---|---|---|---|---|
| 68.35 | 88.03 | 58.10 | 76.74 | 50.53 |

Total modules in report: 21

| SCORE | LINE | COND | TOGGLE | FSM | NAME |
|---|---|---|---|---|---|
| 56.40 | 60.94 | 33.33 | 97.98 | 33.33 | top_fpalu |
| 56.40 | 60.94 | 33.33 | 97.98 | 33.33 | fpalu_verification |
| 65.92 | 97.85 | 50.00 | 65.38 | 50.46 | fp_multiplication_outputpipe |
| 72.71 | 100.00 | | 66.28 | 51.85 | fp_multiplication_input_pipe2 |
| 74.27 | 77.78 | 47.62 | 97.41 | | fp_multiplication_round_normalized |
| 74.82 | 100.00 | | 72.60 | 51.85 | fp_multiplication_input_pipe1 |
| 75.34 | 100.00 | | 50.68 | | mux |
| 76.14 | 77.78 | 52.38 | 98.28 | | multiplication_rounding_verification |
| 76.49 | 71.98 | 64.18 | 93.30 | | fp_addition |
| 79.41 | 94.55 | 50.00 | 93.67 | | fpalu_fixture |
| 79.59 | 96.91 | | 90.00 | 51.85 | fsm_multiplication |
| 83.71 | 89.63 | 68.06 | 93.45 | | addition_verification |
| 87.25 | 100.00 | | 74.51 | | dffa |
| 87.58 | 100.00 | 66.67 | 96.06 | | multiplication_verification |
| 87.58 | 100.00 | 66.67 | 96.06 | | fp_multiplication_prenormalization |
| 97.05 | 100.00 | | 94.11 | | multiplication |
| 98.88 | | | 98.88 | | fpalu |
| 99.06 | 100.00 | | 98.11 | | dffb |
| 99.35 | 100.00 | | 98.70 | | finalshift |
| 99.50 | | | 99.50 | | fp_multiplication |
| 100.00 | | | 100.00 | | adder |