# Verification of AXI4 Lite Bus Protocol

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Introduction

- The AXI4-Lite (Advanced eXtensible Interface 4 Lite) bus protocol is a simplified, high-performance memory-mapped interface within the ARM Advanced Microcontroller Bus Architecture (AMBA) specification.
- For this project, we have opted for a configuration with a sole master and a singular slave.
- There are five channels, specifically the Read Address Channel, Read Data Channel, Write Address Channel, Write Data Channel, and Write Response Channel.

AXI4 Lite Architecture
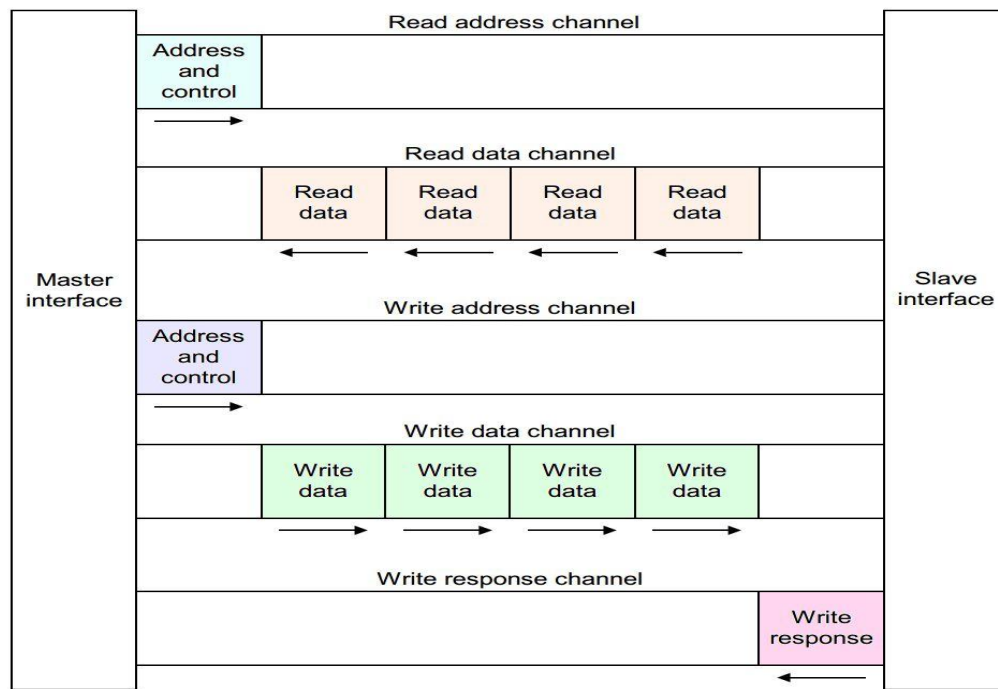
The key functionality of AXI4-Lite operation is:

- All transactions are of burst length 1
- All data accesses use the full width of the data bus
- All accesses are Non-modifiable, Non-bufferable
- Exclusive accesses are not supported
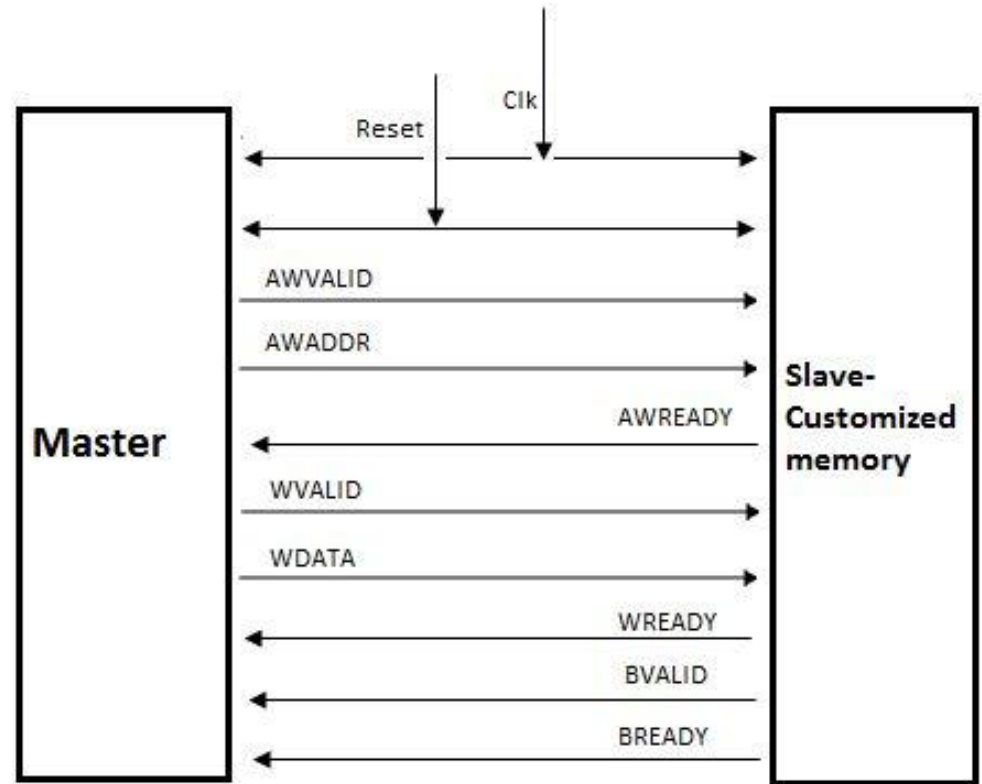
Read & Write Operations

Read Operation:

1. Master sends address; ARVALID goes high.
2. Slave acknowledges with ARREADY.
3. Handshake on rising clock edge; deassert ARVALID and ARREADY.
4. Slave puts data on bus; RVALID goes high.
5. Master accepts data with RREADY.
6. Transaction completes on next rising clock edge; deassert RREADY and RVALID.

Write Operation:

1. Master sends address; AWVALID goes high.
2. Slave acknowledges with AWREADY.
3. Handshake on Write Address and Write Data channels; deassert Valid and Ready.
4. Master sends data; WVALID goes high.
5. Slave accepts data with WREADY.
6. Slave asserts BVALID for a valid response on Write Response channel.
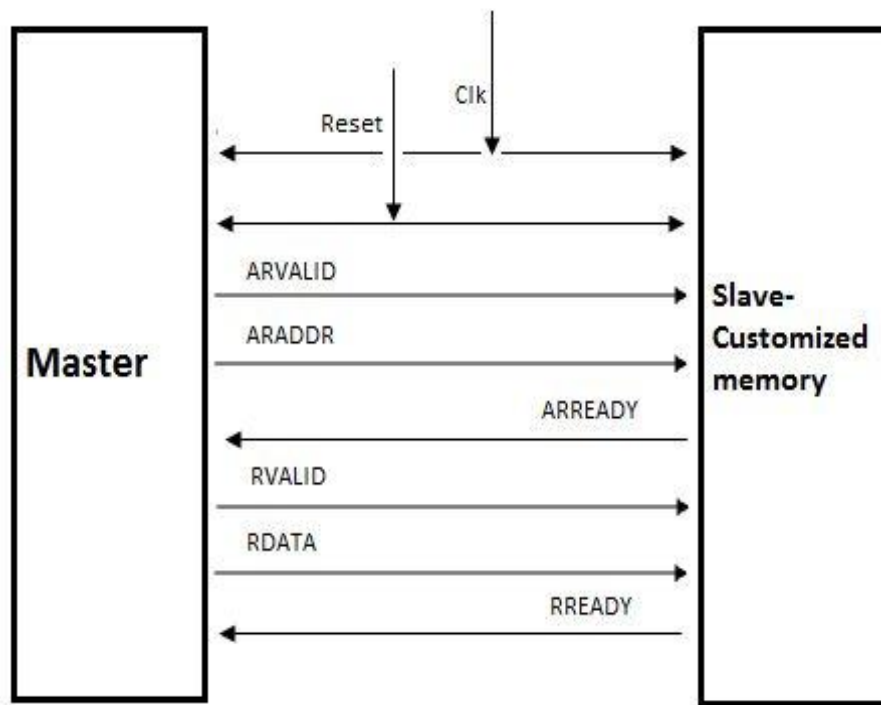
AXI4-Lite architecture during read operation

AXI4-Lite architecture during write operation

Verification Plan

Our goal here is to verify basic read/write operations between the master and slave occur as expected in the given design using FPV.

Assumptions:

- Read and write address should not be unknown
- AWADDR and WDATA are 32 - bit values
- Data provided as input should not be an unknown value
- Wr_en and rd_en cannot be high at the same time

Verification Plan

Assertions for AXI lite Read Address & Read Data Channels:

- When ARVALID is true and ARREADY is low, ARADDR will remain stable. (Similar assertion is written to verify the Read Data Channel)
- When ARVALID is high it must remain high until ARREADY is asserted. (Similar assertion is written to verify the Read Data Channel)
- ARREADY cannot be indefinitely low while ARVALID is true (Similar assertion is written to verify the Read Data Channel)
- When reset is asserted ARREADY and ARVALID cannot be unknown
- For every request ARVALID and ARREADY there must follow one clock period sometime later where RVALID and RREADY is true

Verification Plan

Assertions for AXI lite Write Address & Write Data Channels:

- When AWVALID is true and AWREADY is low, AWADDR will remain stable. (Similar assertion is written to verify the WriteData Channel)
- When AWVALID is high it must remain high until AWREADY is asserted. (Similar assertion is written to verify the Write Data Channel)
- AWREADY cannot be indefinitely low while AWVALID is true (Similar assertion is written to verify the Write Data Channel)
- When reset is asserted AWREADY and AWVALID cannot be unknown
- AWVALID is low for the first cycle after reset is asserted (Similar assertion is written to verify the Write Data Channel)

Verification Plan

Assertions for AXI lite Write Response Channel:

- When BVALID is asserted, it must remain asserted until BREADY is HIGH
- When reset is not asserted BVALID and BREADY cannot be unknown
- BVALID is LOW for the first cycle after Reset is asserted
- When AWREADY and WREADY are false, BREADY will also be low
- BREADY cannot be indefinitely low while BVALID is true

AXI4 Lite Read Transaction
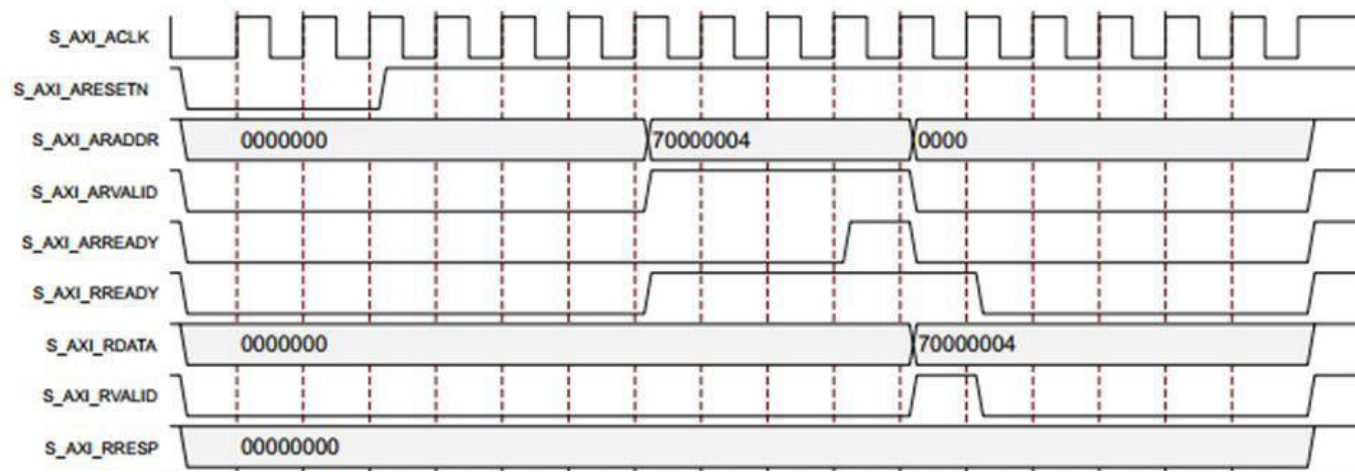
AXI4 Lite Write Transaction
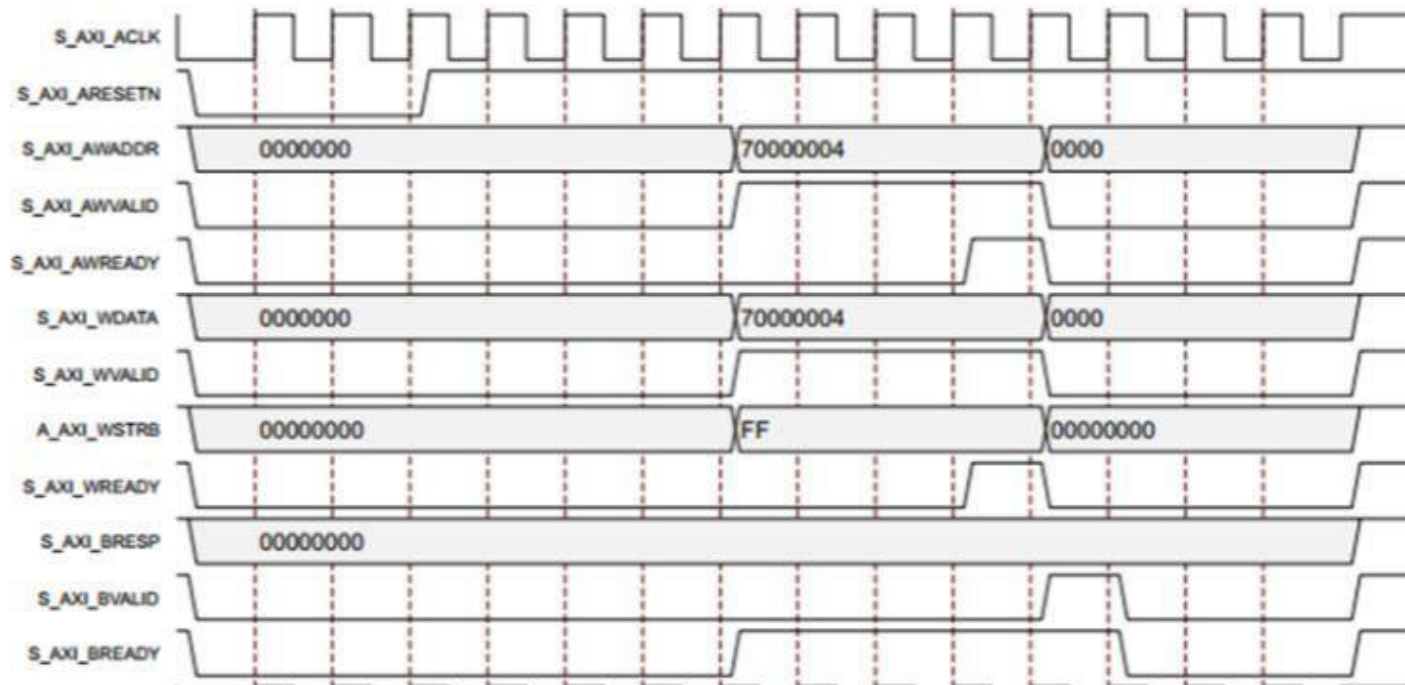
Bugs Found

The following Assertions have failed during simulation

- ARADDR Remains Stable when ARVALID is asserted and ARREADY is low
- RDATA Remains Stable when RVALID is asserted and RREADY is low
- AWADDR Remains Stable when AWVALID is asserted and AWREADY is low
- WDATA Remains Stable when WVALID is asserted and WREADY is low

Thank You