



EFR32xG22 QFN40 Radio Board

2.4 GHz 6 dBm


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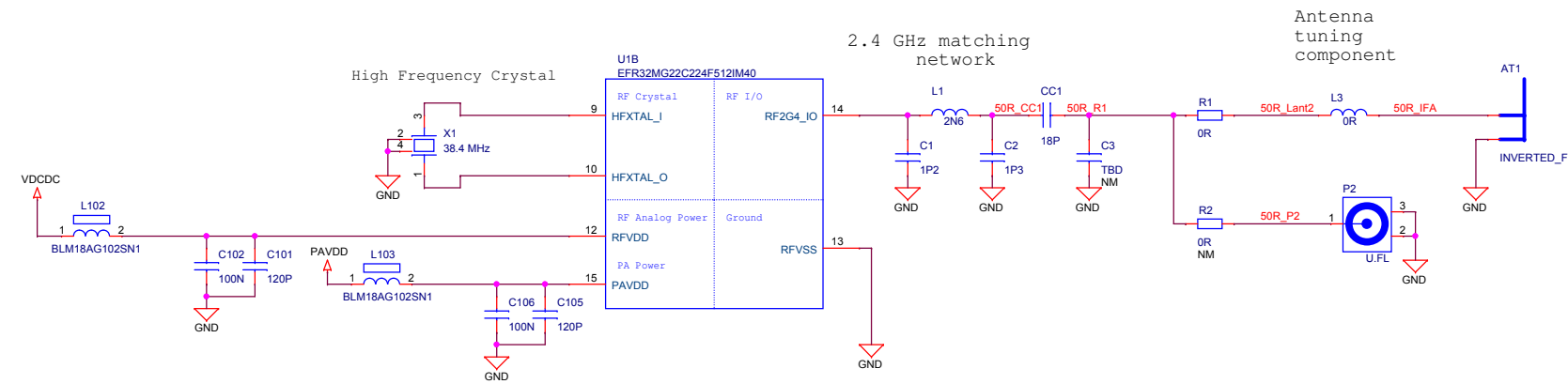
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Revision History

Rev.	Description
A00	Initial production release.
A01	Mounted U1. Updated C1, C2 P/N.
A02	Matching layout improvement at C1 GND pad.
B00	X3-->X1. Updated U1, X1 P/N, matching and USART markings. PCB siksreen fix.
B01	Updated matching network.
B02	Updated matching network.
B03	Updated U1 P/N. Fixed X2 P/N.
B04	Removed optional/not mounted components. Fixed L101 P/N.
B05	New P/N for X2.
B06	Updated P200, P201, P2, U200 OPNs.

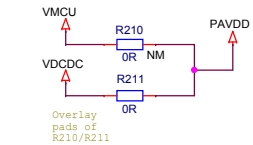
 SILICON LABS		Board Name EFR32xG22 QFN40 2.4 GHz 6 dBm Radio Board	
		Page Title Title Page	
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Size A3	Sheet Modified Date Friday, April 09, 2021	Board Number BRD4182A	Revision B06
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Antenna & Radio Interface

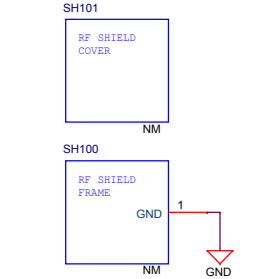


PAVDD Configuration

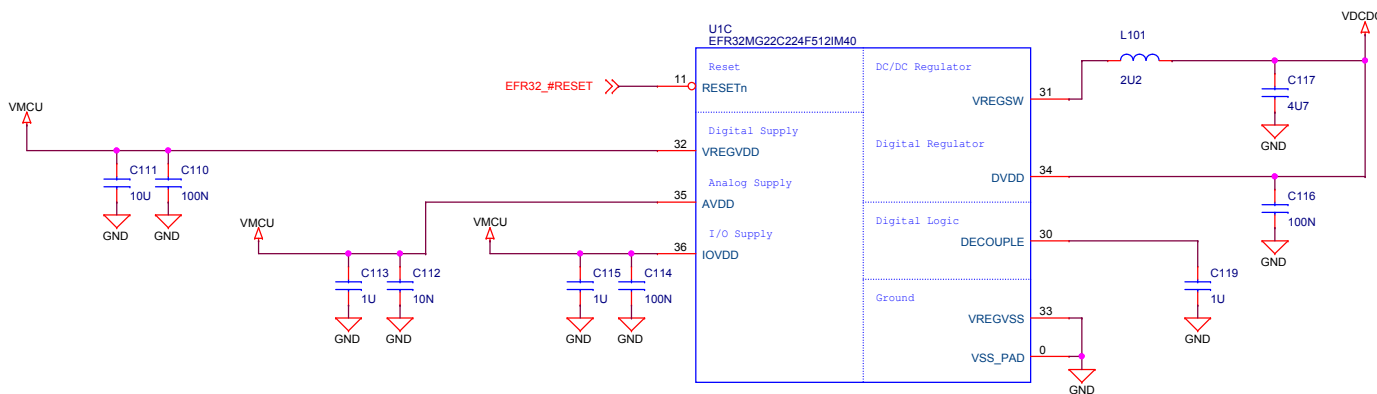
	Power Config 1 VMCU to PAVDD	Power Config 2 DCDC to PAVDD
R210	Mount	Not mount
R211	Not mount	Mount




RF Shielding



Power & Decoupling





SILICON LABS

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EFR32xG22 QFN40 2.4 GHz 6 dBm Radio Board

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RF, Antenna and Power

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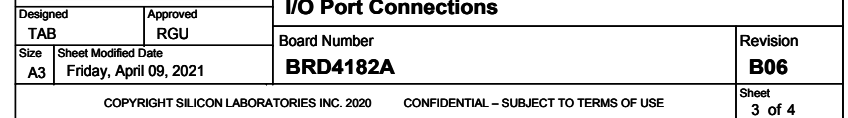
The diagram illustrates the pin connections for the EFR32 PA0[8..0] pin, showing connections to various peripherals and WSTK pins. The connections are organized into several sections:

- EFR32 PA0[8..0] Section:** Shows connections for EFR32 pins (PA00 to PA08) to WSTK pins (P14 to P21) and various peripherals (DBG_SWCLK, DBG_SWDIOTMS, DBG_SWO/DBG_TDO, DEBUG_TRACED0, DEBUG_TRACECLK/DBG_TDI, US1_TX, US1_RX, US1_RTS, US1_CTS). It also shows connections to WSTK pins (P14 to P21) and various peripherals (DISP_EXTCOMIN, DISP_TCK_SWCLK, DISP_TMS_SWCLK, DISP_TDO_SWO, WSTK_F18, WSTK_F1, WSTK_F0, WSTK_F2, TP_TCK_SWCLK, TP_TMS_SWCLK, TP_TDO_SWO, WSTK_F3, TP_TDI, VCOM_TX, VCOM_RX, VCOM_RTS, VCOM_CTS, WSTK_F6, WSTK_F7, WSTK_F8, TP_VCOM_TX, TP_VCOM_RX, TP_VCOM_RTS, TP_VCOM_CTS).
- EFR32 PB0[4..0] Section:** Shows connections for EFR32 pins (PB00 to PB04) to WSTK pins (P4 to P15) and various peripherals (EXP_HEADER7, EXP_HEADER9, EXP_HEADER15, EXP_HEADER16, I2C0_SCL, I2C0_SDA). It also shows connections to WSTK pins (P4 to P15) and various peripherals (UIF_BUTTON0, UIF_BUTTON1, VCOM_ENABLE, WSTK_F12, WSTK_F13, WSTK_F5).
- EFR32 PC0[7..0] Section:** Shows connections for EFR32 pins (PC00 to PC07) to WSTK pins (P1 to P31) and various peripherals (US0_TX, US0_RX, US0_CLK, FLASH_MOSI, FLASH_MISO, FLASH_SCLK, EXP_HEADER4, EXP_HEADER6, EXP_HEADER3, EXP_HEADER8, EXP_HEADER10, EXP_HEADERS, R216, R217, R204, R205, R206, R207, R208, VMCU, SENSOR_ENABLE, WSTK_P37). It also shows connections to WSTK pins (P1 to P31) and various peripherals (DISP_MOSI, DISP_SCL, DISP_EXTCOMIN, DISP_TCK_SWCLK, DISP_TMS_SWCLK, DISP_TDO_SWO, WSTK_F16, WSTK_F15, WSTK_F20, WSTK_F19, WSTK_F17, WSTK_F14, PTL_DATA, PTL_SYNC, DISP_SCS, DISP_ENABLE).
- EFR32 PD0[3..0] Section:** Shows connections for EFR32 pins (PD00 to PD03) to WSTK pins (P8 to P10) and various peripherals (LFXTAL_O, LFXTAL_I, X2 32.768 kHz, EXP_HEADER11, EXP_HEADER13). It also shows connections to WSTK pins (P8 to P10) and various peripherals (UIF_LED0, UIF_LED1, WSTK_F10, WSTK_F11).
- Reset Section:** Shows connections for EFR32_RESET to WSTK_F4 and TP_RESET.

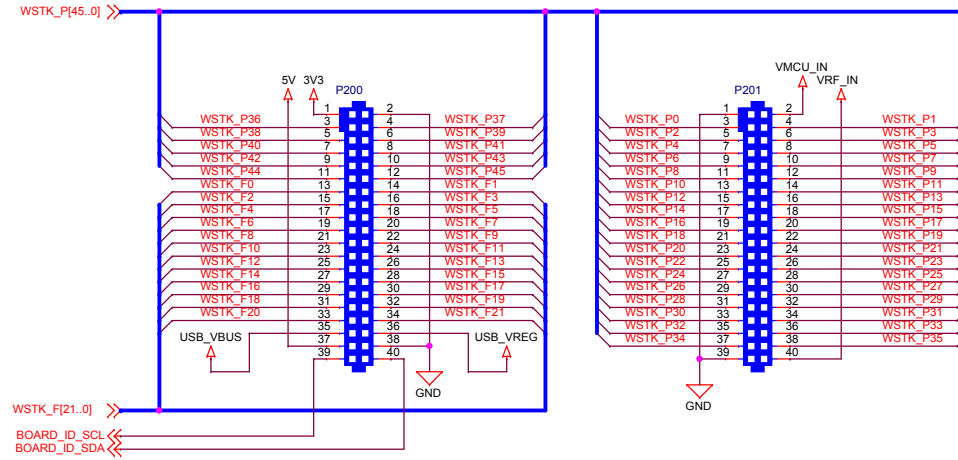
Left Pin Group	Right Pin Group
EFR32_PA0[8..0]	PA00
	PA01
	PA02
	PA03
	PA04
	PA05
	PA06
	PA07
	PA08
EFR32_PB0[4..0]	PB00
	PB01
	PB02
	PB03
	PB04
EFR32_PC0[7..0]	PC00
	PC01
	PC02
	PC03
	PC04
	PC05
	PC06
	PC07
EFR32_PD0[3..0]	PD00
	PD01
	PD02
	PD03

The schematic diagram shows the connection of two MX25R8035F SPI flash memory chips, U100A and U100B, to a VMCU and GND. U100A is connected to the VMCU and GND. U100B is connected to the VMCU and GND. The circuit includes a 330K resistor (R103) and a 100N capacitor (C124). The connections are as follows:

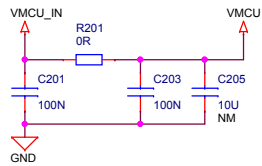
- U100A: D2 to VMCU, E1 to VMCU, A3 to VMCU, E3 to VMCU, C1 to VMCU, C3 to FLASH_MISO, WP# / SI02 to VMCU, RESET# / SI03 to VMCU, SI / SI00 to VMCU, SO / SI01 to VMCU, CS# to VMCU.
- U100B: VCC to VMCU, A1 to VMCU, B2 to GND.
- R103 (330K) is connected between VMCU and GND.
- C124 (100N) is connected between VMCU and GND.
- FLASH_MOSI, FLASH_SCLK, and FLASH_SCS are connected to the VMCU.



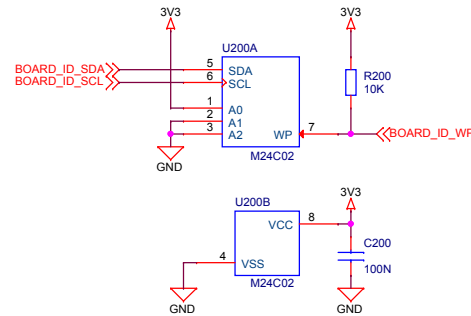
WSTK Connectors



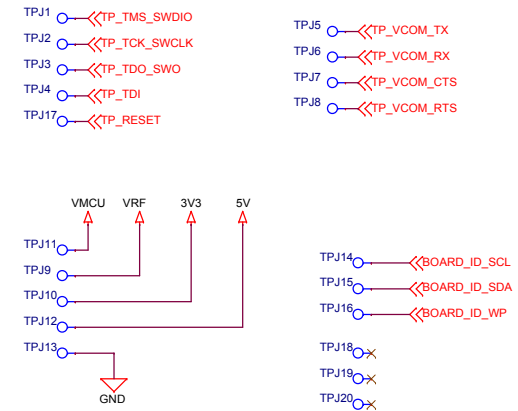
WSTK Power Decoupling




Board Identification



Test Points



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