



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB -2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=19$ and $B=25$ using GNUSim.	25	1	3
2	Explain the concept of Read-Only Memory (ROM) in computer systems, elaborating on its characteristics, applications, and importance in modern computing. Write C program to illustrate the ROM and discussing its fundamental purpose in storing permanent or semi-permanent data and instructions that are essential for system operation.	25	4	3
3	Draw the Half Adder circuit and verify the truth table using Logisim software	25	2	3
4	Provide a C Program including how the product register is updated during each iteration. Illustrate the application of Booth multiplication specifically for the multiplication of 12 and 14, showing the intermediate results at each stage.	25	2	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB-2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=19$ and $B=25$ using GNUSim.	25	1	3
2	Discuss the concept of Random Access Memory (RAM) in computer systems, elaborating on its role, architecture, and significance in modern computing. Write C program to illustrate the RAM and explaining its fundamental function in providing temporary storage for data and program instructions during active use.	25	4	3
3	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
4	Pipelining is the process of storing and prioritizing computer instructions that the processor executes . Two stage pipelining includes the steps Fetch and Execute. Using 2 stage pipeline concept, identify the clock cycles needed to perform the addition of two numbers say 8 and 10 using any high level language.	25	3	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=29$ and $B=35$ using GNUSim.	25	1	3
2	Explain the concept of memory allocation in computer systems, outlining its significance in managing and optimizing memory usage. Write C program to illustrate the memory allocation and discussing its role in dynamically assigning memory resources to programs and data structures during program execution.	25	4	3
3	Draw the Half Adder circuit and verify the truth table using Logisim software	25	2	3
4	Get the decimal input 2810 from the user. This is to be converted to Hexa decimal number. Write a program to convert Decimal number to Hexadecimal number using any high level language.	25	2	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB-2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=53$ and $B=32$ using GNUSim.	25	2	3
2	Discuss the concept of CPU performance in computer systems, detailing the factors that influence it and the methods used to measure and evaluate it. Write C program to illustrate the CPU performance and explaining its importance in determining the overall efficiency and responsiveness of a computing device. Describe the key metrics used to assess CPU performance, such as clock speed, instruction throughput, and execution time.	25	1	3
3	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
4	Pipelining is the process of storing and prioritizing computer instructions that the processor executes. Two stage pipelining includes the steps Fetch and Execute. Using 2 stage pipeline concept, identify the clock cycles needed to perform the addition of two numbers say 8 and 10 using any high level language.	25	3	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB-2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for subtraction of two 8-bit data A7 A6 A5 A4 A3 A2 A1 A0 and B7 B6 B5 B4 B3 B2 B1 B0 using 8085 processor for A=48 and B=12 using GNUSim.	25	2	3
2	Describe the organization of a computer system where a set of general-purpose registers, program counters, instruction registers, memory address registers (MAR), and memory data registers (MDR) are interconnected via a multiple bus. Write C program to illustrate the role of each component in the system, highlighting their functions in executing instructions and managing data.	25	1	3
3	A software has simple toolbar to simulate the circuit design is Logisim. Identify the logic gates for the implementation of full adder of your choice. There are 3 inputs A,B and C with Sum and Carry as the output. The result should be tested with the Full adder Truth table. .	25	2	3
4	When the processing happens in an overlapped manner or introducing parallel execution is called as Pipelining. ARM devices need pipelining because of RISC and emphasizes the compiler complexity. Consider each stage in pipelining is equivalent to 1 cycle, that is n stages = n cycles. Consider here n=3 because it performs Fetch, Decode and Execute. Implement the design of 3 stage pipeline and calculate the total clock cycles needed to complete 1 instruction using any high-level language.	25	3	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=19$ and $B=25$ using GNUSim.	25	2	3
2	Describe the organization of a computer system where a set of general-purpose registers, program counters, instruction registers, memory address registers (MAR), and memory data registers (MDR) are interconnected via a single bus. Write C program to illustrate the role of each component in the system, highlighting their functions in executing instructions and managing data.	25	1	3
3	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
4	Develop a C program that explores potential data hazards or race conditions, instruction hazards, and structure hazards.	3	3	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB-2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 8-bit data $A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$ and $B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0$ using 8085 processor for $A=29$ and $B=35$ using GNUSim.	25	1	3
2	Explain the concept of register transfer language (RTL) as a symbolic notation for describing micro-operation transfers between registers in a computer system. Discuss how RTL facilitates the representation of low-level operations within a processor's architecture. Write C program to enhance the significance of hardware logic circuits capable of executing specified micro-operations and transferring the results between registers, which is referred to as register transfer.	25	2	3
3	Draw the Half Adder circuit and verify the truth table using Logisim software	25	2	3
4	<p>Consider a simple cache memory simulation program written in C. The program simulates a direct-mapped cache with a given cache size and main memory size. The cache is represented by an array of cache blocks, where each block consists of a valid bit, tag bits, and data. The main memory is represented by an array.</p> <p>Program Description:</p> <p>The provided C program simulates cache memory access with the following features:</p> <p style="padding-left: 40px;">Cache memory size: 256 bytes</p> <p style="padding-left: 40px;">Main memory size: 1024 bytes</p> <p>Cache structure: Each cache block contains a valid bit, tag bits, and data.</p> <p>Cache access function: Simulates cache access by checking for cache hits or misses and loading data from main memory to cache if needed.</p>	25	3	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES

MODEL EXAM FEB-2024



CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 16-bit data 45 and 12 using 8086 processor implementing by GNUSim.	25	2	3
2	Discuss how dynamic prediction predicts the outcome of a branch solely based on the branch instruction itself, considering past runtime behaviour. Write a C Program to ensure the potential enhancements or adaptations to static prediction techniques to improve their accuracy or applicability in modern computing environments.	25	3	3
3	Logisim is a tool to design the logic gates for Full Subtractor and implement the same using simulator.	25	2	3
4	Design a C program to simulate a device controller that manages the on/off state of a device based on user requests. The program should provide the following functionalities: i). Define a global variable deviceStatus to represent the current state of the device (for turning the device ON, 2 for turning it OFF, and 0 to exit). ii). Implement a function handleDeviceRequest that takes an integer argument request representing user input.	25	5	4



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	The user is giving 110011012 as input and they are in a need of its equivalent in Octal format. Write a program to perform this conversion using any high level language.	25	2	4
2	A software has simple toolbar to simulate the circuit design is Logisim. Identify the logic gates for the implementation of full adder of your choice. There are 3 inputs A,B and C with Sum and Carry as the output. The result should be tested with the Full adder Truth table. .	25	2	3
3	Discuss how static prediction predicts the outcome of a branch solely based on the branch instruction itself, without considering past runtime behavior. Write a C Program to ensure the potential enhancements or adaptations to static prediction techniques to improve their accuracy or applicability in modern computing environments.	25	3	3
4	Design a C program to simulate bus arbitration using the round-robin algorithm. Implement a function called bus_arbitration_round_robin that takes an array of devices requesting access to the bus and determines the order in which they are granted access based on the round-robin scheduling policy. Each device is represented by a unique identifier, and the array contains the IDs of devices requesting access to the bus. The function should return the order in which the devices are granted access to the bus. Test the function with different input scenarios, including cases with varying numbers of devices and requests, and analyze the fairness and efficiency of the round-robin arbitration algorithm in managing bus access.	25	5	4



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE FOR VON -NEUMANN ARCHITECTURE
--------------	--

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Using GNUsim, write an assembly language program for multiplying two 16-bit data 32 and 5 using 8085 processor.	25	2	3
2	A block-set Associate Cache memory consists of lag blocks divided into four blocksets. The main memory Consists of 161384 blocks & each block contains 256 eight-bit words. Write a C Program to find how many bits are required for addressing - the main memory?	25	3	3
3	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
4	Pipelining is the process of storing and prioritizing computer instructions that the processor executes . Two stage pipelining includes the steps Fetch and Execute. Using 2 stage pipeline concept, identify the clock cycles needed to perform the addition of two numbers say 8 and 10 using any high-level language.	25	3	4



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE FOR VON- NEUMANN ARCHITECTURE
--------------	--

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Get the decimal input 2810 from the user. This is to be converted to Binary, Octal and Hexa decimal number. Write a program to convert Decimal number to Hexadecimal number using any high-level language.	25	2	4
2	A computer with virtual menory has an access time to Main memory 50ns, the time to transfer a block from the virtual into main memory is 10ns, the probability for the page fault is 10^{-6} . Write a C Program to find the average access Time if the page table is in the main memory.	25	3	3
3	Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. Now, identify the logic gates needed to implement half adder and draw the circuit diagram using Logisim simulator. Finally test your design using the truth table.	25	2	3
4	Develop a C program to access two I/O devices using interrupts, utilizing only the SIGINT signal and the SIG_DFL action to handle interrupts. Implement interrupt service routines (device1_isr and device2_isr) to process interrupts generated by the devices. Inside the main loop, continuously check for data received from the devices and display the received data. After processing data from each device, reset the signal handler for SIGINT to its default behavior using SIG_DFL. Test the program with simulated data transmission scenarios and analyze the effectiveness of using signal handlers for interrupt-driven I/O communication.			



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write a C Program including how the product register is updated during each iteration. Illustrate the application of Booth multiplication specifically for the multiplication of 11 and 13, showing the intermediate results at each stage.	25	2	3
2	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
3	Develop a C program that explores potential data hazards or race conditions, instruction hazards, and structure hazards.	25	3	3
4	Pipelining is the process of storing and prioritizing computer instructions that the processor executes . Two stage pipelining includes the steps Fetch and Execute. Using 2 stage pipeline concept, identify the clock cycles needed to perform the addition of two numbers say 8 and 10 using any high level language.	25	3	4



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Using GNUSim, write an assembly language program for multiplication of two 8-bit data A7 A6 A5 A4 A3 A2 A1 A0 and B7 B6 B5 B4 B3 B2 B1 B0 using 8085 processor for 14 and 22.	25	1	3
2	Write a C Program of each step, illustrating how the registers are updated throughout the process of 8/3. Finally, present the final quotient obtained from the non - restoring division and discuss any potential limitations or challenges encountered during the computation."	25	2	3
3	A software has simple toolbar to simulate the circuit design is Logisim. Identify the logic gates for the implementation of full adder of your choice. There are 3 inputs A, B and C with Sum and Carry as the output. The result should be tested with the Full adder Truth table. .	25	2	3
4	Develop a C program to simulate Random Access Memory (RAM) operations. The goal is to implement functionalities that involve memory allocation, access, and manipulation.	25	4	3



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write a C Program of each step, illustrating how the registers are updated throughout the process of $11/3$. Finally, present the final quotient obtained from the restoring division and discuss any potential limitations or challenges encountered during the computation."	25	2	3
2	Using GNUsim, write an assembly language program for multiplying two 16-bit data 15 and 9 using 8085 processor.	25	2	3
3	Logisim is a tool to design the logic gates for Full adder and implement the Full adder using only NAND gates using simulator.	25	2	3
4	Develop a C program to simulate PCI interrupts. The objective is to create a simulation where a PCI device triggers interrupts that are handled by the CPU	25	5	3



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Explain the process of performing multiplication and division of two fractional (floating) numbers. Provide the C program by outlining the steps involved in aligning the numbers, handling the exponent, and performing the arithmetic operation on the mantissa	25	2	3
2	Discuss the concept of CPU performance in computer systems, detailing the factors that influence it and the methods used to measure and evaluate it. Write C program to illustrate the CPU performance and explaining its importance in determining the overall efficiency and responsiveness of a computing device. Describe the key metrics used to assess CPU performance, such as clock speed, instruction throughput, and execution time.	25	1	3
3	Draw the Full subtractor circuit and verify the truth table using Logisim software	25	2	3
4	Design a C program to simulate a device controller that manages the on/off state of a device based on user requests. The program should provide the following functionalities: i). Define a global variable deviceStatus to represent the current state of the device (for turning the device ON, 2 for turning it OFF, and 0 to exit). ii). Implement a function handleDeviceRequest that takes an integer argument request representing user input.	25	5	4



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Write an assembly language program for adding two 16-bit data 65 and 72 using 8086 processor implementing by GNUSim.	25	2	3
2	Explain the process of performing addition and subtraction of two floating point numbers. Write the C program by outlining the steps involved in aligning the numbers, handling the exponent, and performing the arithmetic operation on the mantissa	25	2	3
3	Using Logisim software, design digital circuits to implement both a Half Subtractor and a Full Subtractor.	25	2	3
4	Develop a C program to simulate accessing I/O devices. The objective is to create a simulation where the program interacts with I/O devices, such as sensors, actuators, or any other simulated devices.	25	5	2



SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Explain the process of performing multiplication and division of two integer numbers. Provide the C program by outlining the steps involved in aligning the numbers, handling the exponent, and performing the arithmetic operation on the mantissa	25	2	3
2	Using GNUsim, write an assembly language program for division of two 8-bit data A7 A6 A5 A4 A3 A2 A1 A0 and B7 B6 B5 B4 B3 B2 B1 B0 using 8085 processor for 9 by 2.	25	1	3
3	Logisim is a tool to design the logic gates for Full and half Adder and implement the same using simulator.	25	2	3
4	Develop a C program to simulate Read-Only Memory (ROM) operations. The goal is to create a simulation where the program emulates the behavior of a ROM, allowing users to read data stored in the memory.	25	4	2



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Explain the process of performing addition and subtraction of two integer numbers. Provide the C program by outlining the steps involved in aligning the numbers, handling the exponent, and performing the arithmetic operation on the mantissa	25	2	3
2	Using GNUsim, write an assembly language program for division of two 8-bit data A7 A6 A5 A4 A3 A2 A1 A0 and B7 B6 B5 B4 B3 B2 B1 B0 using 8085 processor for 9 by 2.	25	1	3
3	Logisim is a tool to design the logic gates for Full subtractor and implement the same using simulator.	25	2	3
4	Develop a C program to simulate Virtual Memory operations. The objective is to create a simulation where the program emulates the behavior of a virtual memory system, including address translation, page faults, and paging strategies	25	3	3



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Describe the process of representing the decimal number 1259.125 in double precision floating-point format. Include the steps involved, such as converting the number to binary, determining the sign, exponent, and mantissa, and finally encoding these components according to IEEE 754 standard. Provide the C program for binary representation of each component and explain how they combine to represent the given decimal number accurately.	25	1	3
2	Utilizing GNU Software to perform 16-bit addition and subtraction operations.	25	1	3
3	Logisim is a tool to design the logic gates for half subtractor and implement the same using simulator.	25	2	3
4	Develop a C program to simulate PCI interrupts. The objective is to create a simulation where a PCI device triggers interrupts that are handled by the CPU.	25	5	3



**SAVEETHA SCHOOL OF ENGINEERING
SAVEETHA INSTITUTE OF MEDICAL AND TECHNICAL
SCIENCES**



MODEL EXAM FEB-2024

CSA12	COMPUTER ARCHITECTURE
--------------	------------------------------

	ANSWER ALL THE QUESTIONS	Marks	CO	BTL
1	Describe the process of representing the decimal number 1259.125 in single precision floating-point format. Include the steps involved, such as converting the number to binary, determining the sign, exponent, and mantissa, and finally encoding these components according to IEEE 754 standard. Provide the C program for binary representation of each component and explain how they combine to represent the given decimal number accurately	25	1	3
2	Utilizing GNU Software to perform 16-bit addition and subtraction operations.	25		3
3	Logisim is a tool to design the logic gates for half subtractor and implement the same using simulator.	25	2	3
4	The performance of the CPU is basically depends on response time, throughput and execution time of a computer system. Write a program to find the CPU performance of a processor using any high level language.	25	3	2